TEXAS INSTRUMENTS
TPS54JA20
JAJSKP4C – MARCH 2020 – REVISED JULY 2021

TPS54JA20 2.7V～16V 入力、12A 同期整流式降圧コンバータ、リモート・センス機能、3V LDO、ラッチ・オフ電流制限機能搭載

1 特長

- 入力範囲:4V～16V、最大 12A 、外部バイアスなし
- 入力範囲:2.7V～16V、最大 12A 、外部バイアス・レンジ 3.13V～5.3V
- 出力電圧範囲:0.9V ～5.5V
- 10.2mΩ と 3.1mΩ の内蔵 MOSFET
- D-CAP3™ による超高速負荷ステップ応答
- すべての出力コンデンサでセラミック・コンデンサの使用をサポート
- 差動リモート・センス、V_{REF} = 0.9V ±1% (–40℃～+125℃の接合部温度)
- 自動スキップ Eco-mode™ により軽負荷時の効率を向上
- 電流制限を R_{TRIP} でプログラム可能
- スイッチング周波数をピンで選択可能:600kHz、800kHz、1MHz
- ソフトスタート時間をプログラム可能
- トラッキング用の外部リファレンス入力
- プリバイアス付きスタートアップ機能
- オープン・ドレインのパワー・グッド出力
- OC、UV、OV フォルトのラッチオフ
- 4mm × 3mm、21 ピンの QFN パッケージ
- 15A *TPS548A28*/*TPS548A29* とピン互換
- RoHS に完全準拠 (適用除外なし)

2 アプリケーション

- ラック・サーバーおよびブレード・サーバー
- ハードウェア・アクセラレータおよびアドイン・カード
- データ・センター向けスイッチ
- 産業用 PC

3 概要

TPS54JA20 デバイスは、適応型オン時間 D-CAP3 制御モードを備えた小型で高効率の同期整流式降圧コンバータです。外部補償が不要のため、本デバイスは使いやすく、外付け部品をほとんど必要としません。本デバイスは、スペースに制約のあるデータ・センター・アプリケーションによく適しています。

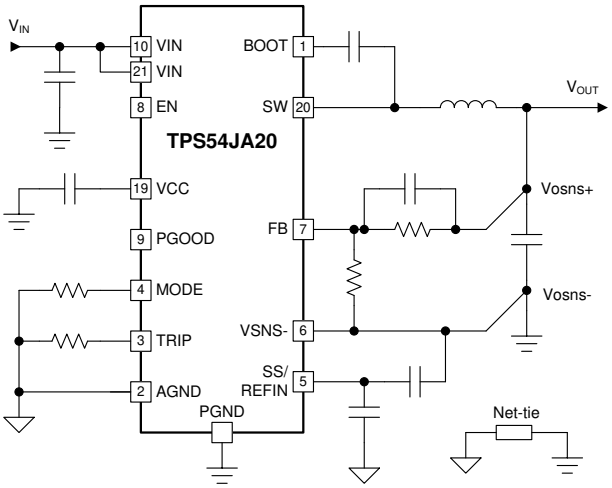
TPS54JA20 デバイスは、差動リモート・センス、高性能の内蔵 MOSFET、動作時接合部温度の全範囲にわたって高精度 (±1%) の 0.9V 基準電圧を備えています。本デバイスは、高速な負荷過渡応答、精密な負荷レギュレーションとライン・レギュレーション、スキップ・モードまたは FCCM 動作、プログラム可能なソフトスタートを特長としています。

TPS54JA20 デバイスは、鉛フリーのデバイスです。RoHS に完全準拠しています (適用除外なし)。

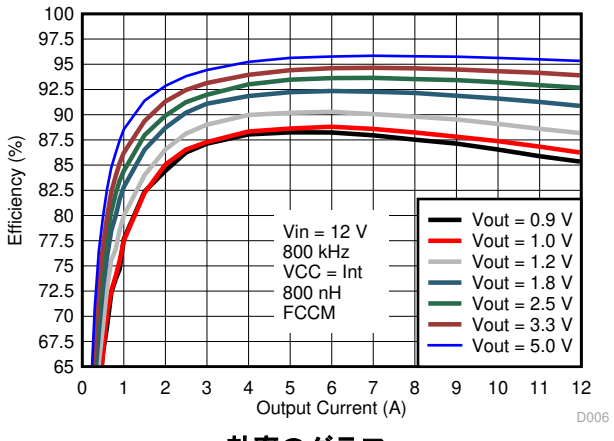
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS54JA20	VQFN-HR (21)	4.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



効率のグラフ

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2020) to Revision C (July 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「アプリケーション」にリンクを追加	1
• VIN-SW: Transient changed from 10ns to 20ns, Changed Min from -1.5V to -4V	5
• VIN-PGND: Transient changed from 10ns to 20ns	5
• Updated Switching Frequency minimum and maximum values	6
• Fixed cross references for 式 10 through 式 17 and corrected equation errors	27
• Added R_{TRIP} value to paragraph	27
• Updated typical valley current in the text from 12.8 A to 10.66 A to match 式 14	27
• Added "Round up to use a valley current limit of 15 A."	27
• Updated Switching Frequency vs Output Voltage graph	32

Changes from Revision A (June 2020) to Revision B (June 2020)	Page
• Deleted redundant LDO specification	6

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5 Pin Configuration and Functions

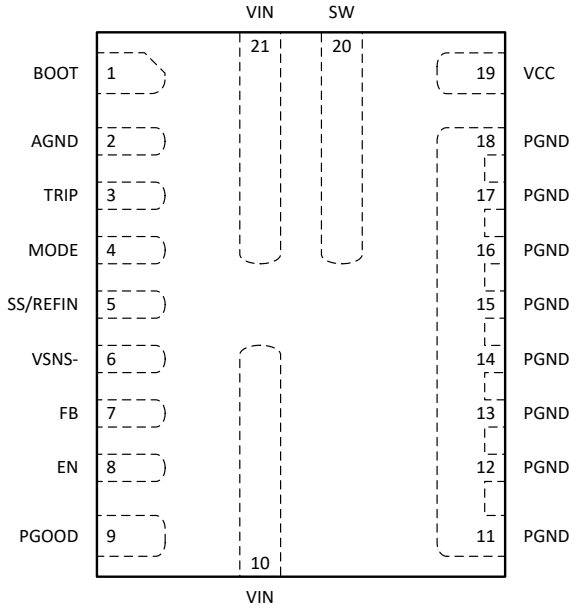


図 5-1. RWW Package 21-Pin VQFN-HR Top View

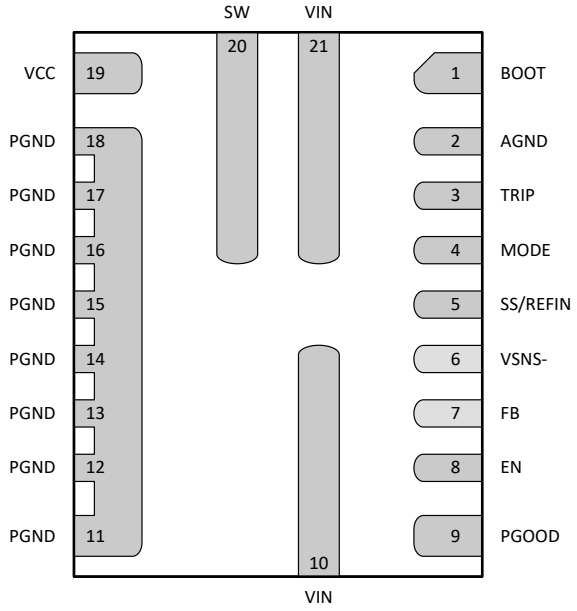


図 5-2. RWW Package 21-Pin VQFN-HR Bottom View

表 5-1. Pin Functions

NO.	NAME	I/O(1)	DESCRIPTION
1	BOOT	I/O	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to SW node.
2	AGND	G	Ground pin, reference point for the internal control circuits
3	TRIP	I/O	Current limit setting pin. Connect a resistor to AGND to set the current limit trip point. A ±1% tolerance resistor is highly recommended. See *セクション 7.3.9* for details on OCL setting.
4	MODE	I	The MODE pin sets the forced continuous-conduction mode (FCCM) or Skip-mode operation. It also selects the operating frequency by connecting a resistor from the MODE pin to the AGND pin. ±1% tolerance resistor is recommended. See 表 7-1 for details.
5	SS/REFIN	I/O	Dual-function pin. Soft-start function: Connecting a capacitor to VSNS– pin programs soft-start time. Minimum soft-start time (1.5 ms) is fixed internally. A minimum 1-nF capacitor is required for this pin to avoid overshoot during the charge of soft-start capacitor. REFIN function: The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. The internal reference voltage can be overridden by an external DC voltage source on this pin for tracking application.
6	VSNS–	I	The return connection for a remote voltage sensing configuration. It is also used as ground for the internal reference. Short to AGND for single-end sense configuration.
7	FB	I	Output voltage feedback input. A resistor divider from the V_{OUT} to VSNS– (tapped to FB pin) sets the output voltage.
8	EN	I	Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating EN pin before start-up disables the converter. The recommended operating condition for EN pin is maximum 5.5 V. *Do not* connect EN pin to VIN pin directly.
9	PGOOD	O	Open-drain power-good status signal. When the FB voltage moves outside the specified limits, PGOOD goes low after 2-µs delay.

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表 5-1. Pin Functions (continued)

NO.	NAME	I/O(1)	DESCRIPTION
10, 21	VIN	P	Power-supply input pins for both integrated power MOSFET pair and the internal LDO. Place the decoupling input capacitors from VIN pins to PGND pins as close as possible.
11, 12, 13, 14, 15, 16, 17, 18	PGND	G	Power ground of internal low-side MOSFET. At least six PGND vias are required to be placed as close as possible to the PGND pins. This minimizes parasitic impedance and also lowers thermal resistance.
19	VCC	I/O	Internal 3-V LDO output. An external bias with 3.3-V or higher voltage can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. Requires a 2.2-µF, at least 6.3-V rating ceramic capacitor from the VCC pin to PGND pins as the decoupling capacitor and the placement is required to be as close as possible.
20	SW	O	Output switching terminal of the power converter. Connect this pin to the output inductor.

(1) I = Input, O = Output, P = Supply, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	18	V
Pin voltage	VIN – SW, DC	–0.3	18	V
Pin voltage	VIN – SW, < 20 ns transient	–4	25	V
Pin voltage	SW – PGND, DC	–0.3	18	V
Pin voltage	SW – PGND, < 20 ns transient	–5	21.5	V
Pin voltage	BOOT – PGND	–0.3	24	V
Pin voltage	BOOT – SW	–0.3	6	V
Pin voltage	VCC	–0.3	6	V
Pin voltage	EN, PGOOD	–0.3	6	V
Pin voltage	MODE	–0.3	6	V
Pin voltage	TRIP, SS/REFIN, FB	–0.3	3	V
Pin voltage	VSNS–	–0.3	0.3	V
Sinking current	Power Good sinking current capability		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range when VCC pin is powered by a valid external bias	2.7		16	V
V_{IN}	Input voltage range when using the internal VCC LDO	4.0		16	V
V_{IN}	Minimum VIN before enabling the converter when using the internal VCC LDO	3.0			V
V_{OUT}	Output voltage range	0.9		5.5	V
Pin voltage	External VCC bias	3.13		5.3	V
Pin voltage	BOOT to SW	–0.1		5.3	V
Pin voltage	EN, PGOOD	–0.1		5.5	V
Pin voltage	MODE	–0.1		VCC	V
Pin voltage	TRIP, SS/REFIN, FB	–0.1		1.5	V
Pin voltage	VSNS– (refer to AGND)	–50		50	mV
I_{PG}	Power Good input current capability	0		10	mA
IL_{PEAK}	Maximum peak inductor current			25	A
	Minimum R_{TRIP}			4.0	kΩ
T_J	Operating junction temperature	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS54JA20		UNIT
		RWW (QFN, JEDEC)	RWW (QFN, TI EVM)	
		21 PINS	21 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.5	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.2	Not applicable [2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	Not applicable [2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.2	9.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Not applicable to an EVM layout.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	V_{IN} = 12 V, V_{EN} = 2 V, V_{FB} = V_{INTREF} + 50mV (non-switching), no external bias on VCC pin		680	850	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{IN} = 12 V, V_{EN} = 0 V, no external bias on VCC pin		9.5	20	µA
$I_{Q(VCC)}$	VCC quiescent current	T_J = 25°C, V_{IN} = 12 V, V_{EN} = 2 V, V_{FB} = V_{INTREF} + 50mV (non-switching), 3.3V external bias on VCC pin		680	820	µA
I_{VCC}	VCC external bias current [1]	3.3 V external bias on VCC pin, regular switching. T_J = 25°C, V_{IN} = 12 V, V_{EN} = 2 V, R_{MODE} = 0 Ω to AGND		7		mA
		3.3 V external bias on VCC pin, regular switching. T_J = 25°C, V_{IN} = 12 V, V_{EN} = 2 V, R_{MODE} = 30.1 kΩ to AGND		9.5		mA
		3.3 V external bias on VCC pin, regular switching. T_J = 25°C, V_{IN} = 12 V, V_{EN} = 2 V, R_{MODE} = 60.4 kΩ to AGND		11.5		mA
$I_{SD(VCC)}$	VCC shutdown current	V_{EN} = 0 V, V_{IN}=0 V, 3.3 V external bias on VCC pin		40	60	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	VIN rising, VCC = 3.3 V external bias	2.1	2.4	2.7	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	VIN falling, VCC = 3.3 V external bias	1.55	1.85	2.15	V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.17	1.22	1.27	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.97	1.02	1.07	V
$V_{EN(H)}$	EN voltage hysteresis			0.2		V
$I_{EN(LKG)}$	EN input leakage current	V_{EN} = 3.3 V		0.5	5	µA
	EN internal pull-down resistance	EN pin to AGND		6500		kΩ
INTERNAL LDO (VCC PIN)						
	Internal LDO output voltage	V_{IN} = 12 V, $I_{LOAD(VCC)}$ = 2 mA	2.90	3.02	3.12	V
$VCC_{UVLO(R)}$	VCC UVLO rising threshold	VCC rising	2.80	2.87	2.94	V
$VCC_{UVLO(F)}$	VCC UVLO falling threshold	VCC falling	2.62	2.70	2.77	
$VCC_{UVLO(H)}$	VCC UVLO hysteresis			0.17		V
	VCC LDO dropout voltage	T_J = 25°C, V_{IN} = 3.0 V, I_{VCC_LOAD} = 2 mA, non-switching			27	mV
	VCC LDO short-circuit current limit	V_{IN} = 12 V, all temperature	52	105	158	mA
REFERENCE VOLTAGE						
	Internal voltage reference range	T_J = 0°C to 85°C	896		904	mV
	Internal voltage reference range	T_J = –40°C to 125°C	891		909	mV

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T_J = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{FB(LKG)}$	Input leakage current into FB pin	V_{FB} = V_{INTREF}		1	40	nA
	SS/REFIN-to-FB Accuracy	T_J = -40°C to 125°C, $V_{SS/REFIN}$ = 0.9 V, VSNS- = AGND, refer to V_{INTREF}	–0.6%		0.6%	
SWITCHING FREQUENCY						
f_{SW}	SW switching frequency, FCCM operation	T_J = 25°C, V_{IN} = 12 V, V_{OUT}=1.2V, No load, R_{MODE} = 0 Ω to AGND	0.54	0.62	0.70	MHz
		T_J = 25°C, V_{IN} = 12 V, V_{OUT}=1.2V, No load, R_{MODE} = 30.1 kΩ to AGND	0.72	0.8	0.88	
		T_J = 25°C, V_{IN} = 12 V, V_{OUT}=1.2V, No load, R_{MODE} = 60.4 kΩ to AGND	0.82	0.97	1.1	
STARTUP						
	EN to first switching delay, internal LDO	The delay from EN goes high to the first SW rising edge with internal LDO configuration. C_{VCC} = 2.2 µF. $C_{SS/REFIN}$ = 220 nF.		0.93	2	ms
	EN to first switching delay, external VCC bias	The delay from EN goes high to the first SW rising edge with external VCC bias configuration. VCC bias should reach regulation before EN ramp up. $C_{SS/REFIN}$ = 220 nF.		550	900	µs
t_{SS}	Internal fixed Soft-start time	V_O rising from 0 V to 95% of final setpoint, $C_{SS/REFIN}$ = 1nF	1	1.5		ms
	SS/REFIN sourcing current	$V_{SS/REFIN}$ = 0 V		36		µA
	SS/REFIN sinking current	$V_{SS/REFIN}$ = 1 V		12		µA
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, BOOT–SW = 3 V		10.2		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, VCC = 3 V		3.1		mΩ
$t_{ON(min)}$	Minimum on-time	T_J = 25°C, VCC = Internal LDO		70	85	ns
$t_{OFF(min)}$	Minimum off-time	T_J = 25°C, VCC = Internal LDO, I_O=1.5A, V_{FB} = V_{INTREF} – 20 mV, SW falling edge to rising edge			220	ns
BOOT CIRCUIT						
$I_{BOOT(LKG)}$	BOOT leakage current	T_J = 25°C, $V_{BOOT-SW}$ = 3.3 V		35	50	µA
$V_{BOOT-SW(UV_F)}$	BOOT-SW UVLO falling threshold	T_J = 25°C, V_{IN} = 12 V, $V_{BOOT-SW}$ falling		2.0		V
OVERCURRENT PROTECTION						
R_{TRIP}	TRIP pin resistance range		4.0		14.7	kΩ
	Current limit clamp	Valley current on LS FET, 0 Ω ≤ R_{TRIP} ≤ 3.32 kΩ	15.1	18.4	21.4	A
K_{OCL}	Constant K_{OCL} for R_{TRIP} equation			60000		A × Ω
K_{OCL}	Constant K_{OCL} tolerance	4.02 kΩ ≤ R_{TRIP} ≤ 7.5 kΩ	–15%		18.8%	
K_{OCL}	Constant K_{OCL} tolerance	R_{TRIP} = 10 kΩ	–27%		27%	
I_{NOCL}	Negative current limit threshold	All VINs	–12	–10	–8	A
I_{ZC}	Zero-cross detection current threshold, open loop	V_{IN} = 12 V, VCC = Internal LDO		400		mA
OUTPUT OVP AND UVP						
V_{OVP}	Output Overvoltage-protection (OVP) threshold voltage		113%	116%	119%	
$t_{OVP(delay)}$	Output OVP response delay	With 100-mV overdrive		400		ns
V_{UVP}	Output Undervoltage-protection (UVP) threshold voltage		77%	80%	83%	
$t_{UVP(delay)}$	Output UVP filter delay			68		µs
POWER GOOD						
V_{PGTH}	PGOOD threshold	FB rising, PGOOD low to high	89%	92.5%	95%	
		FB rising, PGOOD high to low	113%	116%	119%	
		FB falling, PGOOD high to low	77%	80%	83%	
	OOB (Out-Of-Bounds) threshold	FB rising, PGOOD stays high	103%	105.5%	108%	

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T_J = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.4 V, V_{IN} = 12 V, VCC = Internal LDO			10	mA
$V_{PG(low)}$	PGOOD low-level output voltage	I_{PGOOD} = 5.5 mA, V_{IN} = 12 V, VCC = Internal LDO			400	mV
$t_{PGDLY(R)}$	Delay for PGOOD from low to high	During startup only		1.06	1.40	ms
$t_{PGDLY(F)}$	Delay for PGOOD from high to low			0.5	5	µs
$I_{PG(LKG)}$	PGOOD leakage current when pulled high	T_J = 25°C, V_{PGOOD} = 3.3 V, V_{FB} = V_{INTREF}			5	µA
	PGOOD clamp low-level output voltage	V_{IN} = 0 V, VCC = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 100-kΩ resistor		710	850	mV
		V_{IN} = 0 V, VCC = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 10-kΩ resistor		850	1000	mV
	Minimum VCC for valid PGOOD output	V_{IN} = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 100-kΩ resistor, V_{PGOOD} ≤ 0.4 V			1.5	V
OUTPUT DISCHARGE						
R_{Dischg}	Output discharge resistance	V_{IN} = 12 V, VCC = Internal LDO, V_{SW} = 0.5 V, power conversion disabled		70		Ω
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising	150	165		°C
T_{HYST}	Thermal shutdown hysteresis (1)			30		°C

(1) Specified by design. Not production tested.

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6.6 Typical Characteristics

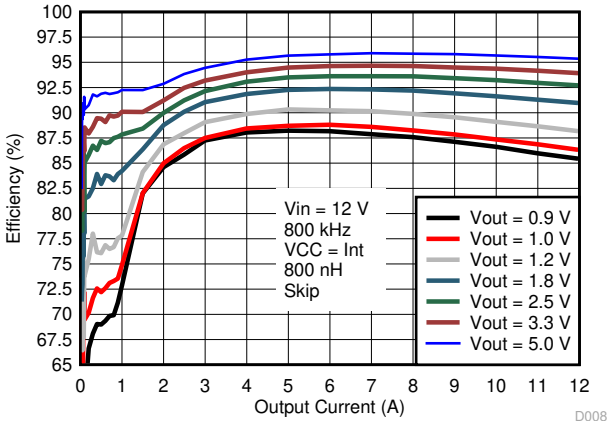


図 6-1. Efficiency vs Output Current, Skip-mode, Internal VCC LDO

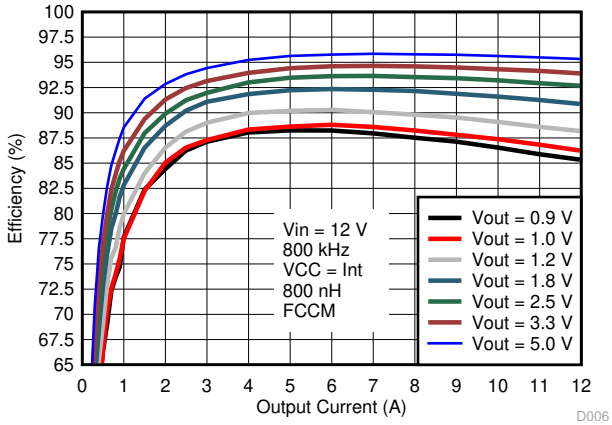


図 6-2. Efficiency vs Output Current, FCCM, Internal VCC LDO

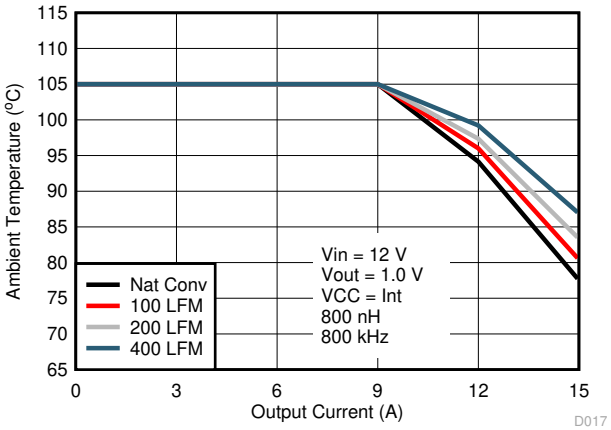


図 6-3. Safe Operating Area, V_{OUT} = 1.0 V

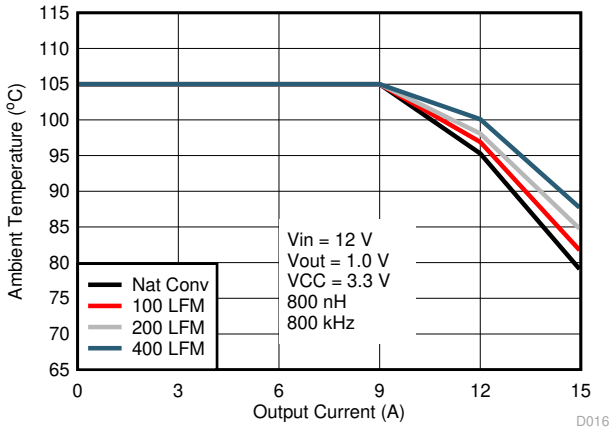


図 6-4. Safe Operating Area, V_{OUT} = 1.0 V

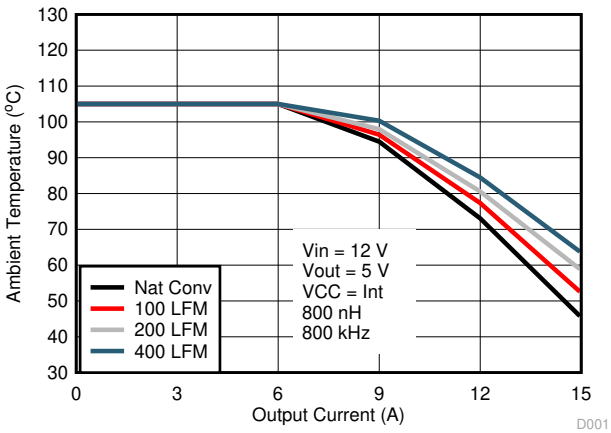


図 6-5. Safe Operating Area, V_{OUT} = 5 V

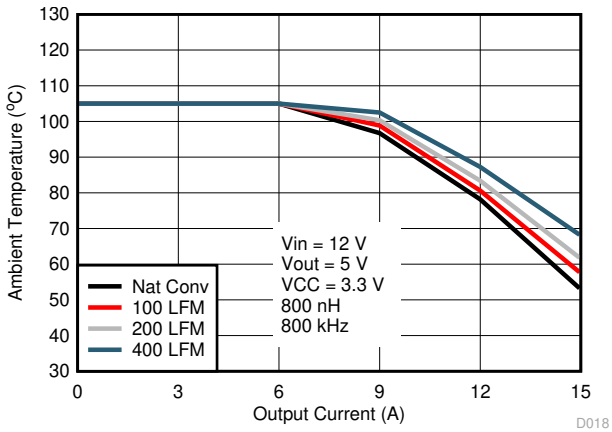


図 6-6. Safe Operating Area, V_{OUT} = 5 V

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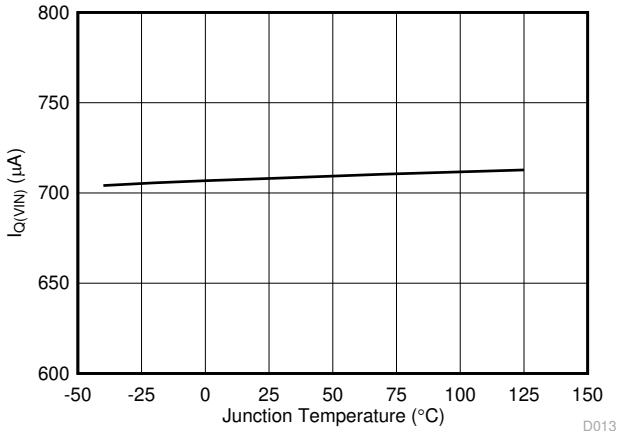
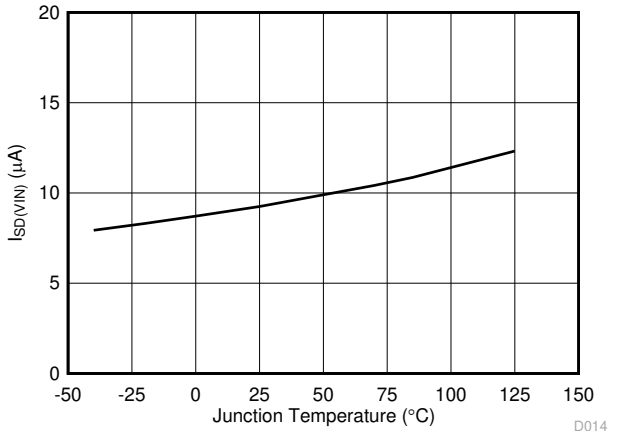
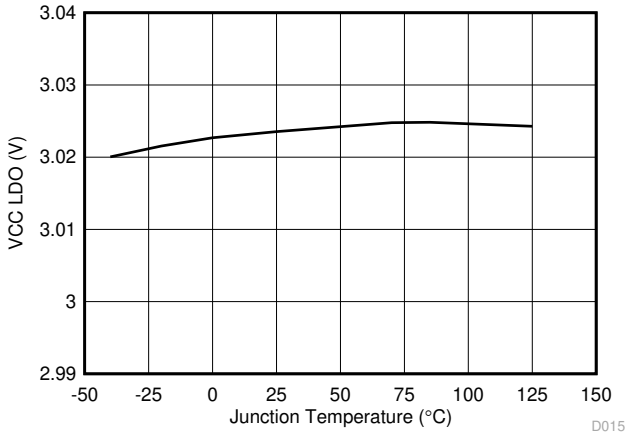


図 6-7. $I_{Q(VIN)}$ vs Junction Temperature



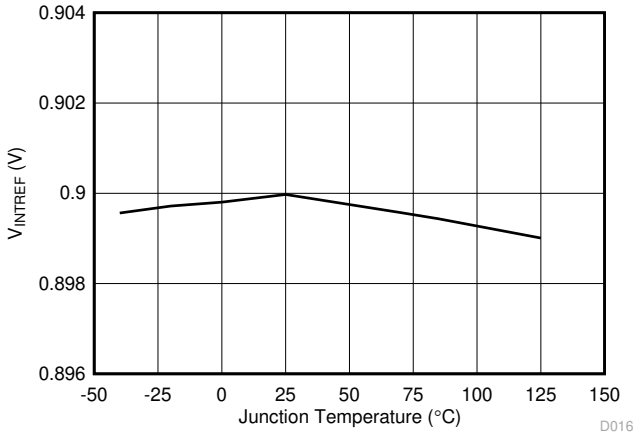
V_{IN} = 12 V V_{EN} = 0 V Internal VCC LDO

図 6-8. $I_{SD(VIN)}$ vs Junction Temperature



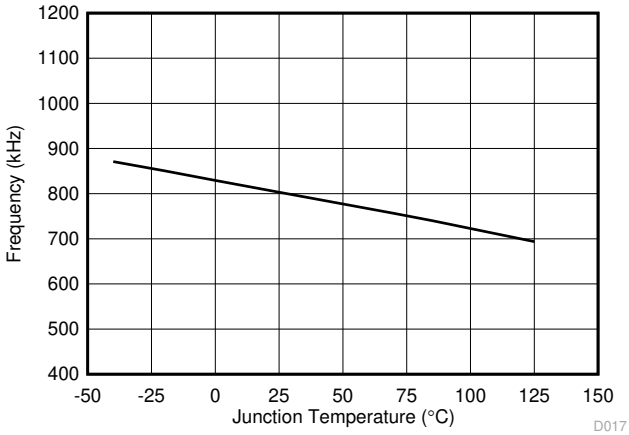
V_{IN} = 12 V I_{VCC} = 2 mA

図 6-9. VCC LDO vs Junction Temperature



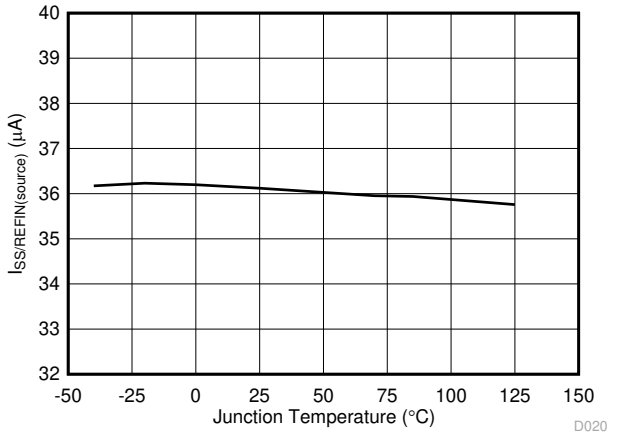
V_{IN} = 12 V

図 6-10. V_{INTREF} vs Junction Temperature



V_{IN} = 12 V

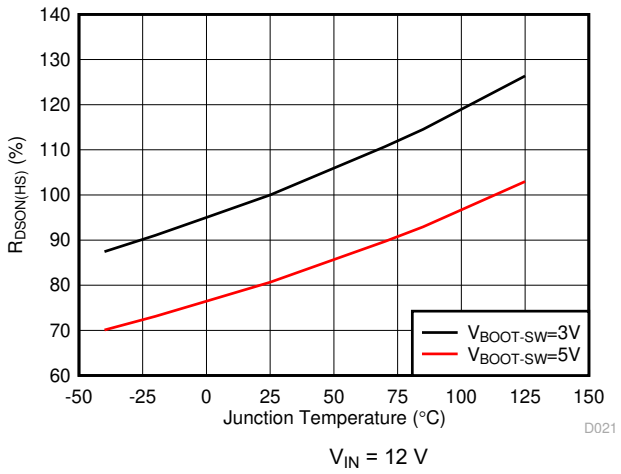
図 6-11. Switching Frequency vs Junction Temperature



V_{IN} = 12 V

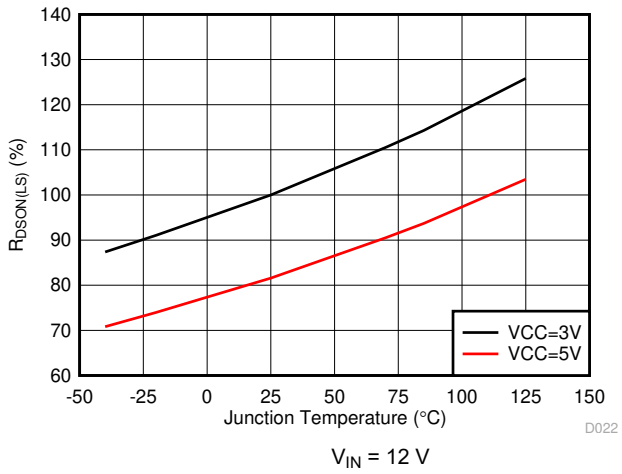
図 6-12. $I_{SS(source)}$ vs Junction Temperature

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V_{IN} = 12 V

図 6-13. $R_{DSON(HS)}$ vs Junction Temperature



V_{IN} = 12 V

図 6-14. $R_{DSON(LS)}$ vs Junction Temperature

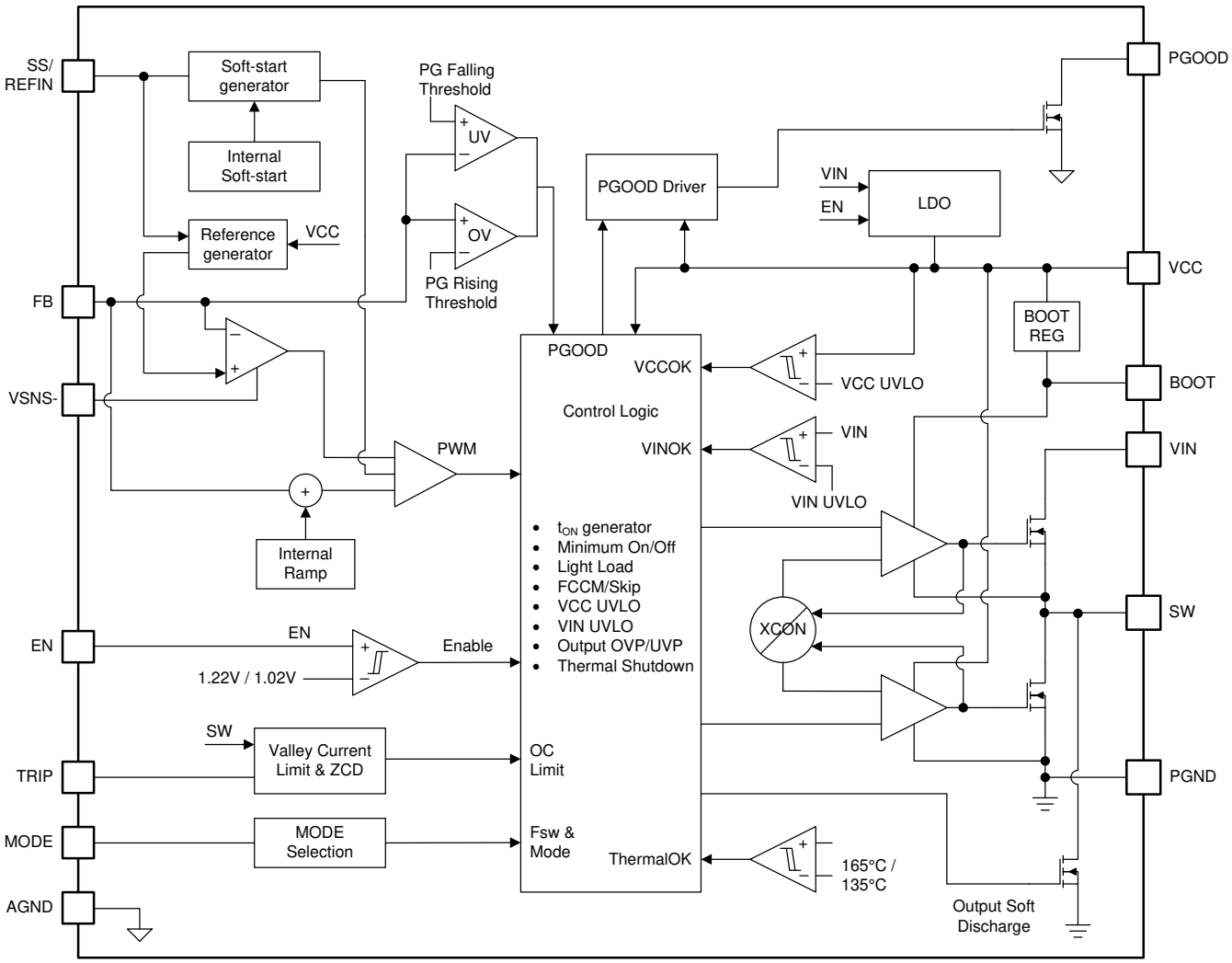
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7 Detailed Description

7.1 Overview

The TPS54JA20 device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device suits low output voltage point-of-load applications with 12-A or lower output current in server, storage, and similar computing applications. The TPS54JA20 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an ideal fashion. The output voltage ranges from 0.9 V to 5.5 V. The conversion input voltage ranges from 2.7 V to 16 V, and the VCC input voltage ranges from 3.13 V to 5.3 V. The D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy to use and also allows low external component count. Further advantage of this control scheme is that it supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low-ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during load-step transient.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Internal VCC LDO And Using External Bias On VCC Pin

The TPS54JA20 has an internal 3-V LDO featuring input from VIN and output to VCC. When the EN voltage rises above the enable threshold (typically 1.22 V), the internal LDO is enabled and starts regulating output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.

The VCC pin needs to be bypassed with a 2.2-µF, at least 6.3-V rating ceramic capacitor. An external bias that is above the output voltage of the internal LDO can override the internal LDO. This enhances the efficiency of the converter because the VCC current now runs off this external bias instead of the internal linear regulator.

The VCC UVLO circuit monitors the VCC pin voltage and disables the whole converter when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

The following are considerations when using an external bias on the VCC pin:

- When the external bias is applied on the VCC pin early enough (for example, before EN signal comes in), the internal LDO will be always forced off and the internal analog circuits will have a stable power supply rail at their power enable.
- (Not recommended) When the external bias is applied on the VCC pin late (for example, after EN signal comes in), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. It is important to understand that an external discharge path on the VCC pin, which can pull a current higher than the current limit of the internal LDO from the VCC pin and can potentially turn off VCC LDO thereby shutting down the converter output.
- A good power-up sequence is at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. For example, a practical power-up sequence is: VIN applied first, then the external bias applied, and then EN signal goes high.

7.3.2 Enable

When the EN pin voltage rises above the enable threshold voltage (typically 1.22 V) and V_{IN} rises above the VIN UVLO rising threshold, the device enters its internal power-up sequence. The EN to first switching delay is specified in the Start-up section of the *Electrical Characteristics*.

When using the internal VCC LDO, the internal power-up sequence includes three sequential steps. During the first period, the VCC voltage is charged up on a VCC bypass capacitor by an 11-mA current source. The length of this VCC LDO start-up time varies with the capacitance on the VCC pin. However, if the V_{IN} voltage ramps up very slowly, the VCC LDO output voltage will be limited by the V_{IN} voltage level, thus the VCC LDO start-up time can be extended longer. Since the VCC LDO start-up time is relatively long, the internal V_{INTREF} build-up happens and finishes during this period. Once the VCC voltage crosses above the VCC UVLO rising threshold (typically 2.87 V), the device moves to the second step, power-on delay. The MODE pin setting detection, SS/REFIN pin detection, and control loop initialization are finished within this 285-µs delay. A soft-start ramp starts when the 285-µs power-on delay finishes. During the soft-start ramp power stage, switching does not happen until the SS/REFIN pin voltage reaches 50 mV. This introduced a SS delay which varies with the external capacitance on the SS/REFIN pin.

図 7-1 shows an example where the VIN UVLO rising threshold is satisfied earlier than the EN rising threshold. In this scenario, the VCC UVLO rising threshold becomes the gating signal to start the internal power-up sequence, and the sequence between VIN and EN does not matter.

When using an external bias on the VCC pin, the internal power-up sequence still includes three sequential steps. The first period is much shorter since VCC voltage is built up already. A 100-µs period allows the internal references to start up and reach regulation points. This 100-µs period includes not only the 0.9-V V_{INTREF}, but also all of the other reference voltages for various functions. The device then moves to the second step, power-on delay. The MODE pin setting detection, SS/REFIN pin detection, and control loop initialization are finished within this 285-µs delay. A soft-start ramp starts when the 285-µs power-on delay finishes. During the soft-start ramp power stage, switching does not happen until the SS/REFIN pin voltage reaches 50 mV. This introduced a SS delay which varies with the external capacitance on SS/REFIN pin.

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図 7-2 shows an example where both the VIN UVLO rising threshold and EN rising threshold are satisfied later than the VCC UVLO rising threshold. In this scenario, the VIN UVLO rising threshold or EN rising threshold, whichever is satisfied later, becomes the gating signal to start the internal power-up sequence.

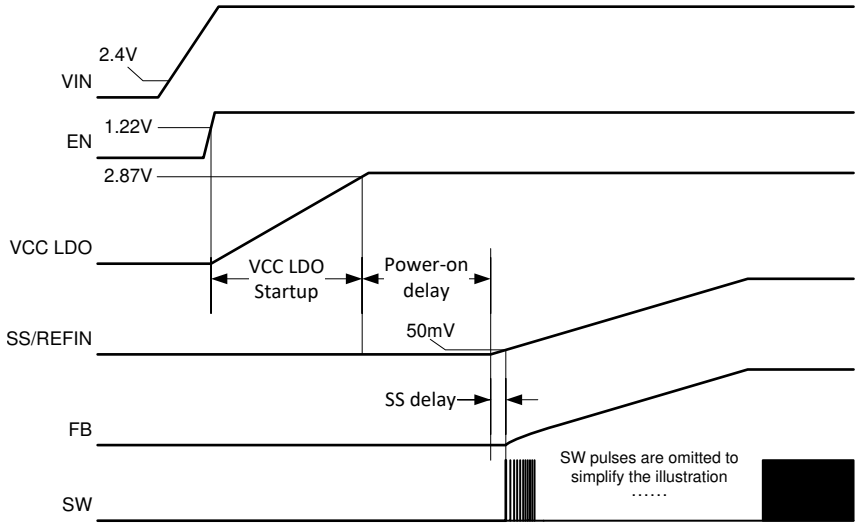


図 7-1. Internal Power-up Sequence Using Internal LDO

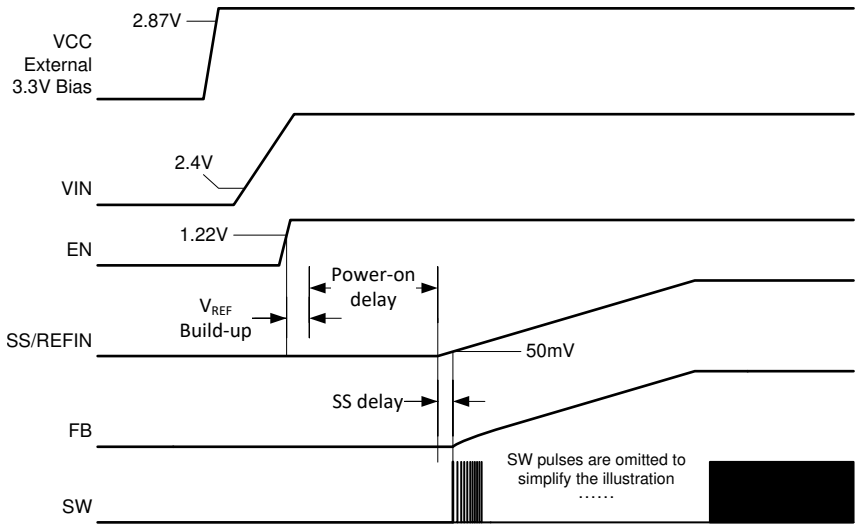


図 7-2. Internal Power-up Sequence Using External Bias

The EN pin has an internal filter to avoid unexpected ON or OFF due to small glitches. The time constant of this RC filter is 5 µs. For example, when applying a 3.3-V voltage source on the EN pin, which jumps from 0 V to 3.3 V with ideal rising edge, the internal EN signal will reach 2.086 V after 5 µs, which is 63.2% of applied 3.3-V voltage level.

A internal pulldown resistor is implemented between the EN pin and AGND pin. To avoid impact to the EN rising/falling threshold, this internal pulldown resistor is set to 6.5 MΩ. With this pulldown resistor, floating the EN pin before start-up keeps the TPS54JA20 device under disabled state. During nominal operation when the power stage switches, this large internal pulldown resistor may not have enough noise immunity to hold EN pin low.

The recommended operating condition for EN pin is maximum 5.5 V. *Do not* connect the EN pin to the VIN pin directly.

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7.3.3 Output Voltage Setting

The output voltage is programmed by the voltage divider resistors, R_{FB_HS} and R_{FB_LS}. Connect R_{FB_HS} between the FB pin and the positive node of the load, and connect R_{FB_LS} between the FB pin and VSNS– pin. The recommended R_{FB_LS} value is 10 kΩ, ranging from 1 kΩ to 20 kΩ. Determine R_{FB_HS} by using 式 1.

$$R_{FB_HS} = \frac{V_O - V_{INTREF}}{V_{INTREF}} \times R_{FB_LS} \quad (1)$$

The FB accuracy is determined by two elements. The first element is the accuracy of the internal 900-mV reference, which will be applied to the SS/REFIN pin unless an external V_{REF} is applied. The TPS54JA20 device offers ±0.5% V_{INTREF} accuracy from 0°C to 85°C, and ±1.0% V_{INTREF} accuracy from -40°C to 125°C. The second element is the SS/REFIN-to-FB accuracy, which tells you how accurately the control loop regulates FB node to SS/REFIN pin. The TPS54JA20 device offers ±0.6% SS/REFIN-to-FB accuracy from -40°C to 125°C. For example, when operating from 0°C to 85°C, the total FB accuracy is ±1.1% which includes the impact from chip junction temperature and also the variation from part to part.

To improve the overall V_{OUT} accuracy, using ±1% accuracy or better resistor for the FB voltage divider is highly recommended.

Regardless of remote sensing or single-end sensing connection, the FB voltage divider, R_{FB_HS} and R_{FB_LS}, should be always placed as close as possible to the device.

7.3.3.1 Remote Sense

The TPS54JA20 device offers remote sense function through the FB and VSNS– pins. Remote sense function compensates a potential voltage drop on the PCB traces, thus helps maintain V_{OUT} tolerance under steady state operation and load transient event. Connecting the FB voltage divider resistors to the remote location allows sensing the output voltage at a remote location. The connections from the FB voltage divider resistors to the remote location should be a pair of PCB traces with at least 12-mil trace width, and should implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher. The ground connection of the remote sensing signal must be connected to the VSNS– pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor, R_{FB_LS}, terminated at the VSNS– pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines should stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. It is recommended to shield the pair of remote sensing lines with ground planes above and below.

Single-ended Vo sensing is often used for local sensing. For this configuration, connect the higher FB resistor, R_{FB_HS}, to a high-frequency local bypass capacitor of 0.1 µF or higher, and short VSNS– to AGND.

The recommended VSNS– operating range (refer to AGND pin) is –50 mV to +50 mV.

7.3.4 Internal Fixed Soft Start and External Adjustable Soft Start

The TPS54JA20 implements a circuit to allow both internal fixed soft start and external adjustable soft start. The internal soft-start time is typically 1.5 ms. The soft-start time can be increased by adding a soft-start (SS) capacitor between the SS/REFIN and VSNS– pins. The total SS capacitor value can be determined by 式 2. The device follows the longer SS ramp among the internal SS time and the SS time determined by the external SS capacitors. The recommended maximum SS capacitor is 1 µF. A minimum 1-nF SS capacitor is required.

The device does not require a capacitor from the SS/REFIN pin to AGND, thus it is not recommenced to place a capacitor from the SS/REFIN pin to AGND. If both $C_{SS/REFIN}$-to-VSNS– and $C_{SS/REFIN}$-to-AGND capacitors exist, place $C_{SS/REFIN}$-to-VSNS– more closely with shortest trace back to the VSNS– pin.

The SS/REFIN pin is discharged internally during the internal power-on delay to make sure the soft-start ramp always starts from zero.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 36(\mu A)}{V_{INTREF}(V)} \quad (2)$$

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7.3.5 External REFIN For Output Voltage Tracking

The TPS54JA20 provides an analog input pin (SS/REFIN) to accept an external reference (that is, a DC voltage source). The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. When an external voltage reference is applied between the SS/REFIN pin and VSNS– pin, it acts as the reference voltage, thus the FB voltage follows this external voltage reference exactly. The same ±0.6% SS/REFIN-to-FB accuracy from -40°C to 125°C applies here too.

In the middle of internal power-on delay, a detection circuit senses the voltage on the SS/REFIN pin to tell you whether an active DC voltage source is applied. Before the detection happens, the SS/REFIN pin tries to discharge any energy on the SS/REFIN capacitors through an internal 120-Ω resistor to AGND. This discharge lasts for 125 µs. Then, within a 32-µs window, the detection circuit compares the SS/REFIN pin voltage with an internal reference equal to 89% of V_{INTREF}. This discharge operation ensures a SS capacitor with left-over energy will not be wrongly detected as a voltage reference. If the external voltage reference fails to supply sufficient current and hold voltage level higher than 89% of V_{INTREF}, the SS/REFIN detection circuit will provide a wrong detection result.

If the detection result is that the SS/REFIN pin voltage falls below 89% of V_{INTREF} which tells you no external reference is connected, the device first uses the internal fixed V_{INTREF} as the reference for the PGOOD threshold, V_{OUT} OVP, and V_{OUT} UVP threshold. On this configuration, given the SS/REFIN pin sees a soft-start ramp on this pin, the slower ramp among the internal fixed soft start and the external soft start determines the start-up of FB. Once both the internal and external soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2 ms to finish. The external soft-start done signal goes high when FB reaches a threshold equal to V_{INTREF} – 50 mV. The device waits for the PGOOD status transition from low to high, then starts using the SS/REFIN pin voltage instead of the internal V_{INTREF} as the reference for PGOOD threshold, V_{OUT} OVP, and V_{OUT} UVP threshold.

If the detection result is that the SS/REFIN pin voltage holds higher than 89% of V_{INTREF} which tells you an active DC voltage source is used as an external reference, the device always uses the SS/REFIN pin voltage, instead of the internal V_{INTREF}, as the reference for PGOOD threshold, V_{OUT} OVP, and V_{OUT} UVP threshold. On this configuration, since the SS/REFIN pin sees a DC voltage and no soft-start ramp on this pin, the internal fixed soft start is used for start-up. Once the internal soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2 ms to finish because the soft-start ramp goes beyond V_{INTREF}.

On this external REFIN configuration, applying a stabilized DC external reference to the SS/REFIN pin before EN high signal is recommended. During the internal power-on delay, the external reference should be capable to hold the SS/REFIN pin equal to or higher than 89% of V_{INTREF}, so that the device can correctly detect the external reference and choose the right thresholds for Power Good, V_{OUT} OVP, and V_{OUT} UVP. After the Power Good status transits from low to high, the external reference can be set in a range of 0.5 V to 1.2 V. To overdrive the SS/REFIN pin during nominal operation, the external reference has to be able to sink more than 36-µA current if the external reference is lower than the internal V_{INTREF}, or source more than 12-µA current if the external reference is higher than the internal V_{INTREF}. When driving the SS/REFIN pin by an external reference through a resistor divider, the resistance of the divider should be low enough to provide the sinking or sourcing current capability.

The configuration of applying the EN high signal first, then applying an external ramp on the SS/REFIN pin as a tracking reference can be achieved, as long as design considerations for Power Good, V_{OUT} OVP, and V_{OUT} UVP have been taken. Please contact Texas Instruments for detailed information about this configuration.

If the external voltage source must transition up and down between any two voltage levels, the slew rate must be no more than 1 mV/µs.

7.3.6 Frequency and Operation Mode Selection

The TPS54JA20 provides forced CCM operation for tight output ripple application and auto-skip Eco-mode for high light-load efficiency. The TPS54JA20 allows users to select the switching frequency and operation mode by connecting a resistor from the MODE pin to AGND pin. 表 7-1 lists the resistor values for the switching frequency

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and operation mode selection. TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

The MODE state will be set and latched during the internal power-on delay period. Changing the MODE pin resistance after the power-on delay will not change the status of the device. The internal circuit will set the MODE pin status to 600 kHz / skip mode if the MODE pin is left open during the power-on delay period.

To make sure the internal circuit detects the desired option correctly, *do not* place any capacitor on the MODE pin.

表 7-1. MODE Pin Selection

MODE PIN CONNECTIONS	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)
Short to VCC	Skip-mode	600
243-kΩ ± 10% to AGND	Skip-mode	800
121-kΩ ± 10% to AGND	Skip-mode	1000
60.4-kΩ ±10% to AGND	Forced CCM	1000
30.1-kΩ ±10% to AGND	Forced CCM	800
Short to AGND	Forced CCM	600

7.3.7 D-CAP3 Control

The TPS54JA20 uses D-CAP3 mode control to achieve the fast load transient while maintaining the ease-of-use feature. The D-CAP3 control architecture includes an internal ripple generation network, enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low-ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP3 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop operation. The amplitude of the ramp is determined by V_{IN}, V_{OUT}, operating frequency, and the R-C time-constant of the internal ramp circuit. At different switching frequency settings (see 表 7-1), the R-C time-constant varies to maintain relatively constant ramp amplitude. Also, the device utilizes internal circuitry to cancel the dc offset caused by injected ramp and significantly reduce the dc offset caused by the output ripple voltage, especially under light load condition.

For any control topologies that do not support external compensation design, there is a minimum range of the output filter, maximum range of the output filter, or both, it can support. The output filter used with the TPS54JA20 is a low-pass L-C circuit. This L-C filter has double pole that is described in 式 3.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54JA20. The low frequency L-C double pole has a 180-degree drop in-phase. At the output filter frequency, the gain rolls off at a –40-dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40-dB to –20-dB per decade and increases the phase by 90 degrees per decade above the zero frequency.

After identifying the application requirements, the output inductance should be designed so that the inductor peak-to-peak ripple current is approximately between 15% and 40% of the maximum output current.

The inductor and capacitor selected for the output filter must be such that the double pole of 式 3 is located no higher than 1/30 of operating frequency. Choose very small output capacitance leads to relative high frequency L-C double pole which allows that overall loop gain stays high until the L-C double frequency. Given the zero from the internal ripple generation network is relatively high frequency as well, the loop with very small output capacitance can have too high of crossover frequency which is not desired. Use 表 7-2 to help locate the internal zero based on the selected switching frequency.

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表 7-2. Locating the Zero

SWITCHING FREQUENCIES (f_{SW}) (kHz)	ZERO (f_Z) LOCATION (kHz)
600	84.5
800	84.5
1000	106

In general, where reasonable (or smaller) output capacitance is desired, the output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation.

For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100 of operating frequency. With this starting point, verify the small signal response on the board using the following one criteria:

- Phase margin at the loop crossover is greater than 50 degrees

The actual maximum output capacitance can go higher as long as phase margin is greater than 50 degrees. However, small signal measurement (bode plot) should be done to confirm the design.

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10 µF, X5R, and 6.3 V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case, is 40% and 4 µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system/applications.

For higher output voltage at or above 2 V, additional phase boost can be required to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on-time (t_{ON})) setting in a fixed-on-time topology based operation. A feedforward capacitor placing in parallel with R_{FB_HS} is found to be very effective to boost the phase margin at loop crossover. Refer to the *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application report for details.

Besides boost the phase, a feedforward capacitor feeds more V_{OUT} node information into the FB node by AC coupling. This feedforward during load transient event enables the control loop to a faster response to V_{OUT} deviation. However, this feedforward during steady state operation also feeds more V_{OUT} ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double pulse behavior. To determine the final feedforward capacitor value, impacts to phase margin, load transient performance and ripple, and noise on FB should be all considered. Using Frequency Analysis equipment to measure the crossover frequency and the phase margin is recommended.

7.3.8 Low-side FET Zero-Crossing

The TPS54JA20 uses a zero-crossing circuit to perform the zero inductor-current detection during skip-mode operation. The function compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. The zero-crossing threshold is set to a positive value to avoid negative inductor current. As a result, the device delivers better light-load efficiency.

7.3.9 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on-time of the high-side FET, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time, and the output inductor value. During the on-time of the low-side FET, this current decreases linearly. The average value of the switch current equals to the load current.

The output overcurrent limit (OCL) in the TPS54JA20 device is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the on-time of the low-side FET by measuring the low-side FET drain-to-source current. If the measured drain-to-source current of the low-side FET is above the current limit threshold, the low-side FET stays ON until the current level becomes lower than the current limit threshold. This type of behavior reduces the average output current sourced by the device. During an overcurrent condition, the current to the load exceeds the current to the output capacitors. Thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold

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(80%), the UVP comparator detects it and shuts down the device after a wait time of 68 µs. The device remains latched off state (both high-side and low-side FETs are latched off) until a reset of V_{IN} or a re-toggling on EN pin. 図 7-3 shows the cycle-by-cycle valley current limit behavior as well as the wait time before the device shuts down.

If an OCL condition happens during start-up, the device still has cycle-by-cycle current limit based on low-side valley current. After soft start is finished, the UV event, which is caused by the OC event, shuts down the device and enters latch-off mode with a wait time of 68 µs.

The resistor, R_{TRIP}, connected from the TRIP pin to AGND sets current limit threshold. A ±1% tolerance resistor is highly recommended because a worse tolerance resistor provides less accurate OCL threshold. 式 4 calculates the R_{TRIP} for a given overcurrent limit threshold on the device. To simplify the calculation, use a constant, K_{OCL}, to replace the value of $6x10^4$. 式 5 calculates the overcurrent limit threshold for a given R_{TRIP} value. The tolerance of K_{OCL} is listed in the *Electrical Characteristics* to help you analyze the tolerance of the overcurrent limit threshold.

To protect the device from unexpected connection on TRIP pin, an internal fixed OCL clamp is implemented. This internal OCL clamp limits the maximum valley current on LS FET when the TRIP pin has too small resistance to AGND, or is accidently shorted to ground.

$$R_{TRIP} = \frac{6 \times 10^4}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN}-V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}}} = \frac{K_{OCL}}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN}-V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}}} \quad (4)$$

where

- I_{OCLIM} is overcurrent limit threshold for load current in A
- R_{TRIP} is TRIP resistor value in Ω
- K_{OCL} is a constant for the calculation
- V_{IN} is input voltage value in V
- V_O is output voltage value in V
- L is output inductor value in µH
- f_{SW} is switching frequency in MHz

$$I_{OCLIM} = \frac{K_{OCL}}{R_{TRIP}} + \frac{1}{2} \times \frac{(V_{IN}-V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}} \quad (5)$$

where

- I_{OCLIM} is overcurrent limit threshold for load current in A
- R_{TRIP} is TRIP resistor value in Ω
- K_{OCL} is a constant for the calculation
- V_{IN} is input voltage value in V
- V_O is output voltage value in V
- L is output inductor value in µH
- f_{SW} is switching frequency in MHz

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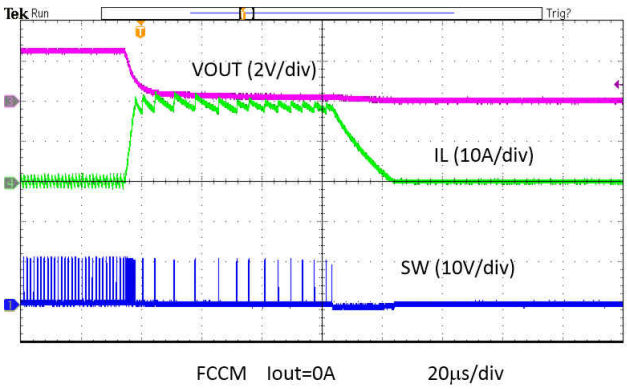


図 7-3. Overcurrent Protection

7.3.10 Low-side FET Negative Current Limit

The device has a fixed, cycle-by-cycle negative current limit. Similar with the positive overcurrent limit, the inductor current is monitored during the on-time of the low-side FET. To prevent too large of negative current flowing through the low-side FET, when the low-side FET detects –10-A current (typical threshold), the device turns off the low-side FET and then turns on the high-side FET for a proper on-time (determined by $V_{IN}/V_O/f_{SW}$). After the high-side FET on-time expires, the low-side FET turns on again.

The device should not trigger the –10-A negative current limit threshold during nominal operation unless too small inductor value is chosen or the inductor becomes saturated. This negative current limit is utilized to discharge output capacitors during an output OVP or an OOB event. See *セクション 7.3.12* and *セクション 7.3.13* for details.

7.3.11 Power Good

The device has power-good output that indicates high when the converter output is within the target. The power-good output is an open-drain output and must be pulled up to VCC pin or an external voltage source (<5.5 V) through a pullup resistor (typically 30.1 kΩ). The recommended power good pullup resistor value is 1 kΩ to 100 kΩ.

Once both the internal and external soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2 ms to finish. The external soft-start done signal goes high when FB reaches a threshold equal to V_{INTREF} – 50 mV. If the FB voltage drops to 80% of the V_{INTREF} voltage or exceeds 116% of the V_{INTREF} voltage, the power-good signal latches low after a 2-µs internal delay. The power-good signal can only be pulled high again after re-toggling EN or a reset of V_{IN}.

If the input supply fails to power up the device, for example VIN and VCC both stay at zero volt, the power-good pin clamps low by itself when this pin is pulled up through an external resistor.

Once the VCC voltage level rises above the minimum VCC threshold for valid PGOOD output (maximum 1.5 V), an internal power-good circuit is enabled to hold the PGOOD pin to the default status. By default, PGOOD is pulled low and this low-level output voltage is no more than 400 mV with 5.5-mA sinking current. The power-good function is fully activated after the soft start operation is completed.

7.3.12 Overvoltage and Undervoltage Protection

The device monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage events. When the FB voltage becomes lower than 80% of the V_{INTREF} voltage, the UVP comparator detects and an internal UVP delay counter begins counting. After the 68-µs UVP delay time, the device latches OFF both high-side and low-side FETs drivers. The UVP function enables after the soft start period is complete.

When the FB voltage becomes higher than 116% of the V_{INTREF} voltage, the OVP comparator detects and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until it reaches a negative current limit, I_{NOCL}. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again, for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}. The device operates in this cycle until

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the output voltage is pulled below the UVP threshold voltage for 68 µs. After the 68 µs UVP delay time, both the high-side FET and the low-side FET are latched OFF. The fault is cleared with a reset of VIN or by re-toggling the EN pin.

During the 68-µs UVP delay time, if output voltage becomes higher than UV threshold, thus is not qualified for UV event, the timer will be reset to zero. When the output voltage triggers the UV threshold again, the timer of the 68 µs re-starts.

7.3.13 Out-Of-Bounds (OOB) Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 5% above the V_{INTREF} voltage. OOB protection does not trigger an overvoltage fault, so the device is on non-latch mode after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced CCM mode. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus helps the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.14 Output Voltage Discharge

When the device is disabled through EN, it enables the output voltage discharge mode. This mode forces both high-side and low-side FETs to latch off, but turns on the discharge FET, which is connected from SW to PGND, to discharge the output voltage. Once the FB voltage drops below 90 mV, the discharge FET is turned off.

The output voltage discharge mode is activated by any of the following fault events:

1. EN pin goes low to disable the converter.
2. Thermal shutdown (OTP) is triggered.
3. VCC UVLO (falling) is triggered.
4. VIN UVLO (falling) is triggered.

7.3.15 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the VCC_{UVLO} falling threshold voltage, the device shuts off. If the VCC voltage increases beyond the VCC_{UVLO} rising threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

When the VIN pin voltage is lower than the VIN_{UVLO} falling threshold voltage but VCC pin voltage is still higher than VCC_{UVLO} rising threshold voltage, the device stops switching and discharges the SS/REFIN pin. Once the VIN voltage increases beyond the VIN_{UVLO} rising threshold voltage, the device re-initiates the soft start and switches again. VIN UVLO is a non-latch protection.

7.3.16 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 165°C), the device stops switching and discharges the SS/REFIN pin. When the temperature falls approximately 30°C below the threshold value, the device turns back on with a re-initiated soft start. Thermal shutdown is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Auto-Skip Eco-mode Light Load Operation

While the MODE pin is pulled to VCC directly or connected to the AGND pin through a resistor larger than 121 kΩ, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires

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more time. The transition point to the light-load operation $I_{O(LL)}$ (for example, the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in 式 6.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (6)$$

where

- f_{SW} is the switching frequency

Using only ceramic capacitors is recommended for skip mode.

7.4.2 Forced Continuous-Conduction Mode

When the MODE pin is tied to the AGND pin through a resistor less than 60.4 kΩ, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

7.4.3 Powering The Device From A 12-V Bus

The device works well when powering from a 12-V bus with a single V_{IN} configuration. As a single V_{IN} configuration, the internal LDO is powered by a 12-V bus and generates 3.0-V output to bias the internal analog circuitry and also powers up the gate drives. The V_{IN} input range under this configuration is 4 V to 16 V for up to 15-A load current. The V_{IN} range can be extended down to 3 V if the desired load current is no more than 12 A. 図 7-4 shows an example for this single V_{IN} configuration.

V_{IN} and EN are the two signals to enable the part. For start-up sequence, any sequence between the V_{IN} and EN signals can power the device up correctly.

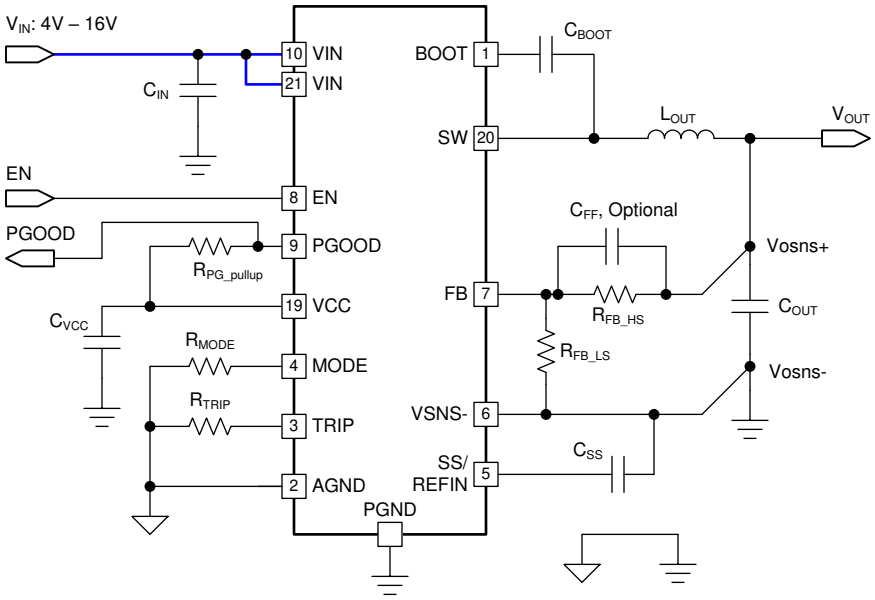


図 7-4. Single V_{IN} Configuration With 12-V Bus

7.4.4 Powering The Device From A 3.3-V Bus

The device can also work for up to 15-A load current when powering from a 3.3-V bus with a single V_{IN} configuration. To ensure the internal analog circuitry and the gate drives are powered up properly, the VCC pin should be shorted to VIN pins with low impedance trace. A trace with at least 24-mil width is recommended. A 2.2-µF, at least 6.3-V rating VCC-to-PGND decoupling capacitor is still recommended to be placed as close as possible to VCC pin. Due to the maximum rating limit on the VCC pin, the V_{IN} input range under this

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configuration is 3 V to 5.3 V. The input voltage must stay higher than both VIN UVLO and VCC UVLO, otherwise the device will shut down immediately. 図 7-5 shows an example for this single V_{IN} configuration.

V_{IN} and EN are the two signals to enable the part. For start-up sequence, any sequence between the V_{IN} and EN signals can power the device up correctly.

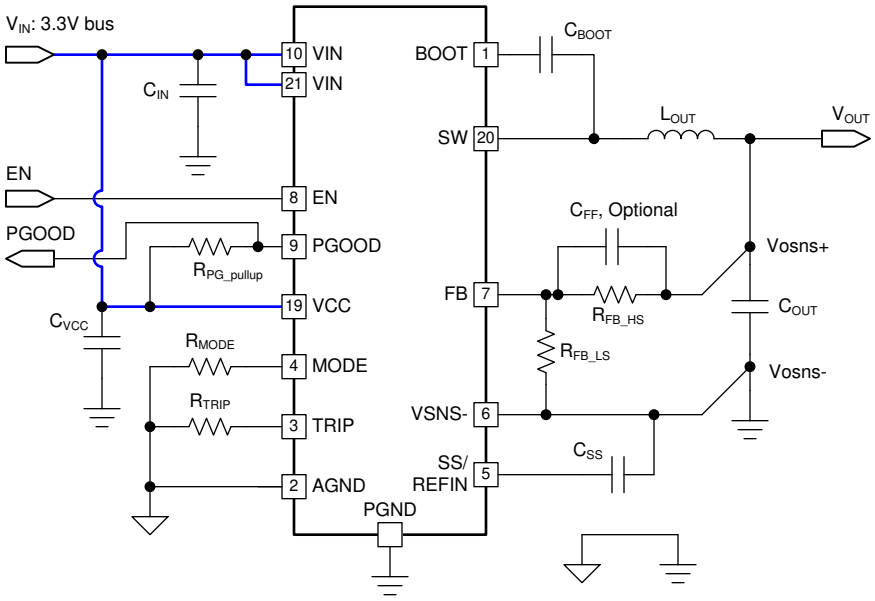


図 7-5. Single VIN Configuration With 3.3-V Bus

7.4.5 Powering The Device From A Split-rail Configuration

When an external bias, which is at a different level from the main V_{IN} bus, is applied onto the VCC pin, the device can be configured to split-rail by utilizing both the main V_{IN} bus and VCC bias. Connecting a valid VCC bias to VCC pin overrides the internal LDO, thus saves power loss on that linear regulator. This configuration helps to improve overall system level efficiency but requires a valid VCC bias. 3.3-V or 5.0-V rail is the common choice as VCC bias. With a stable VCC bias, the V_{IN} input range under this configuration can be as low as 2.7 V and up to 16 V.

The noise of the external bias affects the internal analog circuitry. To ensure a proper operation, a clean, low-noise external bias, and good local decoupling capacitor from the VCC pin to PGND pin are required. 図 7-6 shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and also the operating frequency. For example, by setting the device to skip mode, the VCC pins draw less and less current from the external bias when the frequency decreases under light load condition. The typical VCC external bias current under FCCM operation is listed in the *Electrical Characteristics* to help you prepare the capacity of the external bias.

Under split rail configuration, VIN, VCC bias, and EN are the signals to enable the part. For start-up sequence, it is recommended that at least one of VIN UVLO rising threshold and EN rising threshold is satisfied later than VCC UVLO rising threshold. A practical start-up sequence example is VIN applied first, then the external bias applied, and then EN signal goes high.

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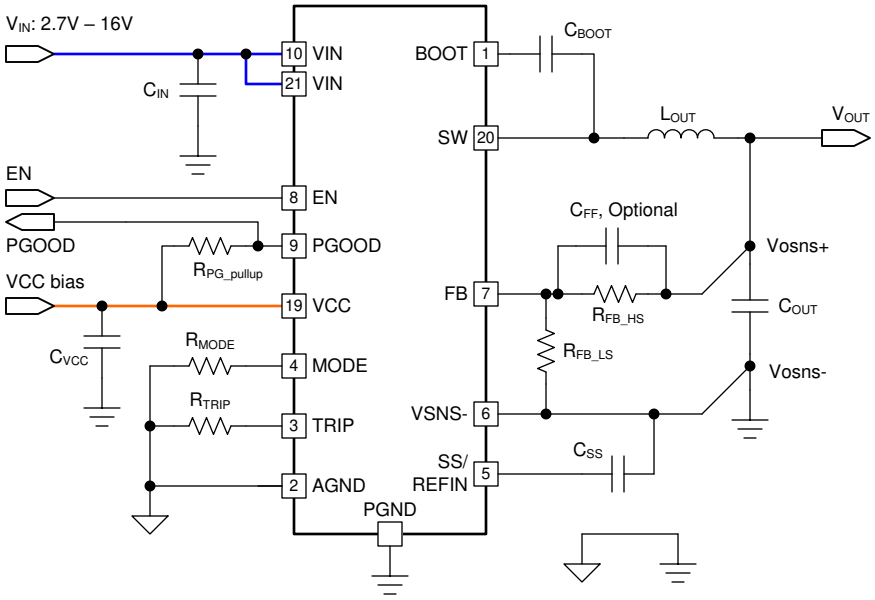


図 7-6. Split Rail Configuration With External VCC Bias

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8 Application and Implementation

Note

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8.1 Application Information

The TPS54JA20 device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device suits low output voltage point-of-load applications with 12-A or lower output current in server, storage, and similar computing applications. The TPS54JA20 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an ideal fashion. The output voltage ranges from 0.9 V to 5.5 V. The conversion input voltage ranges from 2.7 V to 16 V, and the VCC input voltage ranges from 3.13 V to 5.3 V. The D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require an external phase-compensation network, which makes the device easy-to-use and also allows for a low external component count. Another advantage of this control scheme is that it supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low-ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during a load-step transient.

8.2 Typical Application

The schematic shows a typical application for TPS54JA20. This example describes the design procedure of converting an input voltage range of 4-V to 16-V down to 2.5-V with a maximum output current of 12 A.

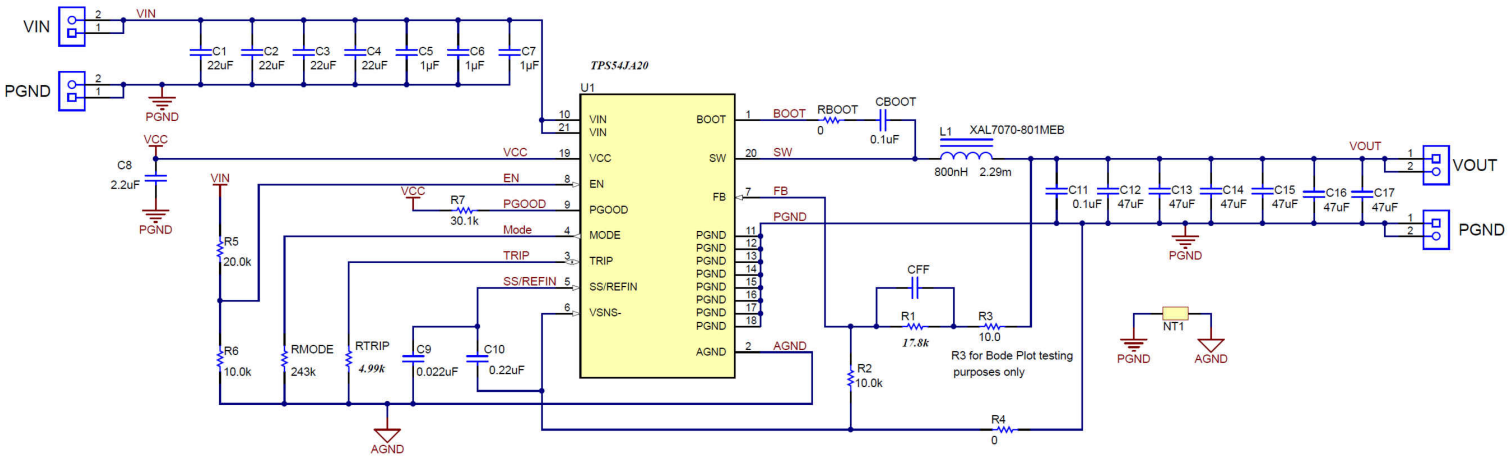


図 8-1. Application Circuit Diagram

8.2.1 Design Requirements

This design uses the parameters listed in 表 8-1.

表 8-1. Design Example Specifications

DESIGN PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Voltage range		4	12	16	V
V_{OUT}	Output voltage			2.5		V
ILOAD	Output load current				12	A
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 12 A		10		mV_{PP}
V_{TRANS}	Output voltage undershoot and overshoot after load step	I_{OUT} = 25% to 75% step, 2 A/µs slew rate		50		mV
I_{OVER}	Output overcurrent			12		A
t_{SS}	Soft-start time			5.5		ms
f_{SW}	Switching frequency			0.8		MHz
	Operating mode			Skip-mode		
T_A	Operating temperature			25		°C

8.2.2 Detailed Design Procedure

The external component selection is a simple process using D-CAP3 mode. Select the external components using the following steps.

8.2.2.1 Output Voltage Setting Point

The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in 式 7. Connect R1 between the FB pin and the output, and connect R2 between the FB pin and VSNS–. The recommended R2 value is 10 kΩ, but it can also be set to another value between the range of 1 kΩ to 20 kΩ. Determine R1 for TPS54JA20 by using 式 7 .

$$R1 = \frac{V_{OUT} - V_{INTREF}}{V_{INTREF}} \times R2 = \frac{2.5V - 0.9V}{0.9V} \times 10k\Omega = 17.8\,k\Omega \tag{7}$$

8.2.2.2 Choose the Switching Frequency and the Operation Mode

The switching frequency and operation mode are configured by the resistor on MODE pin. Select one of three switching frequencies: 600 kHz, 800 kHz, or 1 MHz. Refer to 表 7-1 for the relationship between the switching frequency, operation mode and R_{MODE}.

Switching frequency selection is a tradeoff between higher efficiency and smaller system solution size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, a 243-kΩ resistor is chosen for MODE pin to set the switching frequency to 0.8 MHz and set operation mode as skip mode.

When selecting the switching frequency of a buck converter, the minimum on-time and minimum off-time must be considered. 式 8 calculates the maximum f_{SW} before being limited by the minimum on-time. When hitting the minimum on-time limits of a converter with D-CAP3 control, the effective switching frequency will change to keep the output voltage regulated. This calculation ignores resistive drops in the converter to give a worst case estimation.

$$f_{SW}(max) = \frac{V_{OUT}}{V_{IN}(max)} \times \frac{1}{t_{ON_MIN}(max)} = \frac{2.5\ V}{16\ V} \times \frac{1}{85\ ns} = 1838\ kHz \tag{8}$$

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式 8 calculates the maximum f_{SW} before being limited by the minimum off-time. When hitting the minimum off-time limits of a converter with D-CAP3 control, the operating duty cycle will max out and the output voltage will begin to drop with the input voltage. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the following step so this preliminary calculation assumes a resistance of 2.2 mΩ. If operating near the maximum f_{SW} limited by the minimum off-time, the variation in resistance across temperature must be considered when using 式 9. The selected f_{SW} of 800 kHz is below the two calculated maximum values.

$$f_{SW}(max) = \frac{V_{IN}(min) - V_{OUT} - I_{OUT}(max) \times \left(R_{DCR} + R_{DS(ON)_HS}\right)}{t_{OFF_MIN}(max) \times \left(V_{IN}(min) - I_{OUT}(max) \times \left(R_{DS(ON)_HS} - R_{DS(ON)_LS}\right)\right)}$$

$$f_{SW}(max) = \frac{8\ V - 2.5\ V - 12\ A \times (2.2\ m\Omega + 10.2\ m\Omega)}{220\ ns \times (8\ V - 12\ A \times (10.2\ m\Omega - 3.1\ m\Omega))} = 3020\ kHz \quad (9)$$

8.2.2.3 Choose the Inductor

To calculate the value of the output inductor (L_{OUT}), use 式 10. The output capacitor filters the inductor-ripple current ($I_{IND(ripple)}$). Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. On the other hand, larger ripple current increases output ripple voltage, but improves signal-to-noise ratio and helps to stabilize operation. Generally speaking, the inductance value should set the ripple current at approximately 15% to 40% of the maximum output current for a balanced performance.

For this design, the inductor-ripple current is set to 30% of 12-A output current. With a 0.8-MHz switching frequency, 16 V as maximum V_{IN}, and 2.5 V as the output voltage, the 式 10 calculated inductance is 0.732 µH. A nearest standard value of 0.80 µH is chosen.

$$L = \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{I_{RIPPLE} \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 2.5\ V) \times 2.5\ V}{0.3 \times 12A \times 16\ V \times 800\ kHz} = 0.732\ \mu H \quad (10)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using 式 12. For this design, by selecting 4.99 kΩ as the R_{TRIP}, $I_{OC(valley)}$ is set to 12.8 A, thus peak inductor current under maximum V_{IN} is calculated as 13.65 A.

$$I_{RIPPLE} = \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 2.5\ V) \times 2.5\ V}{0.8\ \mu H \times 16\ V \times 800\ kHz} = 3.3\ A \quad (11)$$

$$I_{L(PEAK)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 12\ A + \frac{3.3\ A}{2} = 13.65\ A \quad (12)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}} = \sqrt{12\ A^2 + \frac{3.3\ A^2}{12}} = 12.04\ A \quad (13)$$

The selected inductance is a XAL7070-801MEB. This has a saturation current rating of 37.8 A, RMS current rating of 20.8 A and a DCR of 2.29 mΩ max. This inductor was selected for its low DCR to get high efficiency.

8.2.2.4 Set the Current Limit (TRIP)

The R_{TRIP} resistor sets the valley current limit. 式 14 calculates the recommended current limit target. This includes the tolerance of the inductor. 式 15 calculates the R_{TRIP} resistor to set the current limit. The typical valley current limit target is 10.66 A. Round up to use a valley current limit of 12 A. The closest standard value for R_{TRIP} is 4.99 kΩ.

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$$I_{LIM_VALLEY} = I_{OUT} - \frac{1}{2} \times \frac{(V_{IN}(min) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(min) \times f_{SW}}$$

$$I_{LIM_VALLEY} = 12\ A - \frac{1}{2} \times \frac{(8\ V - 2.5\ V) \times 2.5\ V}{0.8\ \mu H \times 8\ V \times 800\ kHz} = 10.66\ A \quad (14)$$

$$R_{TRIP} = \frac{60000}{I_{LIM_VALLEY}} = \frac{60000}{12\ A} = 5.0\ k\Omega \quad (15)$$

With the current limit set, 式 16 calculates the typical maximum output current at current limit. 式 17 calculates the typical peak current at current limit. As mentioned in *セクション 8.2.2.3*, the saturation behavior of the inductor at the peak current during current limit must be considered. For worst case calculations, the tolerance of the inductance and the current limit must be included.

$$I_{OUT_LIM}(min) = I_{LIM_VALLEY} + \frac{1}{2} \times \frac{(V_{IN}(min) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(min) \times f_{SW}} = 12\ A + \frac{1}{2} \times \frac{(8\ V - 2.5\ V) \times 2.5\ V}{0.8\ \mu H \times 8\ V \times 800\ kHz} = 13.34\ A \quad (16)$$

$$I_{L(PEAK)} = I_{LIM_VALLEY} + \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = 12\ A + \frac{(16\ V - 2.5\ V) \times 2.5\ V}{0.8\ \mu H \times 16\ V \times 800\ kHz} = 15.30\ A \quad (17)$$

8.2.2.5 Choose the Output Capacitor

There are three considerations for selecting the value of the output capacitor.

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

First, the minimum output capacitance should be calculated based on these three requirements. 式 18 calculates the minimum capacitance to keep the LC double pole below 1/30th the f_{SW} in order to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero. 式 19 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 10 mV. This calculation is for CCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors.

$$C_{OUT_STABILITY} > \left(\frac{30}{2\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{30}{2\pi \times 800\ kHz}\right)^2 \times \frac{1}{0.8\ \mu H} = 44.5\ \mu F \quad (18)$$

$$C_{OUT_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times f_{SW}} = \frac{4.12\ A}{8 \times 10\ mV \times 800\ kHz} = 64.4\ \mu F \quad (19)$$

式 20 and 式 21 calculate the minimum capacitance to meet the transient response requirement of 50 mV with a 6-A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step.

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$$C_{OUT_UNDERSHOOT} > \frac{L \times I_{STEP}^2 \times \left(\frac{V_{OUT}}{V_{IN}(min) \times f_{SW}} + t_{OFF_MIN}(max) \right)}{2 \times V_{TRANS} \times V_{OUT} \times \left(\frac{V_{IN}(min) - V_{OUT}}{V_{IN}(min) \times f_{SW}} - t_{OFF_MIN}(max) \right)}$$

$$C_{OUT_UNDERSHOOT} > \frac{0.8\ \mu H \times 6\ A^2 \times \left(\frac{2.5\ V}{8\ V \times 800\ kHz} + 220\ ns \right)}{2 \times 50\ mV \times 2.5\ V \times \left(\frac{8\ V - 2.5\ V}{8\ V \times 800\ kHz} - 220\ ns \right)} = 110\ \mu F \quad (20)$$

$$C_{OUT_OVERSHOOT} > \frac{L \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{0.8\ \mu H \times 6A^2}{2 \times 50\ mV \times 2.5\ V} = 115.2\ \mu F \quad (21)$$

The output capacitance needed to meet the overshoot requirement is the highest value so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance and 式 22 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the f_{SW}. It is possible to use more output capacitance but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 6 x 47-µF, 6.3-V ceramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to 60% their nominal value giving an effective total capacitance of 169.2 µF. This effective capacitance meets the minimum and maximum requirements.

$$C_{OUT_STABILITY} < \left(\frac{50}{\pi \times f_{SW}} \right)^2 \times \frac{1}{L} = \left(\frac{50}{\pi \times 800\ kHz} \right)^2 \times \frac{1}{0.8\ \mu H} = 494\ \mu F \quad (22)$$

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If you are using non-ceramic capacitors, as a starting point, the ESR should be below the values calculated in 式 23 to meet the ripple requirement and 式 24 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors should be used to determine if the ripple and transient requirements can be met.

$$R_{ESR_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{10\ mV}{4.1\ A} = 2.5\ m\Omega \quad (23)$$

$$R_{ESR_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{50\ mV}{6\ A} = 8.3\ m\Omega \quad (24)$$

8.2.2.6 Choose the Input Capacitors (C_{IN})

The device requires input bypass capacitors between the VIN and PGND pins to bypass the power-stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout will allow. At least 10 µF of ceramic capacitance and 1-µF high frequency ceramic bypass capacitors are required. A 1-µF, 16-V X6S size 0402 ceramic capacitor on VIN pin 21 is required. A 1-µF, 16-V X6S ceramic capacitor on VIN pin 10 is required. A 1-µF 16-V X6S ceramic capacitor on the bottom layer is recommended for high current applications. The high frequency bypass capacitor minimizes high frequency voltage overshoot across the power-stage. The ceramic capacitors must be high-quality dielectric of X6S or better for their high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

The input capacitance required to meet a specific input ripple target can be calculated with 式 25. A recommended target input voltage ripple is 5% the minimum input voltage, 400 mV in this example. The calculated input capacitance is 8.06 µF and the minimum input capacitance of 10 µF exceeds this. This example meets these two requirements with 4 x 22-µF ceramic capacitors.

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$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}(min)}\right)}{f_{SW} \times V_{IN}(min) \times V_{IN_RIPPLE}} = \frac{2.5\ V \times 12\ A \times \left(1 - \frac{2.5}{8}\right)}{800\ kHz \times 8\ V \times 400\ mV} = 8.06\ \mu F \quad (25)$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. The input RMS current the input capacitors must support is calculated by 式 26 and is 5.57 A in this example. The ceramic input capacitors have a current rating greater than this.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}(min)} \times \left(\frac{\left(V_{IN}(min) - V_{OUT}\right)}{V_{IN}(min)} \times {I_{OUT}}^2 + \frac{Iripple^2}{12}\right)} =$$

$$I_{CIN(RMS)} = \sqrt{\frac{2.5\ V}{8\ V} \times \left(\frac{(8\ V - 2.5\ V)}{8\ V} \times 12^2 + \frac{4.12^2}{12}\right)} = 5.57\ A \quad (26)$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, the selection process in the *How To Select Input Capacitors For A Buck Converter* technical brief is recommended.

8.2.2.7 Soft Start Capacitor (SS/REFIN Pin)

The capacitor placed on the SS/REFIN pin can be used to extend the soft start time past the internal 1.5-ms soft start. This example uses a 5.5-ms soft start time and the required external capacitance can be calculated with 式 27. In this example a 220-nF capacitor is used.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} = \frac{36\ \mu A \times 5.5\ ms}{0.9\ V} = 220\ nF \quad (27)$$

A minimum capacitor value of 1 nF is required at the SS/REFIN pin. The SS/REFIN capacitor must use the VSNS– pin for its ground.

8.2.2.8 EN Pin Resistor Divider

A resistor divider on the EN pin can be used to increase the input voltage the converter begins its start-up sequence. To set the start voltage, first select the bottom resistor (R_{EN_B}). The recommended value is between 1 kΩ and 100 kΩ. There is an internal pulldown resistance with a nominal value of 6 MΩ and this must be included for the most accurate calculations. This is especially important when the bottom resistor is a higher value, near 100 kΩ. This example uses a 10-kΩ resistor and this combined with the internal resistance in parallel, results in an equivalent bottom resistance of 9.98 kΩ. The top resistor value for the target start voltage is calculated with 式 28. In this example, the nearest standard value of 20 kΩ is selected for R_{EN_T}. When selecting a start voltage in a wide input range application, be cautious that the EN pin absolute maximum voltage of 6 V is not exceeded.

$$R_{EN_T} = \frac{R_{EN_B} \times V_{START}}{V_{ENH}} - R_{EN_B} = \frac{10\ k\Omega \times 3.7\ V}{1.22\ V} - 10\ k\Omega = 20\ k\Omega \quad (28)$$

The start and stop voltages with the selected EN resistor divider can be calculated with 式 29 and 式 30.

$$V_{START} = V_{ENH} \times \frac{R_{EN_B} + R_{EN_T}}{R_{EN_B}} = 1.22\ V \times \frac{10\ k\Omega + 20\ k\Omega}{10\ k\Omega} = 3.66V \quad (29)$$

$$V_{STOP} = V_{ENL} \times \frac{R_{EN_B} + R_{EN_T}}{R_{EN_B}} = 1.02\ V \times \frac{10\ k\Omega + 20\ k\Omega}{10\ k\Omega} = 3.06\ V \quad (30)$$

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8.2.2.9 VCC Bypass Capacitor

At a minimum, a 2.2-µF, at least 6.3-V rating, X5R ceramic bypass capacitor is needed on VCC pin located as close to the pin as the layout will allow.

8.2.2.10 BOOT Capacitor

At a minimum, a 0.1-µF 10-V X5R ceramic bypass capacitor is needed between the BOOT and SW pins located as close to the pin as the layout will allow. It is good practice to use a 0-Ω resistor in series with BOOT capacitor.

8.2.2.11 PGOOD Pullup Resistor

The PGOOD pin is open-drain so a pullup resistor is required when using this pin. The recommended value is between 1 kΩ and 100 kΩ.

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8.2.3 Application Curves

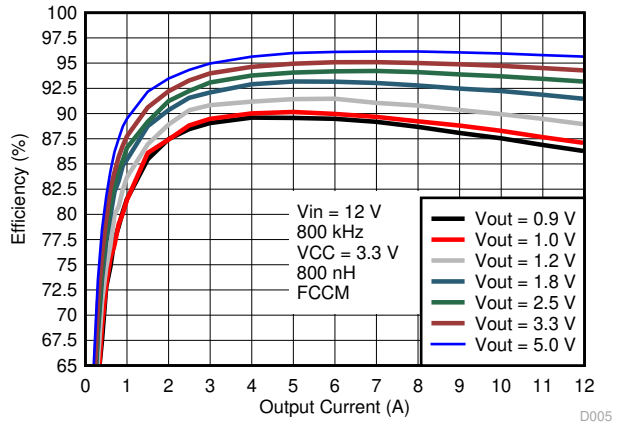


図 8-2. Efficiency vs Output Current, VCC = 3.3V External VCC Bias

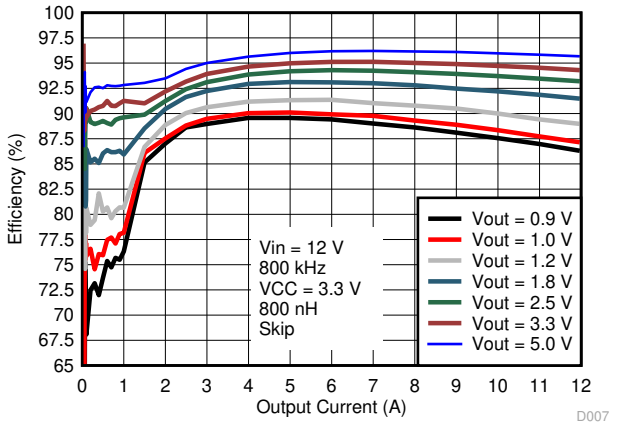


図 8-3. Efficiency vs Output Current, VCC = 3.3V External VCC Bias

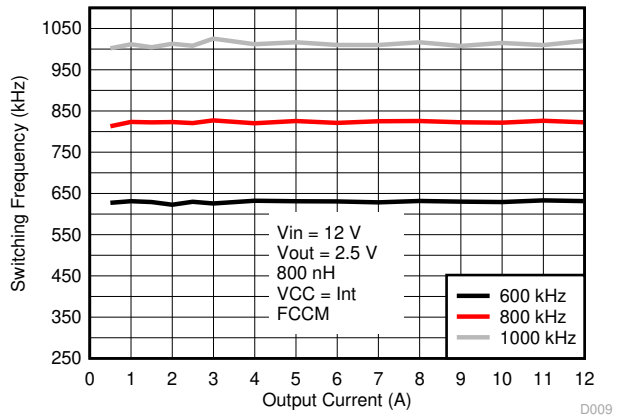


図 8-4. Switching Frequency vs Output Current

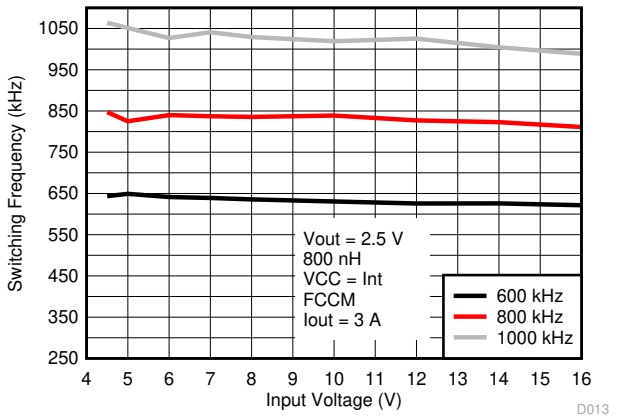


図 8-5. Switching Frequency vs Input Voltage

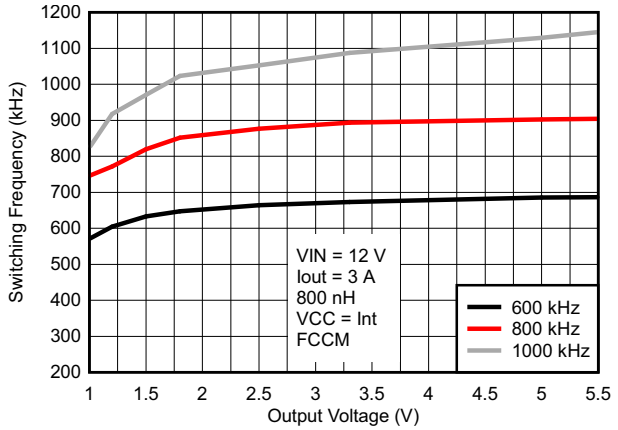


図 8-6. Switching Frequency vs Output Voltage

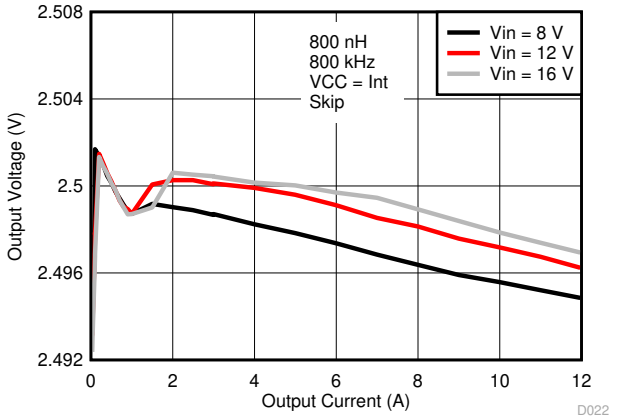


図 8-7. Output Voltage vs Output Current

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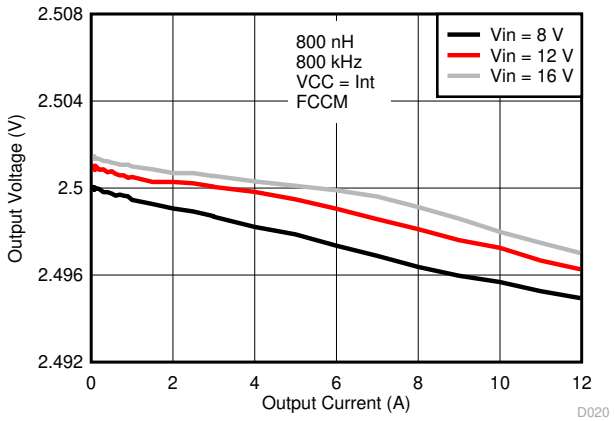


図 8-8. Output Voltage vs Output Current

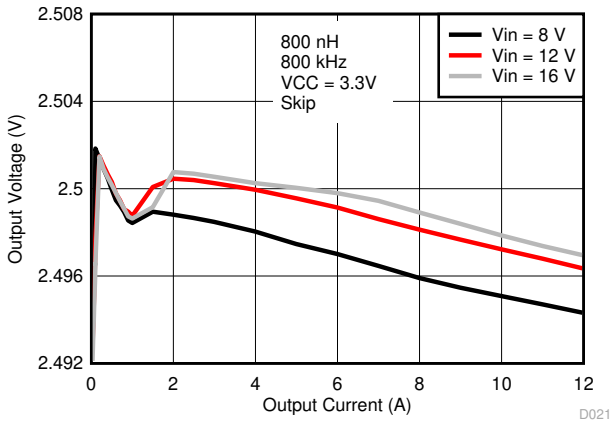


図 8-9. Output Voltage vs Output Current, VCC = 3.3V External Bias

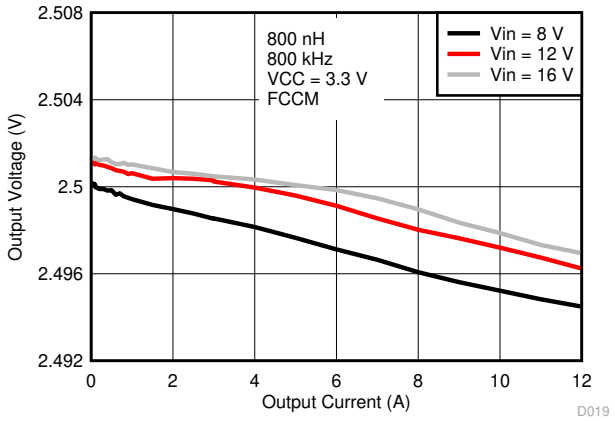


図 8-10. Output Voltage vs Output Current, VCC = 3.3V External Bias

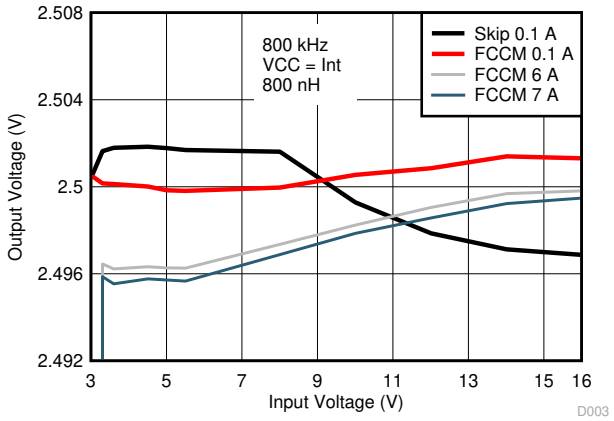


図 8-11. Output Voltage vs Input Voltage VCC = Int

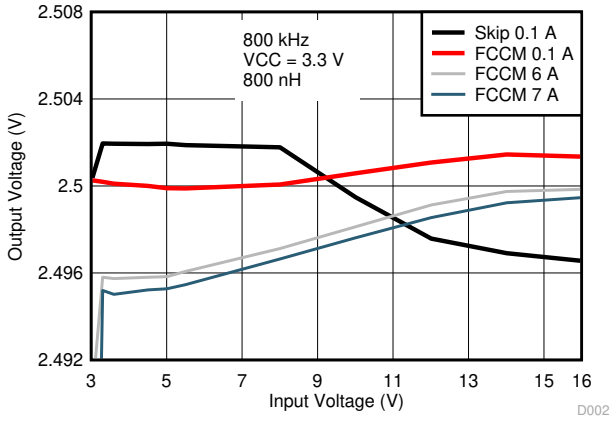


図 8-12. Output Voltage vs Input Voltage VCC = 3.3 V External Bias

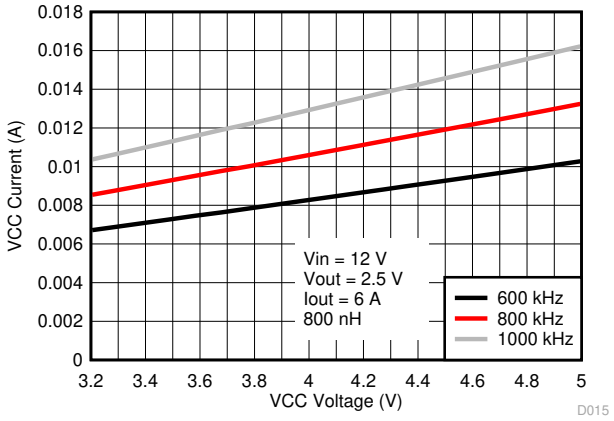


図 8-13. ICC Current vs External VCC Voltage

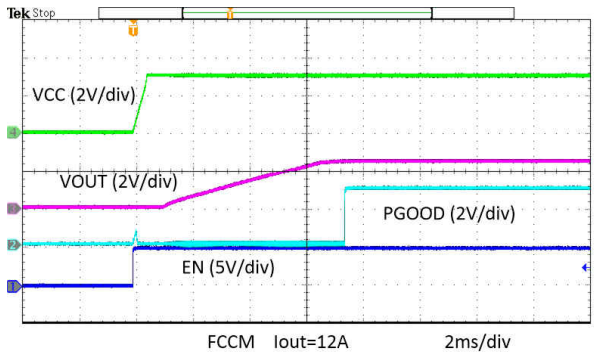


図 8-14. Enable Start-Up, Full Load

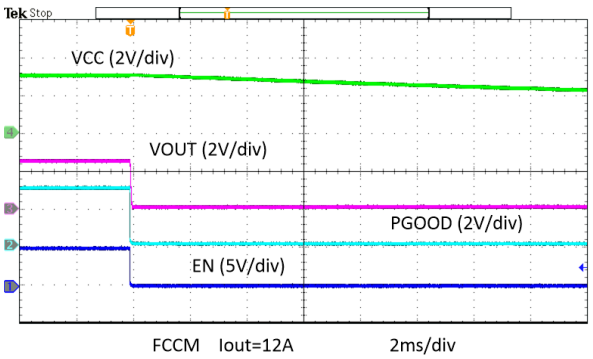


図 8-15. Enable Power Down Full Load

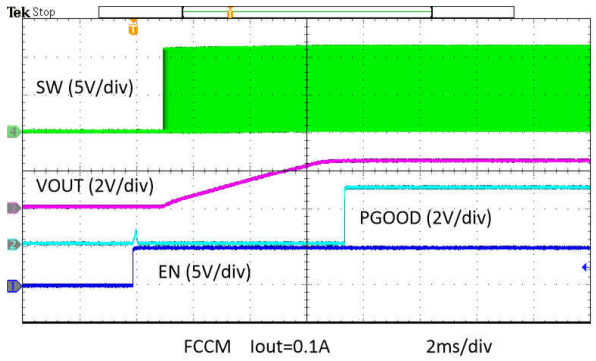


図 8-16. Enable to Power Up Iout = 0.1 A

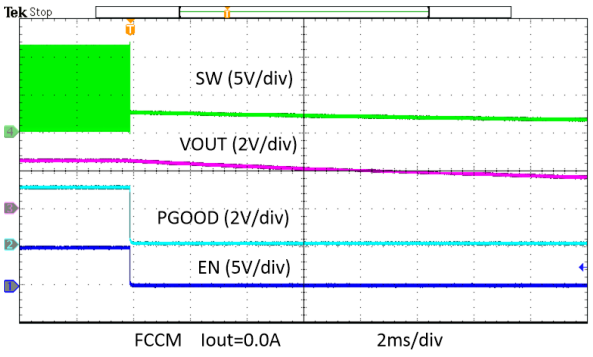


図 8-17. Enable to over Down Iout = 0 A

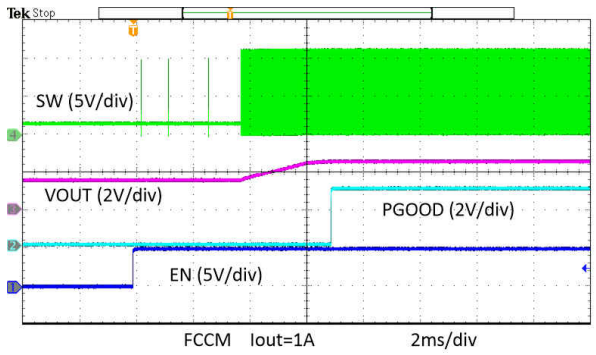


図 8-18. Enable Start-Up, Prebias

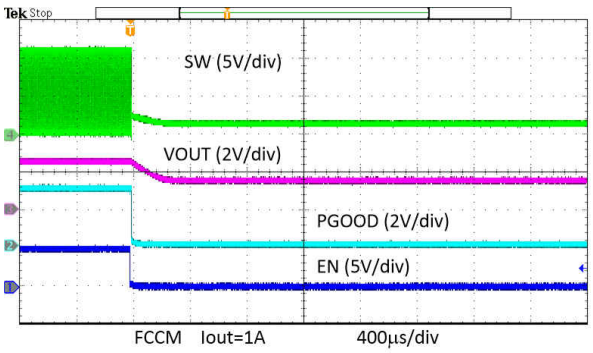


図 8-19. Prebias Power Up

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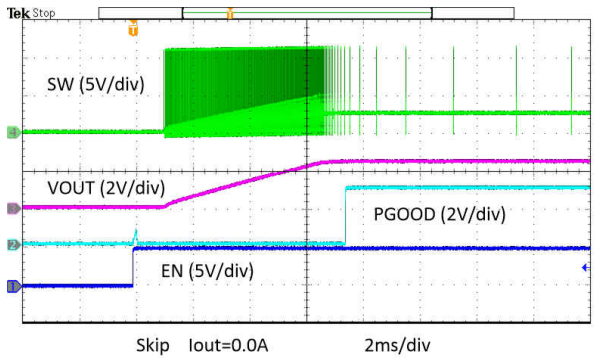


図 8-20. Enable Power Up, Skip

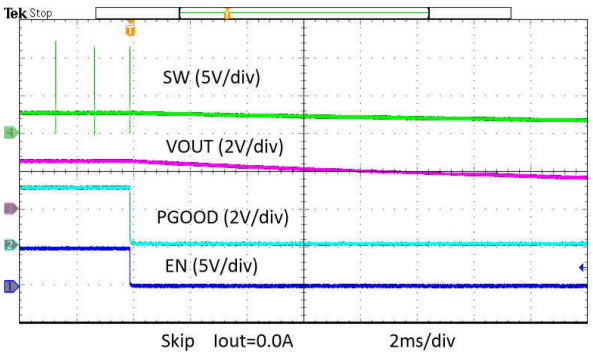


図 8-21. Enable Power Down, Skip

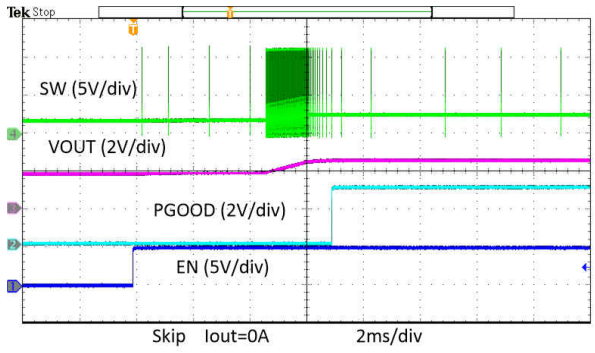


図 8-22. Enable Power Up into Pre-bias, Skip

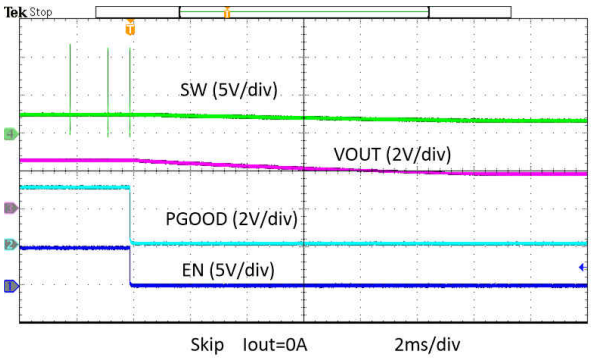


図 8-23. Enable Power Down with Pre-bias, Skip

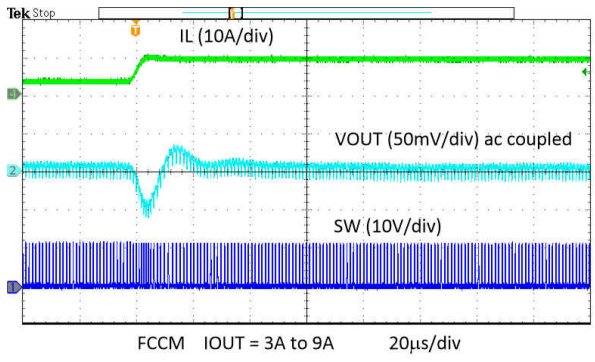


図 8-24. FCCM Mode Load Transient

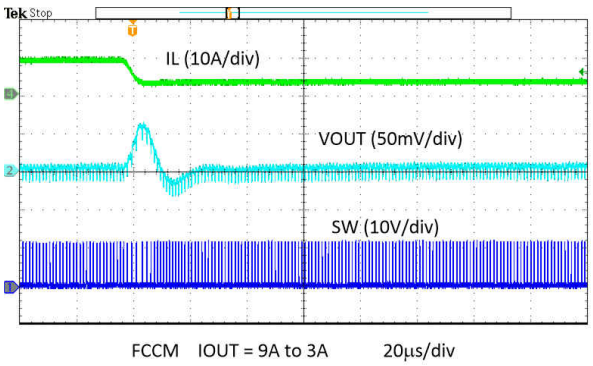


図 8-25. Unload Transient

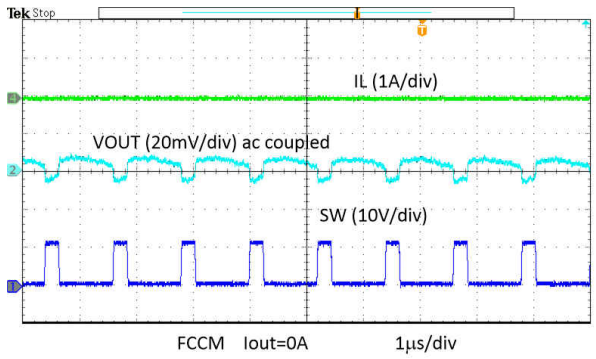


図 8-26. Output Voltage Ripple

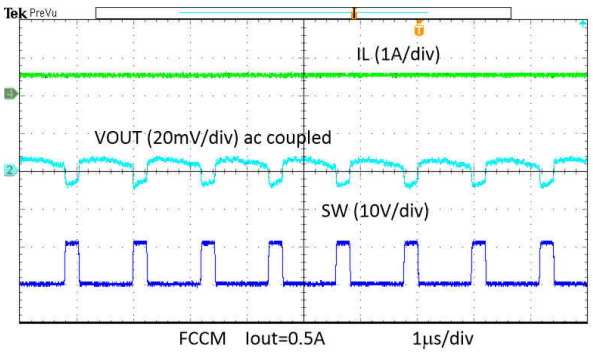


図 8-27. Output Voltage Ripple

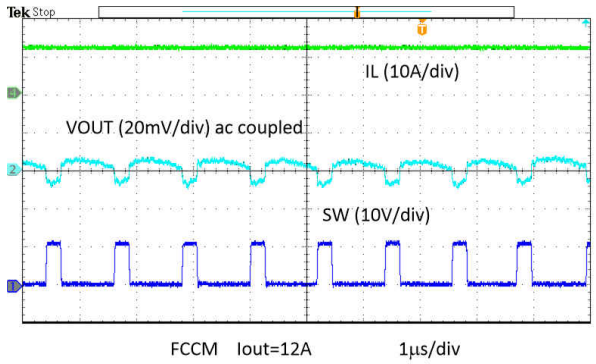


図 8-28. Output Voltage Ripple

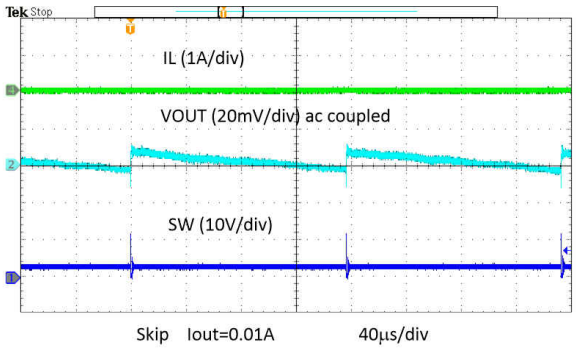


図 8-29. Output Voltage Ripple, Skip

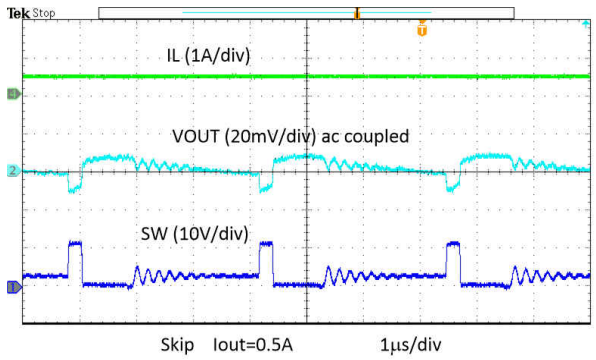


図 8-30. Output Voltage Ripple, Skip

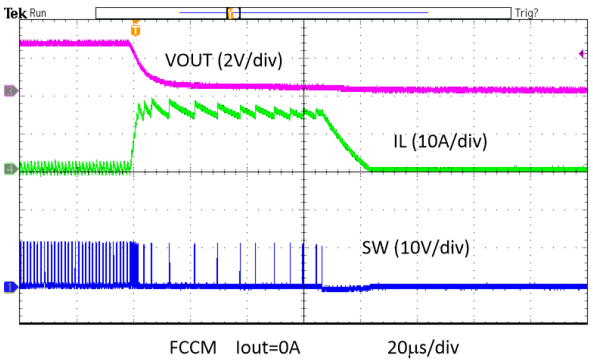


図 8-31. Over Current Protection

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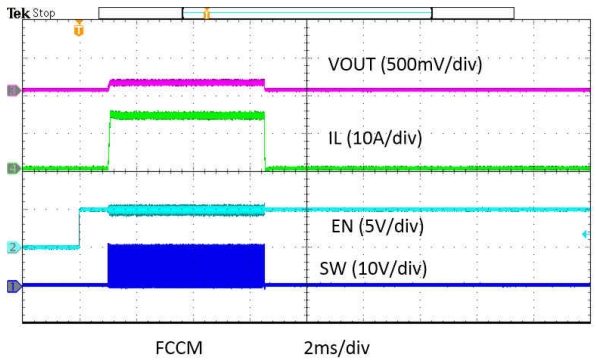


図 8-32. Enable into Overcurrent

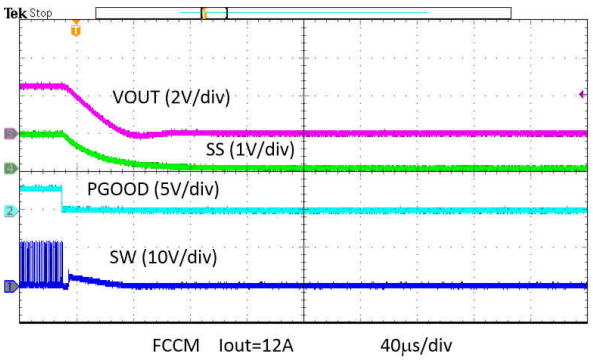


図 8-33. Over Temperature Protection in FCCM

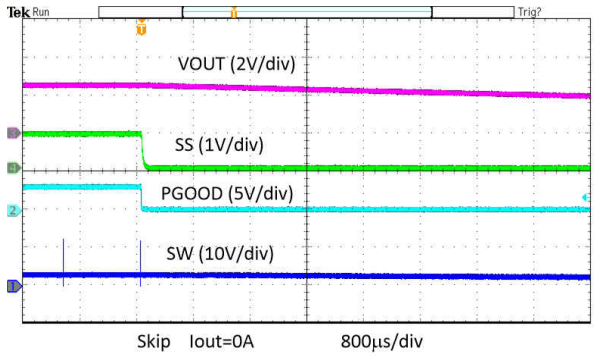


図 8-34. Over Temperature Protection in Skip

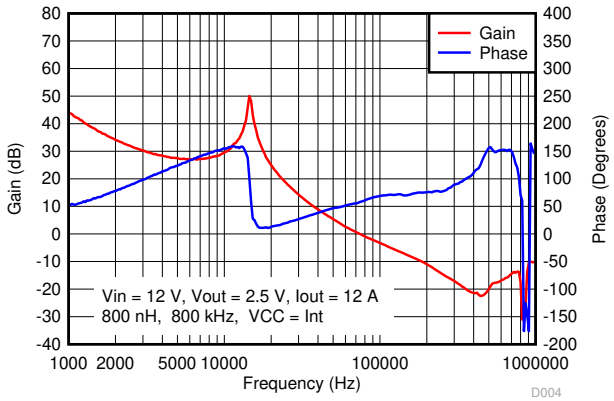


図 8-35. Frequency Response, 12-A Load

9 Power Supply Recommendations

The device is designed to operate from a wide input voltage supply range between 2.7 V and 16 V when the VCC pin is powered by external bias ranging from 3.13 V to 5.3 V. Both input supplies (V_{IN} and VCC bias) must be well regulated. Proper bypassing of input supplies (V_{IN} and VCC bias) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *セクション 10*.

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10 Layout

10.1 Layout Guidelines

Before beginning a design using the device, consider the following:

- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- V_{IN} decoupling capacitors are important for FET robustness. A 1-µF/25-V/X6S/0402 ceramic capacitor on VIN pin 21 is required. The PGND vias for this decoupling capacitor should be placed so that the decoupling capacitor is closer to IC than the PGND vias. To lower ESL from via connection, two 8-mil vias are recommended for the PGND connection to inner PGND plane.
- A 1-µF/25-V/X6S/0402 ceramic capacitor on VIN pin 10 is highly recommended. If this 0402 size capacitor is not used, the bigger size V_{IN} decoupling capacitors (0603 or 0805 size) are required to be placed as close as possible to IC pin 10 and pin 11.
- Two 1-µF/25-V/X6S/0402 ceramic capacitors on the bottom layer are recommended for high current applications (I_{OUT} > 13 A). One of these two capacitors should be centered between VIN pin 10 and pin 21. To have good connection for this capacitor, a V_{IN} copper on the bottom layer and two V_{IN} vias are needed. The other one can be placed close to IC package just like a mirrored copy to the 0402 capacitor on top layer.
- At least six PGND vias are required to be placed as close as possible to the PGND pins (pin 11 to pin 15). This minimizes parasitic impedance and also lowers thermal resistance.
- Place the VCC decoupling capacitor (2.2-µF/6.3-V/X6S/0402 or 2.2-µF/6.3-V/X7R/0603) as close as possible to the device. Ensure the VCC decoupling loop is smallest.
- Place a BOOT capacitor as close as possible to the BOOT and SW pins. Use traces with a width of 12 mil or wider to route the connection. TI recommends using a 0.1-µF to 1-µF bootstrap capacitor with a 10-V rating.
- The PCB trace, which connects the SW pin and high-voltage side of the inductor, is defined as switch node. The switch node must be as short and wide as possible.
- Always place the feedback resistors near the device to minimize the FB trace distance, no matter single-end sensing or remote sensing.
  - For remote sensing, the connections from the FB voltage divider resistors to the remote location should be a pair of PCB traces with at least 12-mil trace width, and should implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher. The ground connection of the remote sensing signal must be connected to VSNS– pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VSNS– pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines should stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. It is recommended to shield the pair of remote sensing lines with ground planes above and below.
  - For single-end sensing, connect the higher FB resistor to a high-frequency local bypass capacitor of 0.1 µF or higher, and short VSNS– to AGND with shortest trace.
- This device does not require a capacitor from rgw SS/REFIN pin to AGND, thus it is not recommenced to place a capacitor from SS/REFIN pin to AGND. If both $C_{SS/REFIN}$-to-VSNS– and $C_{SS/REFIN}$-to-AGND capacitors exist, place $C_{SS/REFIN}$-to-VSNS– more closely with shortest trace to VSNS– pin.
- Pin 2 (AGND pin) must be connected to a solid PGND plane on inner layer. Use the common AGND via to connect the resistors to the inner ground plane if applicable.
- See 図 10-1 for the layout recommendation.

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10.2 Layout Example

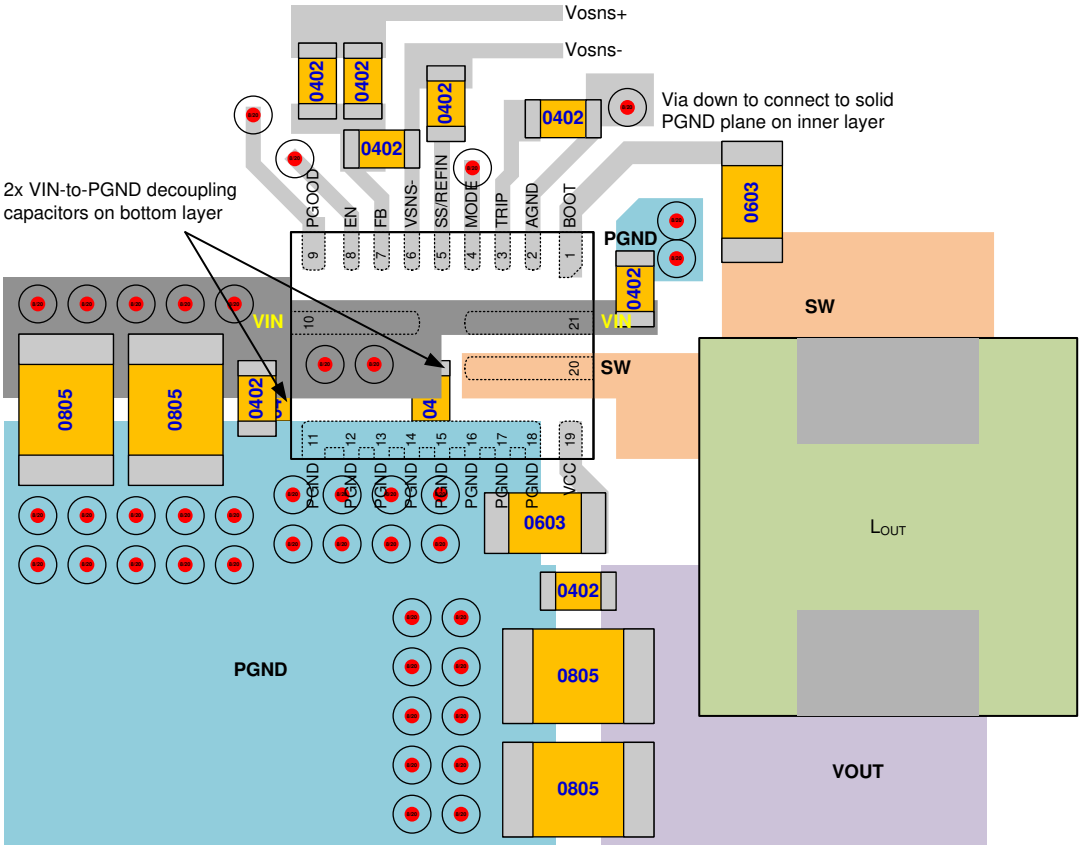


図 10-1. Layout Recommendation

10.2.1 Thermal Performance On TI EVM

Test conditions:

f_{SW} = 800 kHz, V_{IN} = 12 V, VCC = Int LDO, V_{OUT} = 1 V, I_{OUT} = 15 A, Inductor L_{OUT} = 0.8 µH (2.29 mΩ typ), C_{OUT} = 6 × 22 µF (1206/6.3 V/X7R), no R_{BOOT}, no RC Snubber

SP1 (IC): 75.4°C, SP2 (Inductor): 53.3°C

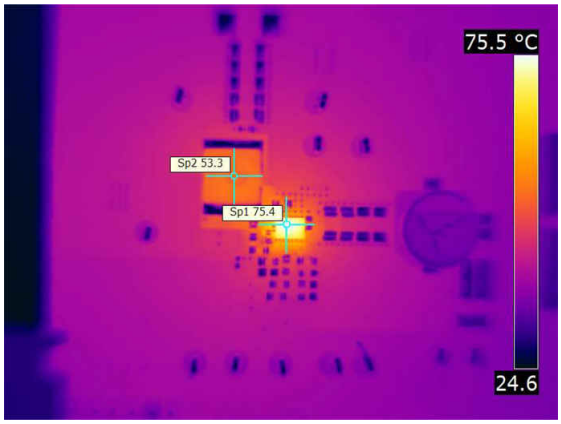


図 10-2. Thermal Image At 25°C Ambient

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *Optimizing transient response of internally compensated dc-dc converters with feedforward capacitor*
- Texas Instruments, *Non-isolated point-of-load solutions for VR13.HC in rack server and datacenter applications*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54JA20RWWR	Active	Production	VQFN-HR (RWW) | 21	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	T54JA20
TPS54JA20RWWR.A	Active	Production	VQFN-HR (RWW) | 21	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T54JA20
TPS54JA20RWWR.B	Active	Production	VQFN-HR (RWW) | 21	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T54JA20

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

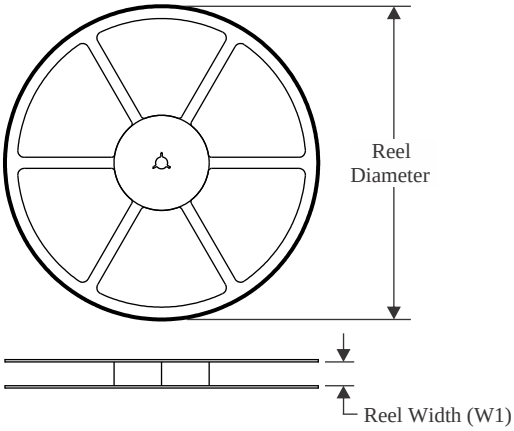
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

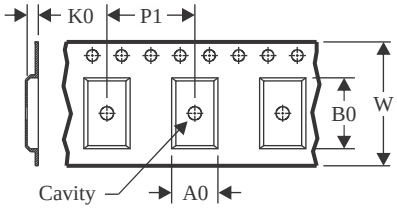
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

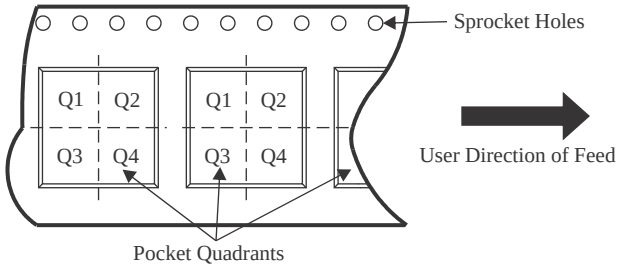


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

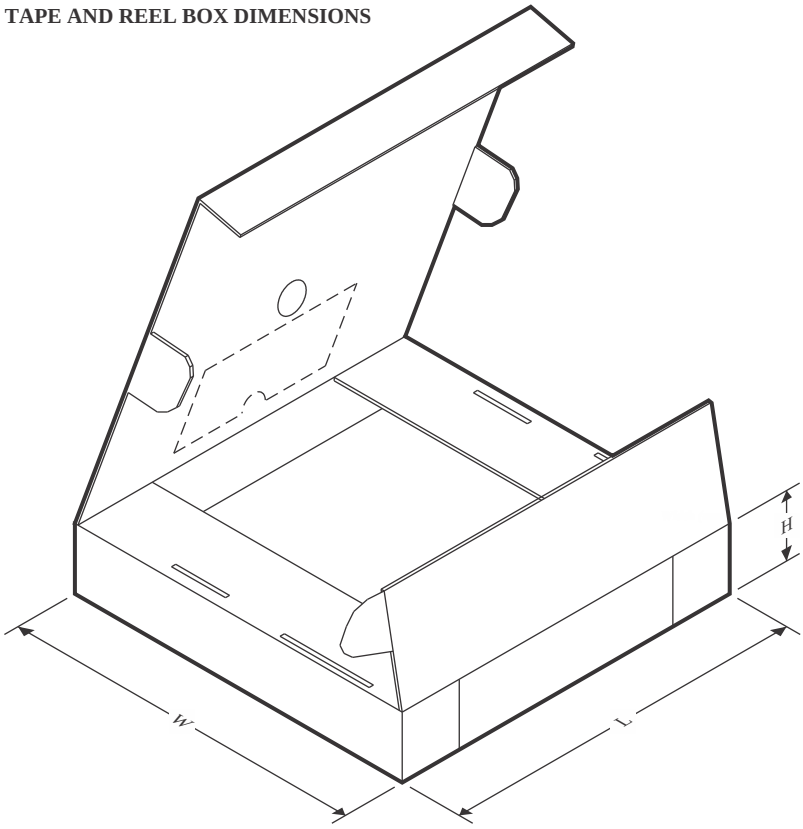
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54JA20RWWR	VQFN-HR	RWW	21	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS54JA20RWWR	VQFN-HR	RWW	21	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

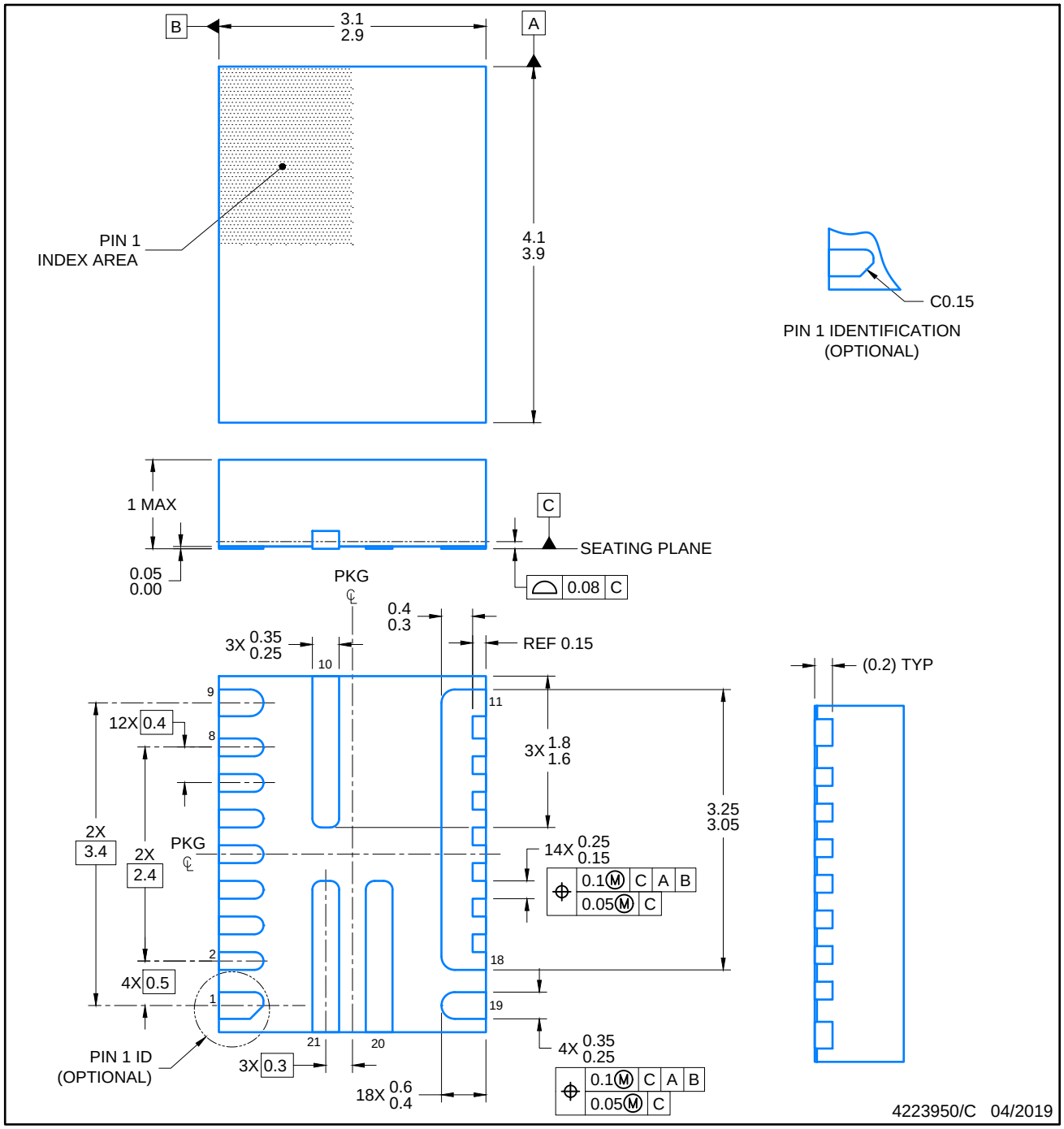
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54JA20RWWR	VQFN-HR	RWW	21	3000	360.0	360.0	36.0
TPS54JA20RWWR	VQFN-HR	RWW	21	3000	346.0	346.0	80.0

PACKAGE OUTLINE

RWW0021A

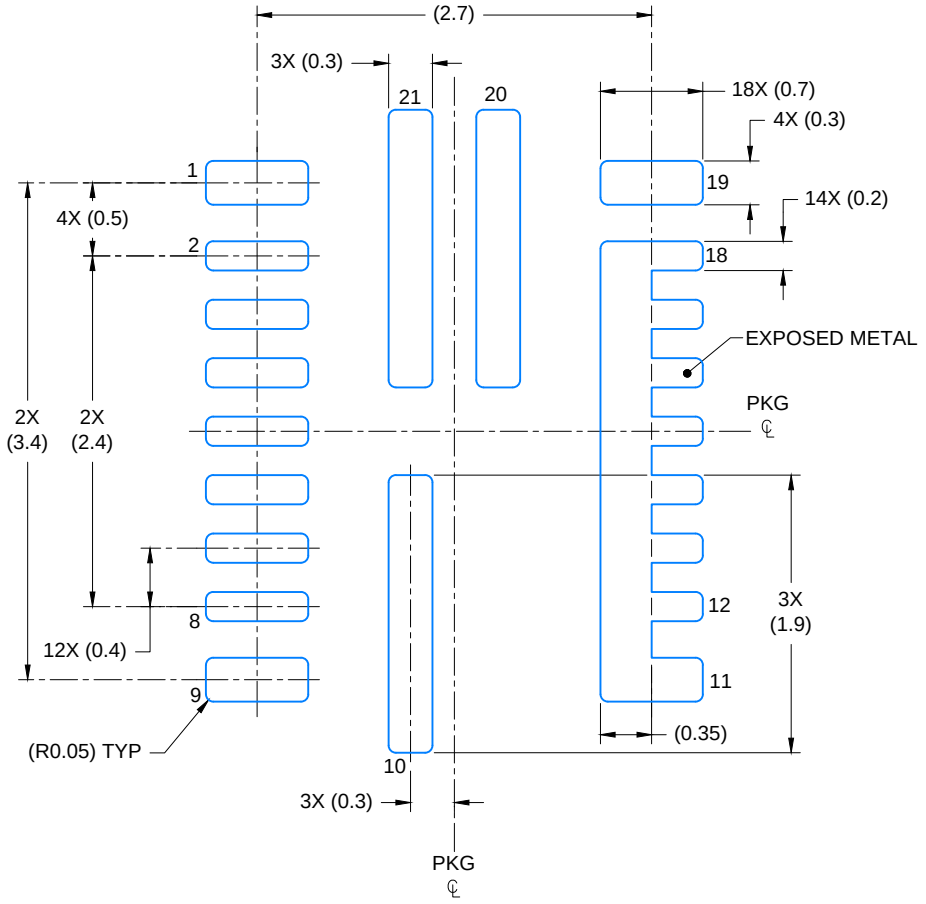
VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD

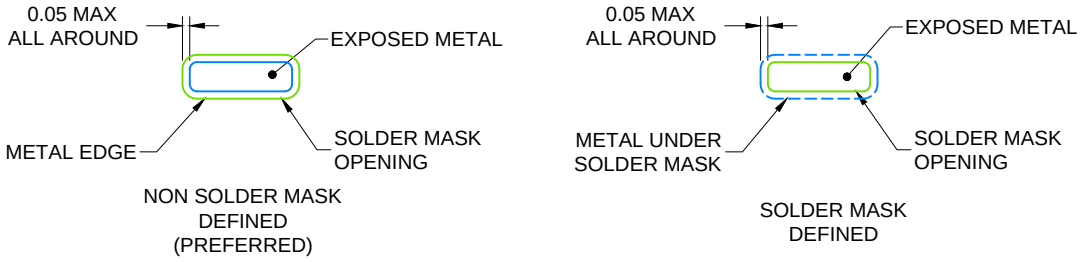


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 20X

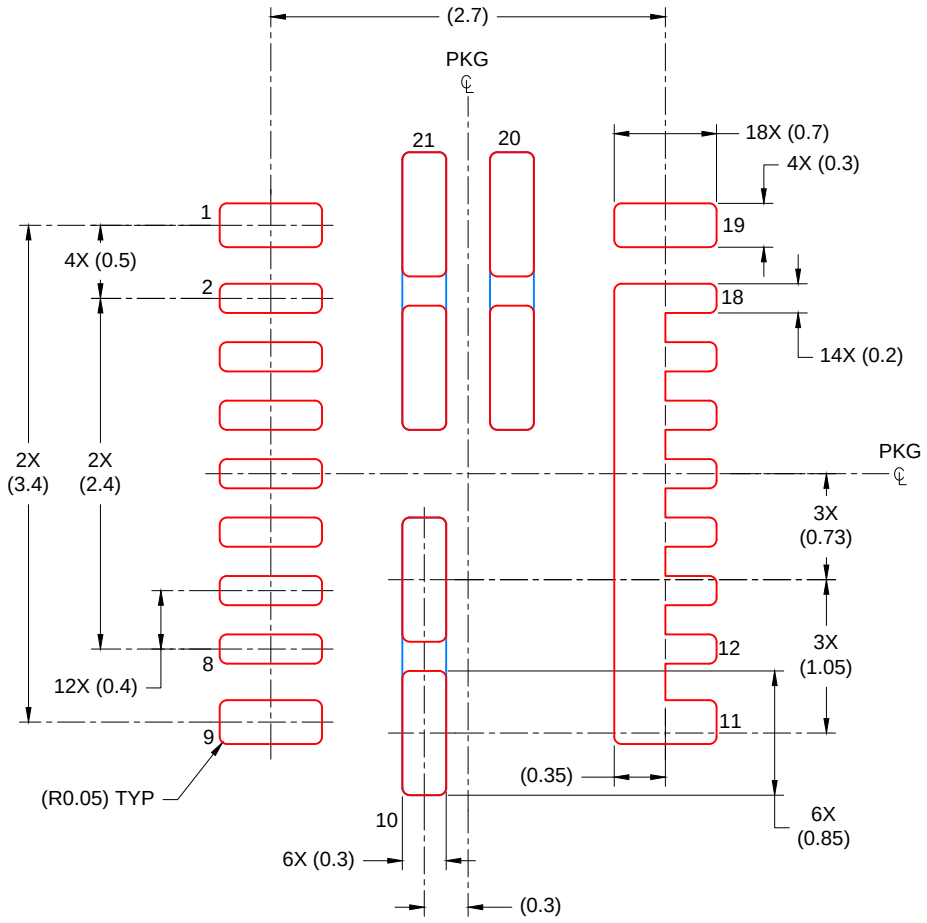


SOLDER MASK DETAILS

4223950/C 04/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
89% PRINTED COVERAGE BY AREA
SCALE: 20X

4223950/C 04/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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