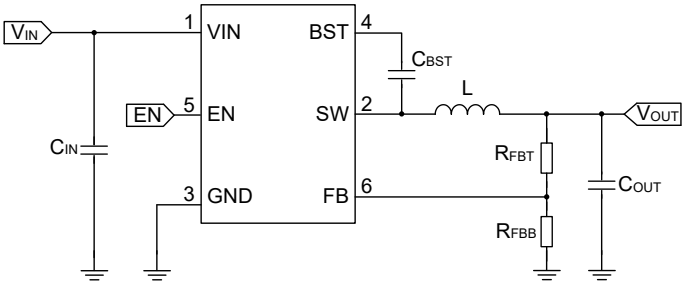
TPS562242 3V～17V 入力、2A 同期整流降圧コンバータ、SOT-563 パッケージ

1 特長

- 多様なアプリケーションに適した構成
  - 3V～17V の入力電圧範囲
  - 0.8V～10V の出力電圧範囲
  - 0.8V の基準電圧
  - 25℃で ±1% の基準電圧精度
  - -40℃～125℃で ±1.5% の基準電圧精度
  - 55.0mΩ および 24.3mΩ の MOSFET を内蔵
  - 100μA の Low 静止電流
  - スイッチング周波数:1.4MHz
  - 最大 94% の高デューティ・サイクル動作
  - 高精度の EN スレッショルド電圧
  - 1.6ms (標準値) の固定ソフトスタート時間
- 使いやすく小さいソリューション・サイズ
  - 軽負荷時の Eco モード
  - TPS562202 とピン互換
  - D-CAP3™ 制御モード
  - あらかじめ出力にバイアスが印加された状態でのスタートアップをサポート
  - ラッチなしの OV/OT/UVLO 保護
  - ヒカップ・モードによる UV 保護
  - サイクル単位の OC 保護
  - 1.6mm × 1.6mm の SOT-563 パッケージ
- WEBENCH® Power Designer により、TPS562242 を使用するカスタム設計を作成

2 アプリケーション

- 家電製品、ビデオ・レコーダ
- WLAN/Wi-Fi アクセス・ポイント、モデム (ケーブル / DSL / GFAST)、小規模企業向けルータ
- TV、STB および DVR



簡素化されたアプリケーション

3 概要

TPS562242 は、3V～17V の入力電圧範囲を持つシンプルで使いやすい高効率、高電力密度の同期整流降圧コンバータであり、0.8V～10V の出力電圧において最大 2A の連続電流に対応します。

TPS562242 は、過渡応答を高速化するため、かつ外部補償を行わなくても低 ESR 出力コンデンサが使えるように、D-CAP3 制御モードを採用しています。このデバイスは、最大 94% のデューティでの動作をサポートできます。

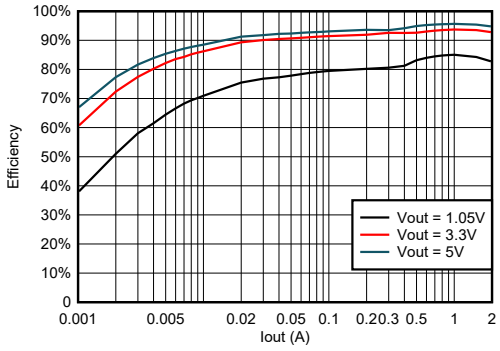
TPS562242 は Eco モードで動作することで、軽負荷時も高い効率を維持します。このデバイスは、OVP、OCP、UVLO、OTP、UVP (ヒカップ機能付き) による完全な保護機能を備えています。

このデバイスは、1.6mm × 1.6mm SOT-563 パッケージで供給されます。接合部温度の仕様は -40℃～125℃です。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS562242	DRL (SOT-563、6)	1.60mm × 1.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TPS562242 の効率 (V_{IN} = 12V 時)

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2022) to Revision A (May 2023)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

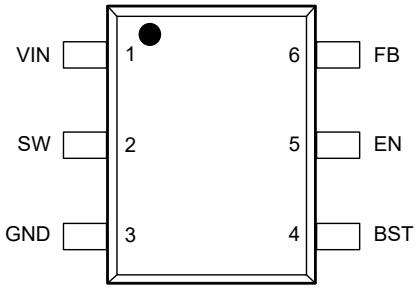


図 5-1. 6-Pin SOT563 DRL Package (Top View)

表 5-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
VIN	1	P	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
SW	2	P	Switch node pin. Connect the output inductor to this pin.
GND	3	G	GND pin for the controller circuit and the internal circuitry.
BST	4	P	Connect a 100-nF ceramic capacitor from this pin to the SW pin or leave it floating.
EN	5	A	Enable control input. Driving EN high or leaving this pin floating enables the converter.
FB	6	A	Converter feedback input. Connect to output voltage with a feedback resistor divider.

(1) A = Analog, P = Power, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	18	V
	FB, EN	–0.3	6	V
	GND	–0.3	0.3	V
	SW	–2	18	V
	SW (transient < 20 ns)	–5.5	20	V
	BST	–2	18	V
	BST (transient < 20 ns)	–5.5	20	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1), all pins	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Pin voltage	VIN	3		17	V
	FB, EN	–0.1		5.5	
	GND	–0.1		0.1	
	SW	–1		17	
	SW (transient < 20 ns)	–5		18	
	BST	–1		17	
	BST (transient < 20 ns)	–5		18	
Output current	I_{OUT}	0		2	A
Temperature	Operating junction temperature, T_J	–40		125	°C
	Storage temperature, T_{stg}	–40		150	

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6.4 Thermal Information

THERMAL METRIC(1)		DRL (SOT-563)	UNIT
		6 PINS	
$R_{\theta JA}$ (2)	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JA_effective}$ (3)	Junction-to-ambient thermal resistance on EVM board	74	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. These values do not represent the performance obtained in an actual application.
(3) This $R_{\theta JA_effective}$ is tested on TPS562242EVM board (2 layer, copper thickness is 2-oz) at V_{IN} = 12 V, V_{OUT} =5 V, I_{OUT} = 2A, T_A = 25°C.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input voltage range	V_{IN}	3		17	V
I_{VIN}	VIN supply current	No load, V_{EN} = 5 V, V_{FB} = 0.85 V, non-switching, ECO version		100		µA
I_{INSDN}	VIN shutdown current	No load, V_{EN} = 0 V		5		µA
UVLO						
V_{IN_UVLO}	Input undervoltage lockout threshold	Rising threshold	2.80	2.92	3.00	V
		Falling threshold	2.60	2.72	2.85	V
		Hysteresis		200		mV
FEEDBACK VOLTAGE						
V_{REF}	FB voltage	T_J = 25°C	792	800	808	mV
		T_J = –40°C to 125°C	788	800	812	mV
INTEGRATED POWER MOSFETS						
R_{DSON_HS}	High-side MOSFET on-resistance	T_J = 25°C, V_{IN} ≥ 5 V		55.0		mΩ
		T_J = 25°C, V_{IN} = 3 V (1)		67.5		mΩ
R_{DSON_LS}	Low-side MOSFET on-resistance	T_J = 25°C, V_{IN} ≥ 5 V		24.3		mΩ
		T_J = 25°C, V_{IN} = 3 V		30.2		mΩ
SWITCHING FREQUENCY						
F_{sw}	Switching frequency	T_J = 25°C, V_{OUT} = 3.3 V		1.4		MHz
$T_{ON(MIN)}$ (1)	Minimum on time			60		ns
$T_{OFF(MIN)}$ (1)	Minimum off time	V_{FB} = 0.6 V		110		ns
LOGIC THRESHOLD						
V_{ENH}	EN threshold high level	Rising enable threshold	1.14	1.17	1.22	V
V_{ENL}	EN threshold low level	Falling disable threshold	0.91	1.00	1.09	V
V_{ENHYS}	EN hystersis	Hysteresis		170		mV
I_{EN}	EN pull up current	V_{EN} = 1.0 V		1.6		uA
CURRENT LIMIT						
I_{OCL_LS}	Overcurrent threshold	Valley current set point	2.3	3.0	3.6	A
SOFT START						
t_{SS}	Internal soft start time			1.6		ms

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6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold	V_{FB} rising	110	115	120	%
t_{OVPDLY}	OVP prop deglitch			24		us
V_{UVP}	UVP trip threshold	V_{FB} falling	55	60	65	%
t_{UVPDLY}	UVP prop deglitch			220		us
t_{UVPEN}	Hiccup enable delay time			14		ms
THERMAL SHUTDOWN						
T_{SDN} (1)	Thermal shutdown threshold	Shutdown temperature		155		°C
T_{OTPHSY} (1)		Hysteresis		20		

(1) Specified by design

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6.6 Typical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

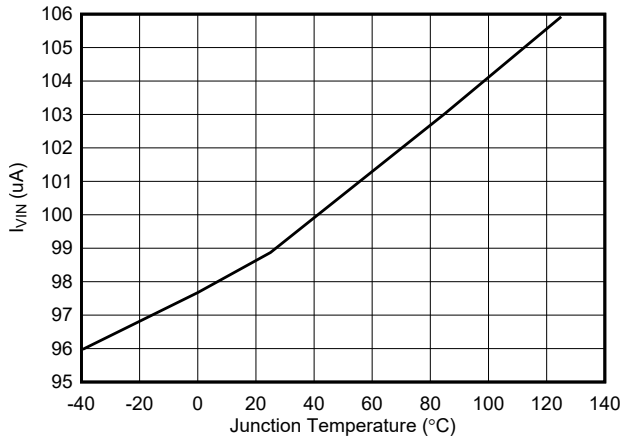


図 6-1. Quiescent Current

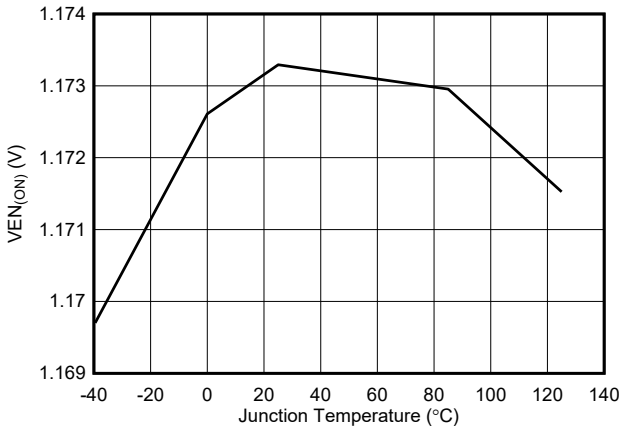


図 6-2. Enable On Threshold Voltage

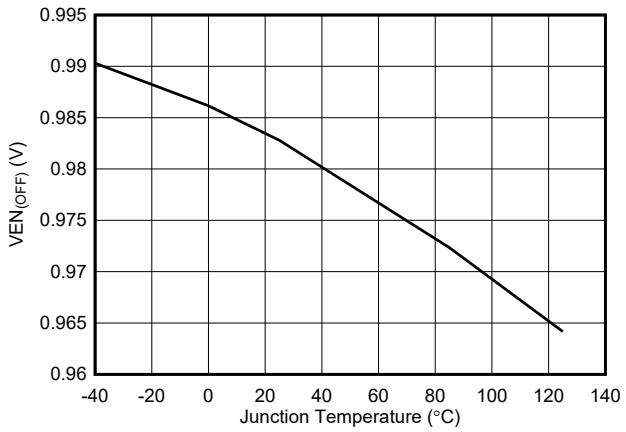


図 6-3. Enable Off Threshold Voltage

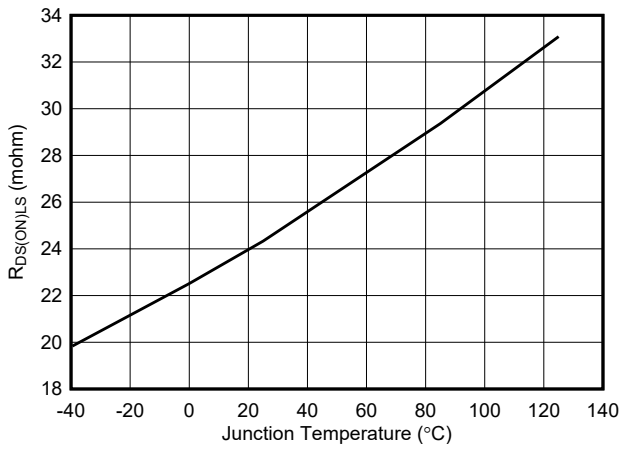


図 6-4. Low-Side $R_{DS(ON)}$

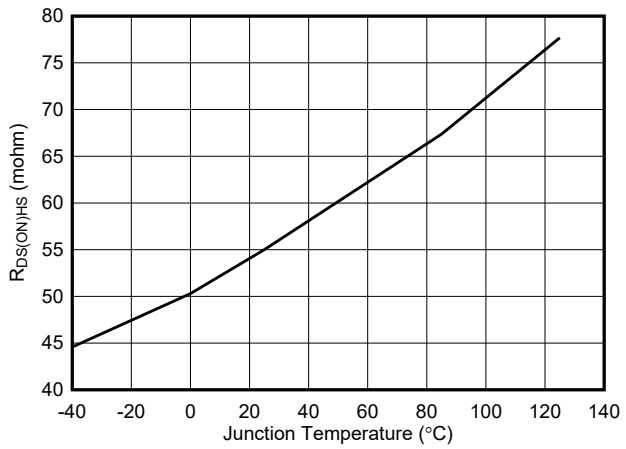


図 6-5. High-Side $R_{DS(ON)}$

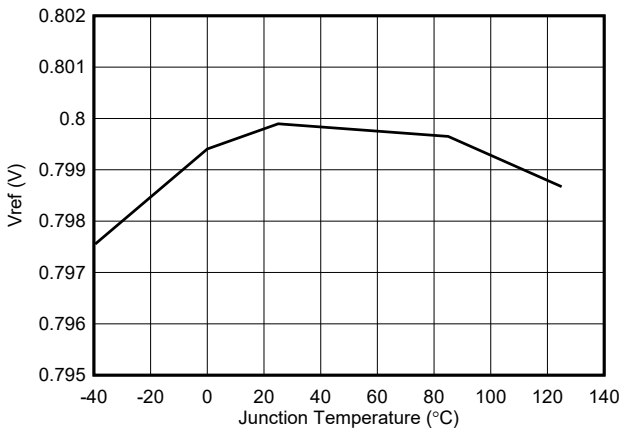


図 6-6. VREF Voltage

6.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

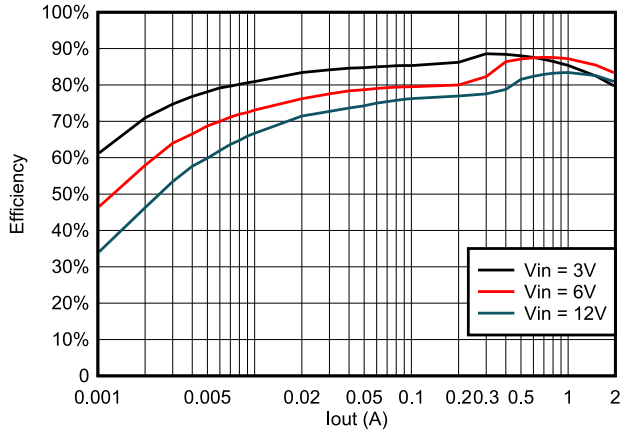


図 6-7. Efficiency at 0.8 V_{OUT} with a 1-µH Inductor

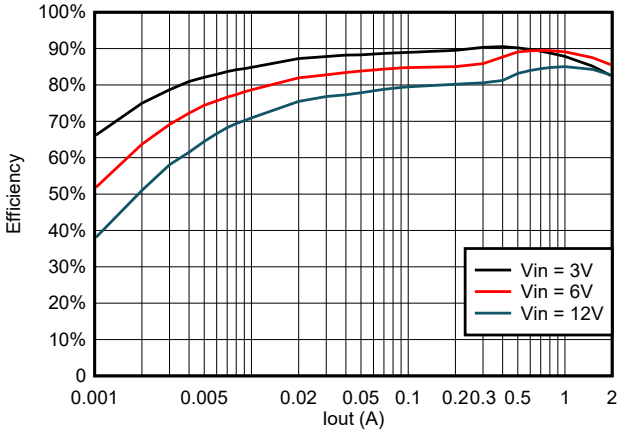


図 6-8. Efficiency at 1.05 V_{OUT} with a 1.2-µH Inductor

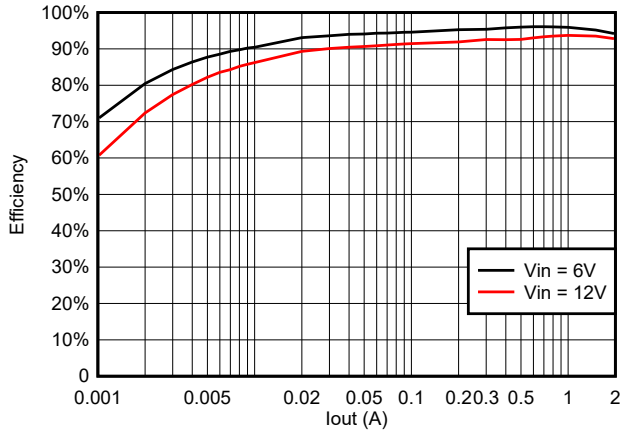


図 6-9. Efficiency at 3.3 V_{OUT} with a 2.2-µH Inductor

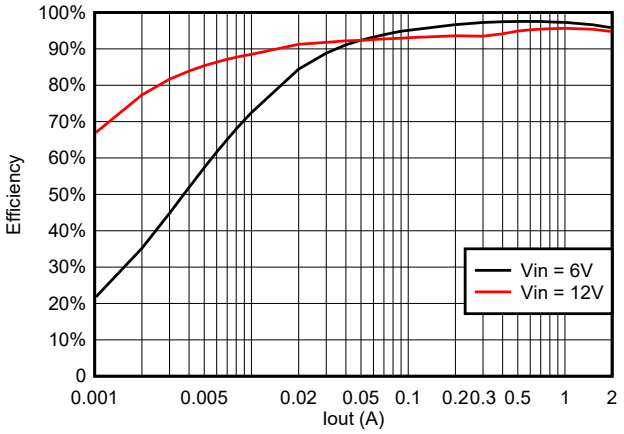


図 6-10. Efficiency at 5 V_{OUT} with a 3.3-µH Inductor

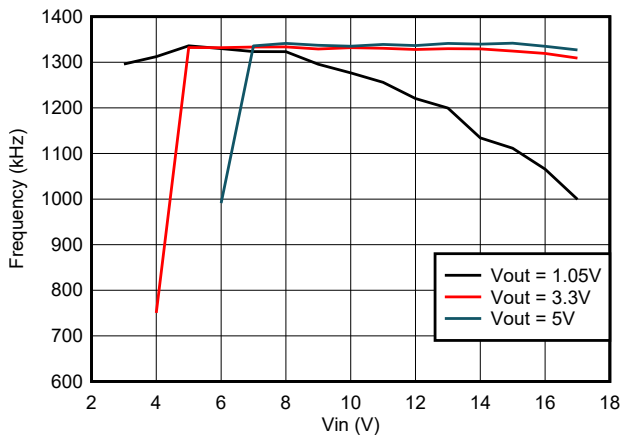


図 6-11. Frequency vs Input Voltage, I_{OUT} = 2 A

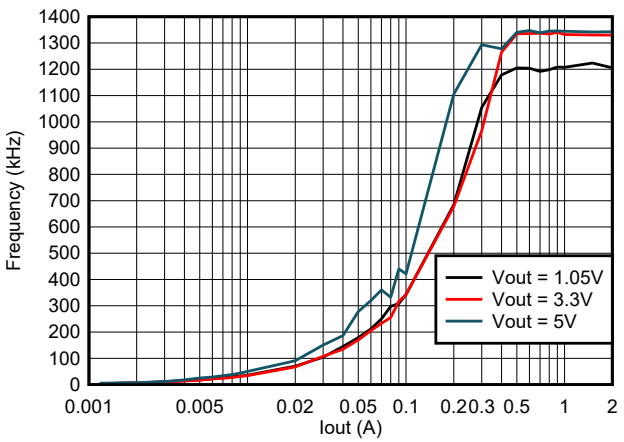


図 6-12. Frequency vs Loading, V_{IN} = 12 V

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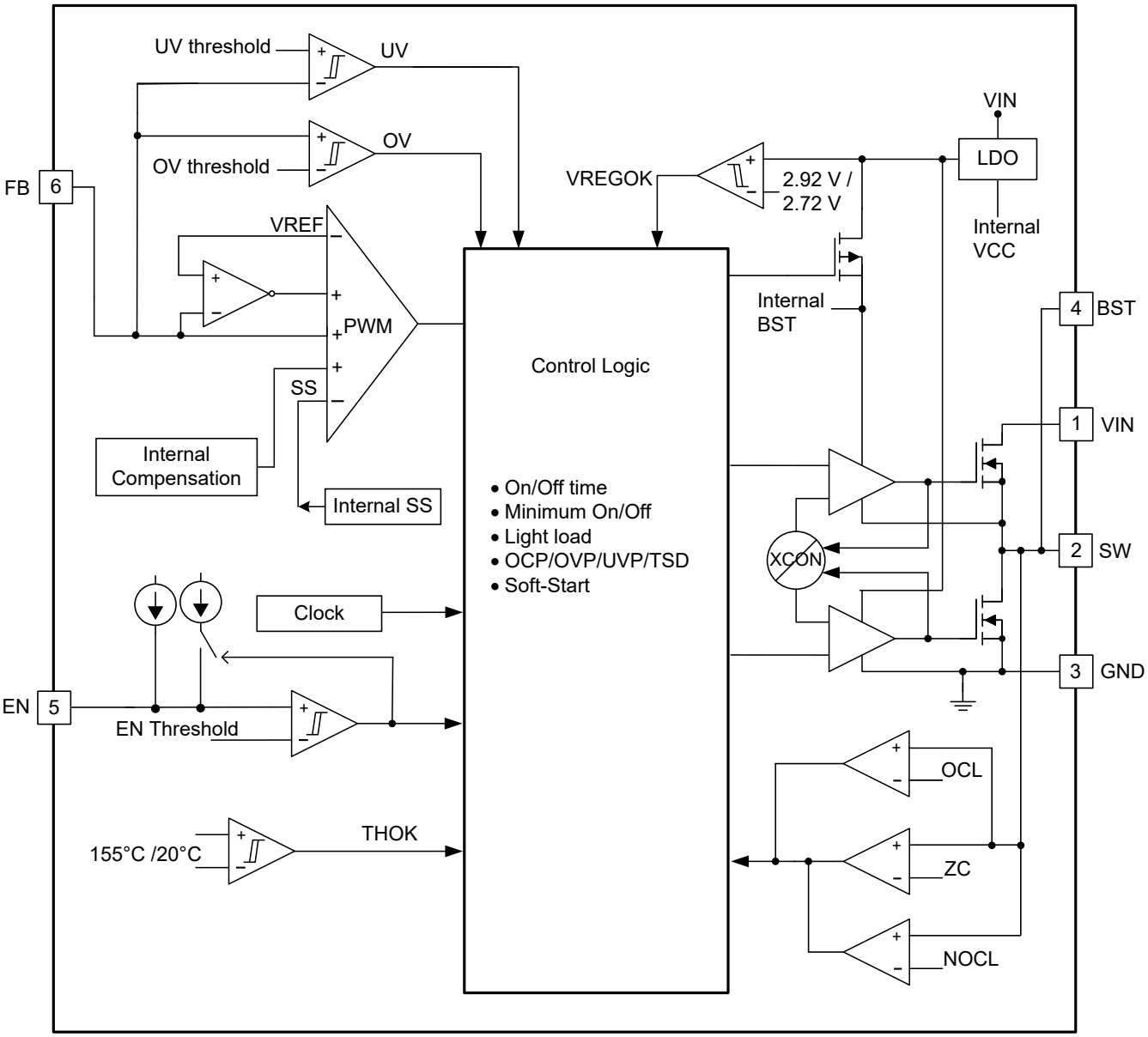
7 Detailed Description

7.1 Overview

The TPS562242 is a 2-A integrated FET synchronous buck converter that operates from 3-V to 17-V input voltage and 0.8-V to 10-V output voltage. The device employs a D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 control mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation mode at lighter load condition.

The Eco-mode version allows the TPS562242 to maintain high efficiency at light load. The TPS562242 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The device is stable even with virtually no ripple at the output. The TPS562242 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence, it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

7.3.2 Eco-mode Control

The TPS562242 is designed with advanced Eco-mode to maintain high light-load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its ripple valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use the below equation to calculate the transition point to the light load operation $I_{OUT(LL)}$ current.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Prebiased Soft Start

The TPS562242 has an internal fixed 1.6-ms soft-start time. The internal soft-start function begins ramping up the reference voltage to the PWM comparator during start-up period.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes higher than the feedback voltage, V_{FB}. This scheme makes sure that the converter ramps up smoothly into the regulation point.

7.3.4 Overvoltage Protection

The TPS562242 has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, the OVP is triggered with a 24-µs deglitch time. Both the high-side MOSFET and the low-side MOSFET drivers are turned off. When the overvoltage condition is removed, the device returns to switching.

7.3.5 Large Duty Operation

The TPS562242 can support large duty operations up to 94% by smoothly dropping down the switching frequency. When V_{IN} / V_{OUT} < 1.6 and V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make t_{ON} extended to implement the large duty operation and improve the performance of the load transient. Please refer frequency test waveform in 図 6-11. The minimum switching frequency is limited to approximately 700 kHz.

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7.3.6 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the off state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- On-time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT}. If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it and the device shuts down after the UVP delay time (typically 220 µs) and restarts after the hiccup wait time (typically 14 ms). After the device enters the hiccup cycling, the hiccup on time is typically 2.2 ms.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

7.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is a non-latch protection.

7.3.8 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This protection is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Eco-mode Operation

The TPS562242 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This action makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical buck DC/DC converter that is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 2 A. The following design procedure can be used to select component values for TPS562242. Alternately, the WEBENCH Power Designer software can be used to generate a complete design. The WEBENCH Power Designer software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in 図 8-1 was developed to meet the requirements in 表 8-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

図 8-1 shows the TPS562242 5-V to 17-V input, 1.05-V output converter schematic.

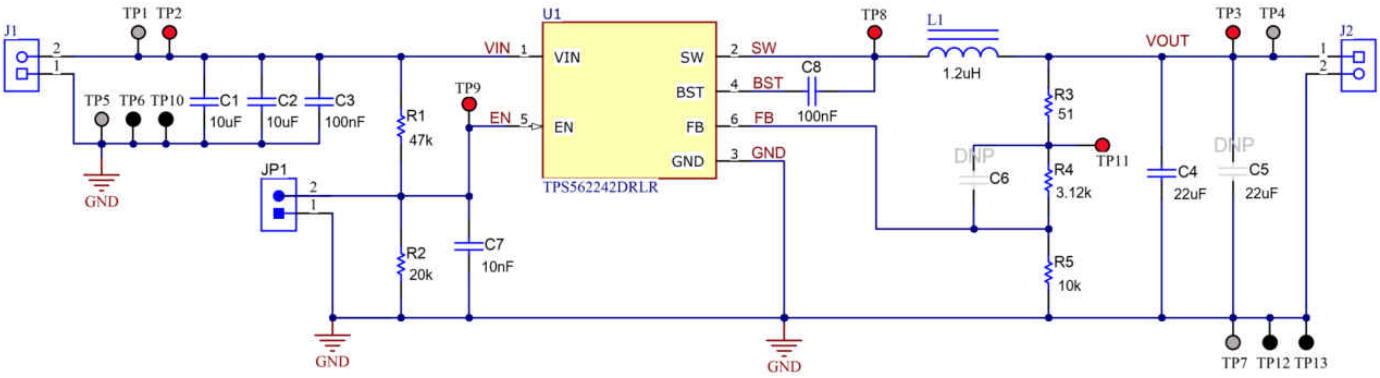


図 8-1. Schematic

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

Parameter		Conditions	MIN	TYP	MAX	Unit
V_{OUT}	Output voltage			1.05		V
I_{OUT}	Output current			2		A
ΔV_{OUT}	Transient response	0.2-A – 1.8-A load step, 0.8-A/µs slew rate		±2% × V_{OUT}		V
V_{IN}	Input voltage		5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		6		mV
F_{SW}	Switching frequency			1.4		MHz
T_A	Ambient temperature			25		°C

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS562242 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Start by using 式 2 to calculate V_{OUT}.

To improve efficiency at very light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. Use a 10-kΩ resistor for R_5 to start the design.

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_4}{R_5}\right) \tag{2}$$

8.2.2.3 Output Filter Selection

The LC filter used as the output filter has a double pole at 式 3. In this equation, C_{OUT} uses its effective value after derating, not its nominal value.

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

For any control topology that is compensated internally, there is a range of the output filter it can support. At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops has a 180 degree drop. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 156 kHz. TI recommends the inductor and capacitor selected for the output filter such that the double pole is located approximately 40 kHz, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system is usually targeted to be less than one-third of the switching frequency (f_{SW}). For high output voltage condition, TI recommends to use 10-100pF feedforward capacitor for enough phase margin.

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表 8-2. Recommended Component Values

Output Voltage (V)	R4 (kΩ)	R5 (kΩ)	Typical L1 (µH)	Typical C_{OUT} (µF)	Typical C_{OUT} (µF) Nominal Value Range	Typical C_{OUT} Category	Typical C6 (pF)
0.8	0	10.0	1	44	22-88	MLCC, 0805, 10V	—
1.05	3.12	10.0	1.2	22	22-66	MLCC, 0805, 10V	—
3.3	94.2	30.0	2.2	22	22-88	MLCC, 0805, 10V	33
5	158.0	30.0	3.3	22	22-88	MLCC, 0805, 10V	33
10	345.0	30.0	4.7	44	44-88	MLCC, 0805, 16V	47

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 式 4, 式 5, and 式 6. Generally, TI recommends the peak-to-peak ripple current to be 20% – 50% of output average current for a comprehensive benefit of efficiency and inductor volume. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \tag{5}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \tag{6}$$

For this design example, the calculated peak current is 2.3 A and the calculated RMS current is 2.00 A. The inductor used is 74438357012 with 7-A rated current and 8.8-A saturation current.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562242 are intended for use with ceramic or other low-ESR capacitors. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{7}$$

For this design, one MuRata GRM21BR61A226ME44L 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.17 A and each output capacitor is rated for 4 A.

8.2.2.4 Input Capacitor Selection

The TPS562242 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. TI recommends an additional 0.1-µF capacitor from the VIN pin to ground to provide high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.2.5 Bootstrap Capacitor Selection

The real BST is integrated inside by using a special charging high side FET circuit. A typical 0.1-µF ceramic capacitor can be connected between the BST to SW pin or leave floating.

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8.2.3 Application Curves

The following data is tested with V_{IN} = 12 V, V_{OUT} = 1.05 V, T_A = 25°C, unless otherwise specified.

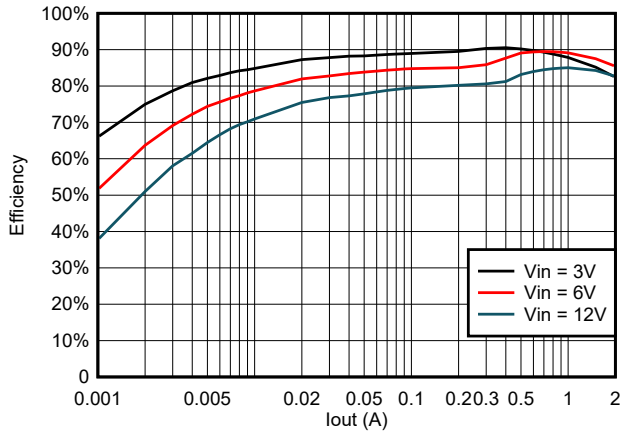


図 8-2. Efficiency vs Loading

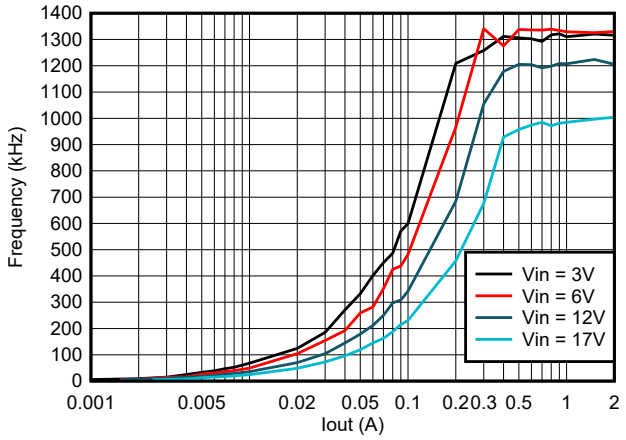


図 8-3. Frequency vs Loading

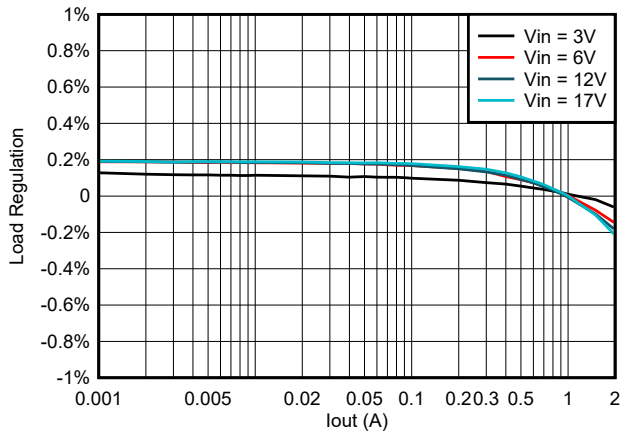


図 8-4. Load Regulation vs Loading

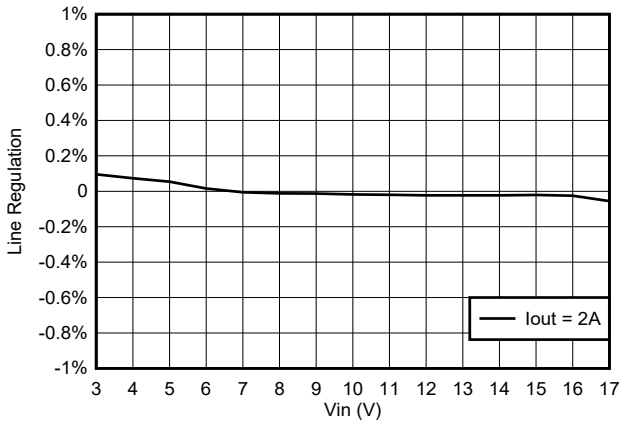


図 8-5. Line Regulation vs V_{IN}

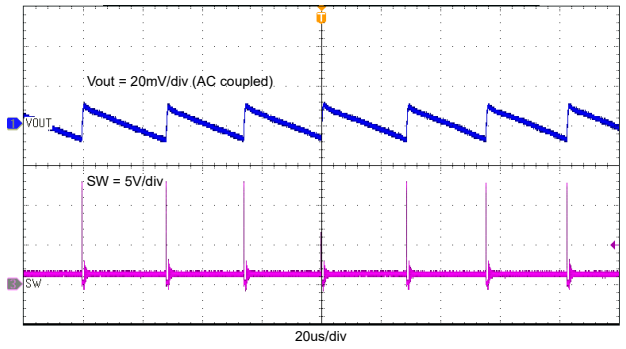


図 8-6. Output Voltage Ripple with 0.01-A Loading

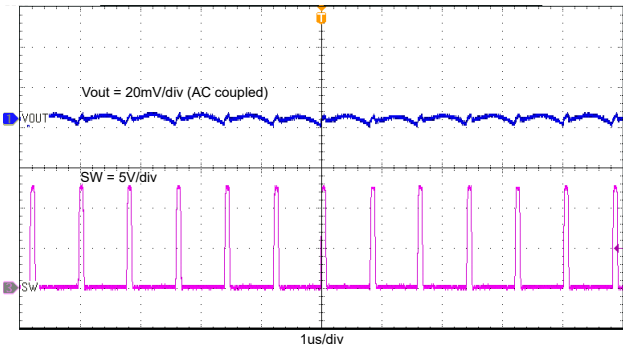


図 8-7. Output Voltage Ripple with 2-A Loading

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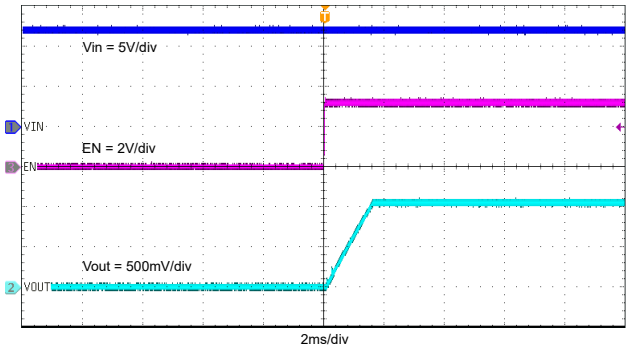


図 8-8. Start-up Through EN, I_{OUT} = 2 A

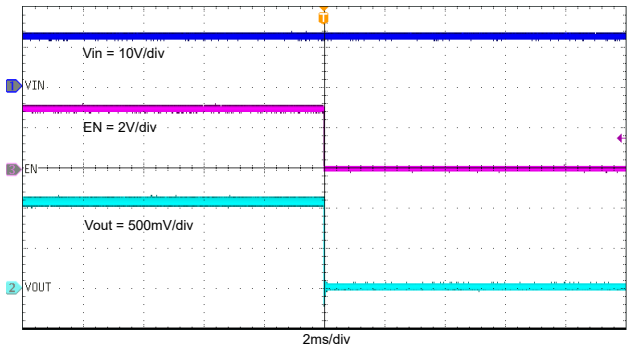


図 8-9. Shutdown Through EN, I_{OUT} = 2 A

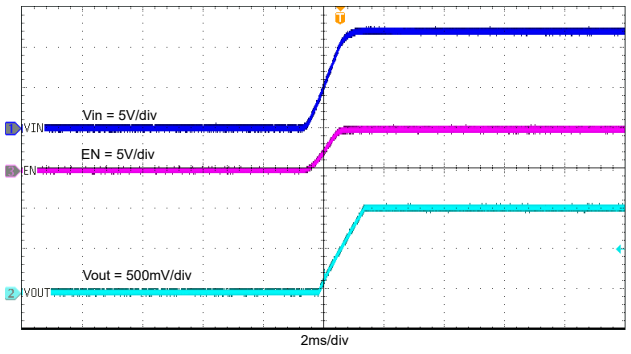


図 8-10. Start-up with V_{IN} Rising, I_{OUT} = 2 A

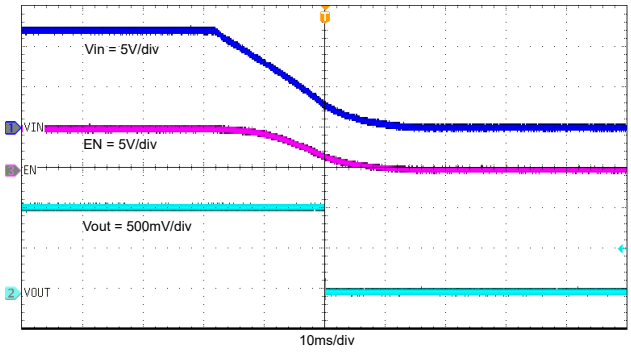


図 8-11. Shutdown with V_{IN} Falling, I_{OUT} = 2 A

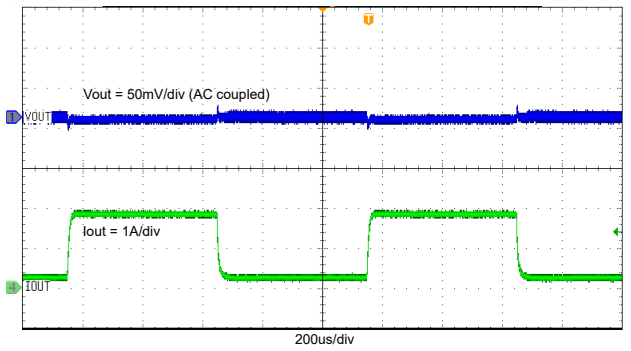


図 8-12. Transient Response with 0.2 A to 1.8 A

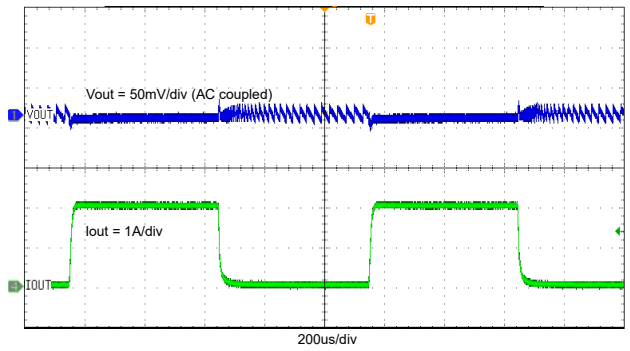


図 8-13. Transient Response with 0.01 A to 2 A

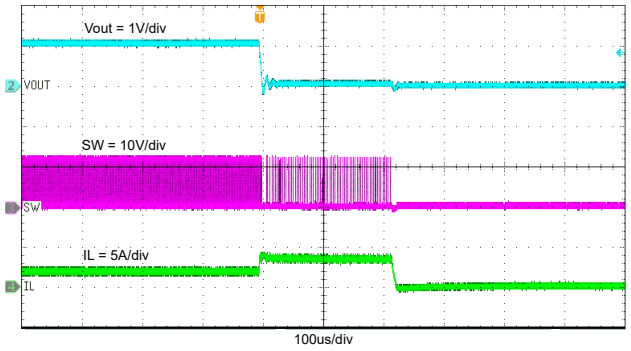


図 8-14. Normal Operation to Output Hard Short

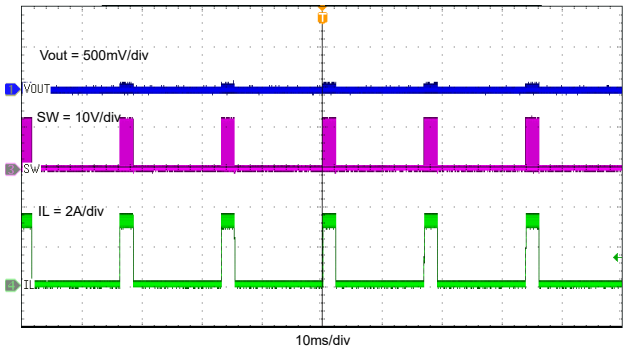


図 8-15. Output Hard Short Hiccup

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8.3 Power Supply Recommendations

The TPS562242 are designed to operate from input supply voltages in the range of 3 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

8.4 Layout

8.4.1 Layout Guidelines

- Keep VIN and GND traces as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- Connect a separate VOUT path to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Place a voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
- Make the trace of the FB node as small as possible to avoid noise coupling.
- Make the GND trace between the output capacitor and the GND pin as wide as possible to minimize its trace impedance.

8.4.2 Layout Example

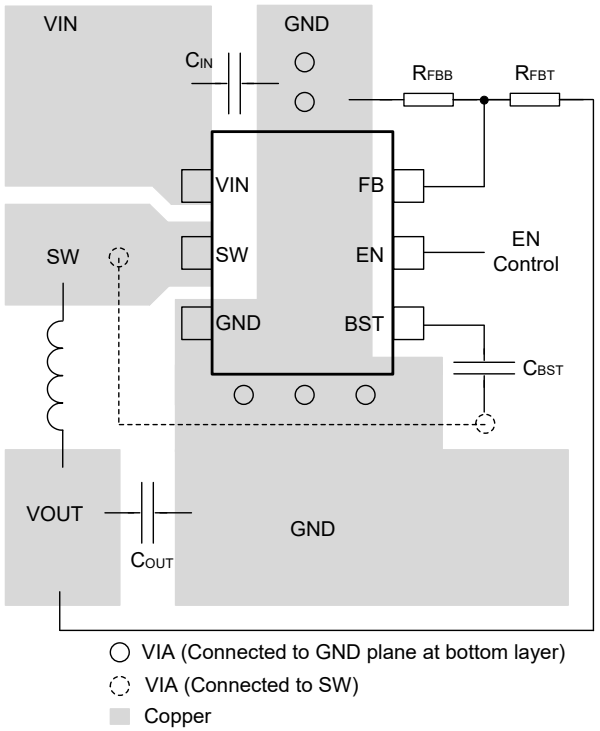


図 8-16. Suggested Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS562242 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS562242DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	2242
TPS562242DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2242

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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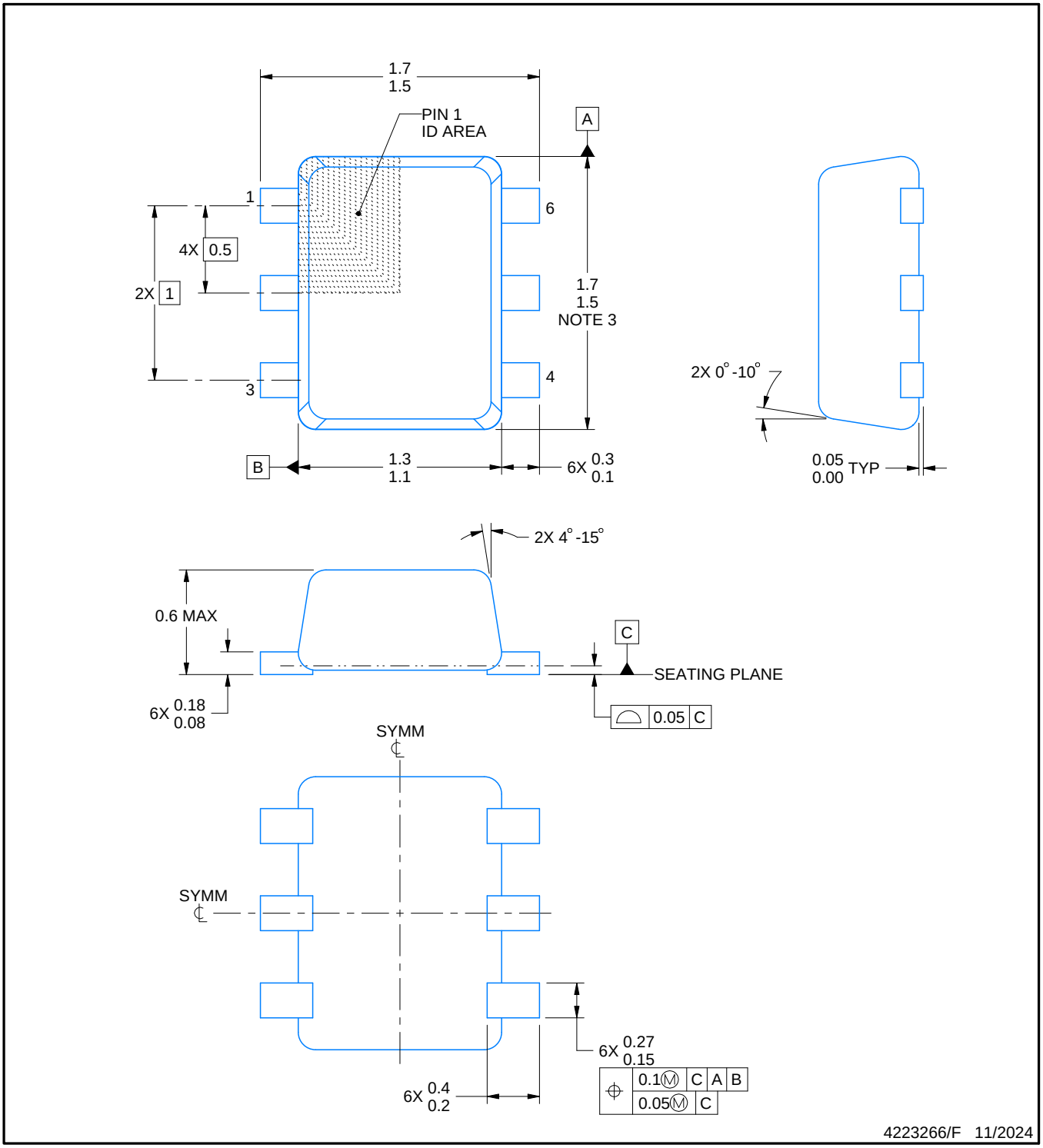


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

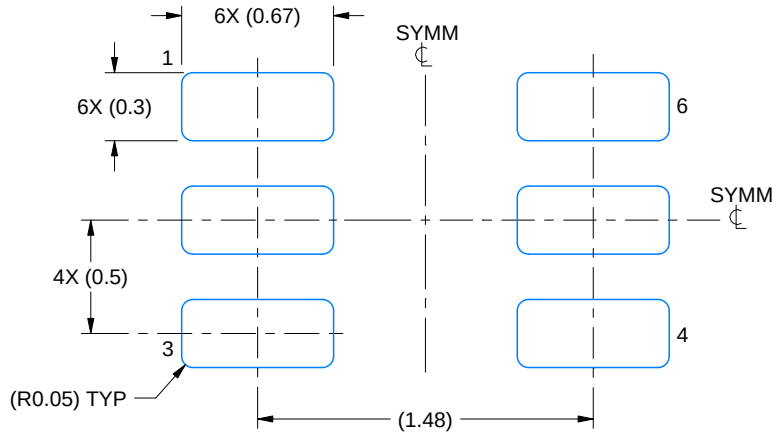
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

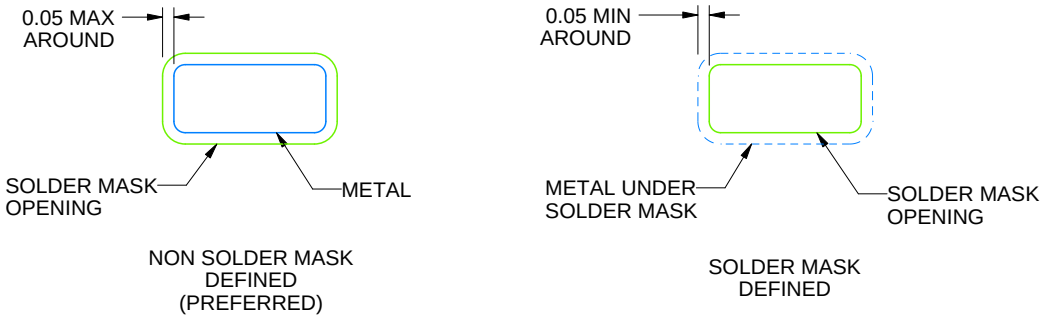
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

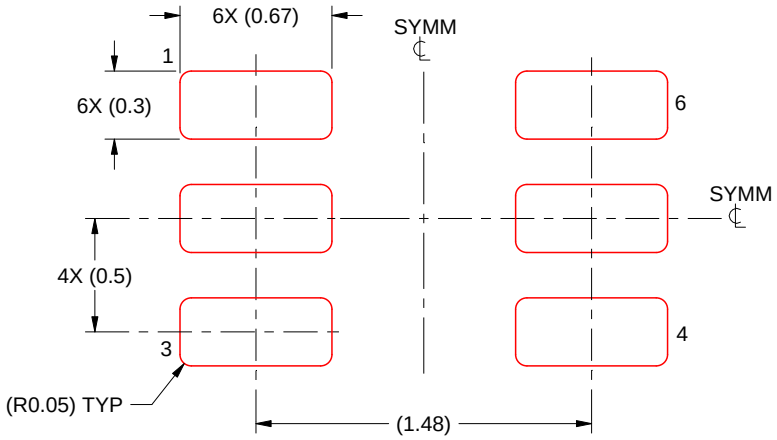
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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