TEXAS INSTRUMENTS
TPS564201
JAJSC68B – MAY 2016 – REVISED AUGUST 2017

TPS564201 SOT-23パッケージ、4.5V～17V入力、4Aの同期整流降圧型電圧レギュレータ

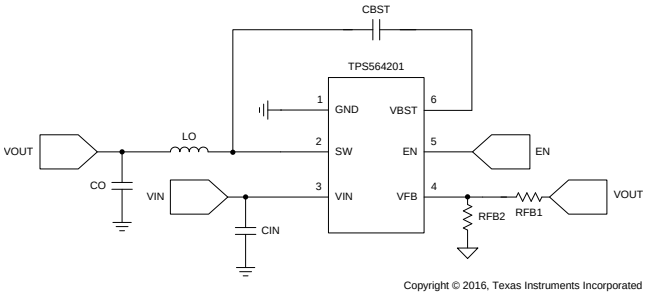
1 特長

- TPS564201: 50mΩおよび22mΩ FET内蔵の4Aコンバータ
- D-CAP2™モード制御による高速過渡応答
- 入力電圧範囲: 4.5V～17V
- 出力電圧範囲: 0.76V～7V
- パルス・スキップ・モード
- 560kHzのスイッチング周波数
- 低いシャットダウン電流: 5μA未満
- 帰還電圧精度: 1.6% (25℃)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- Hiccupモードによる過電流保護
- 非ラッチUVPおよびTSD保護
- 固定ソフトスタート: 1.0ms
- WEBENCH® Power Designerにより、TPS564201を使用するカスタム設計を作成

2 アプリケーション

- デジタル・テレビ用電源
- 高精細 Blu-ray™ディスク・プレイヤー
- ネットワーク・ホーム・ターミナル
- デジタル・セットトップ・ボックス（STB）
- 監視機器

概略回路図



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3 概要

TPS564201は単純で使いやすい、4A同期整流降圧型コンバータで、SOT-23パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

これらのスイッチ・モード電源(SMPS)デバイスは、D-CAP2モード制御を採用し、高速の過渡応答を実現します。また、特殊ポリマーなどESR (等価直列抵抗)の低い出力コンデンサと、超低ESRのセラミック・コンデンサの両方を、外部補償部品なしでサポートします。

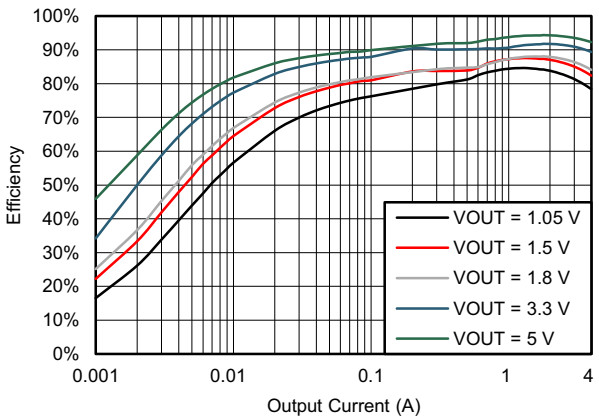
TPS564201はパルス・スキップ・モードで動作し、軽負荷時に高い効率を維持します。TPS564201は、6ピンの1.6mm×2.9mm SOT (DDC)パッケージで供給され、接合部温度-40℃～125℃で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS564201	DDC (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

TPS564201の効率



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (May 2016) から Revision B に変更 **Page**

- 「特長」にWEBENCH® Designerへのリンクを 追加 ... 1
- Changed V_{FBTH} spec MIN from 739 to 745, TYP from 759 to 760, and MAX from 779 to 775 ... 5
- Changed equation Equation 2 ... 13
- 追加 WEBENCH®ツールによるカスタム設計 ... 20

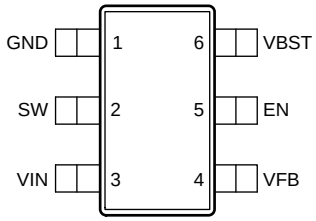
2016年5月発行のものから更新 **Page**

- 完全な仕様のリリース ... 1

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5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27	V
	VBST (vs SW)	–0.3	6.5	V
	VFB	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range		4.5		17	V
V_I	Input voltage range	VBST	–0.1		23	V
		VBST (10 ns transient)	–0.1		26	
		VBST (vs SW)	–0.1		6.0	
		EN	–0.1		17	
		VFB	–0.1		5.5	
		SW	–1.8		17	
		SW (10 ns transient)	–3.5		20	
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS564201 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VIN}	Operating – non-switching supply current	V_{IN} current, EN = 5 V, V_{FB} = 1 V	TPS564201		400	510	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0 V			0.9	5	µA
LOGIC THRESHOLD							
V_{ENH}	EN high-level input voltage	EN		1.6			V
V_{ENL}	EN low-level input voltage	EN				0.8	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	425	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
V_{FBTH}	V_{FB} threshold voltage	V_O = 1.05 V, continuous mode operation		745	760	775	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High-side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V			50		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_A = 25°C			22		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_1 = 1.5 µH		4.2	6	7.7	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature			172		°C
		Hysteresis			38		
ON-TIME TIMER CONTROL							
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.68 V			220	280	ns
SOFT START							
t_{SS}	Soft-start time	Internal soft-start time			1.0		ms
FREQUENCY							
F_{sw}	Switching frequency	V_{IN} = 12 V, V_O = 1.05 V, FCCM mode			560		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)			65%		
T_{HICCUP_WAIT}	Hiccup on time				1.9		ms
T_{HICCUP_RE}	Hiccup time before restart				15.5		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage			4.0	4.3	V
		Shutdown VIN voltage		3.3	3.6		
		Hysteresis VIN voltage (1)			0.4		

(1) Not production tested.

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6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

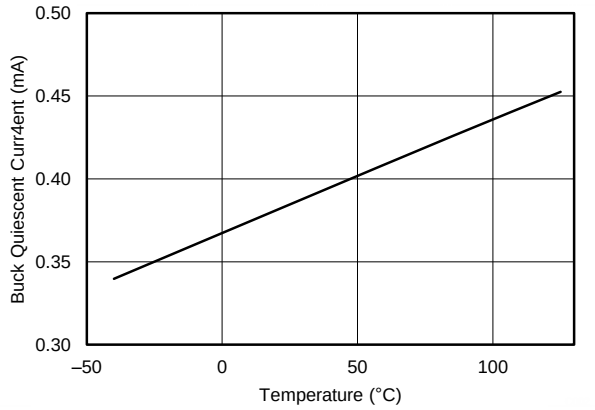


Figure 1. TPS56420 Supply Current vs Junction Temperature

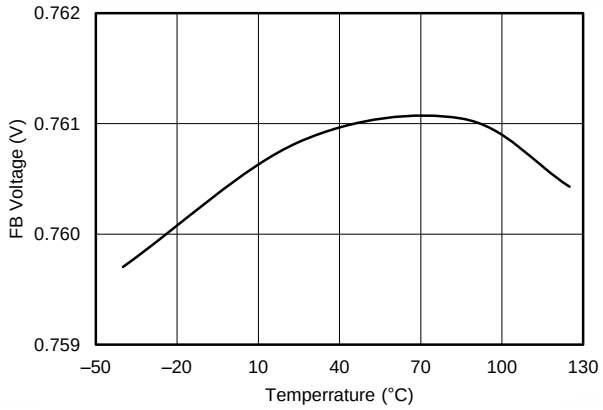


Figure 2. VFB Voltage vs Junction Temperature

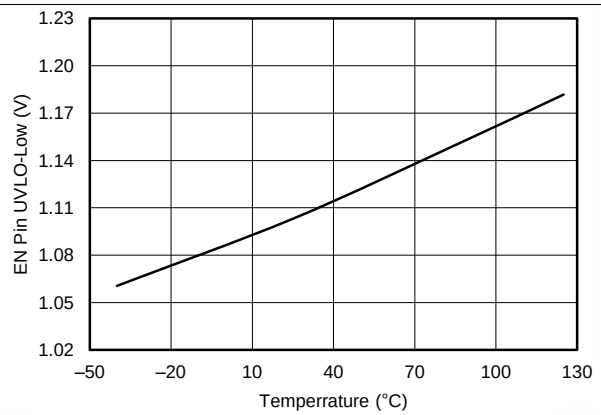


Figure 3. EN Pin UVLO Low Voltage vs Junction Temperature

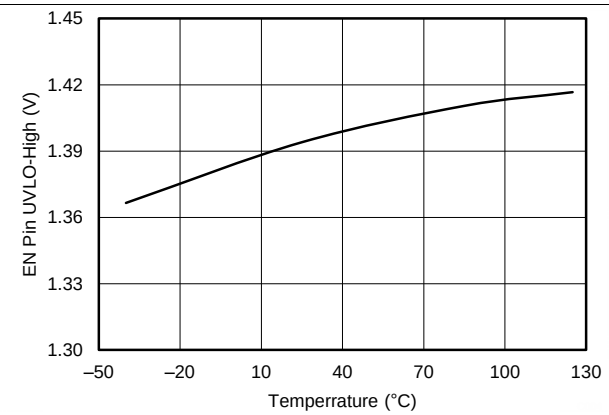


Figure 4. TPS564201 EN Pin UVLO High Voltage vs Junction Temperature

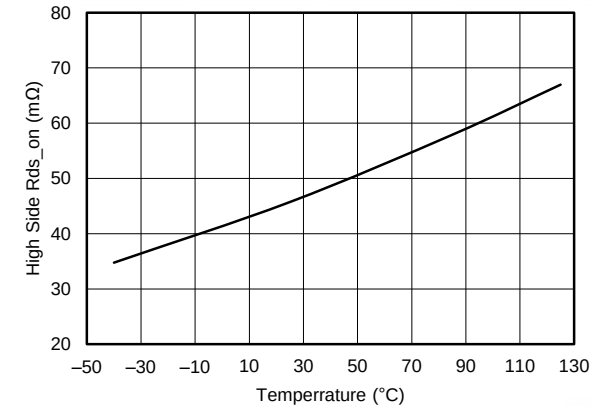


Figure 5. TPS564201 High-Side $R_{ds\text{-}On}$ vs Junction Temperature

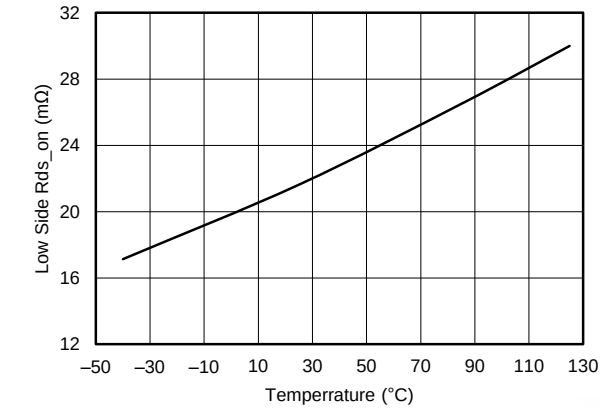


Figure 6. Low-Side $R_{ds\text{-}On}$ vs Junction Temperature

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Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

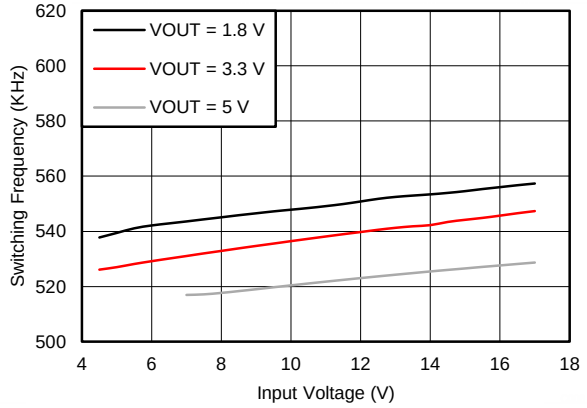


Figure 7. TPS564201 Switching Frequency vs Input Voltage

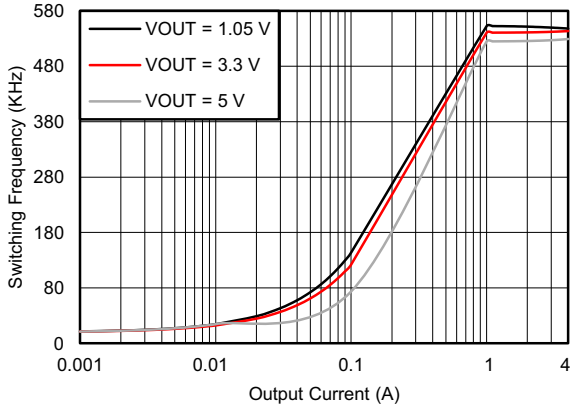
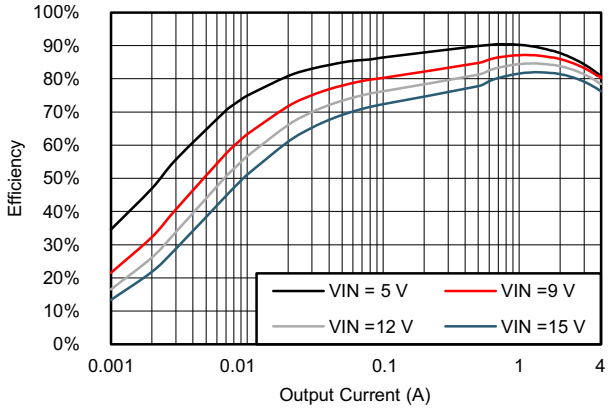
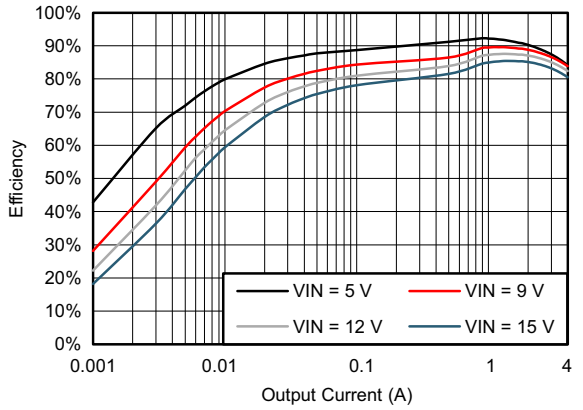


Figure 8. TPS564201 Switching Frequency vs Output Current



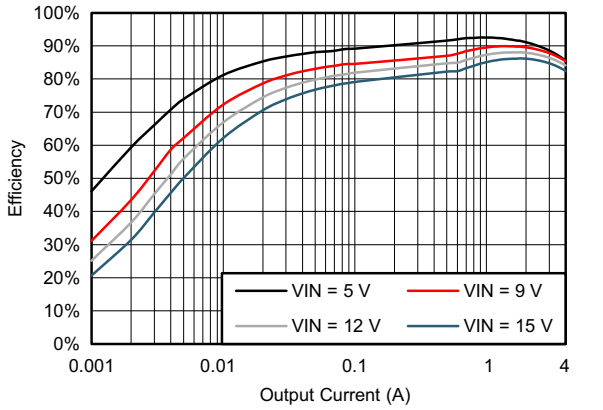
V_{OUT} = 1.05 V L = 2.2 µH

Figure 9. TPS564201 Efficiency vs Output Current



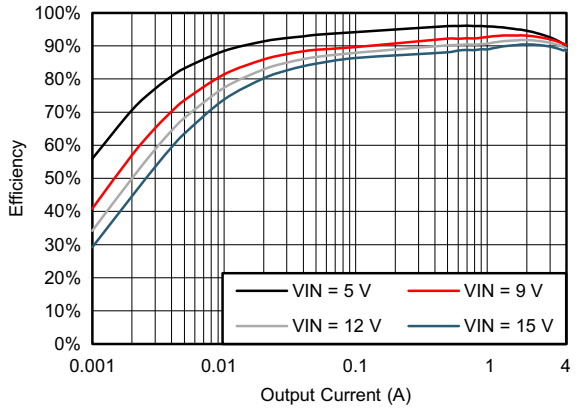
V_{OUT} = 1.5 V L = 2.2 µH

Figure 10. TPS564201 Efficiency vs Output Current



V_{OUT} = 1.8 V L = 2.2 µH

Figure 11. TPS564201 Efficiency vs Output Current



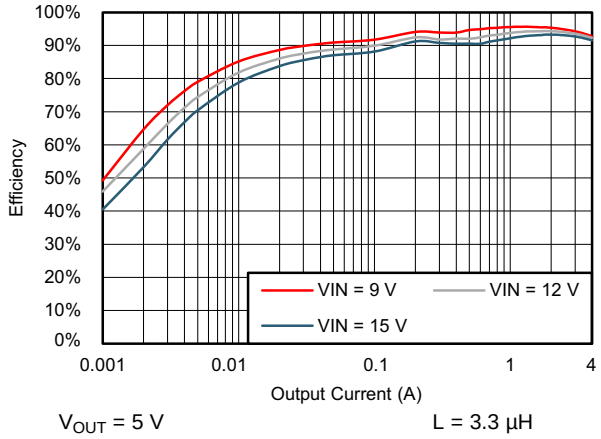
V_{OUT} = 3.3 V L = 2.2 µH

Figure 12. TPS564201 Efficiency vs Output Current

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Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)



V_{OUT} = 5 V L = 3.3 µH

Figure 13. TPS564201 Efficiency vs Output Current

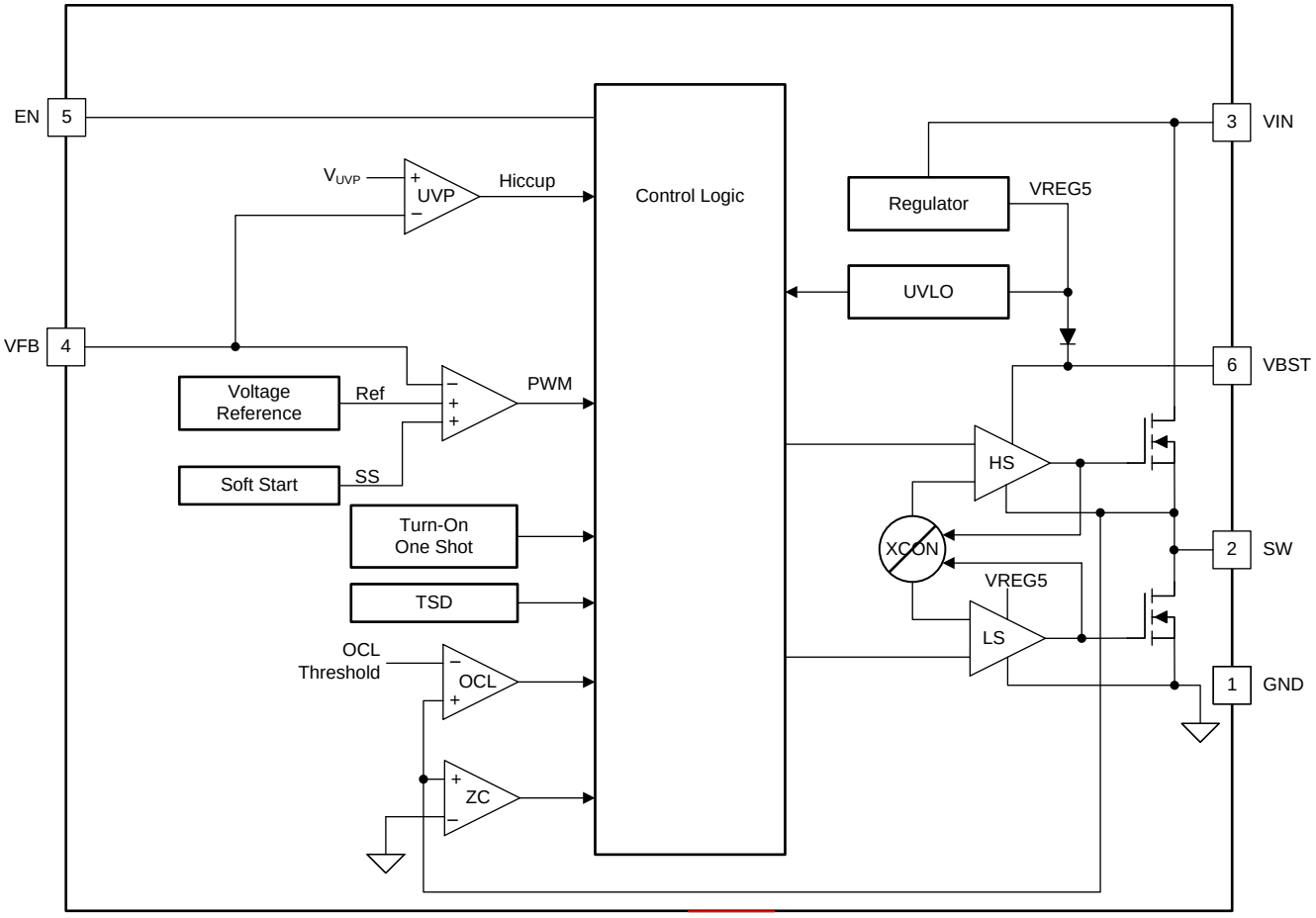
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7 Detailed Description

7.1 Overview

The TPS564201 is a 4-A synchronous step-down converter. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS564201 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot duration is set inversely proportional to the converter input voltage, V_{IN}, and proportional to the output voltage V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 Pulse Skip Mode

The TPS564201 is designed with Advanced Eco-mode™ to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation IOUT(LL) current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Pre-Biased Soft Start

The TPS564201 has an internal 1.0-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converter ramps up smoothly into regulation point.

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Feature Description (continued)

7.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device shuts down after the UVP delay time (typically 24 µs) and re-starts after the hiccup time (typically 15.5 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS564201 operates in the normal switching mode. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS564201 operates at a quasi-fixed frequency of 560 kHz.

7.4.2 Eco-mode™ Operation

When the TPS564201 is in the normal CCM operating mode and the switch current falls to 0A, the TPS564201 begins operating in pulse skipping eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS564201 is operating in either normal CCM or Eco-mode™, it may be placed in standby by asserting the EN pin low.

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8 Application and Implementation

NOTE

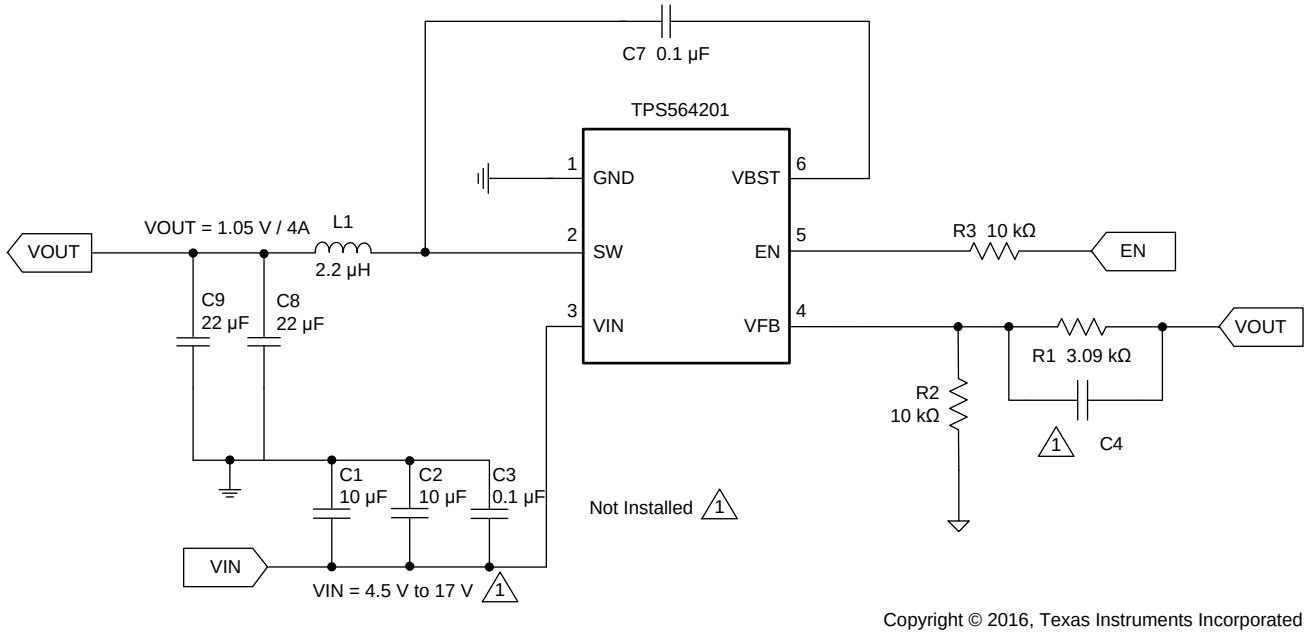
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical step-down DC-DC converter for converting a higher dc voltage to a lower dc voltage with a maximum available output current of 4 A. The following design procedure can be used to select component values for the TPS564201. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in Figure 14 shows the TPS564201 4.5-V to 17-V input, 1.05-V output converter design meeting the requirements for 4-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.



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Figure 14. TPS564201 1.05-V, 4-A Reference Design

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Typical Application (continued)

8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 2-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	4 A
Operating frequency	560 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS564201 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors. However, using too high of resistance causes the circuit to be more susceptible to noise; and, voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.760 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

8.2.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

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At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 to 68
1.05	3.74	10.0	1.5	2.2	4.7	20 to 68
1.2	5.76	10.0	1.5	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 560 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 7.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 4.4 A and the calculated RMS current is 4 A. The inductor used is a WE 74431122 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS564201 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

8.2.2.4 Input Capacitor Selection

The TPS564201 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

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8.2.2.5 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

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8.2.3 Application Curves

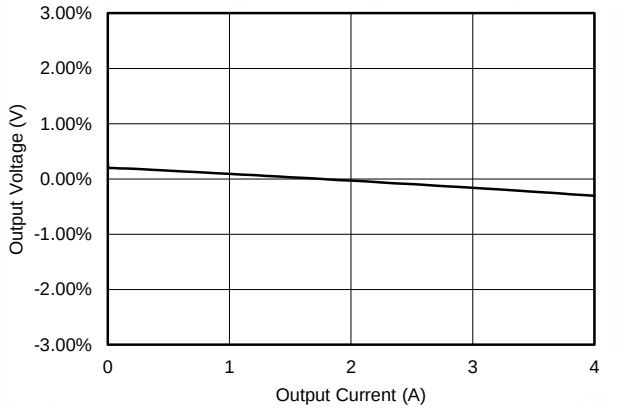


Figure 15. Load Regulation, V_{IN} = 5 V

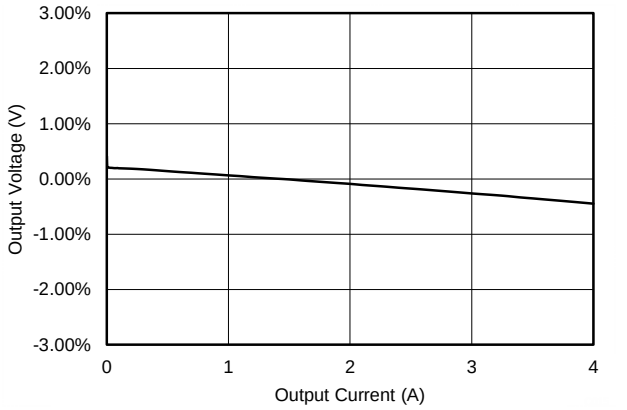


Figure 16. Load Regulation, V_{IN} = 12 V

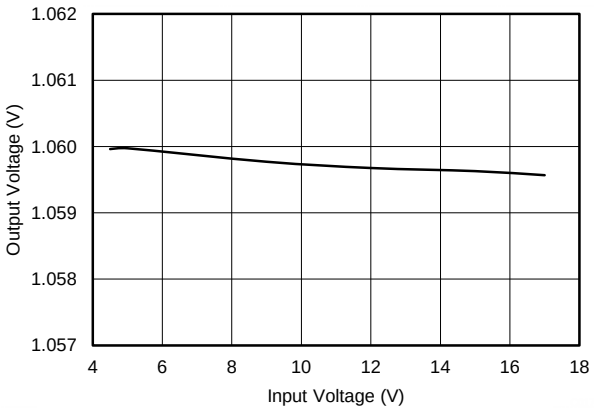


Figure 17. Line Regulation

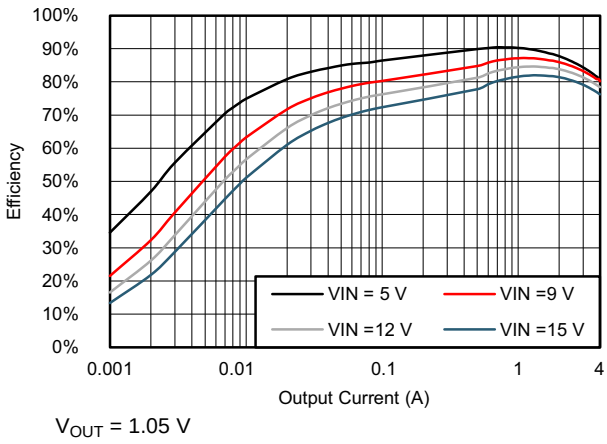


Figure 18. Efficiency vs Output Current

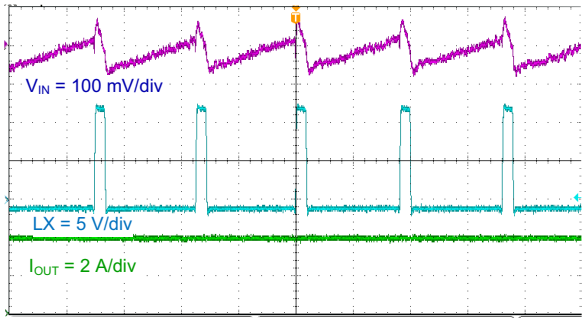


Figure 19. TPS564201 Input Voltage Ripple

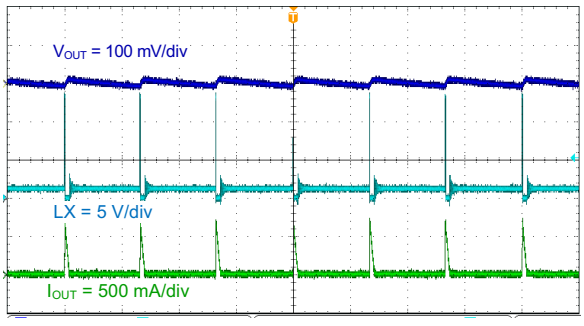


Figure 20. TPS564201 Output Voltage Ripple, No Load

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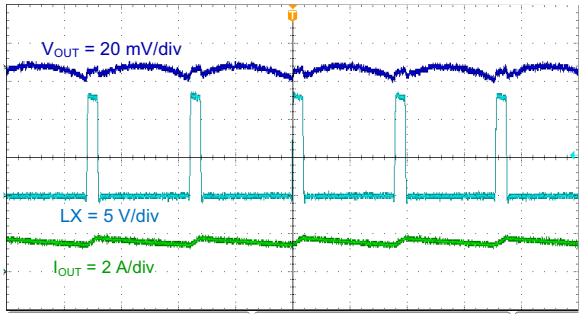


Figure 21. TPS564201 Output Voltage Ripple, I_{OUT} 2 A

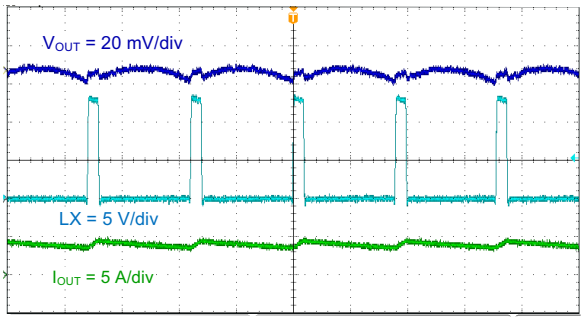


Figure 22. TPS564201 Output Voltage Ripple, I_{OUT} 4 A

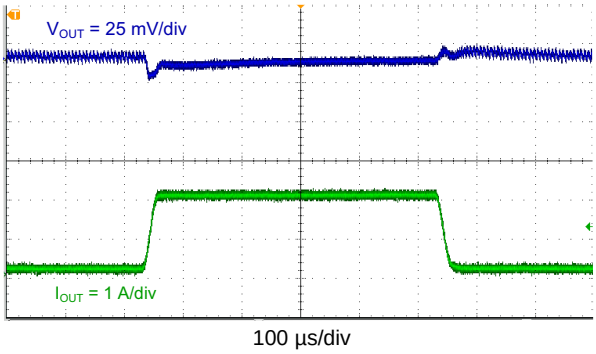


Figure 23. TPS564201 Transient Response 0.1 to 2 A

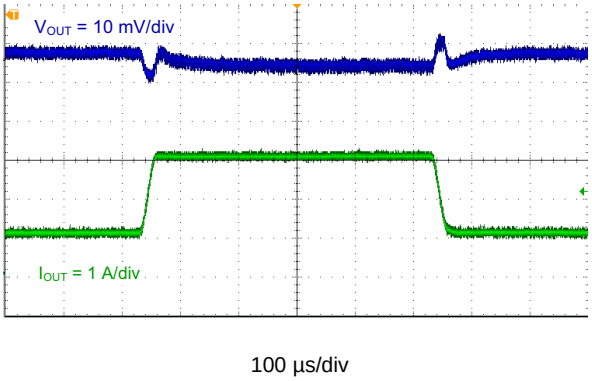


Figure 24. TPS564201 Transient Response, 1 to 3 A

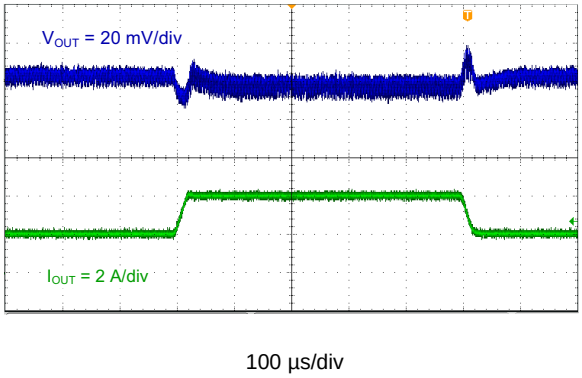


Figure 25. TPS564201 Transient Response, 2 to 4 A

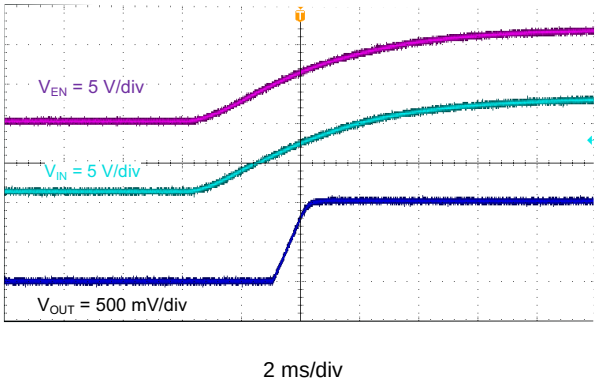


Figure 26. TPS564201 Startup Relative to V_{IN}

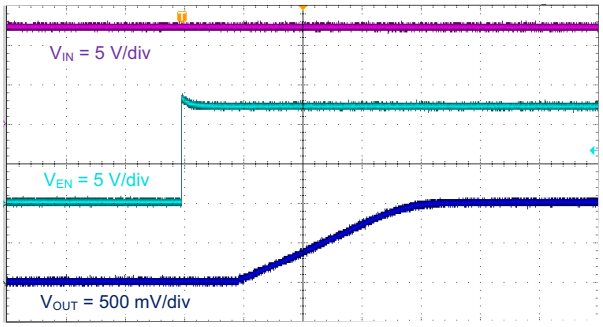


Figure 27. TPS564201 Startup Relative to EN

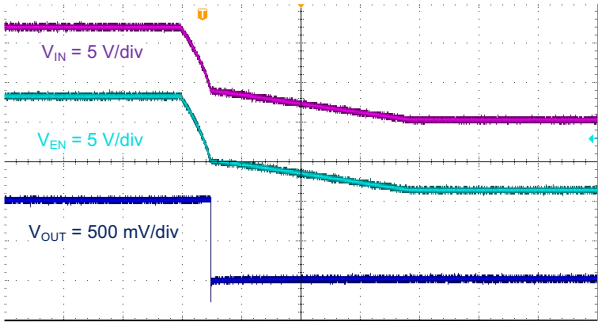


Figure 28. TPS564201 Shutdown Relative to V_{IN}

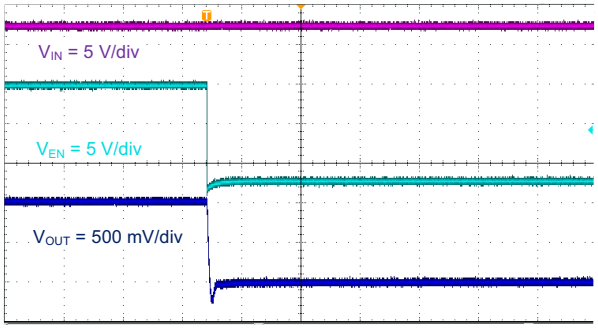


Figure 29. TPS564201 Shutdown Relative to EN

9 Power Supply Recommendations

The TPS564201 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_O / 0.75.

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10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

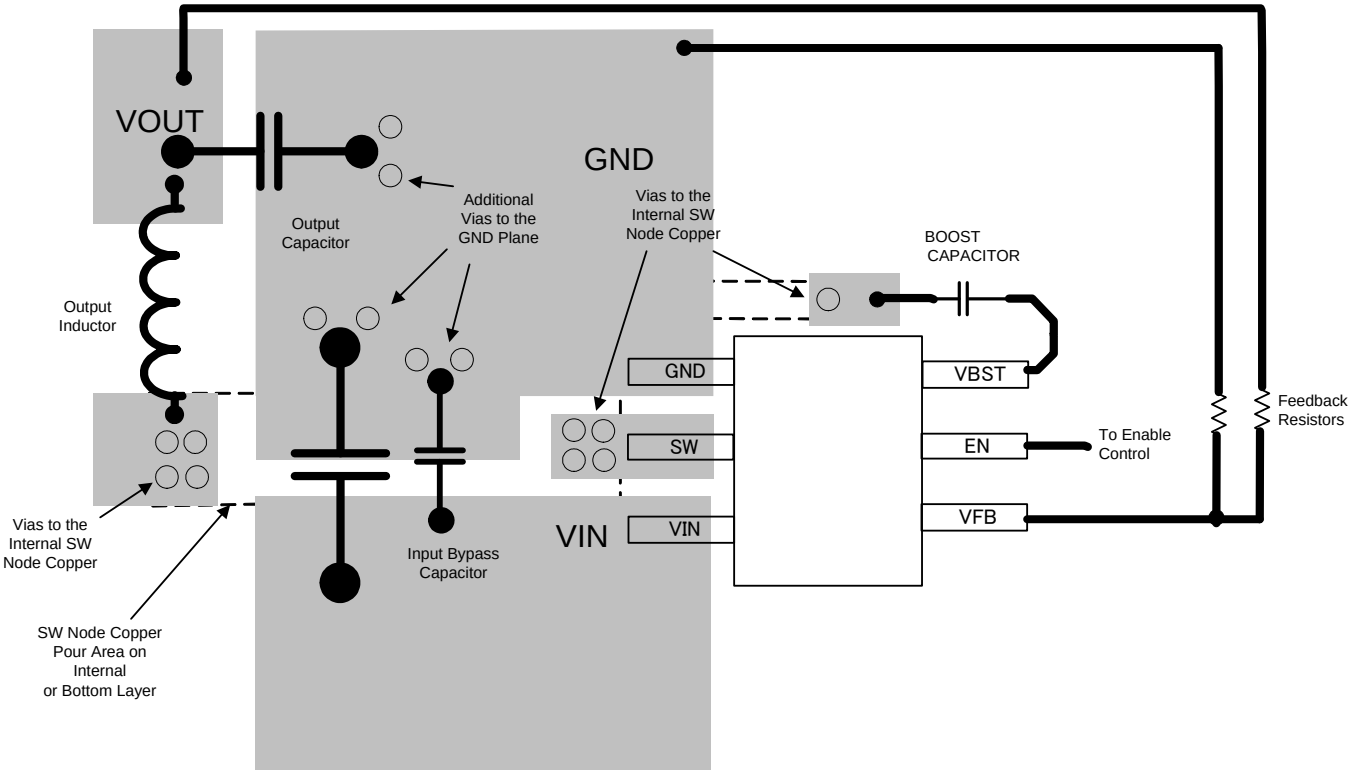


Figure 30. TPS564201 Layout Example

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11 デバイスおよびドキュメントのサポート

11.1 開発サポート

11.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPS564201デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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WEBENCH is a registered trademark of Texas Instruments.
Blu-ray is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS564201DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4201
TPS564201DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4201
TPS564201DDCR.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4201
TPS564201DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4201
TPS564201DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4201
TPS564201DDCT.B	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

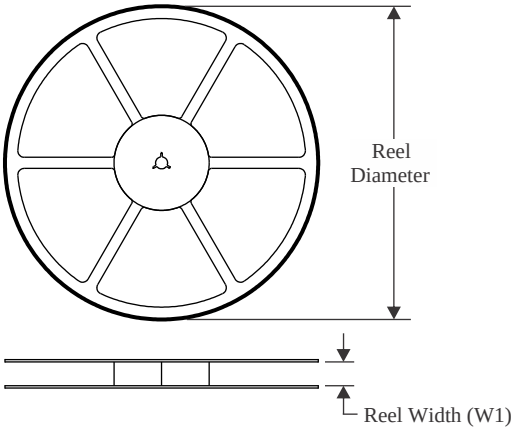
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

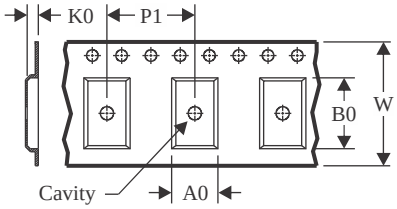
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

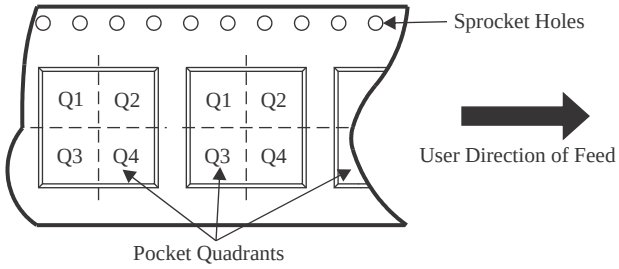


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

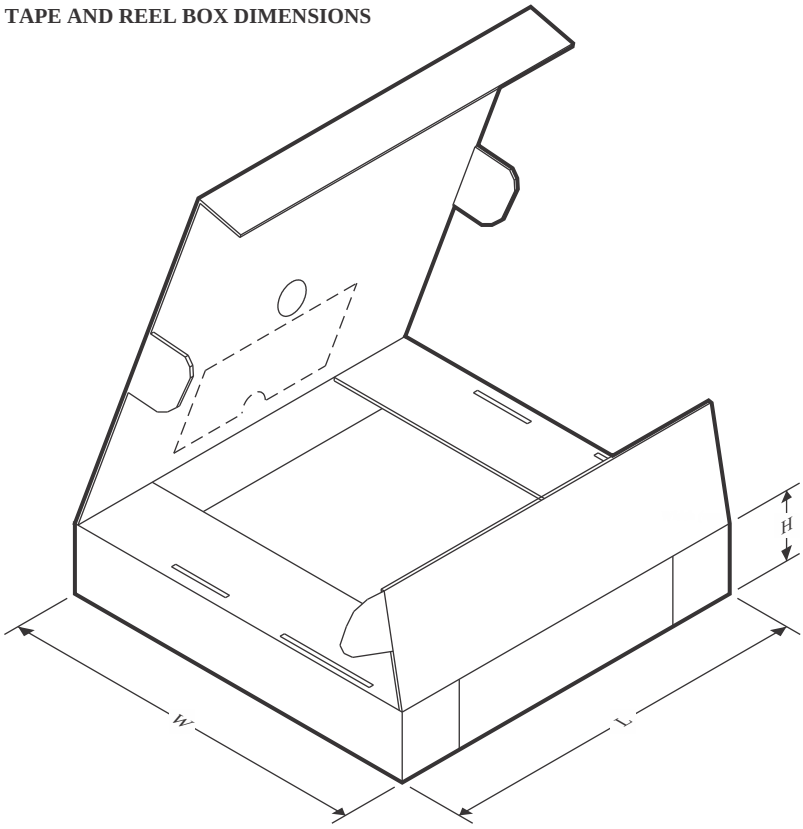
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS564201DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS564201DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS564201DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

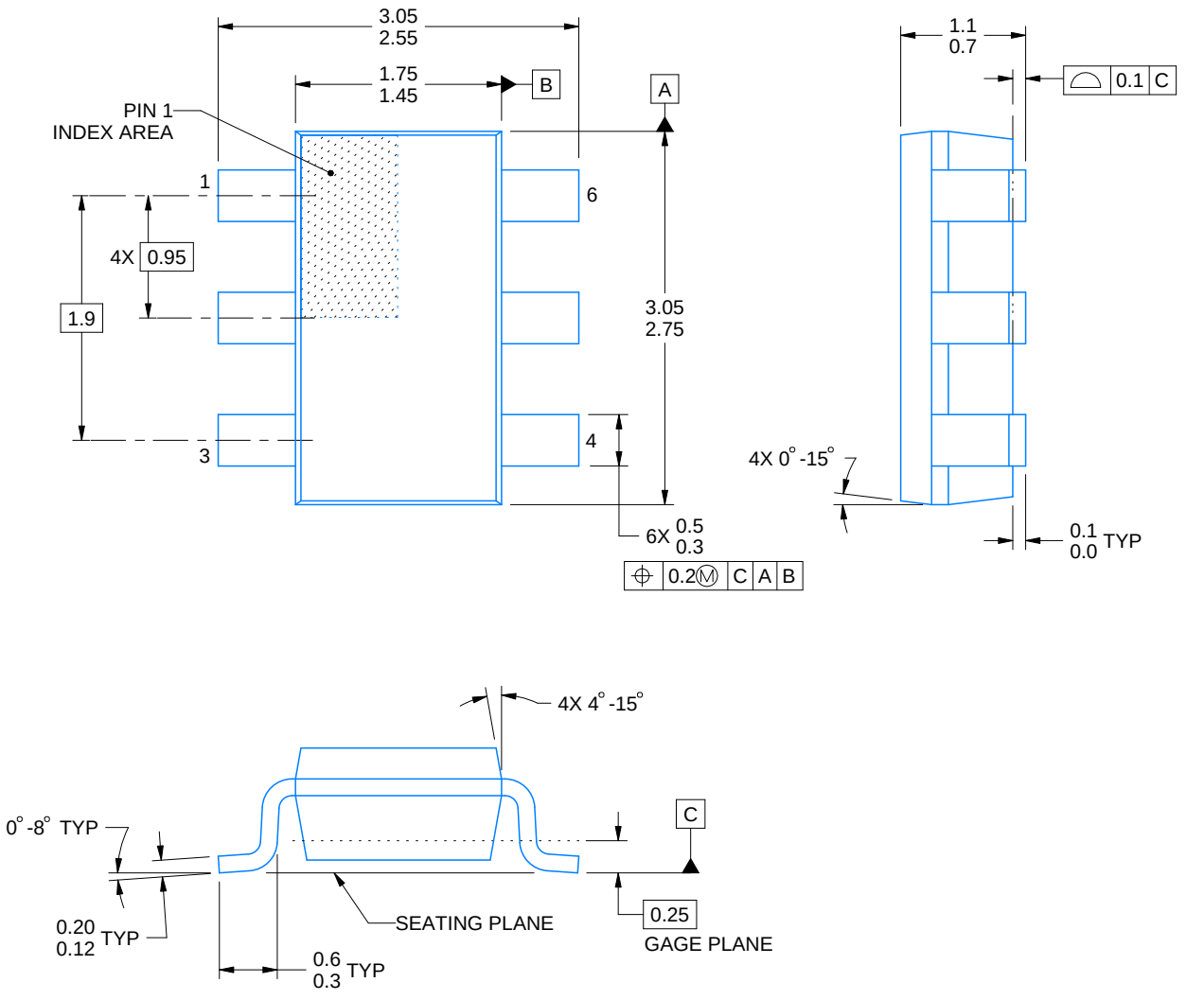
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS564201DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS564201DDCR	SOT-23-THIN	DDC	6	3000	205.0	200.0	30.0
TPS564201DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

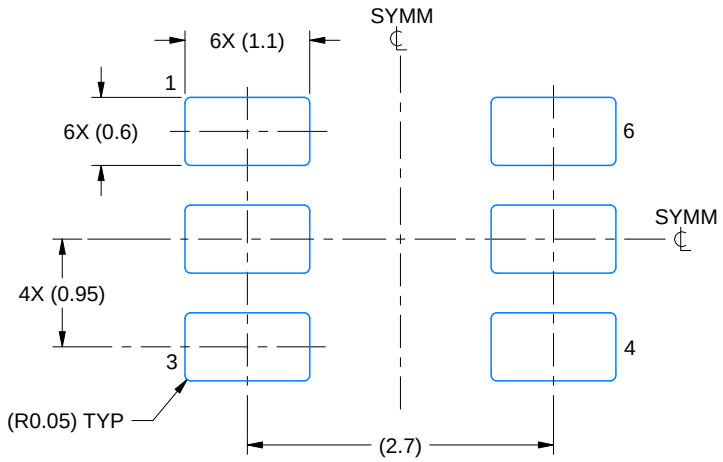
SMALL OUTLINE TRANSISTOR



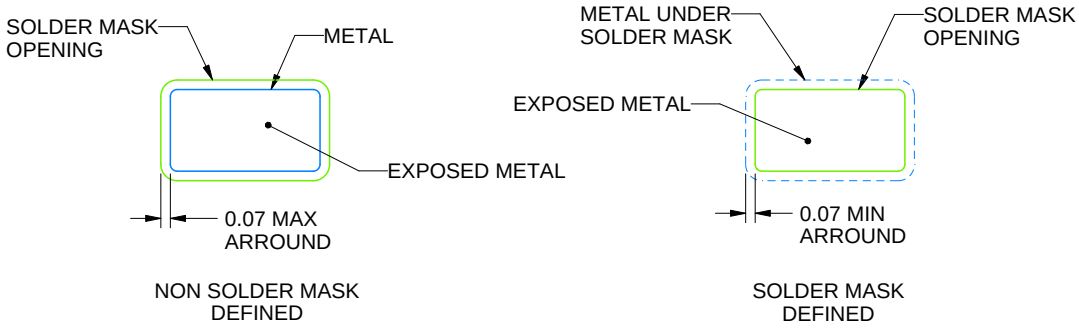
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

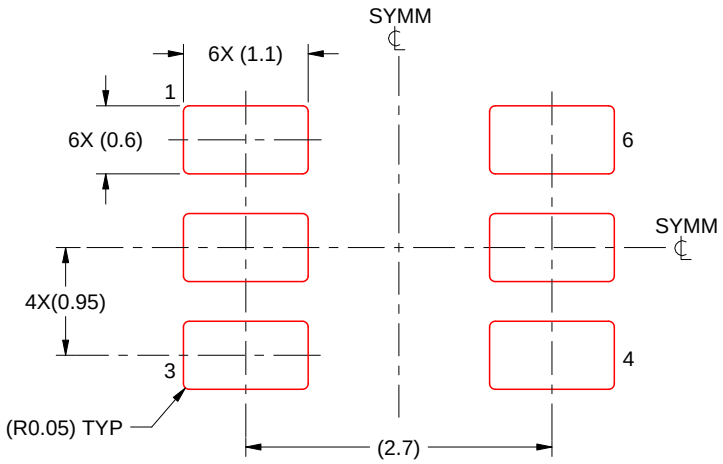


SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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