TEXAS INSTRUMENTS
TPS566231, TPS566238
JAJSJ68B – MAY 2020 – REVISED DECEMBER 2023

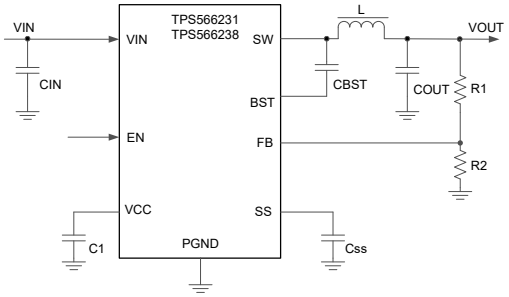
TPS56623x 3V～18V 入力、6A 同期整流降圧電圧レギュレータ

1 特長

- 堅牢なアプリケーション向けの構成
  - 3V ～ 18V の入力電圧範囲
  - 0.6V ～ 7V の出力電圧範囲
  - 連続出力電流:6A
  - 0.6V ±1% の基準電圧 (25℃)
  - 最大デューティ・サイクル:98%
  - スイッチング周波数:600kHz
  - 非ラッチ型 OC、OV、UV、OT 保護
  - 出力放電機能を内蔵
- 多数のピン互換のオプション
  - TPS566231 および TPS566238 は、SS ピンを使用してソフト・スタート時間を調整可能
  - TPS566231P および TPS566238P はパワー グッド インジケータ用 PG ピンを搭載
  - TPS566231 および TPS566231P は自動スキップ・モードに対応
  - TPS566238 と TPS566238P は連続電流モードに対応
- 中国語のデータシートが利用可能です
- 小型の設計サイズと使いやすさ
  - $R_{DS(ON)}$ が 20.8mΩ および 10.6mΩ のパワー MOSFET を内蔵
  - D-CAP3™ 制御モードによる高速過渡応答と内部補償の制御
  - 1.5mm × 2.0mm の HotRod™ QFN パッケージ
  - WEBENCH® Power Designer により、カスタム設計を作成

2 アプリケーション

- デジタル TV、セットトップ・ボックス、ゲーム機
- サーバー、ストレージ、ネットワークの POL
- 産業用 PC、IP カメラ、ファクトリ・オートメーション・アプリケーション



代表的なアプリケーション

3 概要

TPS56623x は、QFN 9 ピン、1.5mm × 2.0mm パッケージに封止された、シンプルで使いやすい高効率の 6A 同期整流降圧コンバータです。

本デバイスは 3V～18V の広い電源電圧範囲で動作します。D-CAP3 制御モードを採用しているため、高速過渡応答や、優れたライン・レギュレーションと負荷レギュレーションを実現し、外部補償が不要で、ESR の小さい出力コンデンサを使用できます。

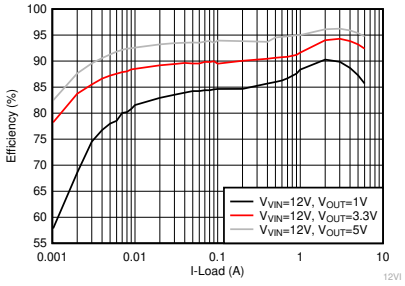
TPS566231 および TPS566231P は軽負荷時には Eco-mode で動作し、高い効率を実現します。これらのデバイスは ULQ™ DC/DC コンバータとして設計されているため、静止電流は 50μA となり、低消費電力アプリケーションにおいて長いバッテリ寿命を実現できます。TPS566238 および TPS566238P は連続電流モードで動作するため、あらゆる負荷条件において出力リップルを低減できます。

TPS566231 および TPS566238 のソフト・スタート時間は、SS ピンを使用して調整できます。TPS566231P および TPS566238P は、PG ピン経由でパワー・グッドを示します。

TPS56623x は最大 98% のデューティ・サイクル動作をサポートし、ヒカップ付きの OVP、OCP、UVLO、OTP、UVP による完全な保護機能が組み込まれています。これらのデバイスは、9 ピン、1.5mm × 2.0mm の HotRod パッケージでそれぞれ供給されます。接合部温度の仕様は -40℃～125℃です。

製品情報

部品番号	軽負荷時のモード	ピン 9 の定義
TPS566231	自動スキップ モード	ソフト スタート ピン
TPS566238	連続電流モード	ソフト スタート ピン
TPS566231P	自動スキップ モード	パワー グッド ピン
TPS566238P	連続電流モード	パワー グッド ピン



TPS566231 の効率と出力電流との関係

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

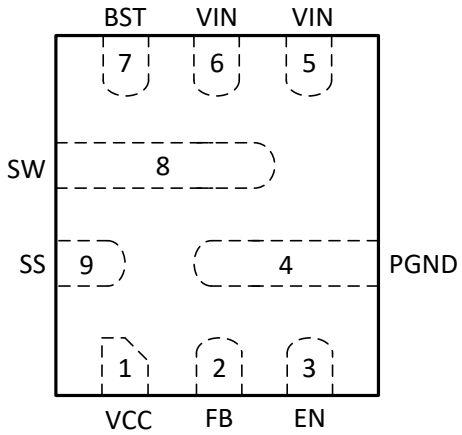


図 4-1. TPS566231, TPS566238 9-Pin RQF, VQFN-HR Package (Top View)

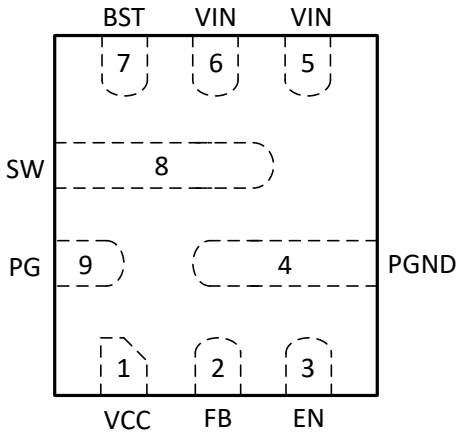


図 4-2. TPS566231P, TPS566238P 9-Pin RQF, VQFN-HR Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VCC	1	O	5.0-V internal VCC LDO output. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 1-µF capacitor. If V_{VIN} is lower than 5 V, VCC follows the V_{IN} voltage.
FB	2	I	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and ground.
EN	3	I	Enable pin of buck converter. The EN pin is a digital input pin, so the pin decides to turn on or turn off the buck converter. If the EN pin is open, the internal pullup current occurs to enable converter.
PGND	4	G	Ground pin. Power ground return for the switching circuit. Connect sensitive SS and FB returns to PGND at a single point.
VIN	5, 6	P	Input voltage supply pin. Connect the input decoupling capacitors between VIN and PGND.
BST	7	O	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW. TI recommends 0.1 µF.
SW	8	O	Switch node terminal. Connect the output inductor to this pin.
SS/PG	9	O	TPS566231 and TPS566238 soft-start control pin. Connecting an external capacitor sets the soft-start time.
		O	TPS566231P and TPS566238P open-drain power good indicator. This pin is asserted low if output voltage is out of PG threshold, over voltage, or if the device is under thermal shutdown, EN shutdown, or during soft start.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Input voltage	VIN	–0.3	20	V
		BST	–0.3	26	V
		BST (10-ns transient)	-0.3	28	V
		BST-SW	–0.3	7	V
		VIN-SW		22	V
		VIN-SW (10-ns transient)		25.5	V
		SS, FB, EN, PG	–0.3	6	V
		PGND	–0.3	0.3	V
	Output voltage	SW	–2	20	V
		SW (10-ns transient)	–5.5	22	V
		VCC	–0.3	6	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	VIN	3	18	V
		BST	–0.1	23.5	V
		BST-SW	–0.1	5.5	V
		SS, FB, EN, PG	–0.1	5.5	V
		PGND	–0.1	0.1	V
	Output voltage	SW	–1	18	V
		VCC	–0.1	5.5	V
I_{OUT}	Output current		0	6	A
T_J	Operating junction temperature		–40	125	°C

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5.4 Thermal Information

THERMAL METRIC[1]		TPS566231/8,TPS5662381P/8P RQF(VQFN) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.6	°C/W
$R_{\theta JA_effective}$	Junction-to-ambient thermal resistance with TI EVM	44	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = -40ºC to 125ºC, V_{IN}=12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range	VIN	3		18	V
I_{VIN}	VIN supply current	No load, V_{EN} = 5V, non-switching (TPS566231/1P)	25	50	75	µA
		No load, V_{EN} = 5V, non-switching (TPS566238/8P)	275	375	475	µA
I_{INSDN}	VIN shutdown current	No load, V_{EN} = 0V		3.2	5	µA
UVLO						
$V_{UVLOVIN}$	VIN UVLO threshold	Wake up VIN voltage	2.62	2.74	2.86	V
		Shut down VIN voltage	2.44	2.54	2.64	V
		Hysteresis VIN voltage		200		mV
VCC OUTPUT						
V_{CC}	VCC output voltage	V_{IN} = 12V	4.7	5	5.2	V
		V_{IN} = 3V		3		V
I_{CC}	VCC current limit	V_{IN}=12V	20			mA
		V_{IN} = 3V	5			mA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	594	600	606	mV
		T_J = –40°C to 125°C	591	600	609	mV
MOSFET						
$R_{DS\ (ON)HI}$	High-side MOSFET Rds(on)	T_J = 25°C, V_{IN} ≥ 5V		20.8		mΩ
		T_J = 25°C, V_{IN} = 3V		25.8		mΩ
$R_{DS\ (ON)LO}$	Low-side MOSFET Rds(on)	T_J = 25°C,V_{IN} ≥ 5V		10.6		mΩ
		T_J = 25°C, V_{IN} = 3V		13		mΩ
I_{OCL}	Over current threshold	Valley current set point	6.1	7.4	8.9	A
I_{NOCL}	Negative over current threshold		2	3.4	5.3	A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	T_J = 25°C, V_{VOUT} = 1.0V		600		kHz
$T_{ON(MIN)}$	Minimum on-time[1]	T_J = 25°C		50	90	ns
$T_{OFF(MIN)}$	Minimum off-time[1]	V_{FB} = 0.5V		100		ns

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5.5 Electrical Characteristics (続き)

T_J = -40ºC to 125ºC, V_{IN}=12 V (unless otherwise noted)

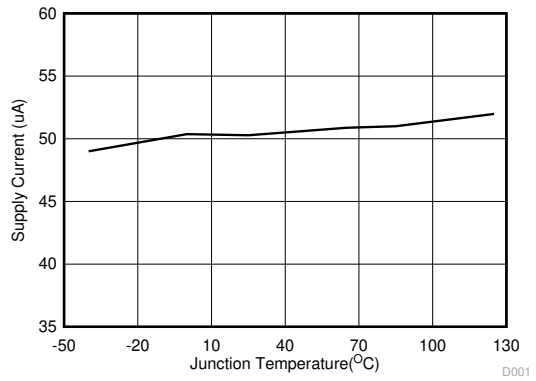
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN threshold high-level		1.13	1.19	1.25	V
$V_{EN(OFF)}$	EN threshold low-level		1.01	1.08	1.16	V
V_{ENHYS}	EN hysteresis			110		mV
I_{EN}	EN pullup current	V_{EN} = 1.0V		2		uA
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge resistance	T_J = 25°C, V_{VOUT} = 0.5V, V_{EN} = 0V		114		Ω
I_{SS}	Soft-start charge current	TPS566231/TPS566238	5	6.5	8.5	uA
T_{SS}	Internal soft-start time	TPS566231P/TPS566238P	0.93	1.9	2.9	ms
POWER GOOD (TPS566231P/TPS566238P)						
T_{PGDLY}	PG start-up delay	PG from low-to-high		1		ms
		PG from high-to-low		32		us
V_{PGTH}	PG threshold	VFB falling (fault)	80	85	90	%
		VFB rising(good)	85	90	95	%
		VFB rising (fault)	110	115	120	%
		VFB falling (good)	105	110	115	%
V_{PG_L}	PG sink current capability	I_{OL} = 4mA			0.4	V
I_{PGLK}	PG leak current	V_{PGOOD} = 5.5V			1	uA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold		110	115	120	%
t_{OVPDLY}	OVP prop deglitch	T_J = 25°C		32		us
V_{UVP}	UVP trip threshold		55	60	65	%
t_{UVPDLY}	UVP prop deglitch			256		us
t_{UVPDEL}	Output hiccup delay relative to SS time	UVP detect		256		us
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect (TPS566231/TPS566238)		7		cycles
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect (TPS566231P/ TPS566238P)		19		ms
THERMAL PROTECTION						
T_{OTP}	OTP trip threshold(1)			160		°C
T_{OTPHSY}	OTP hysteresis(1)			25		°C

(1) No production test, specified by design.

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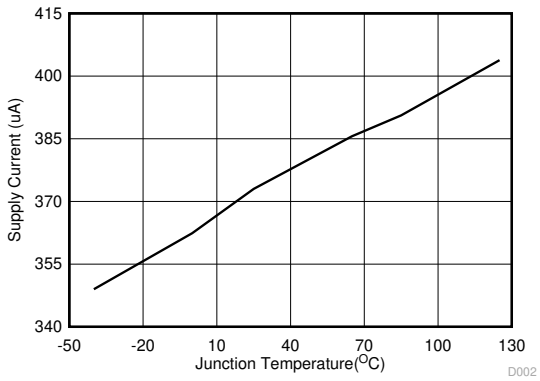
5.6 Typical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)



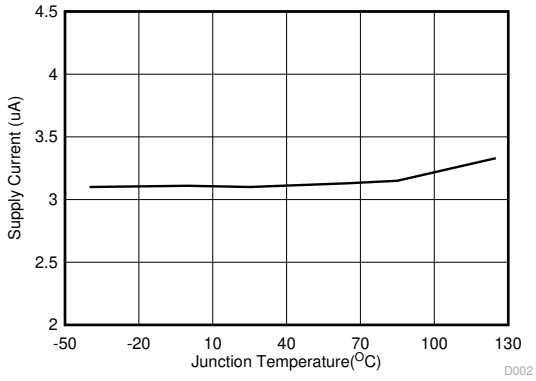
V_{EN} = 5 V TPS566231

図 5-1. Supply Current vs Junction Temperature



V_{EN} = 5 V TPS566238

図 5-2. Supply Current vs Junction Temperature



V_{EN} = 0 V

図 5-3. Shutdown Current vs Temperature

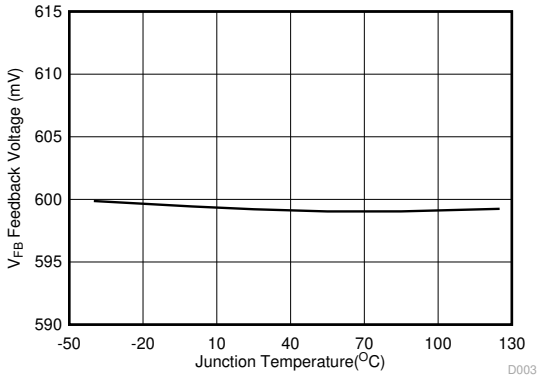


図 5-4. Feedback Voltage vs Junction Temperature

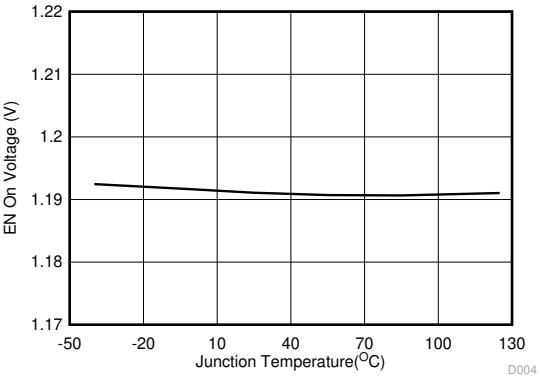


図 5-5. Enable-On Voltage vs Junction Temperature

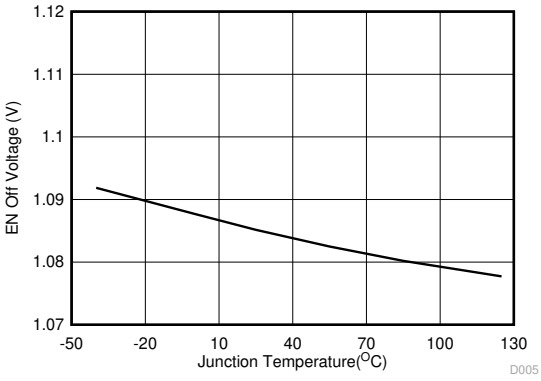
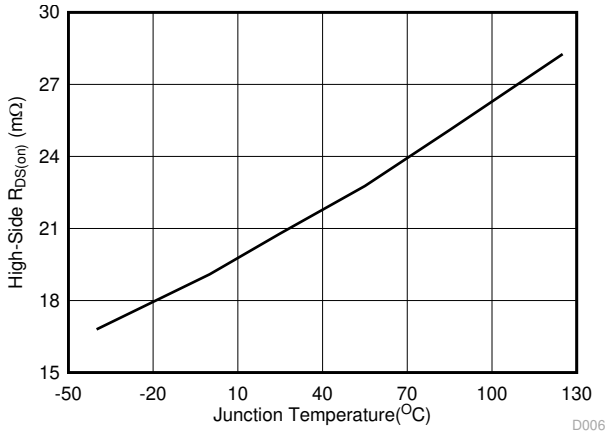


図 5-6. Enable-Off Voltage vs Junction Temperature

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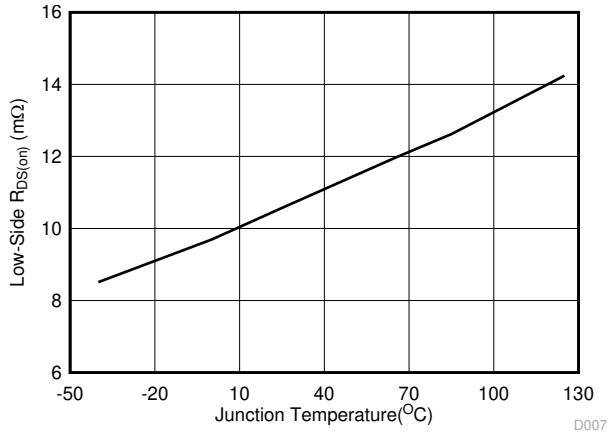
5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)



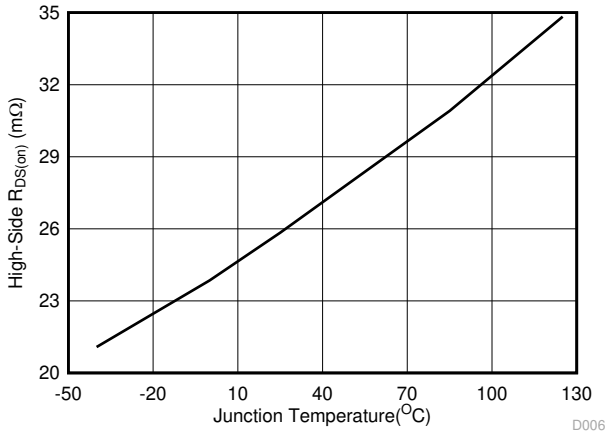
V_{IN} = 12 V

図 5-7. High-Side R_{DS}(on) vs Junction Temperature



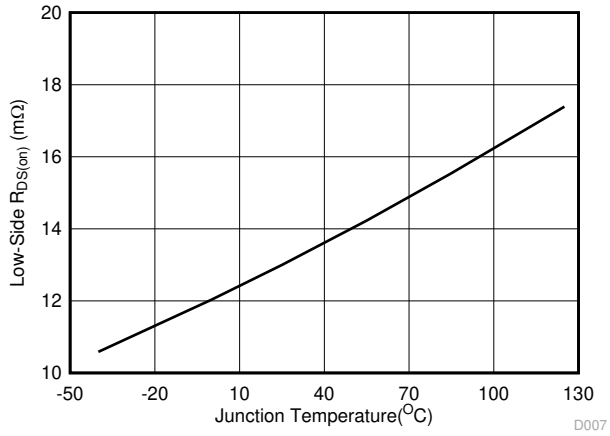
V_{IN} = 12 V

図 5-8. Low-Side $R_{DS(on)}$ vs Junction Temperature



V_{IN} = 3 V

図 5-9. High-Side R_{DS}(on) vs Junction Temperature



V_{IN} = 3 V

図 5-10. Low-Side $R_{DS(on)}$ vs Junction Temperature

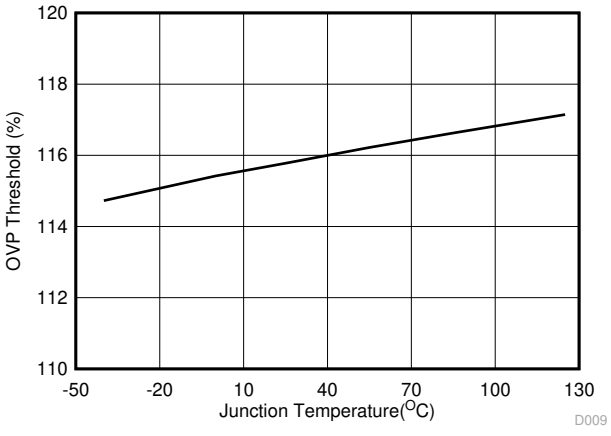


図 5-11. OVP Threshold vs Junction Temperature

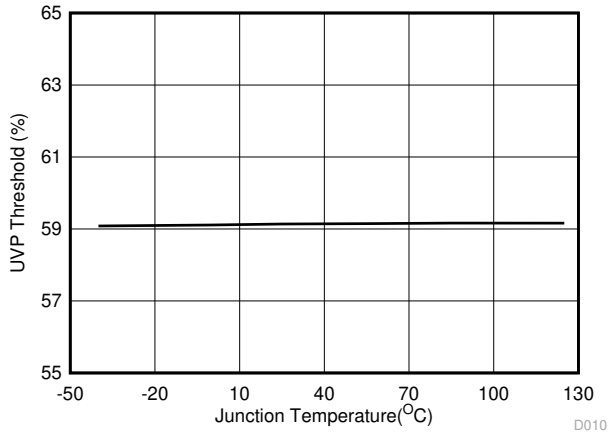


図 5-12. UVP Threshold vs Junction Temperature

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5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

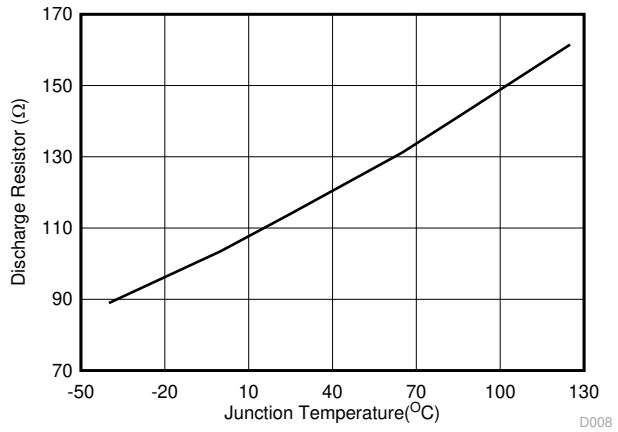


図 5-13. Discharge Resistor vs Junction Temperature

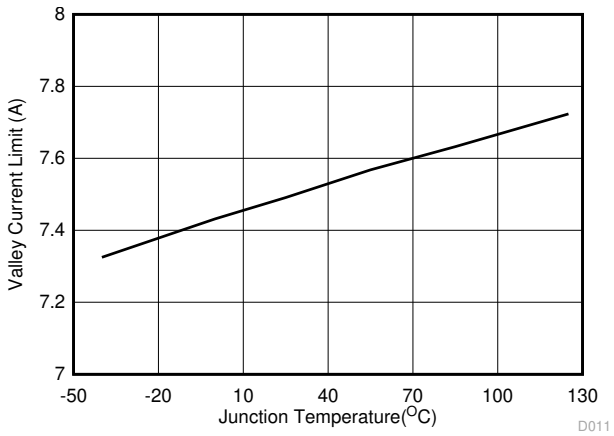
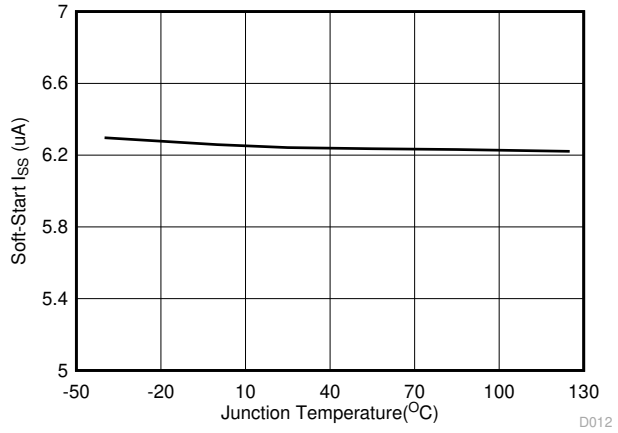
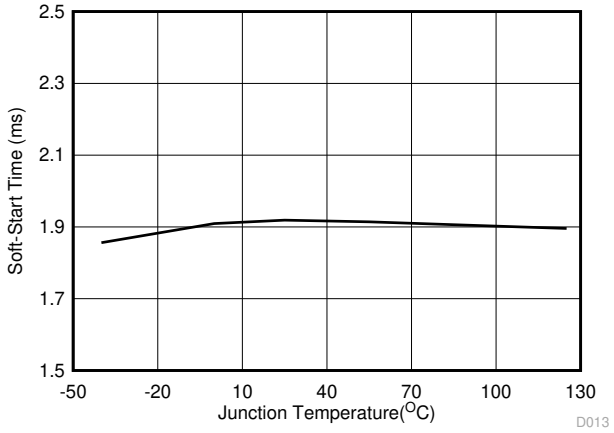


図 5-14. Valley Current Limit vs Junction Temperature



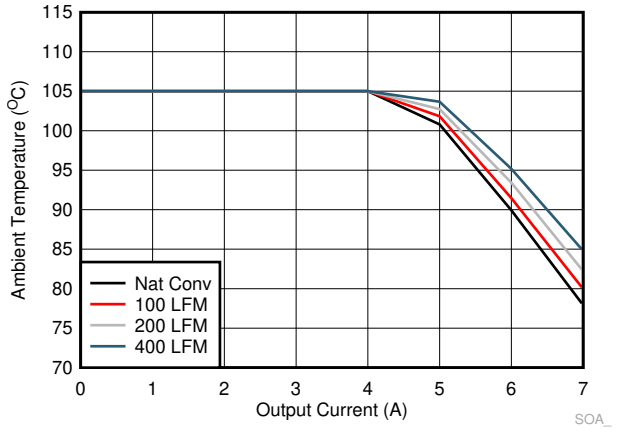
TPS566231 and TPS566238

図 5-15. Soft-Start Charge Current Iss vs Junction Temperature



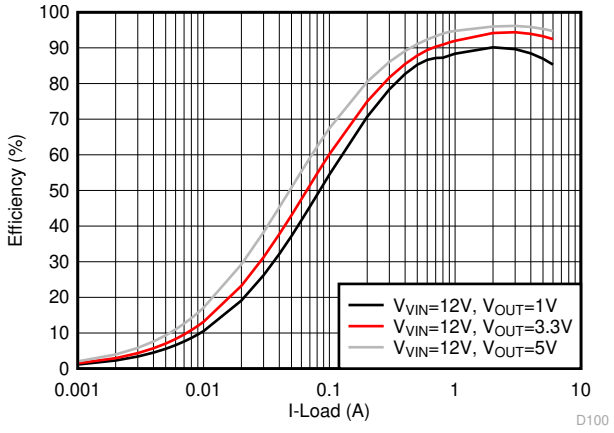
TPS566231P and TPS566238P

図 5-16. Soft-Start Time vs Junction Temperature



V_{IN} = 12 V V_{OUT} = 1.0 V

図 5-17. Safe Operating Area



V_{IN} = 12 V

図 5-18. TPS566238 and TPS566238P Efficiency

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5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

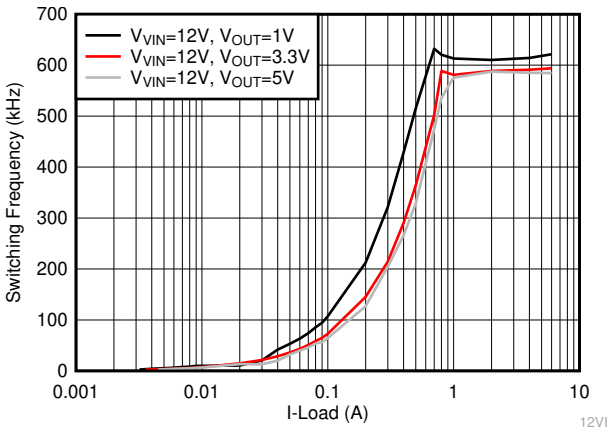


図 5-19. TPS566231 and TPS566231P F_{SW} Load Regulation

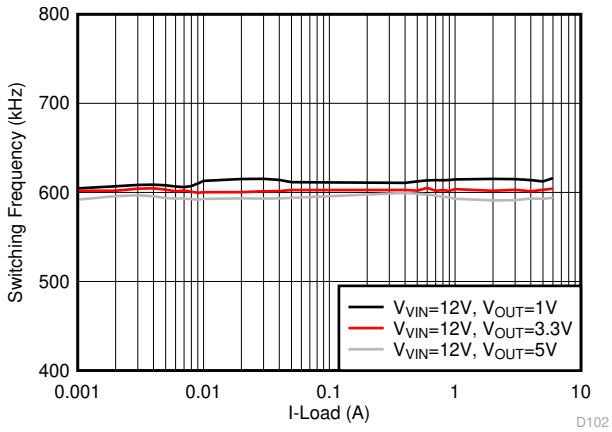


図 5-20. TPS566238 and TPS566238P F_{SW} Load Regulation

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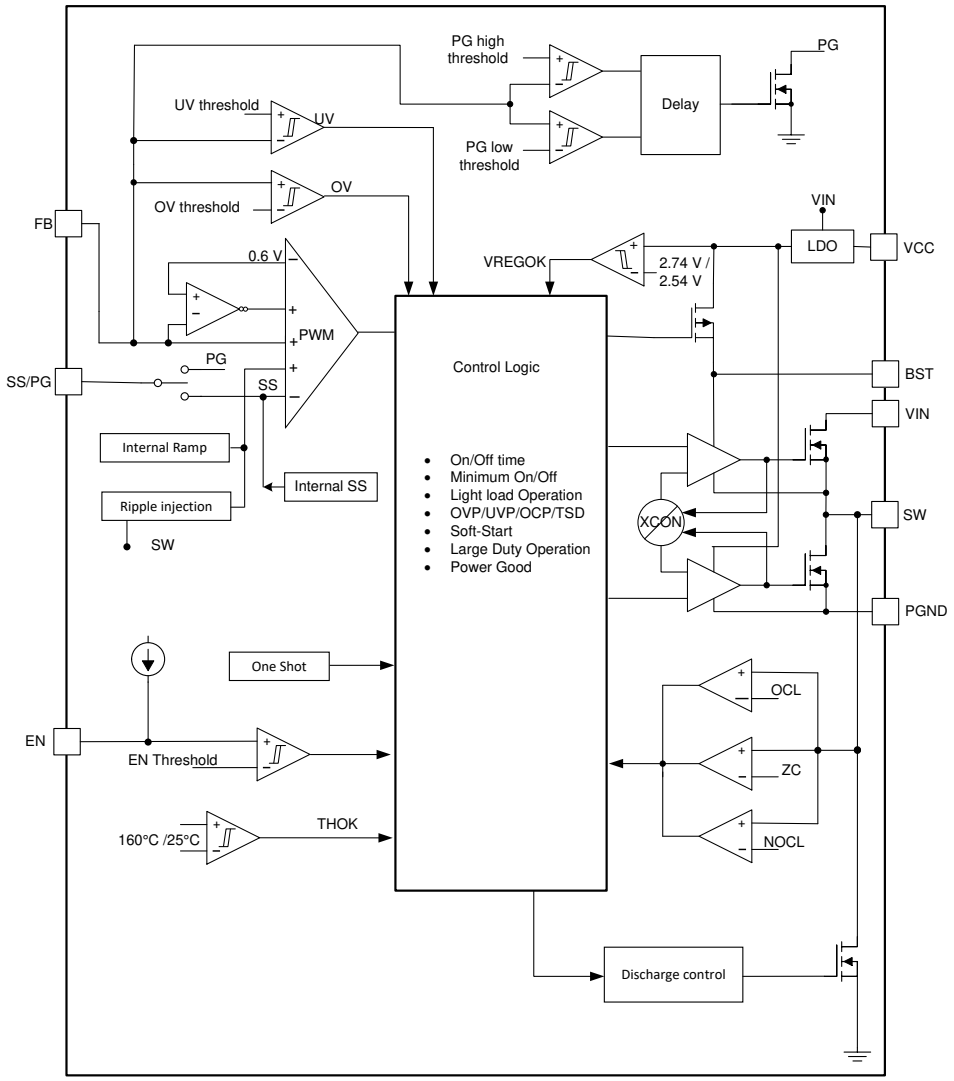
6 Detailed Description

6.1 Overview

The TPS56623x is a 6-A, integrated, FET, synchronous buck converter that operates from 3-V to 18-V input voltage (V_{IN}) and 0.6-V to 7-V output voltage. The proprietary D-CAP3 control mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. As the ULQ ™ DC/DC converter, the device enables long battery life in system standby mode and high efficiency under light load conditions. The devices employ D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides a seamless transition between CCM operating mode in heavier load conditions and DCM operation in lighter load conditions.

Eco-mode allows the TPS566231 and TPS566231P to maintain high efficiency at light load. The TPS566238 and TPS566238P work in continuous current mode to maintain lower output ripple in all load conditions. The soft-start time of the TPS566231 and TPS566238 can be adjusted through the SS pin. The TPS566231P and TPS566238P indicate power good through the PG pin. The devices are able to adapt to both low equivalent series resistance (ESR) output capacitors, such as POS-CAP or SP-CAP, and ultra-low ESR ceramic capacitors.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS56623x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}. This is done to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple. This enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the devices is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in 式 1.

$$f_p = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{1}$$

At low frequency, the overall loop gain is set by the output setpoint resistor divider network and the internal gain of the TPS56623x. The low-frequency L-C double pole has a 180 degree drop in-phase. At the output filter frequency, the gain rolls off at a –40-dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain rolloff from –40-dB to –20-dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is approximately 45 kHz. The inductor and capacitor selected for the output filter is recommended such that the double pole is located close to 1/3 the high-frequency zero. This is done so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system usually must be targeted to be less than one-third of the switching frequency (F_{SW}).

6.3.2 Soft Start

The TPS566231 and TPS566238 have an external SS pin to set the soft-start time. When the EN pin becomes high, the soft start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a longer soft-start time than 0.5 ms, the time can be set by connecting a capacitor on the SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and ground. The devices track the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The estimated equation for the soft-start time (T_{SS}) is shown in 式 2:

$$T_{ss}(ms) = \frac{1.4 \times C_{ss}(nF) \times V_{REF}(V)}{I_{ss}(uA)} \tag{2}$$

where

- V_{REF} is 0.6 V
- I_{SS} is 6.5 µA

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6.3.3 Power Good

The TPS566231P and TPS566238P have the PG pin as a power-good indicator. The PG pin is an open-drain output. After the V_{FB} is between 90% and 110% of the internal reference voltage (V_{REF}), the PG is de-asserted and floats after a 1-ms de-glitch time. TI recommends a 100-kΩ pullup resistor to pull the voltage up to VCC. The PG pin is pulled low when:

- The FB pin voltage is lower than 85% or greater than 115% of the target output voltage
- The device is in an OVP, UVP, or thermal shutdown event
- Or during the soft-start period

6.3.4 Large Duty Operation

The TPS56623x can support large duty operations by smoothly dropping down the switching frequency. When V_{IN} / V_{OUT} < 1.6 and the V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make T_{ON} extended. This action is done to implement large duty operation and also improve the performance of the load transient performance. The minimum switching frequency is limited with about 165 kHz with typical 100-ns minimum off-time. The TPS56623x can support up to 98% duty cycle operation.

6.3.5 Overcurrent Protection and Undervoltage Protection

The TPS56623x has overcurrent protection and undervoltage protection. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- the on-time
- the output inductor value

During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse. This is true even if the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is limited. The output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it and the device shuts off after a 256-µs wait time. The device then restarts after the hiccup time (typically 7 × T_{ss}). When the overcurrent condition is removed, the output is recovered.

6.3.6 Overvoltage Protection

The TPS56623x has the overvoltage protection feature. When the output voltage becomes higher than 115% of the target voltage, the OVP is triggered. The output is discharged after a 32-µs wait time, and both the high-side and low-side MOSFET driver turn off. When the overvoltage condition is removed, the output voltage is recovered.

6.3.7 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the V_{IN} power input. When the voltage is lower than UVLO threshold voltage, the device is shut off and output is discharged. This protection is a non-latch protection.

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6.3.8 Output Voltage Discharge

The TPS56623x has the discharge function by using a 114-Ω $R_{DS(on)}$ internal MOSFET, which discharges the output V_{OUT} through the SW node during any event like the following occurs:

- Output overvoltage protection
- Output undervoltage protection
- TSD
- VCC voltage is below the UVLO
- EN pin voltage (V_{EN}) is below the turn-on threshold

The discharge is slow due to the lower current capability of the MOSFET.

6.3.9 Thermal Shutdown

The TPS56623x monitors the internal die temperature. If the temperature exceeds the threshold value (typically 160°C), the device is shut off and the output is discharged. This protection is a non-latched protection. The device restarts switching when the temperature goes below the thermal shutdown threshold.

6.4 Device Functional Modes

6.4.1 Advanced Eco-mode Control

The TPS566231 and TPS566231P operate in advanced Eco-mode mode, which maintains high light-load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually the rippled valley touches zero level. This is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use 式 3 to calculate the light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately 20% to 30% of $I_{OUT(max)}$ (peak current in the application). Make sure to size the inductor properly so that the valley current does not hit the negative low-side current limit.

6.4.2 Force CCM Mode

The TPS566238 and TPS566238P operate in Force CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light-load conditions. FCCM allows the inductor current to become negative. During FCCM mode, the switching frequency (F_{SW}) is maintained at an almost constant level over the entire load range. This is an excellent choice for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

6.4.3 Standby Operation

The TPS56623x can be placed in standby mode by pulling the EN pin low. The device operates with 3.2-µA shutdown current in standby condition. The EN pin is pulled high internally. When floating, the part is enabled by default.

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7 Application and Implementation

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7.1 Application Information

The schematic in 図 7-1 shows a typical application for the TPS566231 with 1-V output. This design converts an input voltage range of 3 V to 18 V down to 1 V with a maximum output current of 6 A.

7.2 Typical Application

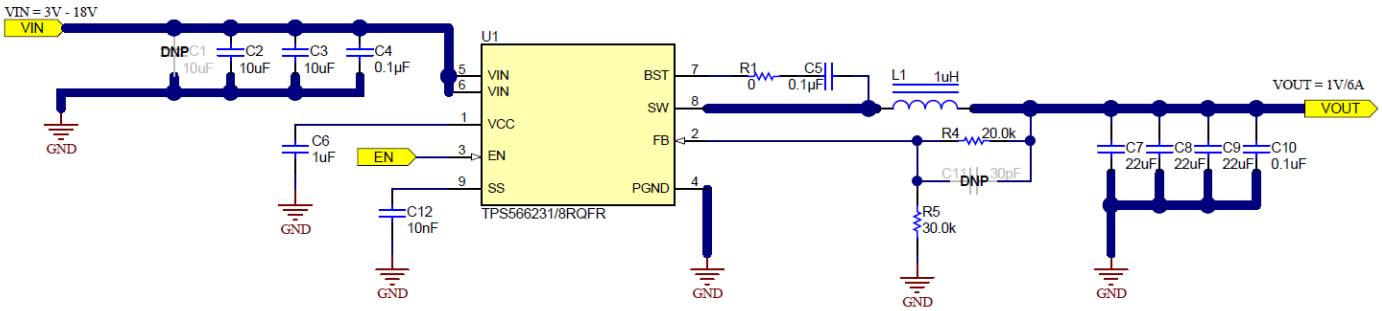


図 7-1. 1-V, 6-A Reference Design

7.2.1 Design Requirements

表 7-1 lists the design parameters for this example.

表 7-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1		V
I_{OUT}	Output current			6		A
ΔV_{OUT}	Transient response	0.1-A – 6-A load step, 2.5 A/µs		±50		mV
V_{IN}	Input voltage		3	12	18	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		14		$mV_{(P-P)}$
F_{SW}	Switching frequency			600		kHz
T_A	Ambient temperature			25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS56623x device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Estimate IC thermal and efficiency performance

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- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Voltage Setpoint

To change the output voltage of the application, changing the value of the upper feedback resistor is necessary. By changing this resistor, the user can change the output voltage above 0.6 V. See 式 4.

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}}) \quad (4)$$

7.2.2.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See 表 7-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 式 5 and 式 6. Make sure that the inductor is rated to handle these currents.

$$I_{L(RMS)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (5)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{L(ripple)}}{2} \quad (6)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device. This means that choosing an inductor with a saturation current higher than the peak current under current limit condition is safe.

7.2.2.4 Output Capacitor Selection

After selecting the inductor the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 7-2. Please note these values are effective capacitance values which take into account the DC-bias applied on the capacitors. TI does not recommend to choose the combination of *minimum* inductance and *minimum* capacitance or *maximum* inductance and *maximum* capacitance.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)} / I_{OUT(ripple)}$.

表 7-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (μH)			C_{OUT} (μF)		C_{FF} (PF)
			MIN	TYP	MAX	MIN	MAX	
0.6	10	0	0.68	1	4.7	44	220	-
1	30	20	0.68	1	4.7	44	220	-
1.2	20	20	1	1.2	4.7	44	220	-
1.8	20	40	1	1.5	4.7	44	220	0-50
3.3	20	90	1.5	2.2	4.7	44	220	10-100

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表 7-2. Recommended Component Values (続き)

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)			C_{OUT} (µF)		C_{FF} (PF)
			MIN	TYP	MAX	MIN	MAX	
5.0	30	220	1.5	2.2	4.7	44	220	10-100

7.2.2.5 Input Capacitor Selection

The devices require input decoupling capacitors on power supply input V_{IN}. Also, bulk capacitors are needed depending on the application. The minimum input capacitance required is given in 式 7.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (7)$$

TI recommends using high-quality X5R or X7R input decoupling capacitors of 30 µF on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 式 8:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (8)$$

A 1-µF ceramic capacitor is needed for the decoupling capacitor on the VCC pin.

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7.2.3 Application Curves

図 7-2 through 図 7-25 apply to the circuit of 図 7-1. V_{IN} = 12 V, T_A = 25°C unless otherwise specified.

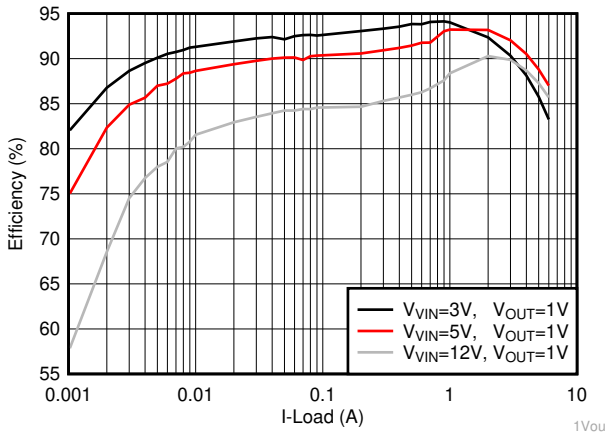


図 7-2. TPS566231 Efficiency Curve

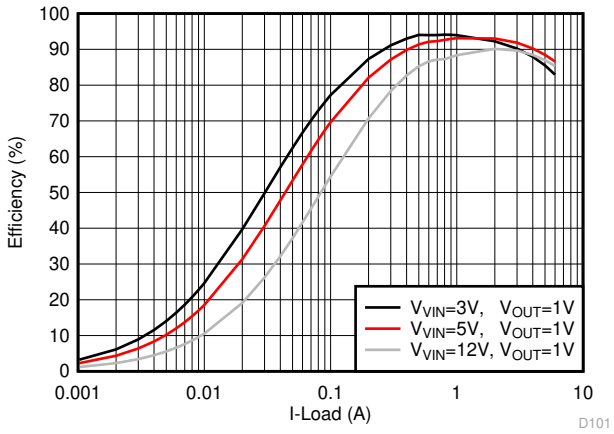


図 7-3. TPS566238 Efficiency Curve

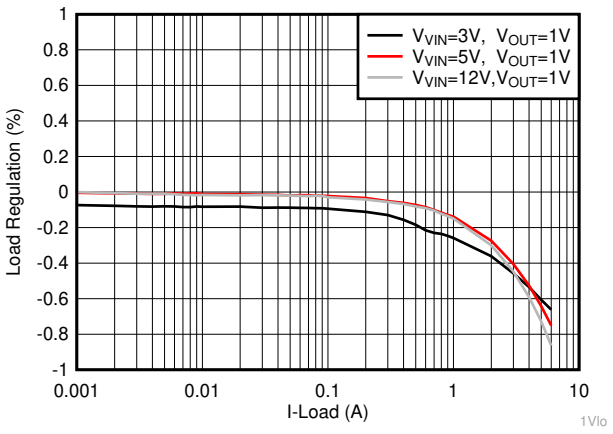


図 7-4. TPS566231 Load Regulation

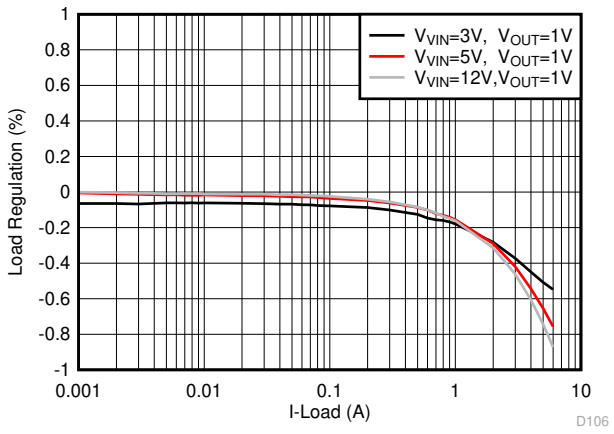


図 7-5. TPS566238 Load Regulation

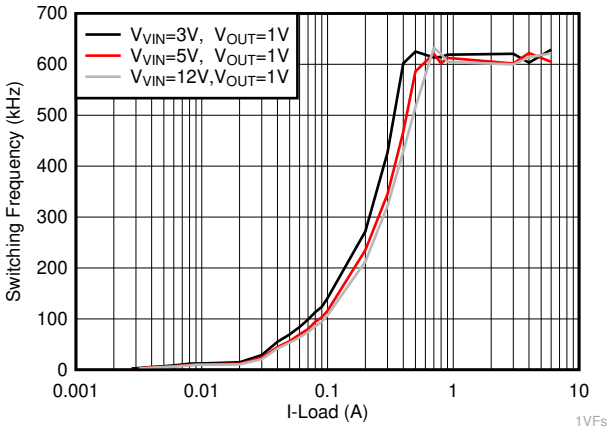


図 7-6. TPS566231 F_{SW} vs Output Load

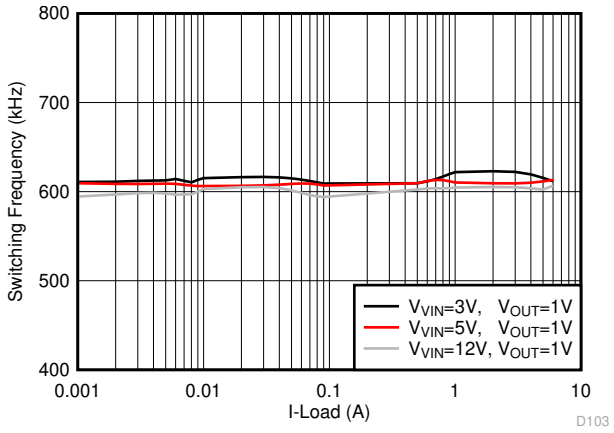
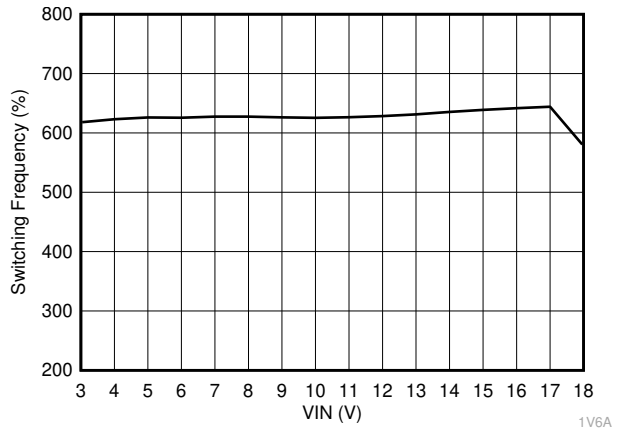


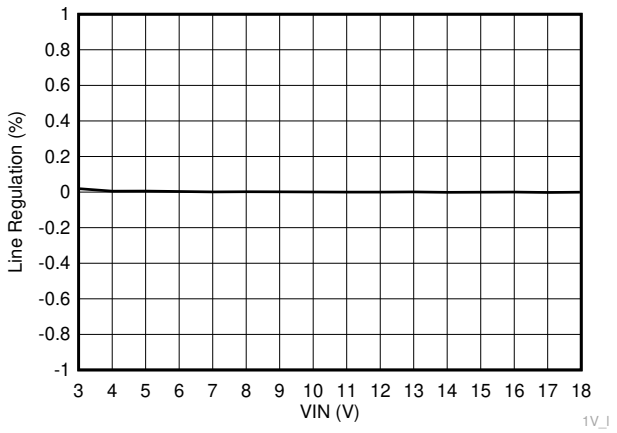
図 7-7. TPS566238 F_{SW} vs Output Load

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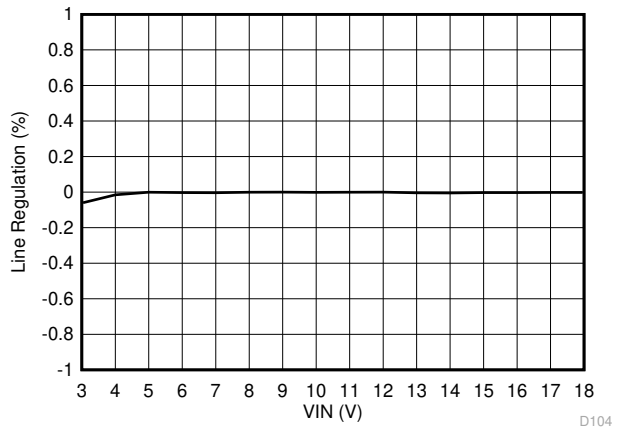
I_{OUT} = 6 A

図 7-8. Switching Frequency vs Input Voltage



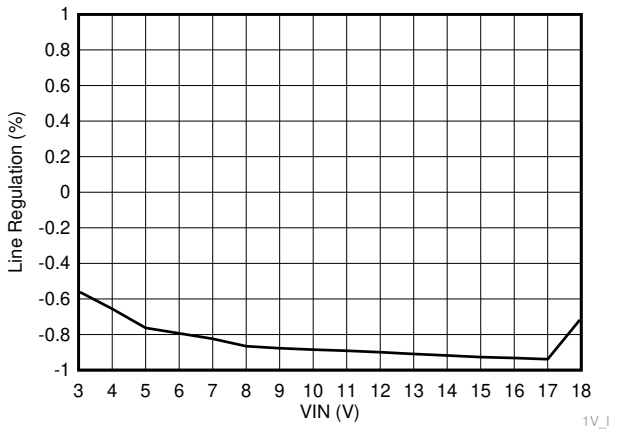
I_{OUT} = 0.1 A

図 7-9. TPS566231 Line Regulation



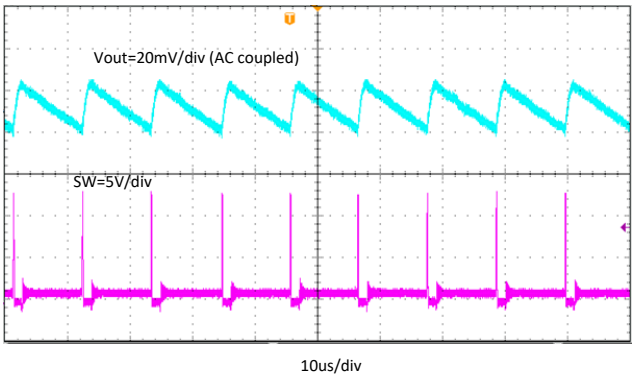
I_{OUT} = 0.1 A

図 7-10. TPS566238 Line Regulation



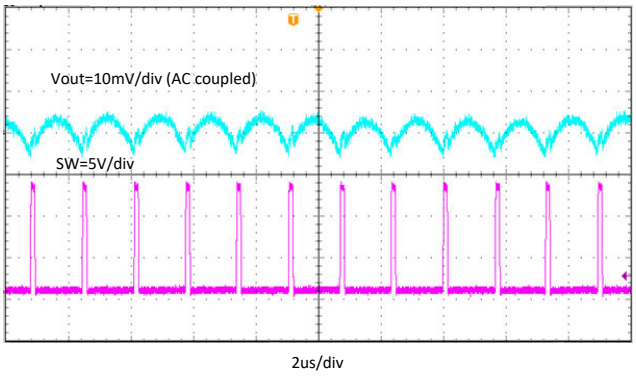
I_{OUT} = 6 A

図 7-11. Line Regulation



I_{OUT} = 0.01 A

図 7-12. TPS566231 Output Voltage Ripple



I_{OUT} = 0.01 A

図 7-13. TPS566238 Output Voltage Ripple

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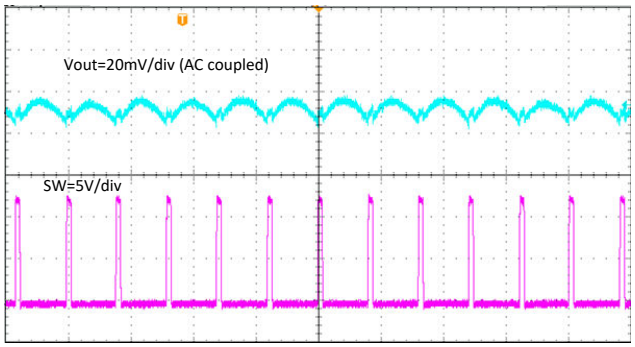


図 7-14. Output Voltage Ripple, I_{OUT} = 6 A

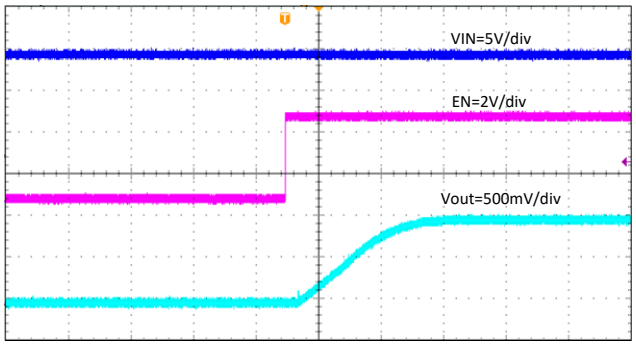


図 7-15. Start-Up Through EN, I_{OUT} = 3 A

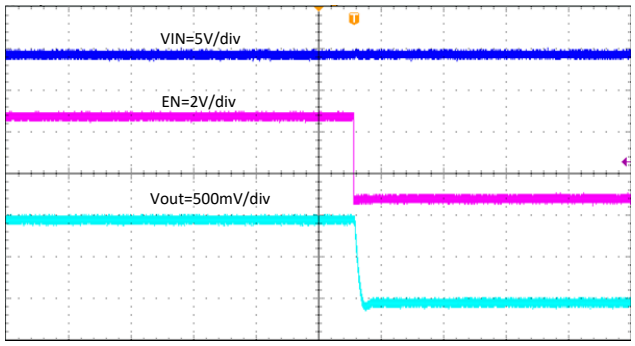


図 7-16. Shutdown Through EN, I_{OUT} = 3 A

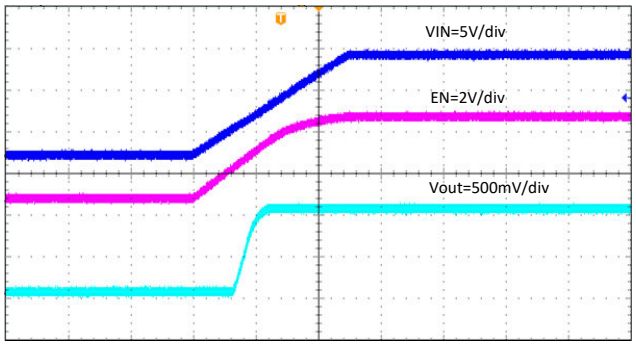


図 7-17. Start-Up with V_{IN} Rising, I_{OUT} = 3 A

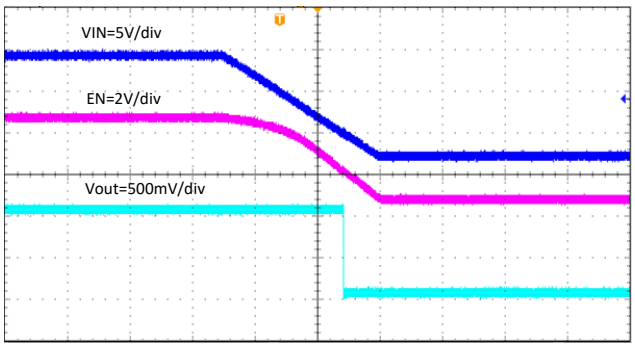


図 7-18. Start-Up with V_{IN} Falling, I_{OUT} = 3 A

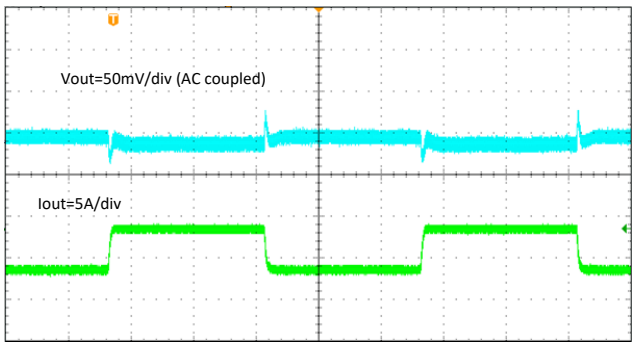
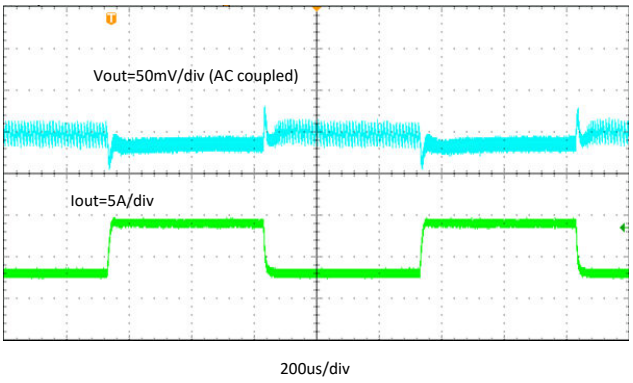
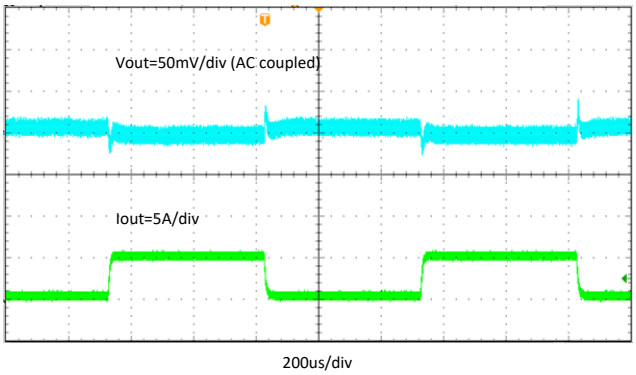


図 7-19. TPS566231 Transient Response



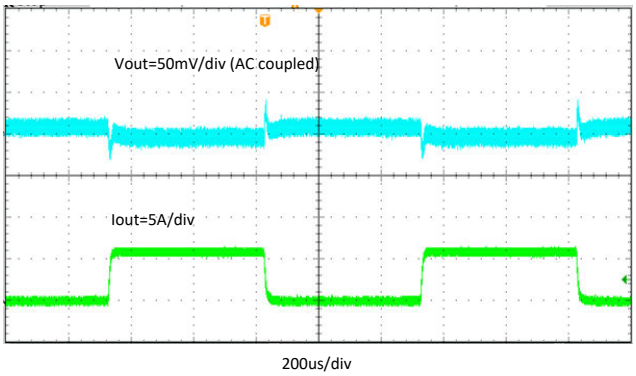
0.1 A to 6 A Slew Rate = 2.5 A/µs

図 7-20. TPS566231 Transient Response



0.6 A to 5.4 A Slew Rate = 2.5 A/µs

図 7-21. TPS566238 Transient Response



0.1 A to 6 A Slew Rate = 2.5 A/µs

図 7-22. TPS566238 Transient Response

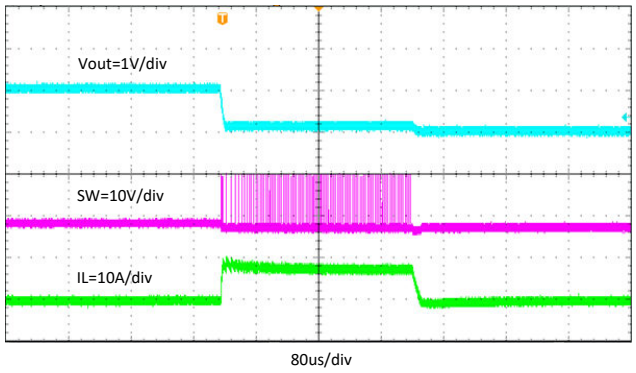


図 7-23. TPS566231 Normal Operation to Output Hard Short

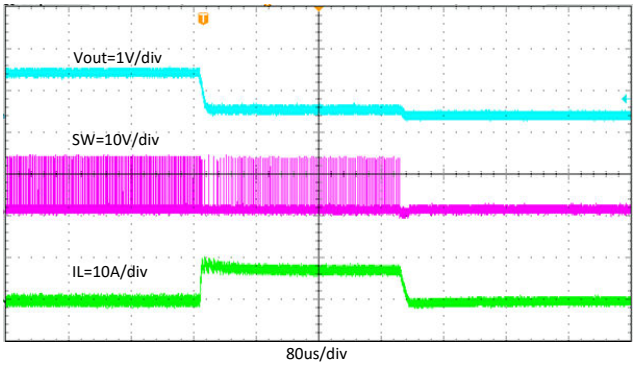


図 7-24. TPS566238 Normal Operation to Output Hard Short

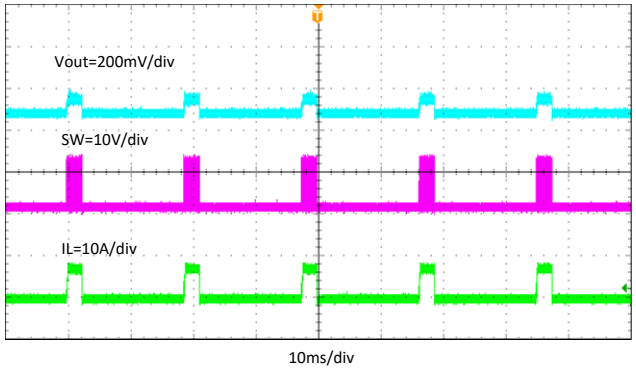


図 7-25. Output Hard Short Hiccup

7.3 Power Supply Recommendations

The TPS56623x is intended to be powered by a well-regulated dc voltage. The input voltage range is 3 V to 18 V. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. TI recommends additional bulk capacitance if the input voltage supply is located far from the TPS56623x circuit. Typical values are 100 µF to 470 µF.

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7.4 Layout

7.4.1 Layout Guidelines

- Use a four-layer PCB for good thermal performance and with maximum ground plane. 55-mm × 60-mm, four-layer PCB with 2-1-1-2 oz copper is used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place an output inductor and capacitors with IC at the same layer. SW routing must be as short as possible to minimize EMI, and must be a width plane to carry big current. Enough vias must be added to the PGND connection of the output capacitor and as close to the output pin as possible.
- Place a BST resistor and capacitor with IC at the same layer, close to BST and SW plane. TI recommends a 15-mil width trace to reduce line parasitic inductance.
- Feedback must be routed away from the switching node, BST node, or other high frequency signal.
- The VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance.

7.4.2 Layout Example

図 7-26 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in 図 7-1. A resistor divider for EN is not used in the circuit of 図 7-1, but are shown in the layout for reference.

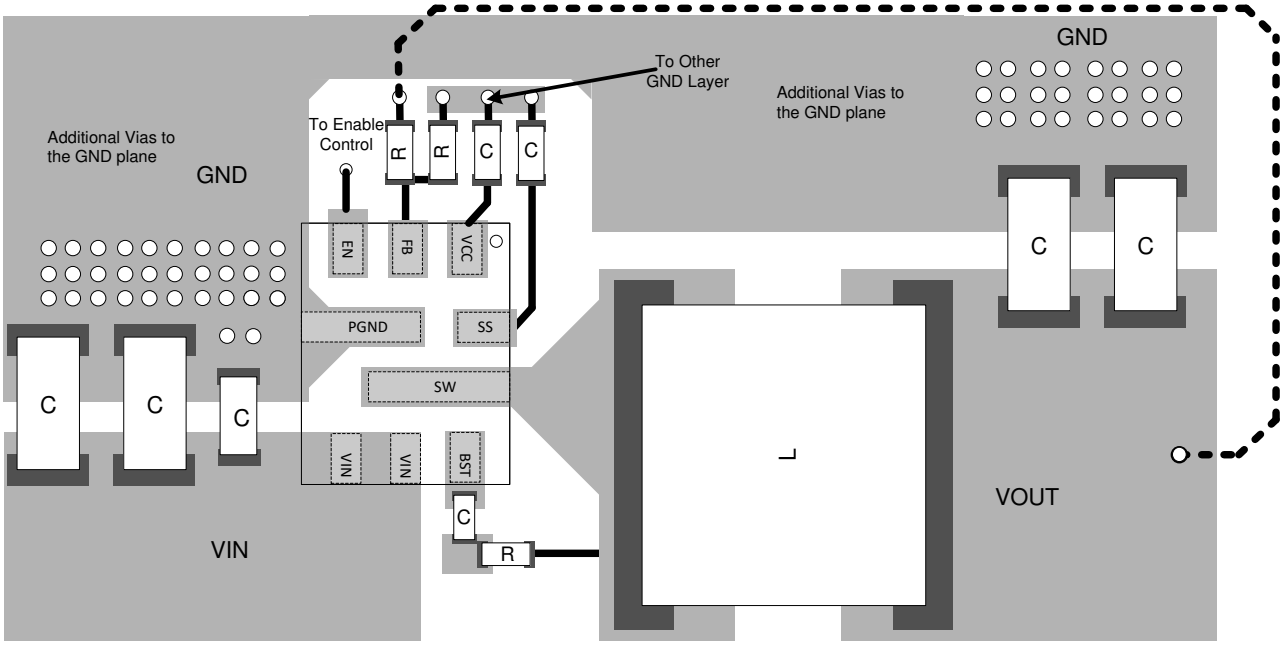


図 7-26. Top-Layer Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS56623x device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Estimate IC thermal and efficiency performance
- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (January 2021) to Revision B (December 2023) **Page**

- 「特長」セクションに利用可能な中国語のデータシートの箇条書き項目を追加、商標情報を更新、最初のページの画像からランダムな色を削除 1
- Updated the *ESD Ratings* table to show CDM testing was per JS-002..... 4
- Added *Custom Design with WEBENCH® Tools* section..... 15
- Added text in *Output Capacitor Selection* to state that the Table 7-2 values are effective values based on DC-bias..... 16
- Added *Custom Design with WEBENCH® Tools* section..... 24

Changes from Revision * (May 2020) to Revision A (January 2021) **Page**

- デバイスのステータスを「事前情報」から「量産データ」に変更..... 1
- 文書全体にわたって表、図、相互参照の採番方法を更新..... 1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS566231PRQFR	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1ID
TPS566231PRQFR.A	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1ID
TPS566231PRQFRG4	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ID
TPS566231PRQFRG4.A	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1ID
TPS566231RQFR	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1H4
TPS566231RQFR.A	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1H4
TPS566231RQFRG4	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H4
TPS566231RQFRG4.A	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H4
TPS566238PRQFR	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1IE
TPS566238PRQFR.A	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1IE
TPS566238RQFR	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1H5
TPS566238RQFR.A	Active	Production	VQFN-HR (RQF) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1H5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

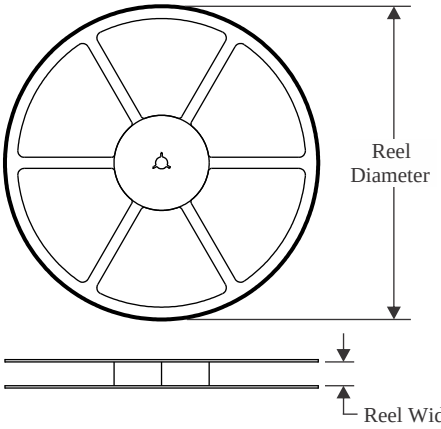
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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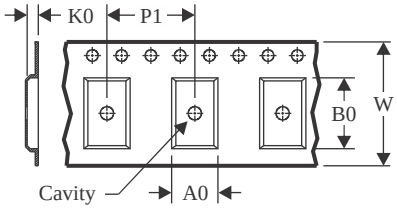
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

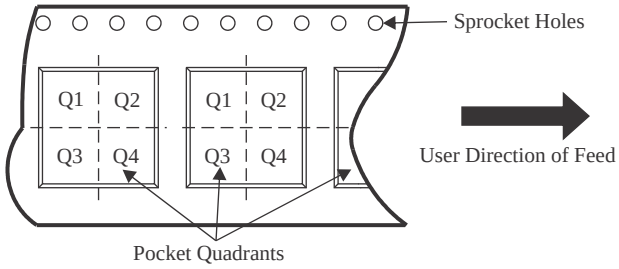


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

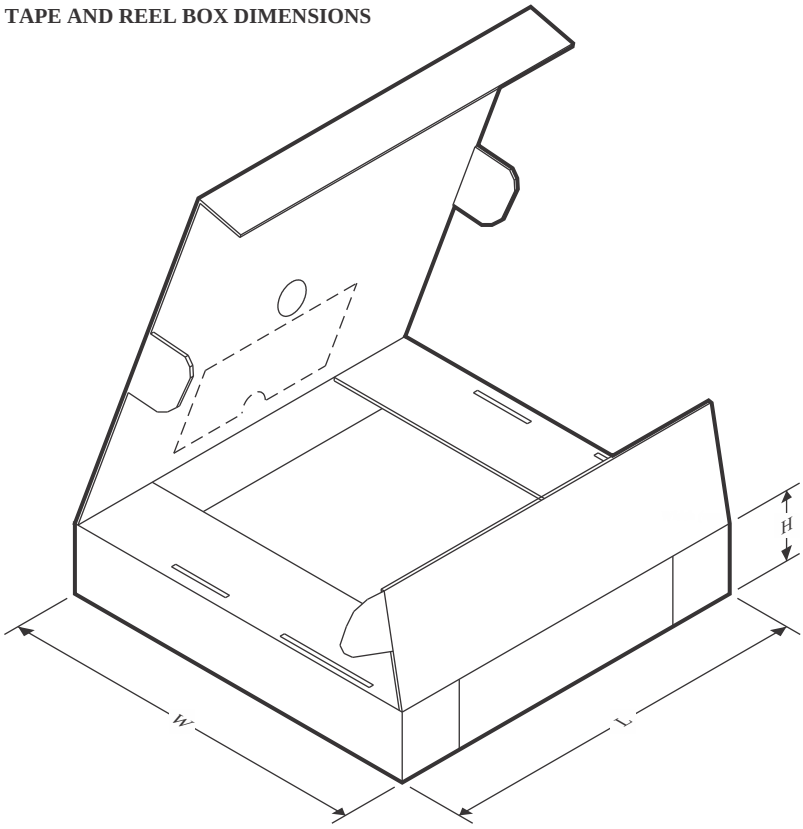
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS566231PRQFR	VQFN-HR	RQF	9	3000	180.0	8.4	1.75	2.25	1.0	4.0	8.0	Q2
TPS566231PRQFRG4	VQFN-HR	RQF	9	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q2
TPS566231RQFR	VQFN-HR	RQF	9	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q2
TPS566231RQFR	VQFN-HR	RQF	9	3000	180.0	8.4	1.75	2.25	1.0	4.0	8.0	Q2
TPS566231RQFRG4	VQFN-HR	RQF	9	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q2
TPS566238PRQFR	VQFN-HR	RQF	9	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q2
TPS566238PRQFR	VQFN-HR	RQF	9	3000	180.0	8.4	1.75	2.25	1.0	4.0	8.0	Q2
TPS566238RQFR	VQFN-HR	RQF	9	3000	180.0	8.4	1.75	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

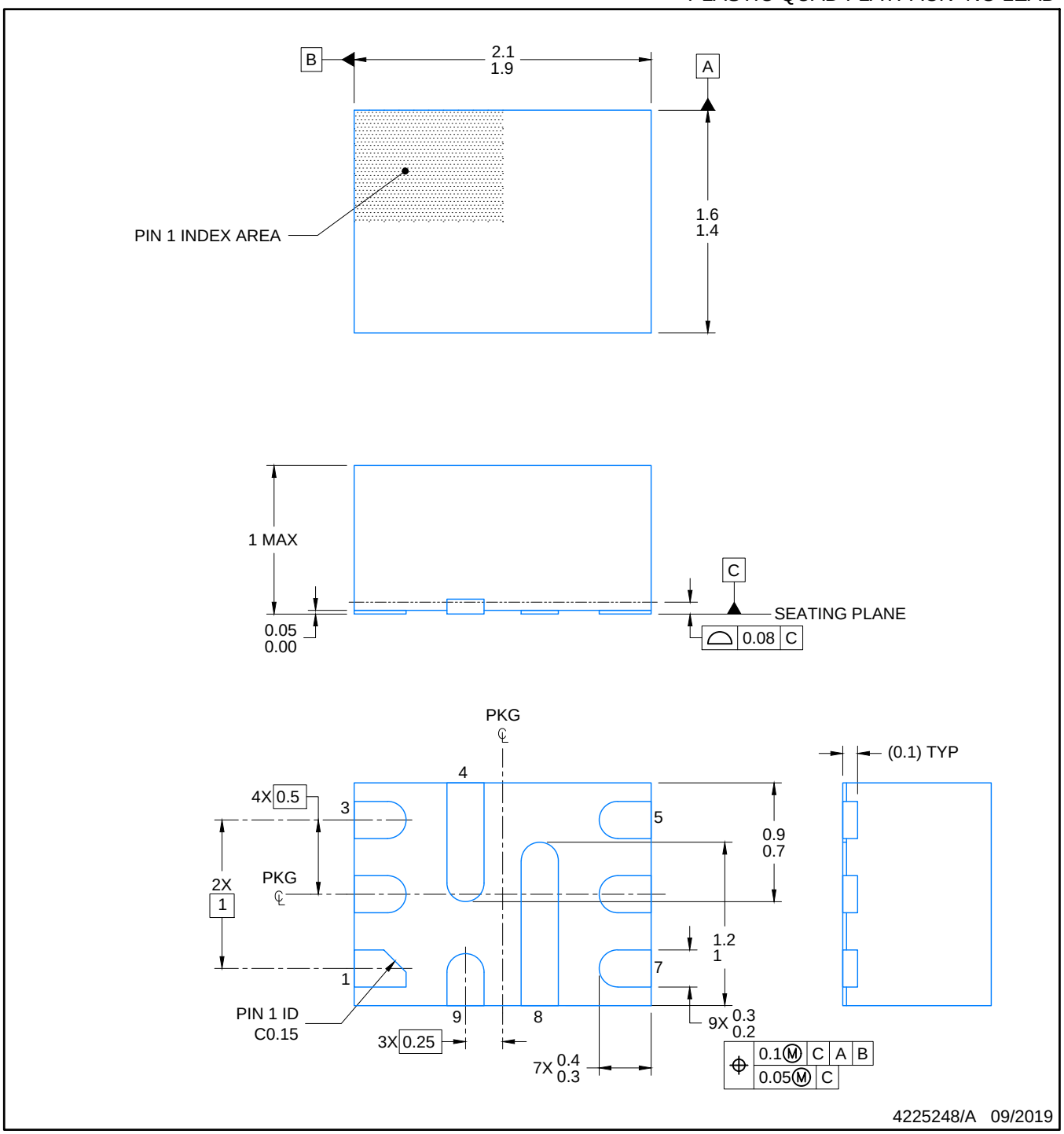
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS566231PRQFR	VQFN-HR	RQF	9	3000	210.0	185.0	35.0
TPS566231PRQFRG4	VQFN-HR	RQF	9	3000	210.0	185.0	35.0
TPS566231RQFR	VQFN-HR	RQF	9	3000	341.0	185.0	80.0
TPS566231RQFR	VQFN-HR	RQF	9	3000	210.0	185.0	35.0
TPS566231RQFRG4	VQFN-HR	RQF	9	3000	210.0	185.0	35.0
TPS566238PRQFR	VQFN-HR	RQF	9	3000	341.0	185.0	80.0
TPS566238PRQFR	VQFN-HR	RQF	9	3000	210.0	185.0	35.0
TPS566238RQFR	VQFN-HR	RQF	9	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RQF0009A

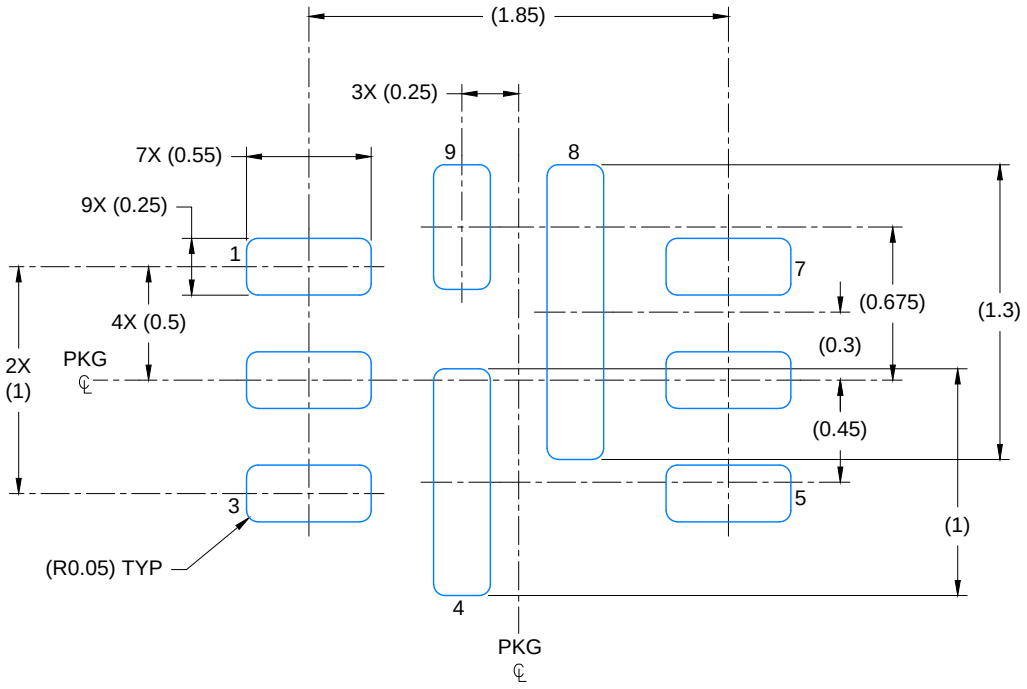
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

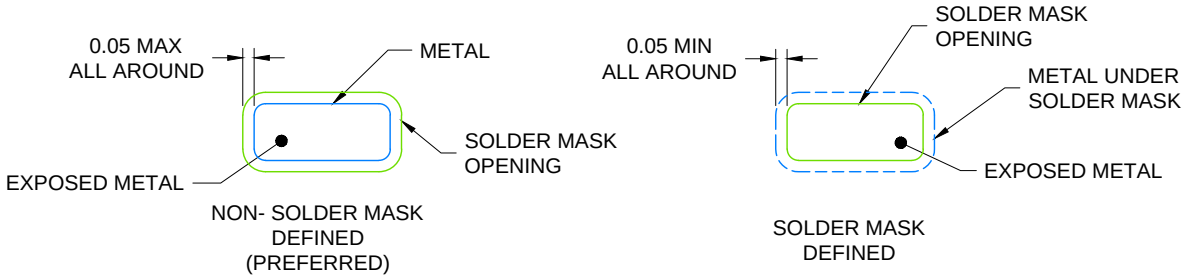


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4225248/A 09/2019

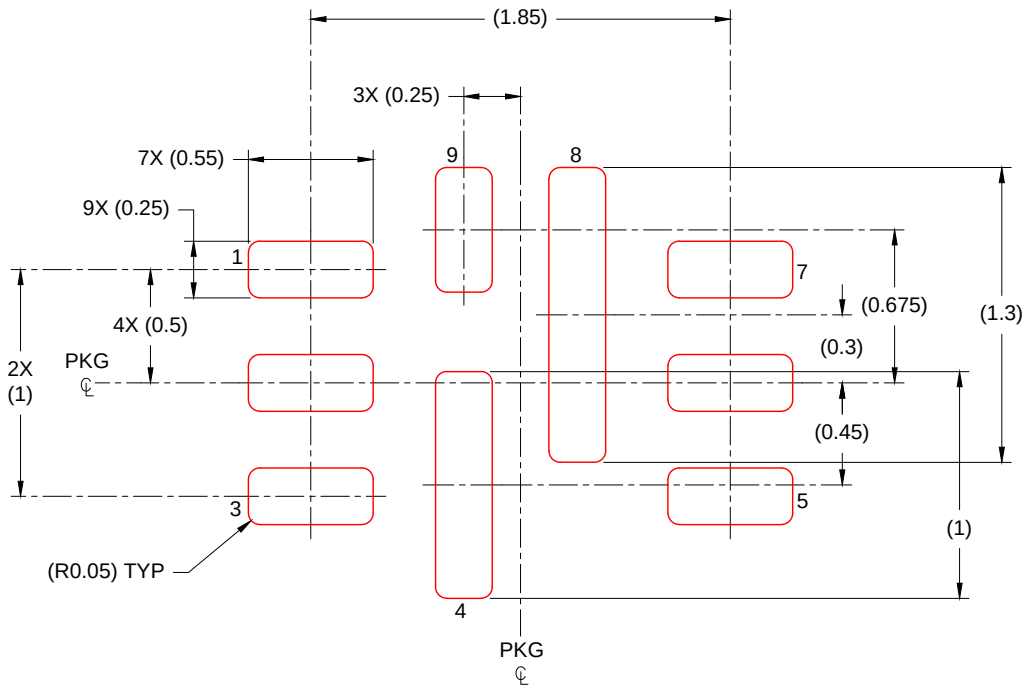
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 30X

4225248/A 09/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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