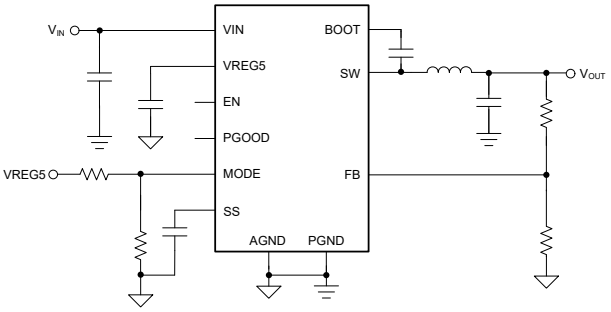
TEXAS INSTRUMENTS
TPS568231
JAJSOG6 – OCTOBER 2022

TPS568231 3.8V～17V 入力、8A、同期整流降圧コンバータ

1 特長

- 入力範囲:4.5V～17V、外部バイアスなし
- 入力範囲:3.8V～17V、外部バイアスなし
- 8A の連続出力電流をサポート
- 7.8mΩ および 3.2mΩ の MOSFET を内蔵
- -40℃～125℃の接合部温度範囲全体にわたって 0.6V ±1% の基準電圧
- 0.6V～5.5V の出力電圧範囲
- 低い静止電流:146μA
- D-CAP3™ 制御モードによる高速過渡応答
- セラミック出力コンデンサに対応
- f_{SW} として 400kHz、800kHz、1.2MHz を選択可能
- 厳しい出力電圧リップルに対応する FCCM (強制連続導通モード) を選択可能
- 軽負荷時に高い効率を実現する Eco-mode™ (自動スキップ・モード) を選択可能
- 外部の 5V バイアスのサポートによる効率向上 (オプション)
- プリバイアス付きスタートアップ機能
- 設定可能なソフトスタート、デフォルトのソフトスタート時間は 1.2ms
- パワー・グッド・インジケータにより出力電圧を監視
- 2 つの調整可能な電流制限設定、ヒカップ再起動機能付き
- ラッチなしの UV、OV、OT、UVLO 保護
- 8A の TPS568215、12A の TPS56C231、TPS56C215 とピン互換
- 動作時接合部温度:-40℃～125℃
- 3.5mm × 3.5mm の 18 ピン HotRod™ QFN パッケージ



概略回路図

2 アプリケーション

- データ・センターおよびエンタープライズ・コンピューティング POL
- ワイヤレス・インフラ
- IPC、ファクトリ・オートメーション、PLC、テスト測定
- ハイエンド DTV

3 概要

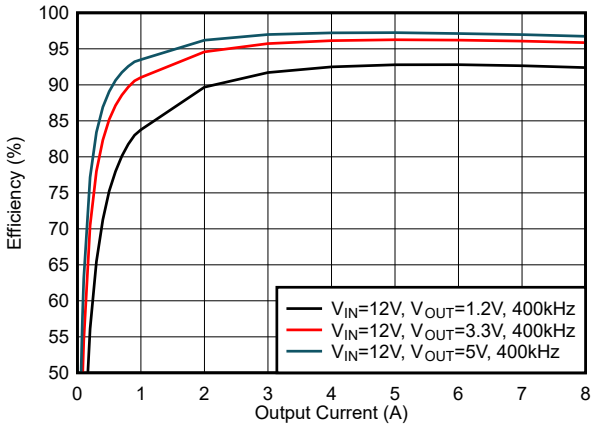
TPS568231 は、適応型オン時間 D-CAP3 制御モードを備えた小型で高効率の同期整流降圧コンバータです。外部補償が不要のため、本デバイスは使いやすく、外付け部品をほとんど必要としません。本デバイスは、スペースに制約のあるデータ・センター・アプリケーションに適しています。

TPS568231 には、非常に正確な基準電圧、高速な負荷過渡応答、外部補償不要、調整可能な電流制限、MODE ピンの設定により軽負荷時に選択できる Eco-mode および FCCM 動作モードなど、競争力のある機能があります。Eco-mode を選択すると、軽負荷時に高い効率を実現できます。厳しい出力電圧リップル要件に対応するには、FCCM を選択できます。TPS568231 は、-40℃～125℃の接合部温度で動作します。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS568231	RNN (VQFN-HR、18)	3.50mm × 3.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率、FCCM モード

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2022	*	Initial release

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5 Pin Configuration and Functions

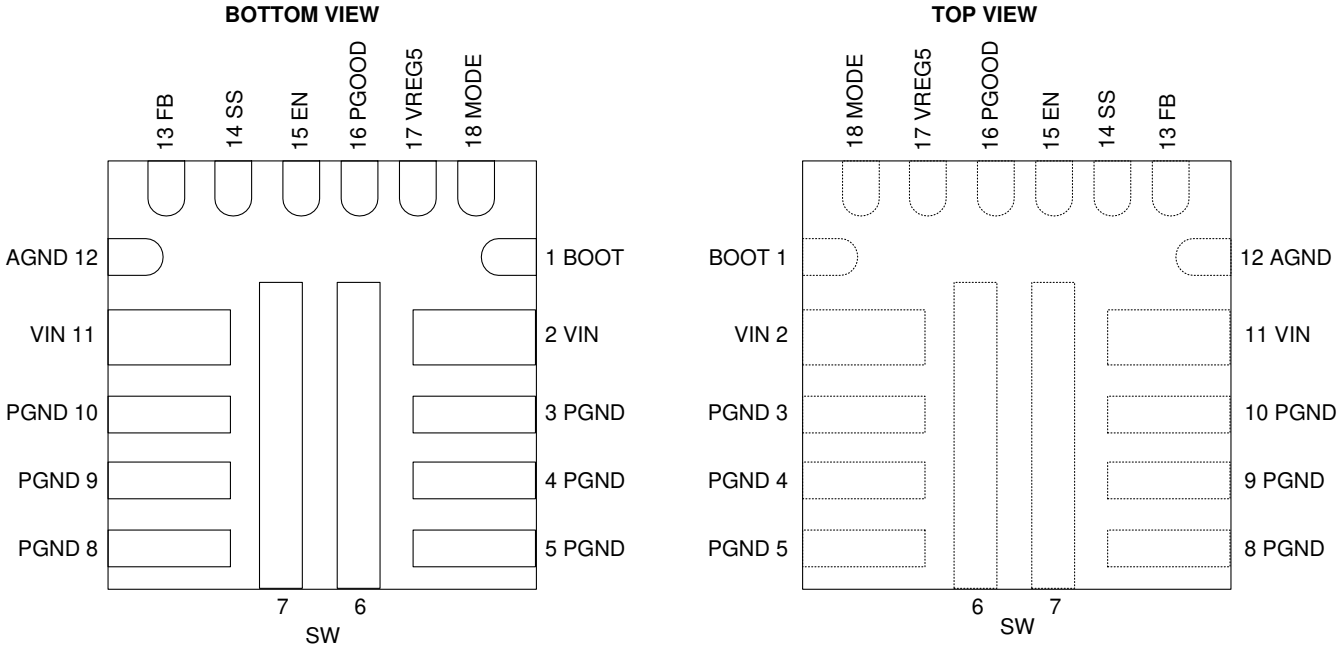


図 5-1. 18-Pin VQFN RNN Package (Bottom View Left, Top View Right)

表 5-1. Pin Functions

Pin		Type	Description
Name	NO.		
BOOT	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BOOT and SW.
VIN	2,11	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
PGND	3, 4, 5, 8, 9, 10	G	Power GND pin for the controller circuit and the internal circuitry. Connect to AGND with a short trace.
SW	6, 7	O	Switch node pin. Connect the output inductor to this pin.
AGND	12	G	Ground of internal analog circuitry. Connect AGND to the PGND plane with a short trace.
FB	13	I	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and AGND.
SS	14	O	Soft-start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the converter starts up in 1.2 ms.
EN	15	I	Enable input control, leaving this pin floating enables the converter. This pin can also be used to adjust the input UVLO by connecting to the center tap of the resistor divider between VIN and EN.
PGOOD	16	O	Open-drain power-good indicator. The pin is asserted low if output voltage is out of the PGOOD threshold, overvoltage, or if the device is under thermal shutdown, EN shutdown, or during soft start.
VREG5	17	I/O	4.7-V internal LDO output that can also be driven externally with a 5-V input. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 4.7-µF capacitor.
MODE	18	I	Switching frequency, current limit selection, and light load operation mode selection pin. Connect this pin to a resistor divider from VREG5 and AGND for different MODE options shown in 表 7-2.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	V_{IN}	–0.3	20	V
	SW	–2	19	
	SW (10-ns transient)	–5	25	
	V_{IN}-SW		22	
	V_{IN}-SW (10-ns transient)		25	
	EN	–0.3	6.5	
	BOOT-SW	–0.3	6.5	
	BOOT-SW (10-ns transient)	–0.3	7.5	
	BOOT	–0.3	25.5	
	SS, MODE, FB	–0.3	6.5	
	VREG5	–0.3	6	
	PGOOD	–0.3	6.5	
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the*Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Pin voltage	V_{IN}	3.8		17	V
	SW	–1.8		17	V
	BOOT	–0.1		23.5	V
	VREG5, MODE, FB, PGOOD, EN	–0.1		5.5	V
Output current	I_{LOAD}	0		8	A
Operating junction temperature	T_J	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		RNN (JEDEC)	RNN (TI EVM)	UNIT
		18 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.9	27	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	Not applicable[2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	Not applicable[2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11	10	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(2) Not applicable to an EVM layout

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN}=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	V_{IN} supply current	T_J = 25°C, V_{EN} = 5 V, non-switching		146		µA
I_{VINSDN}	V_{IN} shutdown current	V_{EN} = 0 V		9.3		µA
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.175	1.225	1.3	V
V_{ENL}	EN L-level threshold voltage		1.025	1.104	1.15	V
V_{ENHYS}				0.121		V
I_{ENp1}	EN pullup current	V_{EN} = 1.0 V	0.35	1.91	2.95	µA
I_{ENp2}		V_{EN} = 1.3 V	3	4.197	5.5	µA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	598	600	602	mV
		T_J = 0°C to 85°C	597.5	600	602.5	mV
		T_J = –40°C to 85°C	594	600	602.5	mV
		T_J = –40°C to 125°C	594	600	606	mV
LDO VOLTAGE						
VREG5	LDO output voltage	T_J = –40°C to 125°C	4.58	4.7	4.83	V
ILIM5	LDO output current limit	T_J = –40°C to 125°C	100	150	200	mA
UVLO						
UVLO	UVLO threshold	VREG5 rising voltage		4.25		V
		VREG5 falling voltage		3.52		V
		VREG5 hysteresis		730		mV
UVLO, VREG5 = 4.7 V	UVLO threshold, VREG5 = 4.7 V	VIN rising voltage, VREG5 = 4.7 V		3.32		V
		VIN falling voltage, VREG5 = 4.7 V		3.24		V
		VIN hysteresis, VREG5 = 4.7 V		80		mV
MOSFET						
$R_{DS(on)H}$	High-side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		7.8		mΩ
$R_{DS(on)L}$	Low-side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		3.2		mΩ
ON-TIME TIMER CONTROL						
$t_{ON\ min}$	SW minimum on time	VIN = 17 V, V_{OUT} = 0.6 V, f_{SW} = 1200 kHz		60		ns
t_{OFF}	SW minimum off time	V_{FB} = 0.5 V			310	ns
SOFT START AND OUTPUT DISCHARGE						

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6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, V_{IN}=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	Soft-start time	Internal soft start time, T_J = –40°C to 125°C		1.2		ms
I_{ss}	Soft-start charge current	T_J = –40°C to 125°C	4.9	6	7.1	µA
R_{DIS}	Discharge resistance	T_J = 25°C, V_{OUT} = 0.5 V, V_{EN} = 0 V		370		Ω
CURRENT LIMIT						
I_{OCL}	Current limit (low-side sourcing)	ILIM-1 option, valley current	6	7.1	8.15	A
		ILIM option, valley current	8	9.4	10.8	A
I_{NOCL}	Current limit (low-side negative)	Valley current		3.9		A
POWER GOOD						
$V_{PGOODTH}$	PGOOD threshold	V_{FB} falling (fault)		84%		
		V_{FB} rising (good)		93%		
		V_{FB} rising (fault)		116%		
		V_{FB} falling (good)		108%		
$t_{PGOODLY}$	PGOOD delay time	Delay from low to high		128		µs
		Delay form high to low		14		µs
I_{PGOOD}	PGOOD sink current	I_{OL} = 4 mA			0.4	V
I_{PGLK}	PGOOD leak current	V_{PGOOD} = 5.5 V			1	V
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect		121%		
T_{OVPDEL}	Output OVP response delay			52		µs
V_{UVP}	Output UVP threshold	Hiccup detect		70%		
t_{UVPDGL}	UVP prop deglitch			1		ms
t_{UVPDEL}	Output hiccup delay relative to SS time	UVP detect		1		cycle
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect		7		cycle
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		160		°C
		Hysteresis		15		°C

(1) Not production tested

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6.6 Typical Characteristics

V_{IN} = 12 V. T_J = –40°C to 125°C（unless otherwise specified).

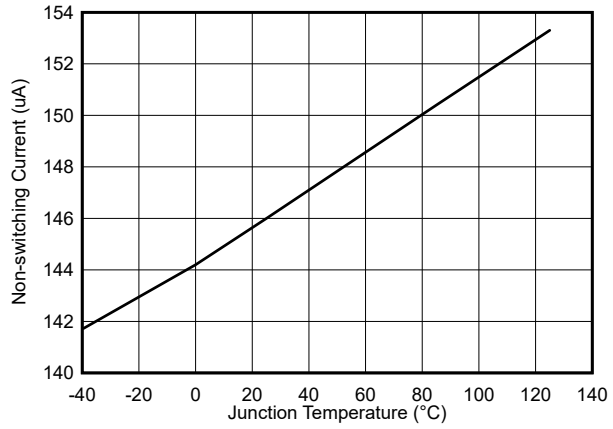


図 6-1. Quiescent Current vs Temperature

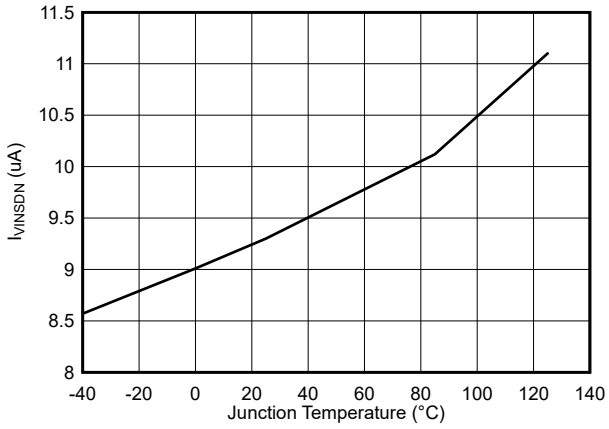


図 6-2. Shutdown Current vs Temperature

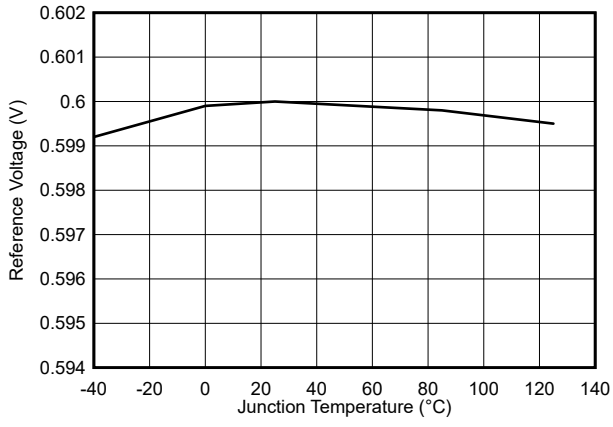


図 6-3. Reference Voltage vs Temperature

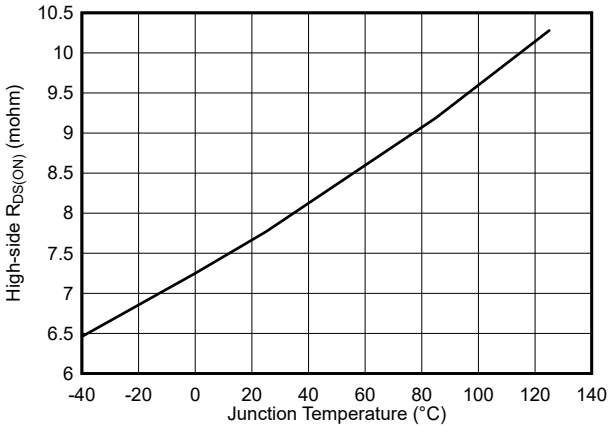


図 6-4. High-Side $R_{DS(on)}$ vs Temperature

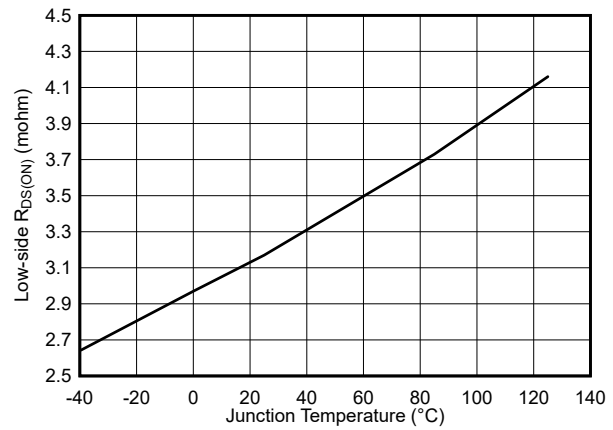


図 6-5. Low-Side $R_{DS(on)}$ vs Temperature

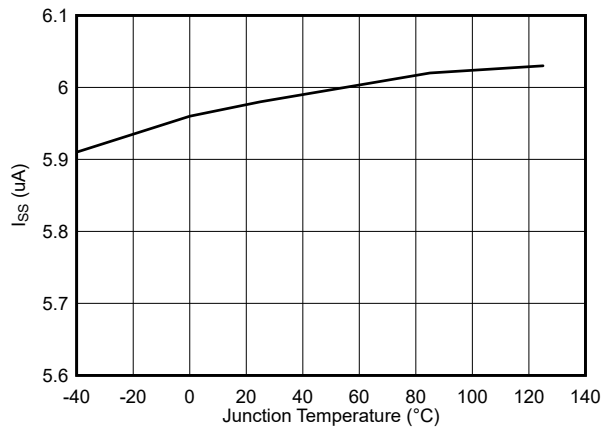


図 6-6. Soft-Start Charge Current vs Temperature

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6.6 Typical Characteristics (continued)

V_{IN} = 12 V. T_J = –40°C to 125°C（unless otherwise specified).

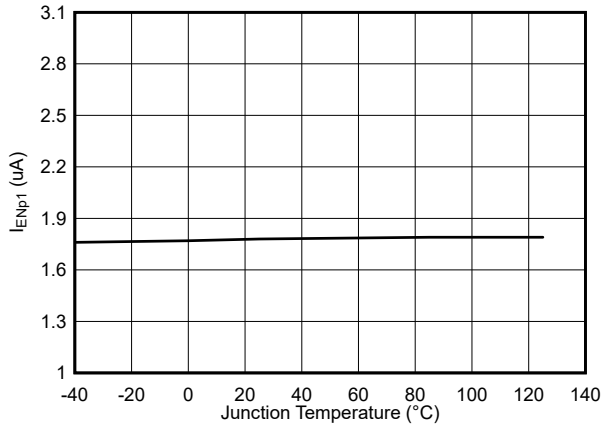


図 6-7. Enable Pullup Current, V_{EN} = 1 V

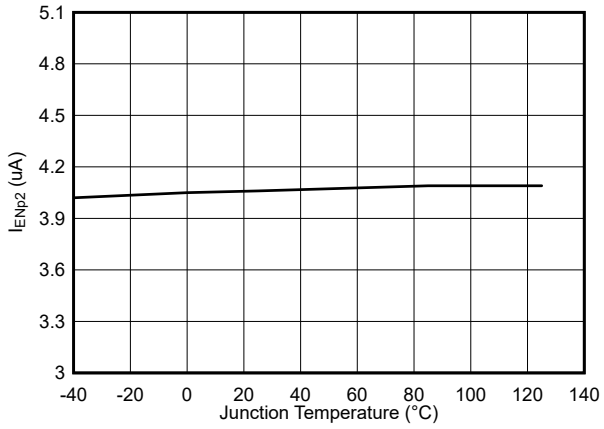


図 6-8. Enable Pullup Current, V_{EN} = 1.3 V

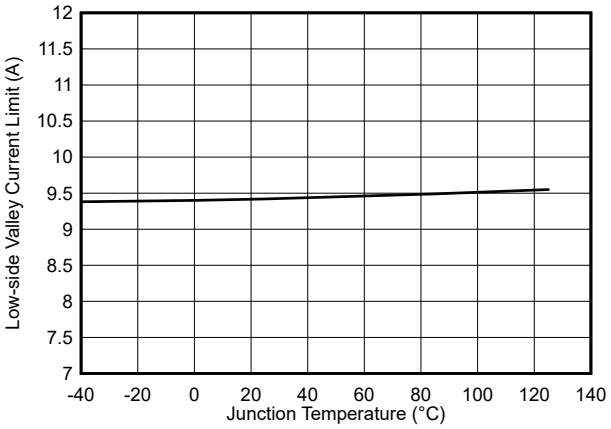


図 6-9. TPS568231 Current Limit (ILIM) vs Temperature

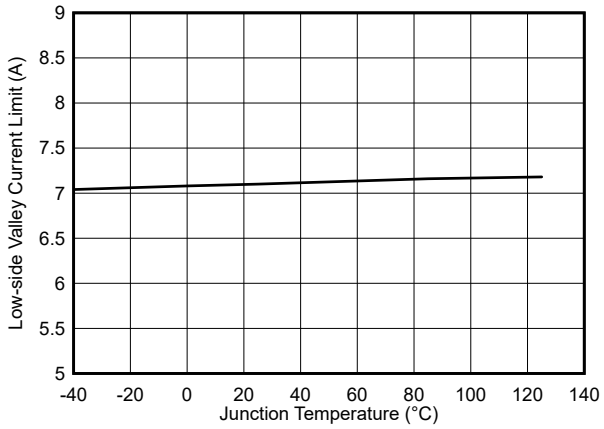


図 6-10. TPS568231 Current Limit(ILIM-1) vs Temperature

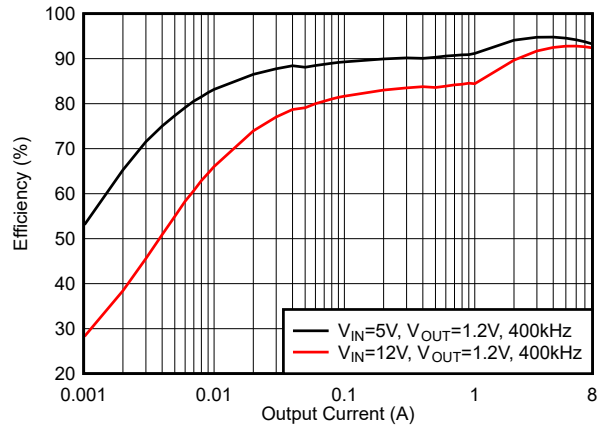


図 6-11. Efficiency, Mode = DCM, f_{SW} = 400 kHz

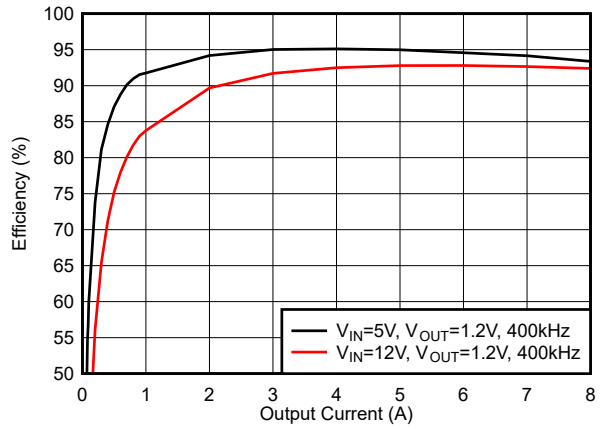


図 6-12. Efficiency, Mode = FCCM, f_{SW} = 400 kHz

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6.6 Typical Characteristics (continued)

V_{IN} = 12 V. T_J = –40°C to 125°C（unless otherwise specified).

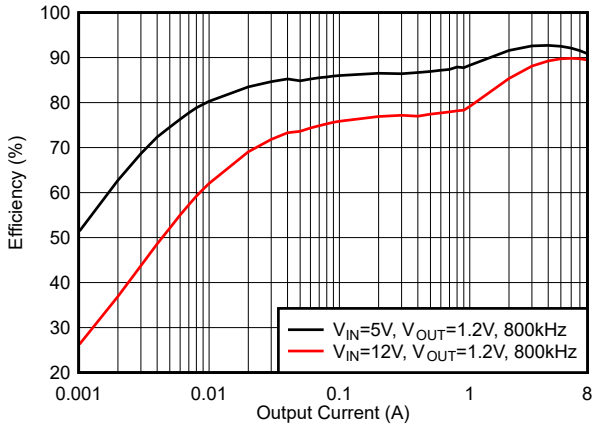


図 6-13. Efficiency, Mode = DCM, f_{SW} = 800 kHz

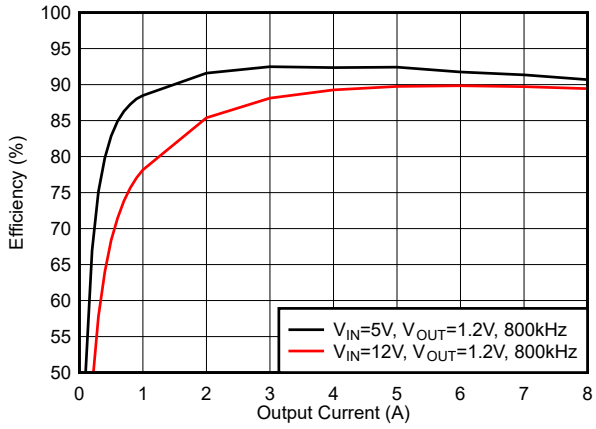


図 6-14. Efficiency, Mode = FCCM, f_{SW} = 800 kHz

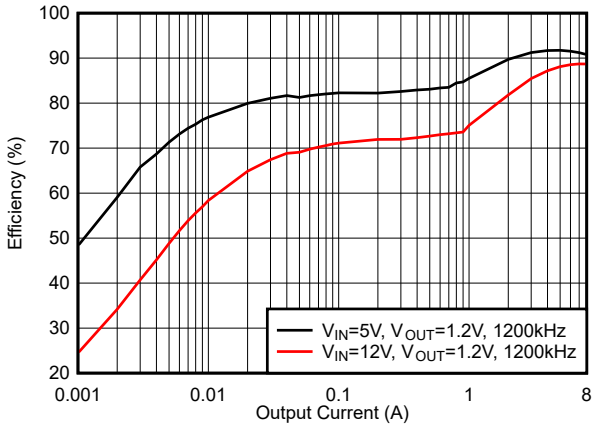


図 6-15. Efficiency, Mode = DCM, f_{SW} = 1200 kHz

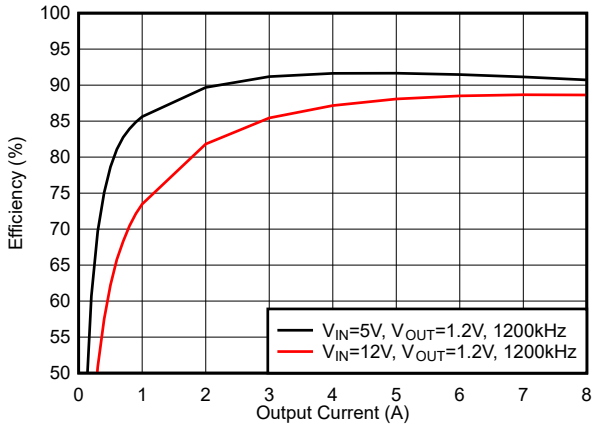


図 6-16. Efficiency, Mode = FCCM, f_{SW} = 1200 kHz

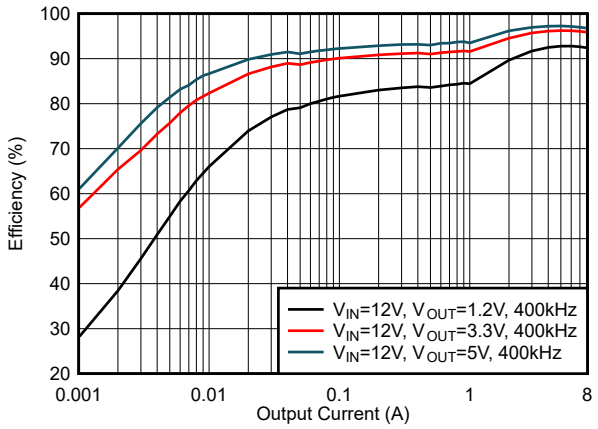


図 6-17. Efficiency, Mode = DCM, f_{SW} = 400 kHz

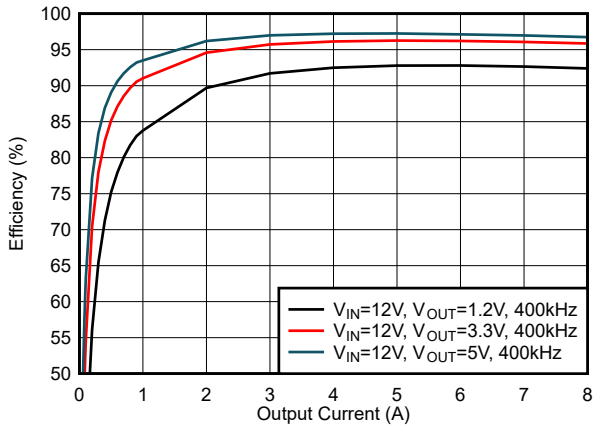


図 6-18. Efficiency, Mode = FCCM, f_{SW} = 400 kHz

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6.6 Typical Characteristics (continued)

V_{IN} = 12 V. T_J = –40°C to 125°C（unless otherwise specified).

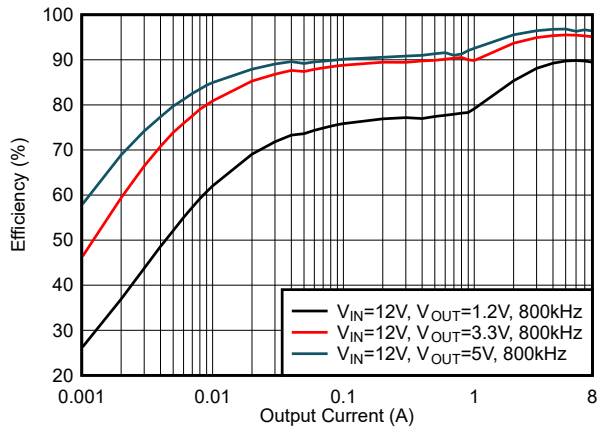


図 6-19. Efficiency, Mode = DCM, f_{SW} = 800 kHz

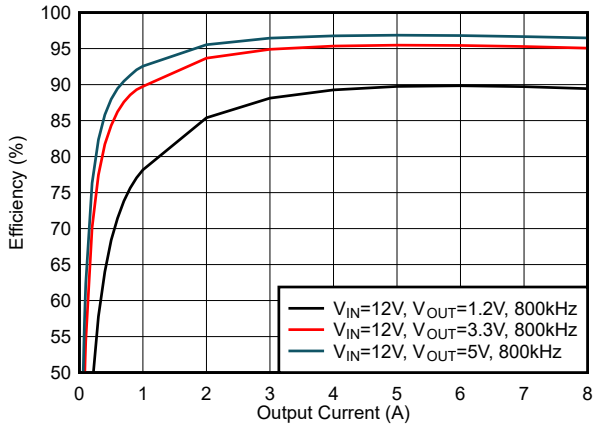


図 6-20. Efficiency, Mode = FCCM, f_{SW} = 800 kHz

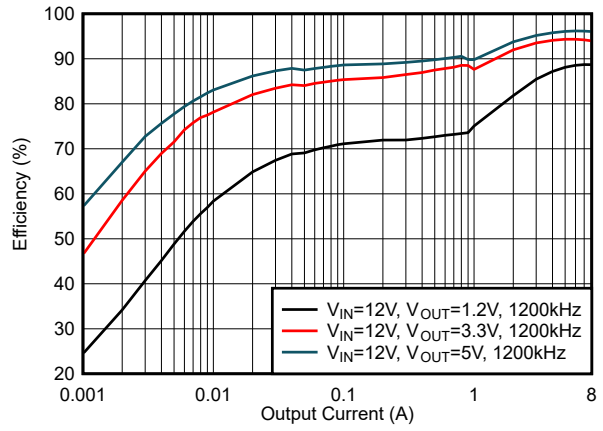


図 6-21. Efficiency, Mode = DCM, f_{SW} = 1200 kHz

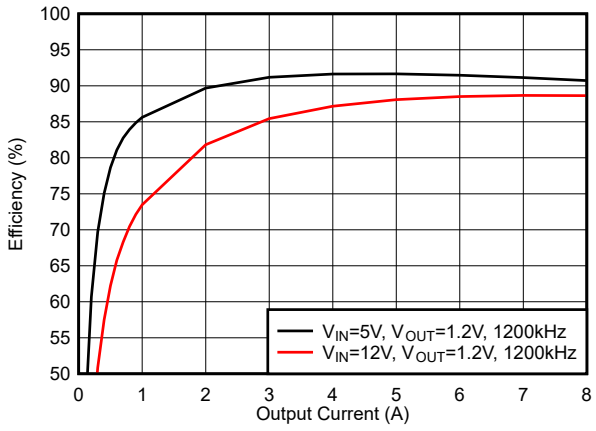


図 6-22. Efficiency, Mode = FCCM, f_{SW} = 1200 kHz

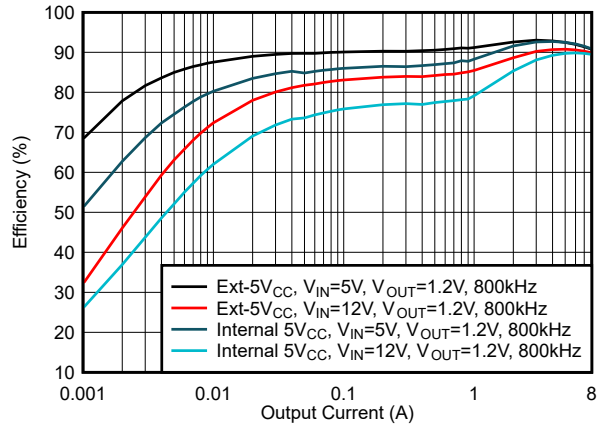


図 6-23. Efficiency, Ext-VCC vs Internal-VCC, Mode = DCM, f_{SW} = 800 kHz

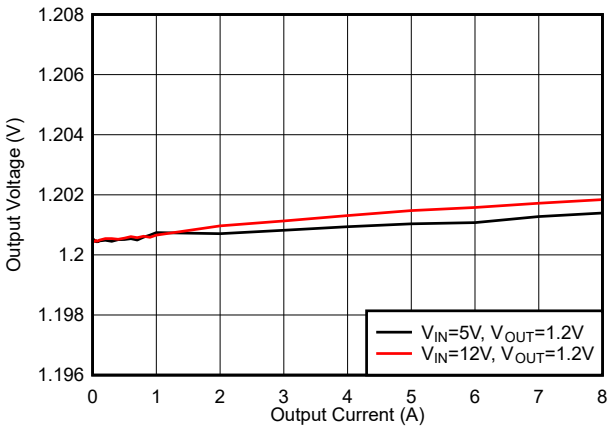


図 6-24. Load Regulation, f_{SW} = 800 kHz

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6.6 Typical Characteristics (continued)

V_{IN} = 12 V. T_J = –40°C to 125°C（unless otherwise specified).

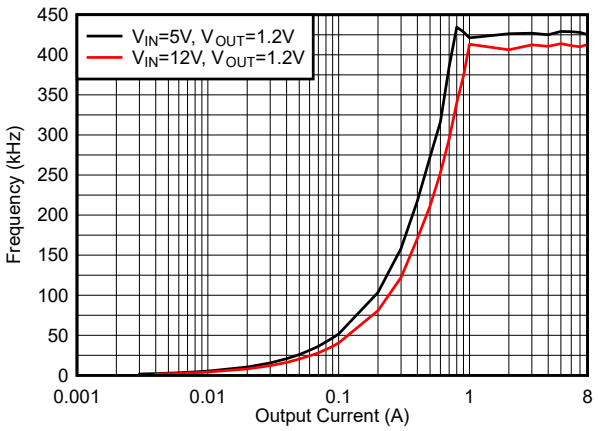


図 6-25. f_{SW} Load Regulation, Mode = DCM, f_{SW} = 400 kHz

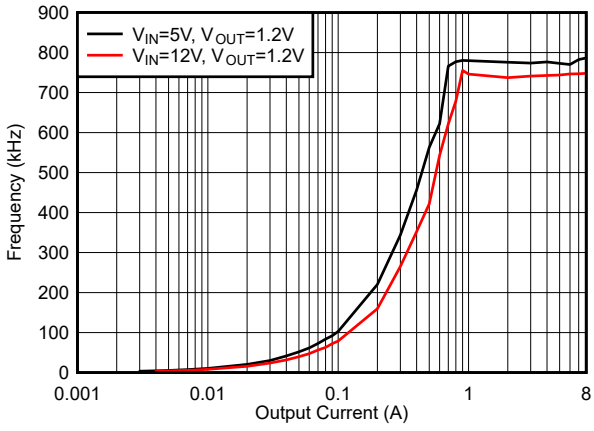


図 6-26. f_{SW} Load Regulation, Mode = DCM, f_{SW} = 800 kHz

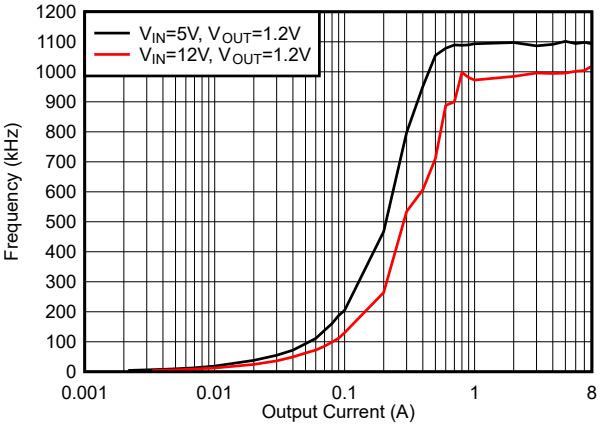


図 6-27. f_{SW} Load Regulation, Mode = DCM, f_{SW} = 1200 kHz

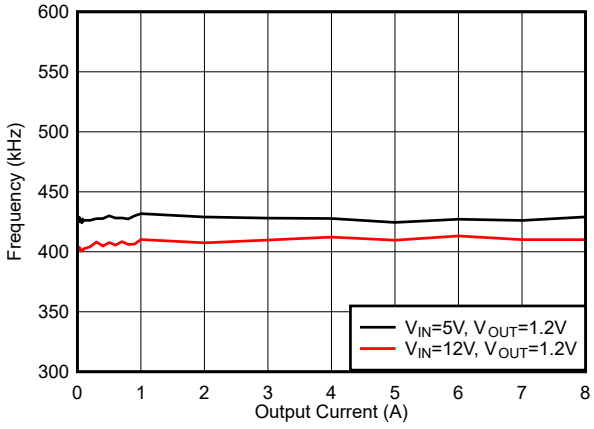


図 6-28. f_{SW} Load Regulation, Mode = FCCM, f_{SW} = 400 kHz

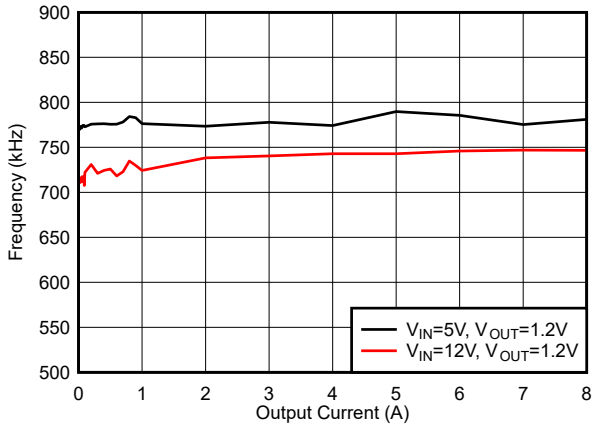


図 6-29. f_{SW} Load Regulation, Mode = FCCM, f_{SW} = 800 kHz

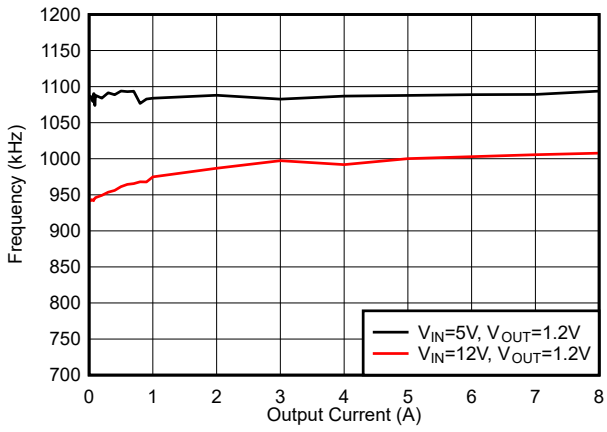


図 6-30. f_{SW} Load Regulation, Mode = FCCM, f_{SW} = 1200 kHz

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6.6 Typical Characteristics (continued)

V_{IN} = 12 V. T_J = –40°C to 125°C（unless otherwise specified).

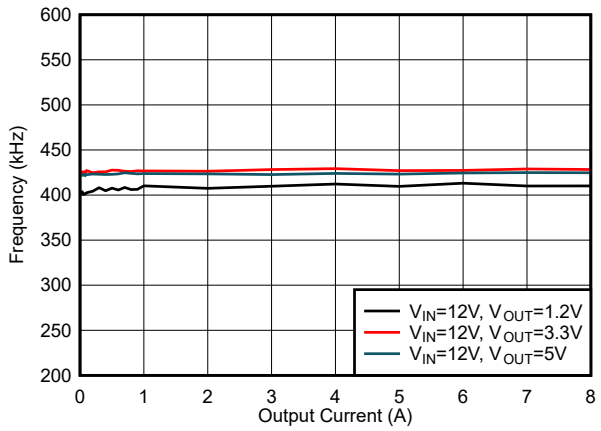


図 6-31. f_{SW} Load Regulation, Mode = FCCM, f_{SW} = 400 kHz

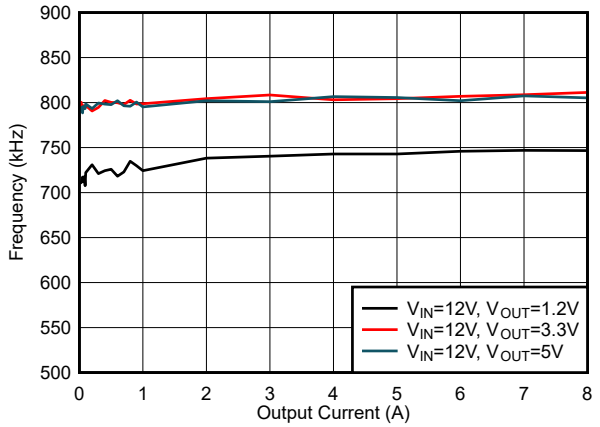


図 6-32. f_{SW} Load Regulation, Mode = FCCM, f_{SW} = 800 kHz

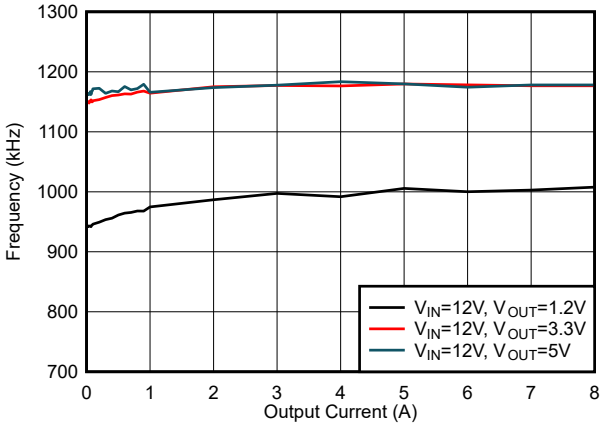


図 6-33. f_{SW} Load Regulation, Mode = FCCM, f_{SW} = 1200 kHz

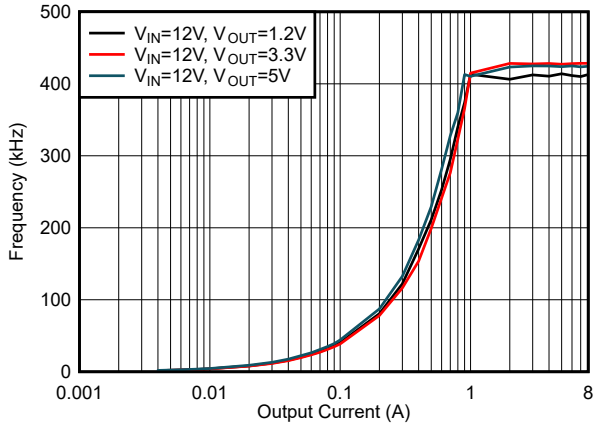


図 6-34. f_{SW} Load Regulation, Mode = DCM, f_{SW} = 400 kHz

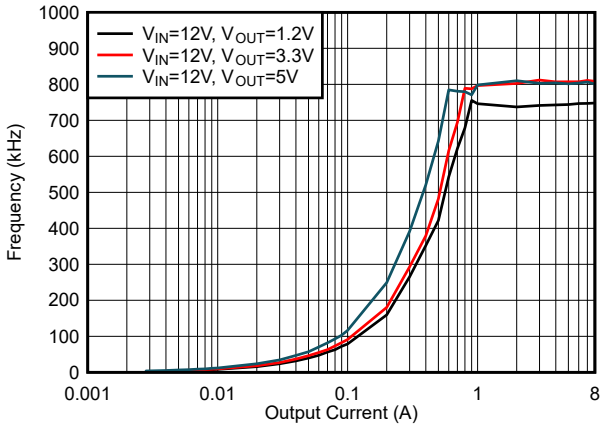


図 6-35. f_{SW} Load Regulation, Mode = DCM, f_{SW} = 800 kHz

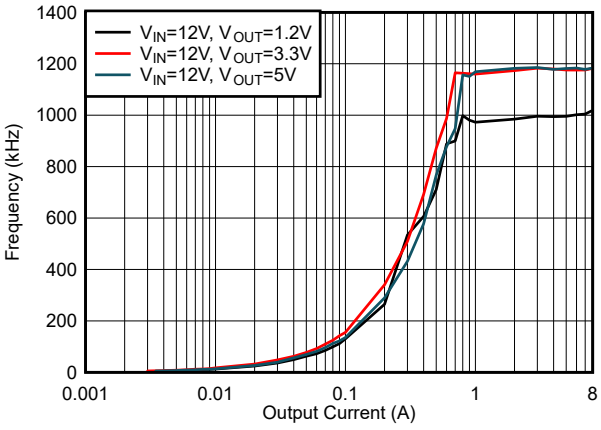


図 6-36. f_{SW} Load Regulation, Mode = DCM, f_{SW} = 1200 kHz

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7 Detailed Description

7.1 Overview

The TPS568231 is a high-density, synchronous step-down buck converter that can operate from 3.8-V to 17-V input voltage (V_{IN}). The device has 7.8-mΩ and 3.2-mΩ integrated MOSFETs that enable high efficiency up to 8 A. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides a seamless transition between FCCM operating mode at higher load condition and Eco-mode operation at lighter load condition. Eco-mode allows the TPS568231 to maintain high efficiency at light load. The TPS568231 can adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

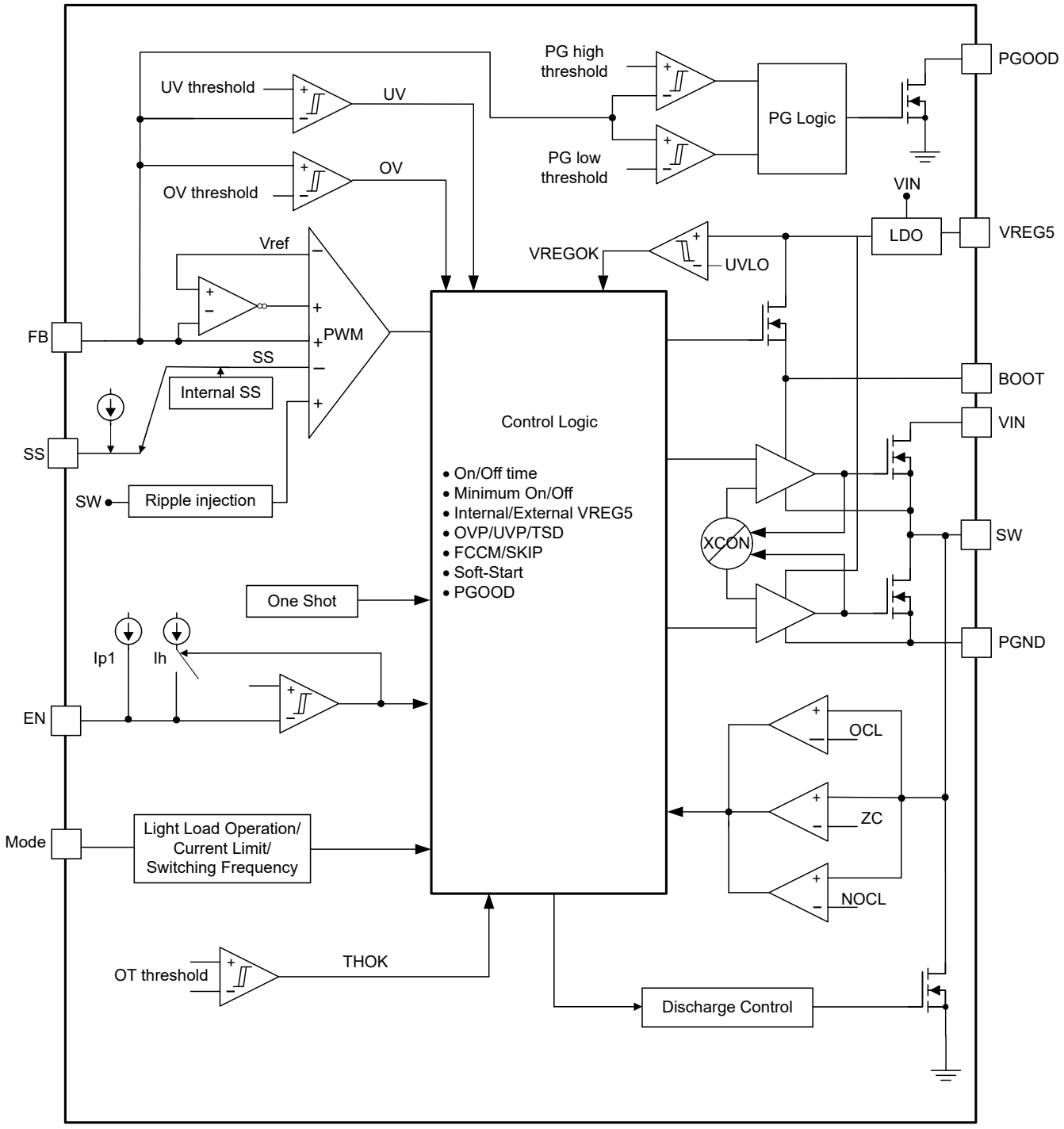
The TPS568231 has three selectable switching frequencies (f_{SW}): 400 kHz, 800 kHz, and 1200 kHz. These frequencies give the flexibility to optimize the design for higher efficiency or smaller size. There are two selectable current limits. All these options are configured by choosing the right voltage on the MODE pin.

The TPS568231 has a 4.7-V internal LDO that creates bias for all internal circuitry. There is a feature to overdrive this internal LDO with an external voltage on the VREG5 pin which improves the efficiency of the converter. The undervoltage lockout (UVLO) circuit monitors the VREG5 pin voltage to protect the internal circuitry from low input voltages. The device has an internal pullup current source on the EN pin, which can enable the device even with the pin floating.

Soft-start time can be selected by connecting a capacitor to the SS pin. The device is protected from output short, undervoltage, and overtemperature conditions.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control Mode

The TPS568231 operates using the adaptive on-time PWM control with a proprietary D-CAP3 control mode, which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle, the high-side MOSFET is turned on for an on time set by an internal one-shot timer. This on time is set based on the input voltage of the converter, output voltage of the converter, and the pseudo-fixed frequency, hence this type of control topology is called an adaptive on-time control. The one-shot timer resets and turns on again after the feedback voltage (V_{FB}) falls below the internal reference voltage (V_{REF}). An internal ramp is generated, which is fed to the FB pin to simulate the output voltage ripple, enabling the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode topology.

The TPS568231 includes an error amplifier that makes the output voltage very accurate. This error amplifier is absent in other flavors of D-CAP3 control mode. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS568231 is a low-pass L-C circuit. This L-C filter has double pole that is described in 式 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS568231. The low frequency L-C double pole has a 180 degree in-phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is changed according to the switching frequency selected as shown in 表 7-1. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system is usually targeted to be less than one-fifth of the switching frequency (f_{SW}).

表 7-1. Ripple Injection Zero

Switching Frequency (kHz)	Zero Location (kHz)
400	17.8
800	27.1
1200	29.8

7.3.2 Eco-mode™ Control

The TPS568231 is designed with Eco-mode control to increase efficiency at light loads. This option can be chosen using the MODE pin as shown in 表 7-2. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept approximately the same as it is in continuous conduction mode. The off time increases as it takes more time to discharge the output with a smaller load current. Use 式 2 to calculate the light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

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After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). Size the inductor properly so that the valley current does not hit the negative low-side current limit.

7.3.3 4.7-V LDO

The VREG5 pin is the output of the internal 4.7-V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VREG5 pin must be bypassed with a 4.7-µF capacitor. An external voltage that is above the internal output voltage of the LDO can override the internal LDO, switching it to the external rail after a higher voltage is detected. This action enhances the efficiency of the converter because the quiescent current now runs off this external rail instead of the input power supply. The UVLO circuit monitors the VREG5 pin voltage and disables the output when VREG5 falls below the UVLO threshold. When using an external bias on the VREG5 rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VREG5 rail that can pull a current higher than the internal current limit of the LDO (ILIM5) from the VREG5, then the VREG5 LDO turns off thereby shutting down the output of TPS568231. If such condition does not exist and if the external VREG5 rail is turned off, the VREG5 voltage switches over to the internal LDO voltage, which is 4.7 V typically in a few nanoseconds.

7.3.4 MODE Selection

The TPS568231 has a MODE pin that can offer 12 different states of operation as a combination of current limit, switching frequency, and light load operation. The device can operate at two different current limits, ILIM-1 and ILIM, to support an output continuous current of 8 A, respectively.

The TPS568231 is designed to compare the valley current of the inductor against the current limit thresholds so make sure to understand that the output current is half the ripple current higher than the valley current. Take the ILIM current limit selection as an example. The OCL threshold is 8-A minimum, which means that a pk-pk inductor ripple current of 2-A minimum is needed to draw 9 A out of the converter without entering an overcurrent condition.

The TPS568231 can operate at three different frequencies of 400 kHz, 800 kHz, and 1200 kHz and also can choose between Eco-mode and FCCM mode. In Eco-mode, TPS568231 works in DCM (discontinuous conduction mode) with high efficiency in light loading, In FCCM mode, TPS568231 works in forced PWM (forced continuous conduction mode) with tight output voltage ripple. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed in 表 7-2. The voltage on the MODE pin can be set by connecting this pin to the center tap of a resistor divider connected between VREG5 and AGND. A guideline for the top resistor (R_{M_H}) and the bottom resistor (R_{M_L}) in 1% resistors is shown in 表 7-2. Make sure that the voltage for the MODE pin is derived from the VREG5 rail only because internally this voltage is referenced to detect the MODE option. The MODE pin setting can be reset only by a VIN power cycling.

表 7-2. MODE Pin Resistor Settings

R_{M_L} (kΩ)	R_{M_H} (kΩ)	Light Load Operation	Current Limit	Frequency (kHz)
5.1	300	FCCM	ILIM-1	400
10	200	FCCM	ILIM	400
20	160	FCCM	ILIM-1	800
20	120	FCCM	ILIM	800
51	200	FCCM	ILIM-1	1200
51	180	FCCM	ILIM	1200
51	150	DCM	ILIM-1	400
51	120	DCM	ILIM	400
51	91	DCM	ILIM-1	800
51	82	DCM	ILIM	800
51	62	DCM	ILIM-1	1200
51	51	DCM	ILIM	1200

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図 7-1 shows the typical start-up sequence of the device after the EN pin voltage crosses the EN turn-on threshold. After the voltage on VREG5 pin crosses the rising UVLO threshold, it takes 144 µs to read the first MODE setting and maximum approximately 180 µs from accomplishing MODE to soft start. The output voltage starts ramping after the MODE setting reading is completed.

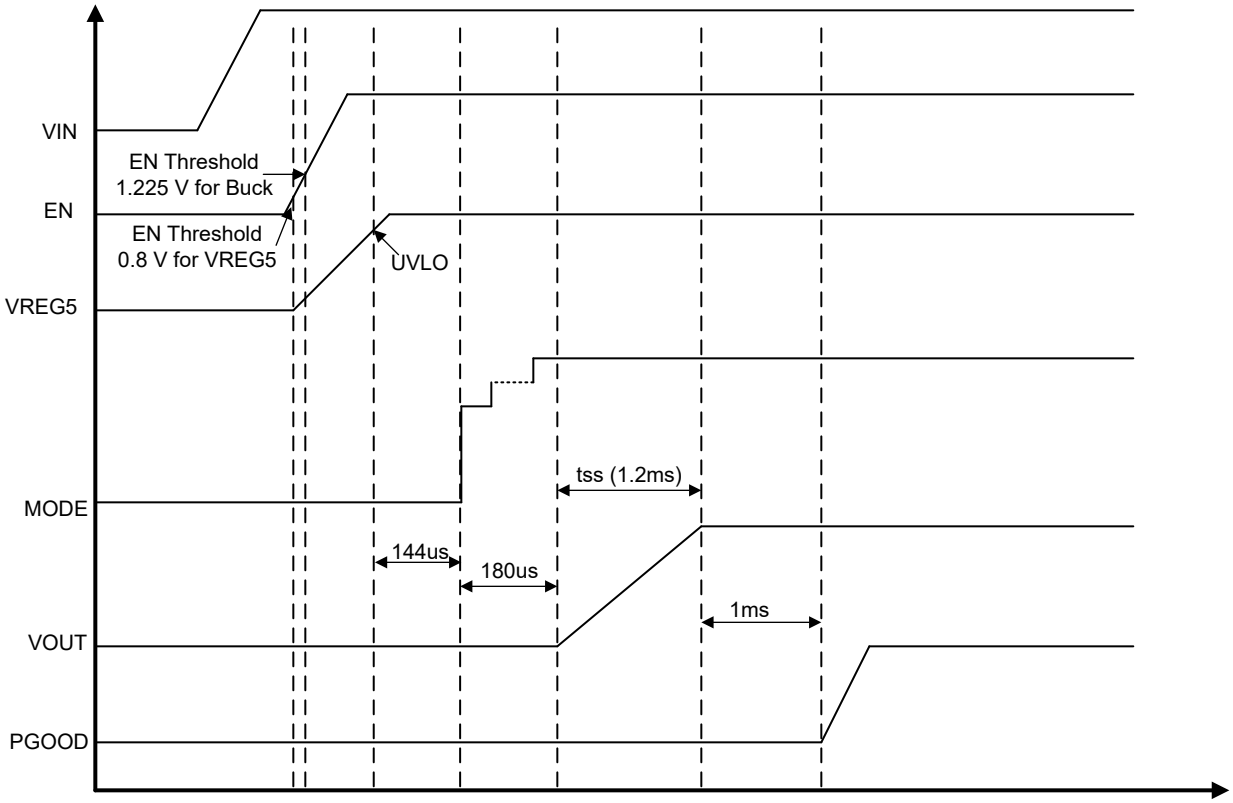


図 7-1. Power-Up Sequence

7.3.5 Soft Start and Prebiased Soft Start

The TPS568231 has an internal 1.2-ms soft-start time and an external adjustable soft-start time that can be set by connecting a capacitor on the SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The device tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. 式 3 is the equation for the soft-start time (t_{SS}):

$$T_{SS(S)} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (3)$$

where

- V_{REF} is 0.6 V and I_{SS} is 6 µA.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.6 Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold, which is approximately 1.2 V, the device starts switching and when the EN pin voltage falls below the turn-off threshold, which is approximately 1.1 V, it stops switching. If the user application requires a different turn-on (V_{START}) and turn-off thresholds (V_{STOP}), respectively, the EN pin can be configured as shown in 図 7-2 by

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connecting a resistor divider between VIN and EN. The EN pin has a pullup current, I_{p1}, that sets the default state of the pin when it is floating. This current increases to I_{p2} when the EN pin voltage crosses the turn-on threshold. Use 式 4 and 式 5 to set the UVLO thresholds.

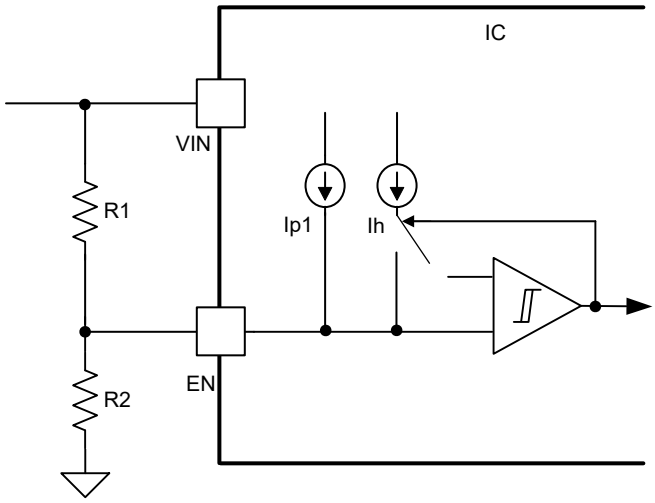


図 7-2. Adjustable V_{IN} Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_{p1}\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\ I_{p2}} \quad (5)$$

where

- I_{p2} is 4.197 µA.
- I_{p1} is 1.91 µA.
- I_h is 2.287 µA.
- $V_{ENRISING}$ is 1.225 V.
- $V_{ENFALLING}$ is 1.104 V.

7.3.7 Power Good

The power-good (PGOOD) pin is an open-drain output. After the FB pin voltage is between 93% and 108% of the internal reference voltage (V_{REF}), PGOOD is de-asserted and floats after a 14-µs de-glitch time. TI recommends a 10-kΩ pullup resistor to pull it up to VREG5. The PGOOD pin is pulled low when the FB pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold, in an event of thermal shutdown, or during the soft-start period.

7.3.8 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the off state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by:

- Input voltage
- Output voltage
- On time

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- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain-to-source voltage of the low-side FET is above the voltage proportional to current limit, the low-side FET stays on until the current level becomes lower than the OCL level, which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 70% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 1 ms, the device restarts after a 7-ms hiccup time. In this type of valley detect control, the load current is higher than the OCL threshold by one half of the peak-to-peak inductor ripple current. When the overcurrent condition is removed, the output voltage returns to the regulated value. If an OCL condition happens during start-up, then the device enters hiccup-mode immediately without a 1-ms wait time.

7.3.9 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the internal VREG5 regulator voltage. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.10 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 160°C), the device shuts off. This protection is a non-latch protection. During start-up, if the device temperature is higher than 160°C, the device does not start switching and does not load the MODE settings. If the device temperature goes higher than T_{SDN} threshold after start-up, it stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. The device re-starts switching when the temperature goes below the thermal shutdown threshold but the MODE settings are not re-loaded again.

7.3.11 Output Voltage Discharge

The device has a 370-Ω discharge switch that discharges the output V_{OUT} through the SW node during any event of fault like output overvoltage, output undervoltage, T_{SD}, and if VREG5 voltage below the UVLO, and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

7.4 Device Functional Modes

7.4.1 Light Load Operation

When the MODE pin is selected to operate in FCCM mode, the converter operates in continuous conduction mode (FCCM) during light-load conditions. During FCCM, the switching frequency (f_{SW}) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. If the MODE pin is selected to operate in Eco-mode, the device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode maintains higher efficiency at light load with a lower switching frequency.

7.4.2 Standby Operation

The TPS568231 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of approximately 9 µA when in standby condition.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The schematic of 図 8-1 shows a typical application for TPS568231. This design converts an input voltage range of 4.5 V to 17 V down to 1.2 V with a maximum output current of 8 A.

8.2 Typical Application

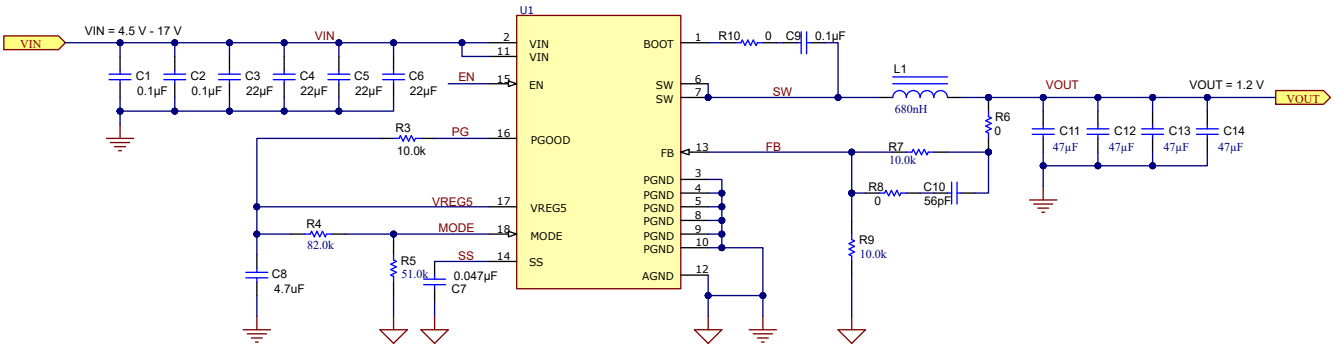


図 8-1. Application Schematic

8.2.1 Design Requirements

表 8-1. Design Parameters

Parameter		Conditions	Min	Typ	Max	Unit
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			8		A
ΔV_{OUT}	Transient response			40		mV
V_{IN}	Input voltage		4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple			20		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		Internal UVLO		V
	Stop input voltage	Input voltage falling		Internal UVLO		V
f_{SW}	Switching frequency			800		kHz
Operating mode				DCM		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, change the value of the upper feedback resistor. By changing this resistor, the user can change the output voltage above 0.6 V. See 式 6.

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$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}}\right) \quad (6)$$

8.2.2.1.2 Switching Frequency and MODE Selection

Switching frequency, current limit, and switching mode (DCM or FCCM) are set by a voltage divider from VREG5 to GND connected to the MODE pin. See 表 7-2 for possible MODE pin configurations. Switching frequency selection is a trade-off between higher efficiency and smaller system solution size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses, which impact efficiency and thermal performance. For this design, 800 kHz is chosen as the switching frequency. The switching mode is DCM and the output current is 8 A.

8.2.2.1.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See 表 8-2 for recommended inductor values.

Use 式 7 and 式 8 to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right)^2} \quad (7)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (8)$$

During transient, short-circuit conditions, the inductor current can increase up to the current limit of the device, so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.4 Output Capacitor Selection

After selecting the inductor, the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. 表 8-2 gives the recommended output capacitance range.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)} / I_{OUT(ripple)}$.

表 8-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	f_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
0.6	10	0	400	0.68	300	500	—
			800	0.47	100	500	—
			1200	0.33	88	500	—
1.2	10	10	400	1.2	100	500	—
			800	0.68	88	500	—
			1200	0.47	88	500	—
3.3	10	45.3	400	2.4	88	500	100 – 220
			800	1.5	88	500	100 – 220
			1200	1.2	88	500	100 – 220

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表 8-2. Recommended Component Values (continued)

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	f_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
5.5	10	82.5	400	3.3	88	500	100 – 220
			800	2.4	88	500	100 – 220
			1200	1.5	88	700	100 – 220

8.2.2.1.5 Input Capacitor Selection

式 9 gives the minimum input capacitance required.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (9)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. Use 式 10 to calculate the input ripple current:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (10)$$

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8.2.3 Application Curves

V_{IN} = 12 V. T_a = 25°C unless otherwise specified.

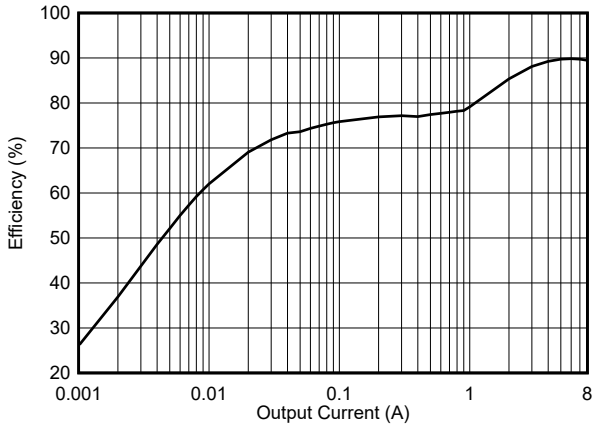


図 8-2. Efficiency

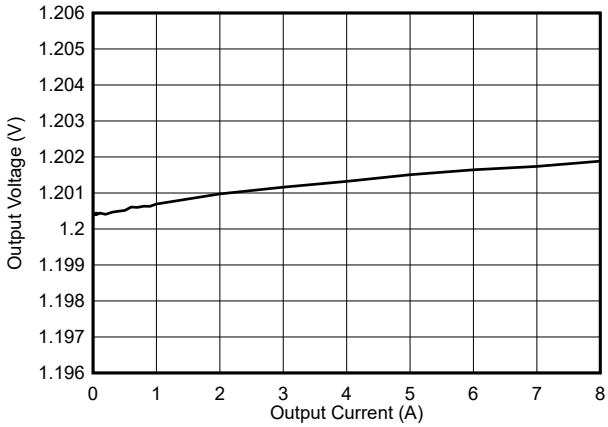


図 8-3. Load Regulation

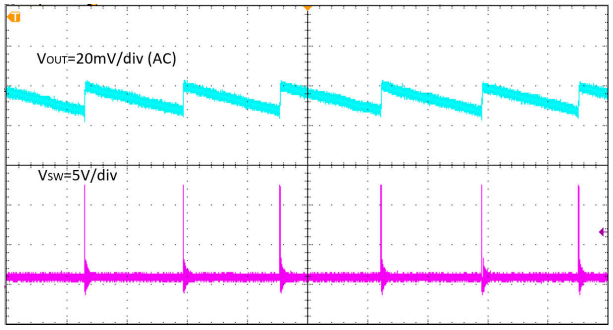


図 8-4. Output Voltage Ripple, I_{OUT} = 10 mA, Time = 80 µS/div

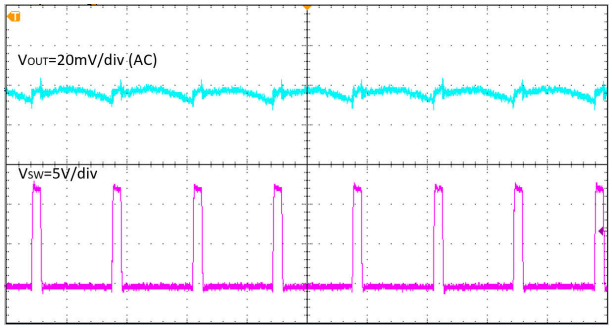


図 8-5. Output Voltage Ripple, I_{OUT} = 8 A, Time = 1 µS/div

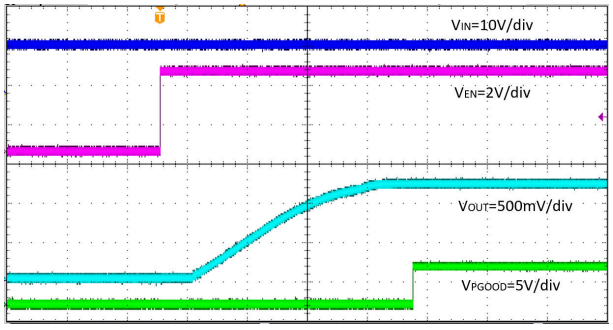


図 8-6. Start-Up Relative to EN Rising, Time = 2 ms/div

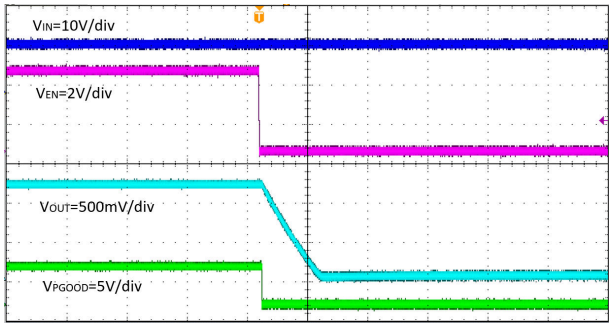


図 8-7. Shutdown Relative to EN Falling, Time = 200 µS/div

8.3 Power Supply Recommendations

The TPS568231 is intended to be powered by a well regulated DC voltage. The input voltage range is 3.8 V to 17 V. The TPS568231 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS568231 circuit, TI recommends some additional input bulk capacitance. Typical values are 100 µF to 470 µF.

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8.4 Layout

8.4.1 Layout Guidelines

- Use a four-layer or six-layer PCB for good thermal performance and with maximum ground plane. 3-inch × 3-inch, four-layer PCB with 2-oz copper is used as an example.
- VIN, PGND, and SW traces must be as wide as possible to reduce trace impedance and improve heat dissipation.
- Place equal capacitors on each side of the IC. Place them right from each VIN to PGND pin as close as possible to the device on the same side of the PCB.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer.
- Use multiple vias near both PGND pins and use the layer directly below the device to connect them together, which helps to minimize noise and can help heat dissipation.
- Inner layer 1 is ground with the PGND to AGND net tie.
- Inner layer 2 has VIN copper pour that has vias to the top layer VIN.
- Bottom layer is GND with the BOOT trace routing.
- Reference feedback to the quiet AGND and route away from the switch node. Also keep feedback resistors and the feedforward capacitor near the IC.

8.4.2 Layout Example

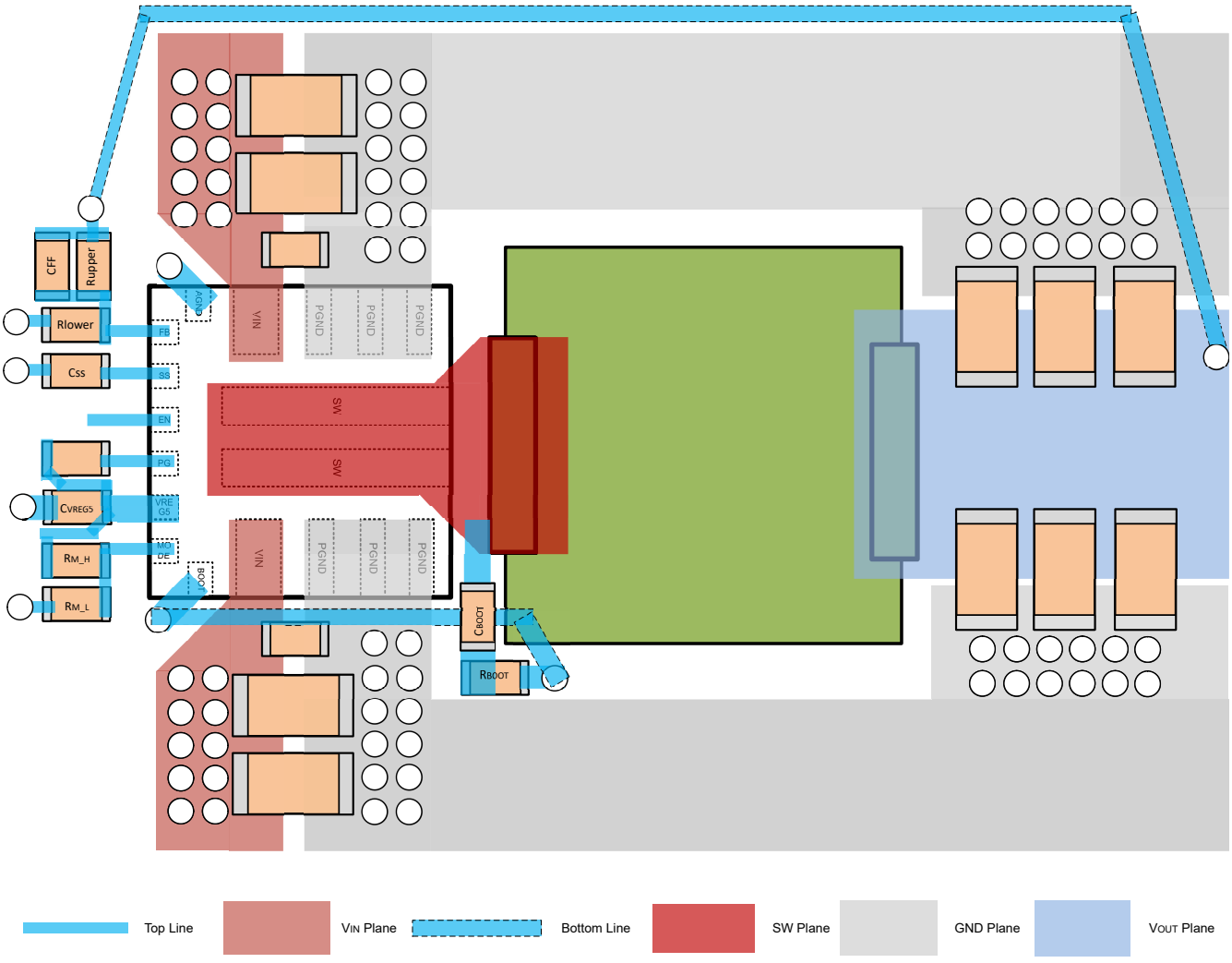


図 8-8. Layout Example

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS568231RNNR	Active	Production	VQFN-HR (RNN) | 18	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	568231
TPS568231RNNR.A	Active	Production	VQFN-HR (RNN) | 18	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	568231

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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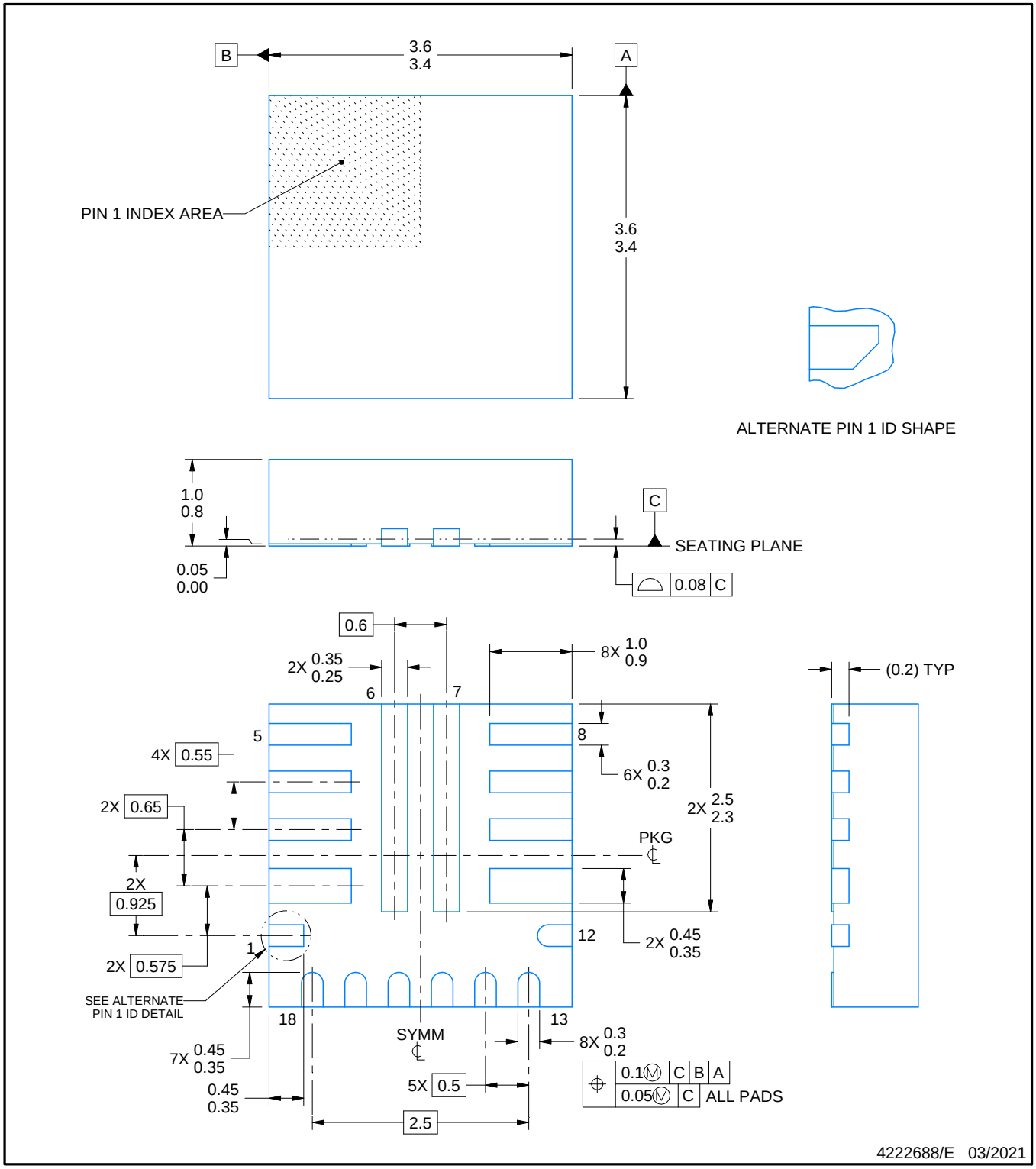
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RNN0018A

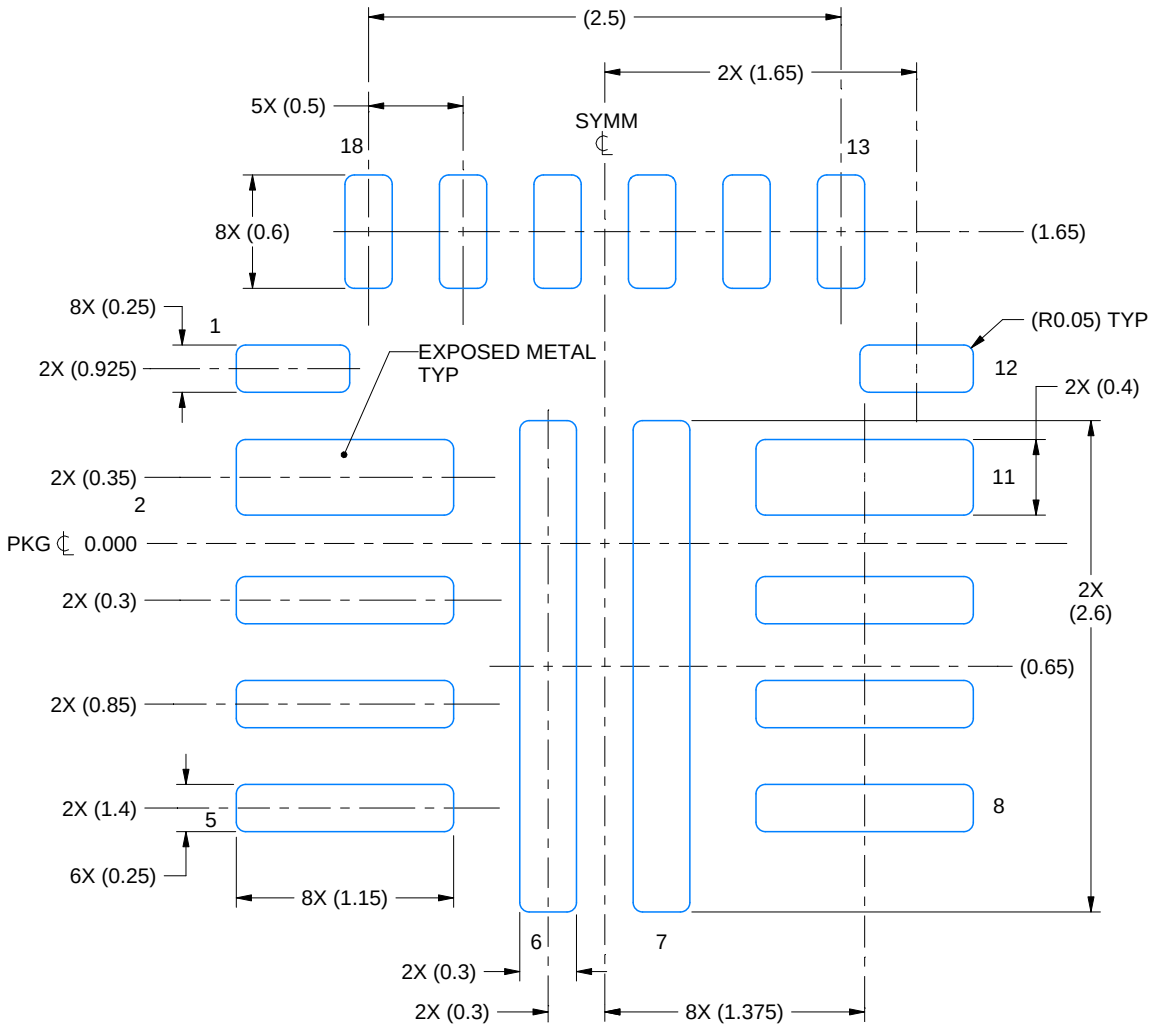
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

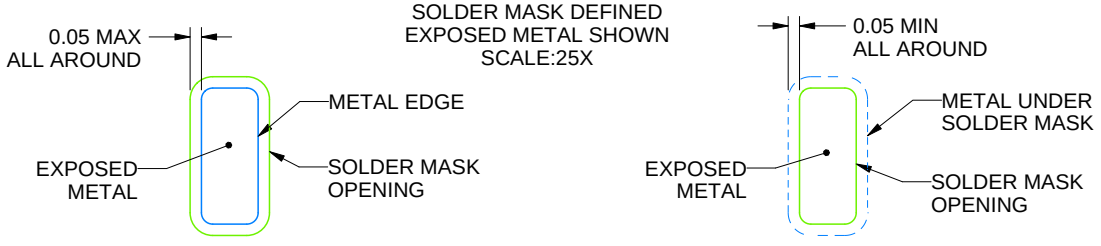


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

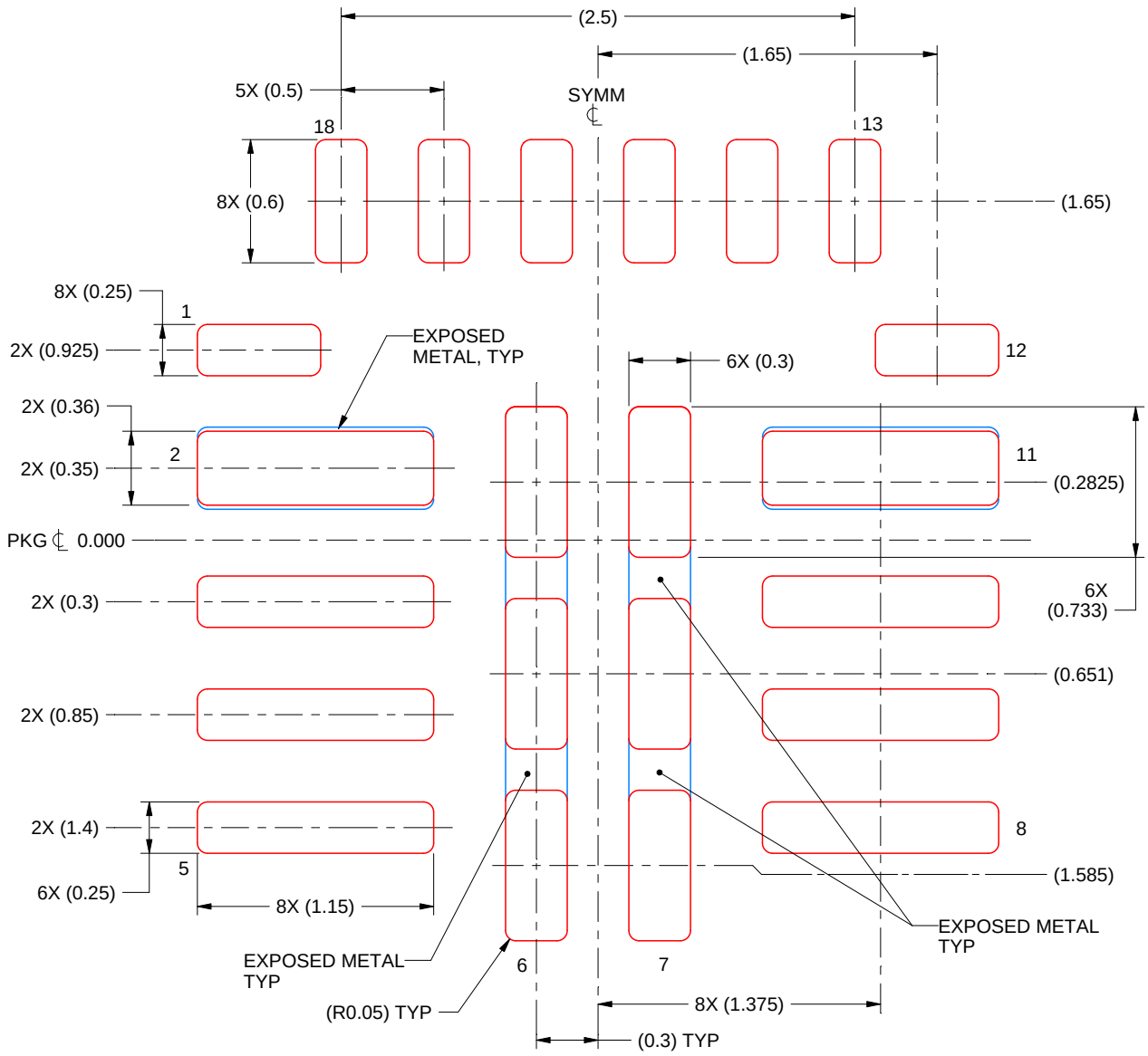
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4222688/E 03/2021

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 83% - PADS 2 & 11: 90%
SCALE:30X

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NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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