TPS59603-Q1 車載高周波数 CPU コア電源向け同期整流降圧 FET ドライバ

1 特長

- 車載アプリケーション用にAEC-Q100認定済み
  - デバイス温度グレード1: -40℃～125℃
  - デバイス HBM (人体モデル) ESD 分類レベル H2
  - デバイス CDM (デバイス帯電モデル) ESD 分類レベル C3B
- デッドタイム短縮駆動回路により CCM を最適化
- 自動ゼロクロス検出機能により DCM 効率を最適化
- 複数の低消費電力モードにより軽負荷時効率を最適化
- 信号経路の遅延を最適化して高周波数での動作を実現
- 内蔵する BST スイッチの駆動能力を RdsON の小さい FET 用に最適化
- 5V FET 駆動用に最適化
- 変換入力電圧範囲 (V_{IN}) : 2.5～28V
- 2mm × 2mm、8 ピン、ウェッタブル・フランク WSON サーマル・パッド・パッケージ

2 アプリケーション

- 高周波数 CPU を搭載した車載リアシート・エンターテインメント (RSE) タブレット
- 車載 ADAS プロセッサ・コア電源

3 概要

TPS59603-Q1 ドライバは、高周波数 CPU V_{CORE} アプリケーション向けに最適化されています。デッドタイム短縮駆動や自動ゼロクロス検出といった高度な機能により、全負荷範囲にわたって効率を最適化できます。

$\overline{\text{SKIP}}$ ピンにより CCM 動作を実現し、出力電圧の制御管理をサポートします。また、TPS59603-Q1 は 2 つの低消費電力モードに対応しています。トライステートの PWM 入力により、静止電流を 130μA まで低減し、高速応答を実現します。$\overline{\text{SKIP}}$ がトライステート状態に維持されると、電流は 8μA まで低減します (スイッチングを再開するには標準で 20μs 必要)。適切な TI コントローラを組み合わせることにより、極めて高性能の電源システムを実現できます。

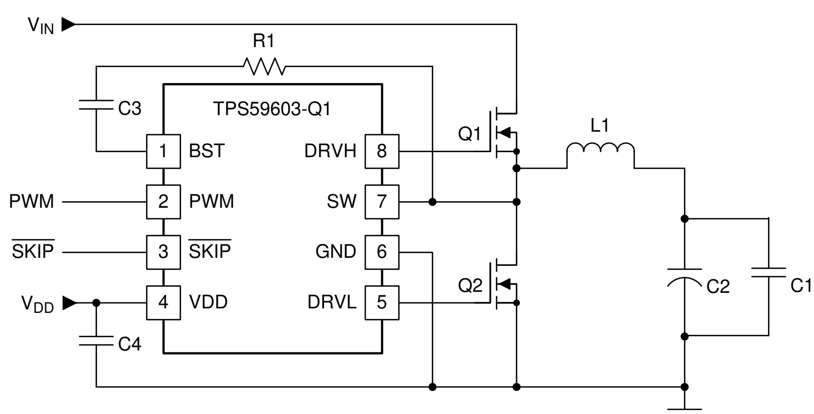
TPS59603-Q1 は省スペースで放熱特性に優れた 8 ピン、2mm x 2mm ウェッタブル・フランク WSON パッケージで供給され、–40℃～125℃で動作します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS59603-Q1	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーション概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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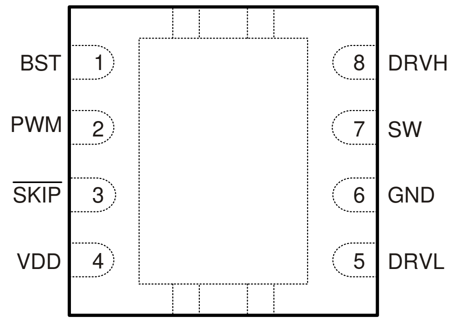
• 変更「関連資料」セクションのハイパーリンク	14

5 Pin Configuration and Functions

DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
BST	1	I	High-side N-channel FET bootstrap voltage input; power supply for high-side driver
DRVH	8	O	High-side N-channel gate drive output
DRVL	5	O	Synchronous low-side N-channel gate drive output
GND	6	G	Synchronous low-side N-channel gate drive return and device reference
PWM	2	I	PWM input. A tri-state voltage on this pin turns off both the high-side (DRVH) and low-side drivers (DRVL)
$\overline{\text{SKIP}}$	3	I	When $\overline{\text{SKIP}}$ is LO, the zero crossing comparator is active. The power chain enters discontinuous conduction mode when the inductor current reaches zero. When $\overline{\text{SKIP}}$ is HI, the zero crossing comparator is disabled, and the driver outputs follow the PWM input. A tri-state voltage on $\overline{\text{SKIP}}$ puts the driver into a very-low power state.
SW	7	I/O	High-side N-channel gate drive return. Also, zero-crossing sense input
VDD	4	I	5-V power supply input; decouple to GND with a ceramic capacitor with a value of 1 µF or greater
Thermal Pad		G	Tie to system GND plane with multiple vias

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings(1) (2)

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD	–0.3	6	V
	PWM, $\overline{\text{SKIP}}$	–0.3	6	
Output voltage	BST	–0.3	35	V
	BST (transient <20 ns)	–0.3	38	
	BST to SW; DRVH to SW	–0.3	6	
	SW	–2	30	
	DRVH, SW (transient <20 ns)	–5	38	
	DRVL	–0.3	6	
Ground pins	GND to PAD	–0.3	0.3	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature range, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VDD	4.5	5	5.5	V
	PWM, $\overline{\text{SKIP}}$	–0.1		5.5	
Output voltage	BST	–0.1		34	V
	BST to SW; DRVH to SW	–0.1		5.5	
	SW	–1		28	
	DRVL	–0.1		5.5	
Ground pins	GND to PAD	–0.1		0.1	V
Operating junction temperature, T_J		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS59603-Q1 WSON (DSG) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.7	°C/W

(1) 従来および新しい熱測定値の詳細については、『*Semiconductor and IC Package Thermal Metrics*』アプリケーション・レポート(SPRA953)を参照してください。

6.5 Electrical Characteristics

These specifications apply for –40°C ≤ T_J ≤ 125°C, and V_{VDD} = 5 V unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD INPUT SUPPLY						
I_{CC}	Supply current (operating)	$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = High		160	600	µA
		$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = Low		250		
		$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = Float		130		
		$V_{\overline{SKIP}}$ = Float		8		
VDD UNDERVOLTAGE LOCKOUT (UVLO)						
V_{UVLO}	UVLO threshold	Rising threshold			4.19	V
		Falling threshold	3.65			
V_{UVHYS}	UVLO hysteresis			0.2		V
PWM AND $\overline{\text{SKIP}}$ I/O SPECIFICATIONS						
R_I	Input impedance	Pullup to VDD		1.7		MΩ
		Pulldown (to GND)		800		kΩ
V_{IL}	Low-level input voltage				0.6	V
V_{IH}	High-level input voltage		2.70			V
V_{IHH}	Hysteresis			0.2		V
V_{TS}	Tri-state voltage		1.3		2.0	V
$t_{THOLD(off1)}$	Tri-state activation time (falling) PWM			60		ns
$t_{THOLD(off2)}$	Tri-state activation time (rising) PWM			60		ns
t_{TSKF}	Tri-state activation time (falling) $\overline{\text{SKIP}}$			1		µs
t_{TSKR}	Tri-state activation time (rising) $\overline{\text{SKIP}}$			1		µs
$t_{3RD(PWM)}$	Tri-state exit time PWM				100	ns
$t_{3RD(\overline{SKIP})}$	Tri-state exit time $\overline{\text{SKIP}}$				50	µs
HIGH-SIDE GATE DRIVER (DRVH)						
$t_{R(DRVH)}$	Rise time	DRVH rising, C_{DRVH} = 3.3 nF; 20% to 80%		30		ns
$t_{RPD(DRVH)}$	Rise time propogation delay	C_{DRVH} = 3.3 nF		40		ns
R_{SRC}	Source resistance	Source resistance, (V_{BST} – V_{SW}) = 5 V, high state, (V_{BST} – V_{DRVH}) = 0.1 V		2	4	Ω
$t_{F(DRVH)}$	Fall time	DRVH falling, C_{DRVH} = 3.3 nF		8		ns
$t_{FPD(DRVH)}$	Fall-time propagation delay	C_{DRVH} = 3.3 nF		25		ns
R_{SNK}	Sink resistance	Sink resistance, (V_{BST} – V_{SW}) forced to 5 V, low state (V_{DRVH} – V_{SW}) = 0.1 V		0.5	1.6	Ω
R_{DRVH}	DRVH to SW resistance (1)			100		kΩ

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

These specifications apply for –40°C ≤ T_J ≤ 125°C, and V_{VDD} = 5 V unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE GATE DRIVER (DRVL)						
$t_{R(DRVL)}$	Rise time	DRVL rising, C_{DRVL} = 3.3 nF; 20% to 80%		15		ns
$t_{RPD(DRVL)}$	Rise time propagation delay	C_{DRVL} = 3.3 nF		35		ns
R_{SRC}	Source resistance	Source resistance, (V_{VDD}–GND) = 5 V, high state, (V_{VDD} – V_{DRVL}) = 0.1 V		1.5	3	Ω
$t_{F(DRVL)}$	Fall time	DRVL falling, C_{DRVL} = 3.3 nF		10		ns
$t_{FPD(DRVL)}$	Fall-time propagation delay	C_{DRVL}= 3.3 nF		15		ns
R_{SNK}	Sink resistance	Sink resistance, (V_{VDD}– GND) = 5 V, low state, (V_{DRVL} – GND) = 0.1 V		0.4	1.6	Ω
R_{DRVL}	DRVL to GND resistance[(1)]			100		kΩ
GATE DRIVER DEAD-TIME						
$t_{R(DT)}$	Rising edge		0	20	40	ns
$t_{F(DT)}$	Falling edge		0	10	25	ns
ZERO CROSSING COMPARATOR						
V_{ZX}	Zero crossing offset	SW voltage rising	–2.25	0	2.00	mV
BOOTSTRAP SWITCH						
V_{FBST}	Forward voltage	I_F = 10 mA		120	240	mV
I_{RLEAK}	Reverse leakage	(V_{BST} – V_{VDD}) = 25 V			2	μA
$R_{DS(on)}$	On-resistance			12	24	Ω

6.6 Typical Characteristics

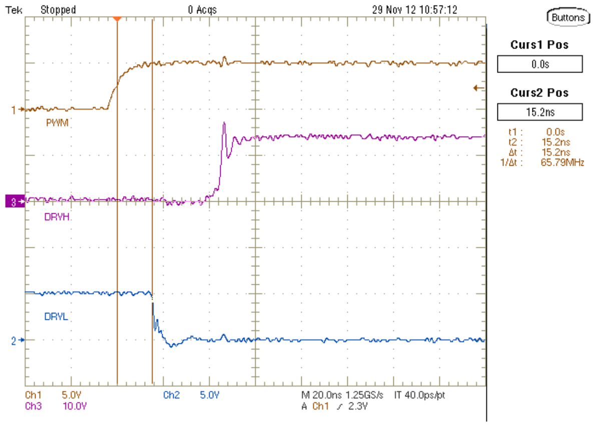


図 1. PWM High to DRVL Low

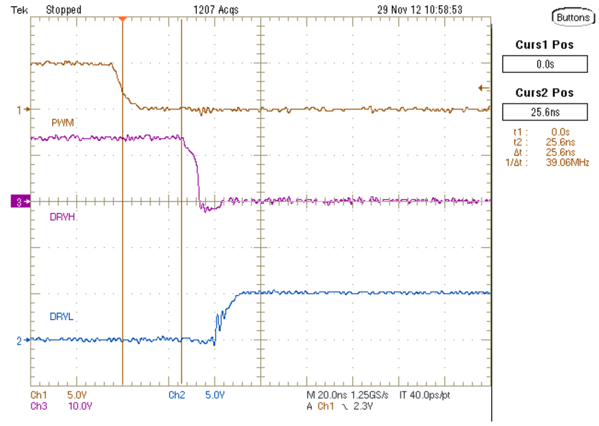


図 2. PWM Low to DRVH Low

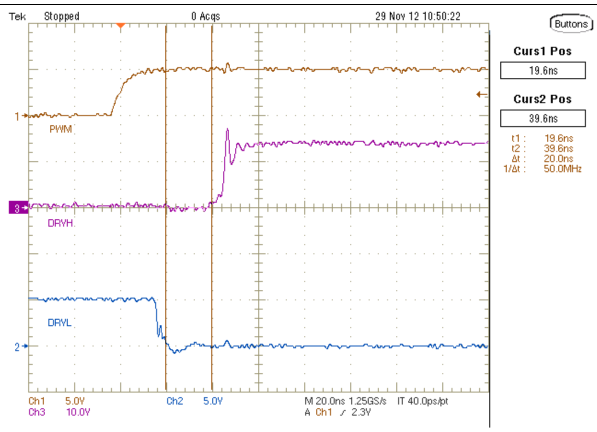


図 3. DRVL Low to DRVH High

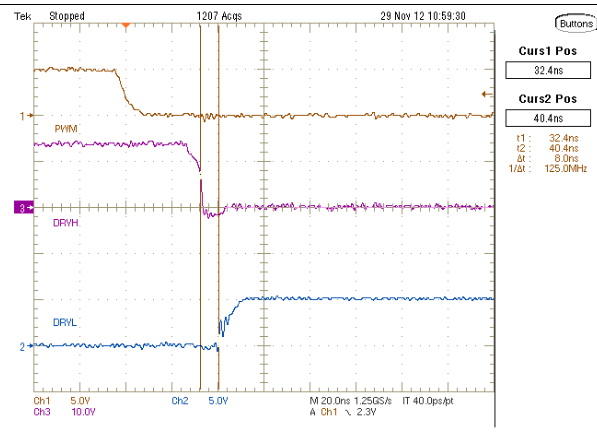


図 4. DRVH Low to DRVL High

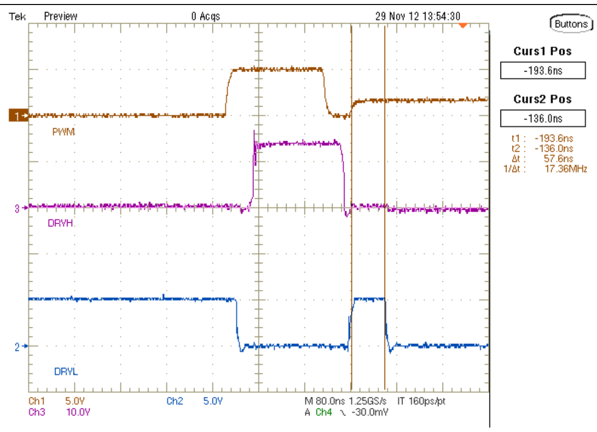


図 5. PWM Low to Tri-State

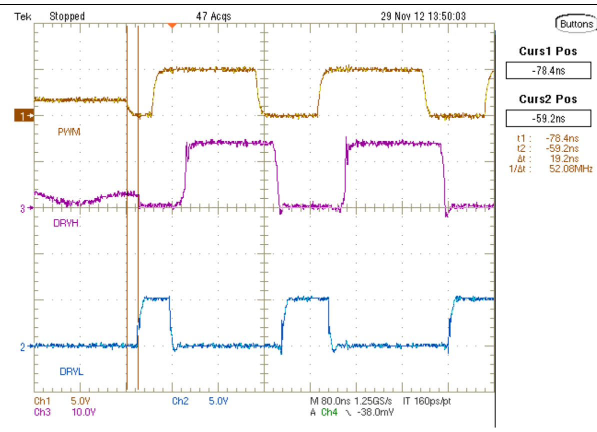


図 6. PWM Tri-State to Low

Typical Characteristics (continued)

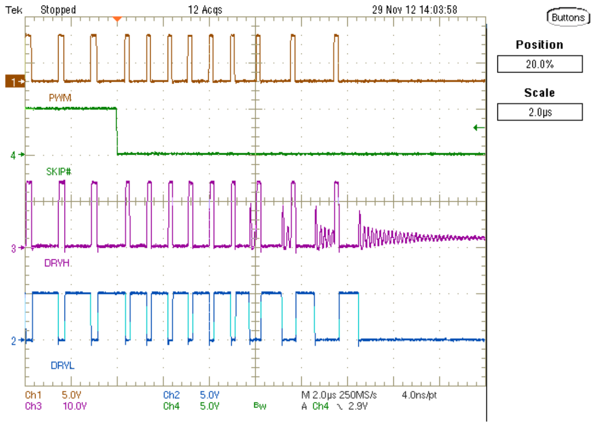


図 7. SKIP Mode Entry

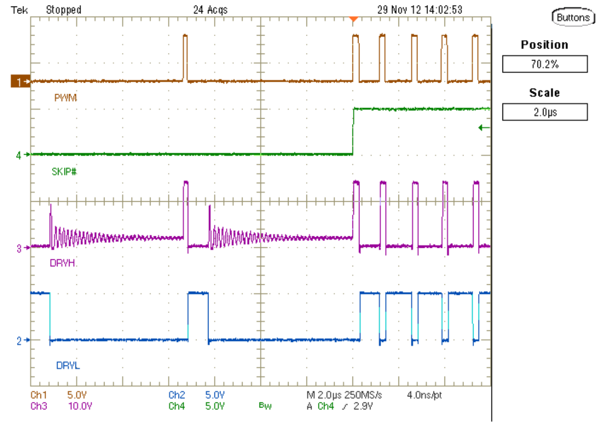


図 8. SKIP Mode Exit

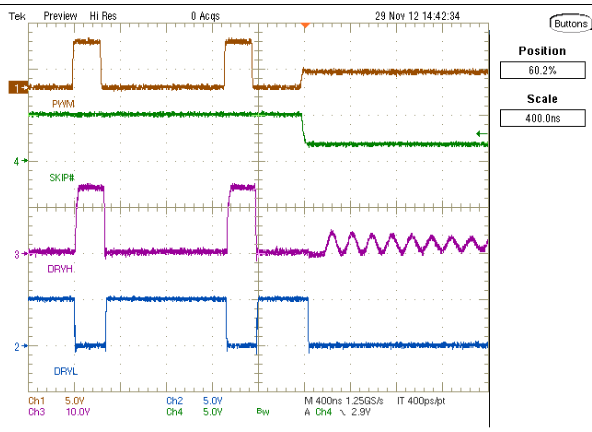


図 9. Very-Low-Power Mode Entry

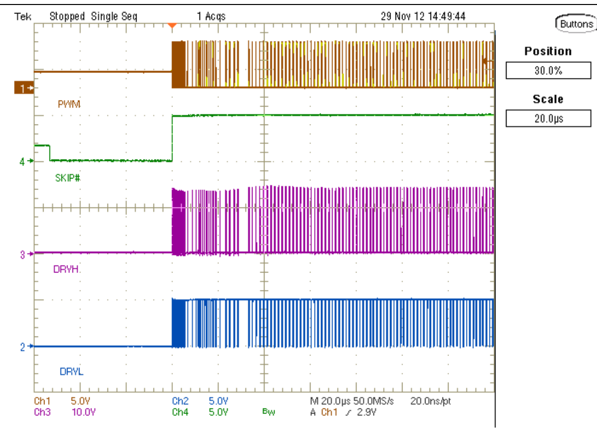
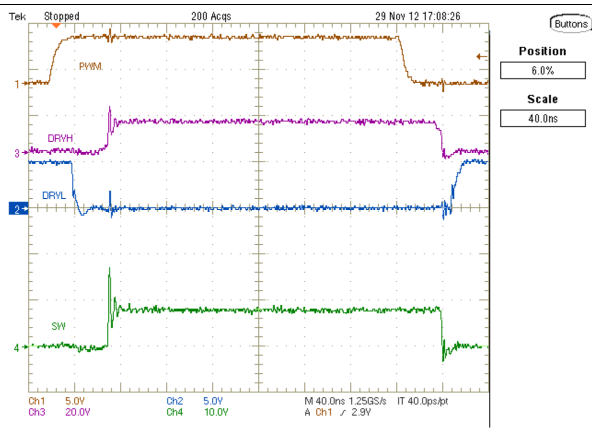
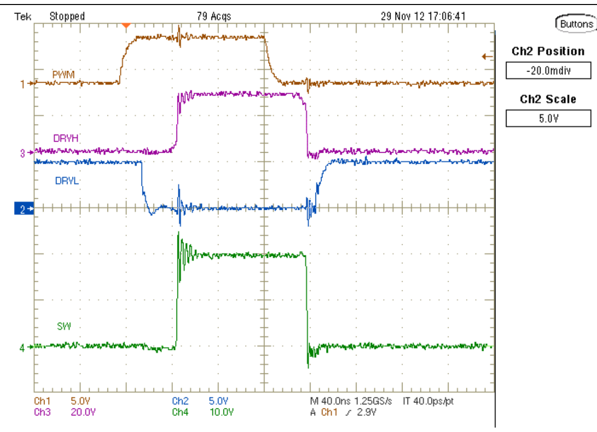


図 10. Very-Low-Power Mode Exit



V_{IN} = 8 V

図 11. SW Node-Ringing



V_{IN} = 20 V

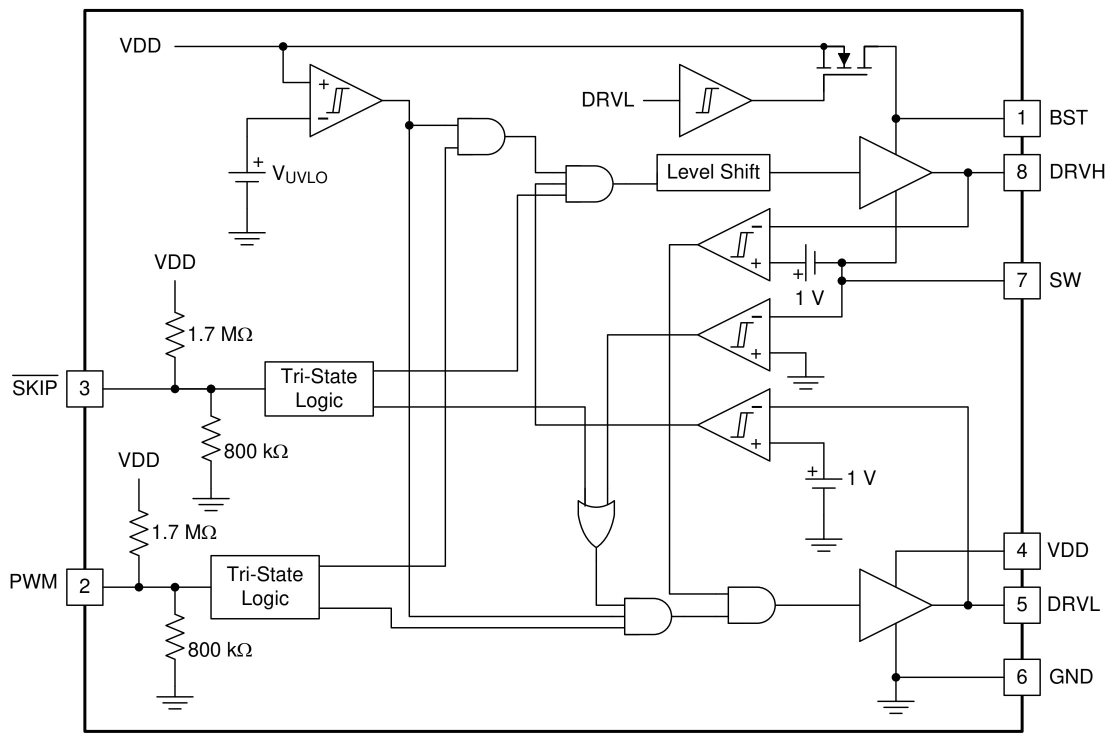
図 12. SW Node-Ringing

7 Detailed Description

7.1 Overview

The TPS59603-Q1 device is a synchronous-buck MOSFET driver designed to drive both high-side and low-side MOSFETs. It allows high-frequency operation with current driving capability matched to the application. The integrated boost switch is internal. The TPS59603-Q1 device employs dead-time reduction control and shoot-through protection, which helps avoid simultaneous conduction of high-side and low-side MOSFETs. Also, the drivers improve light-load efficiency with integrated DCM-mode operation using adaptive crossing detection. Typical applications yield a steady-state duty cycle of 60% or less. For high steady-state duty cycle applications, including a small external Schottky diode may help to ensure sufficient charging of the bootstrap capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 UVLO Protection

The UVLO comparator evaluates the VDD voltage level. As V_{VDD} rises, both DRVH and DRVL hold actively low at all times until V_{VDD} reaches the higher UVLO threshold (V_{UVLO_H}). Then, the driver becomes operational and responds to PWM and $\overline{\text{SKIP}}$ commands. If VDD falls below the lower UVLO threshold (V_{UVLO_L} = V_{UVLO_H} – Hysteresis), the device disables the driver and drives the outputs of DRVH and DRVL actively low. 図 13 shows this function.

> **注意**
>
> Do not start the driver in the very low power mode ($\overline{\text{SKIP}}$ = Tri-state).

Feature Description (continued)

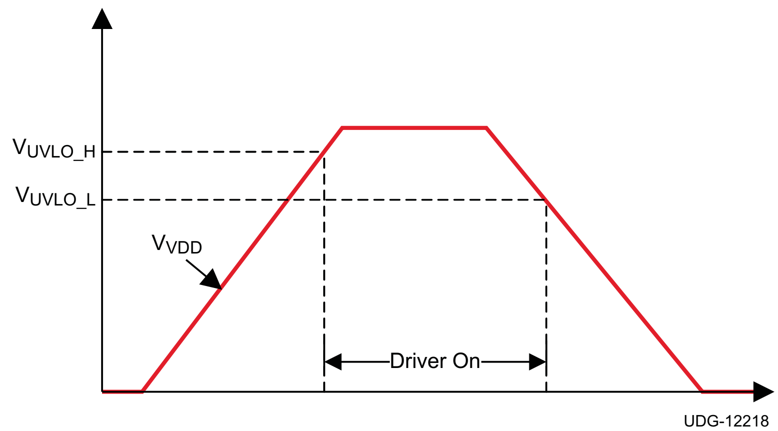


図 13. UVLO Operation

7.3.2 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pullup to maintain the voltage within the tri-state window during low-power modes. Operation into and out of a tri-state condition follows the timing diagram outlined in 図 14.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined as the PWM voltage range between PWM logic high (V_{IH}) and logic low (V_{IL}) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3-V (typical) and 5-V (typical) PWM drive signals.

When the PWM exits the tri-state condition, the driver enters CCM for a period of 4 µs, regardless of the state of the $\overline{\text{SKIP}}$ pin. Typical operation requires this time period in order for the auto-zero comparator to resume.

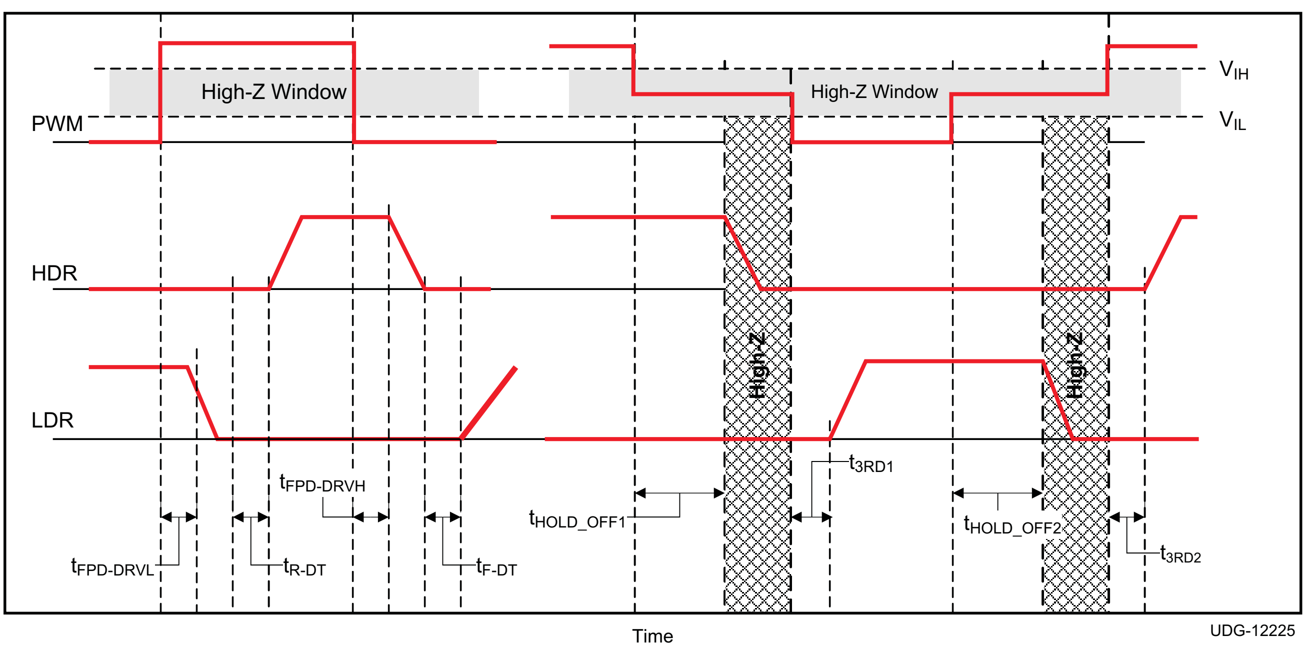


図 14. PWM Tri-State Timing Diagram

Feature Description (continued)

7.3.3 $\overline{\text{SKIP}}$ Pin

The $\overline{\text{SKIP}}$ pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When $\overline{\text{SKIP}}$ is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When $\overline{\text{SKIP}}$ is high, the ZX comparator disables, and the converter enters FCCM mode. When the $\overline{\text{SKIP}}$ pin is in a tri-state condition, typical operation forces the gate driver outputs low and the driver enters a very-low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When the $\overline{\text{SKIP}}$ pin voltage is pulled either low or high, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

表 1 shows the logic functions of UVLO, PWM, $\overline{\text{SKIP}}$, DRVH, and DRVL.

表 1. Logic Functions

UVLO	PWM	$\overline{\text{SKIP}}$	DRVL	DRVH	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High (1)	Low	DCM (1)
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	Low power
Inactive	—	Tri-state	Low	Low	Very-low power

(1) Until zero crossing protection occurs.

7.3.3.1 Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

7.3.4 Adaptive Dead-Time Control and Shoot-Through Protection

The driver utilizes an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time and maintain high efficiency. When the PWM input voltage becomes high, the low-side MOSFET gate voltage begins to fall after a propagation delay. At the same time, DRVL voltage is sensed, and high-side driving voltage starts to increase after DRVL voltage is lower than a proper threshold.

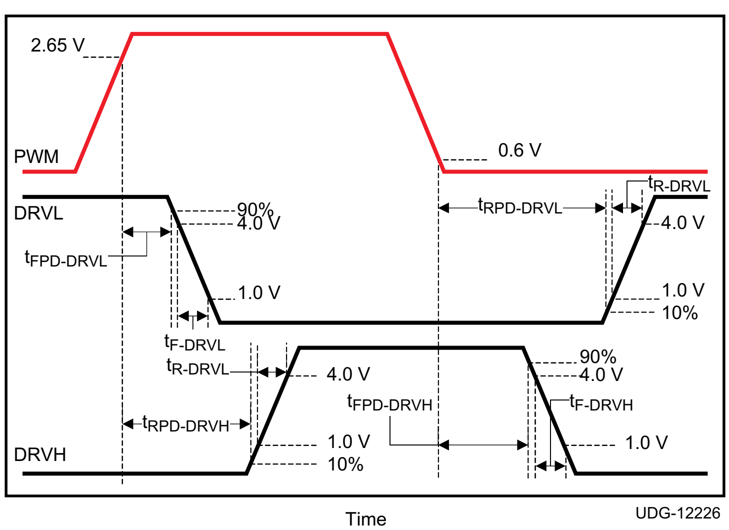


図 15. Rise and Fall Timing and Propagation Delay Definitions

Typical operation manages to near zero the dead-time between the low-side gate turn-off to high-side gate voltage turn-on, and high-side gate turn-off to low-side gate turn-on, in order to avoid simultaneous conduction of both MOSFETs, as well as to reduce body diode conduction and recovery losses. This operation also reduces ringing on the leading edge of the SW waveform.

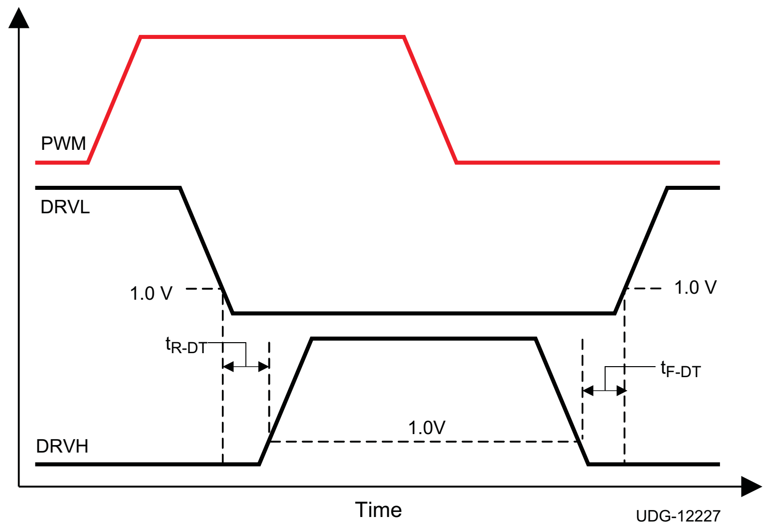


図 16. Dead-Time Definitions

7.3.5 Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and BST pin is replaced by a FET, which is gated by the DRVL signal.

7.4 Device Functional Modes

The TPS59603-Q1 device operates in CCM mode when the $\overline{\text{SKIP}}$ pin is high, and it enters DCM mode when the $\overline{\text{SKIP}}$ pin is low. When both the $\overline{\text{SKIP}}$ pin and the PWM pin are in a tri-state condition, it forces the gate driver outputs low and the driver enters a very-low-power state.

8 Power Supply Recommendations

The voltage range for the VDD pin is between 4.5 V and 5.5 V. A 5-V power supply is recommended for the VDD pin of the TPS59603-Q1 device.

9 Layout

9.1 Layout Guidelines

To improve the switching characteristics and design efficiency, these layout rules must be considered:

- Locate the driver as close as possible to the MOSFETs.
- Locate the VDD and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET, but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the switch-node as for the GND.
- Use wide traces for DRVH and DRVL closely following the related SW and GND traces. A width of between 80 and 100 mils is preferable where possible.
- Place the bypass capacitors as close as possible to the driver.
- Avoid PWM and enable traces going close to the SW and pad where high dV/dT voltage can induce significant noise into the relatively high-impedance leads.

A poor layout can decrease the reliability of the entire system.

9.2 Layout Recommendation

図 17 above shows the primary current loops in each phase, numbered in order of importance.

The most important loop to minimize the area of is loop 1, the path from the input capacitor through the high and low-side FETs, and back to the capacitor through ground.

Loop 2 is from the inductor through the output capacitor, ground, and Q2. The layout of the low-side gate drive (Loops 3a and 3b) is important. The guidelines for the gate drive layout are:

- Make the low-side gate drive length as short as possible (1 inch or less preferred).
- Make the DRVL width to length ratio of 1:10, wider (1:5) if possible.
- If changing layers is necessary, use at least two vias.

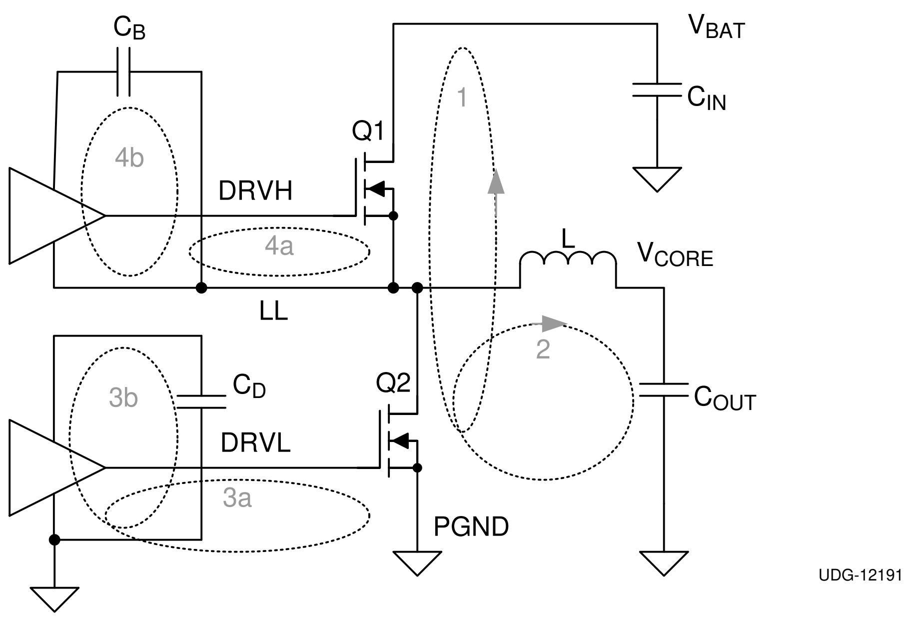


図 17. Layout recommendations to minimize major Current loops

10 デバイスおよびドキュメントのサポート

10.1 デバイス・サポート

10.1.1 開発サポート

Power Stage Designer については、最も一般的に使用されるスイッチ・モード電源に使用可能な Power Stage Designer[tm] ツールを参照してください。

10.2 ドキュメントのサポート

10.2.1 関連資料

『TPS59632-Q1 2.5-V To 24-V, 3-, 2-, and 1-Phase Step-Down Driverless Controller for Automotive ADAS Applications』データシート (英語)

10.3 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS59603QDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	603Q
TPS59603QDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	603Q
TPS59603QDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	603Q
TPS59603QDSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	603Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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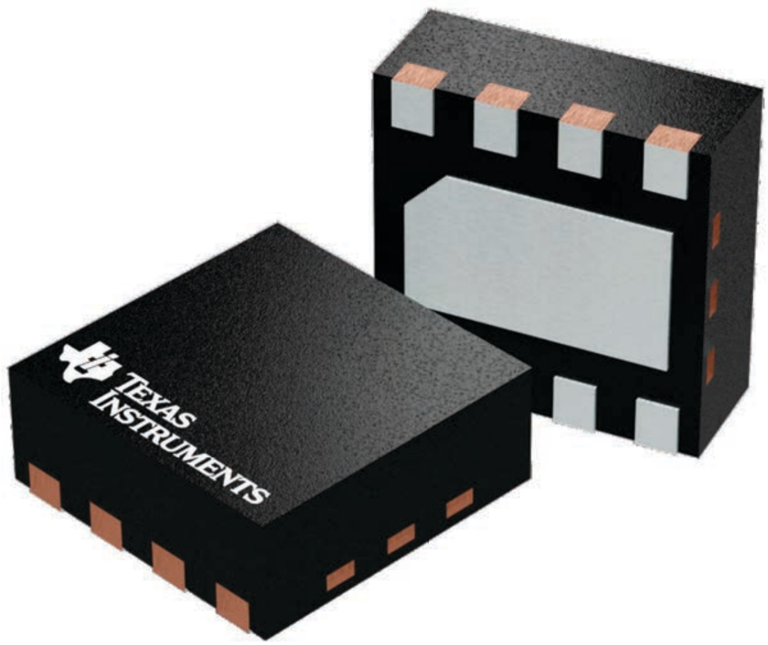
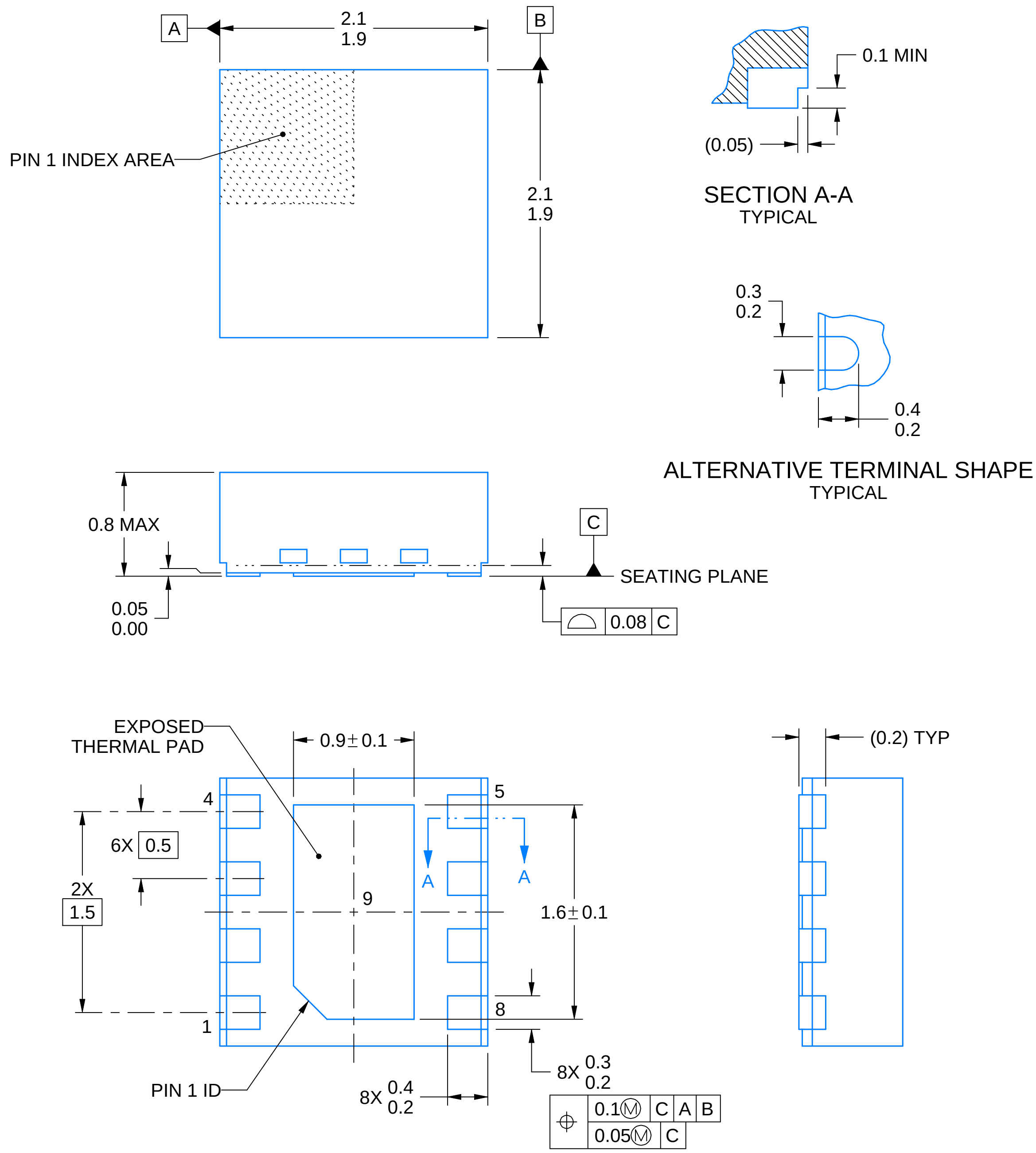
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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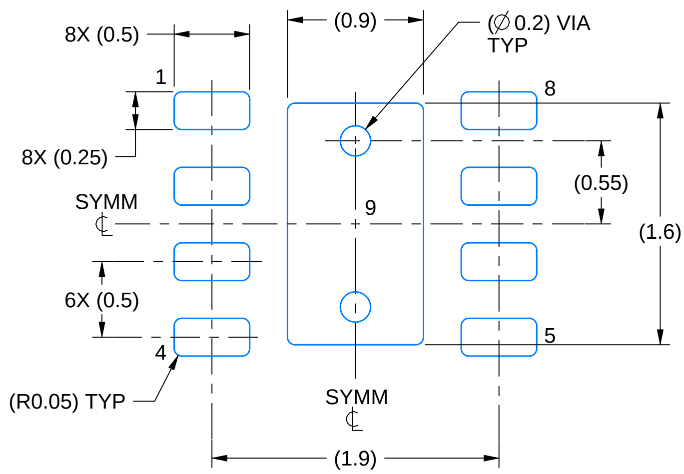
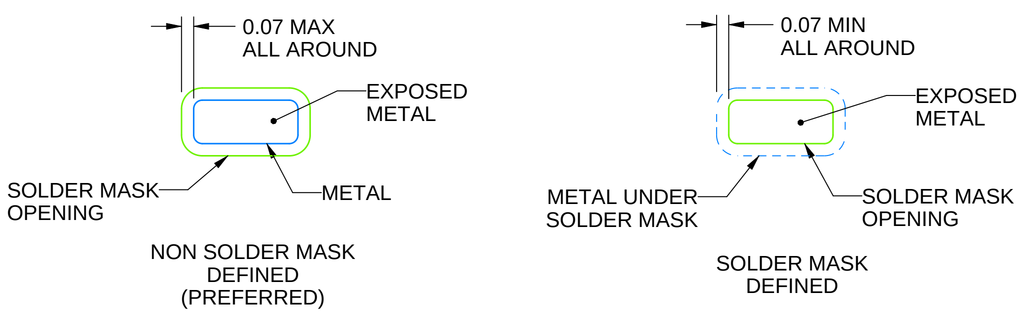
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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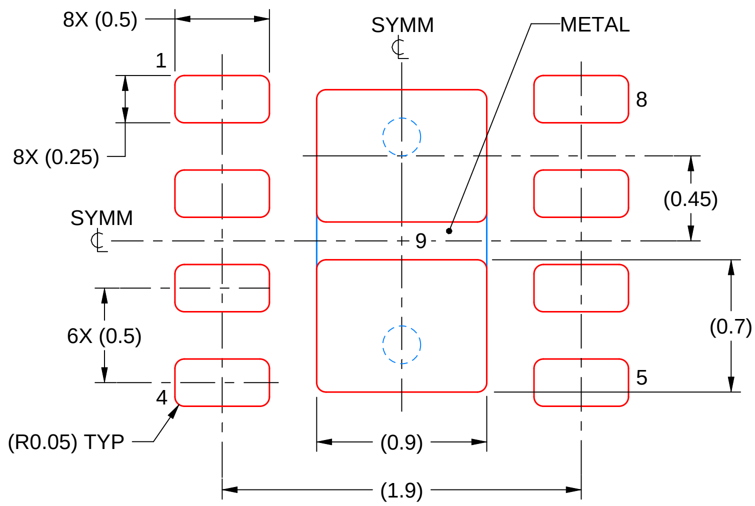
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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