TEXAS INSTRUMENTS
TPS61260, TPS61261
JAJSFC2C – MAY 2011 – REVISED APRIL 2018

TPS6126x 0.8V入力、同期整流昇圧コンバータ、100mA出力電流

1 特長

- 入力電圧範囲: 0.8V～4.0V
- 最大95%の効率
- 3.3V_{out}時出力電流100mA (VIN＞1V)
- 1.8V～4.0Vの固定および可変出力電圧オプション
- 10mA～100mAのプログラミング可能な平均出力電流
- 可変出力電流制限により超小型インダクタに対応
- パワー・セーブ・モードによる低出力電力時の効率向上
- 29µAの静止電流
- 高度なソフトスタート
- 2.5MHzの疑似固定周波数動作
- 出力過電圧保護
- シャットダウン中の負荷切断
- 低電圧誤動作防止
- 2.00×2.00mmの6ピンWSONパッケージで供給

2 アプリケーション

- あらゆる1セル/2セルのアルカリ/ニッカド/ニッケル水素バッテリ駆動製品
- 高出力インピーダンス・バッテリ(コイン電池)駆動製品
- 個人用医療機器
- LEDドライバ
- レーザーポインタ
- ワイヤレス・ヘッドセット
- 産業用の計測機器

3 概要

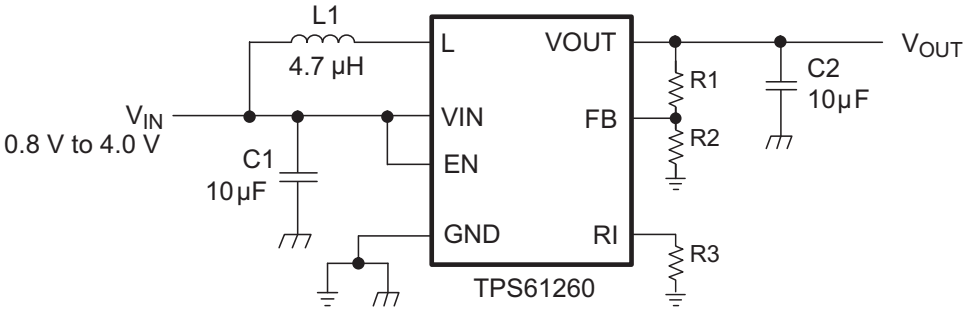
TPS6126xは、1セル/2セルのアルカリ/ニッカド/ニッケル水素バッテリで駆動する製品向けの電源ソリューションを提供します。独自の高度なソフトスタートにより、コイン電池などの高出力インピーダンス・バッテリで駆動する製品にも適しています。1セルのアルカリ・バッテリから最大100Aの電流を出力でき、0.8V以下まで放電できます。

この昇圧コンバータは、疑似固定周波数のパルス幅変調(PWM)コントローラを基礎とし、同期整流を使用して最大の効率を実現しています。負荷電流が低い時にはコンバータがパワー・セーブ・モードに移行し、広い負荷電流範囲にわたって高効率を維持します。スイッチの最大平均電流は、最大700mAまでのプログラミング可能な値に制限されます。出力電圧については、外付けの分圧抵抗を使用してプログラミングすることも、チップ内部で固定された電圧を使用することもできます。また、平均出力電流もプログラミング可能です。プログラミングされた出力電圧や出力電流は、コンバータによりレギュレートされるため、出力電力は低減されます。コンバータをディセーブルして、バッテリの消耗を最小限に抑えることができます。シャットダウン時には、バッテリーから負荷が切断されます。このデバイスは、6ピンのWSON (DRV)パッケージに封止されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS61260	WSON (6)	2.00mm×2.00mm
TPS61261		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。
English Data Sheet: SLVSA99

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (November 2014) から Revision C に変更 **Page**

- 変更 term from µs to (µH) in 式 3. ... 14

Revision A (February 2013) から Revision B に変更 **Page**

- 「取り扱いに関する定格」の表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加 ... 1
- Changed Minimum input voltage for startup, -40°C < T_J < 105°C, Max from 0.8 V to 1.2 V ... 5
- Added V_{EN} = 0 V, V_{IN} = 1.2 V, T_A = 25°C Test Condition and values to Shutdown current ... 5

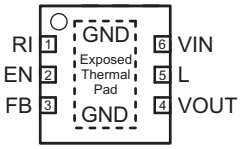
2011年5月発行のものから更新 **Page**

- Changed Supply voltage to Input supply in RECOMMENDED OPERATING CONDITIONS ... 4
- Changed ELECTRICAL CHARACTERISTICS ... 5
- 変更 Synchronous Boost Operation section ... 11
- 削除 Dynamic Current Limit section ... 12
- 変更 Inductor Selection section ... 14
- 変更 Capacitor Selection section ... 15
- 変更 PowerPAD™ to Exposed Thermal Pad ... 18

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5 Pin Configuration and Functions

6-Pin WSON
DRV Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
EN	2	I	Enable input. (High = enabled, Low = disabled). Do not leave floating.
FB	3	I	Voltage feedback of adjustable versions. Must be connected to VOUT on fixed output voltage versions.
GND	Exposed Thermal Pad		Must be soldered to achieve appropriate power dissipation and mechanical reliability. Must be connected to GND.
L	5	I	Connection for inductor
RI	1	I	Average output current programming input. A resistor with a value between 2 kΩ and 20 kΩ must be connected between the RI pin and GND.
VIN	6	I	Supply voltage for control stage
VOUT	4	O	Boost converter output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, L, VOUT, EN, FB	–0.3	5.0	V
	RI	–0.3	3.6	V
Operating junction temperature range, T_J		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
V_{ESD}	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)		0.5	kV

(1) ESD testing is performed according to the respective JESD22 JEDEC standard.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input supply voltage at VIN	0.8		4.0	V
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61260, TPS61261 DRV (6 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100	
$R_{\theta JB}$	Junction-to-board thermal resistance	35	
ψ_{JT}	Junction-to-top characterization parameter	2	
ψ_{JB}	Junction-to-board characterization parameter	36	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			0.8		4.0	V
V_{IN}	Minimum input voltage for startup		-40°C < T_J < 105°C			1.2	V
V_{OUT}	TPS61260 output voltage range			1.8		4.0	V
V_{FB}	TPS61260 feedback voltage		-40°C < T_J < 85°C	495	500	505	mV
V_{OUT}	TPS61261 output voltage			3.27	3.3	3.33	V
I_{LIM}	Average switch current limit				7 x I_{OUT}		mA
$R_{DS(on)}$	High side switch on resistance		V_{IN} = 1.2 V, V_{OUT} = 3.3 V		1000		mΩ
$R_{DS(on)}$	Low side switch on resistance		V_{IN} = 1.2 V, V_{OUT} = 3.3 V		250		mΩ
	Output voltage line regulation		PWM mode		0.5%		
	Output voltage load regulation		PWM mode		0.5%		
I_{OUT}	Average output current programming range			10		100	mA
	Average output current		R_I = 10 kΩ, T_A = 25 °C, V_{IN} < V_{OUT}	19	20	21	mA
	Average output current		R_I = 10 kΩ, 0°C < T_J < 60°C, V_{IN} < V_{OUT}	18	20	22	mA
	Average output current line regulation				0.5%		
	Average output current load regulation				0.5%		
I_Q	Quiescent current	VIN	I_O = 0 mA, V_{EN} = V_{IN} = 1.2 V, V_{OUT} = 3.3 V, Device not switching		4	7	µA
		VOUT			25	40	µA
	TPS61261 FB pin input impedance		V_{EN} = HIGH		1		MΩ
I_{SD}	Shutdown current		V_{EN} = 0 V, V_{IN} = 1.2 V		0.1	1.5	µA
			V_{EN} = 0 V, V_{IN} = 1.2 V, T_A = 25°C		0.1	0.3	µA
CONTROL STAGE							
V_{UVLO}	Under voltage lockout threshold		Falling V_{IN}	0.6	0.7	0.8	V
V_{UVLO}	Under voltage lockout threshold hysteresis				200		mV
V_{IL}	Low level input threshold voltage (EN)		V_{IN} ≤ 1.8 V, -40°C < T_J < 85°C			0.2 × V_{IN}	V
V_{IL}	Low level input threshold voltage (EN)		V_{IN} > 1.8 V, -40°C < T_J < 85°C			0.36	V
V_{IH}	High level input threshold voltage (EN)		V_{IN} ≤ 1.5 V	0.8 × V_{IN}			V
V_{IH}	High level input threshold voltage (EN)		V_{IN} > 1.5 V	1.2			V
I_{LKG}	Input leakage current (EN)		EN = GND or VIN		0.01	0.1	µA
V_{OVP}	Output overvoltage protection			4.0		4.5	V

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6.6 Typical Characteristics

Table of Graphs

DESCRIPTION		FIGURE
Maximum output current	vs Input voltage (TPS61260, VOUT = {1.8 V; 2.5 V; 4.0 V})	図 1
	vs Input voltage (TPS61261, VOUT = 3.3 V)	図 2
Efficiency	vs Output current (TPS61260, VOUT = {1.8 V; 2.5 V; 4.0 V})	図 3
	vs Output current (TPS61261, VOUT = 3.3 V)	図 4
	vs Input voltage (TPS61260, VOUT = 1.8 V, IOUT = {10; 20; 50 mA})	図 5
	vs Input voltage (TPS61260, VOUT = 2.5 V, IOUT = {10; 20; 50 mA})	図 6
	vs Input voltage (TPS61260, VOUT = 4.0 V, IOUT = {10; 20; 50; 100 mA})	図 7
	vs Input voltage (TPS61261, VOUT = 3.3V, IOUT = {10; 20; 50 mA})	図 8
Output current	vs Resistance at RI	図 9
Output voltage	vs Output current (TPS61260, VOUT = 1.8 V)	図 10
	vs Output current (TPS61260, VOUT = 2.5 V)	図 11
	vs Output current (TPS61260, VOUT = 4.0 V)	図 12
	vs Output current (TPS61261, VOUT = 3.3 V)	図 13
Output current	vs Output voltage	図 14

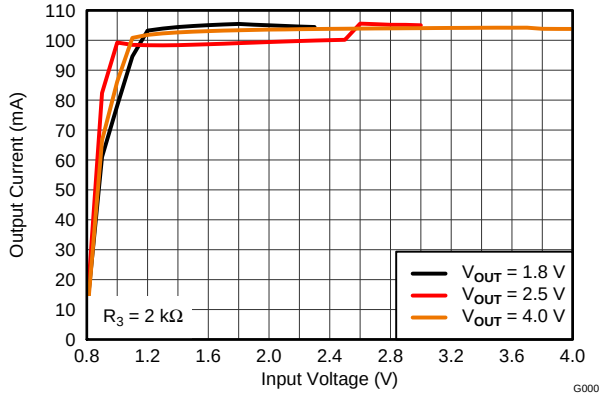


図 1. Maximum Output Current vs Input Voltage

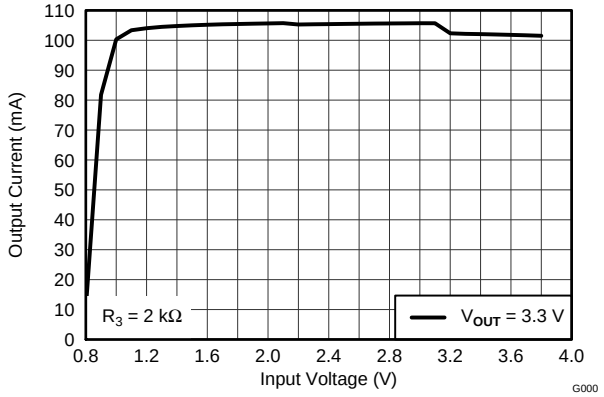


図 2. Maximum Output Current vs Input Voltage

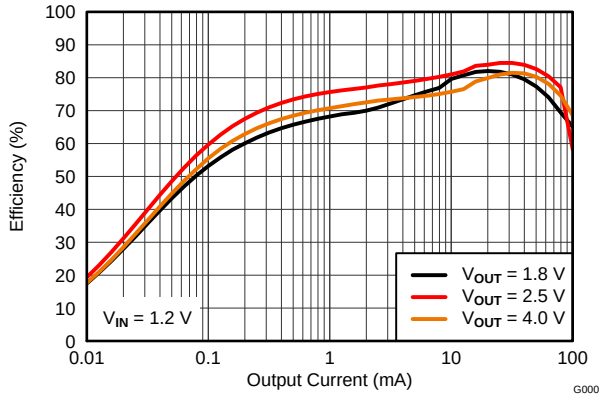


図 3. Efficiency vs Output Current

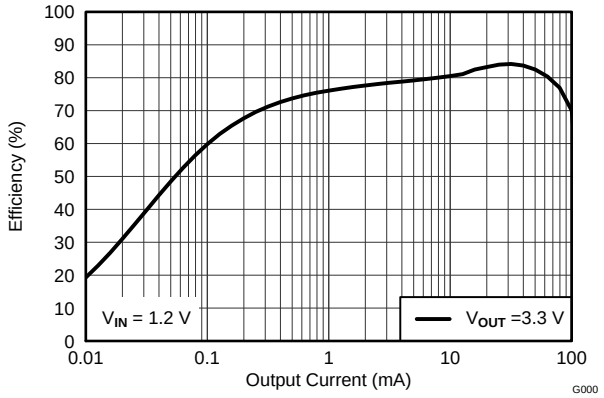


図 4. Efficiency vs Output Current

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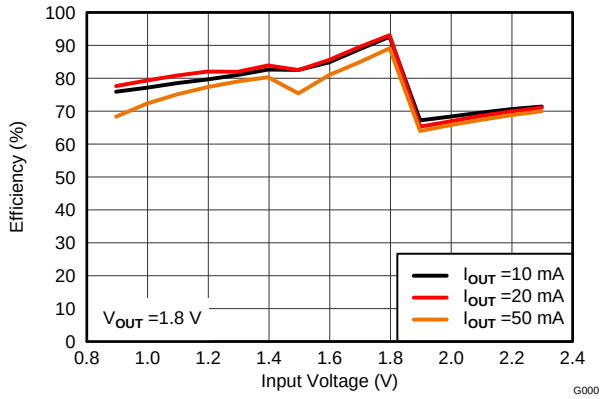


図 5. Efficiency vs Input Voltage

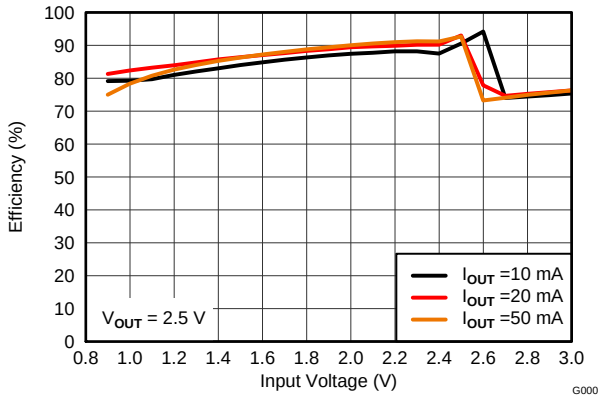


図 6. Efficiency vs Input Voltage

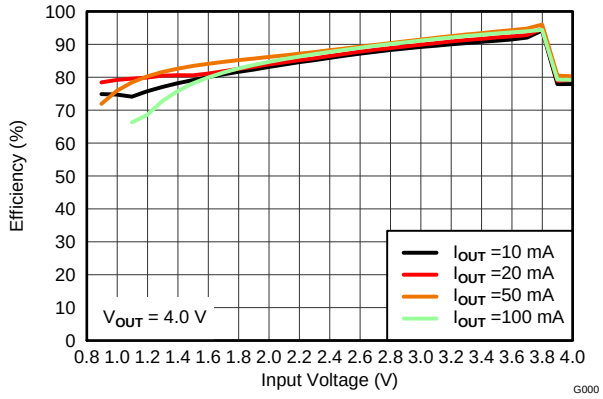


図 7. Efficiency vs Input Voltage

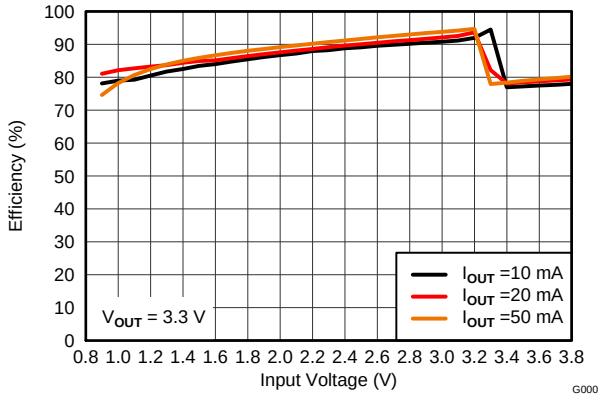


図 8. Efficiency vs Input Voltage

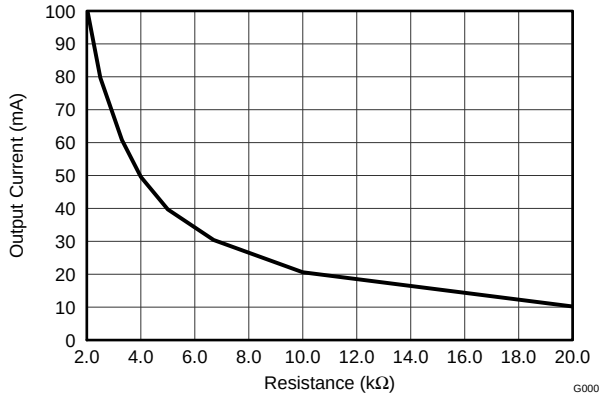


図 9. Output Current vs Resistance at RI

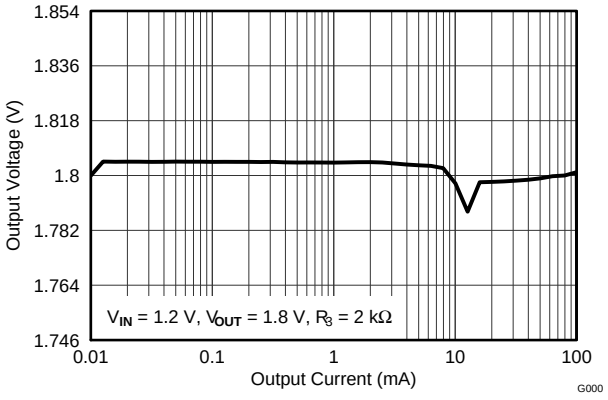


図 10. Output Voltage vs Output Current

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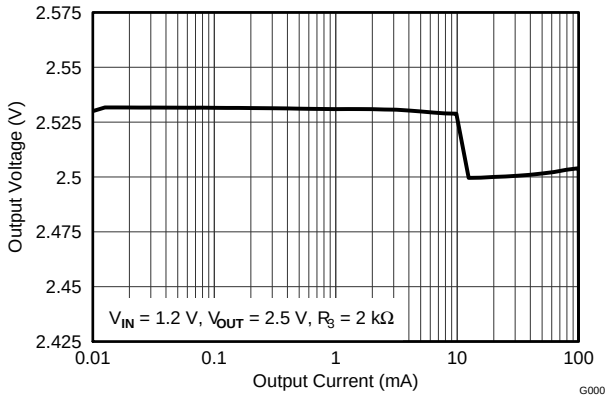


図 11. Output Voltage vs Output Current

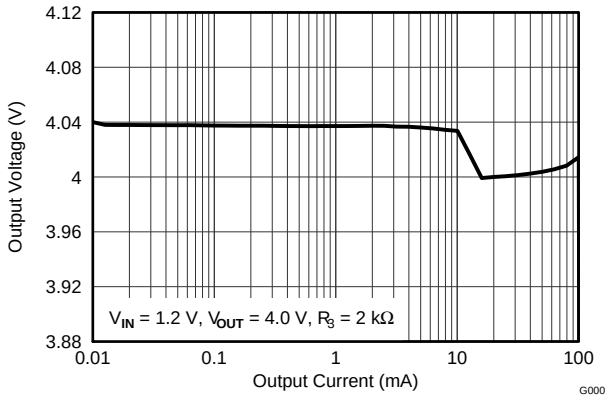


図 12. Output Voltage vs Output Current

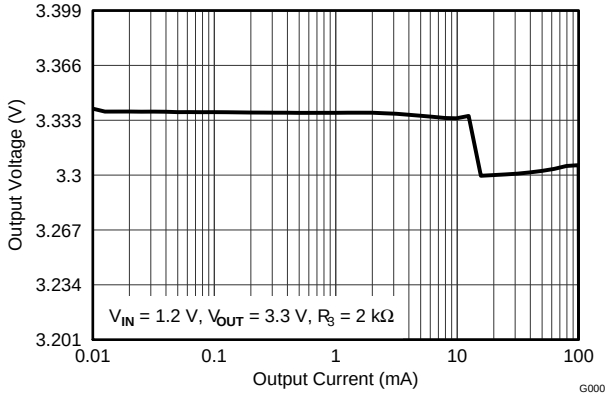


図 13. Output Voltage vs Output Current

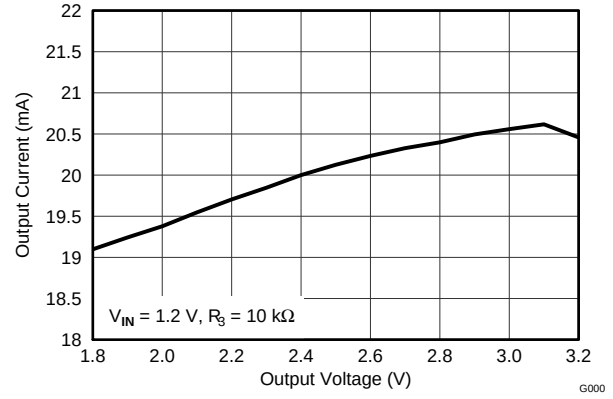


図 14. Output Current vs Output Voltage

7 Parameter Measurement Information

7.1 Schematic and List of Components

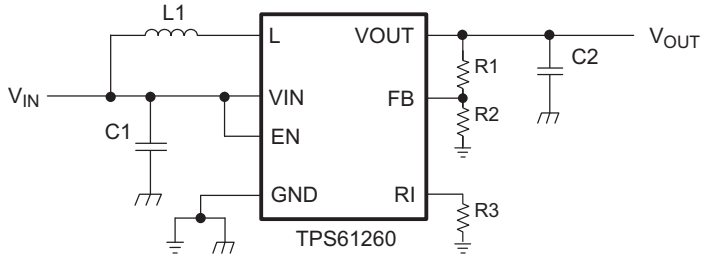


表 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS61260 / 1	Texas Instruments
L1	4.7 µH, 2.5 mm x 2 mm	LQM2HPN4R7MG0, Murata
C1	10 µF 6.3 V, 0603, X5R ceramic	GRM188R60J106KME84D, Murata
C2	10 µF 6.3 V, 0603, X5R ceramic	GRM188R60J106KME84D, Murata
R1	Depending on the output voltage at TPS61260. 0 Ω at TPS61261	

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Schematic and List of Components (continued)

表 1. List of Components (continued)

REFERENCE	DESCRIPTION	MANUFACTURER
R2	Depending on the output voltage at TPS61260. Not used at TPS61261	
R3	Depending on the output current	

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8 Detailed Description

8.1 Overview

The TPS6126x is based on a quasi-fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save Mode to ensure high efficiency over a wide load current range. The TPS6126x is based on a current mode topology. The inductor current is regulated by a fast current regulator loop which is controlled by either a voltage control loop or a reference current. The controller also uses input and output voltage feedforward. Changes of the input and output voltages are monitored and immediately change the duty cycle in the modulator to achieve a fast response to those errors. In addition, the average output current can be programmed as well. An external resistor is used to program the average output current.

8.2 Functional Block Diagrams

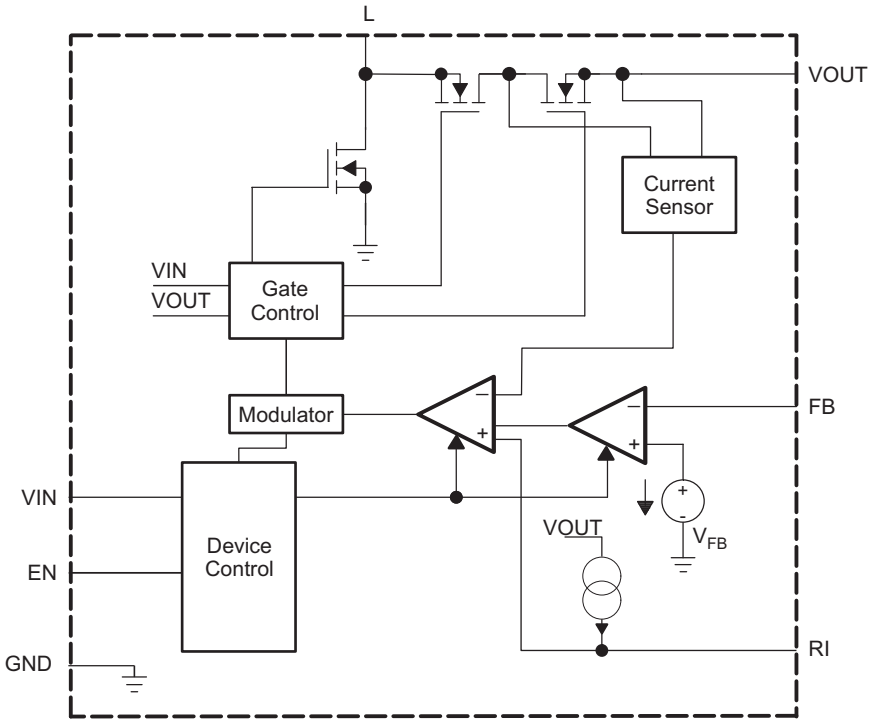


図 15. TPS61260

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Functional Block Diagrams (continued)

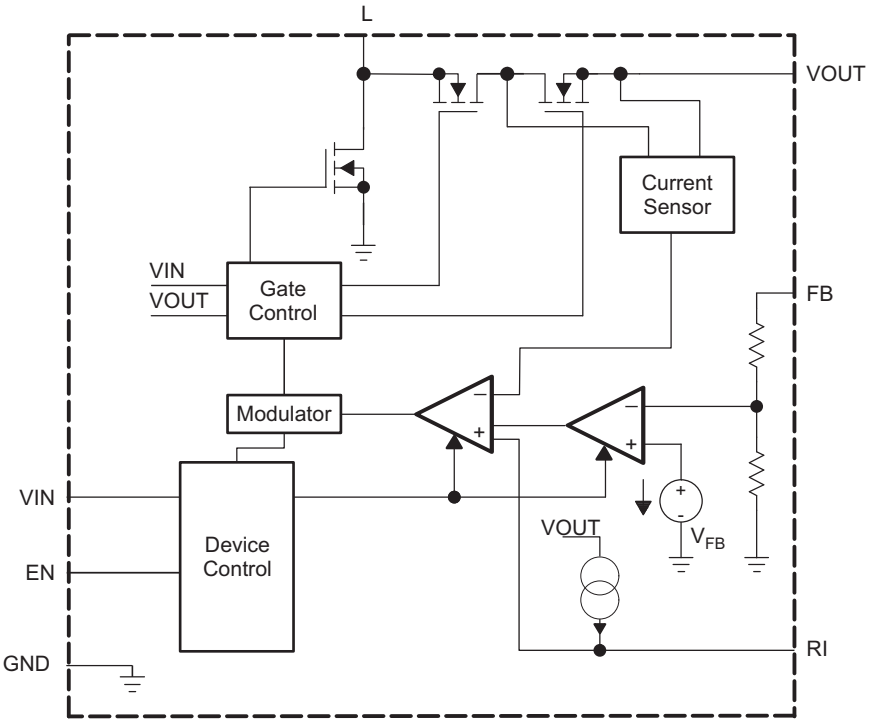


図 16. TPS61261

8.3 Feature Description

8.3.1 Controller Circuit

The controlling circuit of the device is based on a current mode topology. The inductor current is regulated by a fast current regulator loop which is controlled by either a voltage control loop or a reference current. The controller also uses input and output voltage feedforward. Changes of the input and output voltages are monitored and immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. For the adjustable output voltage version, a resistive voltage divider must be connected to that pin. For the fixed output voltage version, the FB pin must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage. The reference current for average output current control is programmed with a resistor connected between the RI pin and GND.

The programming of the average output current also affects the maximum switch current in the main switch which basically is the input current. The lower the average output current is programmed, the lower the maximum input current. Now, maximum input power is controlled as well as the maximum peak current to achieve safe and stable operation under all possible conditions. Smaller inductors with lower saturation current ratings can be used, when lower average output currents are programmed.

8.3.2 Synchronous Boost Operation

The device uses 3 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. Using 2 rectifying switches also enables the device to control the output voltage and current during startup conditions when the input voltage is higher than the output voltage. During startup, the rectifying switch works in a linear mode until the output voltage is near the input voltage. Once in regulation, operating with the input voltage greater than the output voltage may cause either the output voltage or current to exceed its regulation value. Although this operating point is not recommended, the device will not be damaged by this as long as absolute maximum ratings are not violated.

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Feature Description (continued)

As opposed to a standard boost converter, the implemented 3 switch topology enables the output to be disconnected from the input during device shutdown when disabled. Current does not flow from output to input or from input to output.

8.3.3 Power Save Mode

At normal load conditions with continuous inductor current, the device operates at a quasi fixed frequency. If the load gets lower, the inductor current decreases and becomes discontinuous. If this happens and the load is further decreased, the device lowers the switching frequency and turns off parts of the control to minimize internal power consumption. The output voltage is controlled by a low power comparator at a level about 1% higher than the nominal output voltage. If the output voltage reaches the nominal value or drops below it, device control is turned on again to handle the new load condition. The boundary between power save mode and PWM mode is when the inductor current becomes discontinuous.

Accurate average output current regulation requires continuous inductor current. This means that there is no power save mode during current regulation.

8.3.4 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that output voltage can drop below input voltage during shutdown.

8.3.5 Softstart and Short Circuit Protection

During startup of the converter, duty cycle and peak current are limited in order to avoid high peak currents flowing from the input. After being enabled, the device starts operating. Until the output voltage reaches about 0.4 V, the average output current ramps up from zero to the programmed value, as the output voltage increases. As soon as the output current has reached the programmed value, it stays regulated at that value until the load conditions demand less current. This typically happens when the output capacitor is charged and the output voltage is regulated.

During startup, the device can seamlessly change modes of operation. When the input voltage is higher than the output voltage, the device operates in a linear mode using the rectifying switches for control. If the input voltage is lower than the output voltage it operates in a standard boost conversion mode. Boost conversion is non-synchronous when the output voltage is below approximately 1.8 V and it is synchronous if the output voltage is higher than approximately 1.8 V.

At short circuit conditions at the output, the output current is limited to the programmed average current. If the short at the output causes the output voltage to drop below 0.4 V, the average current decreases approximately linearly with the output voltage down to zero.

The devices can monotonically start into a pre-bias on the output.

8.4 Device Functional Modes

8.4.1 Undervoltage Lockout

An undervoltage lockout function prevents device startup if the supply voltage on VIN is lower than the undervoltage lockout threshold defined in the *Electrical Characteristics*. When in operation, the device automatically shuts down the power stage if the voltage on VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

8.4.2 Output Overvoltage Protection

If, for any reason, the output voltage of the device (as measured at the VOUT pin) exceeds its maximum recommended value, the device stops operating. It continues operating as soon as the output voltage has dropped below this threshold.

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8.5 Programming

8.5.1 Programming the Output Voltage

Within the TPS6126x family, there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. For the adjustable output voltage version, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between the VOUT, FB, and GND pins. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 4.0 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μA, and the voltage across the resistor between the FB and GND pins, R2, is typically 500 mV. Based on these two values, the recommended value for R_2 should be lower than 500 kΩ, in order to set the divider current at 1 μA or higher. It is also recommended to keep the total value for the resistor divider, **R1 + R2**, in the range of 1 MΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using 式 1:

$$R1 = R2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

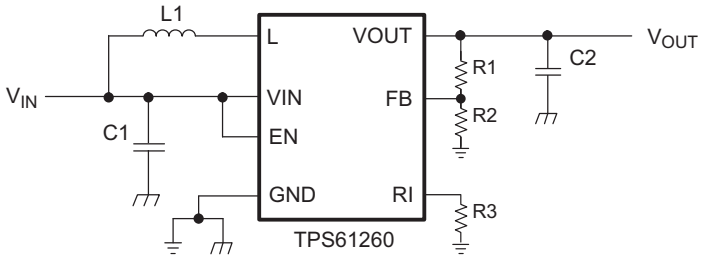


図 17. Typical Application Circuit for Adjustable Output Voltage Option

8.5.2 Programming the Output Current

The devices of the TPS6126x family also support average output current regulation. An external resistor is used to program the average output current. The resistor must be connected between the RI and GND pins. When the average output current is regulated properly, the typical value of the voltage at the RI pin is 400 mV. The maximum recommended value for the regulated average output current is 100 mA. The value of the resistor R3 should be between 2 kΩ and 20 kΩ. It can be calculated, depending on the needed average output current (I_{OUT}), using 式 2:

$$R3 = \frac{200V}{I_{OUT}} \quad (2)$$

Accurate regulation of the average output current only is possible if the inductor current is continuous. Please check the *Inductor Selection* section to calculate the required parameters for selecting an appropriate inductor.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are designed to operate from an input voltage supply range between 1.2 V (Vin falling UVLO is 0.8 V) and 4.0 V with a maximum output current of 100 mA. The devices operate in PWM mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode the TPS61260 converter operates with the nominal switching frequency of 2.5 MHz which provides a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

9.2 Typical Applications

9.2.1 TPS61260 3.3-V Output Application

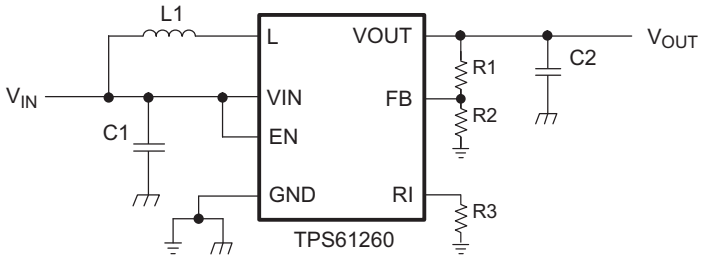


図 18. TPS61260 Typical Application Circuit

9.2.1.1 Design Requirements

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 4.0 V
Output voltage	3.3 V
Input ripple voltage	±200 mV
Output ripple voltage	±3% V_{OUT}
Output current rating	100 mA
Operating frequency	2.5 MHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

To properly configure the TPS6126x devices, an inductor must be connected between the VIN pin and the L pin. 式 3 is used to estimate the minimum inductance value for accurate average output current regulation; the inductor current should be continuous.

$$L_{MIN} = \frac{V^2_{IN} \cdot (V_{OUT} - V_{IN})}{V^2_{OUT} \cdot I_{OUT}} \cdot 0.2\ (\mu H) \quad (3)$$

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In 式 3, the minimum inductance value required for accurate average output current regulation is calculated. V_{IN} is the input voltage. For typical applications which require voltage regulation, the recommended inductor value is 4.7 µH. Applications with higher inductance values have lower light load efficiency. The recommended range for the inductor value is from 2.2 µH up to 22 µH. The current rating required for this inductor is I_{LIM} and depends on the programmed output current I_{OUT}. Please refer to the *Electrical Characteristics*. 表 3 contains a list of inductors recommended for the TPS6126x:

表 3. List of Inductors

VENDOR	INDUCTOR SERIES
Murata	LQM2HP_G0
Toko	DFE252012C
Hitachi Metals	KSLI-252010AG

9.2.1.2.2 Capacitor Selection

9.2.1.2.2.1 Input Capacitor

At least a 4.7-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

9.2.1.2.2.2 Output Capacitor

For the output capacitor, use of a small X5R or X7R ceramic capacitor placed as close as possible to the VOUT and GND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

The output capacitor should be at least 2.2 µF. There are no additional requirements regarding minimum ESR. There is also no theoretical upper limit for the output capacitance value. The device has been tested with capacitors up to 100 µF. In general, larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients. To improve control performance, especially when using high output capacitance values, a feedforward capacitor in parallel to R1 is recommended. The value should be in the range of the value calculated in 式 4:

$$C_{ff} = 0.3 \cdot \Omega \cdot \frac{C2}{R2} \tag{4}$$

9.2.1.3 TPS61260 3.3-V Output Application Performance Plots

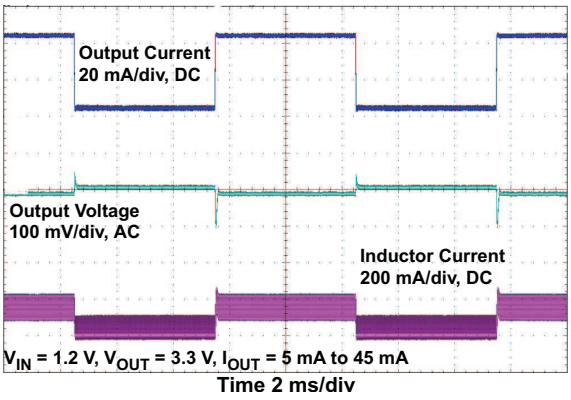


図 19. Load Transient Response

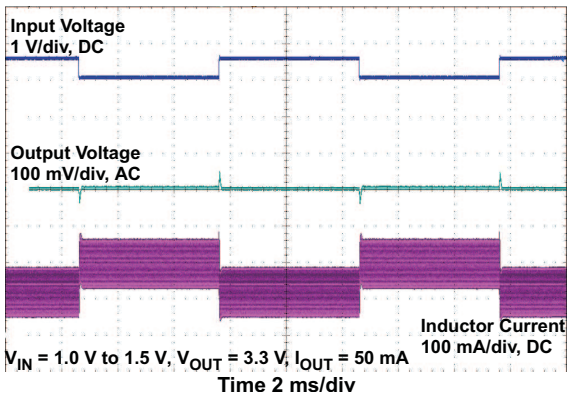


図 20. Line Transient Response

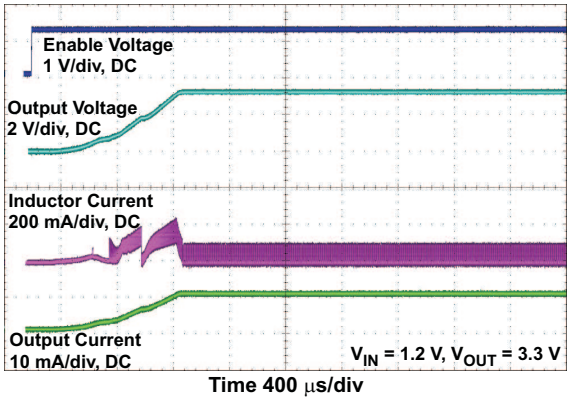


図 21. Startup After Enable

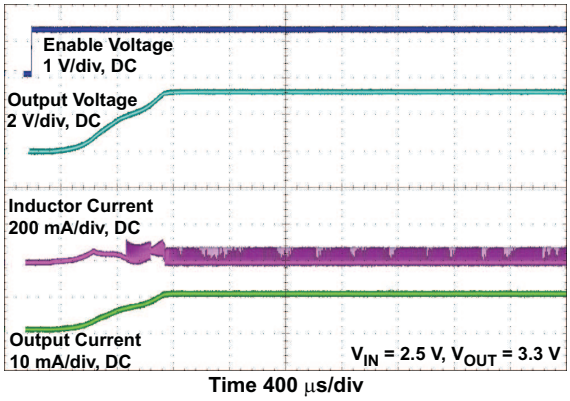


図 22. Startup After Enable

9.2.2 TPS61261 Application as LED Driver

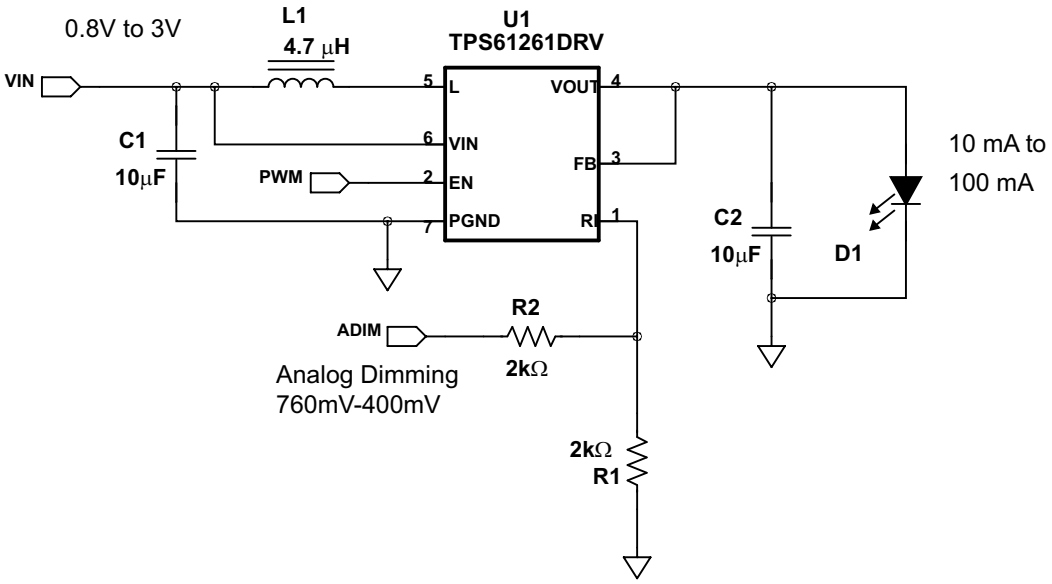


図 23. TPS61260 LED Driver Application Circuit

9.2.2.1 Design Requirements

表 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3 V
Output current rating	10 mA -100 mA
Operating frequency	2.5 MHz

9.2.2.2 Detailed Design Procedure

図 23 shows the TPS61261 configured to drive an LED with analog and/or PWM dimming. This circuit does not require an external current sensing resistor and so provides high efficiency, as shown in 図 24. This design is available as the TPS61261EVM-208.

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9.2.2.3 TPS61261 Application as LED Driver Performance Plots

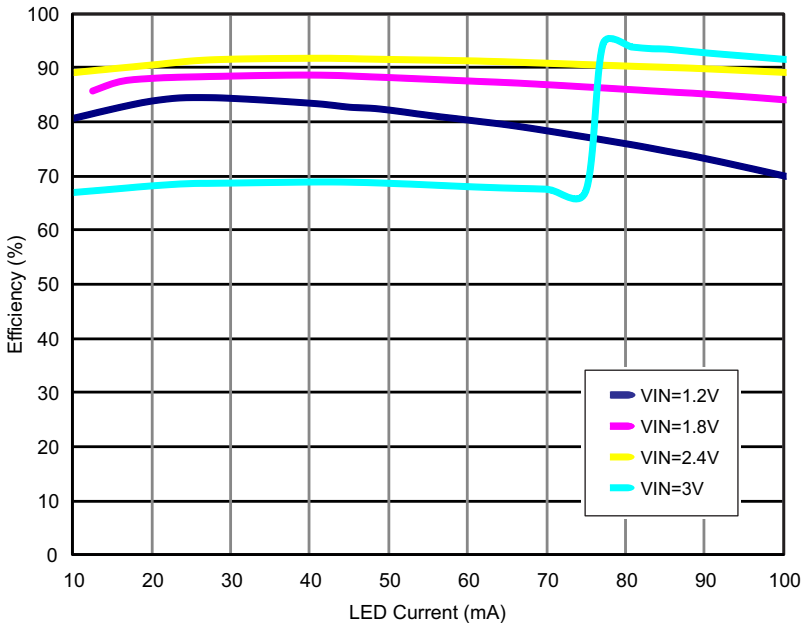


図 24. LED Driver Efficiency

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.2 V and 4.0 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 μF is a typical choice.

11 Layout

11.1 Layout Guidelines

- For all switching power supplies, layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pin of the IC.
- The feedback divider should be placed as close as possible to the control ground connection. To lay out the control ground, short traces are recommended as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. See 図 25 for the recommended layout.

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11.2 Layout Example

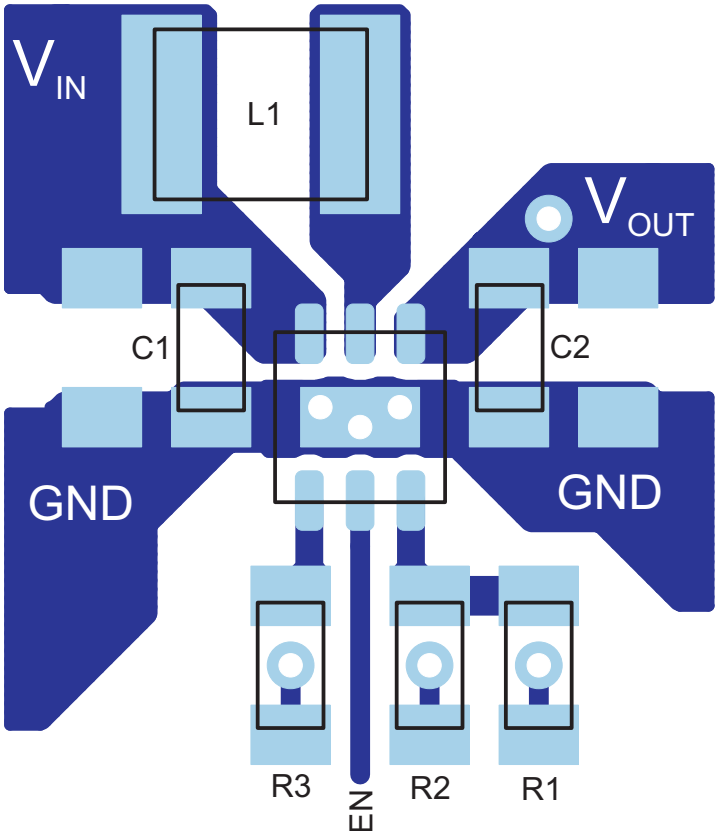


図 25. PCB Layout Suggestion

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table, please check the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report* (SZZA017) and the *Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953).

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.2 ドキュメントのサポート

12.2.1 関連資料

『TPS61261EVM-208評価モジュール・ユーザー・ガイド』(SLVU851)

『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』アプリケーション・レポート(SZZA017)

『半導体およびICパッケージの熱指標』アプリケーション・レポート(SPRA953)

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS61260	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS61261	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 商標

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12.5 静電気放電に関する注意事項



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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61260DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD
TPS61260DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD
TPS61260DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD
TPS61260DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD
TPS61260DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD
TPS61260DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD
TPS61261DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWE
TPS61261DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWE
TPS61261DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWE
TPS61261DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWE
TPS61261DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

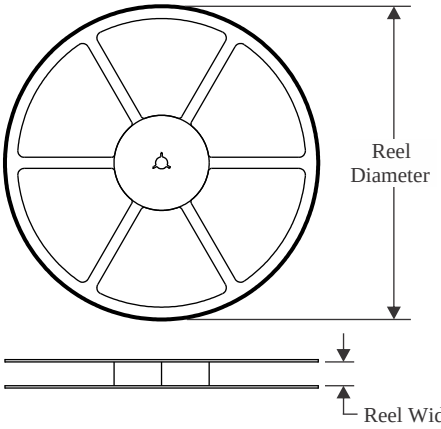
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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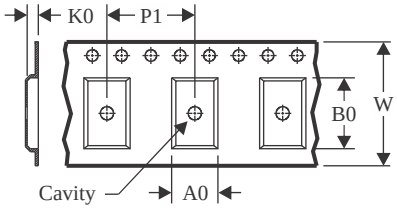
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

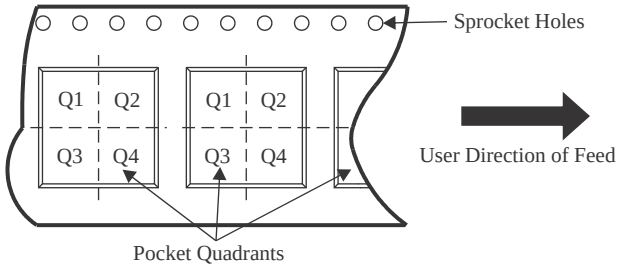


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

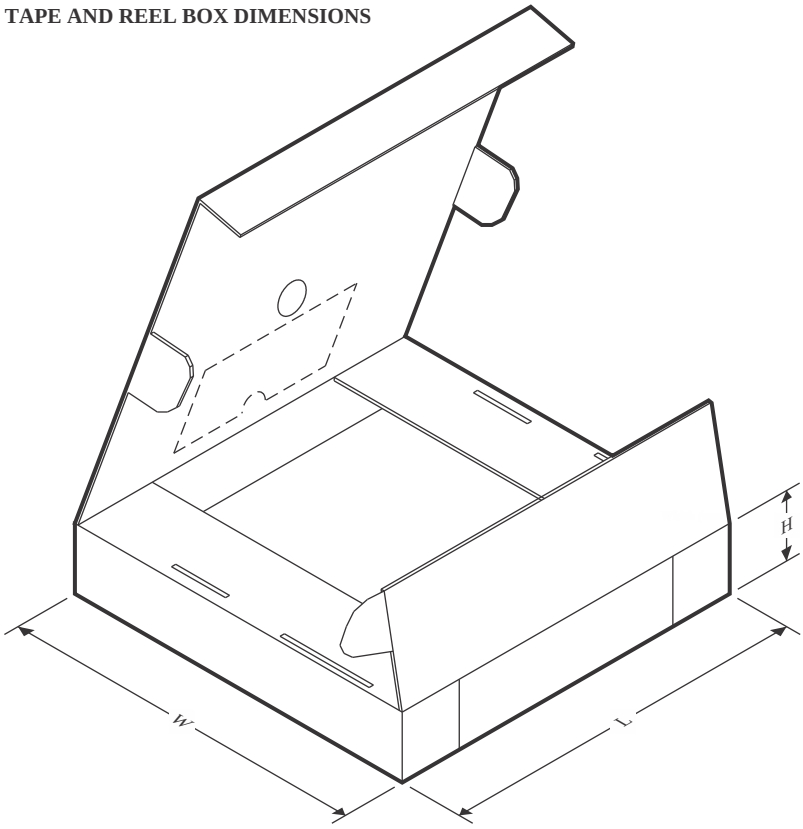
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61260DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61260DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61260DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61260DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61261DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61261DRVT	WSON	DRV	6	250	180.0	12.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

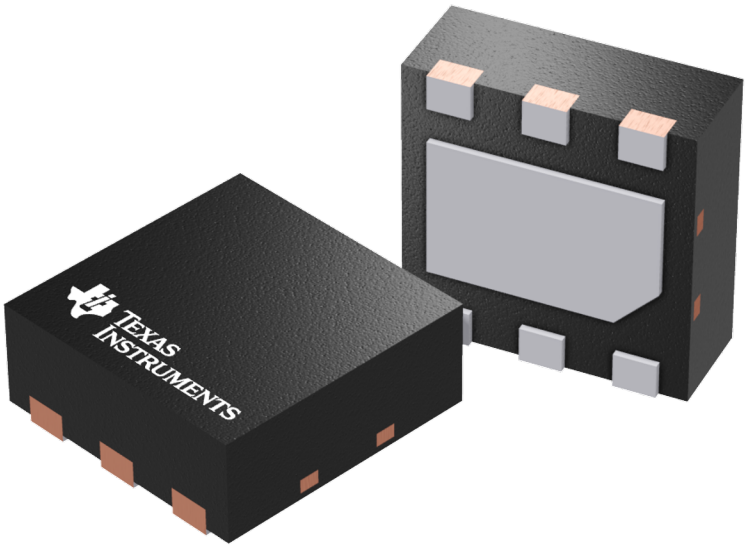


*All dimensions are nominal

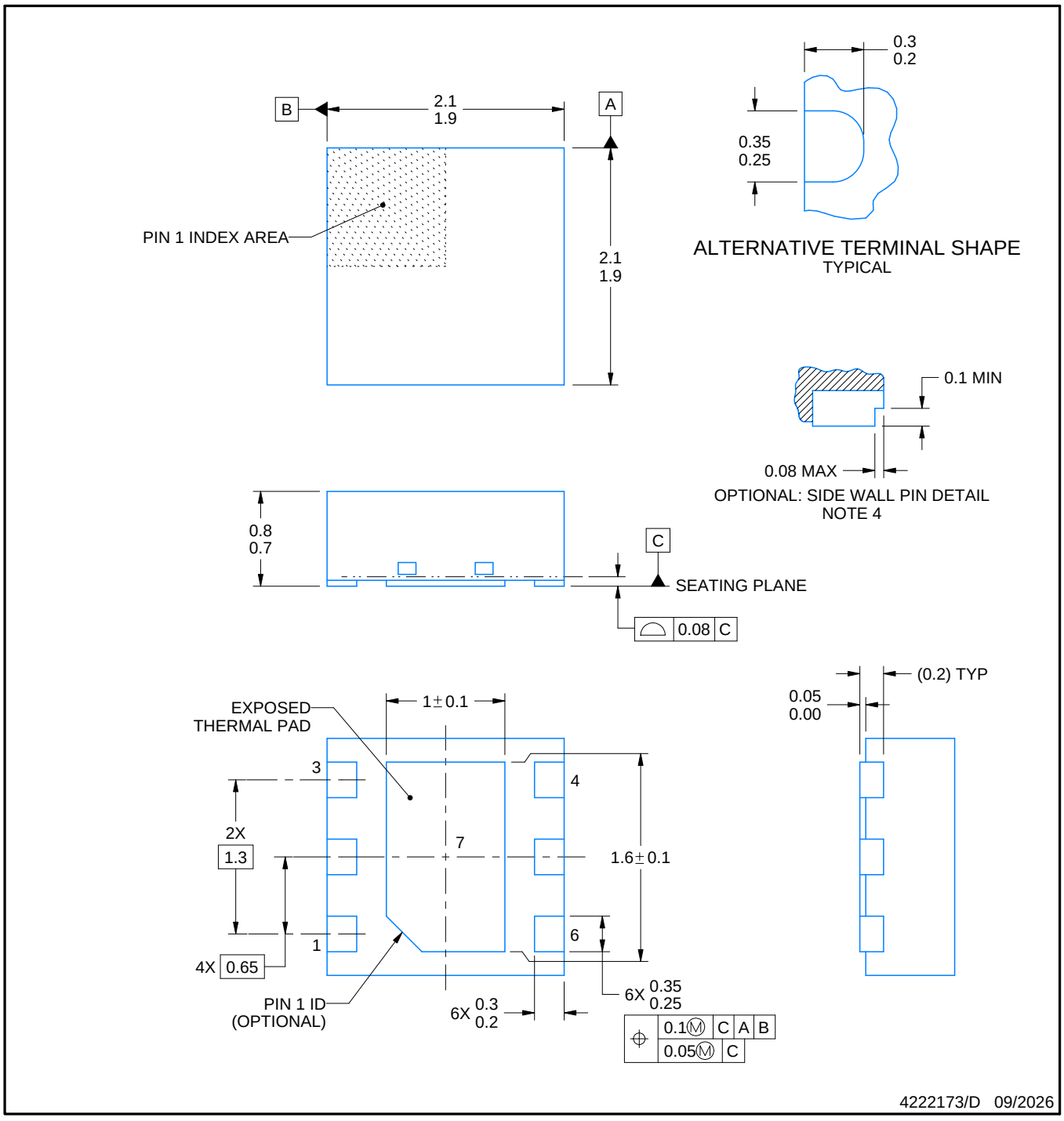
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61260DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS61260DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS61260DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS61260DRVT	WSON	DRV	6	250	213.0	191.0	35.0
TPS61261DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS61261DRVT	WSON	DRV	6	250	213.0	191.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

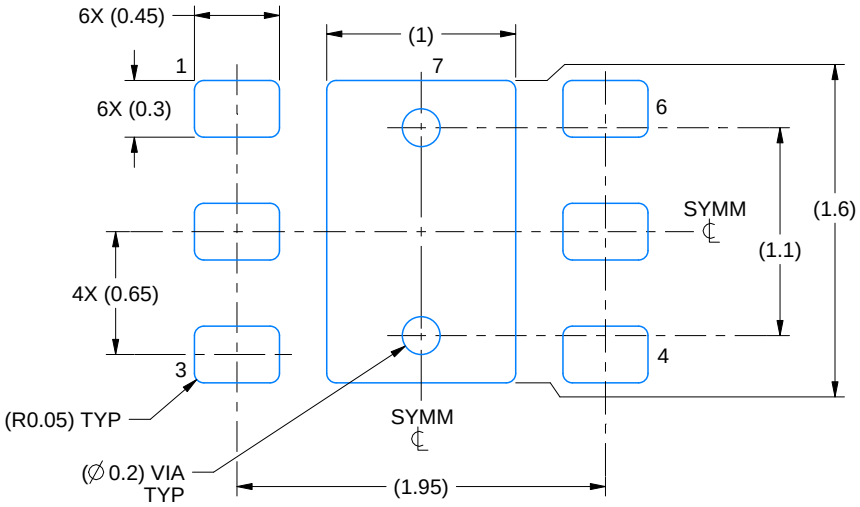


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

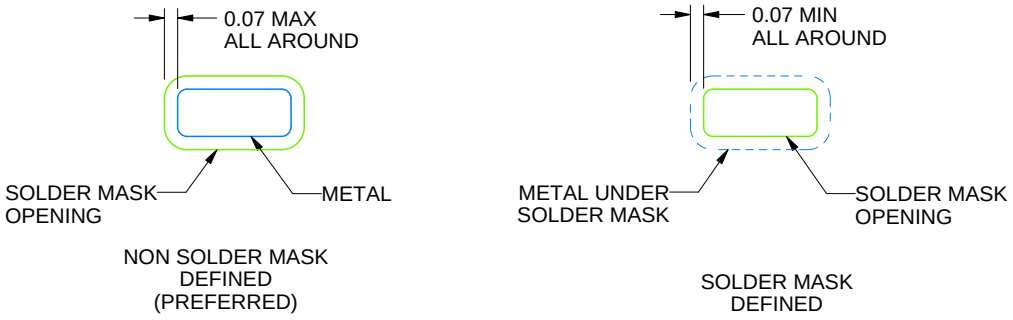


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

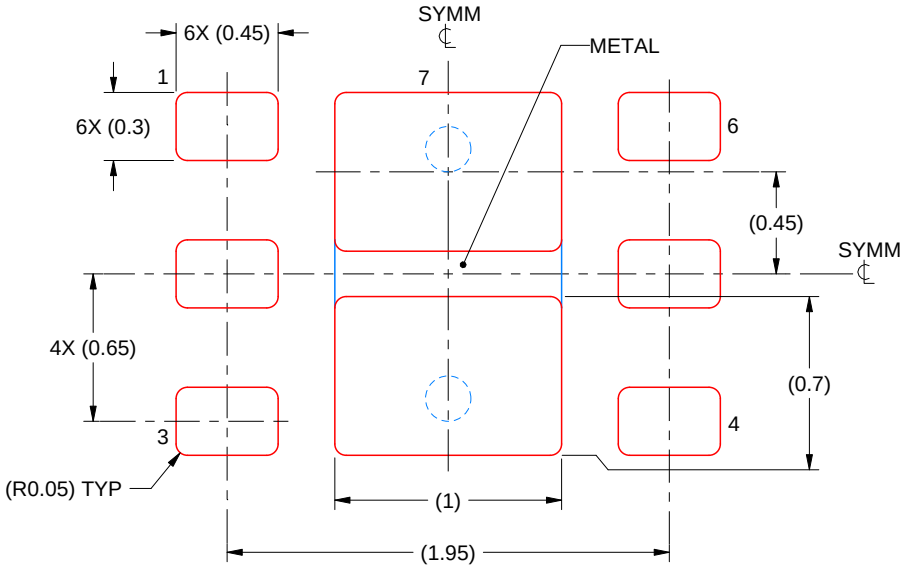


SOLDER MASK DETAILS

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NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月