TEXAS INSTRUMENTS
TPS61379-Q1
JAJSLN3B – MARCH 2021 – REVISED OCTOBER 2021

TPS61379-Q1 負荷切断機能搭載、25µA 静止電流、同期整流昇圧コンバータ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 1:–40℃～125℃の動作時周囲温度範囲
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 柔軟な入出力動作範囲
  - 入力電圧範囲:2.3V～14V
  - プログラム可能な出力電圧範囲:4.0V～18.5V
  - 5V、5.25V、5.5V の固定出力オプション
  - 固定 2A ピーク電流制限
- AM 帯域の干渉とクロストークを回避
  - 動的にプログラム可能なスイッチング周波数:200kHz～2.2MHz
  - スペクトラム拡散周波数変調
  - 選択可能なクロック同期
- スペースの制約が厳しいアプリケーションのためにソリューション・サイズを最小化
  - 内蔵 LS/HS/ISO FET:$R_{DS(ON)}$ 50mΩ/50mΩ/100mΩ
  - 小さい L-C で最大 2.2MHz をサポート
- 軽負荷とアイドル状態の消費電流を最小化
  - VIN ピンに流れ込む静止電流:25µA
  - VIN ピンに流れ込むシャットダウン電流:0.5µA
  - 自動 PFM モードと強制 PWM モードを選択可能
  - シャットダウンまたはフォルト状態時の真の負荷接続解除
- 保護機能内蔵
  - VIN が VOUT に近づいても動作可能
  - 入力低電圧誤動作防止と出力過電圧保護
  - ヒカップ出力短絡保護機能
  - パワー・グッド・インジケータ
  - 165℃のサーマル・シャットダウン保護
- 3.3V から 9V への変換で、0.25A 未満の負荷において 90% 以上の効率

2 アプリケーション

- 先進運転支援システム (ADAS)
- 車載インフォテインメントおよびクラスタ
- ボディ・エレクトロニクス / 照明
- 緊急通話 (eCall)

3 概要

TPS61379-Q1 は負荷接続解除機能を搭載したフル統合型同期整流昇圧コンバータです。入力電圧は 2.3V～14V、最大出力電圧は 18.5V です。スイッチング電流制限は 2A (標準値) です。V_{IN} から 25µA の静止電流を消費します。

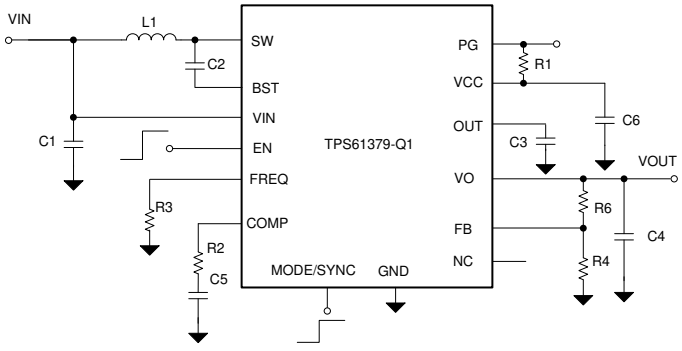
TPS61379-Q1 は、スイッチング周波数を 200kHz～2.2MHz に設定できるピーク電流モード制御を採用しています。本デバイスは、中負荷から重負荷では固定周波数 PWM で動作します。軽負荷時には、効率とノイズ耐性を両立させるため、MODE ピンを設定することで 2 つのモード (自動 PFM モード、強制 PWM モード) のどちらかを選択できます。スイッチング周波数は、外部クロックに同期させることができます。FPWM モードでの EMI を低減するため、TPS61379-Q1 は内部クロックのスペクトラム拡散を採用しています。また、内部ソフト・スタート時間によって突入電流を制限することもできます。

TPS61379-Q1 には各種の固定出力電圧バージョンがそろっているため、外付け帰還抵抗を省略できます。より広い V_{OUT}/V_{IN} 範囲で安定性と過渡応答を最適化できるように、本デバイスは外部ループ補償をサポートしています。出力短絡保護、出力過電圧保護、サーマル・シャットダウン保護などの堅牢な保護機能も内蔵しています。TPS61379-Q1 は、ウェッタブル・フランク付きの 3mm × 3mm 16 ピン QFN パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS61379-Q1	VQFN-16	3.0mm × 3.0mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

Changes from Revision A (June 2021) to Revision B (October 2021)	Page
• Replaced the operating ambient temperature with the operating junction temperature and added table note in セクション 7.3	5
• Updated セクション 8.3.12	13
• Updated 図 9-2	19

Changes from Revision * (March 2021) to Revision A (June 2021)	Page
• Updated resistor from FB to GND values	3
• Updated voltage reference specifications	6
• Updated セクション 9.2.2.1	15

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE (V)	RESISTOR FROM FB TO GND (R_{FB_LOW})	SPREAD SPECTRUM
TPS61379-Q1	5	0Ω≤ R_{FB_LOW} ≤ 2.4 kΩ	Enable
	5.25	3.6kΩ ≤ R_{FB_LOW} ≤ 4.8 kΩ	
	5.5	7.2kΩ ≤ R_{FB_LOW} ≤ 9.6kΩ	
	Adjustable	14.4kΩ≤ R_{FB_LOW} ≤ 100kΩ	

6 Pin Configuration and Functions

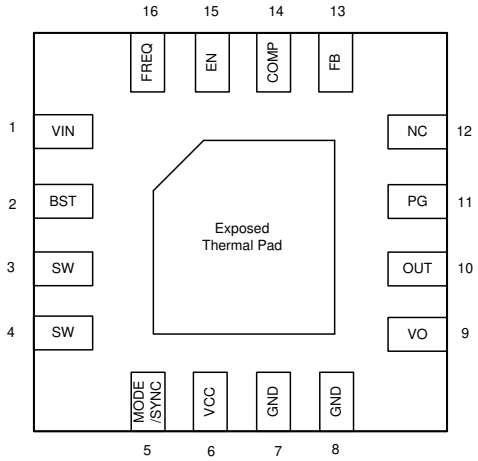


図 6-1. 16-Pin WQFN RTE Package (Transparent Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	IC power supply input
BST	2	I	Power supply for high-side N-MOSFET gate drivers. A capacitor must be connected between this pin and SW pin.
SW	3, 4	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side FET and the source of the high-side FET.
MODE/SYNC	5	I	Mode selection pin. MODE = high, forced PWM mode. MODE = low or floating, auto PFM mode. This pin can also be used to synchronize the external clock. Refer to 表 8-1 for details.
VCC	6	O	Output of internal regulator. A ceramic capacitor with more than 1 µF must be connected between this pin and GND.
GND	7, 8	PWR	Power ground of the IC. It is connected to the source of the low-side FET.
VO	9	PWR	Output of the isolation FET. Connect load to this pin to achieve input/output isolation.
OUT	10	PWR	Output of the drain of the HS FET. Connect this pin as the output can disable the load disconnect/short protection feature (or short this pin with VO pin).
PG	11	O	Power good indicator, open-drain output
NC	12	I	No connection pin
FB	13	I	Feedback pin. Use a resistor divider to set the desired output voltage. Refer to *セクション 9.2.2.1* for details.
COMP	14	I	Output of the internal transconductance error amplifier. An external RC network is connected to this pin to optimize the loop stability and response time.
EN	15	I	Enable logic input
FREQ	16	I	Frequency setting pin. Connect a resistor between this pin and GND pin to set the desired frequency.
Thermal Pad	-	-	The thermal pad must be connected to power ground plane for good power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN	-0.3	16	V
Voltage range at terminals (2)	VO, SW, OUT	–0.3	23	V
	BST	–0.3	SW + 6	V
	MODE/SYNC, FB, FREQ, ILIM, VCC, COMP, EN	–0.3	6	V
	PG	-0.3	20	V
T_J (3)	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(2)		±2000	V
		Charged-device model (CDM), per AEC Q100-011(3)	All pins	±500	
			Corner pins (1, 4, 5, 8, 9, 12, 13, and16)	±750	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.3		14	V
V_{OUT}	Outputvoltage	4		18.5	V
T_J	Operating junction temperature(1)	–40		150	°C

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC(1)		TPS61379-Q1 RTE 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.5	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS61379-Q1 RTE 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = -40 to 125°C, L = 1 µH, V_{IN} = 3.3 V and V_{OUT} = 9 V (VO pin). Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.3		14	V
V_{IN_UVLO}	VIN under voltage lockout threshold	V_{IN} rising		2.2	2.3	V
		V_{IN} falling		2.04	2.2	V
V_{IN_HYS}	VIN UVLO hysteresis			160		mV
V_{CC_UVLO}	VCC UVLO threshold	V_{CC} rising		2.2		V
V_{CC_HYS}	VCC UVLO hysteresis	V_{CC} hysteresis		150		mV
V_{CC}	VCC regulation	I_{VCC} = 6 mA, V_{OUT} = 9V		4.8		V
I_Q	Quiescent current into V_{IN} pin	IC enabled, no load, V_{IN} = 3.3 V, V_{OUT} = 18.5 V, V_{FB} = V_{REF} + 0.1 V		25	35	µA
I_Q	Quiescent current into OUT pin	IC enabled, no load, V_{IN} = 3.3 V, V_{OUT} = 18.5 V, V_{FB} = V_{REF} + 0.1 V		10	20	µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 14 V, EN = GND		0.6	5	µA
I_{SW_LKG}	Leakage current into SW	IC disabled, V_{IN} = OUT = SW = 14 V			5	µA
I_{VO_LKG}	Reverse leakage current into VO	IC disabled, OUT= VO = 5 V, SW = 0			5	µA
OUTPUT VOLTAGE						
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 3.3 V, V_{OUT} rising	19.3	20	20.5	V
V_{OVP_HYS}	Output over-voltage protection hysteresis	V_{IN} = 3.3 V, OVP threshold		0.5		V
VOLTAGE REFERENCE						
V_{REF}	Reference Voltage at FB pin	T_J = -40 to 125°C, R_{FB} = 16.0 kΩ	0.788	0.800	0.812	V
V_{OUT_5V}		T_J = -40 to 125°C, R_{FB} = 2.0 kΩ	4.85	5.00	5.15	V
$V_{OUT\_5.25V}$		T_J = -40 to 125°C, R_{FB} = 4.0 kΩ	5.10	5.25	5.35	V
$V_{OUT\_5.5V}$		T_J = -40 to 125°C, R_{FB} = 8.0 kΩ	5.35	5.50	5.65	V
I_{FB_LKG}	Leakage current into FB pin				50	nA
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{CC} = 4.85 V		50		mΩ
$R_{DS(on)}$	High-side MOSFET on resistance	V_{CC} = 4.85 V		50		mΩ
$R_{DS(on)}$	Isolation MOSFET on resistance	V_{CC} = 4.85 V		100		mΩ
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit Auto PFM	Duty cycle = 65%	1.58	2	2.25	A
I_{LIM_SW}	Peak switching current limit FPWM	Duty cycle = 65%	1.58	2	2.25	A
SWITCHING FREQUENCY						
Fsw	Switching frequency	R_{FREQ} = 18 kΩ	2050	2200	2400	kHz
Fsw	Switching frequency	R_{FREQ} = 218 kΩ	180	200	230	kHz
D_{max}	Maximum Duty Cycle	R_{FREQ} = 18 kΩ	78			%
t_{ON_min}	Minimal on time			70		ns
F_{DITHER}				10%		Fsw
$F_{pattern}$				0.4%		Fsw
ERROR AMPLIFIER						

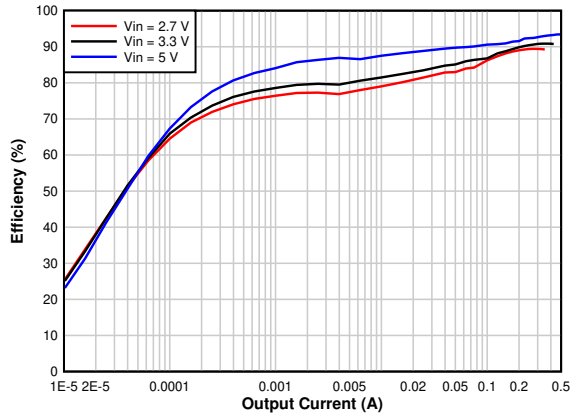
7.5 Electrical Characteristics (continued)

T_J = -40 to 125°C, L = 1 µH, V_{IN} = 3.3 V and V_{OUT} = 9 V (VO pin). Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 0.2V		6		uA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 0.2V		6		uA
V_{CCLPH}	COMP pin high clamp voltage	V_{FB} = V_{REF} - 0.2 V, ILIM = 2 A		1		V
V_{CCLPL}	COMP pin low clamp voltage	V_{FB} = V_{REF} + 0.2 V,		0.6		V
G_{mEA}	Error amplifier trans conductance	V_{COMP} = 1.0 V		70		uS
POWER GOOD						
V_{PG_TH}	PG threhold for rising FB voltage	Reference to V_{REF}		90%		
V_{PG_HYS}	PG hysteresis	Reference to V_{REF}		5%		
I_{PG_SINK}	PG pin sink current capability	V_{PG} = 0.4 V		20		mA
t_{PG_DELAY}	PG delay time		2.5	3.4	4.3	ms
DOWN MODE						
t_{EN_DELAY}	Delay time between EN high and device working			0.4		ms
t_{SS}	Softstart time			2.5		ms
t_{HCP_ON}	Hiccup on time			1.8		ms
t_{HCP_OFF}	Hiccup off time			67		ms
SYNC TIMING						
f_{SYNC_MIN}				200		kHz
f_{SYNC_MAX}				2200		kHz
EN/SYNC LOGIC						
VI_H	EN, MODE/SYNC pins Logic high threshold				1.2	V
VI_L	EN, MODE/SYNC pins Logic Low threshold		0.4			V
R_{DOWN}	EN, MODE/SYNC pins internal pull down resistor			800		kΩ
THERMAL SHUTDOWN						
t_{SD_R}	Thermal shutdown rising threshold	TJ rising		165		°C
t_{SD_F}	Thermal shutdown falling threshold	TJ falling		145		°C

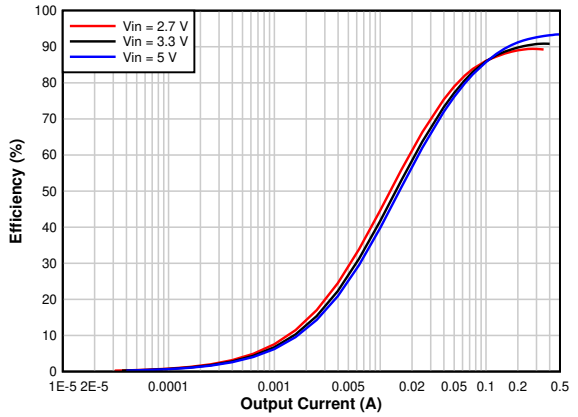
7.6 Typical Characteristics

V_{IN} = 3.3 V, V_{OUT} = 9 V (VO pin), T_A = 25°C, Fsw = 2.2 MHz, unless otherwise noted.



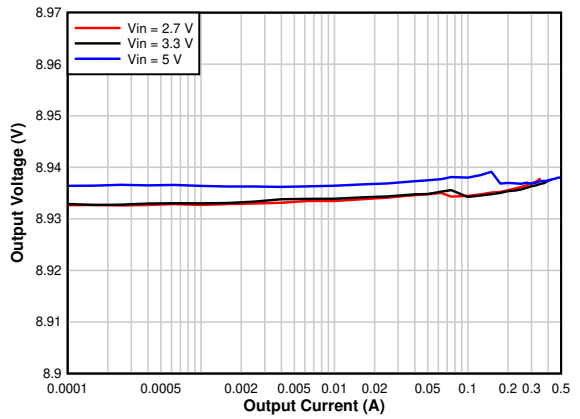
VOUT = 9 V Auto PFM Fsw = 2.2 MHz

図 7-1. 9 V_{OUT} Efficiency vs Output Current



VOUT = 9 V FPWM Fsw = 2.2 MHz

図 7-2. 9 V_{OUT} Efficiency vs Output Current



VOUT = 9 V Auto PFM Fsw = 2.2 MHz

図 7-3. 9 V_{OUT} Regulation vs Output Current

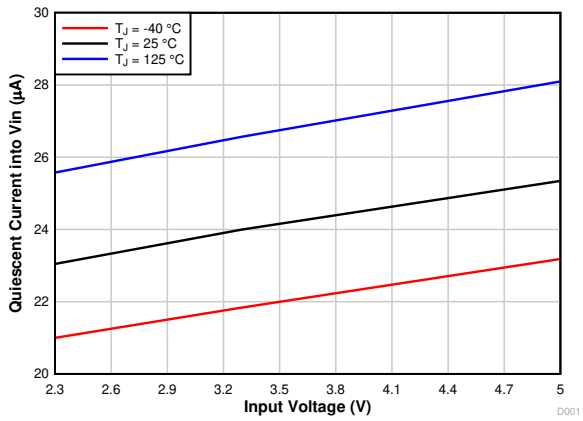


図 7-4. Quiescent Current into V_{IN} vs Input Voltage

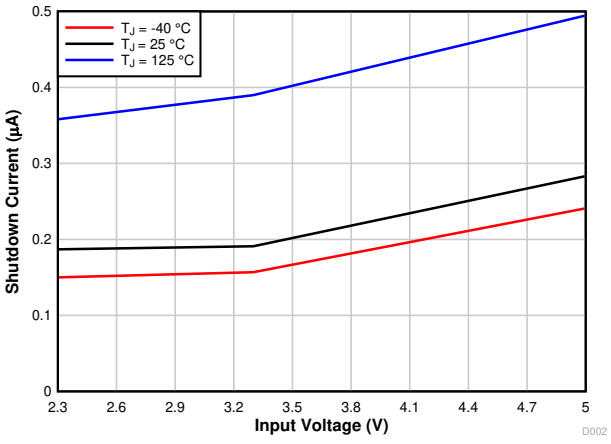


図 7-5. Shutdown Current vs Input Voltage

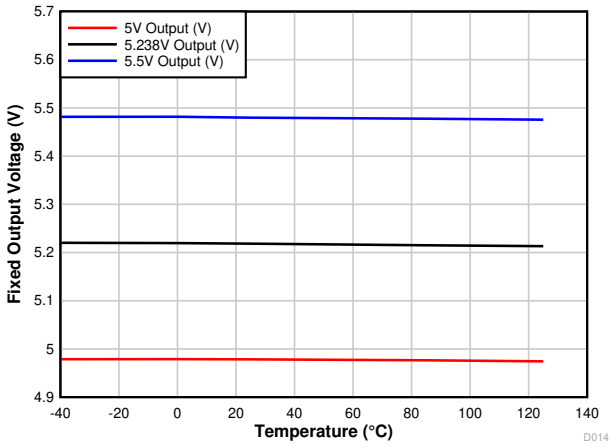


図 7-6. Fixed Output Voltage vs Temperature

7.6 Typical Characteristics (continued)

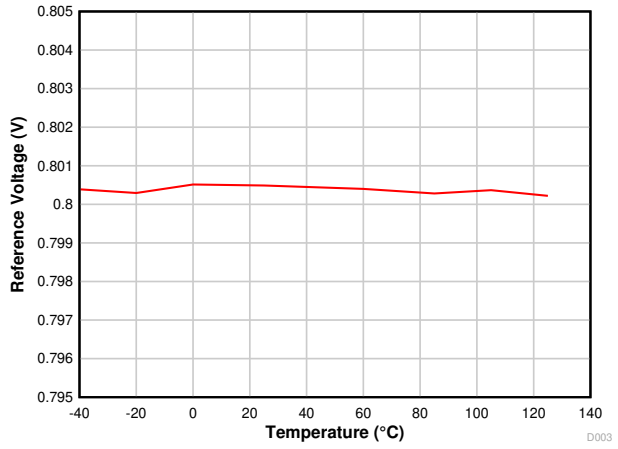


図 7-7. Reference Voltage vs Temperature

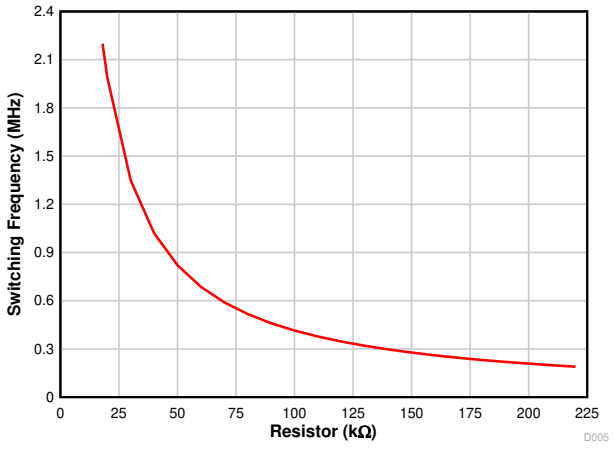


図 7-8. Switching Frequency vs Setting Resistance

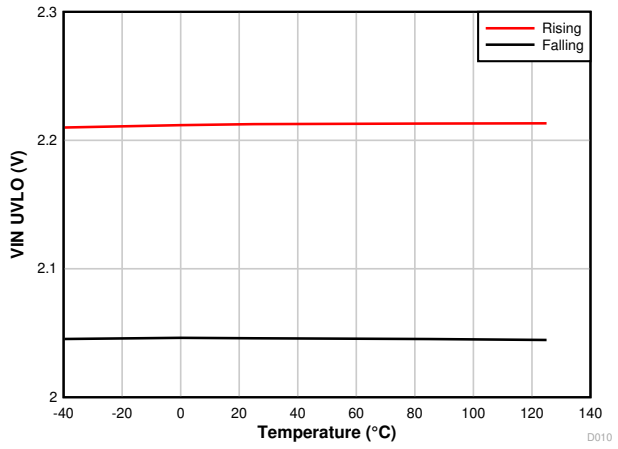


図 7-9. V_{IN} UVLO Threshold Voltage vs Temperature

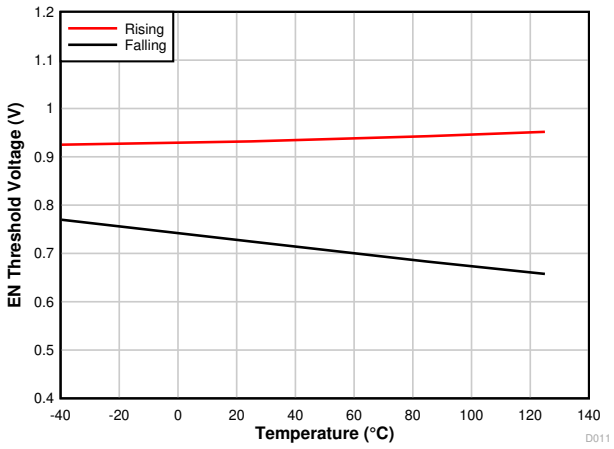


図 7-10. EN Threshold Voltage vs Temperature

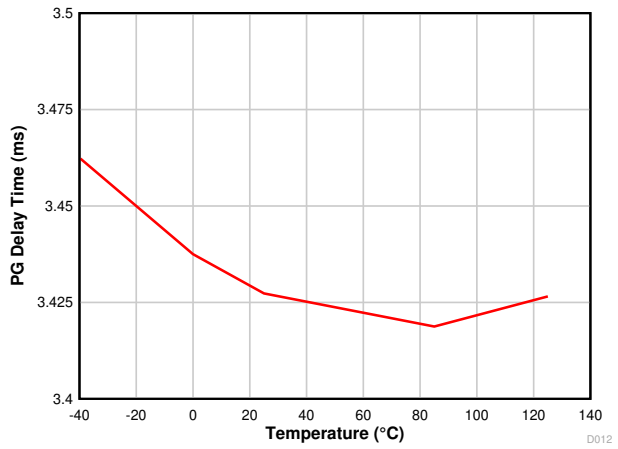


図 7-11. PG Delay Time vs Temperature

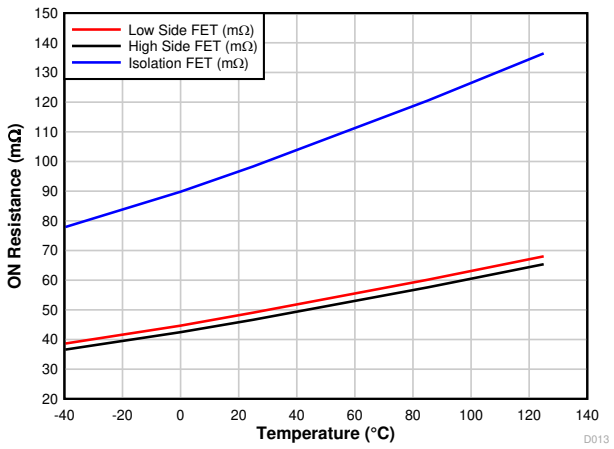


図 7-12. R_{DSON} vs Temperature

8 Detailed Description

8.1 Overview

The TPS61379-Q1 is a fully integrated synchronous boost converter with load disconnect function. It supports output voltage up to 18.5 V with a maximum 2-A fixed switching peak current limit. The input voltage ranges from 2.3 V to 14 V while consuming 25-µA quiescent current.

The device utilizes the fixed frequency peak current control scheme, which has an internal oscillator and supports adjustable switching frequency from 200 kHz to 2.2 MHz.

The device operates with fixed frequency pulse width modulation (PWM) from medium to heavy load. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier (EA). Once the switching peak current triggers the output of the EA, the low-side N-MOSFET is turned off and the high-side N-MOSFET is turned on after a short dead time. The high-side N-MOSFET switch is not turned off until the next cycle as determined by the internal oscillator. The low-side switch turns on again after a short dead time and the switching cycle is repeated.

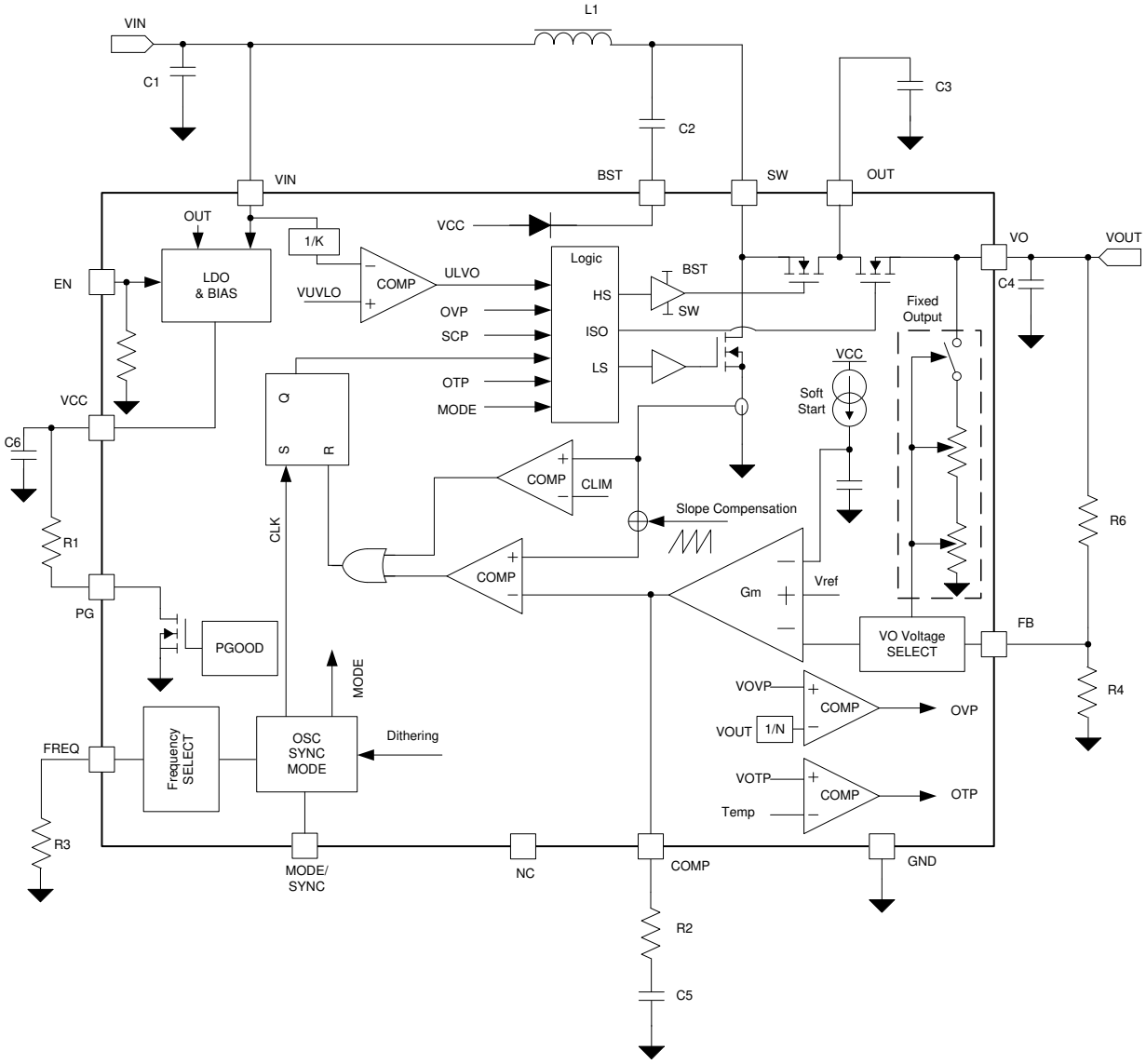
The TPS61379-Q1 provides either Auto PFM or Forced PWM option for light load operation by configuring the MODE/SYNC pin. In Forced PWM mode, the switching frequency remains constant across the entire load range, which helps avoid the frequency variation with load. The internal oscillator can be synchronized to an external clock applied on the MODE / SYNC pin. Spread spectrum modulation of the frequency in Forced PWM mode helps optimize the EMI performance for automotive applications. In Auto PFM mode, the switching frequency can decrease, resulting in higher efficiency.

The device implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. If the output current further increases and triggers the output voltage to fall below the input voltage, the TPS61379-Q1 enters into hiccup mode short protection.

There is a built-in soft-start time that prevents the inrush current during the start-up. The TPS61379-Q1 also provides a power good (PG) indicator to enable the power sequence control for start-up.

The TPS61379-Q1 also has a number of protection features including output short protection, output overvoltage protection (OVP), and thermal shutdown protection (OTP).

8.2 Functional Block Diagrams



8.3 Feature Description

8.3.1 VCC Power Supply

The internal LDO in the TPS61379-Q1 outputs a regulated voltage of 4.8 V with 10-mA output current capability. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor must be above 1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10 V is recommended.

8.3.2 Input Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.04 V (typical). A hysteresis of 160 mV (typical) is added so that the device cannot be enabled again until the input voltage exceeds 2.2 V (typical). This function is implemented to prevent malfunctioning of the device when the input voltage is between 2.04 V and 2.2 V.

8.3.3 Enable and Soft Start

When the input voltage is above the UVLO threshold and the EN pin is pulled above 1.2 V, the TPS61379-Q1 is enabled. The TPS61379-Q1 starts to monitor the FB pin. With a typical 400-µs delay time after EN is pulled high,

the TPS61379-Q1 starts switching. There is an internal built-in start-up time, which is typically 2.5 ms, to limit the inrush current during start-up.

8.3.4 Shut Down

When the input voltage is below the UVLO threshold or the EN pin is pulled low, the TPS61379-Q1 is in shutdown mode and all the functions are disabled. The input voltage is isolated from the output to minimize the leakage currents.

8.3.5 Switching Frequency Setting

The TPS61379-Q1 uses a fixed frequency control scheme. The switching frequency can be programmed between 200 kHz and 2.2 MHz using a resistor from the FREQ pin to GND. The resistor must be connected when the oscillator is synchronized by an external clock. The resistance is defined by 式 1.

$$F_{SW}(MHz) = \frac{41.9}{R_{FREQ}(k\Omega) + 1.05} \quad (1)$$

where

- R_{FREQ} is the resistance between the FREQ pin and the GND pin

For instance, the switching frequency is 2.2 MHz if the resistance between the FREQ pin and GND is 18 kΩ. This pin cannot be left floating or tied to VCC.

8.3.6 Spread Spectrum Frequency Modulation

The TPS61379-Q1 uses a triangle waveform to spread the switching frequency with ±10% of normal frequency. The frequency of the triangle waveform is typically 0.4% of the switching frequency. For example, if the normal switching frequency of TPS61379-Q1 is programmed to 2.2 MHz, the spread spectrum function modulates the switching frequency in the range of 1.98 MHz to 2.42 MHz in a triangle behavior with 8.8 kHz rate.

The spread spectrum is only available while the clock of the TPS61379-Q1 is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- An external clock is applied to the MODE/SYNC pin.
- The device works in the PFM operation at light load.

8.3.7 Bootstrap

The TPS61379-Q1 has an integrated bootstrap regulator circuit. A small ceramic capacitor is needed between the BST pin and SW pin to provide the gate drive supply voltage for the high-side switches. The bootstrap capacitor is charged during the time when the low-side switch is in the ON state. The value of this ceramic capacitor must be above 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3 V is recommended.

8.3.8 Load Disconnect

The TPS61379-Q1 integrates a load disconnect function when the input source is DC, which completely cuts off the path between the input side and the output side during shutdown.

The output disconnect function also allows the output short protection and minimize the inrush current at start-up.

8.3.9 MODE/SYNC Configuration

表 8-1 summarizes the MODE/SYNC function and the entry condition.

表 8-1. MODE/SYNC Configuration

MODE/SYNC PIN CONFIGURATION	MODE
Logic Low or Floating	Auto PFM Mode
Logic High	Forced PWM Mode
External Synchronization	Forced PWM Mode

The TPS61379-Q1 can be synchronized to an external clock applied to the MODE / SYNC pin.

8.3.10 Overvoltage Protection (OVP)

If the output voltage exceeds the OVP threshold (typical 20 V), the TPS61379-Q1 stops switching immediately until the output voltage drops below the recovery threshold (typical 19.5 V). This function protects the device against excessive voltage.

8.3.11 Output Short Protection/Hiccup

In addition to the cycle-by-cycle current limit function, the TPS61379-Q1 also has output short protection. If the output current causes low-side FET to reach current limit and pull the output voltage below the input voltage, the device enters into short circuit protection mode which triggers the hiccup timer. When the hiccup timer is triggered, the device limits the current to a relative lower level for 1.8 ms, and then shuts down. After 67 ms, it restarts. If the short condition disappears, the device automatically restarts.

When FB voltage is below ≤ 0.1 V during fault condition, the current limit threshold is reduced to 1/5 of the programmed current limit, and frequency is clamped to 1.1 MHz if the FREQ pin setting is greater than 1.1 MHz and VIN and V_O voltage delta is greater than 6 V.

8.3.12 Power-Good Indicator

The TPS61379-Q1 integrates a power-good function. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply like VCC. The PG pin goes high with a typical 3.4-ms delay time after VOUT reaches 90% of the target output voltage. When the output voltage drops below 85% of the target output voltage, the PG pin immediately goes low without delay.

8.3.13 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 165°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 145°C (typical).

8.4 Device Functional Modes

8.4.1 Forced PWM Mode

The TPS61379-Q1 enters forced PWM mode by pulling the MODE/SYNC pin to logic high for more than five switching cycles. In forced PWM mode, the TPS61379-Q1 keeps the switching frequency constant at light load condition. When the load current decreases, the output of the internal error amplifier also decreases to keep the inductor peak current down. When the output current decreases further, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant.

8.4.2 Auto PFM Mode

The TPS61379-Q1 enters auto PFM mode by pulling the MODE/SYNC pin to logic low for more than five switching cycles or leave the pin floating. The TPS61379-Q1 improves the efficiency at light load when operating in PFM mode. When the output current decreases to a certain level, the output voltage of the error amplifier is clamped by the internal circuit. If the output current reduces further, the inductor current through the high-side switch is clamped but not further lowered. Pulses are skipped to improve the efficiency at light load.

8.4.3 External Clock Synchronization

The TPS61379-Q1 supports external clock synchronization with a range of 200 kHz to 2.2 MHz. The TPS61379-Q1 remains in the forced PWM mode and operates in CCM across the entire load range if the oscillator is synchronized by an external clock. Spread spectrum feature is disabled when external synchronization is used.

8.4.4 Down Mode

The TPS61379-Q1 features Down mode operation when input voltage is close to or higher than output voltage. In Down mode, output voltage is regulated at target value even when V_{IN} > VO. The high-side and low-side FETs of the TPS61379-Q1 are switching devices that always work in boost operation, where the isolation FET always works as a linear device.

For boost circuits, on time or duty cycle is reduced as input voltage approaches output voltage. The TPS61379-Q1 enters Down mode when V_{IN} reaches 85% (typical) of VO voltage at 2.2 MHz; while exiting Down mode requires V_{IN} to be reduced below 85% (typical) of VO voltage at 2.2 MHz.

In normal operation, isolation FET is fully on.

When Down mode is triggered and V_{IN} is less than VO pin voltage, the OUT pin has a fixed 2 V (typical) above VO pin voltage. Isolation FET works in LDO mode to regulate VO pin voltage with a 2-V constant voltage drop.

When Down mode is triggered and V_{IN} is 100 mV (typical) higher than VO pin voltage, the OUT pin has an approximated 3 V (typical) above V_{IN} pin voltage, as V_{IN} keeps rising, the OUT pin continues to raise with 3 V on top of V_{IN}, isolation FET works in LDO mode to regulate VO pin voltage with a voltage differential of OUT pin and VO pin.

Refer to 図 8-1.

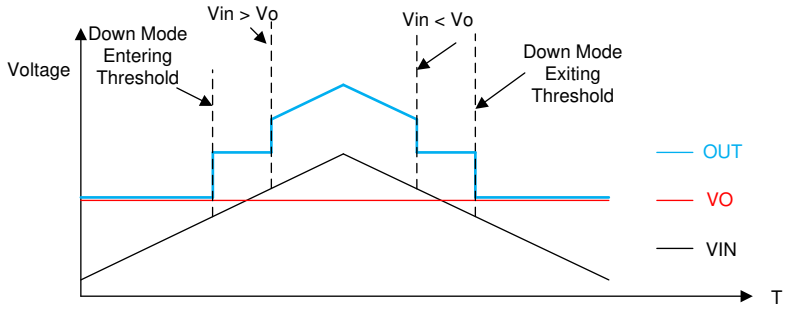


図 8-1. Down Mode

Care should be taken during short-to-ground condition when operation V_{IN} is above 6 V. During hiccup on, the device operates in Down mode and isolation FET voltage drop is V_{IN} + 3 V (OUT pin to VO pin).

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPS61379-Q1 is a 25-µA quiescent current boost converter that supports 2.3-V to 14-V input voltage range. It also supports load disconnect to minimize the leakage current. The following design procedure can be used to select component values for the TPS61379-Q1.

9.2 Typical Application

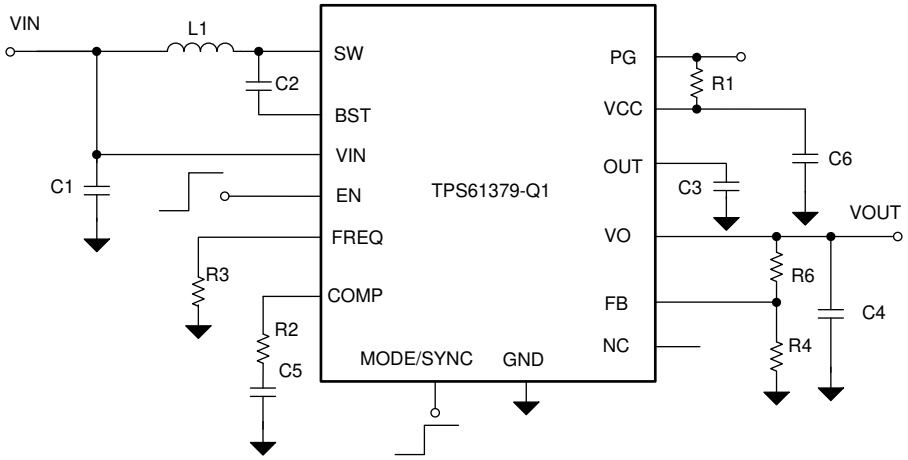


図 9-1. Typical Application

9.2.1 Design Requirements

A typical application example is dual cameras powered through a coax cable, which normally requires 9.0-V output as its bias voltage and consumes less than 200-mA current per camera. 250-mA load current is designed to provide margin. The following design procedure can be used to select external component values for the TPS61379-Q1.

表 9-1. Design Requirements

PARAMETERS	VALUES
Input voltage	3.3 V to 6.4 V
Output voltage	9.0 V
Switching frequency	2.2 MHz
Output current	250 mA
Output voltage ripple	± 25 mV

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Output Voltage

There are two ways to set the output voltage of the TPS61379-Q1: adjustable or fixed. If the resistance between FB and GND is higher than 14.4kΩ and less than 100kΩ during start-up, the TPS61379-Q1 works as an adjustable output version. The FB pin is connected to the negative input of the internal error amplifier directly.

The output voltage can be programmed by adjusting the external resistor divider R_{Upper} and R_{Lower} according to 式 2. When the output voltage is in well regulation, the typical voltage at the FB pin is V_{REF} of 0.8 V.

$$V_{OUT} = V_{REF} \times \frac{(R_{Upper} + R_{Lower})}{R_{Lower}} \quad (2)$$

For some applications where the resistor needs to be as low as possible, the low-side divider can be 20 kΩ. The reference voltage is 0.8 V, the high-side divider is 205 kΩ for 9-V output voltage.

For other applications without specific requirements on divider resistance, the user can choose R_{Lower} to be approximately 80.6 kΩ. Slightly increasing or decreasing R_{Lower} can result in closer output voltage matching when using standard values resistors.

For the best accuracy, R_{Lower} is recommended to be smaller than 100 kΩ to ensure that the current following through R_{Lower} is at least 100 times larger than FB pin leakage current. Changing R_{Lower} towards the lower value increases the robustness against noise injection. Changing the R_{Lower} to higher values reduces the quiescent current for achieving higher efficiency at light load.

If the resistance between FB and GND is less than 9.6kΩ during start-up, the TPS61379-Q1 works as a fixed output voltage version. The TPS61379-Q1 uses the internal resistor divider.

For 5-V fixed output voltage, R_{Lower} is between 0Ω and 2.4kΩ and R_{Upper} should be removed.

For 5.25-V fixed output voltage, R_{Lower} is between 3.6kΩ and 4.8 kΩ and R_{Upper} should be removed.

For 5.5-V fixed output voltage, R_{Lower} is between 7.2kΩ and 9.6kΩ and R_{Upper} should be removed.

9.2.2.2 Setting the Switching Frequency

The switching frequency of the TPS61379-Q1 is set at 2.2 MHz. Use 式 1 to calculate the required resistor value. The calculated value is 18 kΩ to get the frequency of 2.2 MHz.

9.2.2.3 Selecting the Inductor

A boost converter normally requires two main passive components for storing the energy during the power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency) as well as the transient behavior and loop stability, which makes the inductor the most critical component in application.

When selecting the inductor, as well as the inductance, the other important parameters are:

- The maximum current rating (RMS and peak current must be considered)
- The series resistance
- Operating temperature

The TPS61379-Q1 has built-in slope compensation to avoid subharmonic oscillation associated with the current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 2 A, the slope compensation may not be adequate, and the loop can be unstable. Therefore, it is recommended to make the peak-to-peak current ripple between 800 mA to 2 A when selecting the inductor.

The inductance can be calculated by 式 3, 式 4, and 式 5:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (3)$$

$$\Delta I_{L\_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \quad (4)$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \quad (5)$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple % is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches the saturation level, its inductance can decrease 20% to 35% from the value at 0-A bias current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, the switching frequency, the input and output voltages and it can be calculated by 式 6 and 式 7.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \tag{6}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- Δ_{IL} is the ripple current of the inductor

The input DC current is determined by the output voltage, the output current can be calculated by:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{7}$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage, and duty cycle are calculated by 式 3. Replace 式 3 and 式 7 into 式 6 and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1 - D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \tag{8}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor

- f_{SW} is the switching frequency

The heat rating current (RMS) is as below:

$$I_{L\_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \quad (9)$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- Δ_{IL} is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. 表 9-2 lists some recommended inductors.

表 9-2. Recommended Inductors

PART NUMBER	L (μH)	DCR TYP (mΩ) MAX	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR(1)
XGL3515-451ME	0.45	8.2	3.2	3.5 × 3.2 × 1.5	Coilcraft
XGL3515-102ME	1	18.5	2.2	3.5 × 3.2 × 1.5	Coilcraft
TFM252012ALMAR47MTAA	0.47	19	4.9	3.2 × 2.5 × 1.2	TDK
TFM252012ALMA1R0MTAA	1	35	4.7	3.2 × 2.5 × 1.2	TDK

(1) See *Third-party Products Disclaimer*

9.2.2.4 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by 式 10:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (10)$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

The additional output ripple component caused by ESR is calculated by 式 11:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (11)$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using 式 12:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (12)$$

where

- ΔI_{STEP} is the transient load current step
- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

For the output capacitor on the OUT pin, the effective capacitance is recommended between 0.22 µF to 1 µF.

Care must be taken when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of its capacitance at its rated voltage. Therefore, enough margins on the voltage rating must be considered to ensure adequate capacitance at the required output voltage.

9.2.2.5 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22-µF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, must be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

9.2.2.6 Loop Stability and Compensation

9.2.2.6.1 Small Signal Model

The TPS61379-Q1 uses the fixed frequency peak current mode control. There is an internal adaptive slope compensation to avoid the subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. 図 9-2 shows the equivalent small signal elements of a boost converter.

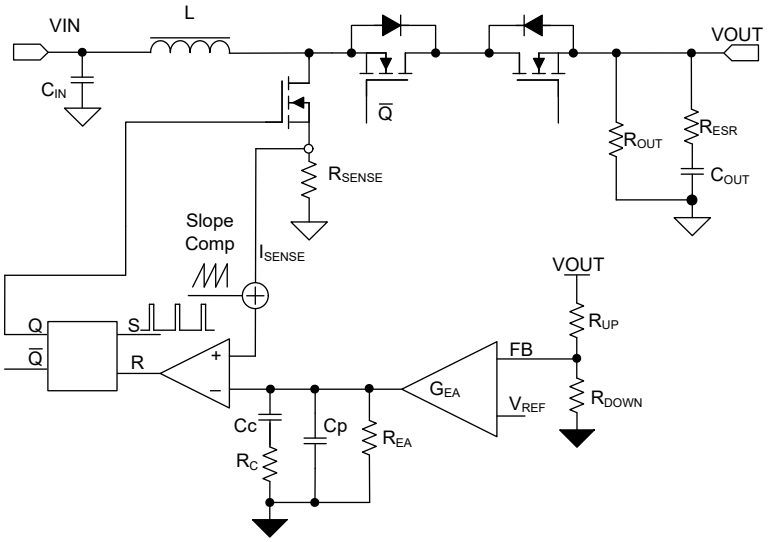


図 9-2. TPS61379-Q1 Control Equivalent Circuitry Model

The small signal of power stage is:

$$K_{PS}(S) = \frac{R_{OUT} \times (1-D)}{2 \times R_{SENSE}} \times \frac{(1+\frac{S}{2\pi \times f_{ESR}})(1-\frac{S}{2\pi \times f_{RHP}})}{(1+\frac{S}{2\pi \times f_P})} \quad (13)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- R_{SENSE} is the equivalent internal current sense resistor, which is typically 118 mΩ

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (14)$$

where

- C_{OUT} is the output capacitance. For a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (15)$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1-D)^2}{2\pi \times L} \quad (16)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance

式 17 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2 \times \pi \times f_Z}}{(1 + \frac{S}{2 \times \pi \times f_{P1}}) \times (1 + \frac{S}{2 \times \pi \times f_{P2}})} \quad (17)$$

where

- R_{EA} is the output impedance of the error amplifier and typical R_{EA} = 500 MΩ.
- f_{P1}, f_{P2} is the pole's frequency of the compensation, f_Z is the zero's frequency of the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c} \quad (18)$$

where

- C_C is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \quad (19)$$

where

- C_P is the pole capacitor compensation
- R_C is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \quad (20)$$

9.2.2.6.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Cross Over Frequency, f_C.**

   The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. Then calculate the loop compensation network values of R_C, C_C, and C_P by the following equations.
2. **Set the Compensation Resistor, R_C.**

   By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} ~ = R_C and so R_C × G_{EA} sets the compensation gain. Setting the compensation gain, $K_{COMP-dB}$, at f_Z, results in the total loop gain, $T_{(s)} = K_{PS(s)} \times H_{EA(s)}$ being zero at f_C.

   Therefore, to approximate a single-pole roll-off up to f_{P2}, rearrange 式 17 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}, read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \quad (21)$$

where

- K_{EA} is gain of the error amplifier network
- K_{PS} is the gain of the power stage
- G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 70 µA / V

3. **Set the Compensation Zero capacitor, C_C.**

Place the compensation zero at the power stage R_{OUT} ,C_{OUT} pole's position to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{22}$$

Set $f_Z = f_P$, and get

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \tag{23}$$

4. **Set the Compensation Pole Capacitor, C_P.**

Place the compensation pole at the zero produced by the R_{ESR} and the C_{OUT}. It is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \tag{24}$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{25}$$

Set $f_{P2} = f_{ESR}$, and get

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \tag{26}$$

9.2.2.6.3 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during turn-on of each cycle and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1 µF to 1 µF. C_{BST} must be a good quality, low-ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1 µF was selected for this design example.

9.2.2.6.4 V_{CC} Capacitor

The primary purpose of the V_{CC} capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the V_{CC} regulator. The value of C_{VCC} must be at least 10 times greater than the value of C_{BST}, and must be a good quality, low-ESR, ceramic capacitor. C_{VCC} must be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 2.2 µF was selected for this design example.

9.2.3 Application Curves

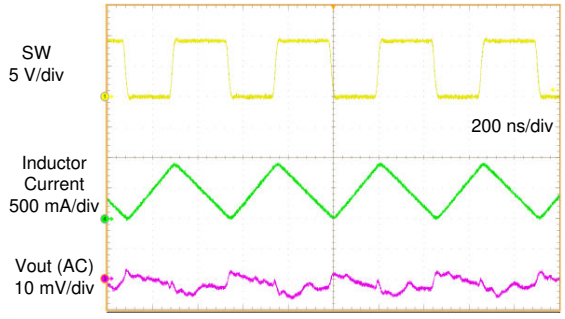


図 9-3. Switching Waveform V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 250 mA, FPWM

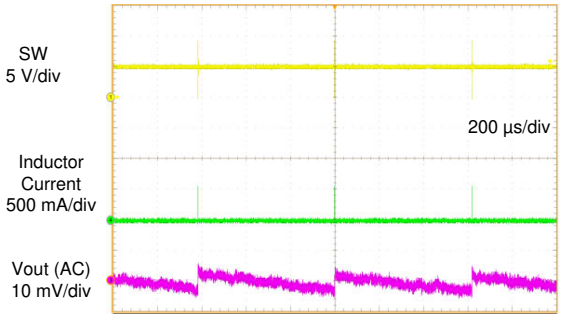


図 9-4. Switching Waveform V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 0 mA, Auto PFM

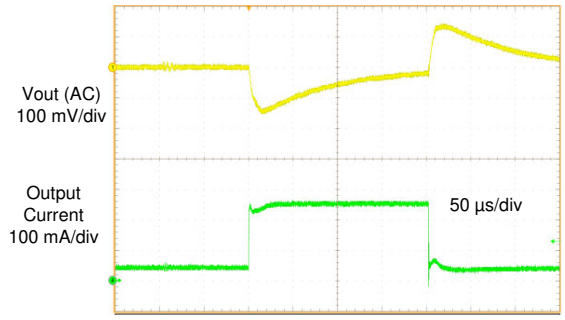


図 9-5. Load Transient V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 50 mA to 250 mA, FPWM

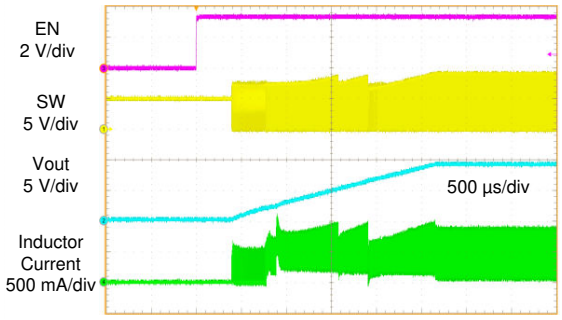


図 9-6. Start-up from EN Waveform V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 250 mA, FPWM

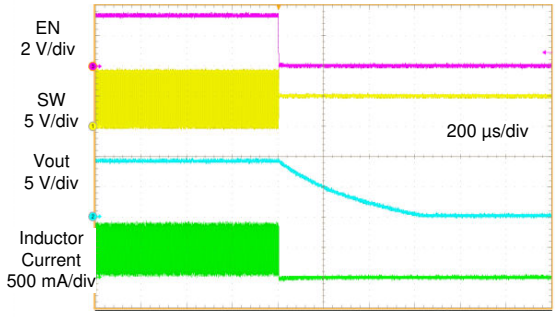


図 9-7. Shutdown from EN Waveforms V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 250 mA, FPWM

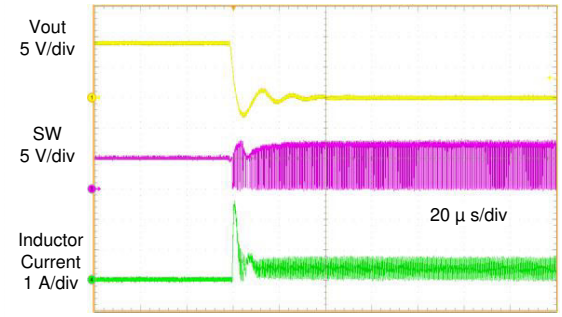


図 9-8. Short Circuit Protection V_{IN} = 5 V, V_{OUT} = 9 V, FPWM

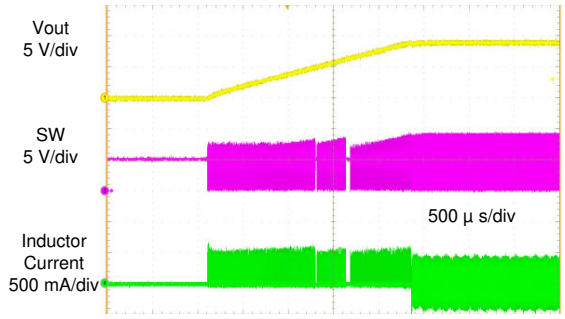


図 9-9. Short Circuit Recovery V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 0 mA, FPWM

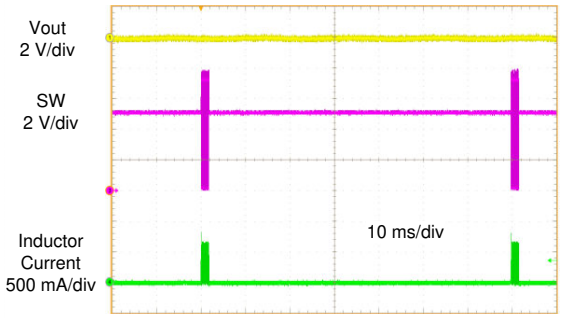


図 9-10. Hiccup Short Circuit Protection V_{IN} = 5 V, V_{OUT} = 9 V, FPWM

10 Power Supply Recommendations

The TPS61379-Q1 is designed to operate from an input voltage supply range between 2.3 V to 14 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor must be placed as close as possible to the IC.

11.2 Layout Example

The bottom layer is a large GND plane connected by vias.

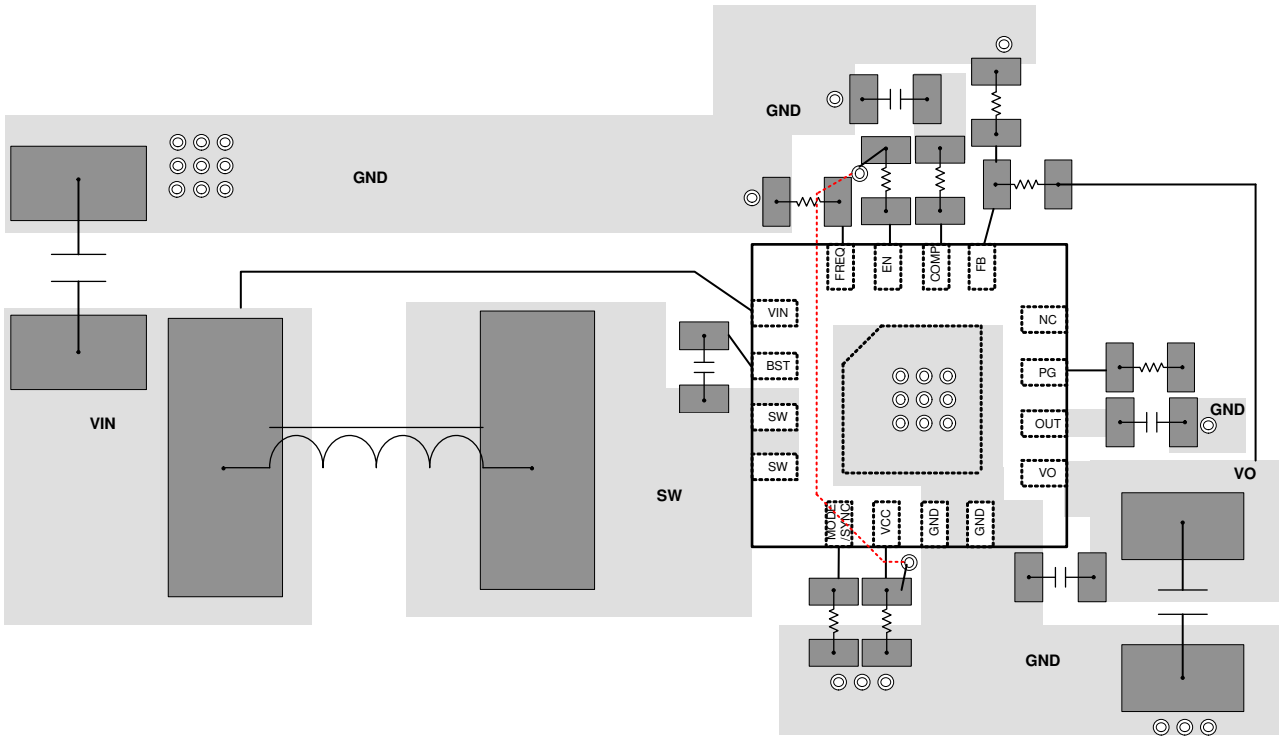


図 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.5 用語集

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12.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61379QWRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2H1H
TPS61379QWRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2H1H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

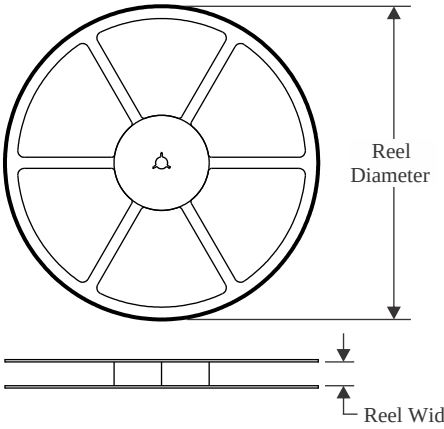
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

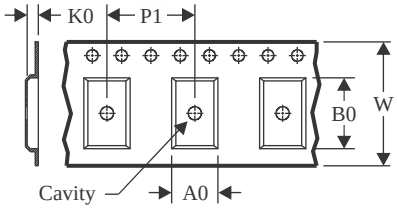
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

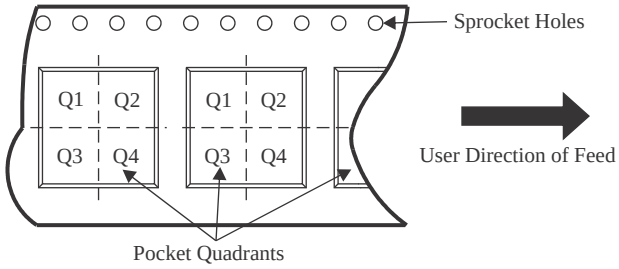


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

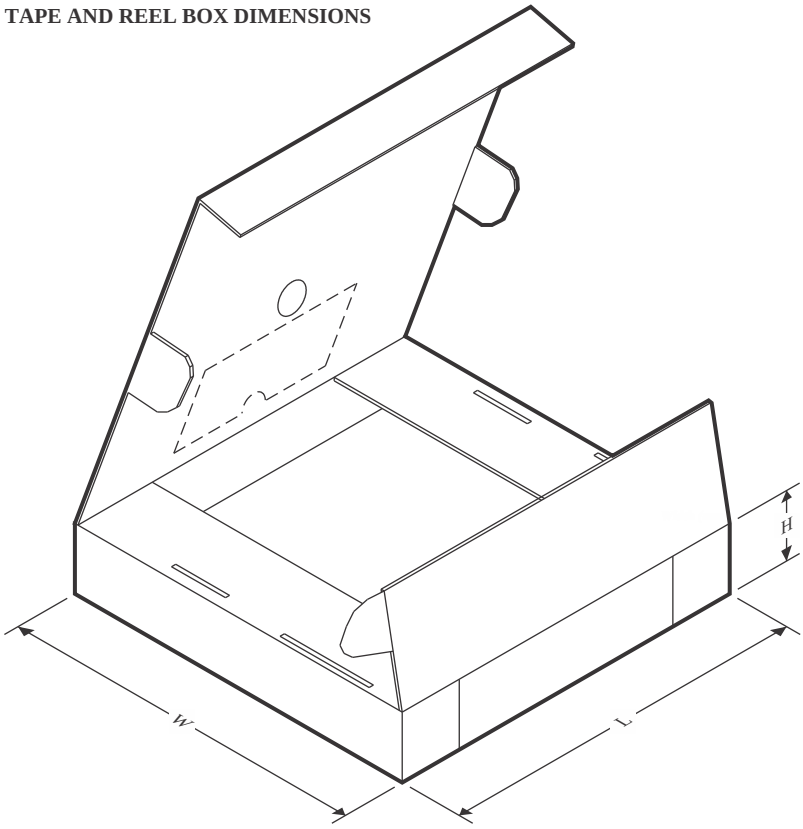
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61379QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61379QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61379QWRTERQ1	WQFN	RTE	16	3000	346.0	346.0	33.0
TPS61379QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

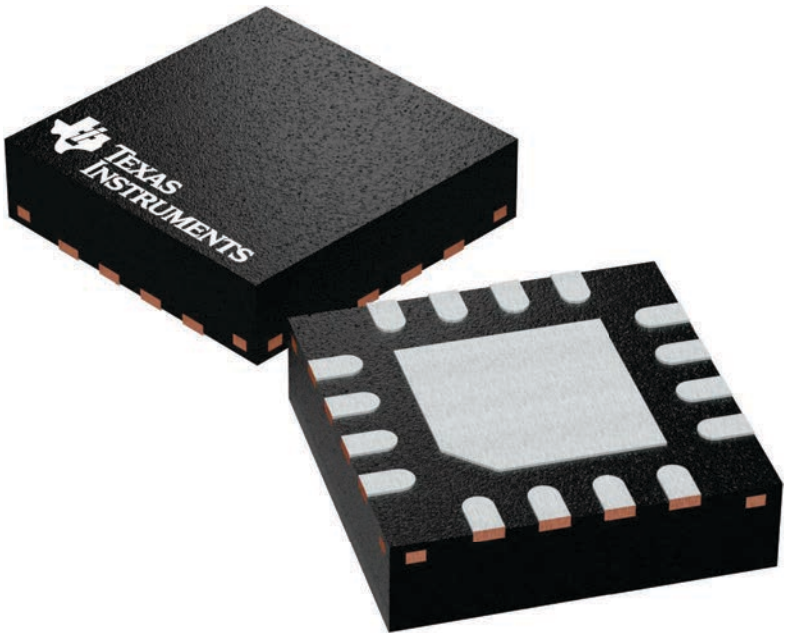
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

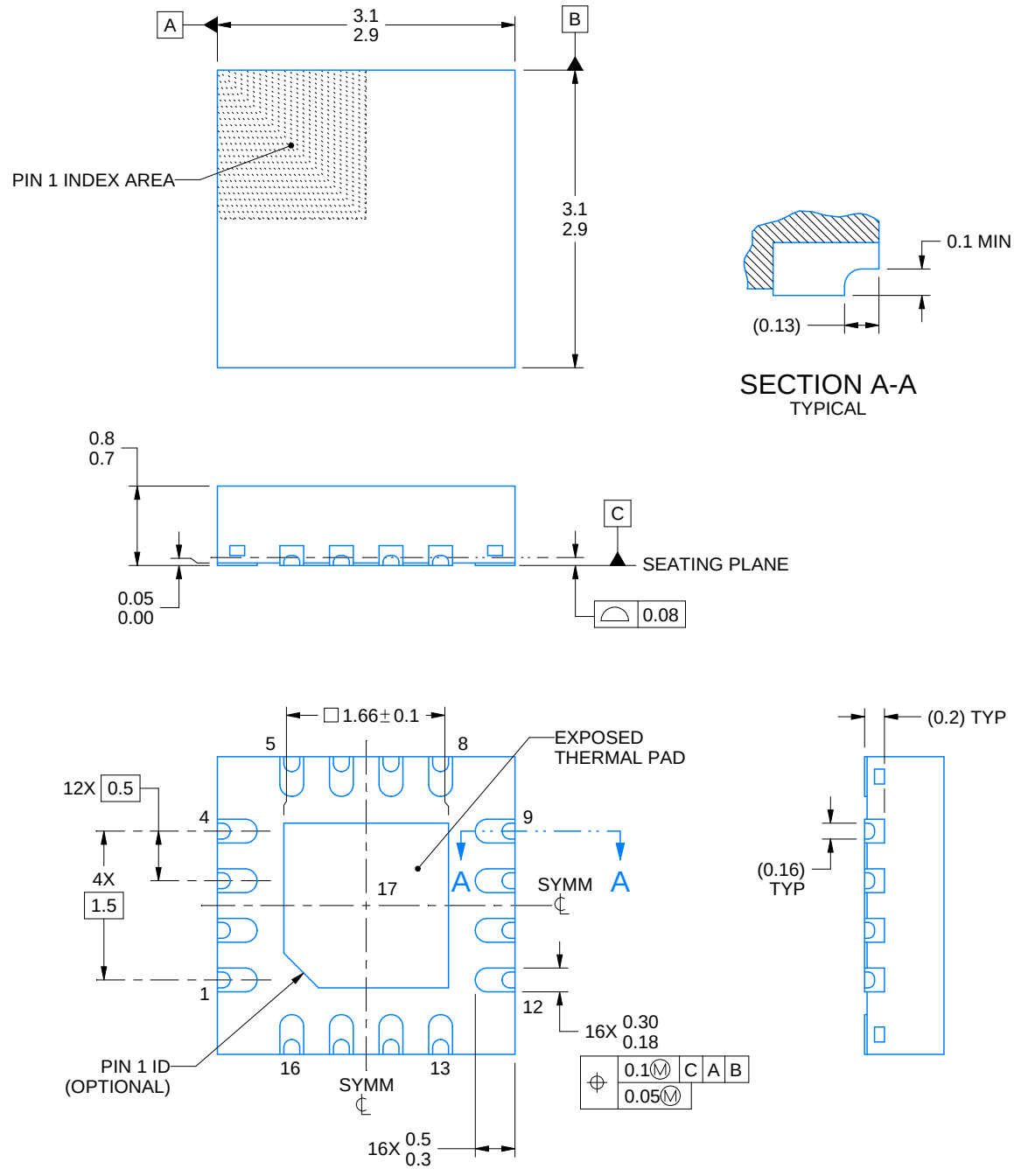


RTE0016K

PACKAGE OUTLINE

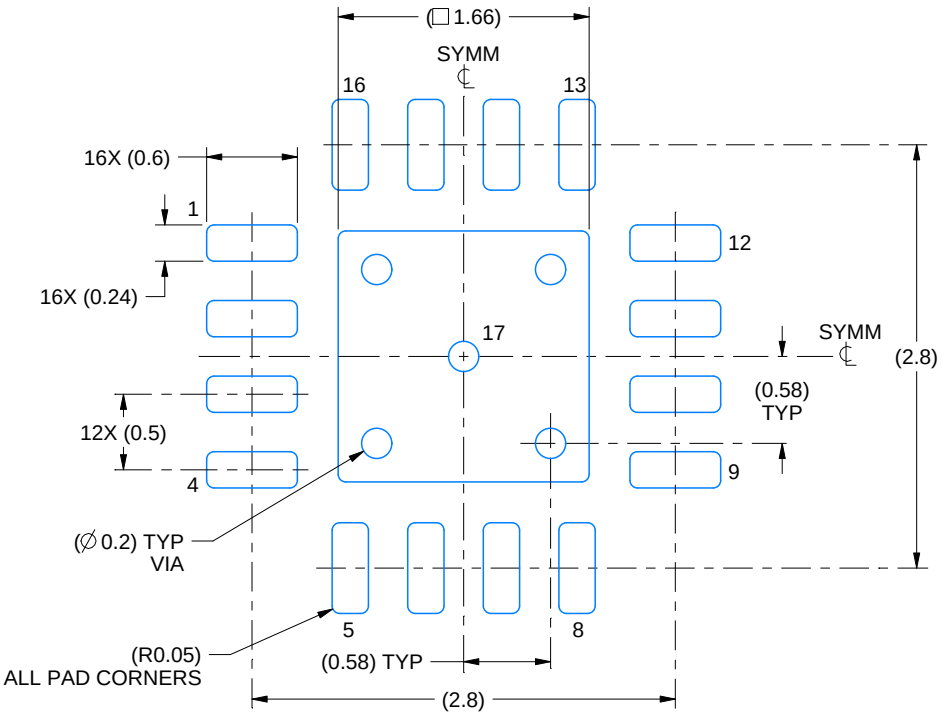
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

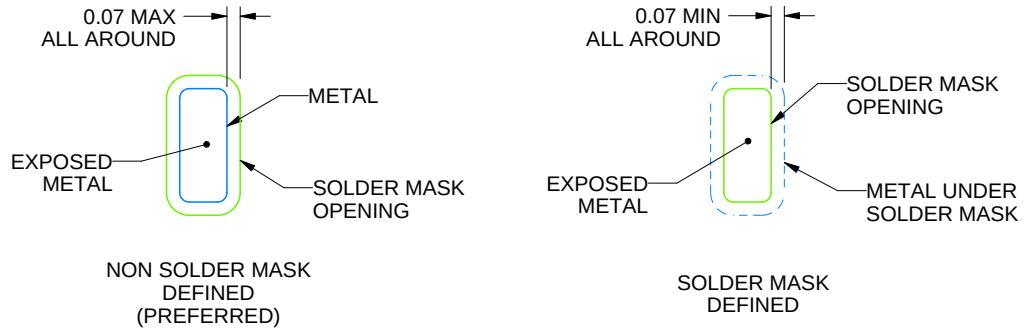


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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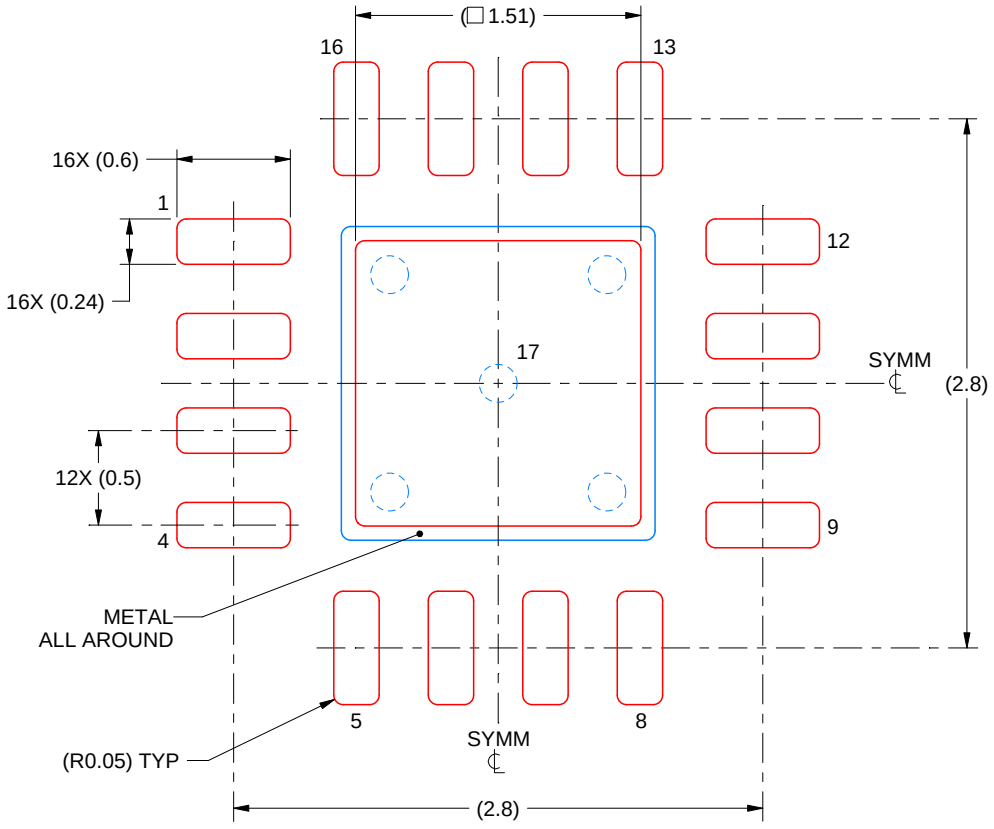
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月