TEXAS INSTRUMENTS

TPS62170, TPS62171, TPS62172, TPS62173

JAJSBL0E – NOVEMBER 2011 – REVISED MAY 2017

TPS6217x 3V～17V、0.5A降圧型コンバータ、DCS-Control™搭載

1 特長

- DCS-Control™トポロジ
- 入力電圧範囲: 3V～17V
- 最大500mAの出力電流
- 出力電圧を0.9V～6Vの範囲で調整可能
- 固定出力電圧バージョン
- シームレスなパワーセーブ・モード移行
- 静止電流17µA (標準値)
- パワー・グッド出力
- 100%デューティ・サイクル・モード
- 短絡保護
- 過熱保護機能
- TPS62160およびTPS62125とピン互換
- 2mm×2mmの8ピンWSONパッケージで供給
- WEBENCH® Power Designerにより、TPS62170を使用するカスタム設計を作成

2 アプリケーション

- 標準の12Vレール電源
- 単一または複数のリチウムイオン・バッテリからのPOL電源
- LDOの代替品
- 組み込みシステム
- デジタル静止画カメラ、ビデオ
- モバイルPC、タブレットPC、モデム

3 概要

TPS6217xデバイス・ファミリは使いやすい同期整流降圧型DC/DCコンバータで、電力密度の高いアプリケーション用に最適化されています。スイッチング周波数が標準値で2.25MHzと高いため、小型のインダクタを使用でき、高速な過渡応答が実現されるとともに、DCS-Control™トポロジの使用によって出力電圧の高い精度が得られます。

3V～17Vの広い入力電圧範囲で動作するため、このデバイスはリチウムイオンや他のバッテリ、および12Vの中間電源レールで動作するシステムに最適です。0.9V～6Vの出力電圧で、0.5Aまでの出力電流を連続的にサポートします(100%デューティ・サイクル・モード時)。

イネーブル・ピンおよびオープン・ドレインのパワー・グッド・ピンの構成により、電源シーケンシングも可能です。

パワーセーブ・モードでは、このデバイスはVINから約17µAの静止電流を消費します。負荷が小さい時には自動的かつシームレスにパワーセーブ・モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。シャットダウン・モードではデバイスがオフになり、シャットダウン時の消費電流は2µA未満です。

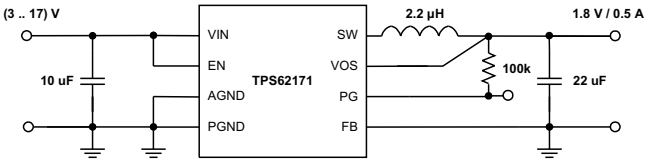
このデバイスには、出力電圧が可変と固定のバージョンがあり、2mm×2mmの8ピンWSONパッケージ(DSG)に封入されています。

製品情報(1)

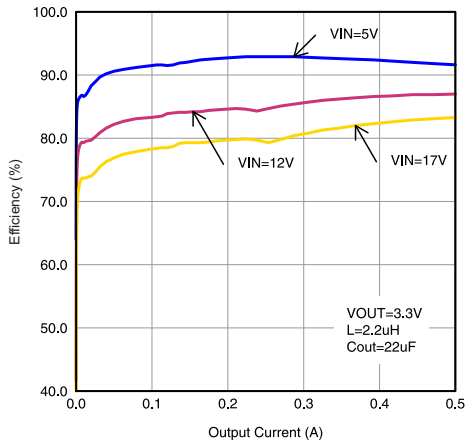
型番	パッケージ	本体サイズ(公称)
TPS6217x	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



効率と出力電流との関係



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目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (October 2014) から **Revision E** に変更 **Page**

- WEBENCH® Designerへのリンクを 追加 ... 1
- Added "SW (AC), less than 10ns" specification to Absolute Maximum Ratings table ... 4
- Changed T_J MAX spec from "125" to "150" ... 4
- Changed Electrical Characteristics Conditions from "free-air temperature range" to "junction temperature range" ... 5
- Added I_Q and I_{SD} specifications ... 5
- Added 125°C plot line in Figure 1 and Figure 4 Typical Characteristics graphic entities. ... 6
- Added Power Good Pin Logic Table ... 9

Revision C (August 2013) から **Revision D** に変更 **Page**

- 「*ピン構成および機能* 」セクション、「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

Revision B (August 2013) から **Revision C** に変更 **Page**

- Changed 50mV/µs to 50mV/s in Enable and Shutdown (EN) section ... 8

Revision A (April 2012) から **Revision B** に変更 **Page**

- Added diode to Figure 41 ... 24

2011年11月 発行のものから更新 **Page**

- Changed Table 2 ... 13

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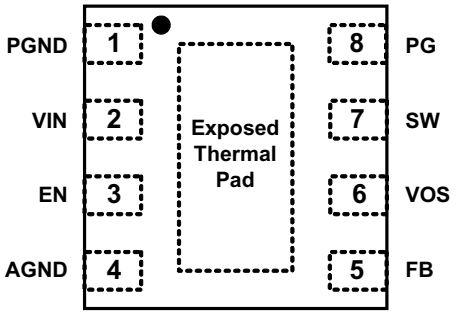
5 Device Voltage Options

OUTPUT VOLTAGE(1)	PART NUMBER	PACKAGE
adjustable	TPS62170	WSON (8)
1.8 V	TPS62171	
3.3 V	TPS62172	
5.0 V	TPS62173	

(1) Contact the factory to check availability of other fixed output voltage versions.

6 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN(1)		I/O	DESCRIPTION
NAME	NO.		
PGND	1	—	Power ground
VIN	2	IN	Supply voltage
EN	3	IN	Enable input (High = enabled, Low = disabled)
AGND	4	—	Analog ground
FB	5	IN	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
VOS	6	IN	Output voltage sense pin and connection for the control loop circuitry.
SW	7	OUT	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	8	OUT	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor; goes high impedance, when device is switched off)
Exposed Thermal Pad		—	Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application Information* sections.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage range(2)	VIN	–0.3	20	V
	EN, SW (DC)	–0.3	V_{IN}+ 0.3	V
	SW (AC), less than 10ns(3)	–2	24.5	
	FB, PG, VOS	–0.3	7	V
Power good sink current	PG		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) While switching.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{IN}	3		17	V
Output Voltage, V_{OUT}	0.9		6	V
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6217x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over junction temperature range (T_J = –40°C to +125°C), typical values at V_{IN} = 12 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range(1)			3		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, device not switching			17	30	µA
			T_J = -40°C to +85°C		17	25	
I_{SD}	Shutdown current(2)	EN = Low			1.5	25	µA
			T_J = -40°C to +85°C		1.5	4	
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage		2.6	2.7	2.82	V
		Hysteresis			180		mV
T_{SD}	Thermal shutdown temperature	rising temperature			160		°C
	Thermal shutdown hysteresis	falling temperature			20		
CONTROL (EN, PG)							
V_{EN_H}	High level input threshold voltage (EN)			0.9	0.6		V
V_{EN_L}	Low level input threshold voltage (EN)				0.56	0.3	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN} or GND			0.01	1	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})		92%	95%	98%	
		Falling (%V_{OUT})		87%	90%	93%	
V_{OL_PG}	Power good output low voltage	I_{PG} = –2 mA			0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V			1	400	nA
POWER SWITCH							
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V			300	600	mΩ
		V_{IN}= 3 V			430		
	Low-side MOSFET ON-resistance	V_{IN}≥ 6 V			120	200	mΩ
		V_{IN} = 3 V			165		
I_{LIMF}	High-side MOSFET forward current limit(3)	V_{IN} = 12 V, T_J= 25°C		0.85	1.05	1.35	A
OUTPUT							
V_{REF}	Internal reference voltage(4)				0.8		V
I_{LKG_FB}	Pin leakage current (FB)	TPS62170, V_{FB}= 1.2 V			5	400	nA
V_{OUT}	Output voltage range (TPS62170)	V_{IN} ≥ V_{OUT}		0.9		6.0	V
	Initial output voltage accuracy(5)	PWM mode operation, V_{IN} ≥ V_{OUT} + 1 V		–3%		3%	
		Power save mode operation, C_{OUT}= 22 µF		-3.5 %		4%	
	DC output voltage load regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation			0.05		%/A
	DC output voltage line regulation	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A, PWM mode operation			0.02		%/V

(1) The device is still functional down to under voltage lockout (see parameter V_{UVLO}).
(2) Current into VIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see *Current Limit and Short Circuit Protection*).
(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For fixed voltage versions, the (internal) resistive feedback divider is included.

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7.6 Typical Characteristics

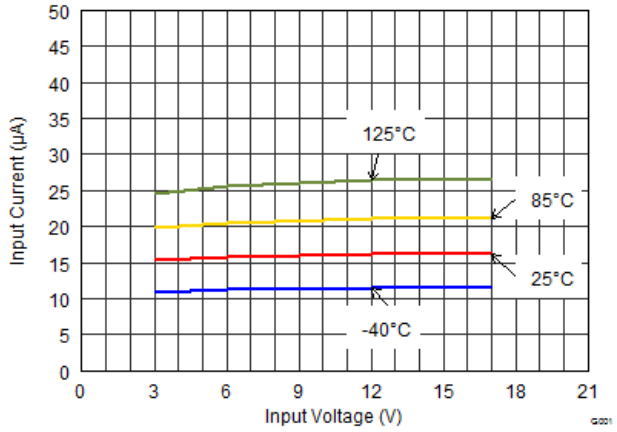

Figure 1. Quiescent Current

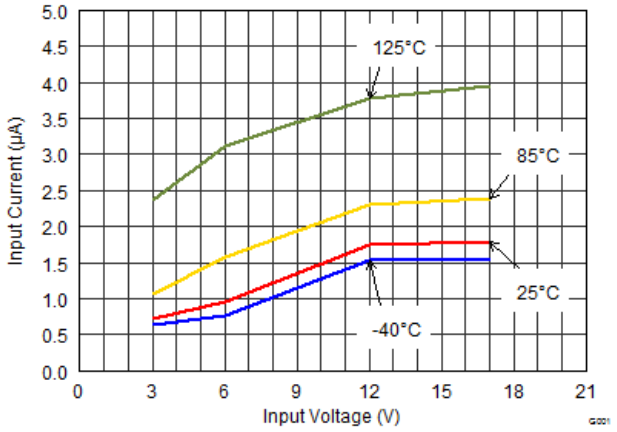

Figure 2. Shutdown Current

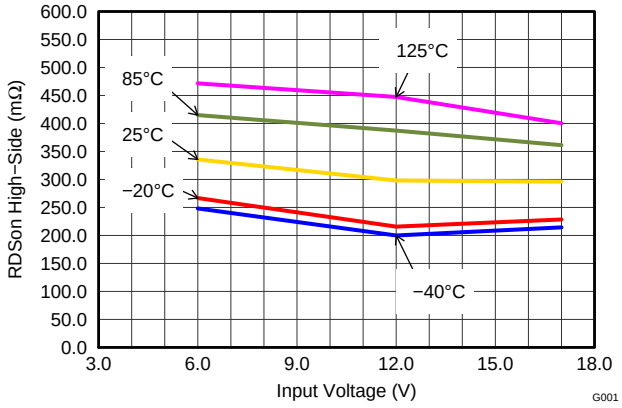

Figure 3. High-Side Switch

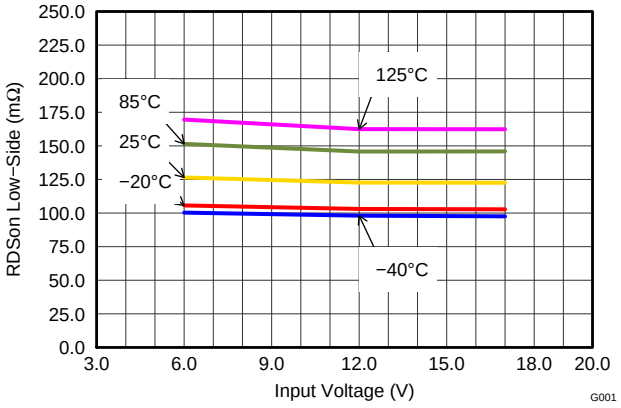

Figure 4. Low-Side Switch

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8 Detailed Description

8.1 Overview

The TPS6217x synchronous step-down DC-DC converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless transition into power save mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports pulse width modulation (PWM) mode for medium and heavy load conditions and a power save mode at light loads. During PWM mode, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power save mode to sustain high efficiency down to very light loads. In power save mode, the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to power save mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 500 mA.

The TPS6217x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram

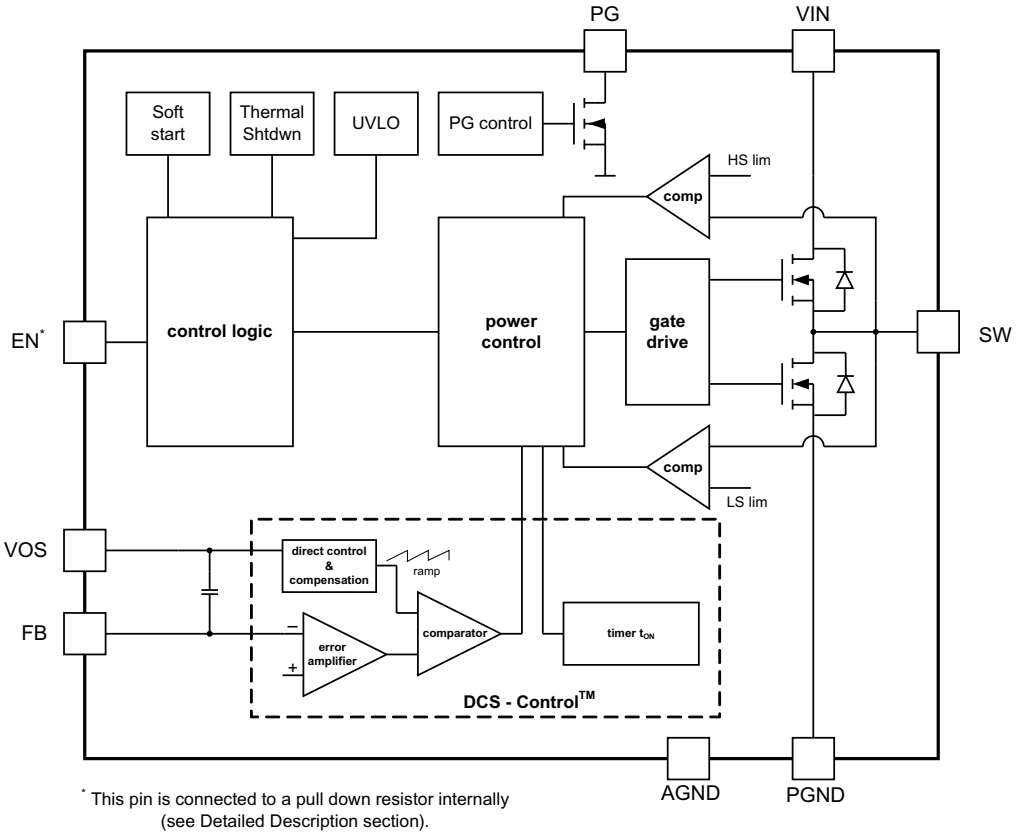

Figure 5. TPS62170 (Adjustable Output Voltage)

Functional Block Diagram (continued)

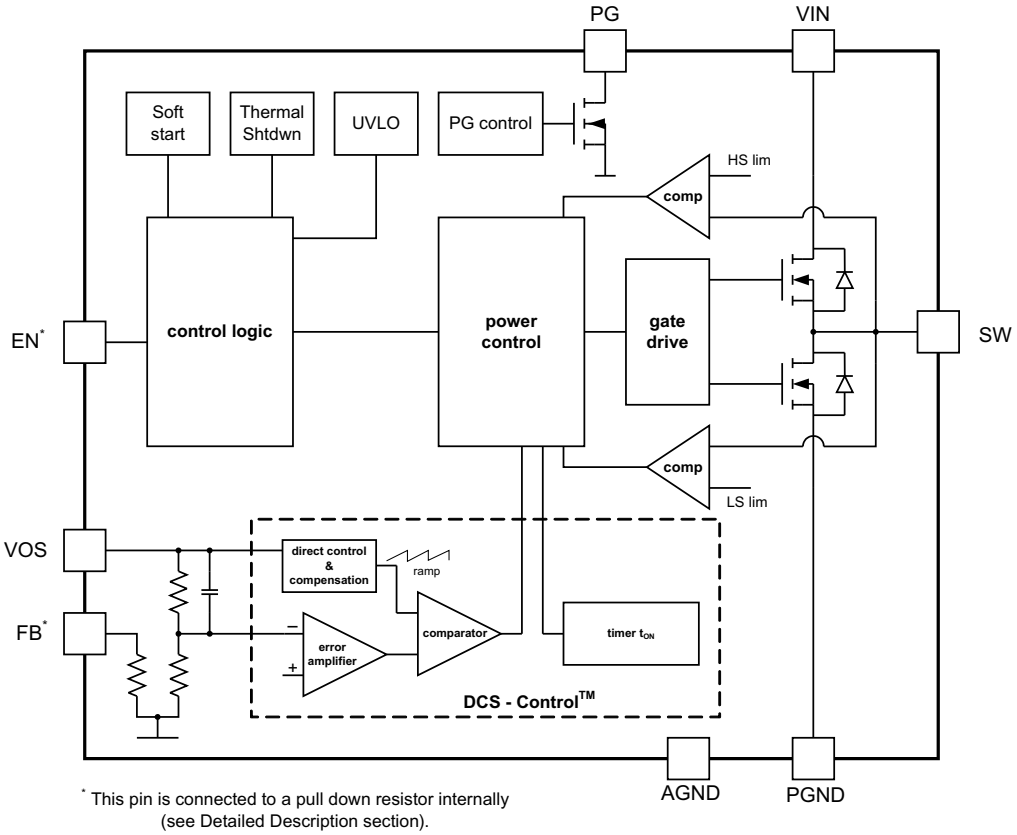

Figure 6. TPS62171/TPS62172/TPS62173 (Fixed Output Voltage)

8.3 Feature Description

8.3.1 Enable and Shutdown (EN)

When enable (EN) is set high, the device starts operation.

Shutdown is forced if EN is pulled low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin is low, an internal pull-down resistor of about 400 kΩ is connected and keeps it low, to avoid bouncing.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Current Limit and Short Circuit Protection

The TPS6217x devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot-through current, the low-side FET is switched on to allow the inductor current to decrease. The high-side FET turns on again, only if the current in the low-side FET decreases below the low-side current limit threshold of typically 0.7A.

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:

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Feature Description (continued)

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in *Electrical Characteristics*
- L is the inductor value
- V_L is the voltage across the inductor
- t_{PD} is the internal propagation delay (1)

The dynamic high-side switch peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (2)$$

Take care with the current limit, if the input voltage is high and very small inductances are used.

8.3.3 Power Good (PG)

The TPS6217x has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown. If not used, the PG pin should be connected to GND but may be left floating.

Table 1. Power Good Pin Logic Table

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{SD}$	√	
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

8.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180 mV.

8.3.5 Thermal Shutdown

The junction temperature (T_j) of the device is monitored by an internal temperature sensor. If T_j exceeds 160°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When T_j decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

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8.4 Device Functional Modes

8.4.1 Soft Start

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and V_{OUT} rises with a slope of about 25 mV/µs. See Figure 30 and Figure 31 for typical startup operation.

The TPS6217x can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

8.4.2 Pulse Width Modulation (PWM) Operation

The TPS6217x operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

8.4.3 Power Save Mode Operation

The TPS6217x's built in power save mode is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of power save mode happens within the entire regulation scheme and is seamless in both directions.

TPS6217x includes a fixed on-time circuitry. This on-time, in steady-state operation, is estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 420ns \tag{3}$$

For very small output voltages, the on-time increases beyond the result of Equation 3, to stay above an absolute minimum on-time, $t_{ON(min)}$, which is around 80 ns, to limit switching losses. The peak inductor current in PSM is approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{4}$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS6217x does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by $D = V_{OUT}/V_{IN}$ and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, such as for the longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

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Device Functional Modes (continued)

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (5)$$

where

- I_{OUT} is the output current
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET
- R_L is the DC resistance of the inductor used

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6217x device family are easy to use synchronous step-down DC-DC converters optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology. With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. It supports up to 0.5-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

9.2 Typical Application

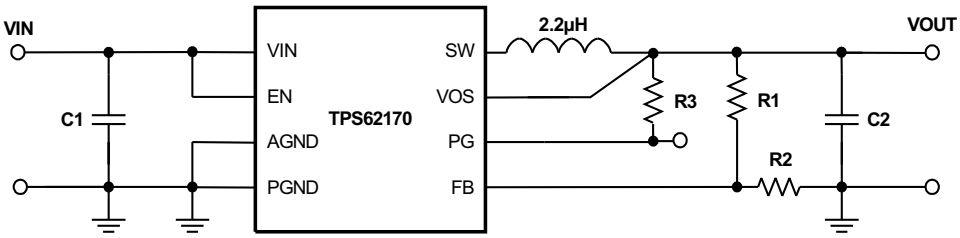

Figure 7. TPS62170 Adjustable Power Supply

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the Recommended Operating Conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS62170 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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Typical Application (continued)

9.2.2.2 Programming the Output Voltage

While the output voltage of the TPS62170 is adjustable, the TPS62171/TPS62172/TPS62173 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. it is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2 uA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (6)$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin to about 7.4 V.

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6217x is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability*). Table 2 can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 2. Recommended LC Output Filter Combinations(1)

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
1µH							
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.
(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in SLVA463.

9.2.2.3.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

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$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right)$$

where

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- L(min) is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency

(8)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. Table 3 lists inductors that are recommended for use with the TPS6217x.

Table 3. List of Inductors

Type	Inductance [µH]	Current [A](1)	Dimensions [L x B x H] mm	MANUFACTURER
VLF3012ST-2R2M1R4	2.2 µH, ±20%	1.9 A	3.0 x 2.8 x 1.2	TDK
VLF302512MT-2R2M	2.2 µH, ±20%	1.9 A	3.0 x 2.5 x 1.2	TDK
VLS252012-2R2	2.2 µH, ±20%	1.3 A	2.5 x 2.0 x 1.2	TDK
XFL3012-222MEC	2.2 µH, ±20%	1.9 A	3.0 x 3.0 x 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.6 A	3.0 x 3.0 x 1.2	Coilcraft
XPL2010-222MLC	2.2 µH, ±20%	1.3 A	1.9 x 2.0 x 1.0	Coilcraft
XPL2010-332MLC	3.3 µH, ±20%	1.1 A	1.9 x 2.0 x 1.0	Coilcraft
LPS3015-332ML	3.3 µH, ±20%	1.4 A	3.0 x 3.0 x 1.4	Coilcraft
PFL2512-222ME	2.2 µH, ±20%	1.0 A	2.8 x 2.3 x 1.2	Coilcraft
PFL2512-333ME	3.3 µH, ±20%	0.78 A	2.8 x 2.3 x 1.2	Coilcraft
744028003	3.3 µH, ±30%	1.0 A	2.8 x 2.8 x 1.1	Wuerth
PSI25201B-2R2MS	2.2 uH, ±20%	1.3 A	2.0 x 2.5 x 1.2	Cyntec
NR3015T-2R2M	2.2 uH, ±20%	1.5 A	3.0 x 3.0 x 1.5	Taiyo Yuden
BRC2012T2R2MD	2.2 µH, ±20%	1.0 A	2.0 x 1.25 x 1.4	Taiyo Yuden
BRC2012T3R3MD	3.3 µH, ±20%	0.87 A	2.0 x 1.25 x 1.4	Taiyo Yuden

(1) I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

TPS6217x can operate with an inductor as low as 2.2 µH. However, for applications running with low input voltages, 3.3 µH is recommended, to allow the full output current. The inductor value also determines the load current at which power save mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L$$

(9)

Using Equation 8, this current level is adjusted by changing the inductor value.

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9.2.2.4 Capacitor Selection

9.2.2.4.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS6217x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.4.2 Input Capacitor

For most applications, 10 µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to those pins.

NOTE

DC bias effect: High capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.5 Output Filter and Loop Stability

The devices of the TPS6217x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency calculated with Equation 10:

$$f_{LC} = \frac{1}{2\pi \sqrt{L \cdot C}} \tag{10}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which is affected. More information including a detailed L-C stability matrix is found in SLVA463.

The TPS6217x devices, both fixed and adjustable versions, include an internal 25 pF feed forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 11 and Equation 12:

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{11}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{12}$$

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Though the TPS6217x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289 and SLVA466.

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see **NOTE** in Capacitor selection section).

9.2.2.6 TPS6216x Components List

Table 4 shows the list of components for the *Application Curves*.

Table 4. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17 V, 0.5A Step-Down Converter, WSON	TPS62170DSG, Texas Instruments
L1	2.2 uH, 1.4 A, 3 mm x 2.8 mm x 1.2 mm	VLF3012ST-2R2M1R4, TDK
C1	10 µF, 25 V, Ceramic, 0805	Standard
C2	22 µF, 6.3 V, Ceramic, 0805	Standard
R1	depending on V_{OUT}	
R2	depending on V_{OUT}	
R3	100 kΩ, Chip, 0603, 1/16 W, 1%	Standard

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9.2.3 Application Curves

V_{IN} = 12V, V_{OUT} = 3.3V, T_A=25°C, (unless otherwise noted)

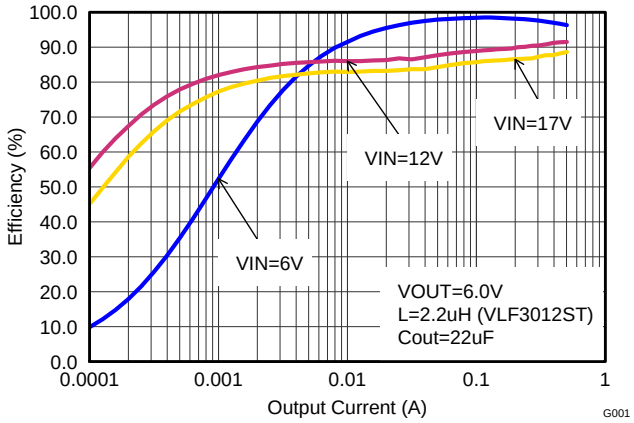

Figure 8. Efficiency vs Output Current, V_{OUT} = 6 V

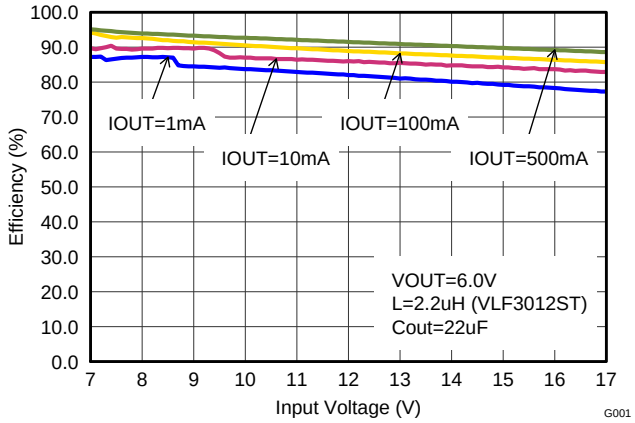

Figure 9. Efficiency vs Input Voltage, V_{OUT} = 6 V

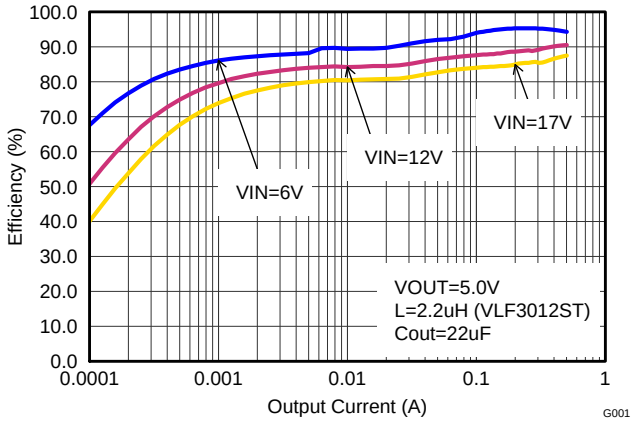

Figure 10. Efficiency vs Output Current, V_{OUT} = 5 V

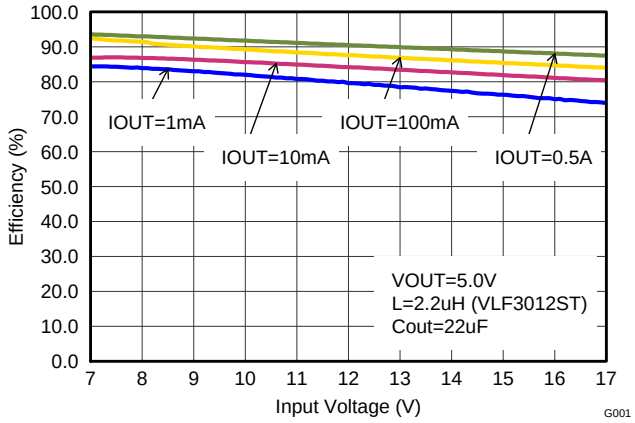

Figure 11. Efficiency vs Input Voltage, V_{OUT} = 5 V

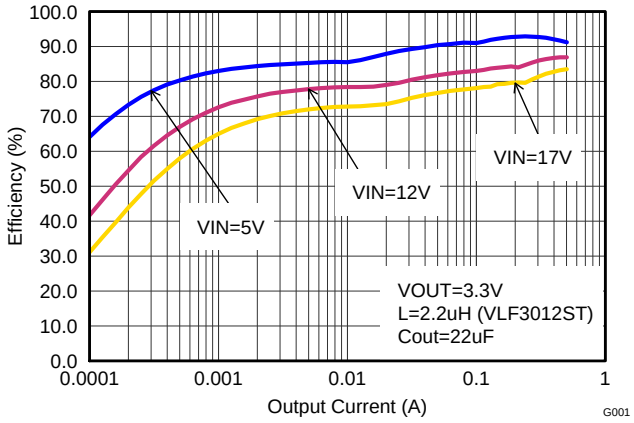

Figure 12. Efficiency vs Output Current, V_{OUT} = 3.3 V

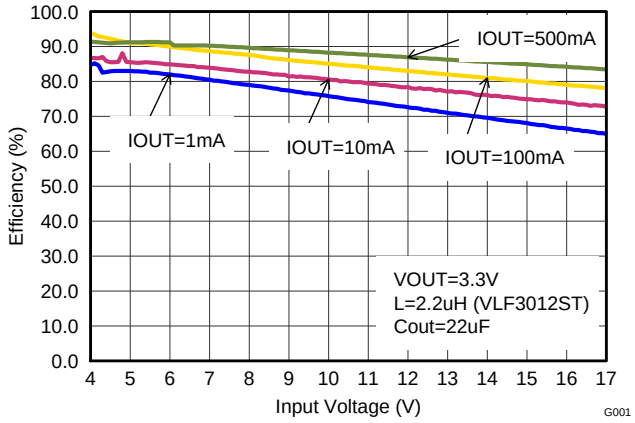

Figure 13. Efficiency vs Input Voltage, V_{OUT} = 3.3 V

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V_{IN} = 12V, V_{OUT} = 3.3V, T_A=25°C, (unless otherwise noted)

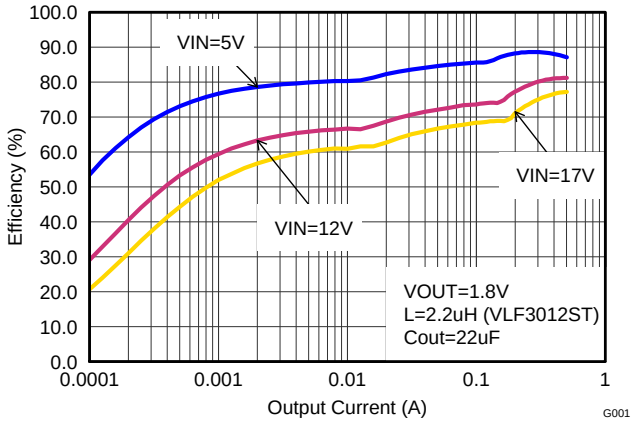

Figure 14. Efficiency vs Output Current, V_{OUT} = 1.8 V

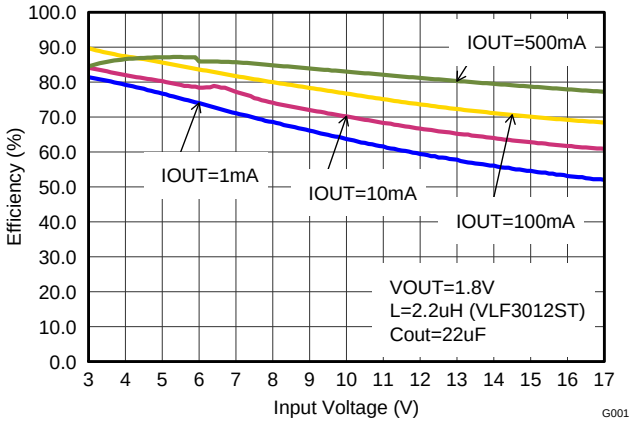

Figure 15. Efficiency vs Input Voltage, V_{OUT} = 1.8 V

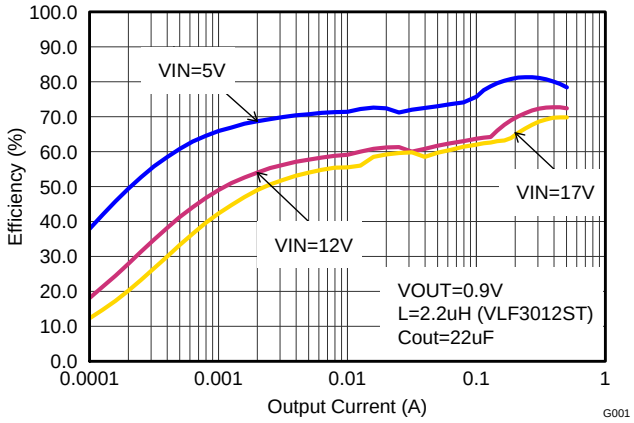

Figure 16. Efficiency vs Output Current, V_{OUT} = 0.9 V

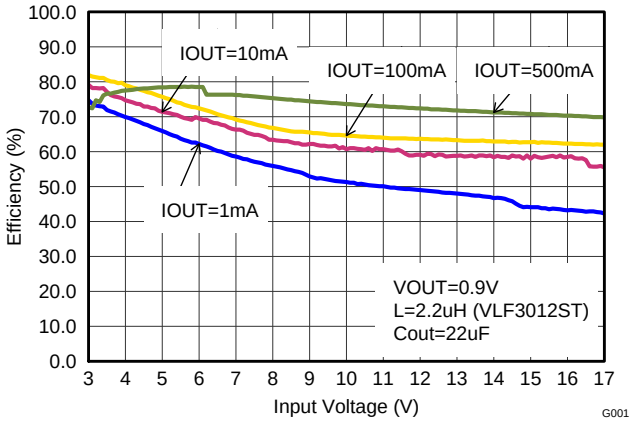

Figure 17. Efficiency vs Input Voltage, V_{OUT} = 0.9 V

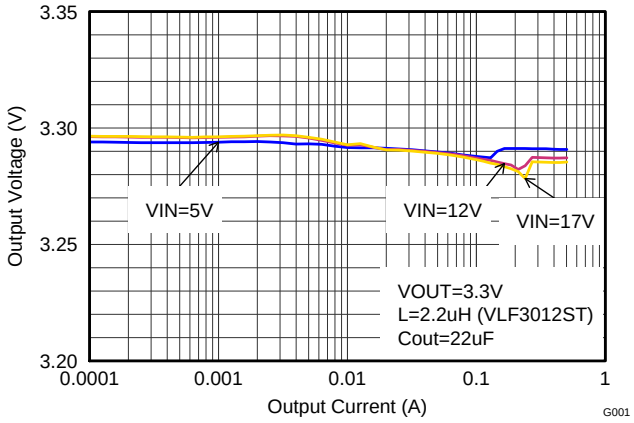

Figure 18. Output Voltage Accuracy (Load Regulation)

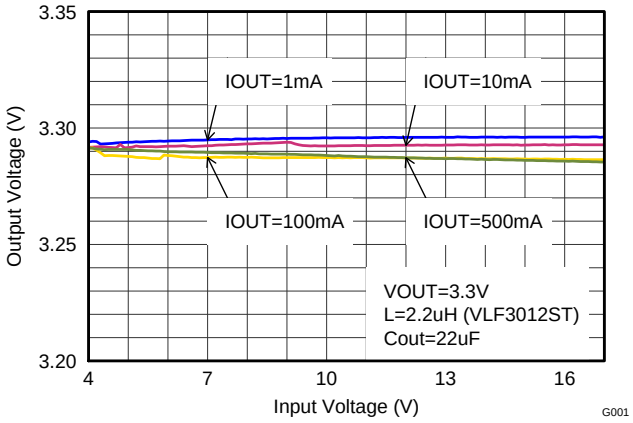

Figure 19. Output Voltage Accuracy (Line Regulation)

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V_{IN} = 12V, V_{OUT} = 3.3V, T_A=25°C, (unless otherwise noted)

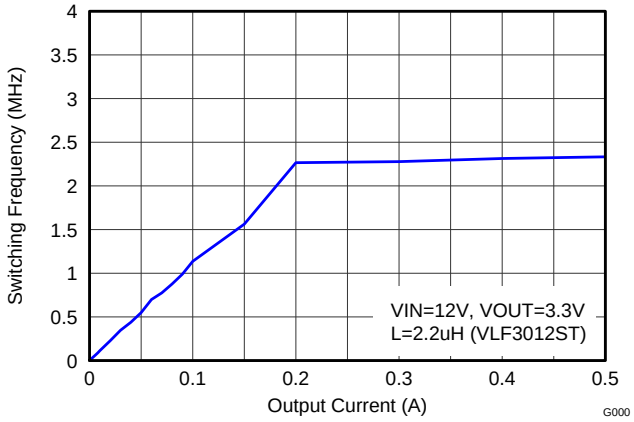

Figure 20. Switching Frequency vs Output Current

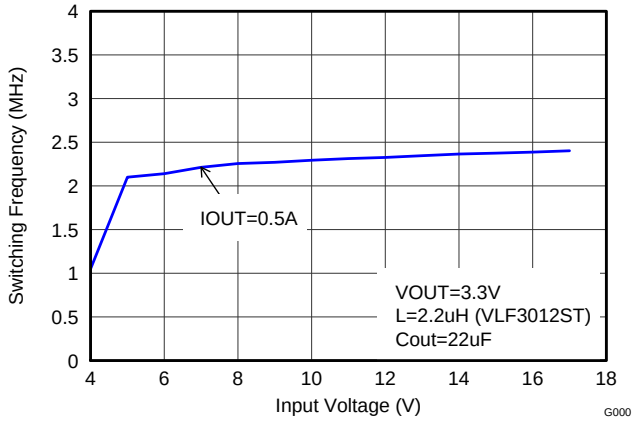

Figure 21. Switching Frequency vs Input Voltage

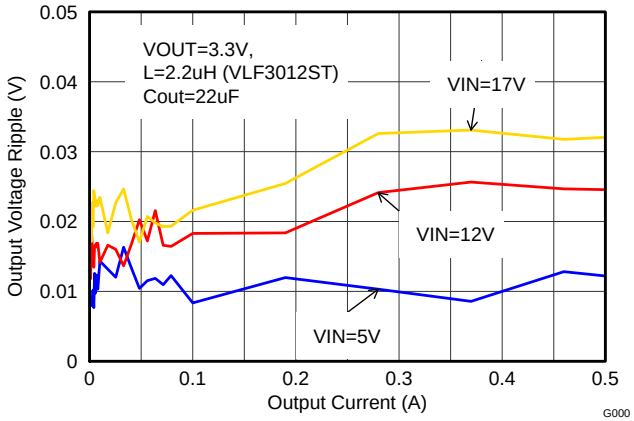

Figure 22. Output Voltage Ripple

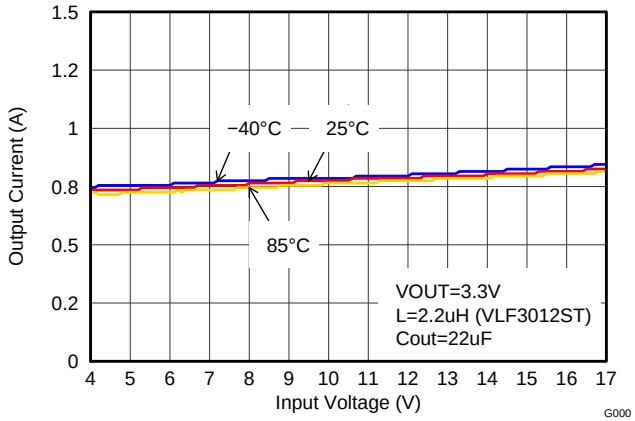

Figure 23. Maximum Output Current

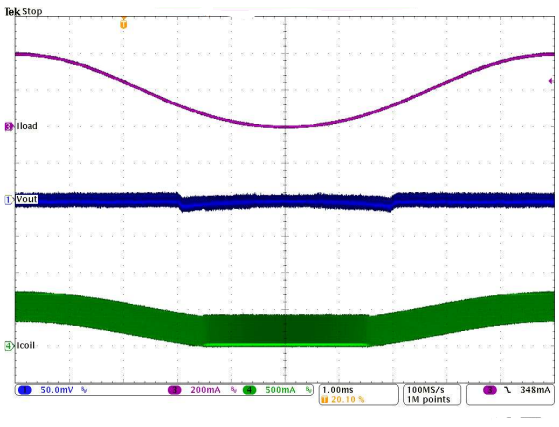

Figure 24. PWM to PSM Mode Transition

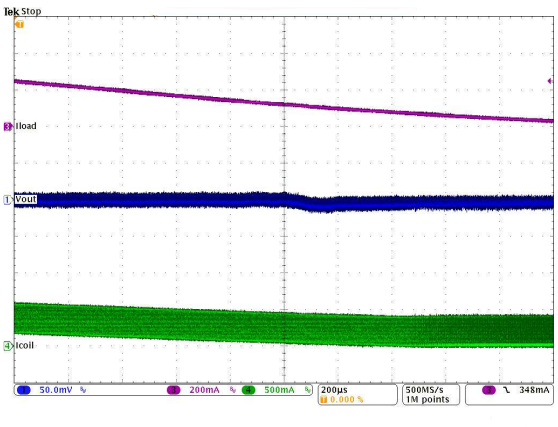

Figure 25. PSM to PWM Mode Transition

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V_{IN} = 12V, V_{OUT} = 3.3V, T_A=25°C, (unless otherwise noted)

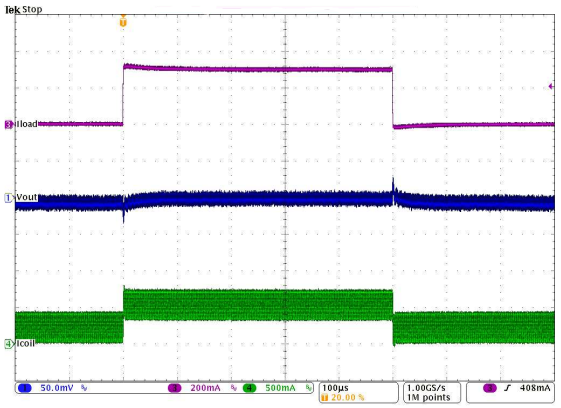

Figure 26. Load Transient Response in PWM Mode (200 mA to 500 mA)

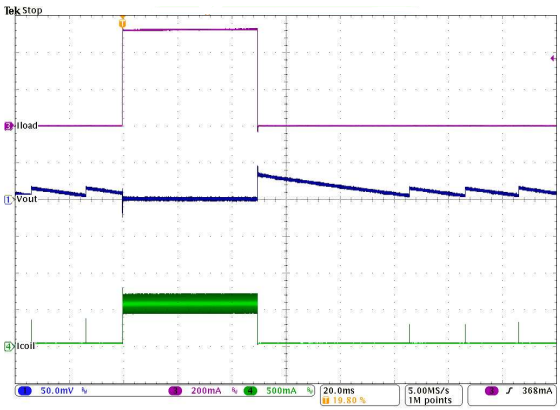

Figure 27. Load Transient Response from Power Save Mode (100 mA to 500 mA)

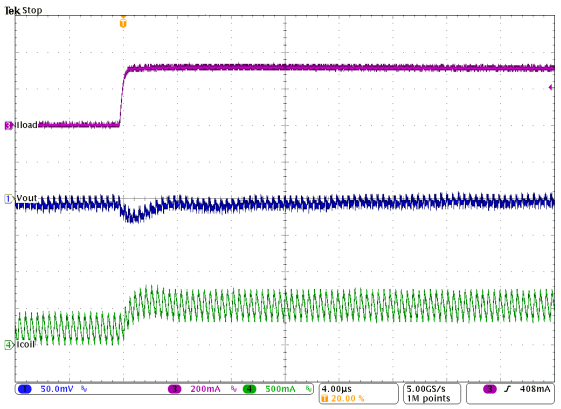

Figure 28. Load Transient Response in PWM Mode (200 mA to 500 mA), Rising Edge

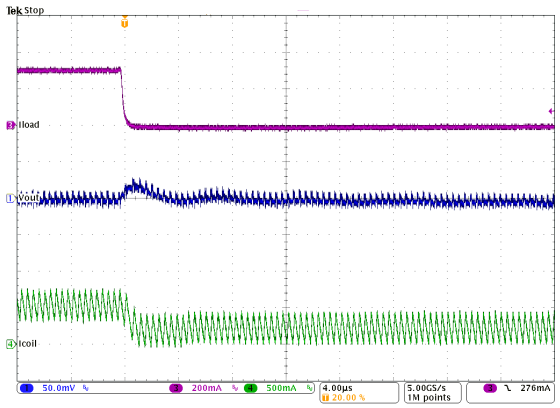

Figure 29. Load Transient Response in PWM Mode (200 mA to 500 mA), Falling Edge

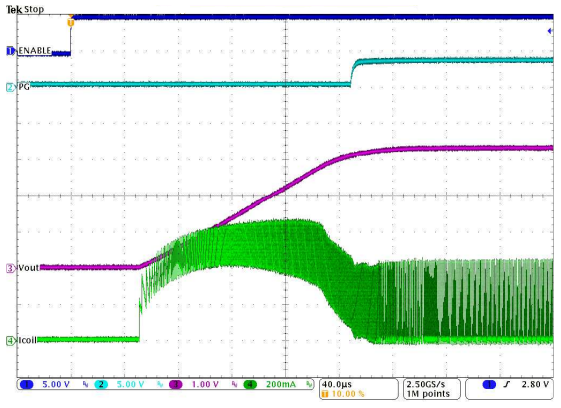

Figure 30. Startup with I_{OUT} = 500 mA, V_{OUT} = 3.3 V

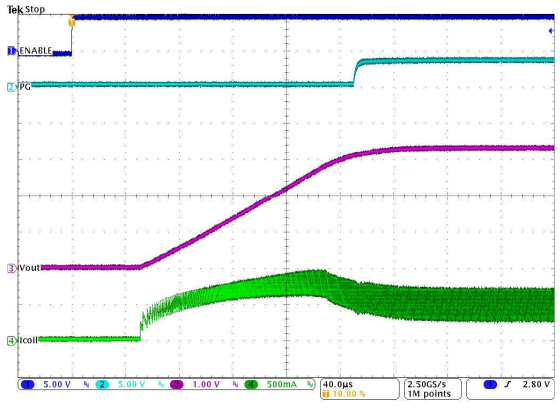

Figure 31. Startup with I_{OUT} = 500 mA, V_{OUT} = 3.3 V

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V_{IN} = 12V, V_{OUT} = 3.3V, T_A=25°C, (unless otherwise noted)

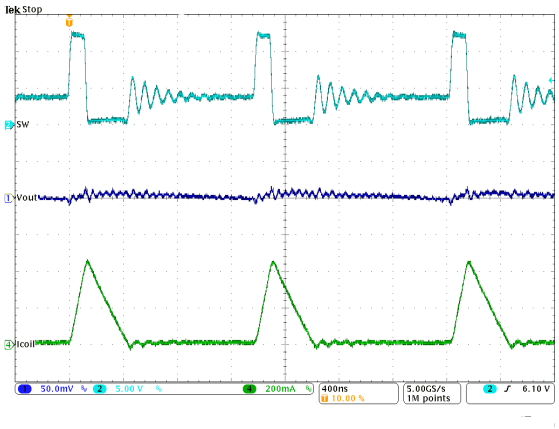

Figure 32. Typical Operation in Power Save Mode (I_{OUT} = 66 mA)

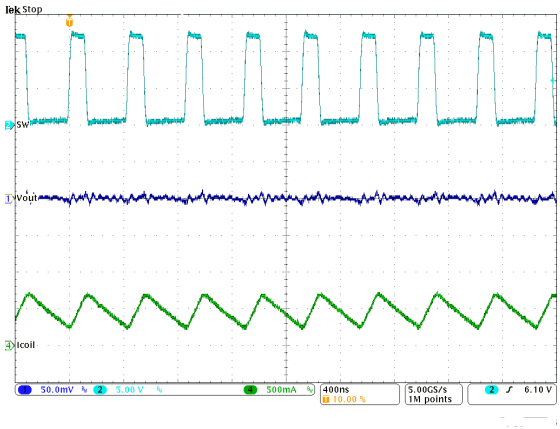

Figure 33. Typical Operation in PWM mode (I_{OUT} = 500 mA)

9.3 System Examples

Figure 34 through Figure 40 show various TPS6217x devices and input voltages that provide a 0.5-A power supply with output voltage options.

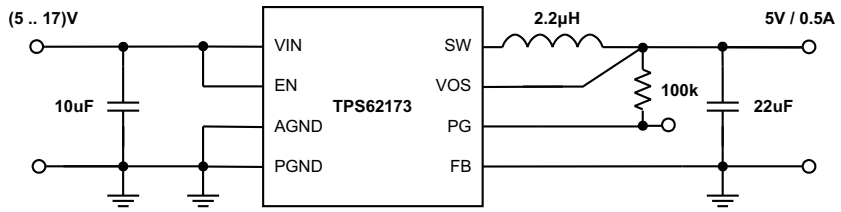

Figure 34. 5-V and 0.5-A Power Supply

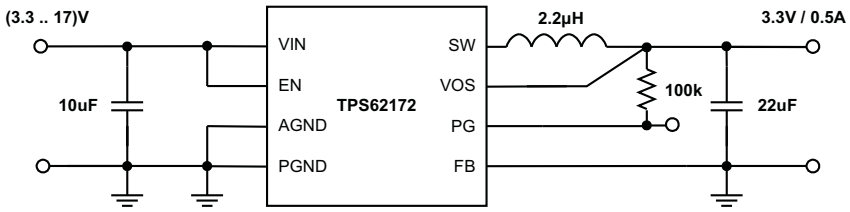

Figure 35. 3.3-V and 0.5-A Power Supply

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System Examples (continued)

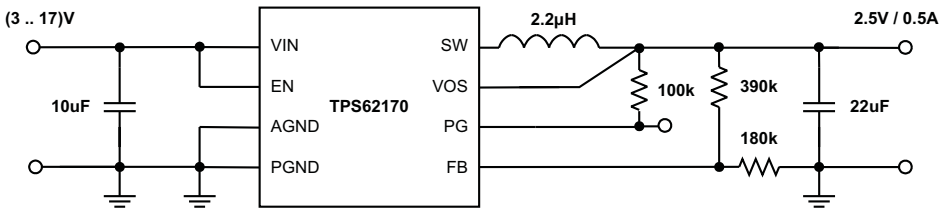

Figure 36. 2.5-V and 0.5-A Power Supply

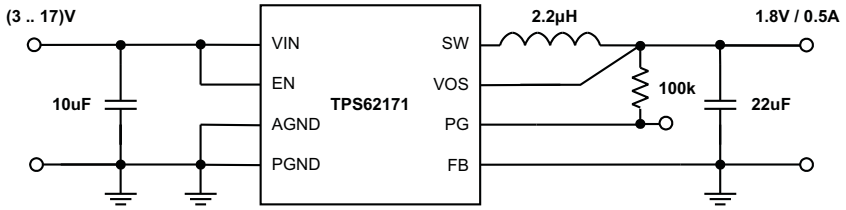

Figure 37. 1.8-V and 0.5-A Power Supply

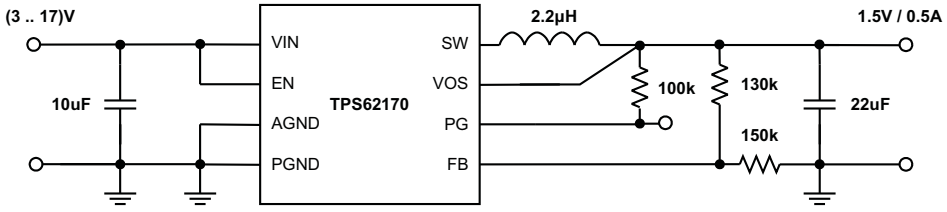

Figure 38. 1.5-V and 0.5-A Power Supply

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System Examples (continued)

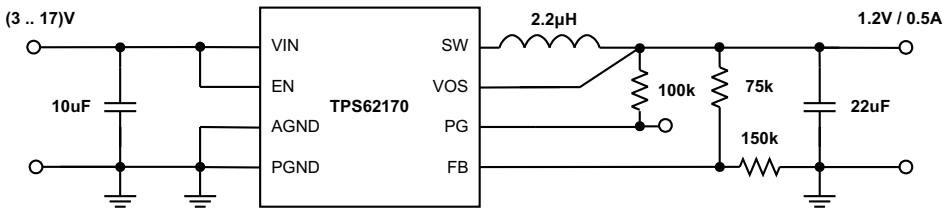

Figure 39. 1.2-V and 0.5-A Power Supply

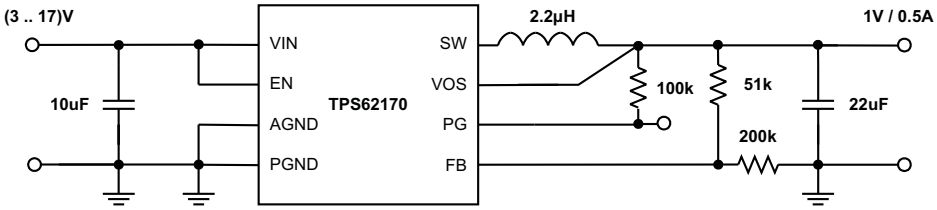

Figure 40. 1-V and 0.5-A Power Supply

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System Examples (continued)

9.3.1 Inverting Power Supply

The TPS6217x can be used as inverting power supply by rearranging external circuitry as shown in Figure 41. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17 V (see Equation 13).

$$V_{IN} + |V_{OUT}| \le V_{IN\,max} \tag{13}$$

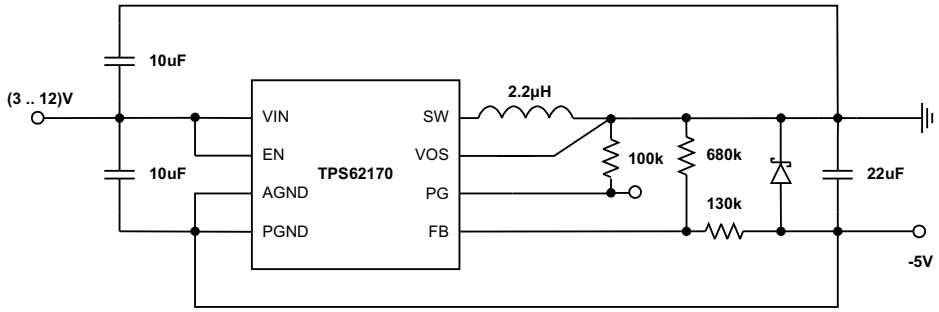

Figure 41. –5-V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a right half plane zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in SLVA469.

10 Power Supply Recommendations

The TPS6217x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6217x.

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11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6217x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

Provide low inductive and resistive paths to ground for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Also sensitive nodes like FB and VOS should be connected with short wires, not nearby high dv/dt signals (such as SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission (such as the feedback divider) should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the VIN and PGND pin of the IC. This connections should be done with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. The feedback resistors, R_1 and R_2, should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and even more to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load.

A single point grounding scheme should be implemented with all grounds (AGND, PGND and the thermal pad) connecting at the IC's exposed thermal pad. See Figure 42 for the recommended layout of the TPS6217x. More detailed information can be found in the EVM Users Guide, SLVU483.

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the exposed thermal pad can be connected to a floating circuit board trace, the device has better thermal performance if it is connected to a larger ground plane. The exposed thermal pad is electrically connected to AGND.

11.2 Layout Example

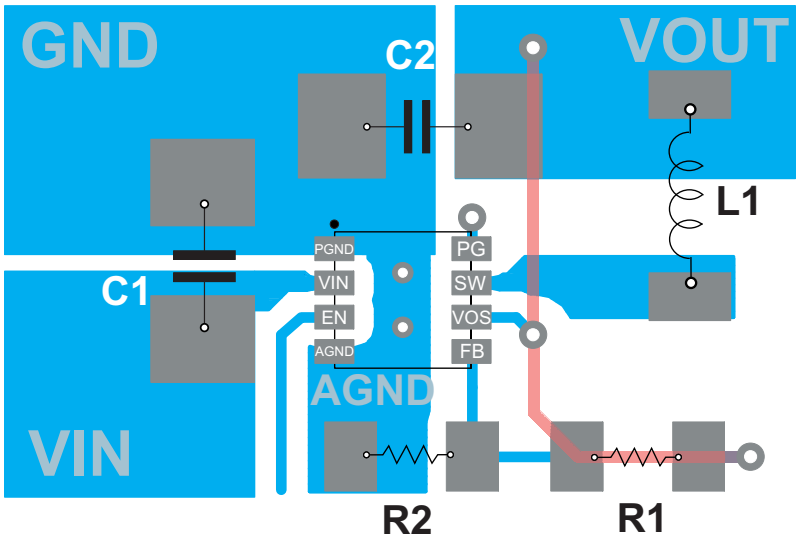

Figure 42. Layout Example

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11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note SZZA017, and SPRA953.

The TPS6217x is designed for a maximum operating junction temperature (T_j) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it is recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.1.2 開発サポート

12.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPS6217xデバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください:

- *『TPS62160 3V～17V 1A降圧型コンバータ、DCS-Control™搭載』*、TPS62160
- *『TPS62125 3V～17V、300mA降圧コンバータ、可変イネーブル・スレッショルドおよびヒステリシス』*、TPS62125
- *『TPS62130/40/50/60/70の出力フィルタの最適化』*、SLVA463
- *『内部的に補正される、フィードフォワード・コンデンサを持つDC/DCコンバータの過渡応答の最適化』*、SLVA289
- *『フィードフォワード・コンデンサを使用してTPS62130/40/50/60/70の安定性と帯域幅を改善する方法』*、SLVA466
- *『反転昇降圧トポロジでのTPS6215xの使用』*、SLVA469
- *『TPS62160EVMおよびTPS62170EVM-627評価モジュール』*、SLVU483
- *『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』*、SZZA017

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS62170	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62171	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62172	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62173	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.5 商標

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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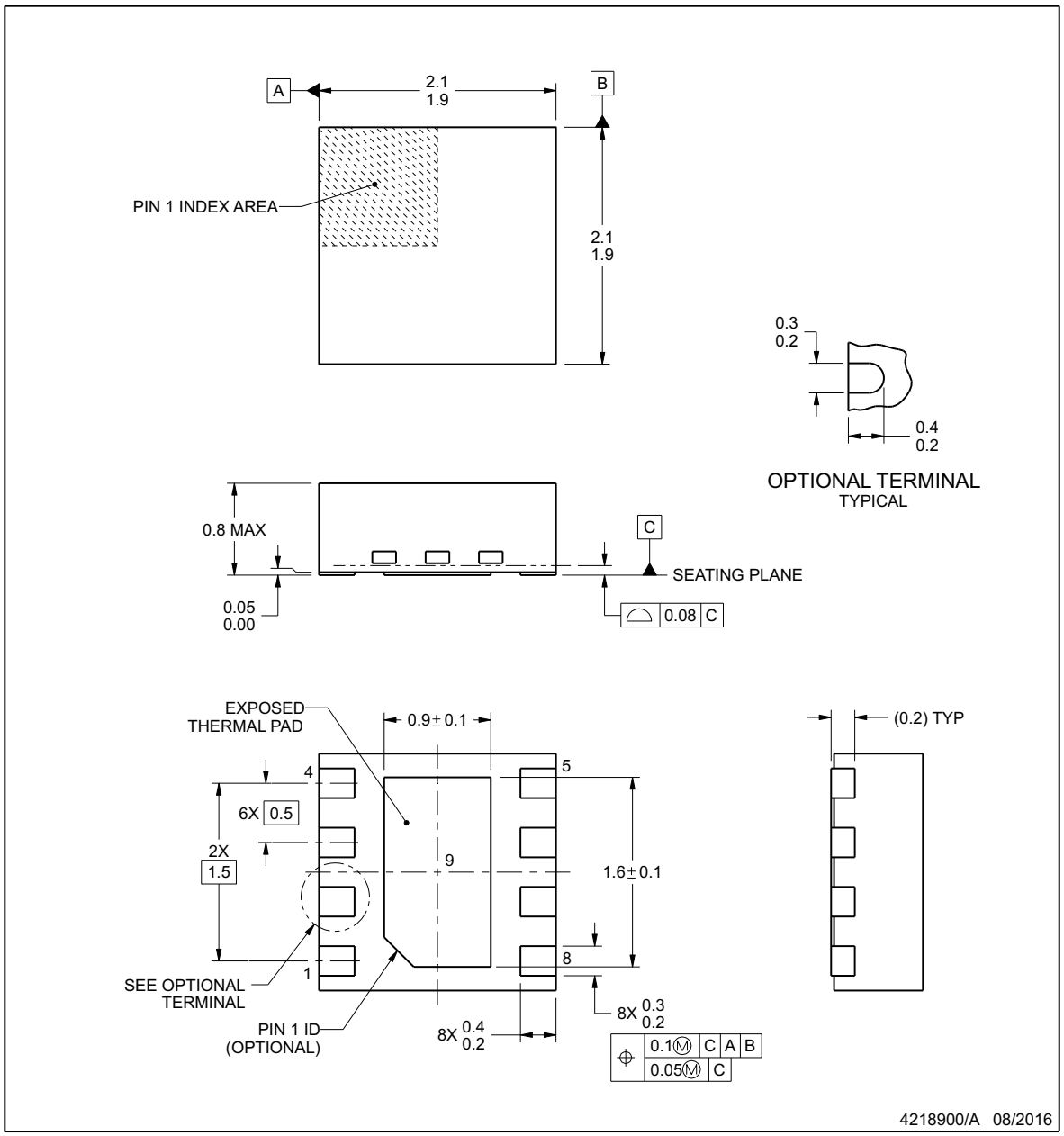
PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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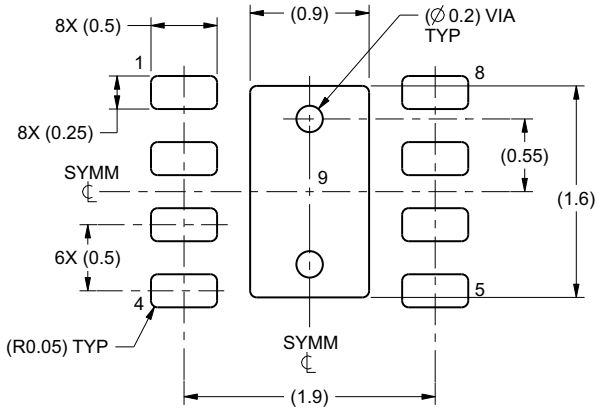
EXAMPLE BOARD LAYOUT

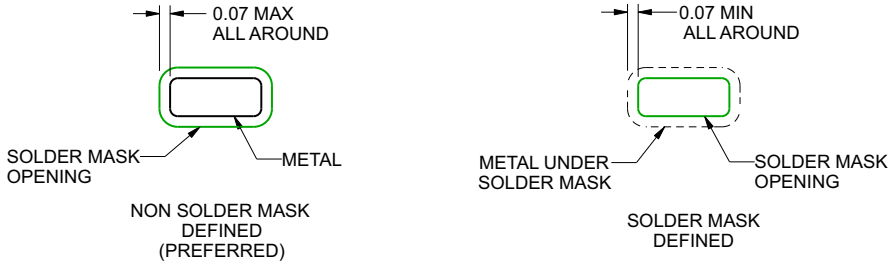
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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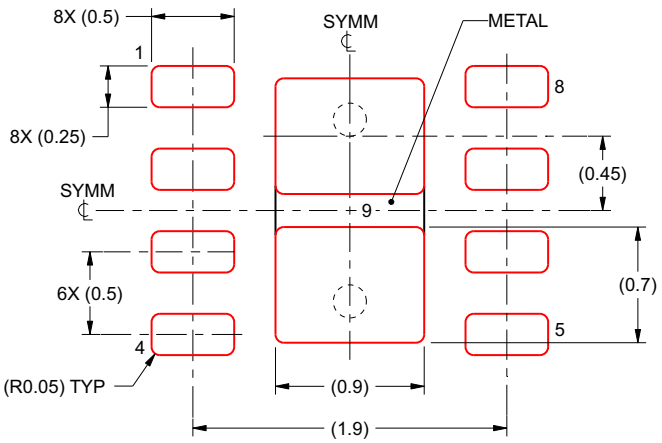
EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62170DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62170DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE
TPS62171DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUF
TPS62171DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUF
TPS62171DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUF
TPS62171DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUF
TPS62172DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG
TPS62172DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG
TPS62172DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG
TPS62172DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG
TPS62172DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	QUG
TPS62172DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG
TPS62173DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH
TPS62173DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH
TPS62173DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH
TPS62173DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH
TPS62173DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH
TPS62173DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62170, TPS62171, TPS62172 :

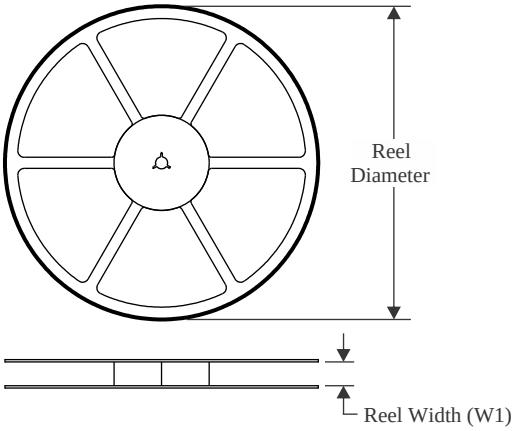
- Automotive : TPS62170-Q1, TPS62171-Q1, TPS62172-Q1

NOTE: Qualified Version Definitions:

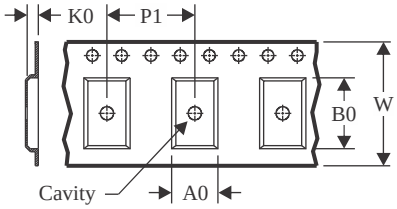
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

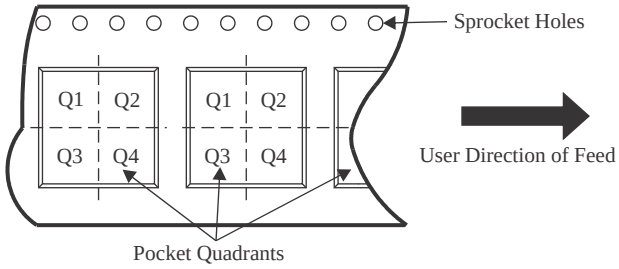


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

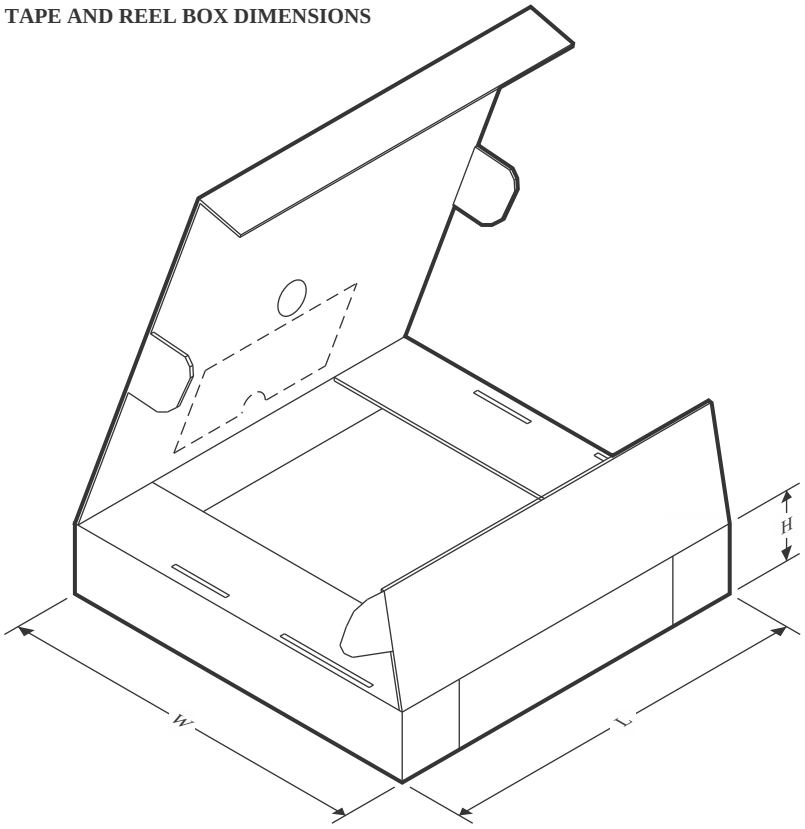
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62170DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62170DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62170DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62170DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62170DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62171DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62171DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62173DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62173DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62173DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62173DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62173DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62170DSGR	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62170DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62170DSGRG4	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62170DSGT	WSON	DSG	8	250	213.0	191.0	35.0
TPS62170DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62171DSGR	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62171DSGT	WSON	DSG	8	250	213.0	191.0	35.0
TPS62172DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62172DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62172DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62173DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62173DSGR	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62173DSGRG4	WSON	DSG	8	3000	213.0	191.0	35.0
TPS62173DSGT	WSON	DSG	8	250	213.0	191.0	35.0
TPS62173DSGT	WSON	DSG	8	250	205.0	200.0	33.0

GENERIC PACKAGE VIEW

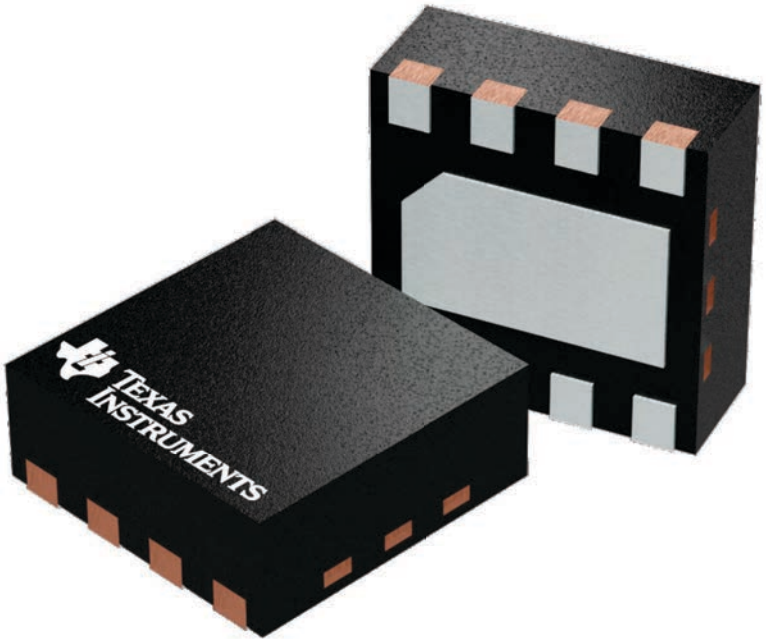
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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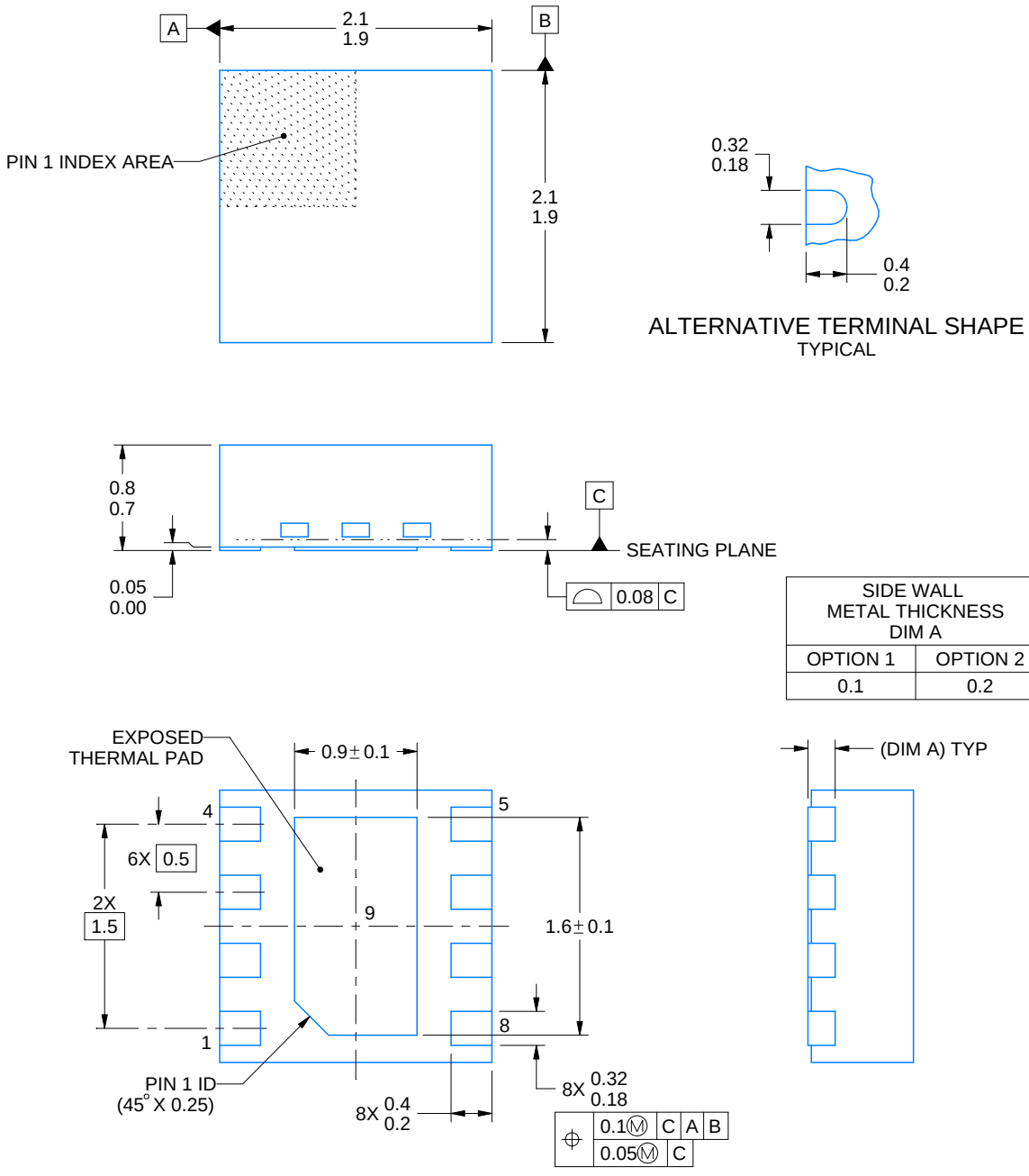
PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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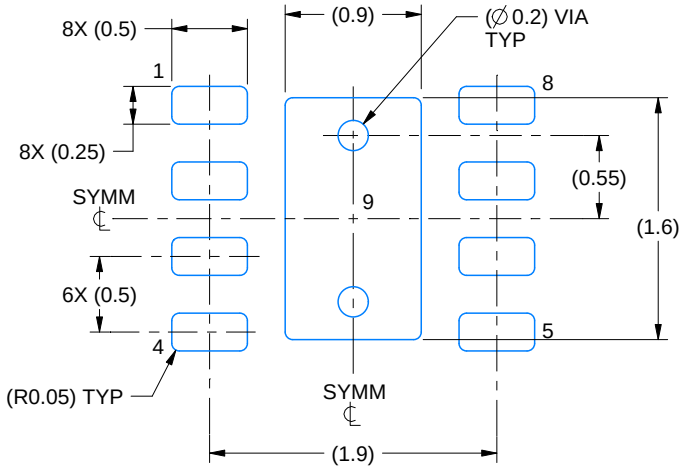
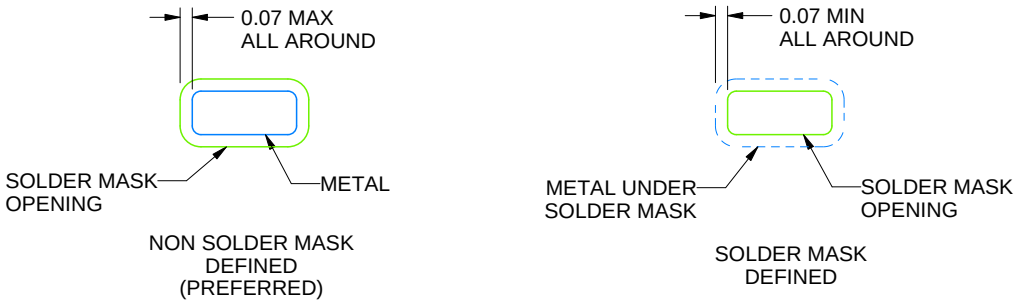
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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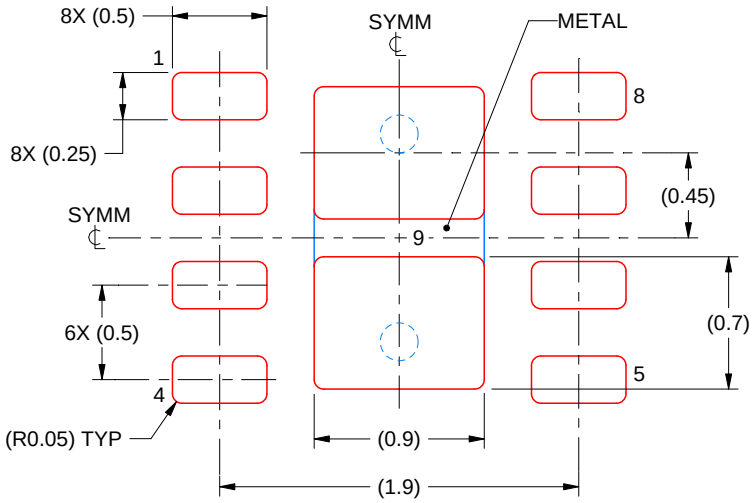
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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