TEXAS INSTRUMENTS

TPS62561
TPS62560, TPS62562

JAJS360D – JANUARY 2008 – REVISED OCTOBER 2016

TPS6256x 2.25MHz、600mA降圧型コンバータ、TSOTおよび2×2×0.8mm QFNパッケージ

1 特長

- 出力電流: 最大600mA
- 入力電圧範囲: 2.5V～5.5V
- PWMモード時の出力電圧精度±2.5%
- 静止電流: 15μA(標準値)
- 100%デューティ・サイクル動作により低いドロップアウト電圧を実現
- ソフト・スタート
- 小型のSOTおよび2mm×2mm×0.8mmのSONパッケージで供給
- 改良された機能セットについては、TPS62290デバイス(SLVS764)を参照してください。

2 アプリケーション

- PDA、Pocket PC、ポータブル・メディア・プレーヤー
- 低電力DSP電源
- ポイント・オブ・ロード(POL)アプリケーション

3 概要

TPS62560デバイスは、高効率の同期整流降圧型コンバータであり、電池式のポータブル・アプリケーションに最適です。単一のLiイオン電池や他のよく使われる単3および単4電池などから、最大600mAの電流を供給します。

入力電圧範囲が2.5～5.5Vのこのデバイスは、広範囲にわたる携帯用機器またはPOLアプリケーションへの電源供給を目的としています。

TPS62560ファミリーは、2.25MHzの固定スイッチング周波数で動作し、軽負荷電流時にはパワーセーブ・モードに自動的に切り替わり、広い負荷電流範囲にわたって高効率を維持します。

パワーセーブ・モードは、低出力電圧リップルに最適化されています。さらに低ノイズが要求されるアプリケーションの場合、本デバイスはMODEピンをHighにすることで、強制的に固定周波数PWMモードにすることができます。シャットダウン・モードでは、消費電流が1μA未満に低減します。TPS62560では、小型のインダクタとコンデンサを使用して、ソリューション・サイズを小さくすることができます。

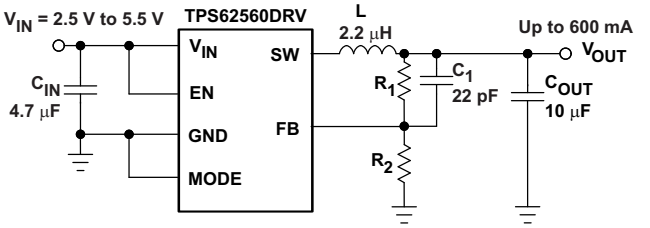
TPS62560とTPS62562は、6ピンの2mm×2mm SONパッケージ、TPS62561は5ピンのSOTパッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS62560、TPS62562	SON (6)	2.00mm×2.00mm
TPS62561	SOT (5)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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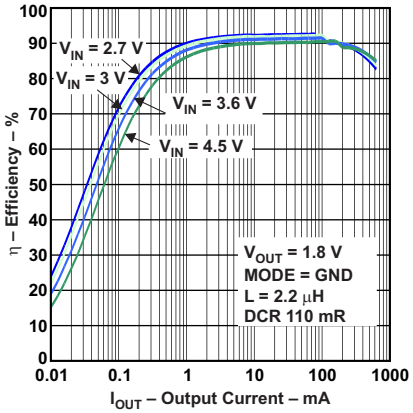
効率と出力電流との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (December 2009) から Revision D に変更 **Page**

- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 ... 1
- *注文情報*の表を削除 ... 1
- テキスト文字列を「最大1000mAの出力電流」から「最大600mAの出力電流」に(「概要」) 変更 ... 1
- Corrected typographical errors in Figure 32; from "V_{IN}= 2 V to 6 V" to "V_{IN} = 2.5 V to 5.5 V" ... 18

Revision B (March 2009) から Revision C に変更 **Page**

- 高効率降圧型コンバータ 削除 ... 1
- 「特長」の箇条書きの「広範な」 削除 ... 1
- 「特長」の「拡張電圧レンジ付きLiイオン電池の」 削除 ... 1
- 「特長」の「調整可能および固定の出力電圧オプション」 削除 ... 1
- 「特長」の「2.25MHz固定周波数動作」 削除 ... 1
- 「特長」の「軽負荷電流時のパワーセーブ・モード」 削除 ... 1
- 「特長」の「軽負荷電流時の電圧ポジショニング」 削除 ... 1
- 「特長」の「1mm未満のソリューション高が可能に」 削除 ... 1
- デバイスの機能およびTPS62260との相違点の詳細 変更 ... 1

Revision A (July 2008) から Revision B に変更 **Page**

- TPS62562デバイスの番号を 追加 ... 1

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2008年1月発行のものから更新 **Page**

- 全レベルで変更。リビジョンAは本データシート全体の書き換えによって 変更 1

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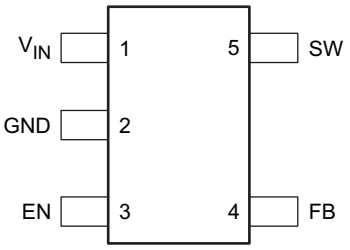
5 Device Comparison Table

Part Number	Package	Mode Pin	Output Voltage(1)	Device Marking(2)
TPS62560	SON (6)	yes	Adjustable	CEY
TPS62561	SOT (5)	forced PWM only	Adjustable	CVO
TPS62562	SON (6)	yes	1.8 V fixed	NXT

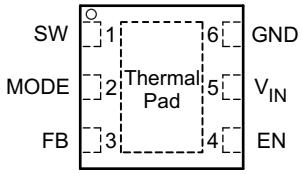
(1) Contact TI for other fixed output voltage options
(2) For the most current package and ordering information, see *メカニカル、パッケージ、および注文情報*, or see the TI website at www.ti.com

6 Pin Configuration and Functions

DDC Package
5-Pin SOT
Top View



DRV Package
6-Pin SON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	No. QFN-6	No. TSOT23-5		
EN	4	3	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
FB	3	4	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In the fixed-output-voltage option, connect this terminal directly to the output capacitor.
GND	6	2	—	GND supply pin
MODE	2	N/A	I	This pin is only available as a QFN package option. MODE pin = high forces the device to operate in the fixed-frequency PWM mode. MODE pin = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
SW	1	5	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this pin and the output capacitor.
V_{IN}	5	1	—	V_{IN} power-supply pin
Exposed Thermal Pad	—	N/A	—	Must be soldered to achieve appropriate power dissipation. Should be connected to GND.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Input voltage range(2)	–0.3	7	V
	Voltage range at EN, MODE	–0.3	V_{IN} +0.3, ≤ 7	
	Voltage on SW	–0.3	7	
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
		Machine model	±200	

(1) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal. The machine model is a 200-pF capacitor discharged directly into each terminal.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply voltage	2.5	5.5	V
V_{OUT}	Output voltage range for adjustable voltage	0.85	V_{IN}	V
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS62560, TPS62562	TPS62561	UNIT
		DRV (SON)	DDC (SOT)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	226.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.6	48.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_{OUT}	Output current	V_{IN} 2.5 V to 5.5 V			600	mA
I_Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND), device not switching		15		µA
		I_{OUT} = 0 mA, PFM mode enabled (MODE = GND), device switching, V_{OUT} = 1.8 V, See (1)		18.5		
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}), PWM operation, V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.5		µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High-level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 5.5 V	1		V_{IN}	V
V_{IL}	Low-level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		252	492	mΩ
	Low side MOSFET on-resistance			194	391	
I_{LIMF}	Forward current limit, high and low side MOSFET	V_{IN} = V_{GS} = 3.6 V	0.8	1	1.2	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal-shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 5.5 V		2.25		MHz
OUTPUT						
V_{OUT}	Adjustable-output voltage range		0.85		V_{IN}	V
V_{OUT}	TPS62562 fixed output voltage	V_{IN} ≥ 1.8 V		1.8		V
V_{ref}	Reference voltage			600		mV
V_{FB}	Feedback voltage, PWM mode	MODE = V_{IN}, PWM operation, for fixed-output-voltage versions V_{FB} = V_{OUT}, 2.5 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 600 mA (2)	–2.5%	0%	2.5%	
	Feedback voltage, PFM mode	MODE = GND, device in PFM mode, voltage positioning active (1)		1%		
	Load regulation	PWM mode		–1		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW terminal	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND (3)		0.5	1	µA

(1) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the section.
(2) For V_{IN} = V_{OUT} + 0.6 V
(3) In fixed-output-voltage versions, the internal resistor divider network is disconnected from the FB terminal.

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7.6 Typical Characteristics

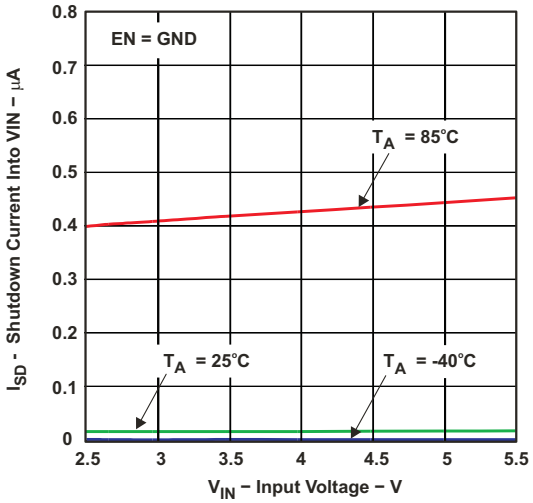

Figure 1. Shutdown Current into VIN vs Input Voltage

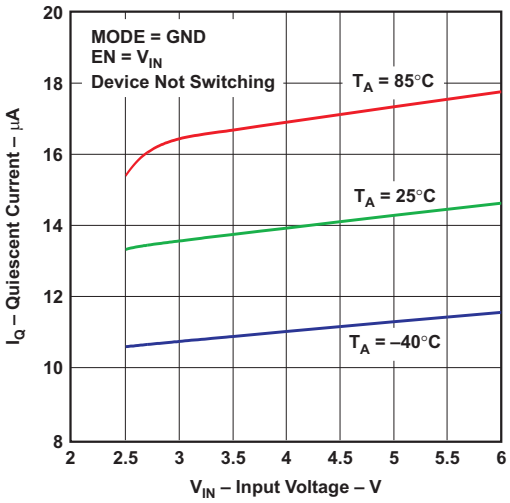

Figure 2. Quiescent Current vs Input Voltage

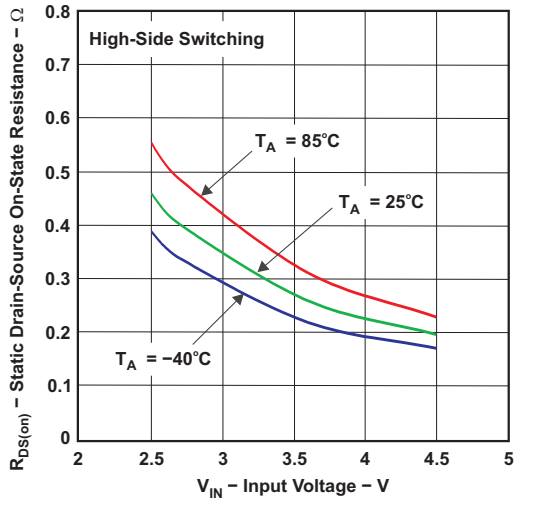

Figure 3. Static Drain-Source ON-State Resistance

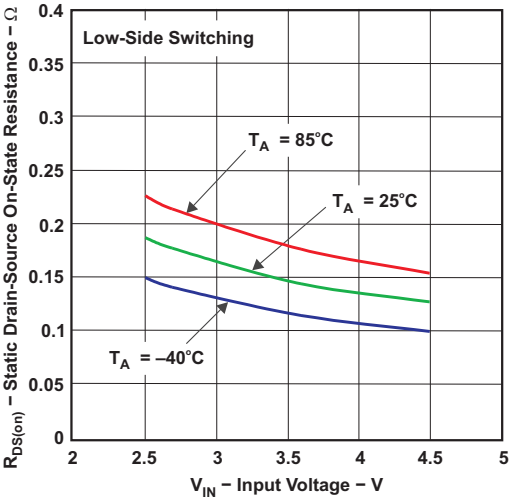

Figure 4. Static Drain-Source ON-State Resistance vs Input Voltage

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8 Detailed Description

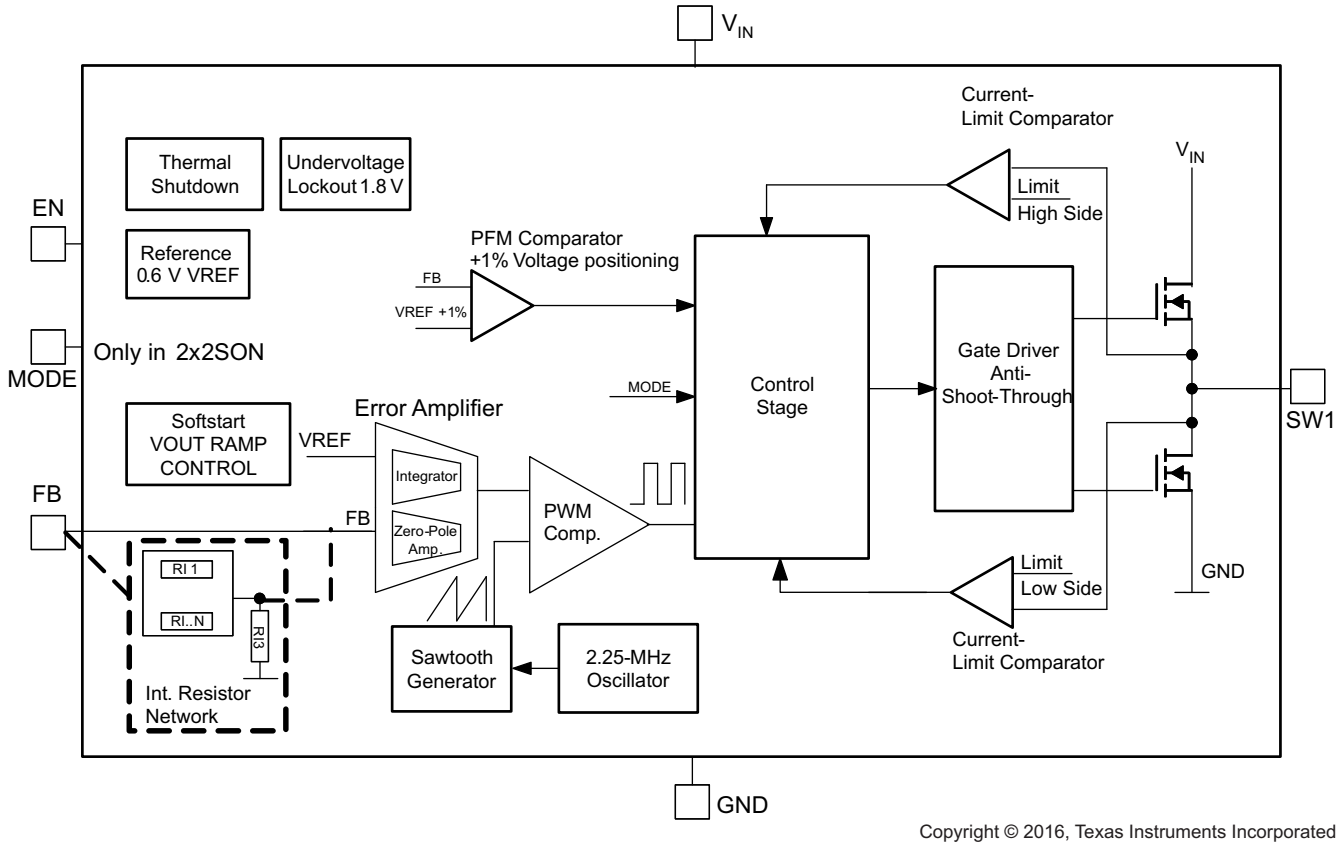
8.1 Overview

The TPS62560/62 step-down converters operate with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode, and then operates in PFM mode. However, the TPS62561 operates with fixed-frequency PWM only, also at light load conditions.

During PWM operation, the converter uses a unique fast-response voltage-mode control scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time, which prevents shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the on the high-side MOSFET switch.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in power-save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

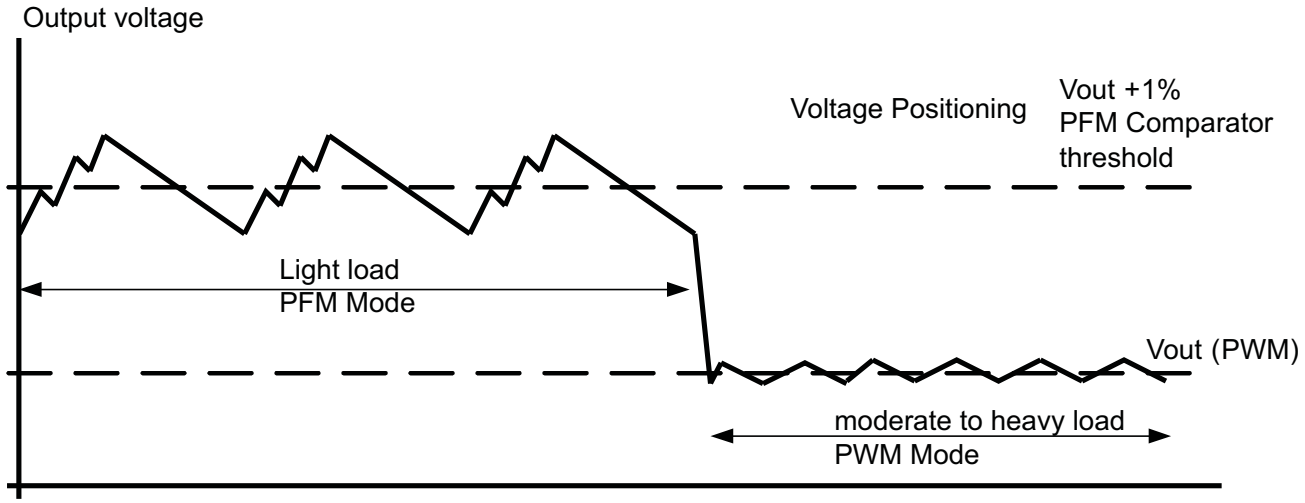

Figure 5. Power Save Mode Operation With Automatic Mode Transition

8.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

8.3.3 Mode Selection

The MODE terminal allows mode selection between forced-PWM mode and power-save mode.

Connecting this terminal to GND enables the power-save mode with automatic transition between PWM and PFM modes. Pulling the MODE terminal high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The state of the MODE terminal can be changed during operation to allow efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.4 Enable

The device is enabled by setting the EN terminal to high. During the start-up time $t_{Start\ Up}$, the internal circuits are settled and the soft-start circuit is activated. The EN input can be used to control power sequencing in a system with various dc/dc converters. The EN terminal can be connected to the output of another converter, to drive the EN terminal high to achieve a sequencing of the given supply rails. With EN = GND, the device enters shutdown mode, in which all internal circuits are disabled. In fixed-output-voltage versions, the internal resistor divider network is then disconnected from the FB terminal.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical), the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

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8.4 Device Functional Modes

8.4.1 Soft-Start

The TPS62560 has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value typically within 250 μs. This limits the inrush current into the converter during ramp-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled within the start-up time $t_{Start\ Up}$.

8.4.2 Power-Save Mode

The power-save mode is enabled with the MODE terminal set to the low level. If the load current decreases, the converter enters the power-save mode of operation automatically. During power-save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power-save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal + 1%, the device starts a PFM current pulse. The high-side MOSFET switch turns on, and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-μA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses is generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output-voltage ripple during PFM-mode operation can be kept small. The PFM pulse is time controlled, which allows modifying the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output-voltage ripple and PFM frequency depend primarily on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimizes the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode. The power-save mode can be disabled by setting the MODE terminal to high. The converter then operates in the fixed-frequency PWM mode.

8.4.2.1 100% Duty-Cycle Low-Dropout Operation

The device starts to enter 100% duty-cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN}, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery-voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage; and, can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times (R_{DS(on)}max + R_L) \quad (1)$$

where

- $I_{OUT}max$ = maximum output current plus inductor ripple current
- $R_{DS(on)}max$ = maximum P-channel switch $R_{DS(on)}$
- R_L = dc resistance of the inductor
- $V_{OUT}max$ = nominal output voltage plus maximum output voltage tolerance

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Device Functional Modes (continued)

8.4.2.2 Short-Circuit Protection

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current-limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current-limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again after the current in the low-side MOSFET switch has decreased below the threshold of its current-limit comparator.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6256x devices are high-efficiency synchronous step-down DC–DC converter featuring power-save mode or 2.25-MHz fixed frequency operation.

9.2 Typical Application

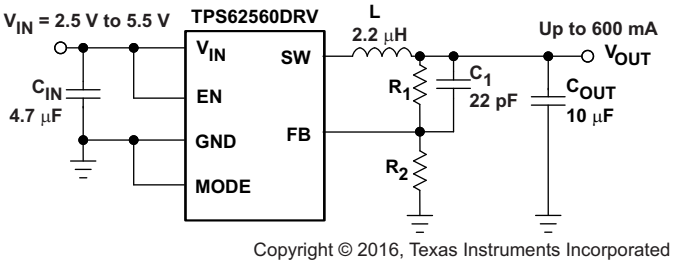

Figure 6. TPS62560DRV Adjustable

9.2.1 Design Requirements

The TPS6256x is a highly integrated DC/DC converter. The output voltage is set with an external voltage divider for the adjustable output voltage version. The output voltage is fixed to 1.8V for the TPS62562. For proper operation a input- and output capacitor and an inductor is required. Table 2 shows the components used for the application characteristic curves.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

For adjustable output voltage versions, the output voltage can be calculated by Equation 2 with the internal reference voltage V_{REF} = 0.6 V typically.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed ~1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_1 is required for optimum load transient response. The value of C_1 should be in the range between 22 pF and 33 pF.

In case of using the fixed output voltage version (TPS62562), V_{out} has to be connected to the feedback pin FB.

Typical Application (continued)

Route the FB line away from noise sources, such as the inductor or the SW line.

9.2.2.2 Output Filter Design (inductor and Output Capacitor)

The TPS62560 is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1 µH effective inductance and 3.5 µF effective capacitance.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection also impacts the output voltage ripple in PFM mode. Higher inductor values lead to lower output voltage ripple and higher PFM frequency; lower inductor values lead to a higher output voltage ripple but lower PFM frequency.

Equation 3 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{3}$$

$$I_L\,max = I_{out}\,max + \frac{\Delta I_L}{2} \tag{4}$$

where

- f = Switching frequency (2.25 MHz, typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_L$max = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

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Table 1. List of Inductors

DIMENSIONS, mm	INDUCTANCE, µH	INDUCTOR TYPE	SUPPLIER(1)
2,5 × 2 × 1 max	2	MIPS2520D2R2	FDK
2,5 × 2 × 1,2 max	2	MIPSA2520D2R2	FDK
2,5 × 2 × 1 max	2.2	KSLI-252010AG2R2	Hitachi Metals
2,5 × 2 × 1,2 max	2.2	LQM2HPN2R2MJ0L	Murata
3 × 3 × 1,5 max	2.2	LPS3015 2R2	Coilcraft

(1) See *Third-Party Products Disclaimer*

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TPS62560 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated by Equation 5:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2\sqrt{3}} \quad (5)$$

At nominal load current, the device operates in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor shown in Equation 6:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (6)$$

At light load currents, the converter operates in power-save mode, and the output voltage ripple is dependent on the output capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

9.2.2.2.3 Input Capacitor Selection

An input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because a ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10-µF input capacitors be used for input voltages > 4.5 V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} terminal. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. List of Capacitors(1)

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7 µF	GRM188R60J475K	0603—1,6 × 0,8 × 0,8 mm	Murata
10 µF	GRM188R60J106M69D	0603—1,6 × 0,8 × 0,8 mm	Murata

(1) See *Third-Party Products Disclaimer*

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9.2.3 Application Curves

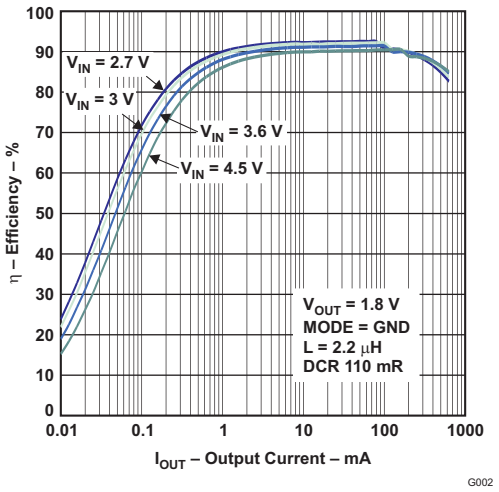

Figure 7. Efficiency vs Output Current

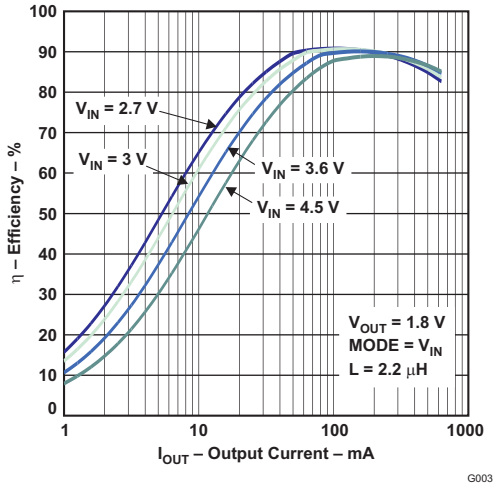

Figure 8. Efficiency vs Output Current

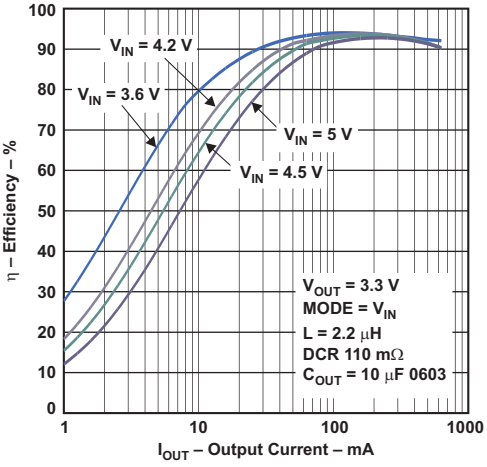

Figure 9. Efficiency vs Output Current

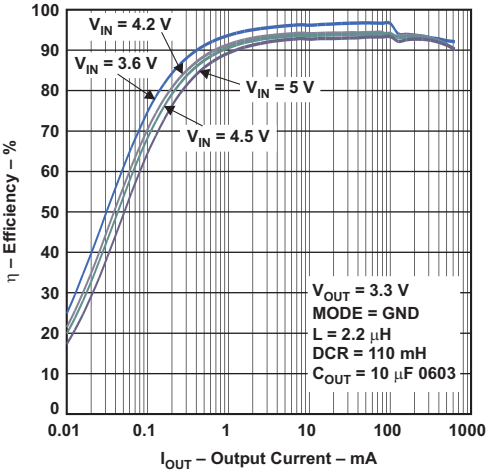

Figure 10. Efficiency vs Output Current

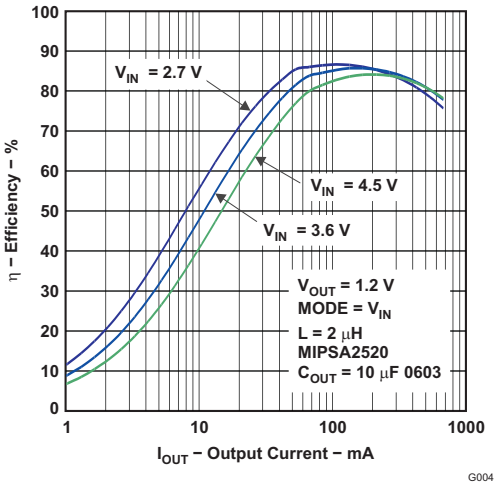

Figure 11. Efficiency vs Output Current

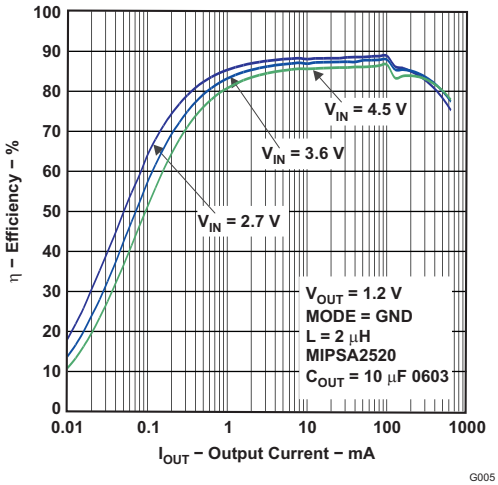

Figure 12. Efficiency vs Output Current

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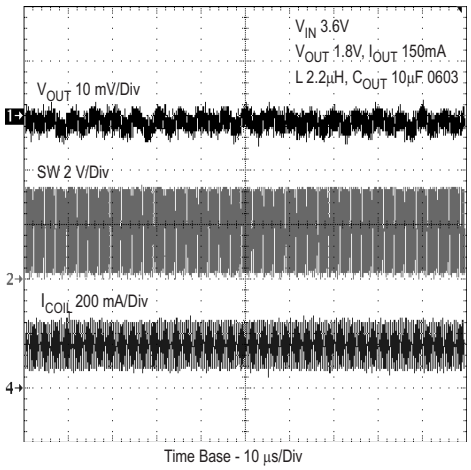

Figure 13. Typical Operation - PWM Mode

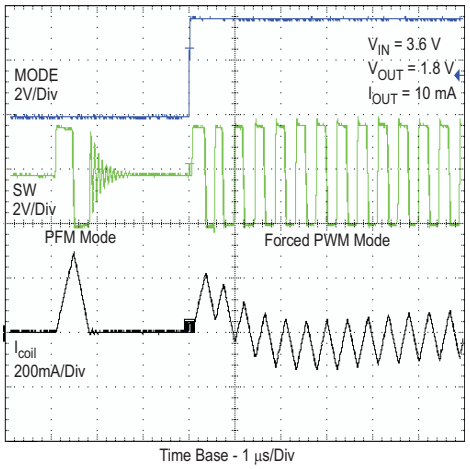

Figure 14. Mode Pin Transition from PFM to FORCED PWM Mode at Light Load

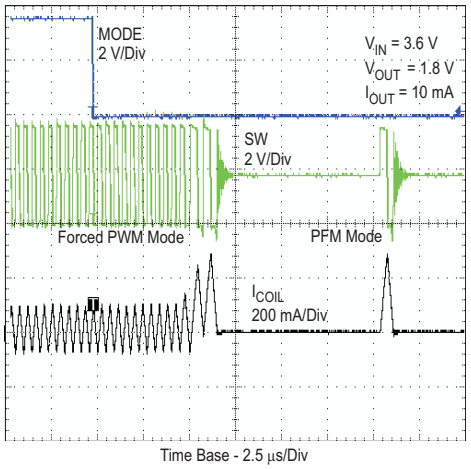

Figure 15. Mode Pin Transition from PWM to PFM MODE at Light Load

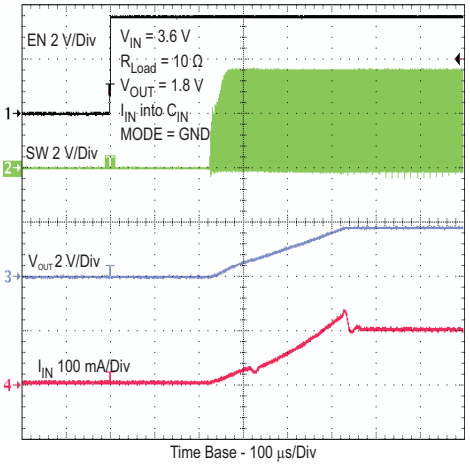

Figure 16. Start-UP Timing

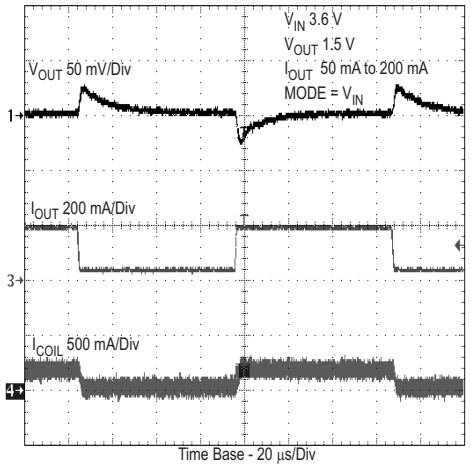

Figure 17. Forced PWM Load Transient

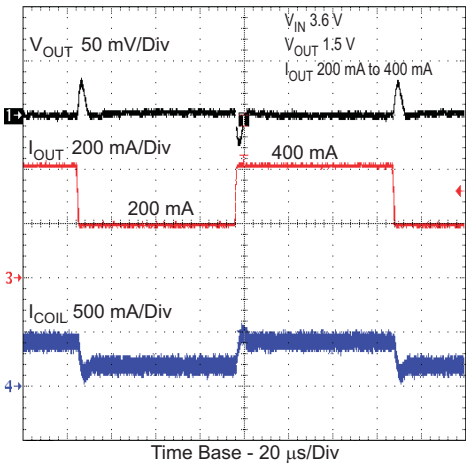

Figure 18. Forced PWM Load Transient

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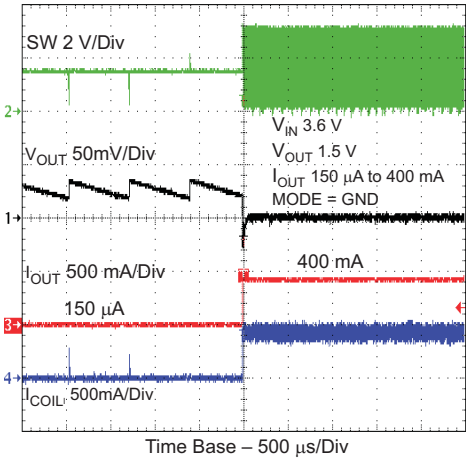

Figure 19. PFM Load Transient

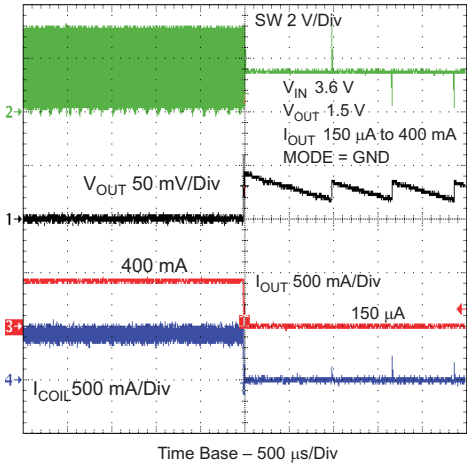

Figure 20. PFM Load Transient

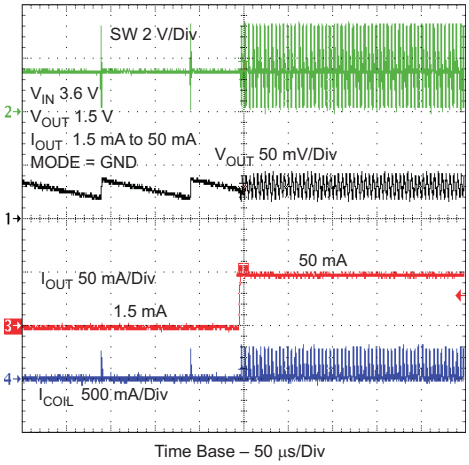

Figure 21. PFM Load Transient

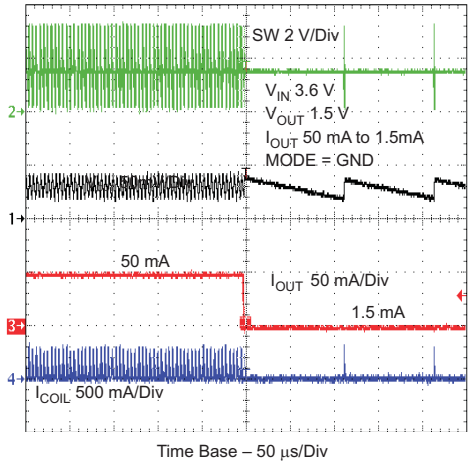

Figure 22. PFM Load Transient

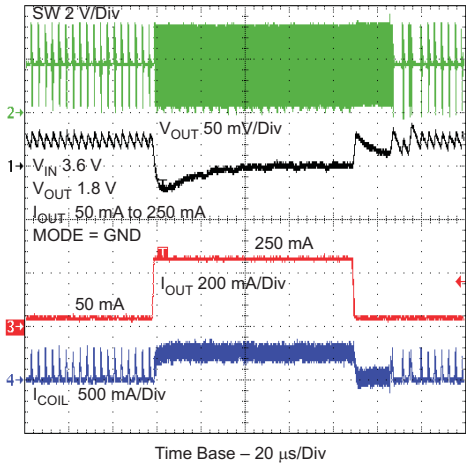

Figure 23. PFM Load Transient

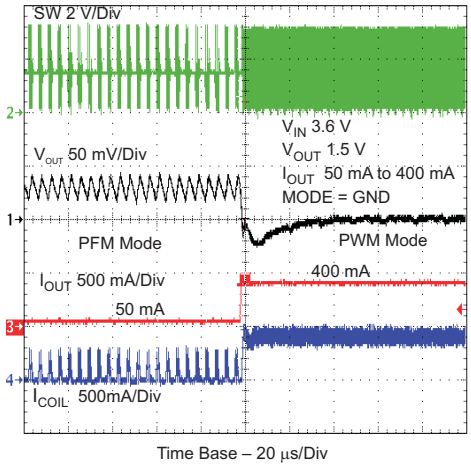

Figure 24. PFM Load Transient

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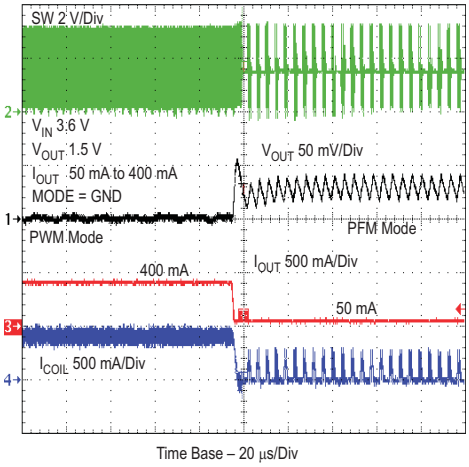

Figure 25. PFM Load Transient

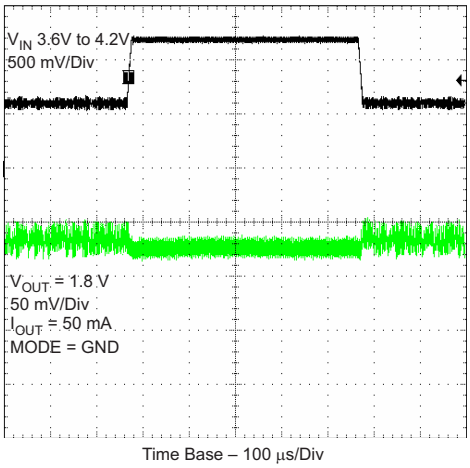

Figure 26. PFM Line Transient

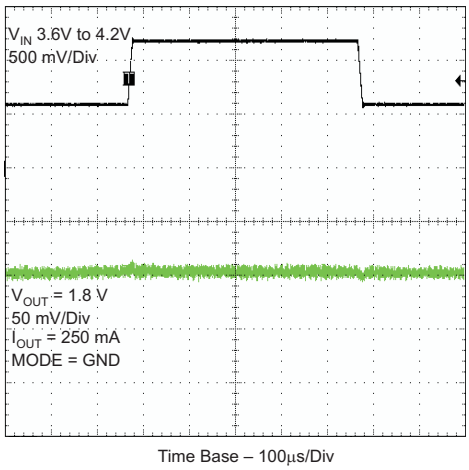

Figure 27. PWM Line Transient

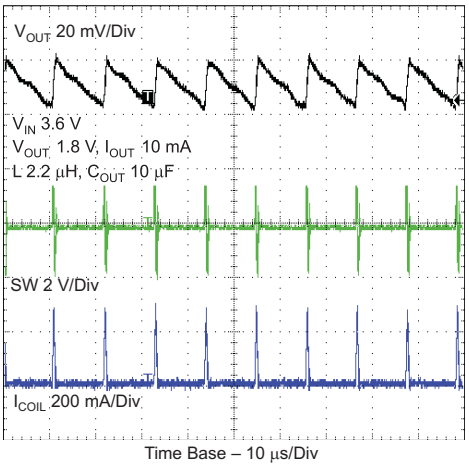

Figure 28. Typical Operation - PFM Mode

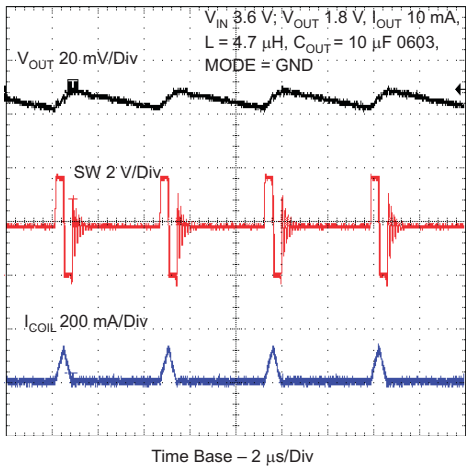

Figure 29. Typical Operation - PFM Mode

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9.3 System Examples

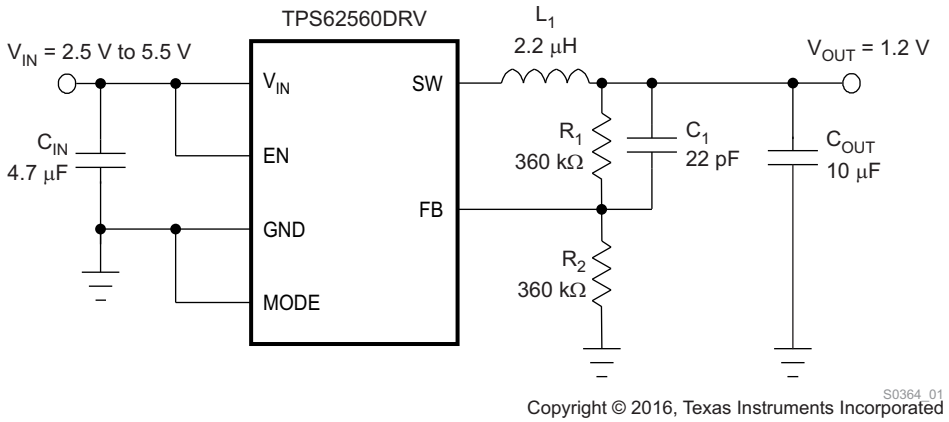

Figure 30. TPS62560 Adjustable 1.2-V Output

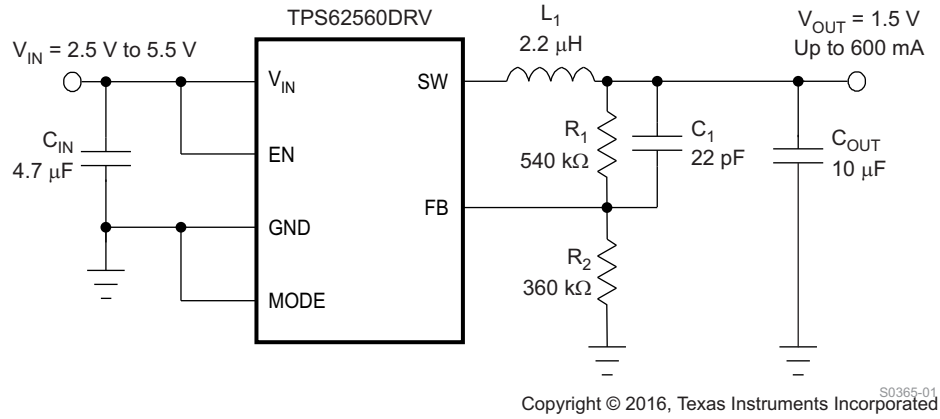

Figure 31. TPS62560 Adjustable 1.5-V Output

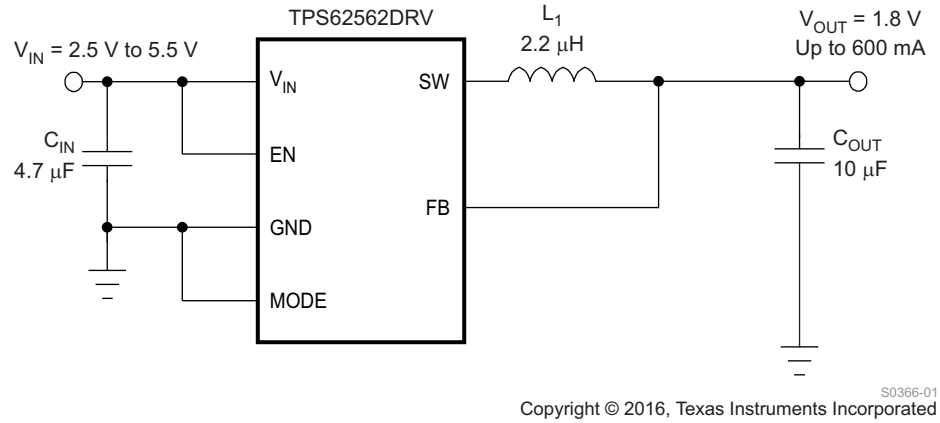

Figure 32. TPS62562 Fixed 1.8-V Output

10 Power Supply Recommendations

The TPS6226x device has no special requirements for its input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6226x.

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11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the exposed thermal pad of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the exposed thermal pad (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the SW line).

11.2 Layout Examples

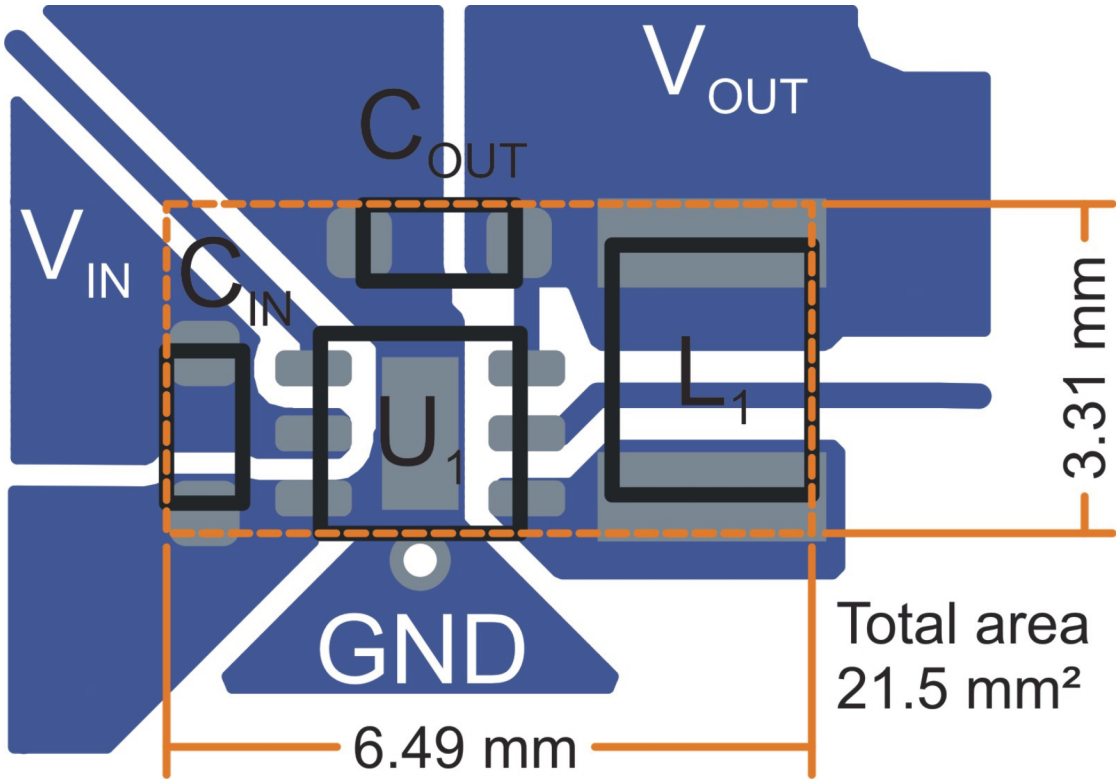

Figure 33. Suggested Layout for Fixed-Output-Voltage Options

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Layout Examples (continued)

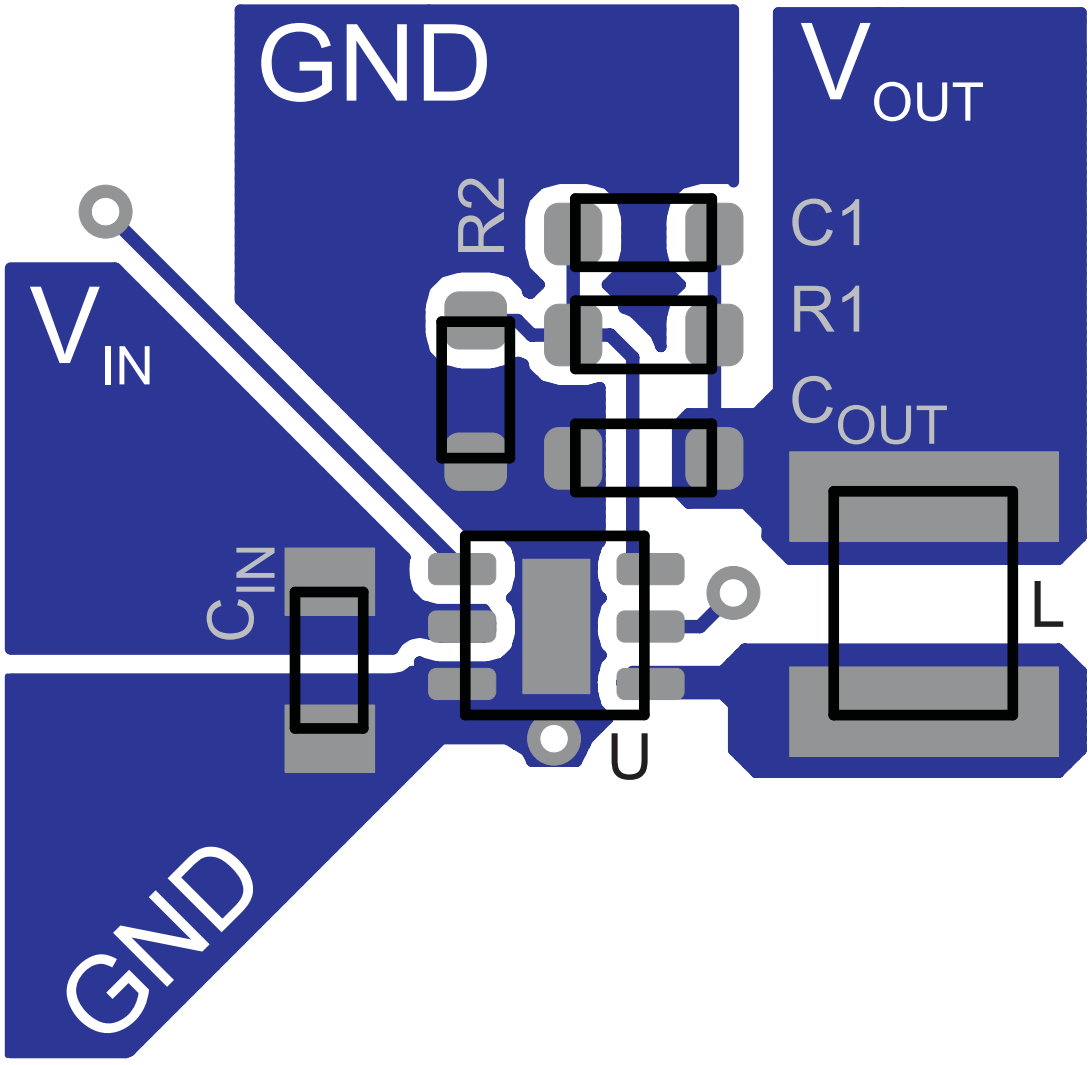

Figure 34. Suggested Layout for Adjustable-Output-Voltage Version

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 Third-Party Products Disclaimer

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12.2 関連リンク

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表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS62560	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62561	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62562	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 静電気放電に関する注意事項

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62560DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVRG4.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62560DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY
TPS62561DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCRG4	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCRG4.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCRG4.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62561DDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO
TPS62562DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	NXT
TPS62562DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT
TPS62562DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT
TPS62562DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	NXT
TPS62562DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62562DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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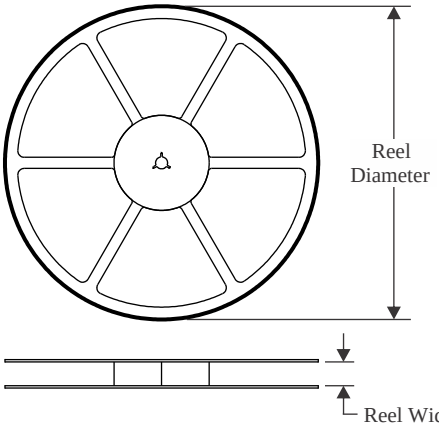
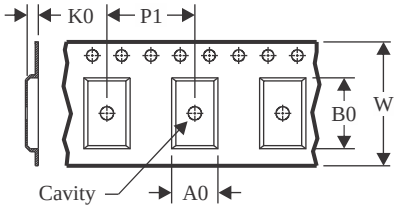
TAPE AND REEL INFORMATION

REEL DIMENSIONS

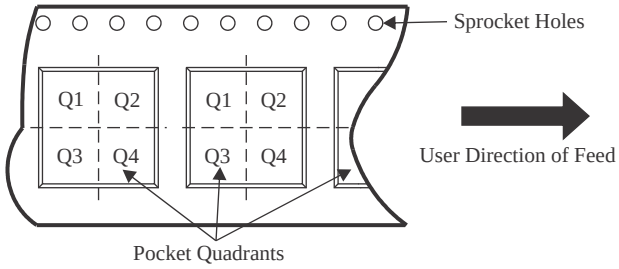


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

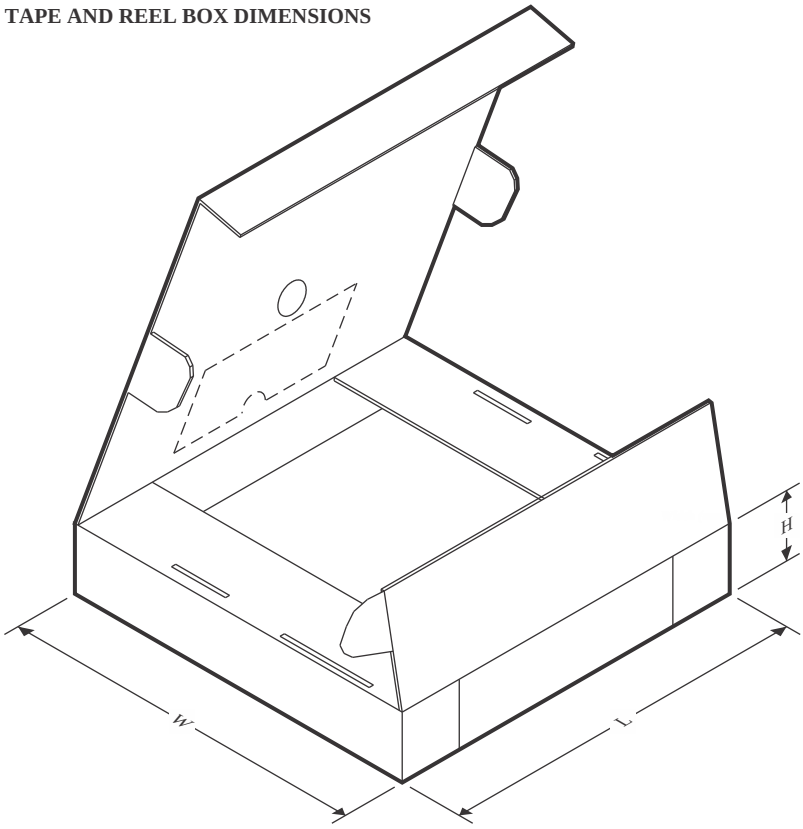
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62560DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62560DRVRG4	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62560DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62561DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62561DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62561DDCRG4	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62561DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62562DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62562DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

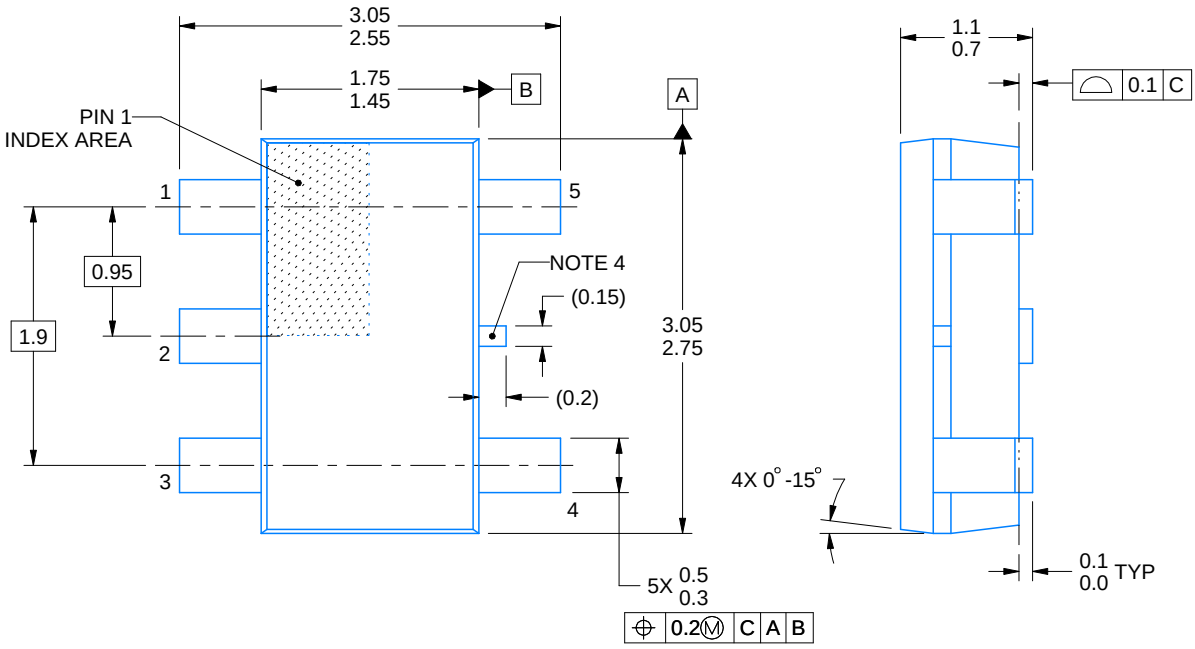
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62560DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62560DRVRG4	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62560DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS62561DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS62561DDCR	SOT-23-THIN	DDC	5	3000	210.0	185.0	35.0
TPS62561DDCRG4	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS62561DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0
TPS62562DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62562DRVT	WSON	DRV	6	250	210.0	185.0	35.0

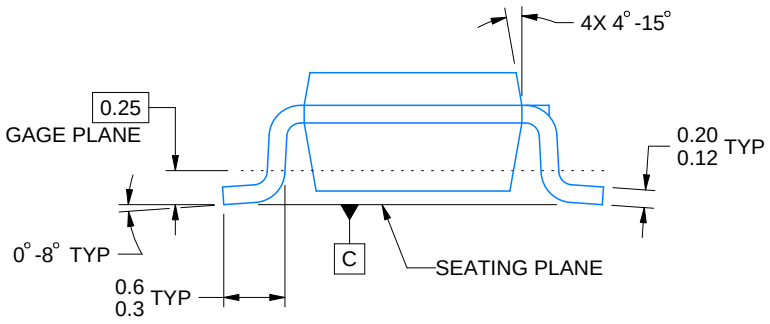
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

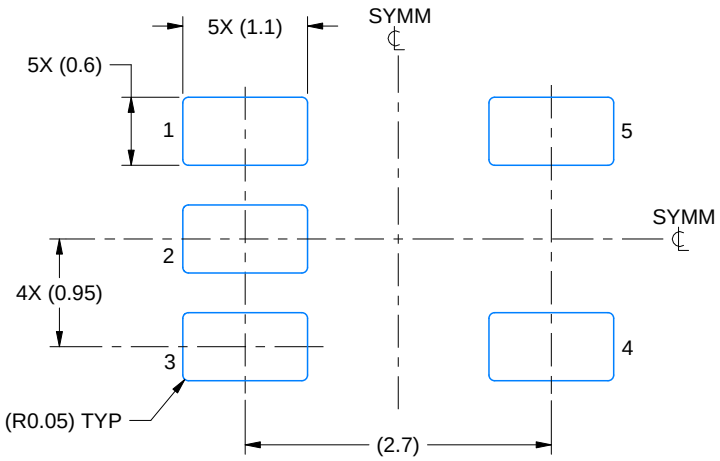




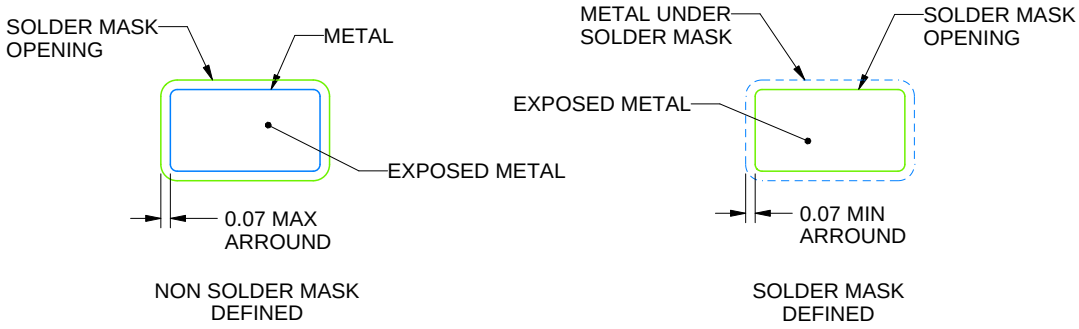
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

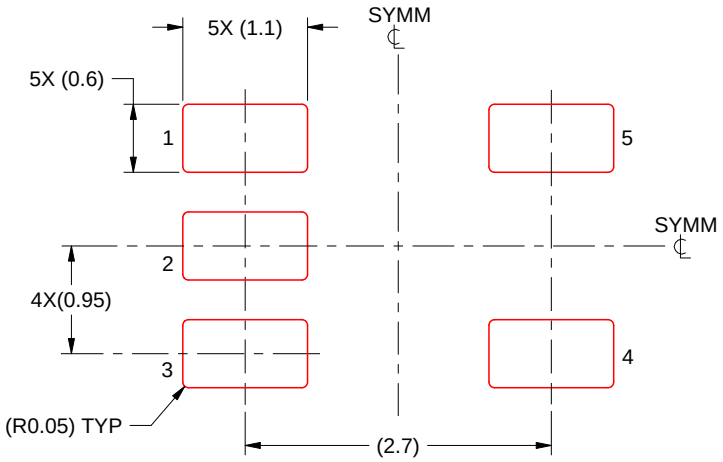


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

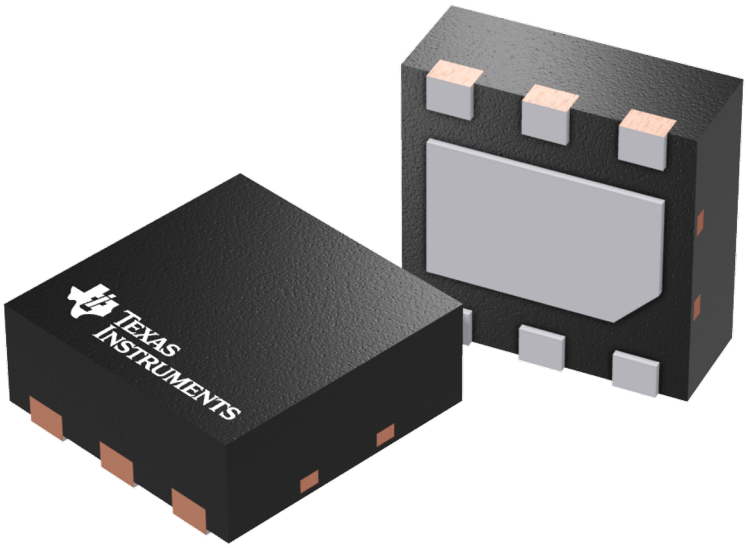
4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



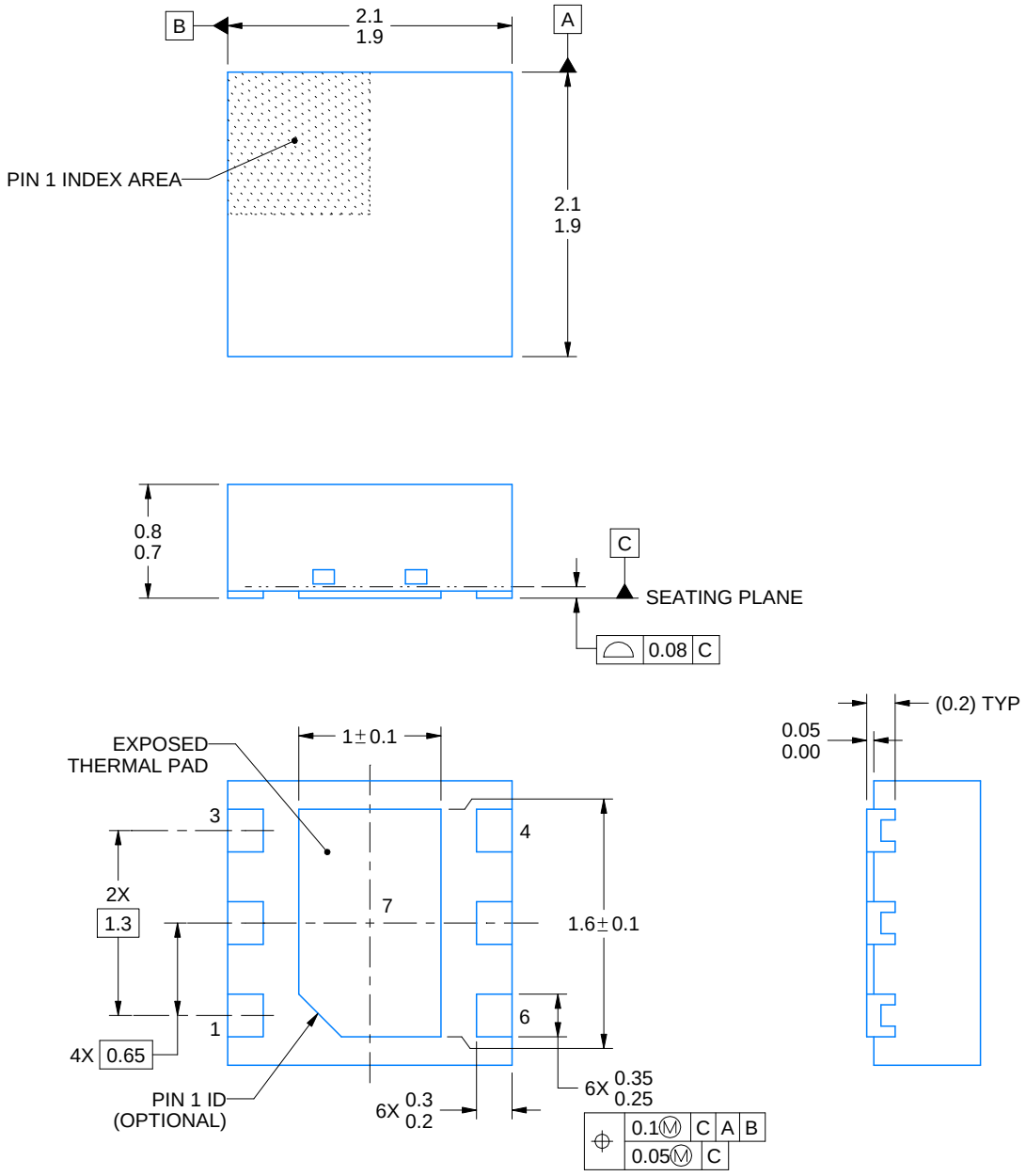
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

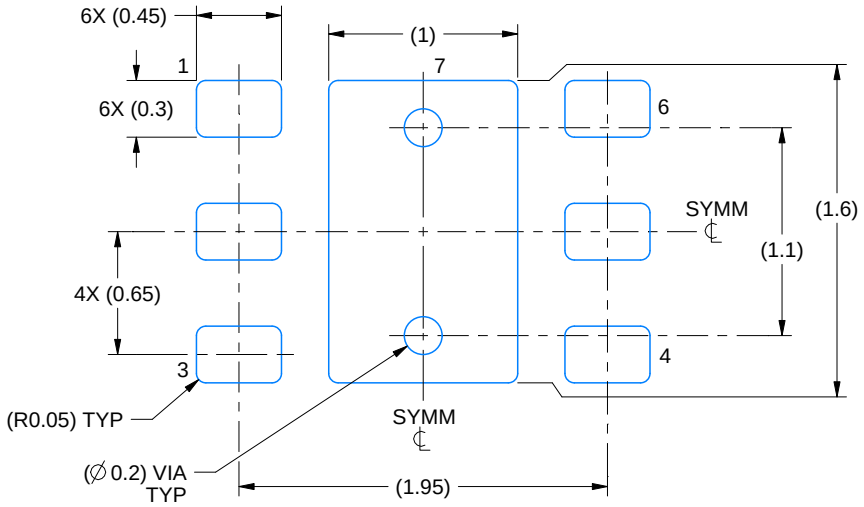
PLASTIC SMALL OUTLINE - NO LEAD



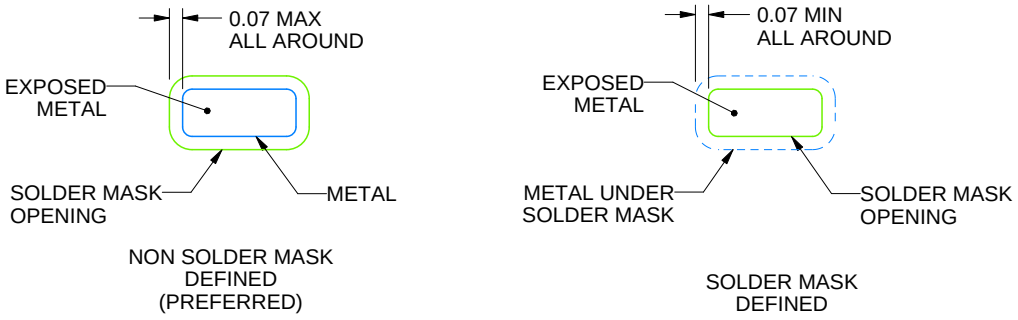
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

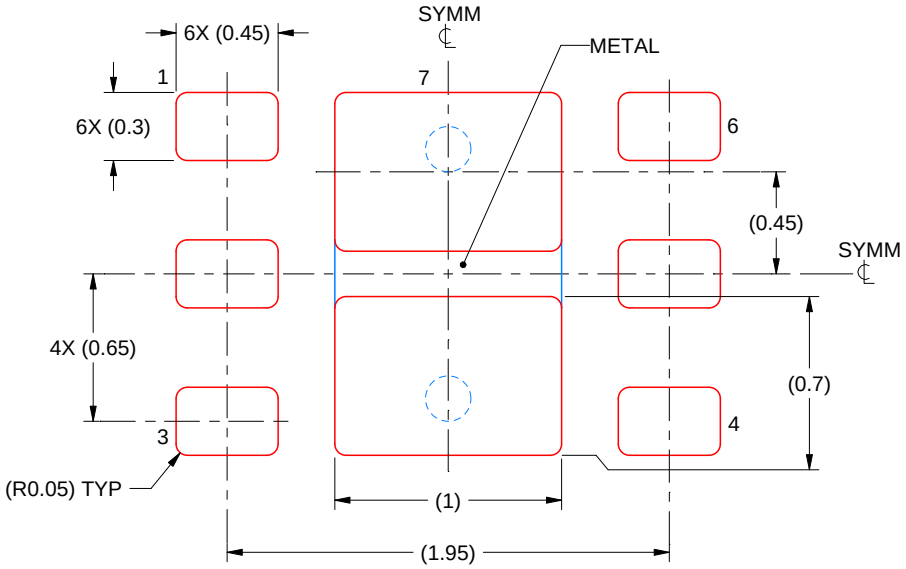


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



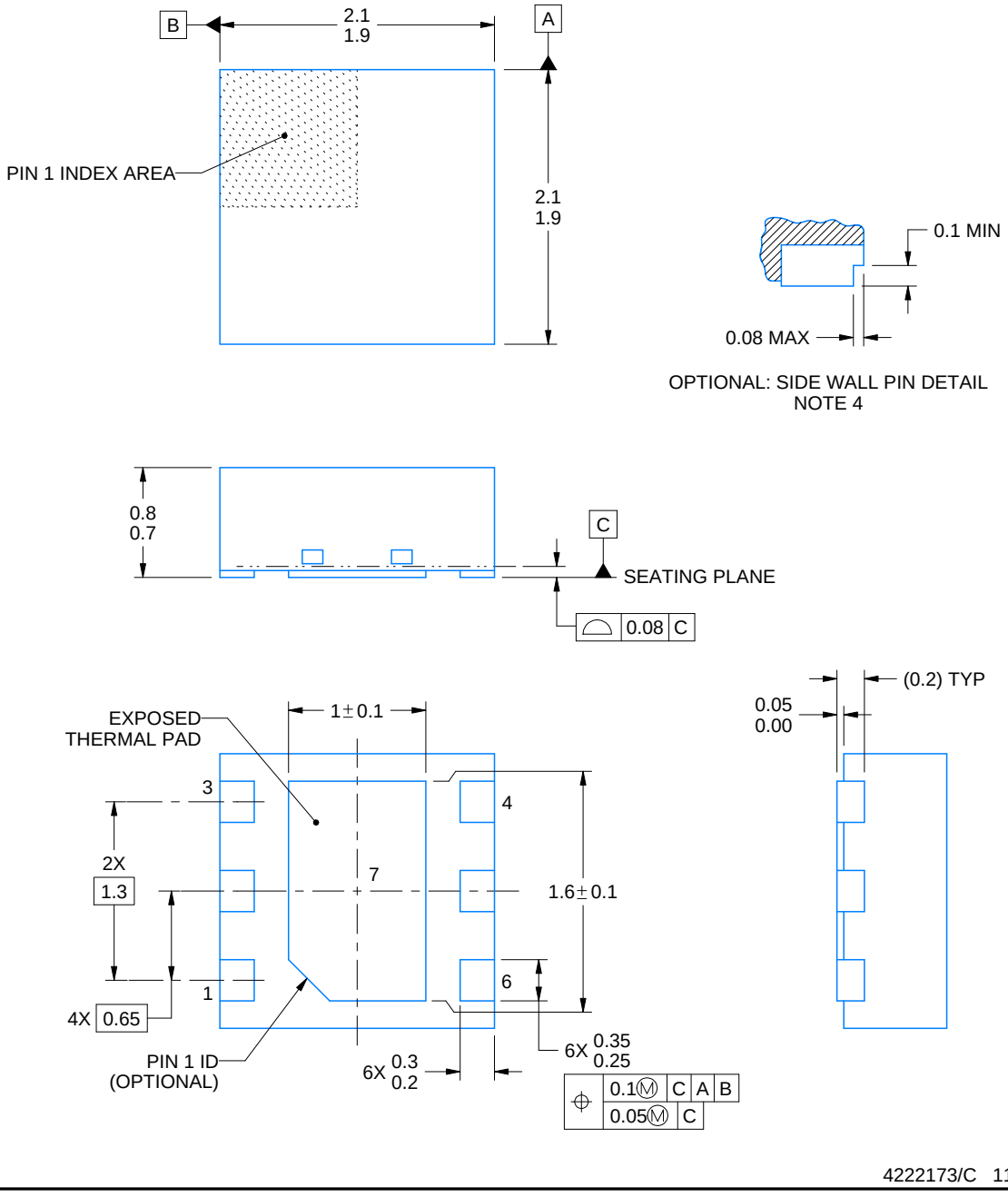
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

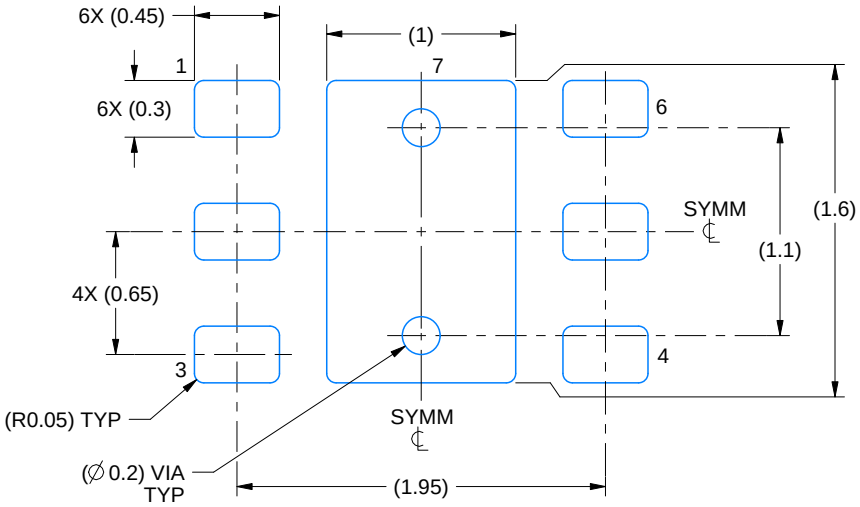
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

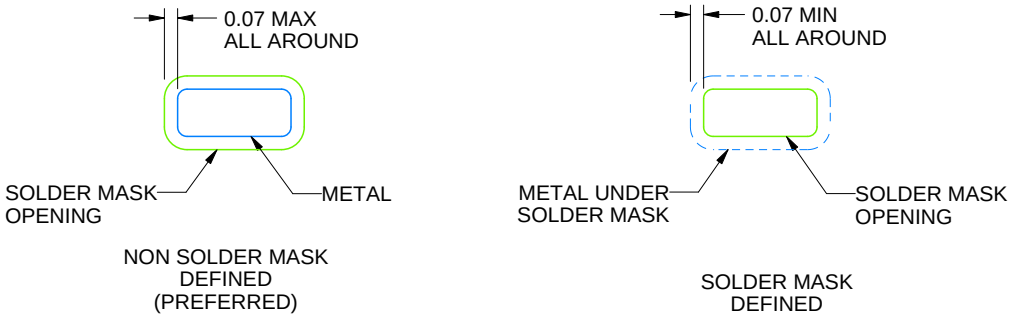


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

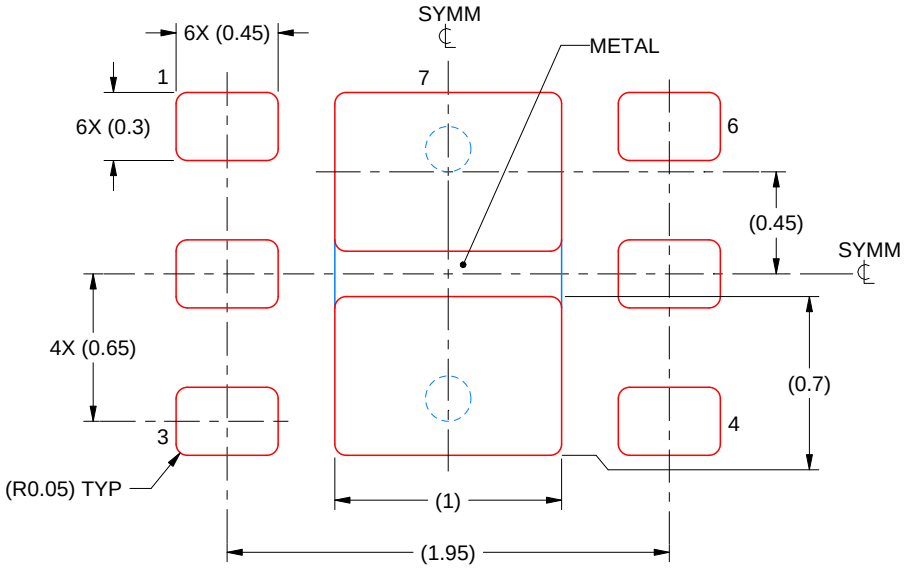


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月