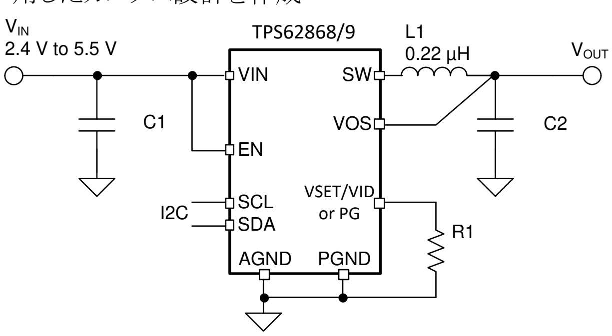
TPS62868x I²C インターフェイス搭載、QFN パッケージ、2.4V～5.5V 入力、4A および 6A 同期整流降圧型コンバータ

1 特長

- 11mΩ および 10.5mΩ のパワー MOSFET を内蔵
- 90% を超える効率 (0.9V 出力)
- DCS-Control トポロジにより、高速過渡応答を実現
- I²C 経由で動的電圧スケーリング (DVS) 用に出力電圧範囲を利用可能
  - 出力電圧範囲は 0.2V ～ 0.8375V、2.5mV ステップ・サイズ
  - 出力電圧範囲は 0.4V ～ 1.675V、5mV ステップ・サイズ
  - 出力電圧範囲は 0.8V ～ 3.35V、10mV ステップ・サイズ
- ±1% の出力電圧精度
- 2.4MHz のスイッチング周波数
- 外付け抵抗による選択
  - スタートアップ時の出力電圧
  - I²C ターゲット・アドレス
- I²C インターフェイスによる選択
  - パワー・セーブ・モードまたは強制 PWM モード
  - 出力放電
  - ヒカップまたはラッチ付き短絡保護
  - 出力電圧のランプ速度
- サーマル事前警告およびサーマル・シャットダウン
- ウィンドウ・コンパレータ付きのパワー・グッド・インジケータ・ピン・オプション
- I²C 互換インターフェイス:最高 3.4Mbps
- 1.5mm x 2.5mm x 1.0mm、9 ピン、0.5mm ピッチの QFN パッケージで供給
- WCSP パッケージでも供給:TPS62866: I²C インターフェイス搭載、1.05mm x 1.78mm WCSP パッケージの 6A 同期整流降圧コンバータ
- TPS62868/9 に WEBENCH® Power Designer を使用したカスタム設計を作成



代表的なアプリケーション

2 アプリケーション

- FPGA、CPU、ASIC、ビデオ・チップセット用のコア電源
- IP ネットワーク・カメラ
- ソリッドステート・ドライブ
- 光モジュール
- LPDDR5 VDDQ レール電源

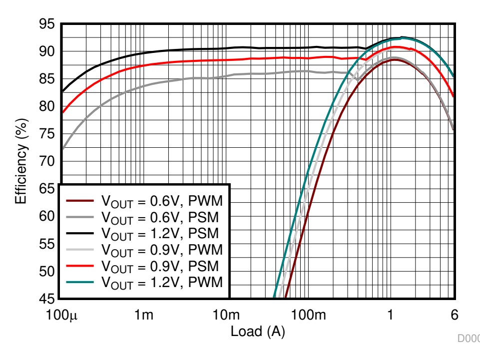
3 概要

TPS62868 および TPS62869 は、高効率、適応型、高電力密度ソリューションを実現する I²C インターフェイス付き高周波数同期整流降圧型コンバータです。中負荷から重負荷では PWM モードで動作し、軽負荷時には自動的に省電力モードへ移行するため、負荷電流の全範囲にわたって高効率が維持されます。このデバイスは、強制的に PWM モードで動作させ、出力電圧リップルを最小化することもできます。DCS-Control アーキテクチャとともに、優れた負荷過渡性能と厳格な出力電圧精度を実現します。I²C インターフェイスと専用 VID ピンにより、常に変化するアプリケーションの性能要件に対する消費電力負荷に合わせて、出力電圧を素早く調整できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS62868	QFN (9)	1.5 x 2.5 x 1.0mm
TPS62869		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



V_{IN} = 3.3V での効率

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2020) to Revision B (July 2021) — **Page**

- I²C に言及されている場合、従来の用語の具体的表現をコントローラーおよびターゲットに全体的に変更.......... 1
- Corrected start-up output voltage for TPS6286xxxC device variants in *Device Options* table.......... 3
- Changed "VID" to "VSET/VID" in *Device Options* table.......... 3
- Added inductor values to *Recommended Operating Conditons* table.......... 5
- Corrected number of pins in *Thermal Information* table.......... 5
- Added quiescent current specification for TPS6286x0A/C devices in *Electrical Characteristics* table 7
- Changed high-level input voltage threshold in *Electrical Characteristics table* 7
- Added separate enable delay time parameter for TPS6286x0C device variants.......... 7
- Added footnote.......... 7
- Added power-good deglitch block to *Functional Block Diagram* 12
- Added *100% Duty Cycle Mode Operation* section.......... 13
- Added section describing the start-up output voltage for TPS6286xxC device variants.......... 14
- Corrected value of C1 in *List of Components* table.......... 22
- Updated data in *Thermal Derating* plot for V_{OUT} = 1.675 V.......... 25
- Added typical application example for TPS6286x0A and TPS6286x0xC device variants.......... 28
- Changed *Layout Example* image.......... 31

Changes from Revision * (September 2020) to Revision A (December 2020) — **Page**

- デバイス・ステータスを「事前情報」から「量産データ」に変更.......... 1

5 Device Options

PART NUMBER[(1)]	FULL OUTPUT VOLTAGE RANGE	START-UP OUTPUT VOLTAGE	DVS STEP SIZE	OUTPUT CURRENT	VSET/VID OR PG PIN
TPS628680**A**RQY	0.2 V to 0.8375 V	0.2 V to 0.575 V, Selectable	2.5 mV	4 A	VSET/VID
TPS6286800**C**RQY		0.5 V			PG
TPS628681**A**RQY	0.4 V to 1.675 V	0.4 V to 1.15 V, Selectable	5 mV		VSET/VID
TPS6286810**C**RQY		0.9 V			PG
TPS628682**A**RQY	0.8 V to 3.35 V	0.8 V to 2.3 V, Selectable	10 mV		VSET/VID
TPS6286820**C**RQY		1.2 V			PG
TPS628690**A**RQY	0.2 V to 0.8375 V	0.2 V to 0.575 V, Selectable	2.5 mV	6 A	VSET/VID
TPS6286900**C**RQY		0.5 V			PG
TPS628691**A**RQY	0.4 V to 1.675 V	0.4 V to 1.15 V, Selectable	5 mV		VSET/VID
TPS6286910**C**RQY		0.9 V			PG
TPS628692**A**RQY	0.8 V to 3.35 V	0.8 V to 2.3 V, Selectable	10 mV		VSET/VID
TPS6286920**C**RQY		1.2 V			PG

(1) For all available packages, see the orderable addendum at the end of the data sheet.

6 Pin Configuration and Functions

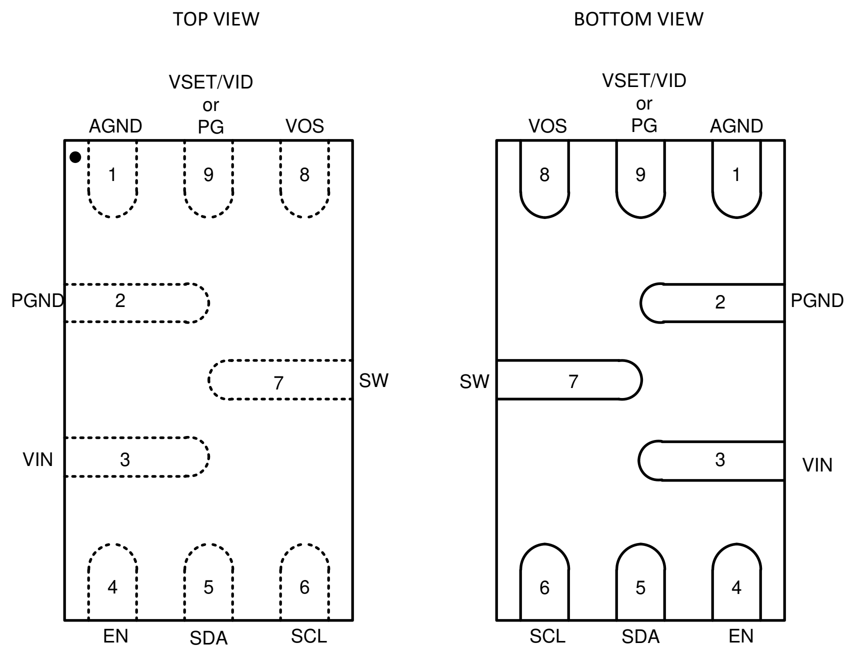


図 6-1. 9-Pin RQY QFN Package (Top View)

表 6-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground pin
VSET/VID	9	Start-up output voltage and device address selection pin. An external resistor must be connected. After start-up, the pin can be used to select the V_{OUT} registers for the output voltage (Low = V_{OUT} register 1; high = V_{OUT} register 2). See *セクション 8.4.4*. This pin is pulled to GND when the device is in shutdown. The function after start-up depends on the device option. See the Device Options.
PG	9	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave it floating. This pin is pulled to GND when the device is in shutdown. The function after start-up depends on the device option. See *セクション 5*.
VOS	8	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PGND	2	Power ground pin
SW	7	Switch pin of the power stage
VIN	3	Power supply input voltage pin
EN	4	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
SDA	5	I^2C serial data pin. Do not leave it floating. Connect it to AGND if not used.
SCL	6	I^2C serial clock pin. Do not leave it floating. Connect it to AGND if not used.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, SDA, SCL, VOS, VSET/VID, VSET/PG	-0.3	6	V
	SW (DC)	-0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	-2.5	10	
I_{SOURCE_PG}	Source current at VSET/PG		1	mA
$I_{SINK\_SDA,SCL}$	Sink current at SDA, SCL		2	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		2.4		5.5	V
t_{F_VIN}	Falling transition time at VIN(1)				10	mV/µs
I_{OUT}	Output current, TPS62868 (2)		0		4	A
	Output current, TPS62869 (3)		0		6	
L	Output inductor	TPS628680x, TPS628690x		110		nH
		TPS628681x, TPS628682x, TPS628691x, TPS628692x		220		
T_J	Junction temperature		-40		125	°C

(1) The falling slew rate of V_{IN} should be limited if V_{IN} goes below V_{UVLO}.
(2) Lifetime is reduced when operating continuously at 4-A output current and the junction temperature is higher than 105 °C.
(3) Lifetime is reduced when operating continuously at 6-A output current and the junction temperature is higher than 85 °C.

7.4 Thermal Information

THERMAL METRIC(1)		TPS62868/ TPS62869 RQY		UNIT
		JEDEC 51-7	TPS62869RQYEVM-118	
		9 PINS	9 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	60.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.0	n/a(2)	°C/W

THERMAL METRIC[1]		TPS62868/ TPS62869 RQY		UNIT
		JEDEC 51-7	TPS62869RQYEVM-118	
		9 PINS	9 PINS	
Ψ_{JT}	Junction-to-top characterization parameter	1.9	3.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	31.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

7.5 Electrical Characteristics

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
I_Q	Quiescent current	TPS6286x1A/C, TPS6286x2A/C	EN = High, no load, device not switching		4	10	µA
		TPS6286x0A/C			9	15	
I_{Q_VOS}	Operating quiescent current into VOS pin		EN = High, no load, device not switching, V_{VOS} = 1.8 V		18		µA
I_{SD}	Shutdown current		EN = Low, T_J = –40°C to 85°C		0.24	1	µA
V_{UVLO}	Undervoltage lockout threshold		V_{IN} rising	2.2	2.3	2.4	V
			V_{IN} falling	2.1	2.2	2.3	V
T_{JW}	Thermal warning threshold		T_J rising		130		°C
	Thermal warning hysteresis		T_J falling		20		°C
T_{JSD}	Thermal shutdown threshold		T_J rising		150		°C
	Thermal shutdown hysteresis		T_J falling		20		°C
LOGIC INTERFACE EN, SDA, SCL							
V_{IH}	High-level input threshold voltage at EN, SCL, SDA, VSET/VID			0.84			V
V_{IL}	Low-level input threshold voltage at EN, SCL, SDA, VSET/VID					0.4	V
$I_{SCL,LKG}$	Input leakage current into SCL pin				0.01	0.8	µA
$I_{SDA,LKG}$	Input leakage current into SDA pin				0.01	0.1	µA
$I_{EN,LKG}$	Input leakage current into EN pin				0.01	0.1	µA
C_{SCL}	Parasitic capacitance at SCL				1		pF
C_{SDA}	Parasitic capacitance at SDA				2.4		pF
STARTUP, POWER GOOD							
t_{Delay}	Enable delay time	TPS6286xA	Time from EN high to device starts switching, R1 = 249kΩ	420	700	1100	µs
		TPS6286x0C	Time from EN high to device starts switching	100	350	900	
t_{Ramp}	Output voltage ramp time		Time from device starts switching to power good	0.85	1	1.5	ms
V_{PG}	Power good lower threshold[1]		V_{VOS} referenced to V_{OUT} nominal	85	91	96	%
	Power good upper threshold		V_{VOS} referenced to V_{OUT} nominal	103	111	120	%
$t_{PG,DLY}$	Power good deglitch delay		Rising and falling edges		34		µs
OUTPUT							
V_{OUT}	Output voltage accuracy		FPWM, no Load, T_J = 0°C to 85°C	-1		1	%
			FPWM, no Load	-2		2	%
$I_{VOS,LKG}$	Input leakage current into VOS pin		EN = Low, Output discharge disabled, V_{VOS} = 1.8 V, TPS6286x1A/C		0.2	2.5	µA
R_{DIS}	Output discharge resistor at VOS pin				3.5		Ω
	Load regulation		V_{OUT} = 0.9 V, FPWM		0.04		%/A
POWER SWITCH							
$R_{DS(on)}$	High-side FET on-resistance				11		mΩ
	Low-side FET on-resistance				10.5		mΩ
I_{LIM}	High-side FET forward current limit		TPS62868	5	5.5	6	A
			TPS62869	7	7.7	8.5	A
	Low-side FET forward current limit		TPS62868		4.5		A
			TPS62869		6.5		A
	Low-side FET negative current limit		TPS62868, TPS62869		-3		A

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 0.9 V		2.4		MHz

(1) TPS6286x0A and TPS6286x00C device variants do not have a lower PG threshold. In these device variants the PG signal is high if the start-up ramp is complete and the output voltage is below the upper PG threshold.

7.6 I²C InterfaceTiming Characteristics

PARAMETER (1) (2)		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
$f_{(SCL)}$	SCL Clock Frequency	Fast mode		400	kHz
$f_{(SCL)}$	SCL Clock Frequency	Fast mode plus		1	MHz
$f_{(SCL)}$	SCL Clock Frequency	High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
$f_{(SCL)}$	SCL Clock Frequency	High-speed mode (read operation), C_B – 100 pF max		3.4	MHz
$f_{(SCL)}$	SCL Clock Frequency	High-speed mode (write operation), C_B – 400 pF max		1.7	MHz
$f_{(SCL)}$	SCL Clock Frequency	High-speed mode (read operation), C_B – 400 pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		µs
t_{BUF}	Bus Free Time Between a STOP and START Condition	Fast mode	1.3		µs
t_{BUF}	Bus Free Time Between a STOP and START Condition	Fast mode plus	0.5		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START condition	Standard mode	4		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START condition	Fast mode	600		ns
t_{HD}, t_{STA}	Hold Time (Repeated) START condition	Fast mode plus	260		ns
t_{HD}, t_{STA}	Hold Time (Repeated) START condition	High-speed mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		µs
t_{LOW}	LOW Period of the SCL Clock	Fast mode	1.3		µs
t_{LOW}	LOW Period of the SCL Clock	Fast mode plus	0.5		µs
t_{LOW}	LOW Period of the SCL Clock	High-speed mode, C_B – 100 pF max	160		ns
t_{LOW}	LOW Period of the SCL Clock	High-speed mode, C_B – 400 pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		µs
t_{HIGH}	HIGH Period of the SCL Clock	Fast mode	600		ns
t_{HIGH}	HIGH Period of the SCL Clock	Fast mode plus	260		ns
t_{HIGH}	HIGH Period of the SCL Clock	High-speed mode, C_B – 100 pF max	60		ns
t_{HIGH}	HIGH Period of the SCL Clock	High-speed mode, C_B – 400 pF max	120		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		µs
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Fast mode	600		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Fast mode plus	260		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	High-speed mode	160		ns
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
t_{SU}, t_{DAT}	Data Setup Time	Fast mode	100		ns
t_{SU}, t_{DAT}	Data Setup Time	Fast mode plus	50		ns
t_{SU}, t_{DAT}	Data Setup Time	High-speed mode	10		ns

PARAMETER [(1)] [(2)]		TEST CONDITIONS	MIN	MAX	UNIT
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
t_{HD}, t_{DAT}	Data Hold Time	Fast mode	0	0.9	µs
t_{HD}, t_{DAT}	Data Hold Time	Fast mode plus	0		µs
t_{HD}, t_{DAT}	Data Hold Time	High-speed mode, C_B – 100 pF max	0	70	ns
t_{HD}, t_{DAT}	Data Hold Time	High-speed mode, C_B – 400 pF max	0	150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode		1000	ns
t_{RCL}	Rise Time of SCL Signal	Fast mode	20 + 0.1 C_B	300	ns
t_{RCL}	Rise Time of SCL Signal	Fast mode plus		120	ns
t_{RCL}	Rise Time of SCL Signal	High-speed mode, C_B – 100 pF max	10	40	ns
t_{RCL}	Rise Time of SCL Signal	High-speed mode, C_B – 400 pF max	20	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Fast mode	20 + 0.1 C_B	300	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Fast mode plus		120	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	High-speed mode, C_B – 100 pF max	10	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	High-speed mode, C_B – 400 pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 C_B	300	ns
t_{FCL}	Fall Time of SCL Signal	Fast mode		300	ns
t_{FCL}	Fall Time of SCL Signal	Fast mode plus		120	ns
t_{FCL}	Fall Time of SCL Signal	High-speed mode, C_B – 100 pF max	10	40	ns
t_{FCL}	Fall Time of SCL Signal	High-speed mode, C_B – 400 pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode		1000	ns
t_{RDA}	Rise Time of SDA Signal	Fast mode	20 + 0.1 C_B	300	ns
t_{RDA}	Rise Time of SDA Signal	Fast mode plus		120	ns
t_{RDA}	Rise Time of SDA Signal	High-speed mode, C_B – 100 pF max	10	80	ns
t_{RDA}	Rise Time of SDA Signal	High-speed mode, C_B – 400 pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode		300	ns
t_{FDA}	Fall Time of SDA Signal	Fast mode	20 + 0.1 C_B	300	ns
t_{FDA}	Fall Time of SDA Signal	Fast mode plus		120	ns
t_{FDA}	Fall Time of SDA Signal	High-speed mode, C_B – 100 pF max	10	80	ns
t_{FDA}	Fall Time of SDA Signal	High-speed mode, C_B – 400 pF max	20	160	ns
t_{SU}, t_{STO}	Setup Time of STOP Condition	Standard mode	4		µs
t_{SU}, t_{STO}	Setup Time of STOP Condition	Fast mode	600		ns
t_{SU}, t_{STO}	Setup Time of STOP Condition	Fast mode plus	260		ns
t_{SU}, t_{STO}	Setup Time of STOP Condition	High-Speed mode	160		ns
C_B	Capacitive Load for SDA and SCL	Standard mode		400	pF
C_B	Capacitive Load for SDA and SCL	Fast mode		400	pF
C_B	Capacitive Load for SDA and SCL	Fast mode plus		550	pF

PARAMETER [1] [2]		TEST CONDITIONS	MIN	MAX	UNIT
C_B	Capacitive Load for SDA and SCL	High-Speed mode		400	pF

(1) All values referred to V_{IL} MAX and V_{IH} MIN levels in ELECTRICAL CHARACTERISTICS table.
(2) For bus line loads C_B between 100 pF and 400 pF, the timing parameters must be linearly interpolated.

7.7 Typical Characteristics

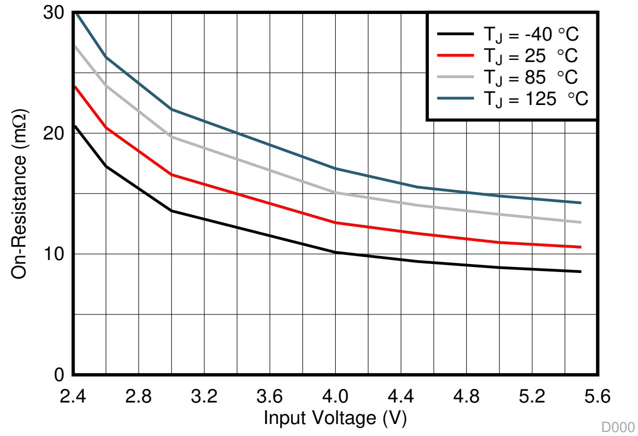


図 7-1. High-Side FET On-Resistance

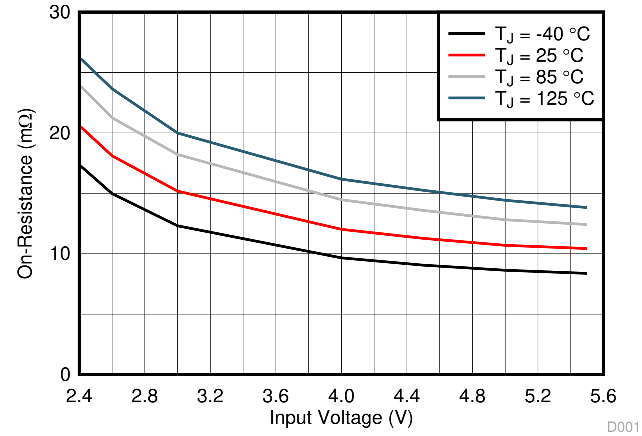


図 7-2. Low-Side FET On-Resistance

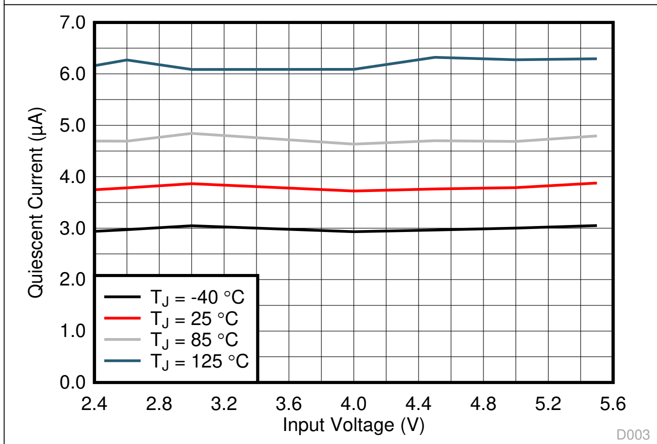


図 7-3. Quiescent Current

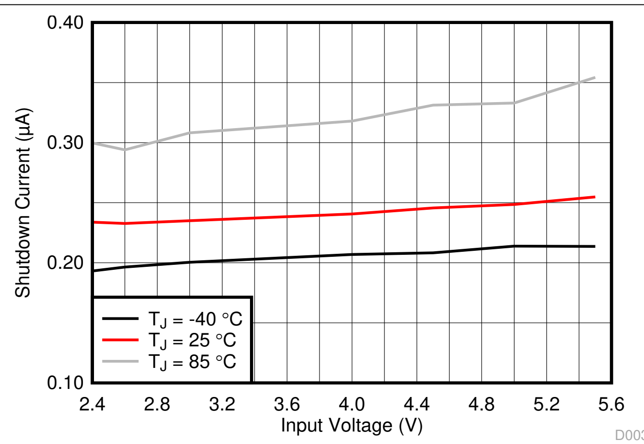


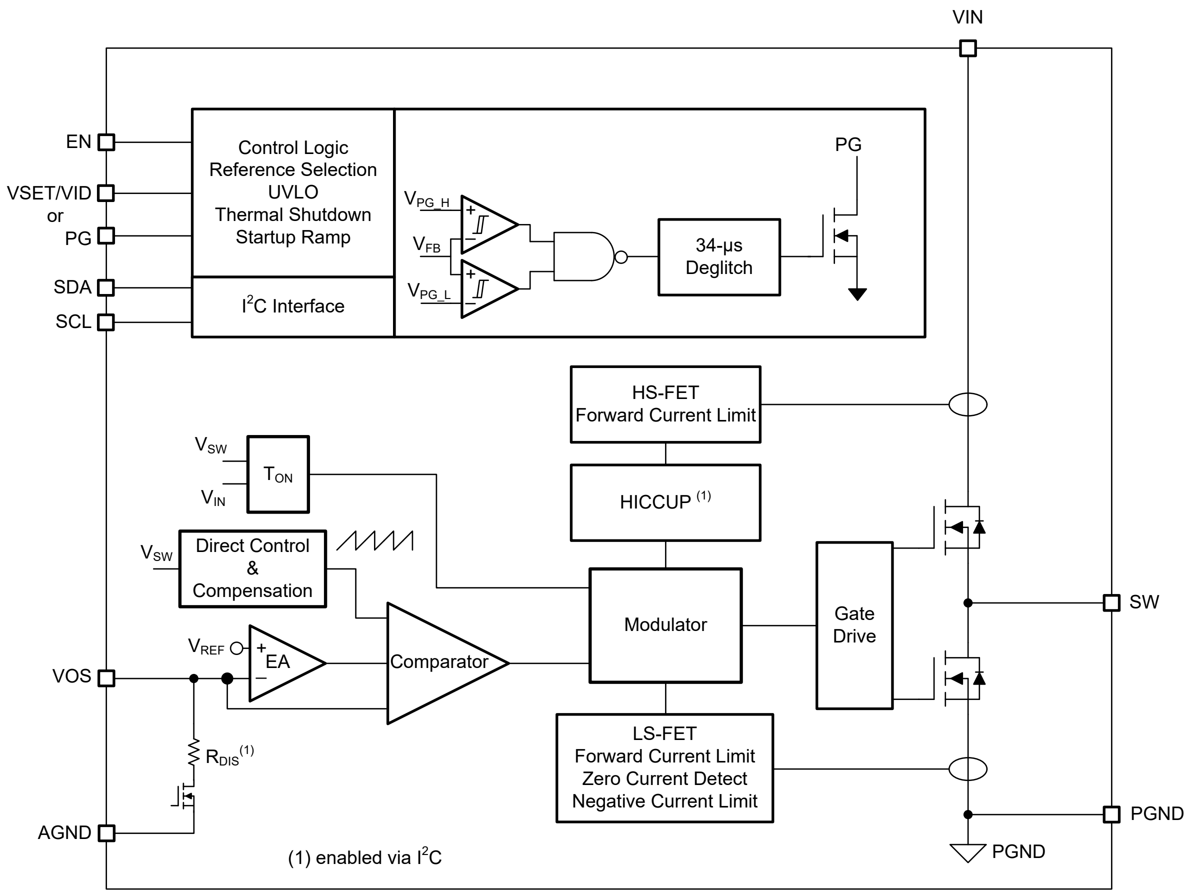
図 7-4. Shutdown Current

8 Detailed Description

8.1 Overview

The DCS-Control™ topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. The devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. Power Save Mode is based on a fixed on-time architecture, as shown in 式 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 416ns \tag{1}$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

When V_{IN} decreases to typically 15% above the V_{OUT}, the TPS6286x does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.3.2 Forced PWM Mode

With I^2C, set the device in forced PWM (FPWM) mode by the CONTROL register. The device switches at 2.4 MHz, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in FPWM mode.

8.3.3 100% Duty Cycle Mode Operation

There is no limitation for small duty cycles since even at very low duty cycles, the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side MOSFET and the DC resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN,MIN} = V_{OUT} + (R_{DS(ON)} + R_L) I_{OUT,MAX} \tag{2}$$

where

- $V_{IN,MIN}$ is the minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ is the maximum output current
- $R_{DS(on)}$ is the high-side FET ON-resistance
- R_L is the inductor ohmic resistance (DCR)

8.3.4 Start-up

After enabling the device, there is an enable delay (t_{Delay}) before the device starts switching. During this period, the device sets the internal reference voltage, and determines the start-up output voltage through the resistor connected to the VSET/VID pin. After t_{delay}, all registers can be read and written by the I^2C interface.

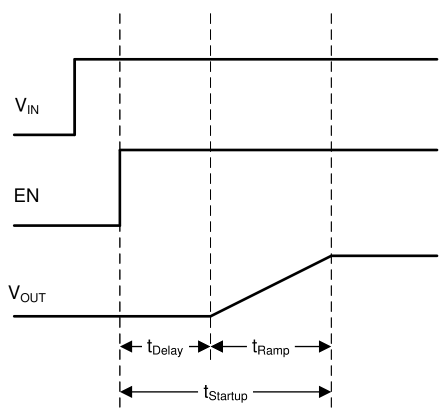


図 8-1. Start-up Sequence

After the enable delay, an internal soft start-up circuitry ramps up the output voltage with a period of 1 ms (t_{Ramp}). This avoids excessive inrush current and creates a smooth output voltage rising-slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-side

MOSFET is turned off and the low-side MOSFET is turned on, while the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically re-starts, with an internal soft start-up, after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

The HICCUP is disabled by the CONTROL register bit Enable HICCUP. Disabling HICCUP changes the overcurrent protection to latching protection. The device stops switching after the high-side MOSFET current limit is triggered 32 times. Toggling the EN pin, removing and reapplying the input voltage, or writing to the CONTROL register bit Software Enable Device unlatches the device.

8.3.6 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, undervoltage lockout (UVLO) is implemented when the input voltage is lower than V_{UVLO}. The device stops switching and the output voltage discharge is active (if enabled through I^2C) when the device is in UVLO. When the input voltage recovers, the device automatically returns to operation with an internal soft start-up. During UVLO, the internal register values are kept.

The UVLO bit in the STATUS Register is set when the input voltage is less than the UVLO falling threshold. When the input voltage is below 1.8 V (typ.), all registers are reset.

8.3.7 Thermal Warning and Shutdown

When the junction temperature goes up to T_{JW}, the device gives a pre-warning indicator in the STATUS register. The device keeps running.

When the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically with an internal soft start-up. During thermal shutdown, the internal register values are kept.

8.4 Device Functional Modes

8.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. In shutdown mode (EN = Low), the internal power switches as well as the entire control circuitry are turned off, and all the registers are reset, except for the Enable Output Discharge bit. Do not leave the EN pin floating.

In shutdown mode (EN = Low), all registers cannot be read and written by the I^2C interface.

The typical threshold value of the EN pin is 0.61 V for rising input signals, and 0.51 V for falling input signals.

The device is also enabled or disabled by setting the bit, Software Enable Device in CONTROL register while EN = High. After being disabled/enabled by this bit, the device stops switching and has a new start-up beginning with t_{Ramp}. There is no T_{Delay} time and the registers are not reset.

8.4.2 Output Discharge

An internal MOSFET switch smoothly discharges the output through the VOS pin in shutdown mode (EN = Low or Software Enable Device bit = 0). The output discharge is also active when the device is in thermal shutdown and UVLO.

When the Enable Output Discharge bit is set to 0, the output discharge function is disabled. The input voltage must remain higher than 1 V (typ.) to keep the output discharge function operational and the status of the Enable Output Discharge bit retained. The Enable Output Discharge bit is reset on the rising edge of the EN pin.

8.4.3 Start-Up Output Voltage and I^2C Target Address Selection

During the ramp up period (t_{Ramp}), the output voltage ramps to the start-up output voltage first, then ramps up or down to the new value when the value of the output register is changed by I^2C interface commands.

8.4.3.1 TPS6286xxA Devices

During the enable delay (t_{Delay}), the start-up output voltage and device I²C target address are set by an external resistor connected to the VSET/VID pin through an internal R2D (resistor to digital) converter. 表 8-1 shows the options.

表 8-1. Start-up Output Voltage and I²C Target Address Options

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID	START-UP OUTPUT VOLTAGE (TYP)	I²C TARGET ADDRESS
249 kΩ	Voltage Factor * 1.15 V	0b1000110 (0x46)
205 kΩ	Voltage Factor * 1.10 V	0b1000101 (0x45)
162 kΩ	Voltage Factor * 1.05 V	0b1000100 (0x44)
133 kΩ	Voltage Factor * 1.00 V	0b1000011 (0x43)
105 kΩ	Voltage Factor * 0.95 V	0b1000010 (0x42)
86.6 kΩ	Voltage Factor * 0.90 V	0b1000001 (0x41)
68.1 kΩ	Voltage Factor * 0.85 V	0b1001000 (0x48)
56.2 kΩ	Voltage Factor * 0.80 V	0b1001001 (0x49)
44.2 kΩ	Voltage Factor * 0.75 V	0b1001010 (0x4A)
36.5 kΩ	Voltage Factor * 0.70 V	0b1001011 (0x4B)
28.7 kΩ	Voltage Factor * 0.65 V	0b1001100 (0x4C)
23.7 kΩ	Voltage Factor * 0.60 V	0b1001101 (0x4D)
18.7 kΩ	Voltage Factor * 0.55 V	0b1001110 (0x4E)
15.4 kΩ	Voltage Factor * 0.50 V	0b1001111 (0x4F)
12.1 kΩ	Voltage Factor * 0.45 V	0b1000000 (0x40)
10 kΩ	Voltage Factor * 0.40 V	0b1000111 (0x47)

表 8-2. Device Option Voltage Factors

DEVICE OPTION	VOLTAGE FACTOR
TPS6286x**0**A	0.5
TPS6286x**1**A	1
TPS6286x**2**A	2

The R2D converter has an internal current source which applies current through the external resistor, and an internal ADC which reads back the resulting voltage level. Depending on the level, the correct start-up output voltage and I²C target address are set. Once this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Ensure that there is no additional current path or capacitance greater than 30 pF from this pin to GND during R2D conversion, otherwise a false value is set.

8.4.3.2 TPS6286xxxC Devices

The start-up output voltage, voltage factor, and I²C target address of the TPS6286xxxC devices are factory-set according to 表 8-3.

表 8-3. Device Option Start-Up Voltage, Voltage Factor, and I²C Target Address

DEVICE OPTION	VOLTAGE FACTOR	START-UP OUTPUT VOLTAGE	I²C TARGET ADDRESS
TPS6286x0xC	0.5	0.5 V	0b1000010 (0x42)
TPS6286x1xC	1	0.9 V	
TPS6286x2xC	2	1.2 V	

8.4.4 Select Output Voltage Registers (VID)

After the start-up period ($t_{Startup}$), the output voltage can be selected between two output voltage registers by the VID pin. When VID is pulled low, the output voltage is set by 表 8-6. When VID is pulled high, the output voltage is set by 表 8-7. This is also called dynamic voltage scaling (DVS).

During an output voltage change through I²C or the VSET/VID pin, the device can be set in FPWM by the Enable FPWM Mode during Output Voltage Change bit in CONTROL register. The output voltage change speed is set by the Voltage Ramp Speed bit.

8.4.5 Power Good (PG)

The TPS62868 and TPS62869 families provide device options with the PG pin instead of a VSET/VID pin. Refer to *セクション 5* to see the according device options.

The PG pin goes high impedance once the output voltage is above 91% and less than 110% of the nominal voltage, and is driven low once the voltage is out of the range. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

The PG has a deglitch time, before the signal goes high or low, during normal operation.

表 8-4. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH	LOW
Enable	$0.91 \times V_{OUT\_NOM} \le V_{VOS} \le 1.11 \times V_{OUT\_NOM}$	√	
	$V_{VOS} < 0.91 \times V_{OUT\_NOM}$ or $V_{VOS} > 1.11 \times V_{OUT\_NOM}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.8\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 1.8\ V$	undefined	

8.5 Programming

8.5.1 Serial Interface Description

I2C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *controller* device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A *target* device receives or transmits data on the bus under control of the controller device, or both.

The device works as a *target* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), fast mode plus (1 Mbps), and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode.

It is recommended that the I²C controller initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I²C engine.

8.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 8-2. All I²C-compatible devices recognize a start condition.

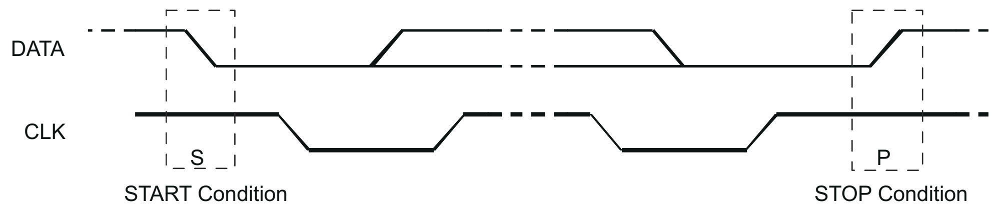


図 8-2. START and STOP Conditions

The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the controller ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 8-3). All devices recognize the address sent by the controller and compare it to their internal fixed addresses. Only the target device with a matching address generates an acknowledge (see 図 8-4) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

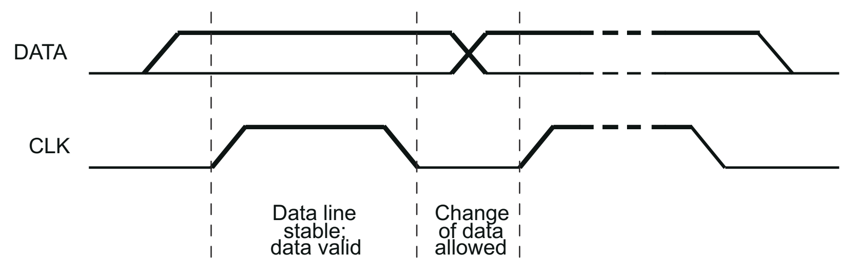


図 8-3. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (R/$\overline{W}$ bit 0) or receive data from the target (R/$\overline{W}$ bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 8-2). This releases the bus and stops the communication link with the addressed target. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

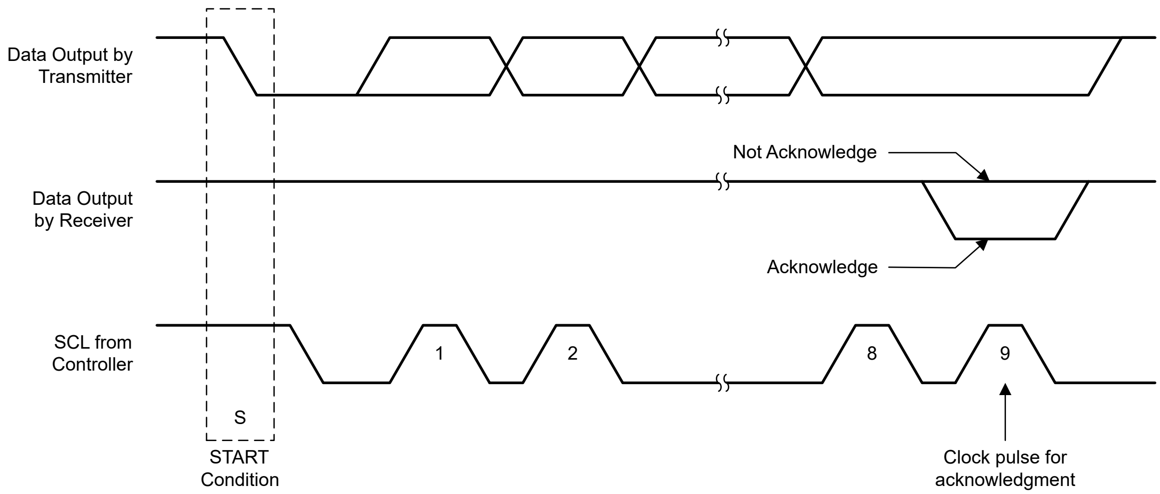


図 8-4. Acknowledge on the I²C Bus

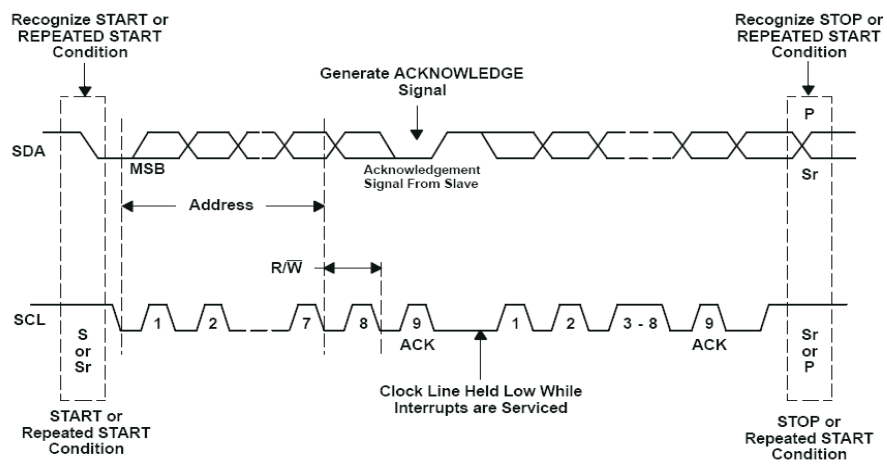


図 8-5. Bus Protocol

8.5.3 HS-Mode Protocol

The controller generates a start condition followed by a valid serial byte containing HS controller code 00001XXX. This transmission is made in F/S-mode at no more than 400 kbps. No device is allowed to acknowledge the HS controller code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

The controller then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the target devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

8.5.4 I²C Update Sequence

The sequence requires a start condition, a valid I²C target address, a register address byte, and a data byte for a single update. After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

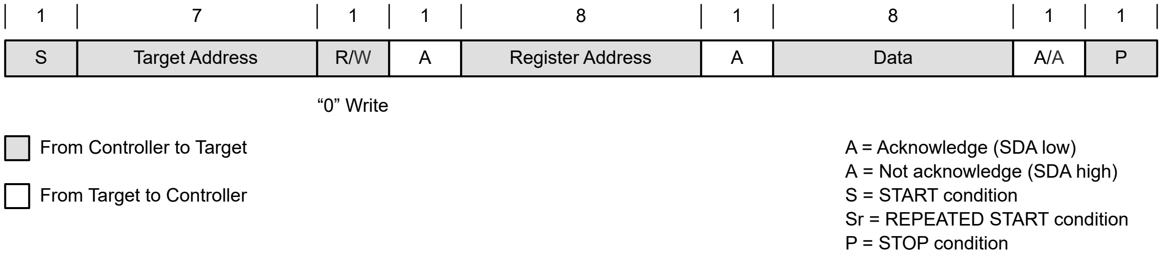


図 8-6. "Write" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

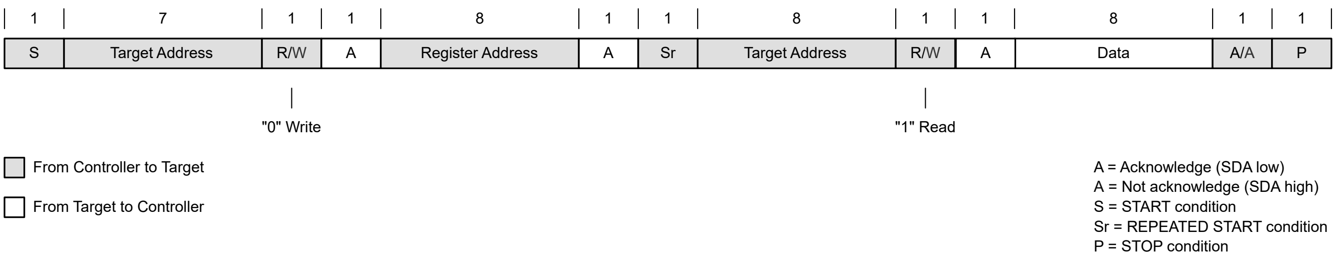


図 8-7. "Read" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

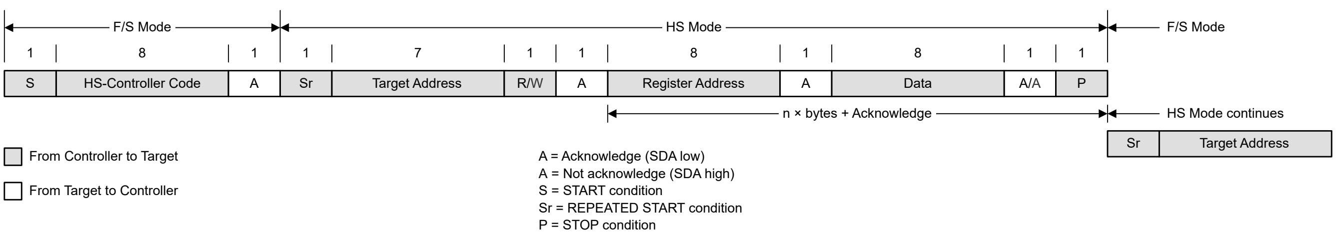


図 8-8. Data Transfer Format in HS-Mode

8.5.5 I²C Register Reset

The I²C registers can be reset by:

- Pulling the input voltage below 1.8 V (typ.)
- A high to low transition on EN
- Setting the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up is begun immediately. After t_{Delay}, the I²C registers can be programmed again.

8.6 Register Map

表 8-5. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V_{OUT} Register 1	0x64	Sets the target output voltage
0x02	V_{OUT} Register 2	0x64	Sets the target output voltage
0x03	CONTROL Register	0x6F	Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags

8.6.1 Target Address Byte

7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	R/$\overline{W}$

The target address byte is the first byte received following the START condition from the controller device. The target addresses can be assigned by an external resistor, see 表 8-1.

8.6.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the target address, the bus controller sends a byte to the device, which contains the address of the register to be accessed.

8.6.3 V_{OUT} Register 1

表 8-6. V_{OUT} Register 1 Description

REGISTER ADDRESS 0X01 READ/WRITE			
BIT	**FIELD**	**VALUE (HEX)**	**OUTPUT VOLTAGE (TYP)**
7:0	VO1_SET	0x00	Voltage Factor * 400 mV
		0x01	Voltage Factor * 405 mV
		...	
		0x64	Voltage Factor * 900 mV
		...	
		0xFE	Voltage Factor * 1670 mV
		0xFF	Voltage Factor * 1675 mV

8.6.4 V_{OUT} Register 2

表 8-7. V_{OUT} Register 2 Description

REGISTER ADDRESS 0X02 READ/WRITE			
BIT	**FIELD**	**VALUE (HEX)**	**OUTPUT VOLTAGE (TYP)**
7:0	VO2_SET	0x00	Voltage Factor * 400 mV
		0x01	Voltage Factor * 405 mV
		...	
		0x64	Voltage Factor * **900 mV** (default value)
		...	
		0xFE	Voltage Factor * 1670 mV
		0xFF	Voltage Factor * 1675 mV

8.6.5 CONTROL Register

表 8-8. CONTROL Register Description

REGISTER ADDRESS 0X03 WRITE ONLY				
BIT	**FIELD**	**TYPE**	**DEFAULT**	**DESCRIPTION**
7	Reset	R/W	0	1 - Reset all registers to default.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change 1 - Force the device in FPWM during output voltage change.
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new start-up without the t_{Delay} period.
4	Enable FPWM Mode	R/W	0	0 - Set the device in power save mode at light loads. 1 - Set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge. 1 - Enable output discharge.
2	Enable HICCUP	R/W	1	0 - Disable HICCUP. Enable latching protection. 1 - Enable HICCUP, Disable latching protection.
0:1	Voltage Ramp Speed	R/W	11	00 - 20mV/µs (0.25 µs/step) 01 - 10 mV/µs (0.5 µs/step) 10 - 5 mV/µs (1 µs/step) 11 - 1 mV/µs (5 µs/step, default)

8.6.6 STATUS Register

表 8-9. STATUS Register Description

REGISTER ADDRESS 0X05 READ ONLY(1)				
BIT	**FIELD**	**TYPE**	**DEFAULT**	**DESCRIPTION**
7:5	Reserved			
4	Thermal Warning	R	0	1: Junction temperature is higher than 130°C.
3	HICCUP	R	0	1: Device has HICCUP status once.
2	Reserved			
1	Reserved			
0	UVLO	R	0	1: The input voltage is less than UVLO threshold (falling edge).

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to its default values.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

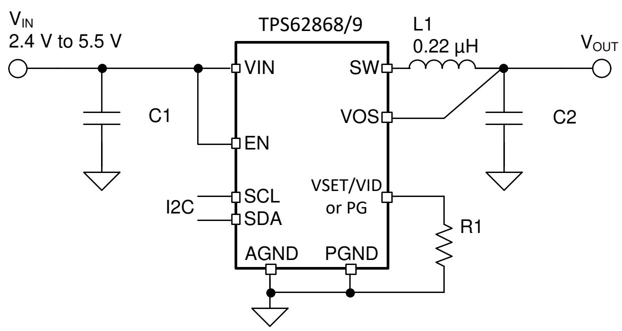


図 9-1. Typical Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	0.9 V
Maximum output current	6 A

表 9-2 lists the components used for the example.

表 9-2. List of Components of 表 9-1

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	2 × 10 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, CL10B106MQ8NRNC	Samsung Electro-Mechanics
C2	2 × 22 µF, Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44L	Murata
L1	0.22 µH, Power inductor, XAL4020-221ME (12 A, 5.81 mΩ)	Coilcraft
R1	Depending on the start-up output voltage, size 0603	Std

(1) See *Third-party Products* disclaimer.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting The Output Voltage

The initial output voltage is set by an external resistor connected to the VSET/VID pin, according to 表 8-1. After the soft start-up, the output voltage can be changed in the V_{OUT} Registers. Refer to 表 8-6 and 表 8-7.

9.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 9-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 9-3. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH][2]	NOMINAL C_{OUT} [µF][3]			
	22	2 x 22 or 47	3 x 22	150
0.24		+[1]	+	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –30%.

9.2.2.3 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 3 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where

- $I_{OUT,MAX}$ = maximum output current
- ΔI_L = inductor current ripple
- f_{SW} = switching frequency
- L = inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. 表 9-4 lists recommended inductors.

表 9-4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING, I_{SAT} [A]	DIMENSIONS [L x W x H mm]	DC RESISTANCE [mΩ]	PART NUMBER
0.22	18.7	4 x 4 x 2	5.81	Coilcraft, XAL4020-221ME
0.24	6.6	2 x 1.6 x 1.2	13	Murata, DFE201612E-R24M

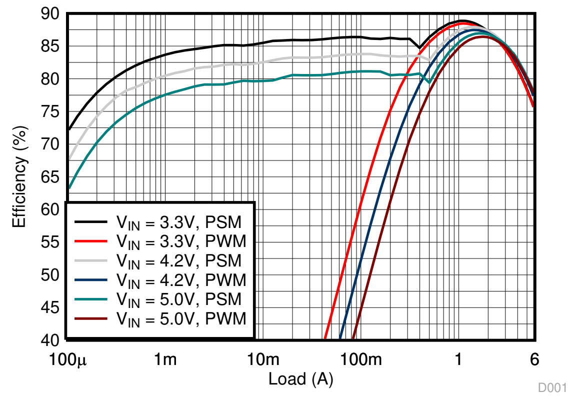
9.2.2.4 Capacitor Selection

The input capacitor is the low-impedance energy source for the converter which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and PGND as close as possible to those pins. For most applications, 8 µF is a sufficient value for the effective input capacitance, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended minimum output effective capacitance is 30 µF; this capacitance can vary over a wide range as outline in the output filter selection table.

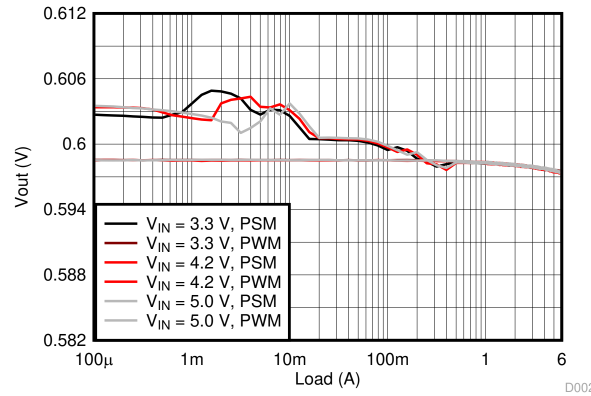
9.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 0.9 V, T_A = 25°C, BOM = 表 9-2, unless otherwise noted.



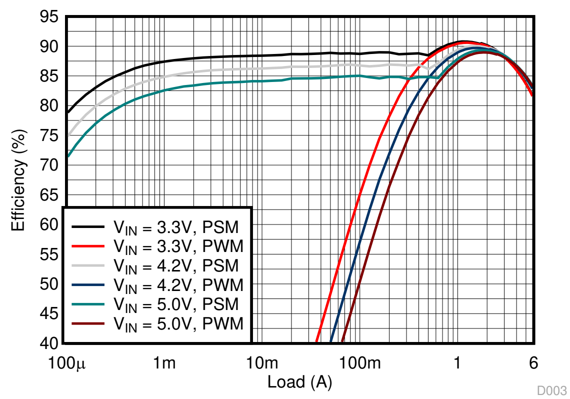
V_{OUT} = 0.6 V

図 9-2. Efficiency



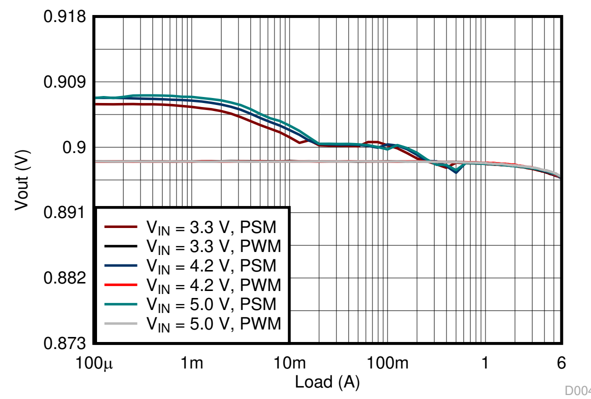
V_{OUT} = 0.6 V

図 9-3. Load Regulation



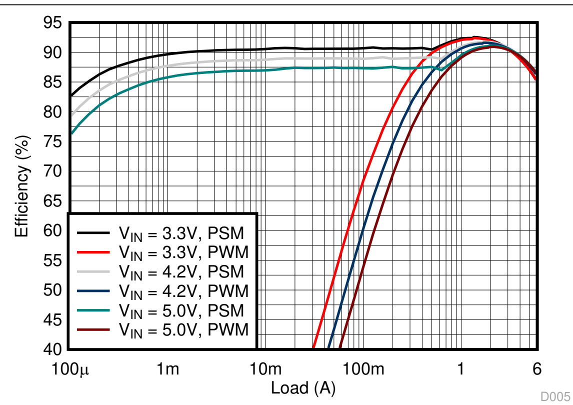
V_{OUT} = 0.9 V

図 9-4. Efficiency



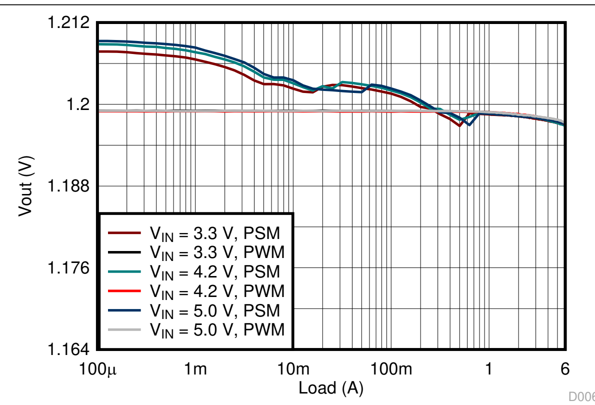
V_{OUT} = 0.9 V

図 9-5. Load Regulation



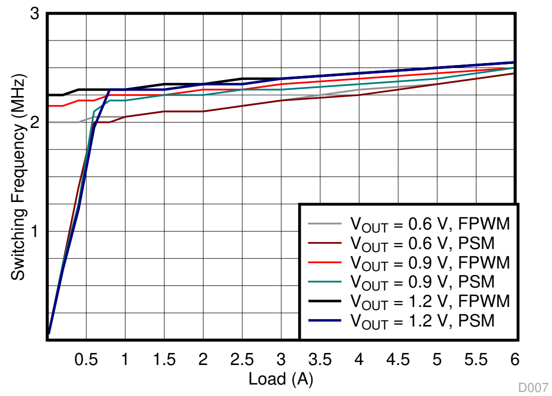
V_{OUT} = 1.2 V

図 9-6. Efficiency



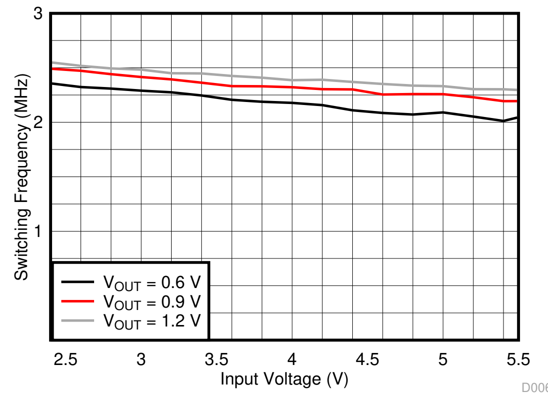
V_{OUT} = 1.2 V

図 9-7. Load Regulation



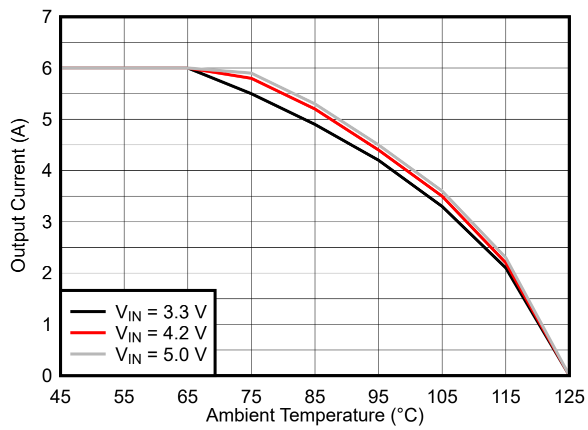
V_{IN} = 5.0 V

図 9-8. Switching Frequency



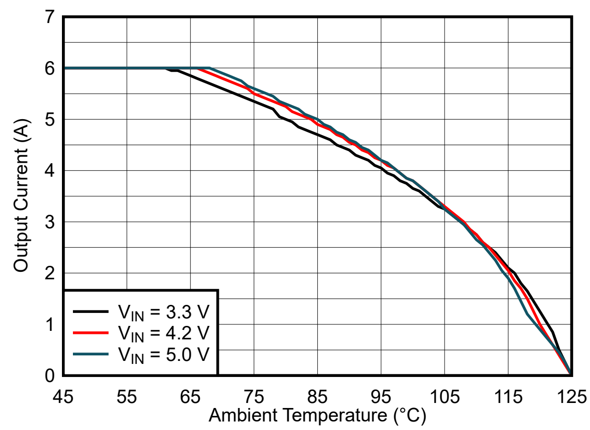
I_{OUT} = 1.0 A

図 9-9. Switching Frequency



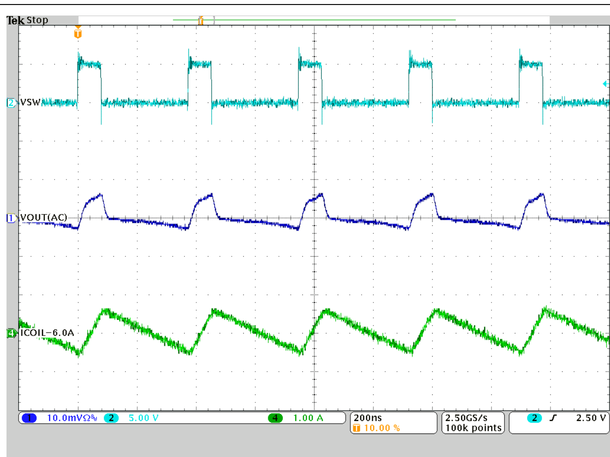
V_{OUT} = 0.9 V θ_{JA} = 60.3°C/W

図 9-10. Thermal Derating



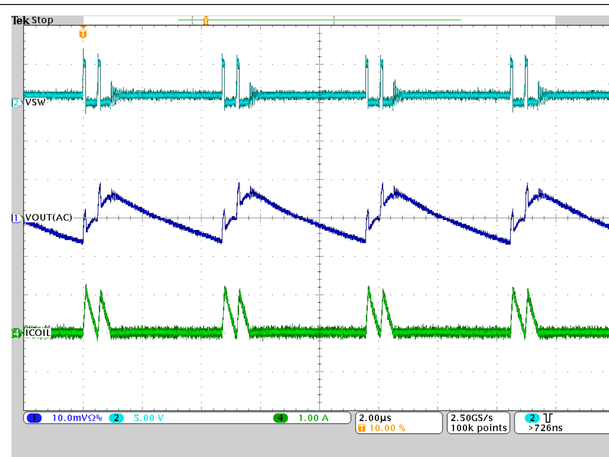
V_{OUT} = 1.675 V θ_{JA} = 60.3°C/W

図 9-11. Thermal Derating



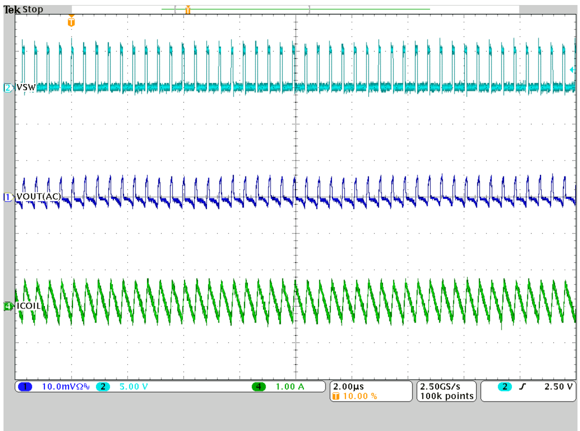
I_{OUT} = 6.0 A

図 9-12. PWM Operation



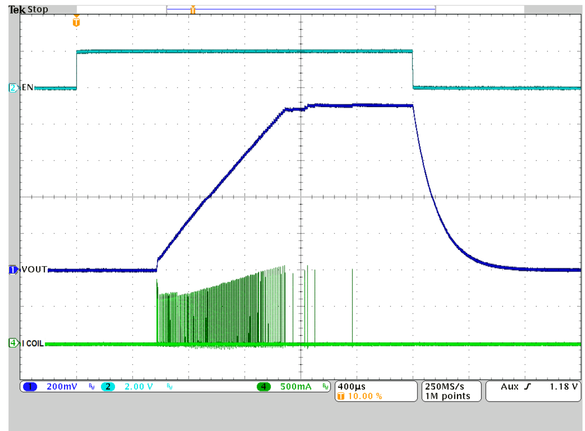
I_{OUT} = 0.1 A

図 9-13. PSM Operation



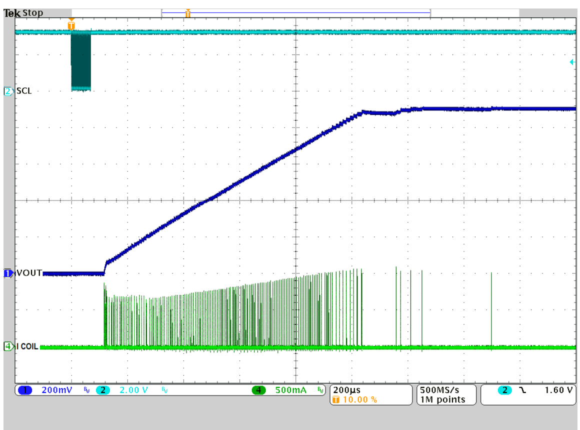
I_{OUT} = 0.1 A

図 9-14. Forced PWM Operation



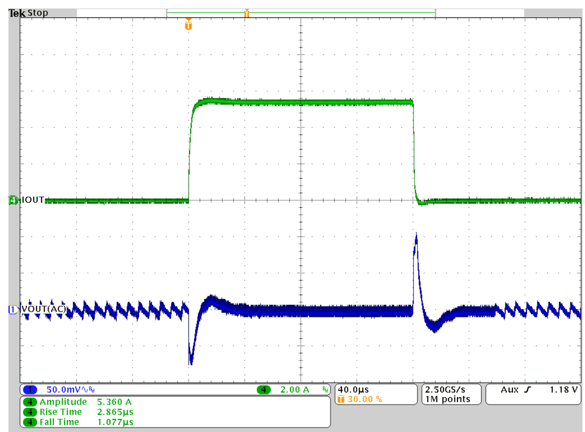
No Load

図 9-15. Startup and Shutdown by EN Pin



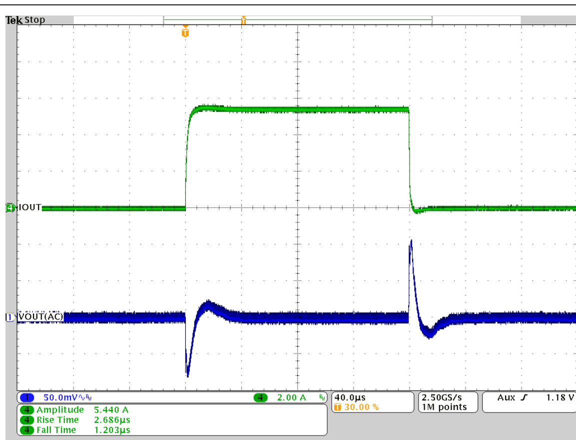
No Load

図 9-16. Start-up by Software Enable Device Bit



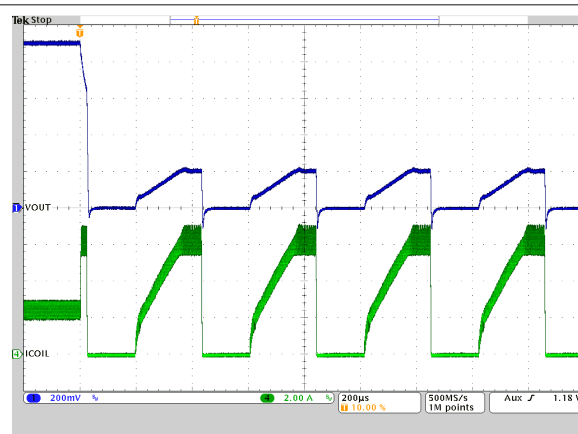
I_{OUT} = 0.06 A to 5.4 A PSM

図 9-17. Load Transient



I_{OUT} = 0.06 A to 5.4 A Forced PWM

図 9-18. Load Transient



I_{OUT} = 2.5 A

図 9-19. HICCUP Protection

9.3 Typical Application – TPS6286x0A and TPS6286x0xC Devices

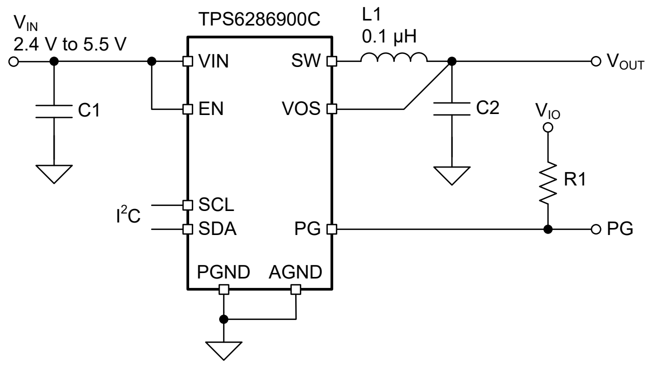


図 9-20. Typical Application

9.3.1 Design Requirements

For this design example, use the parameters listed in 表 9-5 as the input parameters.

表 9-5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	2.4 V to 5.5 V
Output Voltage	0.5 V
Maximum Output Current	6 A

表 9-6 lists the components used in this example.

表 9-6. List of Components of Table 9-5

REFERENCE	DESCRIPTION	MANUFACTURER[1]
C1	2 × 10 µF Ceramic capacitor, 6.3 V, X7R, size 0603, CL10B106MQ8NRNC	Samsung Electro-Mechanics
C2	3 × 22 µF Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44L	Murata
L1	0.1 µH Power inductor, XEL4020-101ME	Coilcraft
R1	10 kΩ, size 0603	Standard

1. See the *Third-Party Products Disclaimer.*

9.3.2 Detailed Design Procedure

9.3.2.1 Setting the Output Voltage

The start-up output voltage of the TPS6286900C device is factory-programmed to 0.5 V and therefore no additional external components are needed. After start-up, the output voltage can be changed by using the I^2C interface to program the VOUT Register 1.

9.3.2.2 Output Filter Design

The inductor and output capacitor form a low-pass filter. To simplify the design process, 表 9-7 outlines possible inductor and capacitor combinations for most applications. Checked cells represent combinations that have been proven for stability by simulation and lab testing. Further combinations, not listed in , should be checked for the specific application.

表 9-7. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH][2]	NOMINAL C_{OUT} [µF][3]			
	22	2 × 22 or 47	3 × 22	150
0.1		+	+[1]	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –30%.

9.3.2.3 Inductor Selection

Inductor selection for the TPS6286x0A and TPS6286x0xC (0.2-V to 0.8375-V) device variants follows the same procedure as for the other device variants (see セクション 9.2.2.3). 表 9-8 lists recommended inductors for the low-voltage device variants.

表 9-8. List of Recommended Inductors

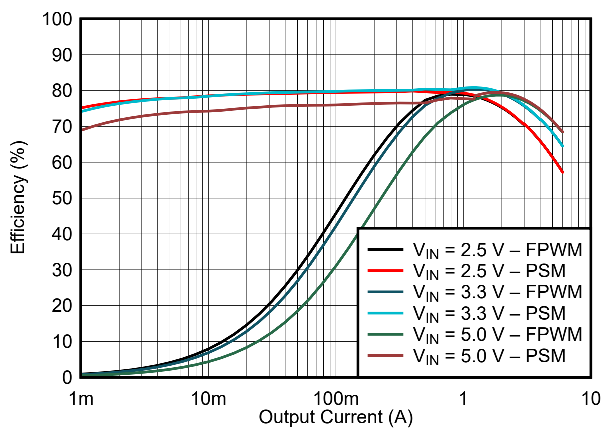
INDUCTANCE [µH]	CURRENT RATING, I_{SAT} [A]	DIMENSIONS [L × W × H mm]	DC RESISTANCE [mΩ]	PART NUMBER
0.1	28.5	4 × 4 × 2	2	Coilcraft, XEL4020-101ME

9.3.2.4 Capacitor Selection

Capacitor selection for the TPS6286x0A and TPS6286x0xC (0.2-V to 0.8375-V) device variants follows the same procedure as for the other device variants (see セクション 9.2.2.4).

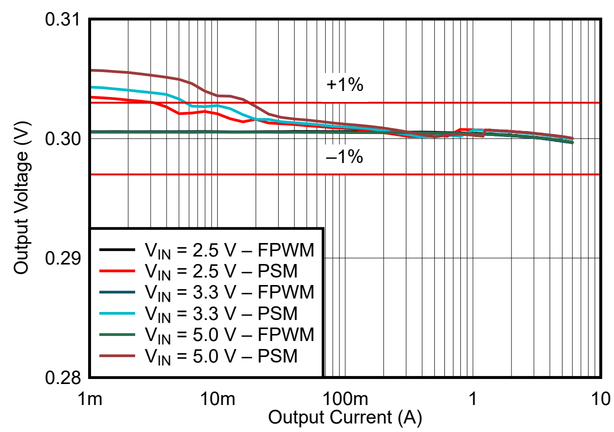
9.3.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 0.5 V, T_A = 25°C, BOM = 表 9-6, unless otherwise noted.



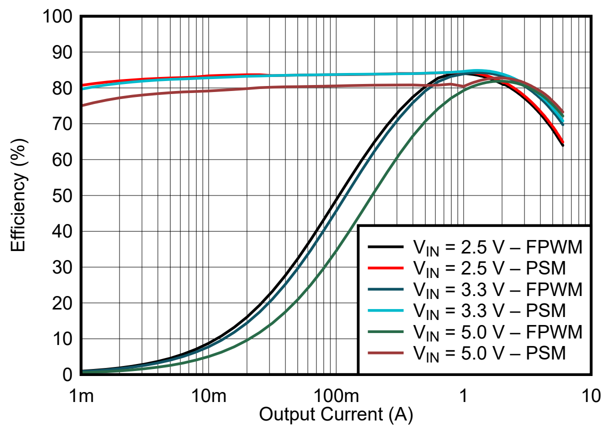
V_{OUT} = 0.3 V

図 9-21. Efficiency



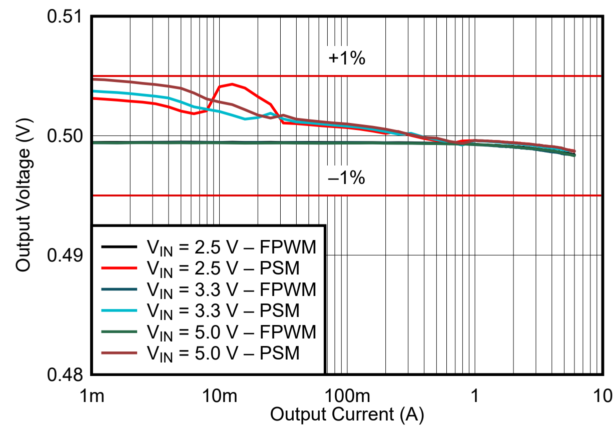
V_{OUT} = 0.3 V

図 9-22. Load Regulation



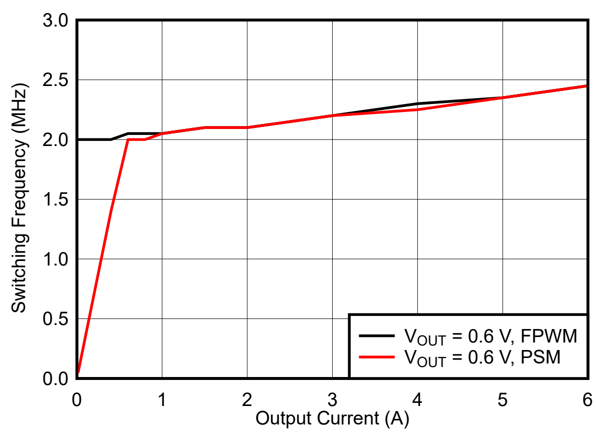
V_{OUT} = 0.5 V

図 9-23. Efficiency



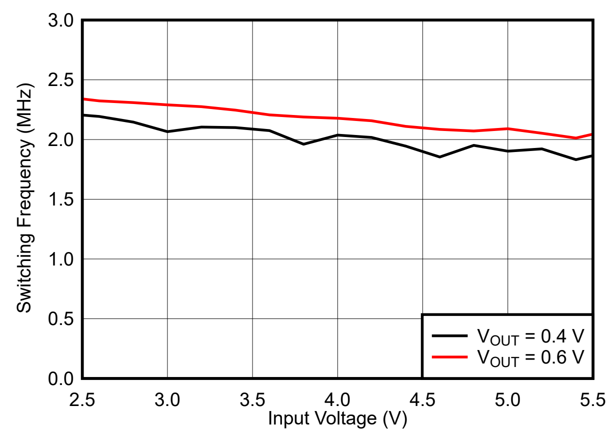
V_{OUT} = 0.5 V

図 9-24. Load Regulation



V_{IN} = 5 V

図 9-25. Switching Frequency



I_{OUT} = 1 A

図 9-26. Switching Frequency

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application. The power supply must avoid a fast ramp down. The falling ramp speed must be slower than 10 mV/µs, if the input voltage drops below V_{UVLO}.

11 Layout

11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device.

- The input/output capacitors and the inductor must be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the PGND to avoid a GND potential shift.
- The sense traces connected to the VOS pin is a signal trace. Special care must be taken to avoid noise being induced. Keep the trace away from SW.
- Refer to 図 11-1 for an example of component placement, routing, and thermal design.

11.2 Layout Example

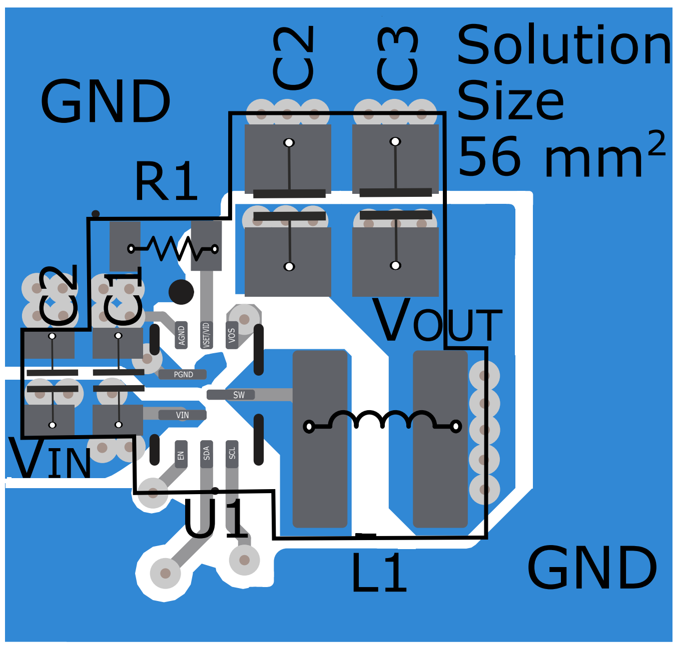


図 11-1. Layout Example

11.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are improving the power dissipation capability of the PCB design and introducing airflow in the system. For more details on how to use the thermal parameters, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

12.3 サポート・リソース

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12.4 Receiving Notification of Documentation Updates

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12.5 Trademarks

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12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6286800CRQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JOH
TPS6286800CRQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JOH
TPS628680ARQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2I8H
TPS628680ARQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2I8H
TPS6286810CRQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JPH
TPS6286810CRQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JPH
TPS628681ARQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2ECH
TPS628681ARQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2ECH
TPS6286820CRQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JQH
TPS6286820CRQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JQH
TPS628682ARQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2IAH
TPS628682ARQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2IAH
TPS6286900CRQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JRH
TPS6286900CRQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JRH
TPS628690ARQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2I7H
TPS628690ARQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2I7H
TPS6286910CRQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JSH
TPS6286910CRQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JSH
TPS628691ARQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2EBH
TPS628691ARQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2EBH
TPS6286920CRQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JTH
TPS6286920CRQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2JTH
TPS628692ARQYR	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2I9H
TPS628692ARQYR.A	Active	Production	VQFN-HR (RQY) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2I9H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[(3)] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[(4)] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[(5)] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[(6)] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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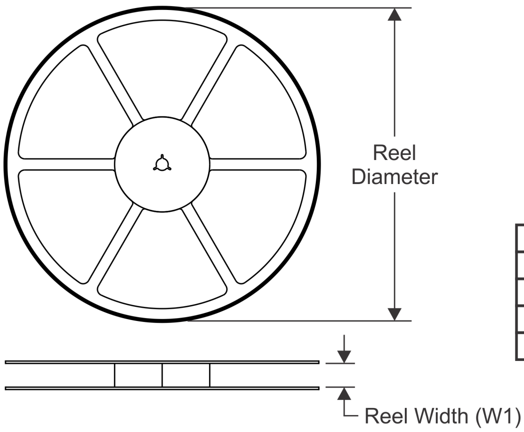
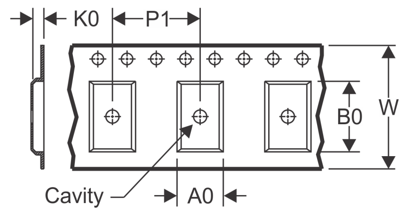
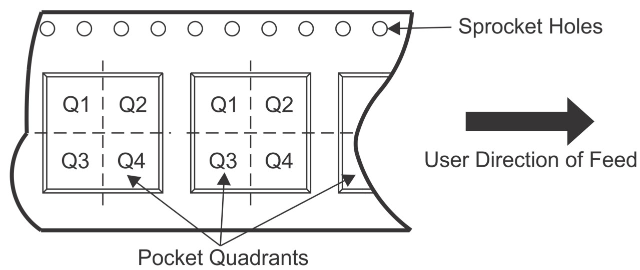
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

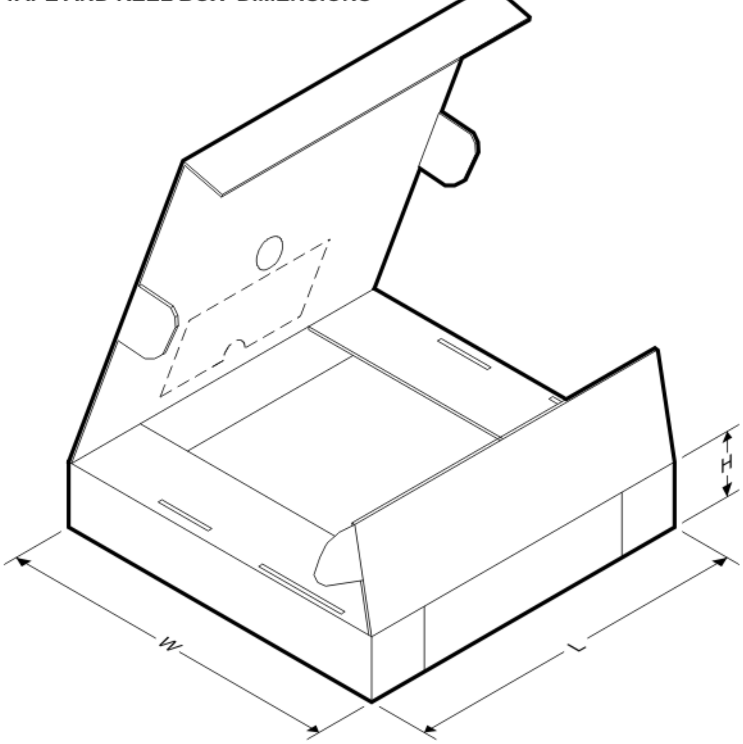


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6286800CRQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628680ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS6286810CRQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628681ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS6286820CRQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628682ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS6286900CRQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628690ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS6286910CRQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628691ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS6286920CRQYR	VQFN-	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1

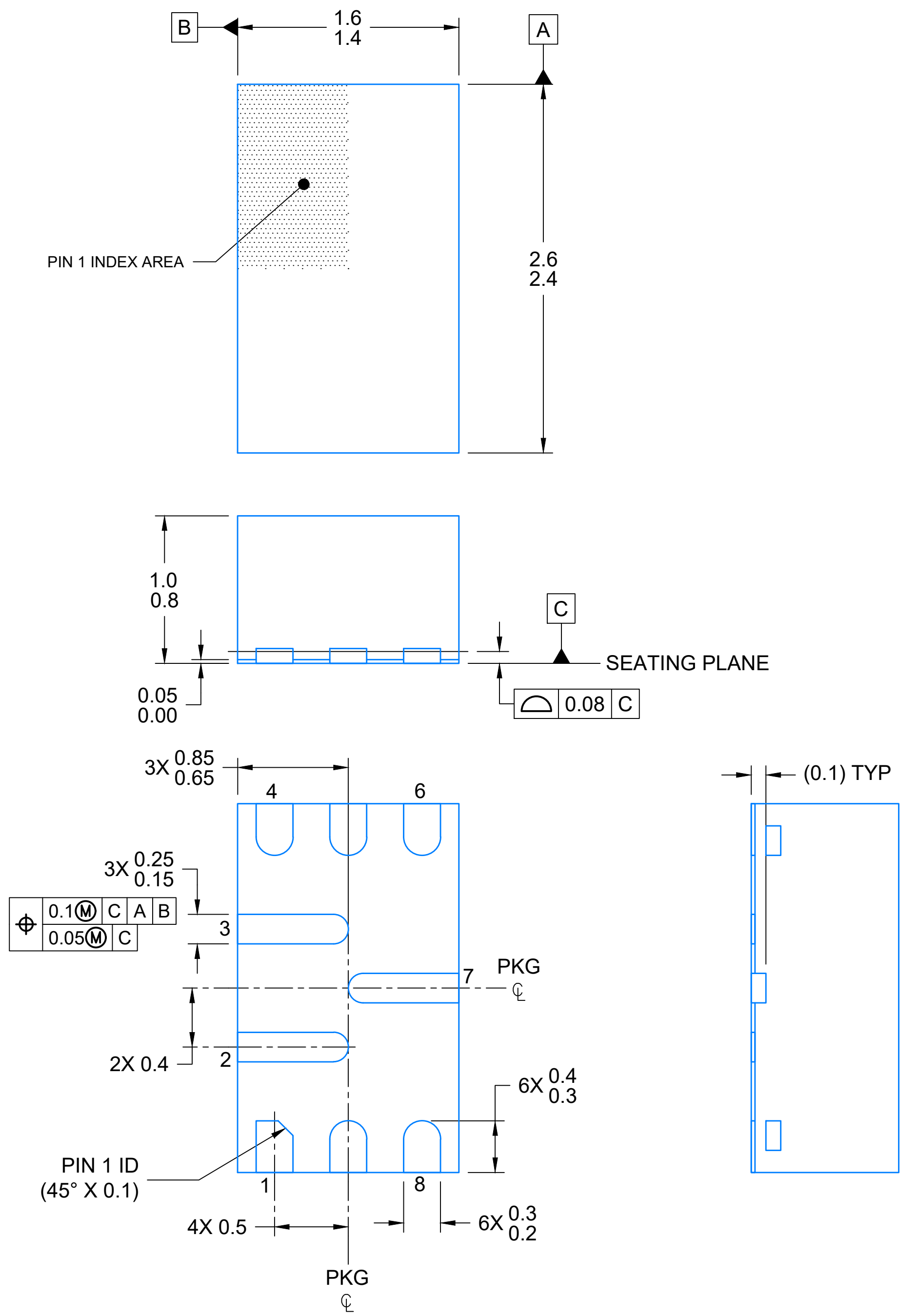
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	HR											
TPS628692ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6286800CRQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628680ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS6286810CRQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628681ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS6286820CRQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628682ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS6286900CRQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628690ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS6286910CRQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628691ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS6286920CRQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628692ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0



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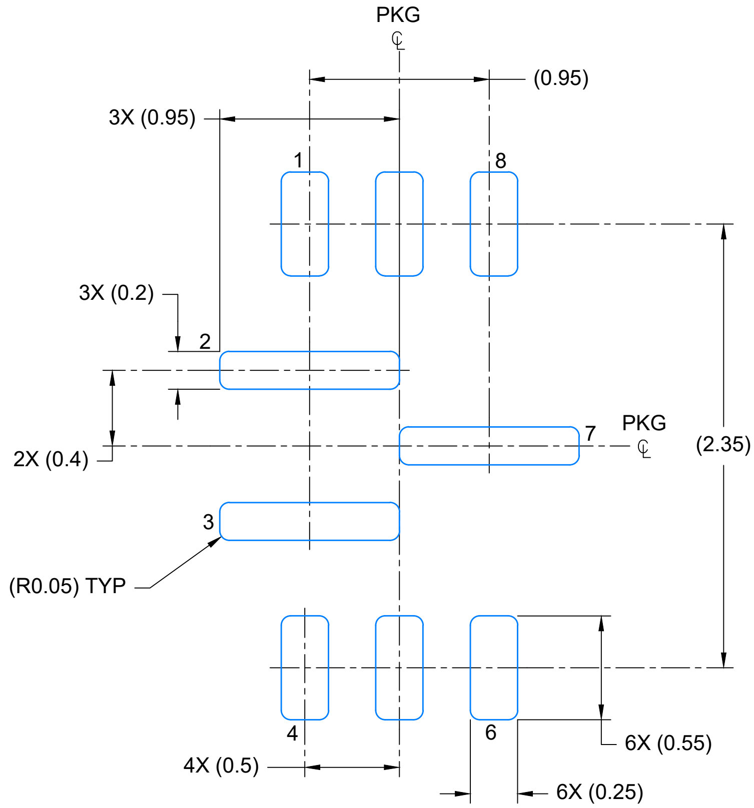
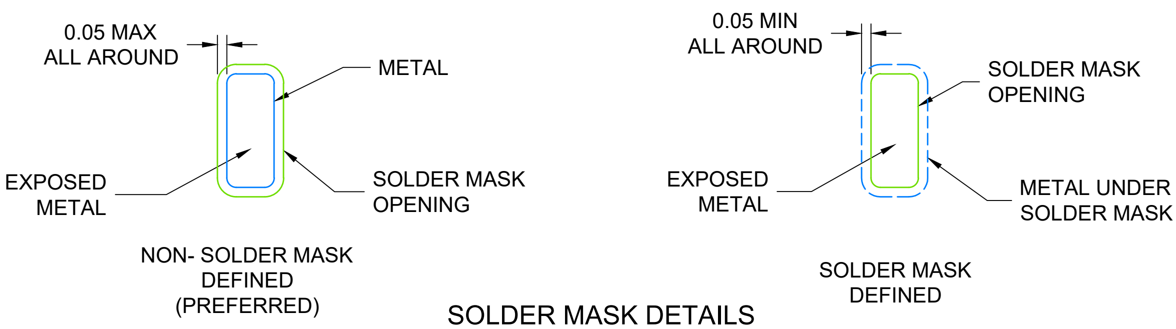
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS
NOT TO SCALE

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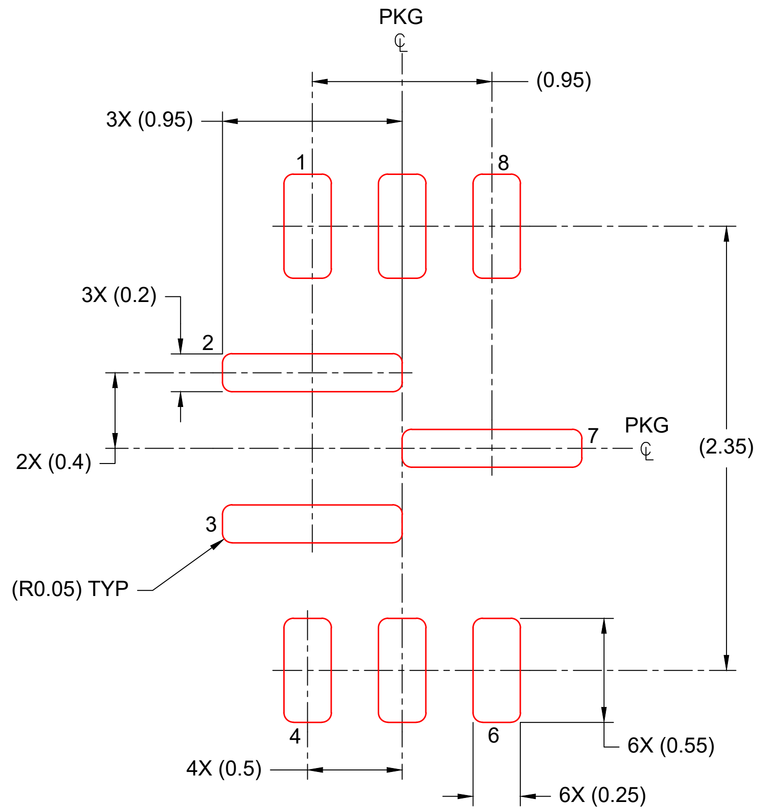
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月