

TPS63802 DFN パッケージの 2A、高効率、低 I_Q 昇降圧コンバータ

1 特長

- 入力電圧範囲: 1.3V~5.5V
 - デバイスのスタートアップ時入力電圧は 1.8V を超えること
- 出力電圧範囲: 1.8V~5.2V (可変)
- 出力電流: 2A ($V_I \geq 2.3V$, $V_O = 3.3V$)
- 全負荷範囲にわたって高効率を実現
 - 動作時の静止電流: 11 μ A
 - パワーセーブ・モードと強制 PWM モードのモード選択
- ピーク電流昇降圧モード・アーキテクチャ
 - 降圧、昇降圧、昇圧動作モード間の遷移点を定義済み
 - 順方向および逆方向電流動作
 - あらかじめ出力にバイアスを印加した状態で起動
- 安全で堅牢な動作を実現する機能
 - ソフト・スタート内蔵
 - 過熱および過電圧保護
 - 負荷の切り離しを伴う真のシャットダウン機能
 - 順方向および逆方向の電流制限
- 小さなソリューション・サイズ: 21.5mm²
 - 小型の SON/DFN パッケージ (QFN と類似)
 - 小型の 0.47 μ H インダクタ
 - 最小 22 μ F の出力コンデンサで動作
- WEBENCH® Power Designer により、TPS63802 を使用するカスタム設計を作成

2 アプリケーション

- システム・プリレギュレータ (トラッキングおよびテレメトリクス、携帯型 POS、ホーム・オートメーション、IP ネットワーク・カメラ)
- ポイント・オブ・ロード・レギュレーション (有線センサ、ポートやケーブルのアダプタとドングル、電子スマート・ロック、IoT)
- バッテリー・バックアップ電源 (電力量計、データ・コンセンサントレータ、電力品質メータ)
- 熱電デバイスの電源 (TEC、光モジュール)
- 汎用電圧スタビライザおよびコンバータ

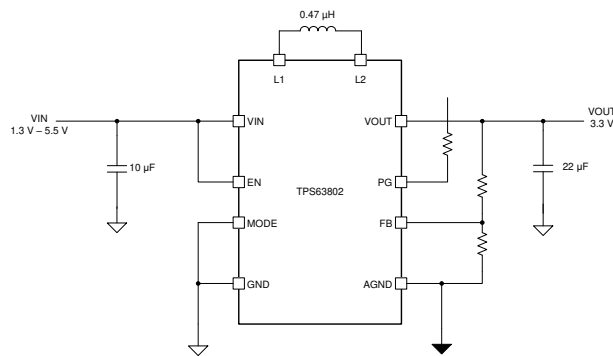
3 概要

TPS63802 は、高効率で出力電流の大きい昇降圧型コンバータです。入力電圧に応じて自動的に昇圧モード、降圧モード、革新的な 4 サイクル昇降圧モード (入力電圧が出力電圧とほぼ等しい場合) のいずれかで動作します。モード間の遷移は定義されたスレッシュホールドで行い、出力電圧リップルを減らすためモード内での不要な切り替えは行いません。本デバイスの出力電圧は、広い出力電圧範囲内で抵抗分圧器を使用して個別に設定されます。静止電流が 11 μ A であるため、無負荷または軽負荷条件で最高の効率が得られます。

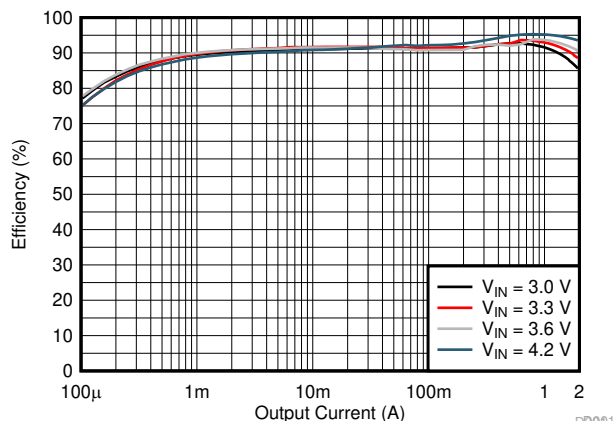
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS63802	10 ピン VSON-HR (0.5mm ピッチ)	3.0mm × 2.0mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション



効率と出力電流との関係 ($V_O = 3.3V$)

DD001



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4 Revision History

Changes from Revision C (June 2020) to Revision D (January 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
Changes from Revision B (September 2019) to Revision C (June 2020)	Page
• Added device comparison	3
• Changed 1x 22 μ F to 2x 22 μ F.....	19
• Changed Part Number from TPS63802RMW to TPS63802DLA	20
• Change MODE from High to Low in <i>Application Curves</i>	20
• Deleted layout guideline to separate AGND and PGND	28
• Changed Use a common-power GND, but connect AGND and PGND through via at a different layer. to Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.	28
Changes from Revision A (January 2019) to Revision B (September 2019)	Page
• デバイスのステータスを「事前情報」から「量産データ」に変更.....	1
• パッケージ・グループ名を変更.....	1
• Added related documentation	29

5 概要 (続き)

TPS63802 は、1.4mm × 2.3mm の熱的に強化された HotRod™ デュアル・フラット鉛フリー (DFN) パッケージで供給されます。部品数が非常に少ないため、小さなソリューションを実現できます。

6 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	$I_{(Q,VIN)}$ (TYP.)	$C_{(O,EFF)}$ (MIN.)	SWITCH CURRENT LIMIT BOOST (MIN.)	PACKAGE
TPS63802	Adjustable	11 μ A	7 μ F	4 A	VSON
SIMILAR TI PARTS					
TPS63805	Adjustable	11 μ A	7 μ F	4 A	WCSP
TPS63810 TPS63811	fixed: 3.3 V/3.45 V or I ² C programmable	15 μ A	16 μ F	5.2 A	WCSP

7 Pin Configuration and Functions

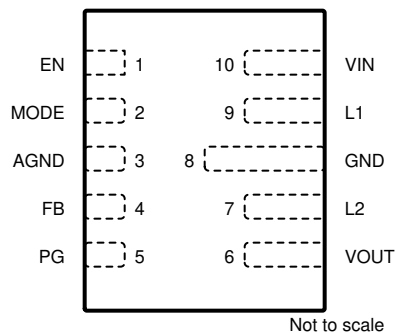


图 7-1. 10-Pin DLA Package (Top View)

表 7-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
EN	1	Device Enable input. Set HIGH to enable and LOW to disable. It must not be left floating.
MODE	2	PFM/PWM mode selection. Set LOW for power save mode, set HIGH for forced PWM mode. It must not be left floating.
AGND	3	Analog ground
FB	4	Voltage feedback sensing pin
PG	5	Power good indicator, open-drain output
VOUT	6	Power stage output
L2	7	Connection for inductor
GND	8	Power ground
L1	9	Connection for inductor
VIN	10	Supply voltage input

8 Specifications

8.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, L1, L2, EN, MODE, VOUT, FB, PG	−0.3	6	V
	L1, L2 (AC, less than 10 ns)	−3	9	V
Operating junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

8.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _I	Input voltage	1.3 ⁽¹⁾		5.5	V
V _O	Output voltage	1.8		5.2 ⁽²⁾	V
C _I	Effective capacitance connected to V _{IN}	4	5		μF
L	Effective inductance	0.37	0.47	0.57	μH
C _O	TPS63802 Effective capacitance connected to V _{OUT}	1.8 V ≤ V _O ≤ 2.3 V		10	μF
		V _O > 2.3 V		7	μF
T _J	Operating junction temperature	−40		125	°C

- (1) Minimum startup voltage of V_I > 1.8 V until power good
- (2) V_O margin for accuracy and load steps is considered in absolute maximum ratings

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

THERMAL METRIC		TPS63802	UNIT
		VSON	
		10 PINS	
R _{ΘJA}	Junction-to-ambient thermal resistance	81.0	°C/W
R _{ΘJC(top)}	Junction-to-case (top) thermal resistance	36.4	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	23.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	23.5	°C/W
R _{ΘJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

8.5 Electrical Characteristics

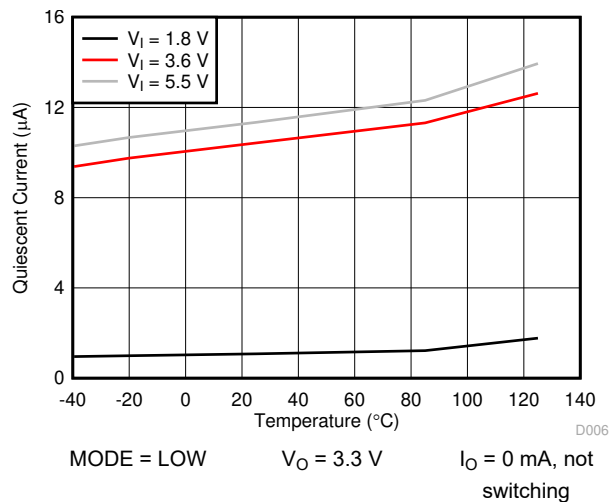
V_{IN} = 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5.2 V, T_J = -40°C to $+125^{\circ}\text{C}$, typical values are at V_{IN} = 3.6 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$V_{IN,LOAD}$	Minimum input voltage for full load, once started	$I_{OUT} = 2\text{ A}$, $V_{OUT} = 3.3\text{ V}$, $T_J = 25^{\circ}\text{C}$		2.3		V
$I_{Q,VIN}$	Quiescent current into VIN	TPS63802; $T_J = 25^{\circ}\text{C}$, $EN = V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$, not switching		11		μA
I_{SD}	Shutdown current into VIN	$EN = \text{low}$, $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 0\text{ V}$		45	600	nA
UVLO	Undervoltage lockout threshold	V_{IN} falling, $V_{OUT} \geq 1.8\text{ V}$, once started	1.2	1.25	1.29	V
	Undervoltage lockout threshold	V_{IN} rising	1.6	1.7	1.79	V
T_{SD}	Thermal shutdown	Temperature rising		150		$^{\circ}\text{C}$
$T_{SD,HYST}$	Thermal shutdown hysteresis			20		$^{\circ}\text{C}$
SOFT-START, POWER GOOD						
T_{ramp}	Soft-start, Current limit ramp time	$T_J = 25^{\circ}\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_O = 3.5\text{ A}$, time from first switching to power good		224		μs
T_{delay}	Delay from EN-edge until rising V_{OUT}	$T_J = 25^{\circ}\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$, Delay from EN-edge until rising first switching		321		μs
LOGIC SIGNALS EN, MODE						
$V_{THR,EN}$	Threshold Voltage rising for EN-Pin		1.07	1.1	1.13	V
$V_{THF,EN}$	Threshold Voltage falling for EN-Pin		0.97	1	1.03	V
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
$V_{PG,rising}$	Power Good threshold voltage	V_{OUT} rising, referenced to V_{OUT} nominal		95		%
$V_{PG,falling}$		V_{OUT} falling, referenced to V_{OUT} nominal		90		%
$V_{PG,Low}$	Power Good low-level output voltage	$I_{SINK} = 1\text{ mA}$			0.4	V
$t_{PG,delay}$	Power Good delay time	V_{FB} falling		14		μs
I_{lkg}	Input leakage current			0.01	0.2	μA
OUTPUT						
I_{SD}	Shutdown current into V_{OUT}	$EN = \text{low}$, $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3.3\text{ V}$		± 0.5	± 600	nA
V_{FB}	Feedback Regulation Voltage			500		mV
V_{FB}	Feedback Voltage accuracy	PWM mode	-1		1	%
	Overvoltage Protection Threshold	V_{OUT} rising	5.5	5.7	5.9	V
		V_{IN} rising	5.5	5.7	5.9	V
$I_{PWM/PFM}$	Peak Inductor Current to enter PFM-Mode	$V_{IN} = 3.6\text{ V}$; $V_{OUT} = 3.3\text{ V}$		1.06		A
I_{FB}	Feedback Input Bias Current	$V_{FB} = 500\text{ mV}$		5	100	nA
I_{PK}	Peak Current Limit, Boost Mode	TPS63802; $V_{IN} \geq 2.5\text{ V}$	4	5	5.75	A
	Peak Current Limit, Buck-Boost Mode			5		A
	Peak Current Limit, Buck Mode			3.8		A
$I_{PK,Reverse}$	Peak Current Limit for Reverse Operation	$V_I = 5\text{ V}$, $V_O = 3.3\text{ V}$		-0.9		A
Buck $R_{DS,ON}$	High-side FET on-resistance	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_{(L2)} = 0.19\text{ A}$	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_O = 0.5\text{ A}$	47		m Ω
	Low-side FET on-resistance	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_{(L2)} = 0.19\text{ A}$	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_O = 0.5\text{ A}$	30		m Ω
Boost $R_{DS,ON}$	High-side FET on-resistance	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_{(L1)} = 0.19\text{ A}$	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_O = 0.5\text{ A}$	43		m Ω
	Low-side FET on-resistance	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_{(L1)} = 0.19\text{ A}$	$V_{IN} = 3\text{ V}$, $V_{OUT} = 3.3\text{ V}$; $I_O = 0.5\text{ A}$	18		m Ω

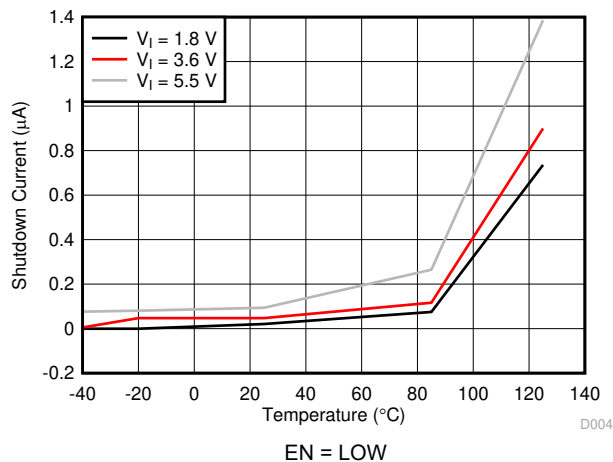
V_{IN} = 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5.2 V, T_J = -40°C to $+125^{\circ}\text{C}$, typical values are at V_{IN} = 3.6 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sw}	Inductor Switching Frequency, Boost Mode	V_{IN} = 2.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C		2.1		MHz
	Inductor Switching Frequency, Buck-Boost Mode	V_{IN} = 3.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C		1.4		MHz
	Inductor Switching Frequency, Buck Mode	V_{IN} = 4.3, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C		1.6		MHz
	Line regulation	V_{IN} = 2.4 V to 5.5 V, V_{OUT} = 3.3V, I_{OUT} = 2 A		0.3		%
	Load regulation	V_{IN} = 3.6 V, V_{OUT} = 3.3V, I_{OUT} = 0 A to 2 A, forced-PWM mode		0.1		%

8.6 Typical Characteristics



8-1. Quiescent Current vs. Temperature



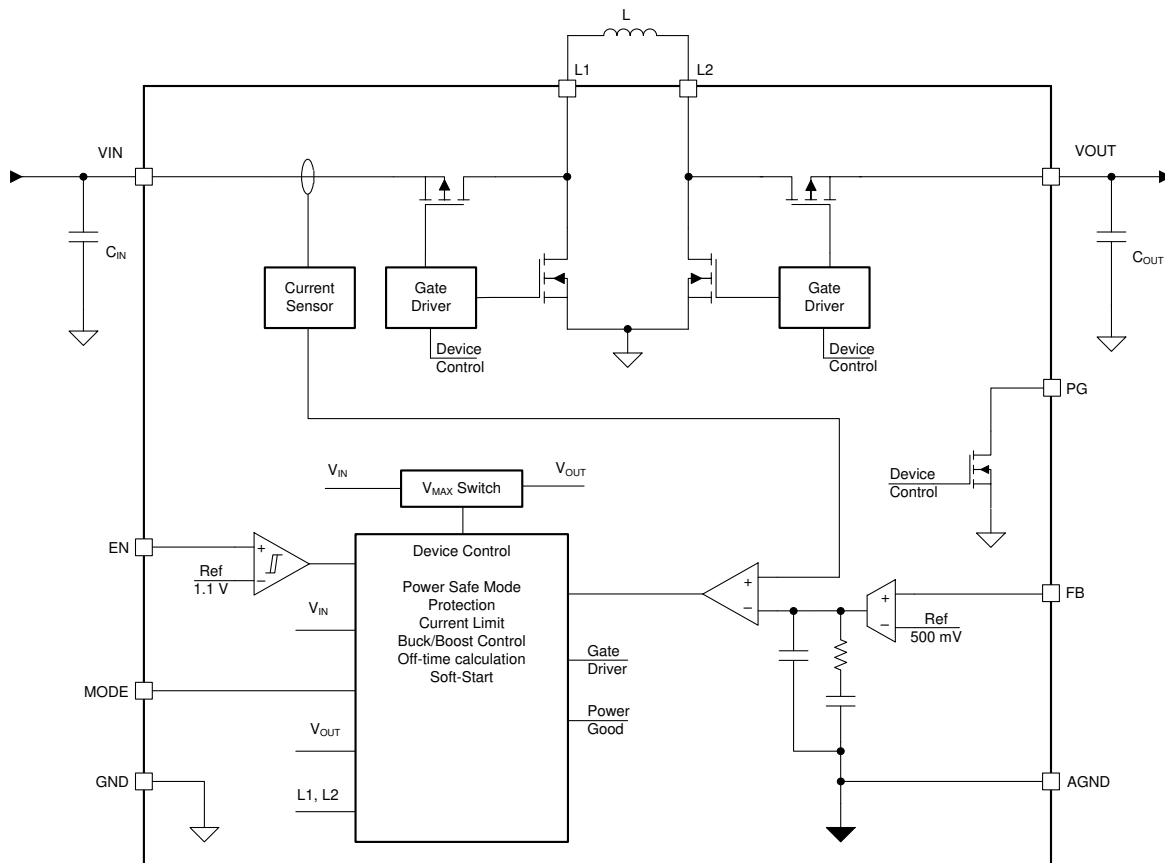
8-2. Shutdown Current vs. Temperature

9 Detailed Description

9.1 Overview

The TPS63802 buck-boost converter uses four internal switches to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output load range. To regulate the output voltage at all possible input voltage conditions, the device automatically transitions between buck, buck-boost, and boost operation as required by the operating conditions. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. When the input voltage is close to the output voltage, it operates in a 3-cycle buck-boost operation. In this mode, all four switches are active (see [セクション 9.4.1.3](#)). The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep high efficiency over the complete input voltage range. The device provides a seamless transition between all modes.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Control Loop Description

The TPS63802 uses a peak current mode control architecture. It has an inner current loop where it measures the peak current of the boost high-side MOSFET and compares it to a reference current. This current is the output of the outer voltage loop. It measures the output voltage via the FB-pin and compares it with the internal voltage reference. That means, the outer voltage loop measures the voltage error ($V_{REF}-V_{FB}$), and transforms it into the system current demand (I_{REF}) for the inner current loop.

Figure 9-1 shows the simplified schematic of the control loop. The error amplifier and the type-2 compensation represent the voltage loop. The voltage output is converted into the reference current I_{REF} and fed into the current comparator.

The scheme shows the skip-comparator handling the power-save mode (PFM) to achieve high efficiency at light loads. See Section 9.4.2 for further details.

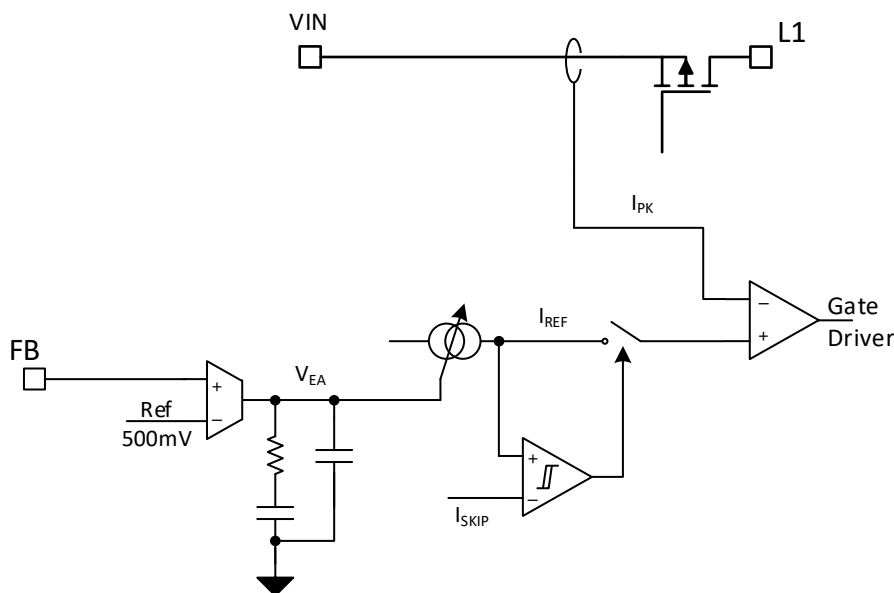


Figure 9-1. Control Loop Architecture Scheme

9.3.2 Precise Device Enable: Threshold- or Delayed Enable

The enable-pin is a digital input to enable or disable the device by applying a high or low level. The device enters shutdown when EN is set low. In addition, this input features a precise threshold and can be used as a comparator that enables and disables the part at a defined threshold. This allows you to drive the state by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. The enable pin can also be used with an external voltage divider to set a user-defined minimum supply voltage. For proper operation, the EN pin must be terminated and must not be left floating.

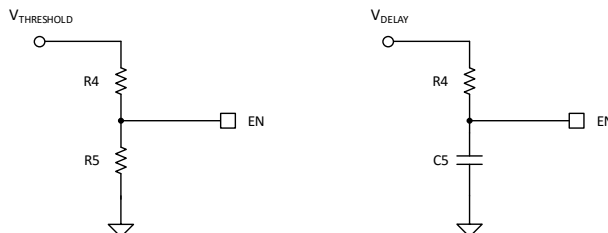


Figure 9-2. Circuit Example for How to Use the Precise Device Enable Feature

9.3.3 Mode Selection (PFM/PWM)

The mode-pin is a digital input to enable the automatic PWM/PFM mode that features the highest efficiency by allowing pulse-frequency-modulation for lower output currents. This mode is enabled by applying a low level. The device can be forced in PWM operation regardless of the output current to achieve minimum output ripple by applying a high level. This pin must not be left floating.

9.3.4 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. It activates the device once the input voltage (V_I) has increased the $UVLO_{rising}$ value. Once active, the device allows operation down to even smaller input voltages, which is determined by the $UVLO_{falling}$. This behavior requires V_O to be higher than the minimum value of 1.8 V.

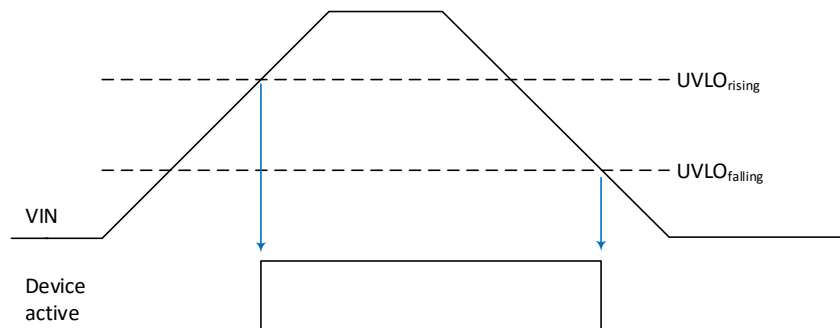


FIG 9-3. Rising and Falling Undervoltage Lockout Behavior

9.3.5 Soft Start

To minimize inrush current and output voltage overshoot during start-up, the device features a controlled soft start-up. After the device is enabled, the device starts all internal reference and control circuits within the enable delay time, T_{delay} . After that, the maximum switch current limit rises monotonically from 0 mA to the current limit. The loop stops switching once V_O is reached. This allows a quick output voltage ramp for small capacitors at the output. The bigger the output capacitor, the longer it takes to settle V_O . A potential load during start-up will lengthen the duration of the output voltage ramp as well. The gradual ramp of the current limit allows a small inrush current for no-load conditions, as well as the possibility to start into high loads at start-up.

The converter can start-up into pre-biased loads by a forced operation in PFM during the soft-start until the first switching cycle request from the output voltage control loop.

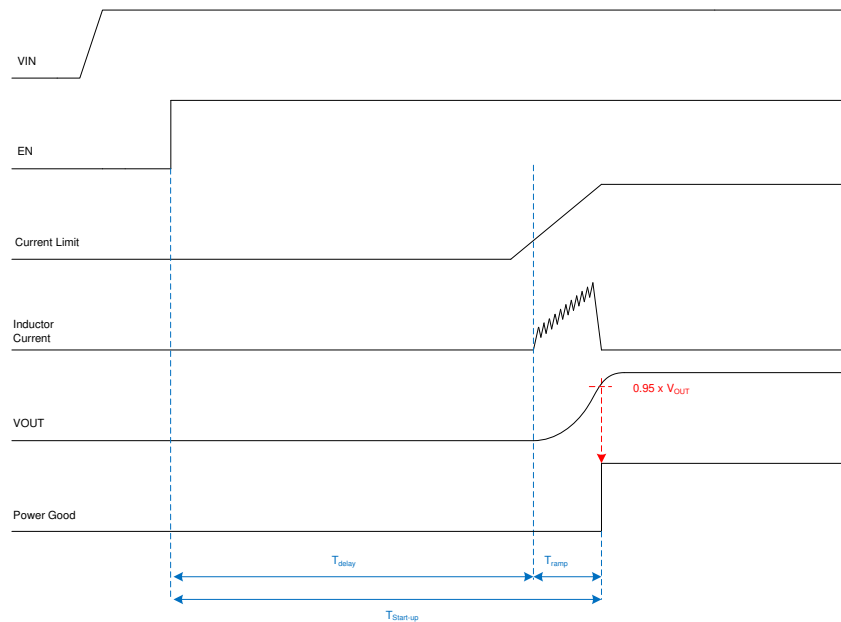


图 9-4. Device Start-up Scheme

9.3.6 Adjustable Output Voltage

The device's output voltage is adjusted by applying an external resistive divider between V_O , the FB-pin, and GND. This allows you to program the output voltage in the recommended range. The divider must provide a low-side resistor of less than 100 k Ω . The high-side resistor is chosen accordingly.

9.3.7 Overtemperature Protection - Thermal Shutdown

The device has a built-in temperature sensor which monitors the junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at junction temperatures at the overtemperature threshold.

9.3.8 Input Overvoltage - Reverse-Boost Protection (IVP)

The TPS63802 can operate in reverse mode where the device transfers energy from the output back to the input. If the source is not able to sink the reverse current, the negative current builds up a charge to the input capacitance and V_{IN} rises. To protect the device and other components from that scenario, the device features an input voltage protection (IVP) for reverse boost operation. Once the input voltage is above the threshold, the converter forces PFM mode and the negative current operation is interrupted.

The PG signal goes low to indicate that behavior.

9.3.9 Output Overvoltage Protection (OVP)

In case of a broken feedback-path connection, the device can lose V_O information and is not able to regulate. To avoid an uncontrolled boosting of V_O , the TPS63802 features output overvoltage protection. It measures the voltage on the VOUT pin and stops switching when V_O is greater than the threshold to avoid harm to the converter and other components.

9.3.10 Power-Good Indicator

The power good goes high-impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. This feature also indicates overvoltage and device shutdown cases as shown in 表 9-1. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used to sequence multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 9-1. Power-Good Indicator Truth Table

LOGIC SIGNALS					PG LOGIC STATUS
EN	V _O	V _I	OVP	IVP	
X	< 1.8 V	< UVLO_R	X	X	Undefined
LOW	X	> UVLO_F	X	X	LOW
HIGH	V _O < 0.9 × target-V _O	> 1.3V	X	X	LOW
HIGH	X	> UVLO_F	HIGH	X	LOW
HIGH	X	> UVLO_F	X	HIGH	LOW
HIGH	V _O > 0.95 × target-V _O	> UVLO_F	LOW	LOW	HIGH Z

9.4 Device Functional Modes

9.4.1 Peak-Current Mode Architecture

The TPS63802 is based on a peak-current mode architecture. The error amplifier provides a peak-current target (voltage that is translated into an equivalent current, see 图 9-1), based on the current demand from the voltage loop. This target is compared to the actual inductor current during the ON-time. The ON-time is ended once the inductor current is equal to the current target and OFF-time is initiated. The OFF-time is calculated by the control and a function of V_I and V_O.

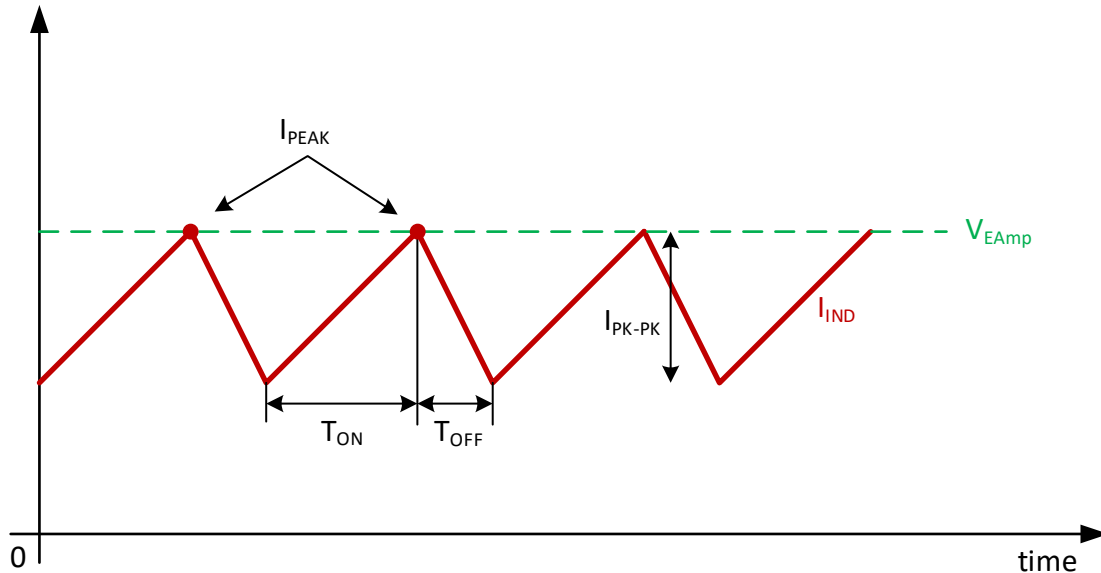


图 9-5. Peak-Current Architecture Operation

9.4.1.1 Reverse Current Operation, Negative Current

When the TPS63802 is forced to PWM operation (MODE = HIGH), the device current can flow in reverse direction. This happens by the negative current capability of the TPS63802. The error amplifier provides a peak-current target (voltage that is translated into an equivalent current, see 图 9-1), even if the target has a negative value. The maximum average current is even more negative than the peak current.

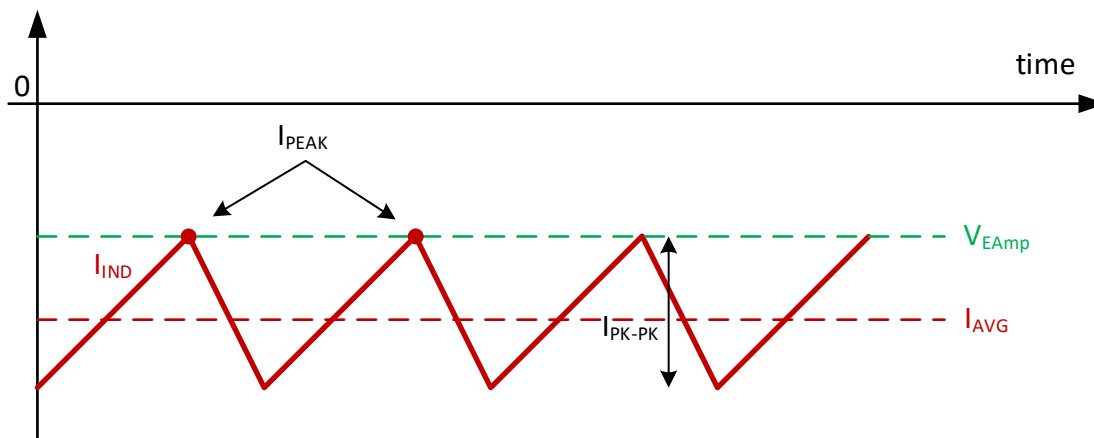


图 9-6. Peak-Current Operation, Reverse Current

9.4.1.2 Boost Operation

When V_I is smaller than V_O (and the voltages are not close enough to trigger buck-boost operation), the TPS63802 operates in boost mode where the boost high-side and low-side switches are active. The buck high-side switch is always turned on and the buck low-side switch is always turned off. This lets the TPS63802 operate as a classical boost converter.

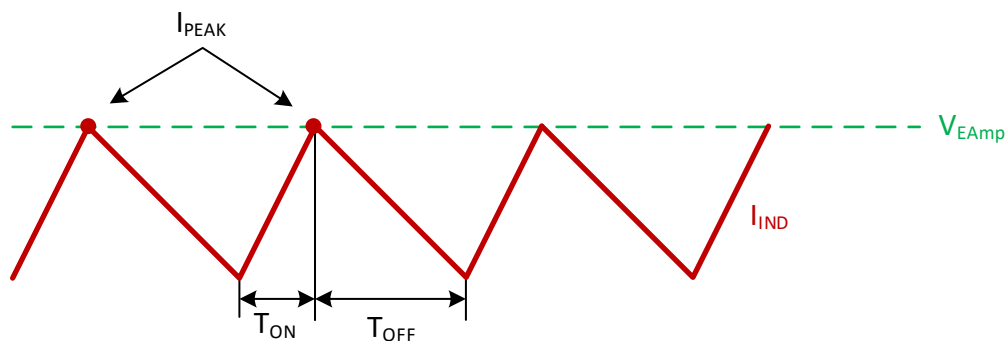
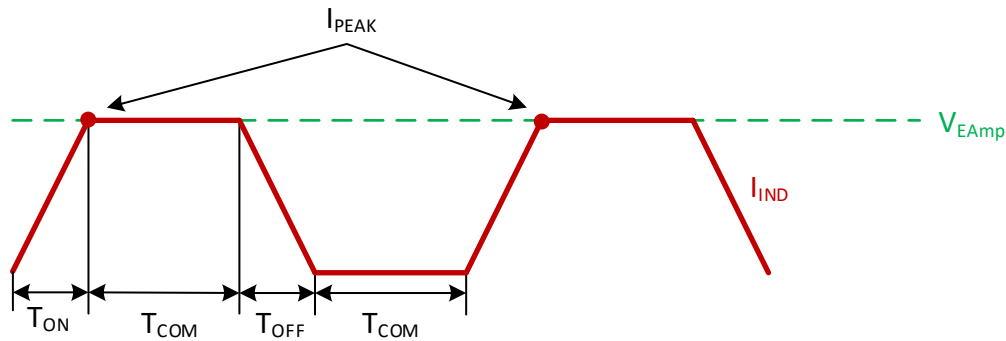


图 9-7. Peak-Current Boost Operation

9.4.1.3 Buck-Boost Operation

When V_I is close to V_O , the TPS63802 operates in buck-boost mode where all switches are active and the device repeats 3-cycles:

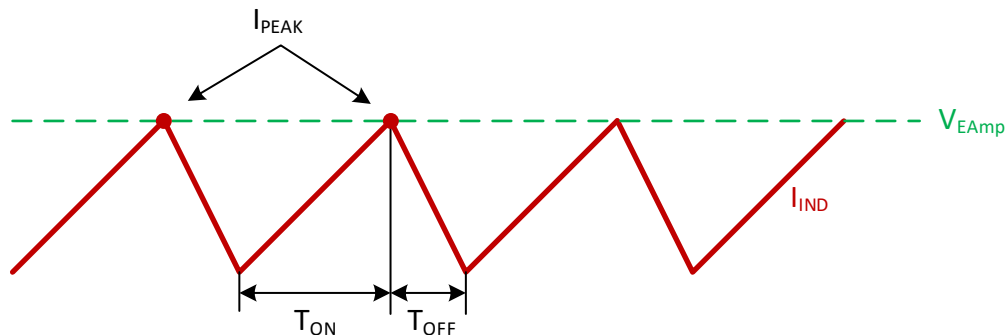
- T_{ON} : Boost-charge phase where boost low-side and buck high-side are closed and the inductor current is built up
- T_{OFF} : Buck discharge phase where boost high-side and buck low-side are closed and the inductor is discharged
- T_{COM} : V_I connected to V_O where all high-side switches are closed and the input is connected to the output



9-8. Peak-Current Buck-Boost Operation

9.4.1.4 Buck Operation

When V_I is greater than V_O (and the voltages are not close enough to trigger buck-boost operation), the TPS63802 operates in buck mode where the buck high-side and low-side switches are active. The boost high-side switch is always turned on and the boost low-side switch is always turned off. This lets the TPS63802 operate as a classical buck converter.



9-9. Peak-Current Buck Operation

9.4.2 Power Save Mode Operation

Besides continuous conduction mode (PWM), the TPS63802 features power save mode (PFM) operation to achieve high efficiency at light load currents. This is implemented by pausing the switching operation, depending on the load current.

The skip comparator manages the switching or pause operation. It compares the current demand signal from the voltage loop, I_{REF} , with the skip threshold, I_{SKIP} , as shown in 9-1. If the current demand is lower than the skip value, the comparator pauses switching operation. If the current demand goes higher (due to falling V_O), the comparator activates the current loop and allows switching according to the loop behavior. Whenever the current loop has risen V_O by bringing charge to the output, the voltage loop output, I_{REF} (respectively V_{EA}), decreases. When I_{REF} falls below I_{SKIP} -hysteresis, it automatically pauses again.

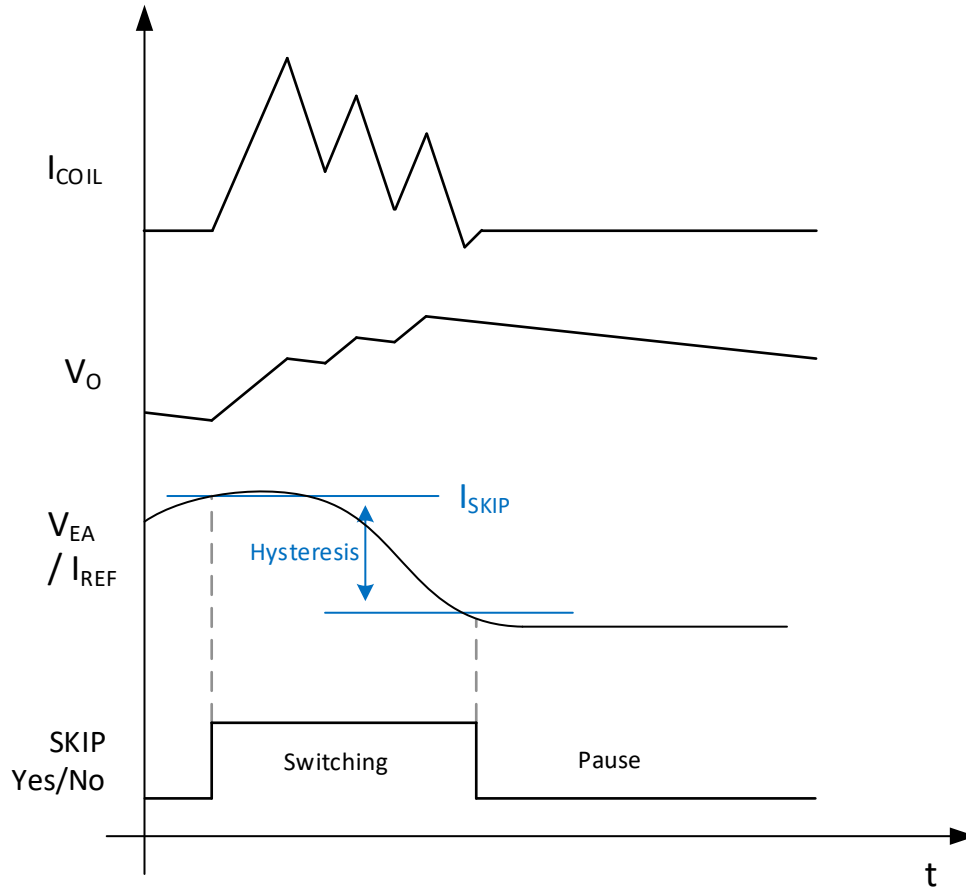


图 9-10. Power Safe Mode Operation Curves

9.4.2.1 Current Limit Operation

To limit current and protect the device and application, the maximum peak inductor current is limited internally on the IC. It is measured at the buck high-side switch which turns into an input current detection. To provide a certain load current across all operation modes, the boost and buck-boost peak current limit is higher than in buck mode. It limits the input current and allows no further increase of the delivered current. When using the device in this mode, it behaves similar to a current source.

The current limit depends on the operation mode (buck, buck-boost, or boost mode).

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The TPS63802 is a high efficiency, low quiescent current, non-inverting buck-boost converter, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage.

10.2 Typical Application

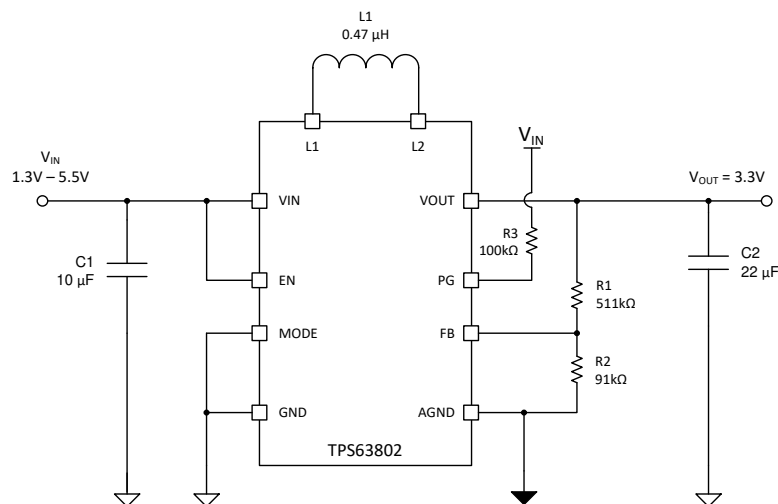


図 10-1. 3.3 V_{OUT} Typical Application

10.2.1 Design Requirements

The design guideline provides a component selection to operate the device within 表 10-1.

表 10-1 shows the list of components for the application characteristic curves.

表 10-1. Matrix of Output Capacitor and Inductor Combinations

NOMINAL INDUCTOR VALUE [µH] ⁽¹⁾	NOMINAL OUTPUT CAPACITOR VALUE [µF] ⁽²⁾				
	10	22	47	66	100
0.47	-	+ ⁽³⁾	+	+	+

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.

(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

(3) TPS63802 typical application. Other check marks indicate possible filter combinations.

10.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, セクション 8.1 outlines minimum and maximum values for inductance and capacitance. Take tolerance and derating into account when selecting nominal inductance and capacitance.

10.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS63802 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Inductor Selection

The inductor selection is affected by several parameters such as the following:

- Inductor ripple current
- Output voltage ripple
- Transition point into power save mode
- Efficiency

See 表 10-2 for typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced, mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady-state operation is calculated using 式 2. Only the equation which defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

$$I_{PEAK} = \frac{I_{OUT}}{\eta \times (1 - D)} + \frac{V_{IN} \times D}{2 \times f \times L} \quad (2)$$

where

- D = Duty Cycle in Boost mode
- f = Converter switching frequency
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

注

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using 式 2. 表 10-2 lists the possible inductors.

表 10-2. List of Recommended Inductors

INDUCTOR VALUE [μH]	SATURATION CURRENT [A]	DCR [mΩ]	PART NUMBER	MANUFACTURER ⁽¹⁾	SIZE (LxWxH mm)
0.47	5.4	7.6	XFL4015-471ME	Coilcraft	4 x 4 x 2
0.47	5.5	26	DFE201612E	Toko	2.0 x 1.6 x 1.2

(1) See [Third-party Products Disclaimer](#).

10.2.2.3 Output Capacitor Selection

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitor value is a single 22 μF for all programmed output voltages ≤ 3.6 V. Above that voltage, 2x 22 μF capacitors are recommended.

It is important that the effective capacitance is given according to the recommended value in [セクション 8.3](#). In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior since higher capacitance reduces transient response overshoot and undershoot and increases transient response time. [表 10-3](#) lists possible output capacitors.

There is no upper limit for the output capacitance value.

表 10-3. List of Recommended Capacitors⁽¹⁾

CAPACITOR [μF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
22	6.3	10	GRM188R60J226MEA0	Murata	0603 (1608)
22	6.3	10	GRM187R61A226ME15	Murata	0603 (1608)
22	10	40	GRM188R61A226ME15	Murata	0603 (1608)
22	10	10	GRM187R60J226ME15	Murata	0603 (1608)
47	6.3	43	GRM188R60J476ME15	Murata	0603 (1608)
47	6.3	43	GRM219R60J476ME44	Murata	0805 (2012)

(1) See [Third-party Products Disclaimer](#).

10.2.2.4 Input Capacitor Selection

A 10 μF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63802 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 μF is a typical choice.

表 10-4. List of Recommended Capacitors⁽¹⁾

CAPACITOR [μF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
10	6.3	10	GRM188R60J106ME84	Murata	0603 (1608)
10	10	40	GRM188R61A106ME69	Murata	0603 (1608)
22	6.3	10	GRM188R60J226MEA0	Murata	0603 (1608)

10.2.2.5 Setting The Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal. The low-side resistor R2 (between FB and GND) must not exceed 100 kΩ. The high-side resistor (between FB and VOUT) R1 is calculated by [式 3](#).

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (3)$$

where

- $V_{FB} = 500 \text{ mV}$

表 10-5. Resistor Selection for Typ. Voltages

V_O [V]	R1 [kΩ]	R2 [kΩ]
2.5	365	91
3.3	511	91
3.6	562	91
5	806	91

10.2.3 Application Curves

表 10-6. Components for Application Characteristic Curves ⁽¹⁾

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER	COMMENT
	TPS63802 2 A Buck-Boost Converter (2 mm x 3 mm QFN)	TPS63802DLA	Texas Instruments	
L1	0.47 μH, 4 mm x 4 mm x 1.5 mm, 5.4 A, 7.6 mΩ	XFL4015-471ME	Coilcraft	
C1	10 μF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J106ME84	Murata	
C2	1x 22 μF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J226MEA0	Murata	$V_O \leq 3.6 \text{ V}$
C2	2x 22 μF, 0603, Ceramic Capacitor, ±20%, 6.3 V	GRM188R60J226MEA0	Murata	$V_O > 3.6 \text{ V}$
R1	511 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	$V_O = 3.3 \text{ V}$
R1	562 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	$V_O = 3.6 \text{ V}$
R1	806 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	$V_O = 5 \text{ V}$
R2	91 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	
R3	100 kΩ, 0603 Resistor, 1%, 100 mW	Standard	Standard	

(1) See [Third-party Products Disclaimer](#).

表 10-7. Typical Characteristics Curves

PARAMETER	CONDITIONS	FIGURE
Output Current Capability		
Typical Output Current Capability versus Input Voltage	$V_O = 3.3\text{ V}$	图 10-2
Switching Frequency		
Typical Inductor Switching Frequency versus Input Voltage	$I_O = 0\text{ A}$, MODE = High	图 10-3
Typical Inductor Burst Frequency versus Output Current	$V_O = 3.3\text{ V}$	图 10-4
Efficiency		
Efficiency versus Output Current (PFM/PWM)	$V_I = 2.5\text{ V}$ to 4.2 V , $V_O = 3.3\text{ V}$, MODE = Low	图 10-5
Efficiency versus Output Current (PWM only)	$V_I = 2.5\text{ V}$ to 4.2 V , $V_O = 3.3\text{ V}$, MODE = High	图 10-6
Efficiency versus Output Current (PFM/PWM)	$V_I = 1.8\text{ V}$ to 5 V , $V_O = 3.3\text{ V}$, MODE = Low	图 10-7
Efficiency versus Output Current (PWM only)	$V_I = 1.8\text{ V}$ to 5 V , $V_O = 3.3\text{ V}$, MODE = High	图 10-8
Efficiency versus. Input Voltage (PFM/PWM)	$V_O = 3.3\text{ V}$, MODE = Low	图 10-9
Efficiency versus Input Voltage (PWM only)	$I_O = 1\text{ A}$, MODE = High	图 10-10
Regulation Accuracy		
Load Regulation, PWM Operation	$V_O = 3.3\text{ V}$, MODE = High	图 10-11
Load Regulation, PFM/PWM Operation	$V_O = 3.3\text{ V}$, MODE = Low	图 10-12
Line Regulation, PWM Operation	$I_O = 1\text{ A}$, MODE = High	图 10-13
Line Regulation, PFM/PWM Operation	$I_O = 1\text{ A}$, MODE = Low	图 10-14
Switching Waveforms		
Switching Waveforms, PFM Boost Operation	$V_I = 2.3\text{ V}$, $V_O = 3.3\text{ V}$, MODE = Low	图 10-15
Switching Waveforms, PFM Buck-Boost Operation	$V_I = 3.3\text{ V}$, $V_O = 3.3\text{ V}$, MODE = Low	图 10-16
Switching Waveforms, PFM Buck Operation	$V_I = 4.3\text{ V}$, $V_O = 3.3\text{ V}$, MODE = Low	图 10-17
Switching Waveforms, PWM Boost Operation	$V_I = 2.3\text{ V}$, $V_O = 3.3\text{ V}$, MODE = High	图 10-18
Switching Waveforms, PWM Buck-Boost Operation	$V_I = 3.3\text{ V}$, $V_O = 3.3\text{ V}$, MODE = High	图 10-19
Switching Waveforms, PWM Buck Operation	$V_I = 4.3\text{ V}$, $V_O = 3.3\text{ V}$, MODE = High	图 10-20
Transient Performance		
Load Transient, PFM/PWM Boost Operation	$V_I = 2.5\text{ V}$, $V_O = 3.3\text{ V}$, Load = 100 mA to 1 A , MODE = Low	图 10-21
Load Transient, PFM/PWM Buck-Boost Operation	$V_I = 3.3\text{ V}$, $V_O = 3.3\text{ V}$, Load = 100 mA to 1 A , MODE = Low	图 10-22
Load Transient, PFM/PWM Buck Operation	$V_I = 4.2\text{ V}$, $V_O = 3.3\text{ V}$, Load = 100 mA to 1 A , MODE = Low	图 10-23
Load Transient, PWM Boost Operation	$V_I = 2.5\text{ V}$, $V_O = 3.3\text{ V}$, Load = 100 mA to 1 A , MODE = High	图 10-24
Load Transient, PWM Buck-Boost Operation	$V_I = 3.3\text{ V}$, $V_O = 3.3\text{ V}$, Load = 100 mA to 1 A , MODE = High	图 10-25
Load Transient, PWM Buck Operation	$V_I = 4.2\text{ V}$, $V_O = 3.3\text{ V}$, Load = 100 mA to 1 A , MODE = High	图 10-26
Line Transient, PWM Operation	$V_I = 2.3\text{ V}$ to 4.3 V , $V_O = 3.3\text{ V}$, Load = 0.5 A , MODE = Low	图 10-27
Line Transient, PWM Operation	$V_I = 2.3\text{ V}$ to 4.3 V , $V_O = 3.3\text{ V}$, Load = 1 A , MODE = Low	图 10-28
Line Transient, PWM Operation	$V_I = 3\text{ V}$ to 3.6 V , $V_O = 3.3\text{ V}$, Load = 0.5 A , MODE = Low	图 10-29
Start-up		
Start-up Behavior from Rising Enable, PFM Operation	$V_I = 2.2\text{ V}$, $V_O = 3.3\text{ V}$, Load = 10 mA , MODE = Low	图 10-30
Start-up Behavior from Rising Enable, PWM Operation	$V_I = 2.2\text{ V}$, $V_O = 3.3\text{ V}$, Load = 10 mA , MODE = High	图 10-31

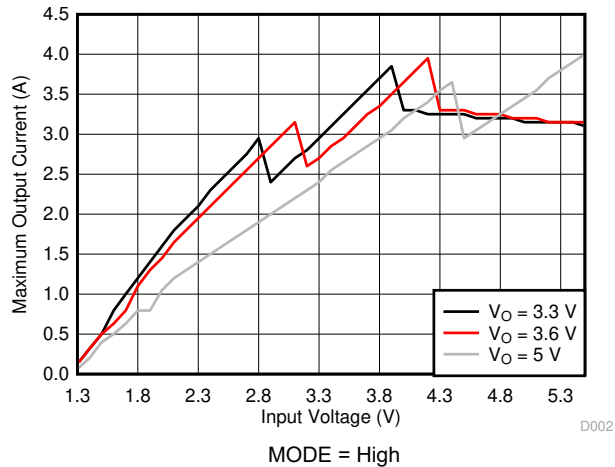


FIG 10-2. Typical Output Current Capability versus Input Voltage

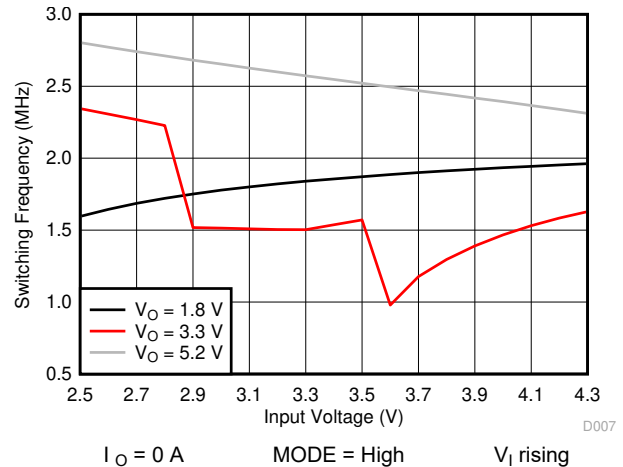


FIG 10-3. Typical Inductor Switching Frequency versus Input Voltage

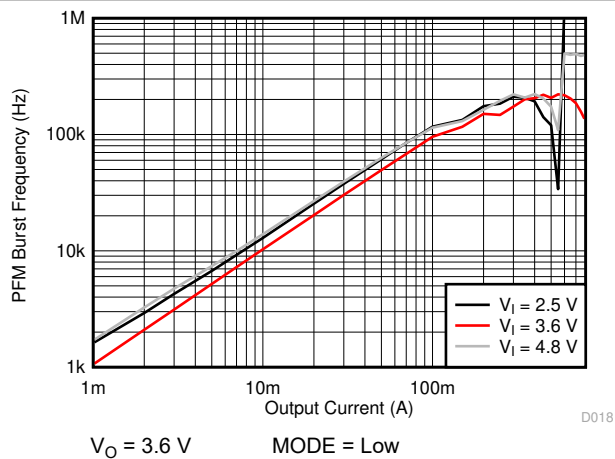


FIG 10-4. Typical Inductor Burst Frequency versus Output Current

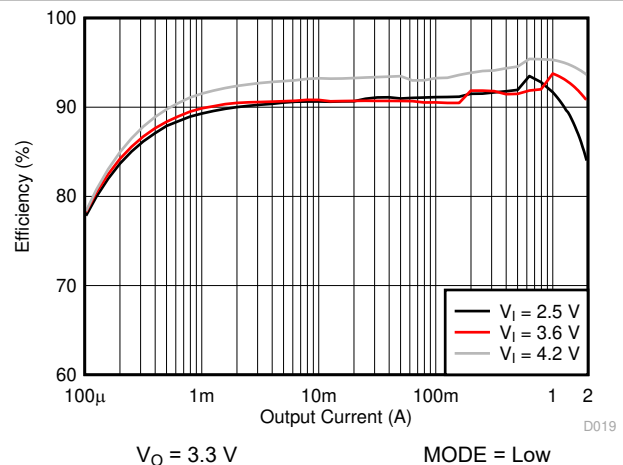


FIG 10-5. Efficiency versus Output Current (PFM/PWM)

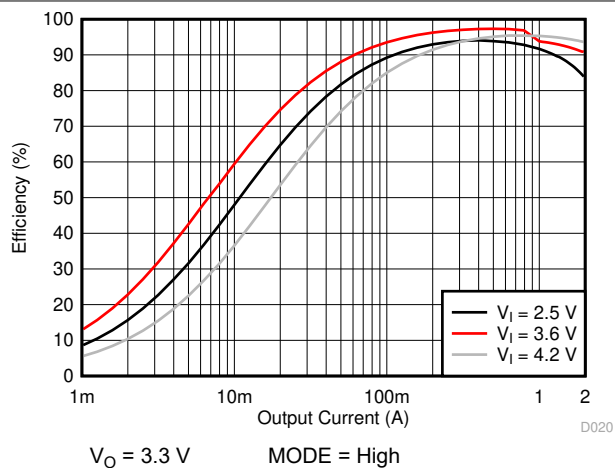


FIG 10-6. Efficiency versus Output Current (PWM Only)

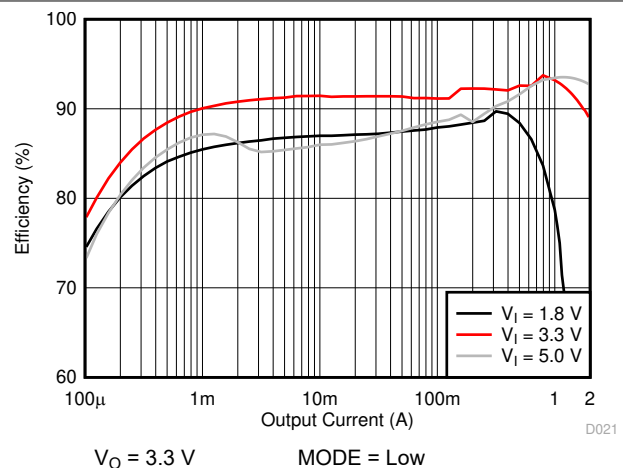
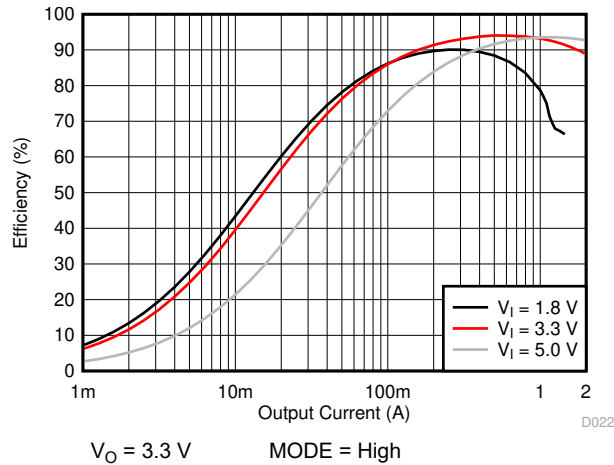
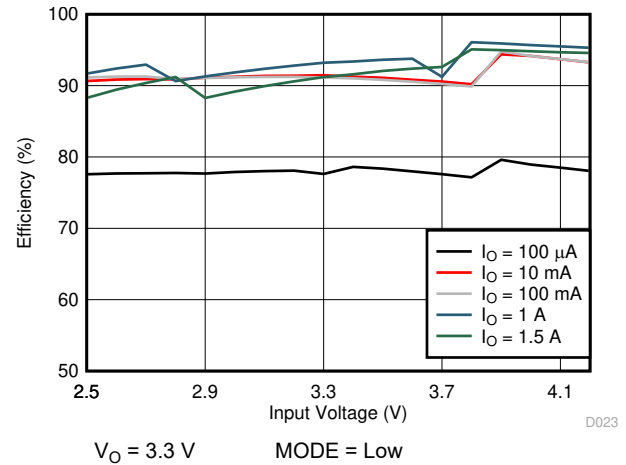


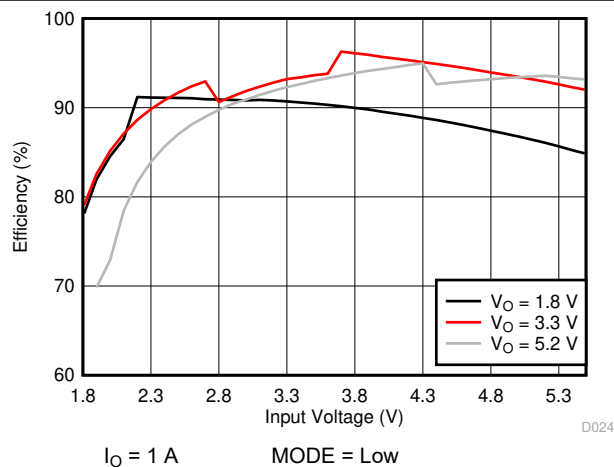
FIG 10-7. Efficiency versus Output Current (PFM/PWM)



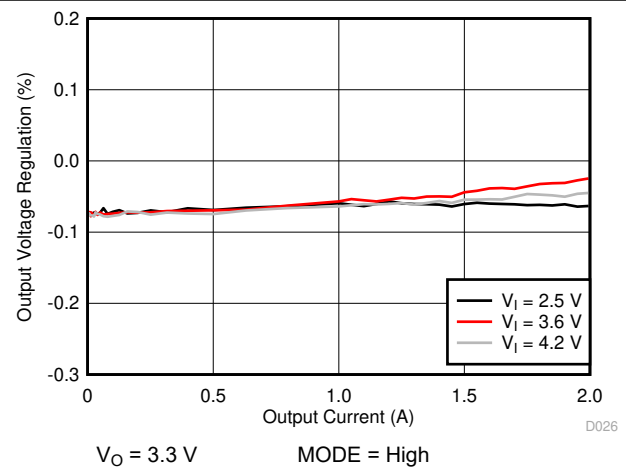
10-8. Efficiency versus Input Voltage (PWM Only)



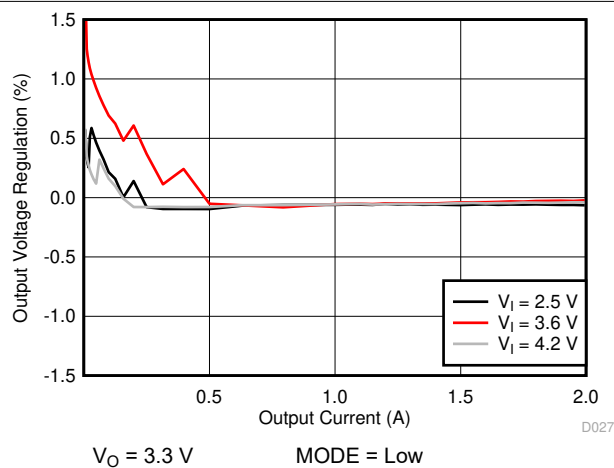
10-9. Efficiency versus Input Voltage (PFM/PWM)



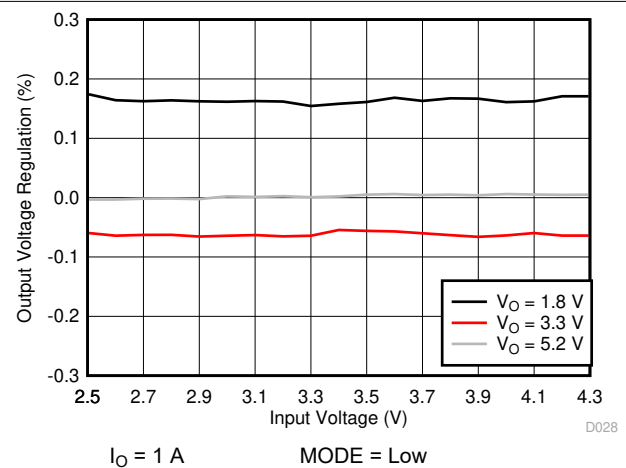
10-10. Efficiency versus Input Voltage (PWM Only)



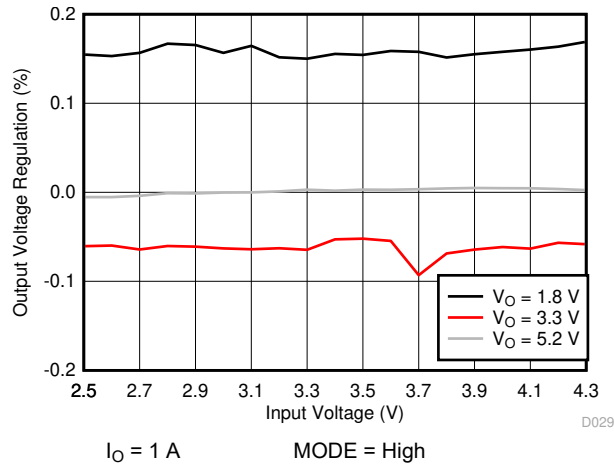
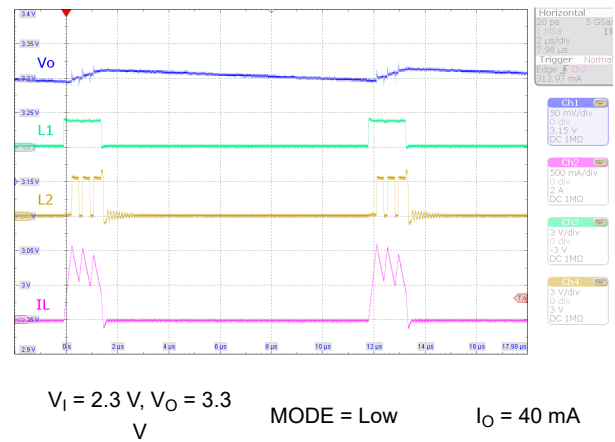
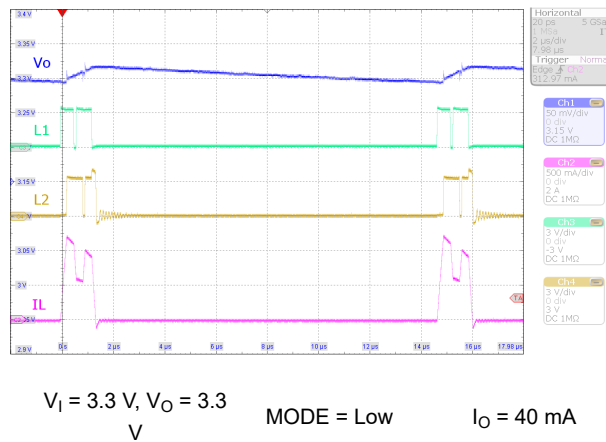
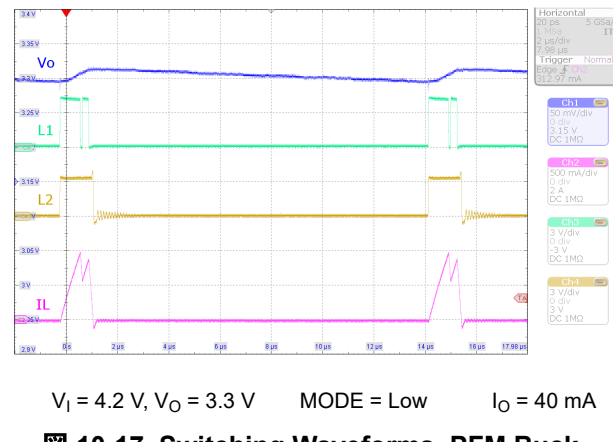
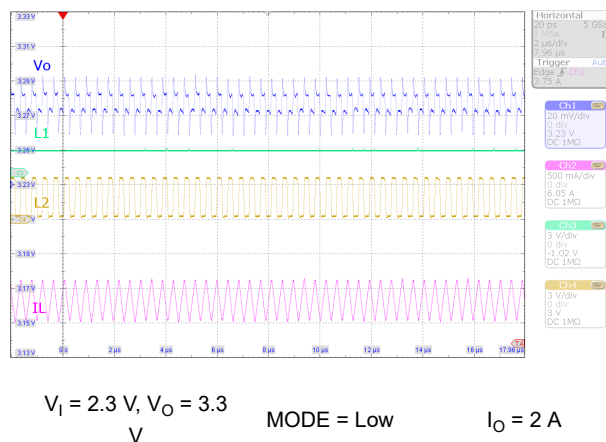
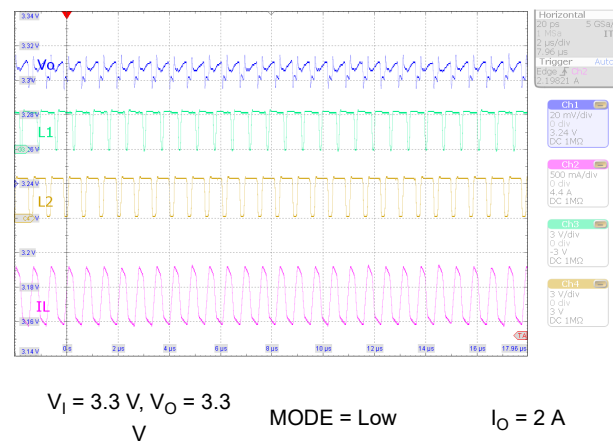
10-11. Load Regulation (PWM Only)

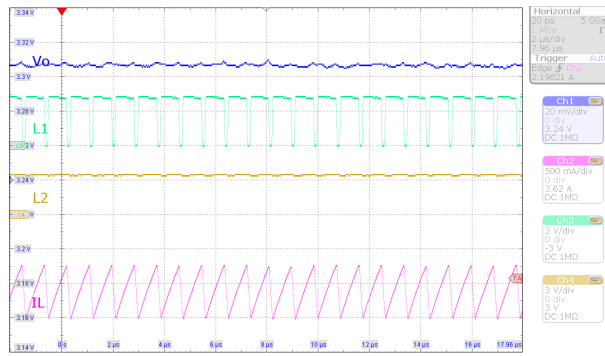


10-12. Load Regulation (PFM/PWM)



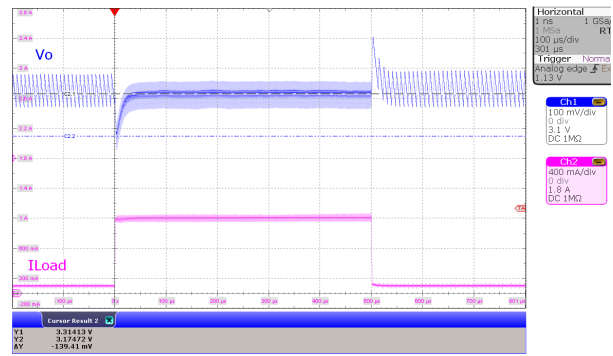
10-13. Line Regulation (PWM Only)


 **10-14. Line Regulation (PFM/PWM)**

 **10-15. Switching Waveforms, PFM Boost Operation**

 **10-16. Switching Waveforms, PFM Buck-Boost Operation**

 **10-17. Switching Waveforms, PFM Buck Operation**

 **10-18. Switching Waveforms, PWM Boost Operation**

 **10-19. Switching Waveforms, PWM Buck-Boost Operation**



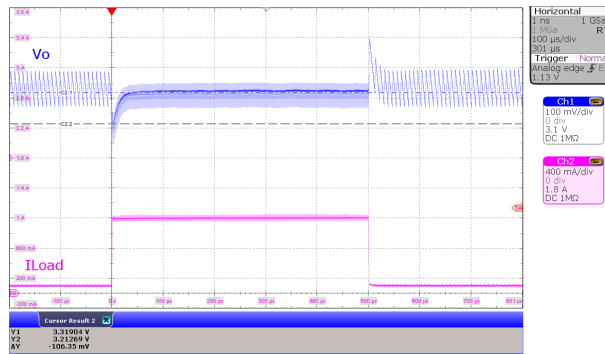
$V_1 = 4.2\text{ V}$, $V_O = 3.3\text{ V}$ MODE = Low $I_O = 2\text{ A}$

10-20. Switching Waveforms, PWM Buck Operation



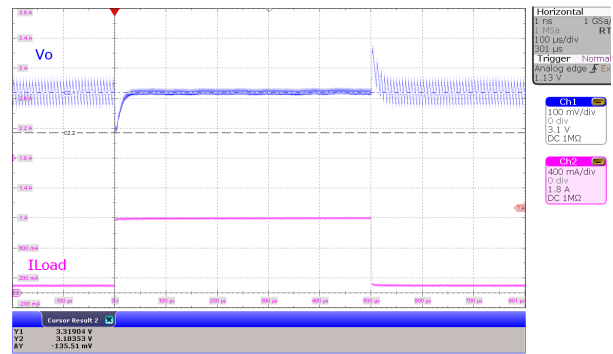
$V_1 = 2.5\text{ V}$, $V_O = 3.3\text{ V}$ I_O from 100 mA to 1 A $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ MODE = Low

10-21. Load Transient, PFM/PWM Boost Operation



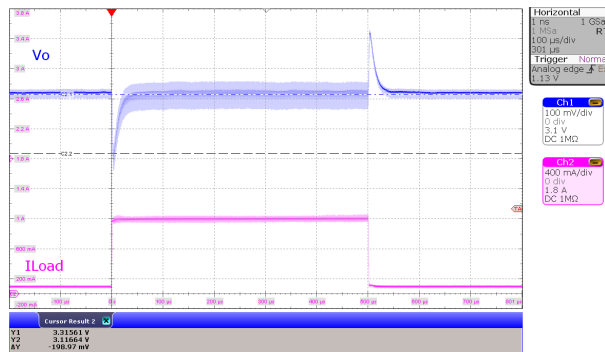
I_O from 100 mA to 1 A $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ $V_1 = 3.3\text{ V}$, $V_O = 3.3\text{ V}$ MODE = Low

10-22. Load Transient, PFM/PWM Buck-Boost Operation



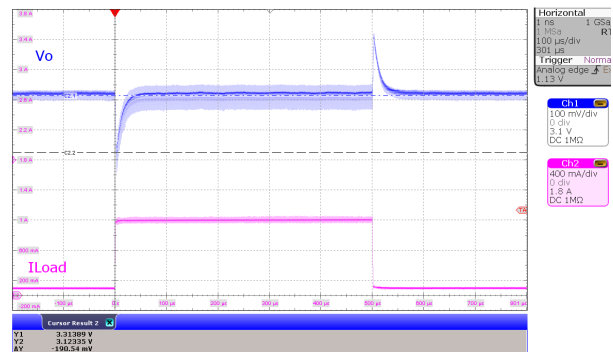
I_O from 100 mA to 1 A $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ $V_1 = 5\text{ V}$, $V_O = 3.3\text{ V}$ MODE = Low

10-23. Load Transient, PFM/PWM Buck Operation



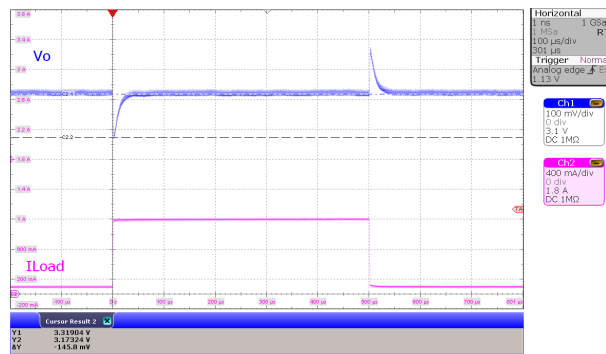
I_O from 100 mA to 1 A $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ $V_1 = 2.5\text{ V}$, $V_O = 3.3\text{ V}$ MODE = High

10-24. Load Transient, PWM Boost Operation



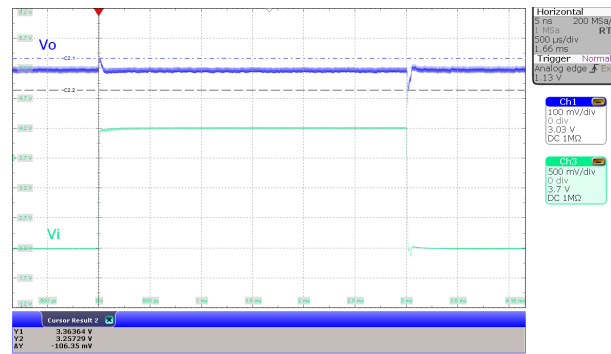
I_O from 100 mA to 1 A $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ $V_1 = 3.3\text{ V}$, $V_O = 3.3\text{ V}$ MODE = High

10-25. Load Transient, PWM Buck-Boost Operation



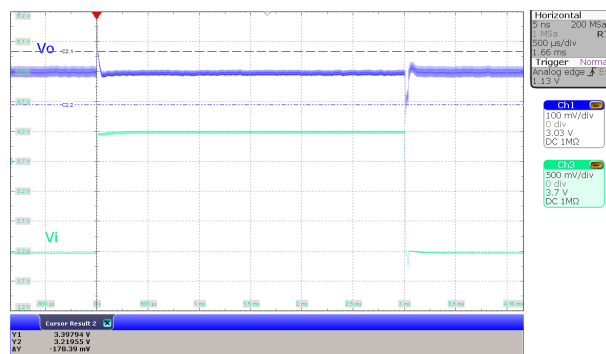
I_O from 100 mA
 $V_I = 5\text{ V}$, $V_O = 3.3\text{ V}$ to 1 A $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ MODE = High

10-26. Load Transient, PWM Buck Operation



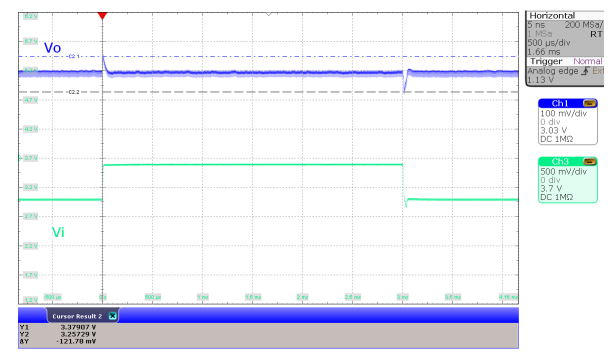
$I_O = 0.5\text{ A}$ V_I from 2.2 V to 4.2 V $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ MODE = High

10-27. Line Transient, PWM Operation



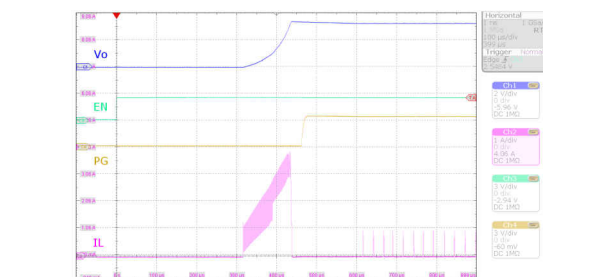
$I_O = 1\text{ A}$ V_I from 2.2 V to 4.2 V $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ MODE = High

10-28. Line Transient, PWM Operation



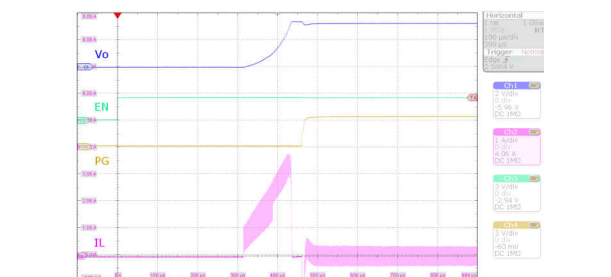
$I_O = 0.5\text{ A}$ V_I from 3 V to 3.6 V $t_r = 1\text{ }\mu\text{s}$, $t_f = 1\text{ }\mu\text{s}$ MODE = High

10-29. Line Transient, PWM Operation



$V_I = 4.2\text{ V}$, $V_O = 3.3\text{ V}$ MODE = Low 100 mΩ resistive load

10-30. Start-up Behavior from Rising Enable, PFM Operation



$V_I = 4.2\text{ V}$, $V_O = 3.3\text{ V}$ MODE = High 100 mΩ resistive load

10-31. Start-up Behavior from Rising Enable, PWM Operation

11 Power Supply Recommendations

The TPS63802 device family has no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS63802.

12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS63802 device.

1. Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Route wide and direct traces to the input and output capacitor results in low trace resistance and low parasitic inductance.
2. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
3. Use separate traces for the supply voltage of the power stage and the supply voltage of the analog stage.
4. The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.

12.2 Layout Example

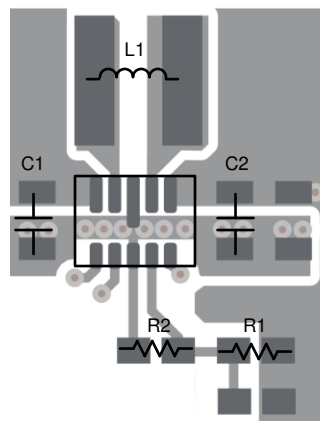


图 12-1. TPS63802 Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.1.2 Development Support

[QFN/SON Package FAQs](#)

13.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS63802 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Selecting a DC/DC Converter for Maximum Battery Life in Pulsed-Load Applications Application Report](#)
- Texas Instruments, [Selecting the Right DC/DC Converter for Maximum Battery Life Application Report](#)
- Texas Instruments, [Supercapacitor Backup Power Supply with TPS63802 Application Report](#)
- Texas Instruments, [Extend Battery Lifetime in Wireless Network Cameras and Video Doorbells Application Note](#)
- Texas Instruments, [Prevent Battery Overdischarge with Precise Threshold Enable Pin Application Note](#)
- Texas Instruments, [Using Non-Inverting Buck-Boost Converter for Voltage Stabilization Application Report](#)
- Texas Instruments, [Precise Delayed Start-up with Precise Threshold Enable-pin Application Note](#)
- Texas Instruments, [Buck-Boost Converters Solving Power Challenges in Optical Modules Application Note](#)
- Texas Instruments, [Improving Load Transient Response for Controlled Loads Application Report](#)
- Texas Instruments, [TPS63802EVM User's Guide](#)
- Texas Instruments, [HotRod QFN Package PCB Attachment Application Report](#)

13.3 ドキュメントの更新通知を受け取る方法

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.7 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63802DLAR	ACTIVE	VSON-HR	DLA	10	3000	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 125	63802	Samples
TPS63802DLAT	ACTIVE	VSON-HR	DLA	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	63802	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

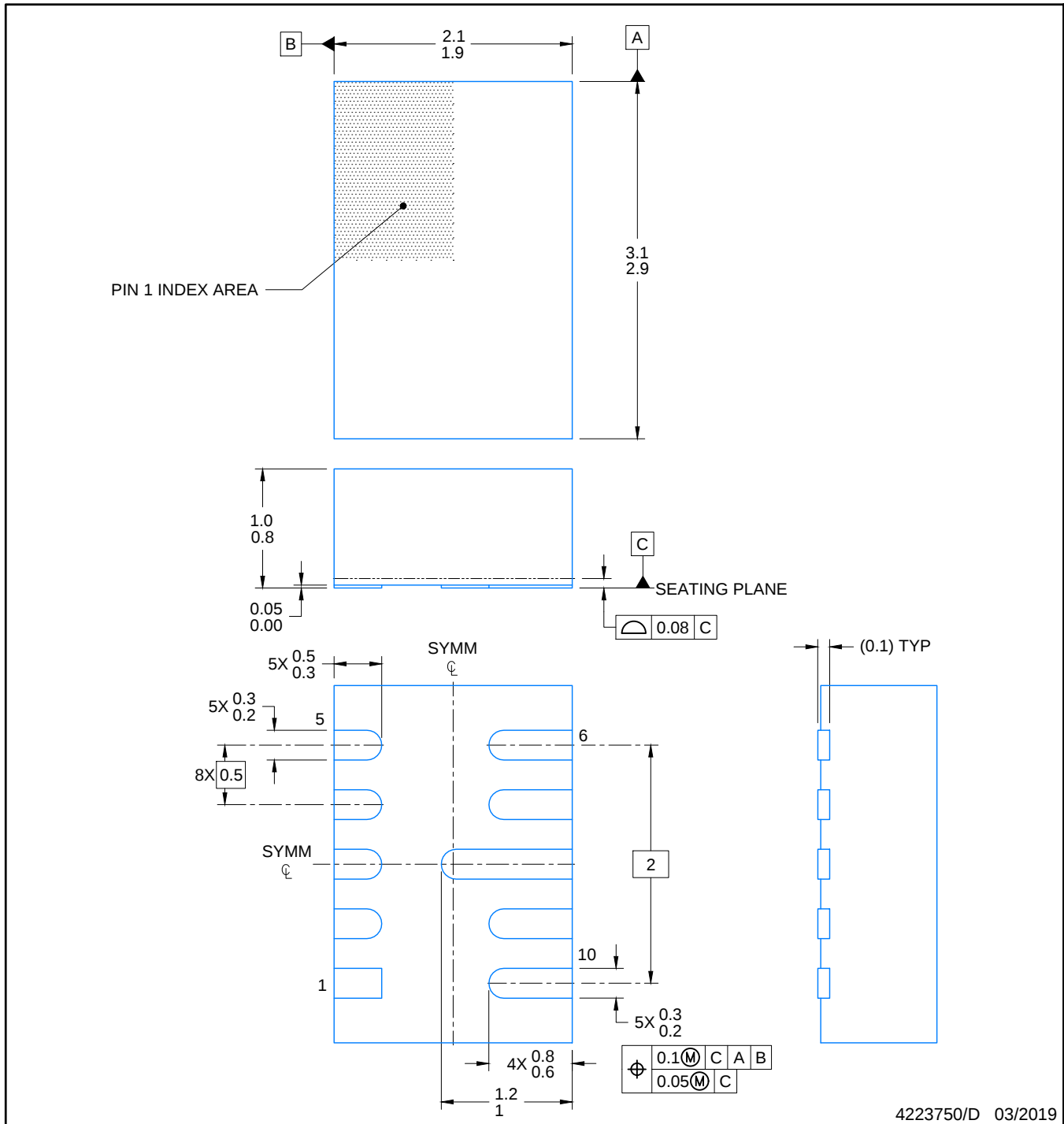
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63802DLAR	VSON-HR	DLA	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS63802DLAT	VSON-HR	DLA	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

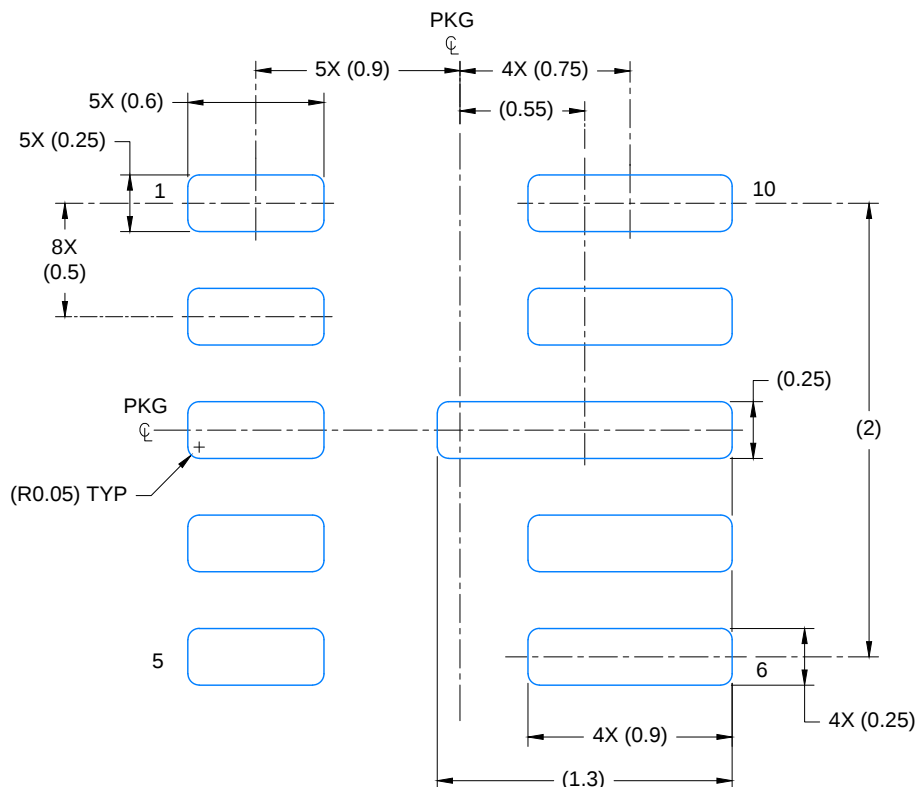


*All dimensions are nominal

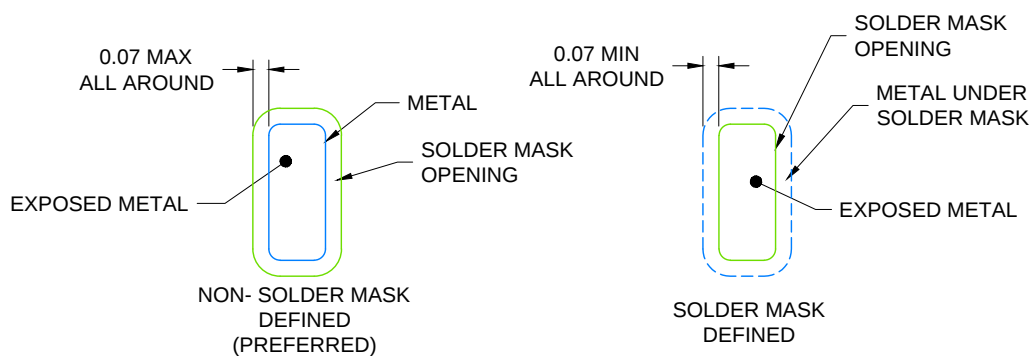
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63802DLAR	VSON-HR	DLA	10	3000	182.0	182.0	20.0
TPS63802DLAT	VSON-HR	DLA	10	250	182.0	182.0	20.0



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LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

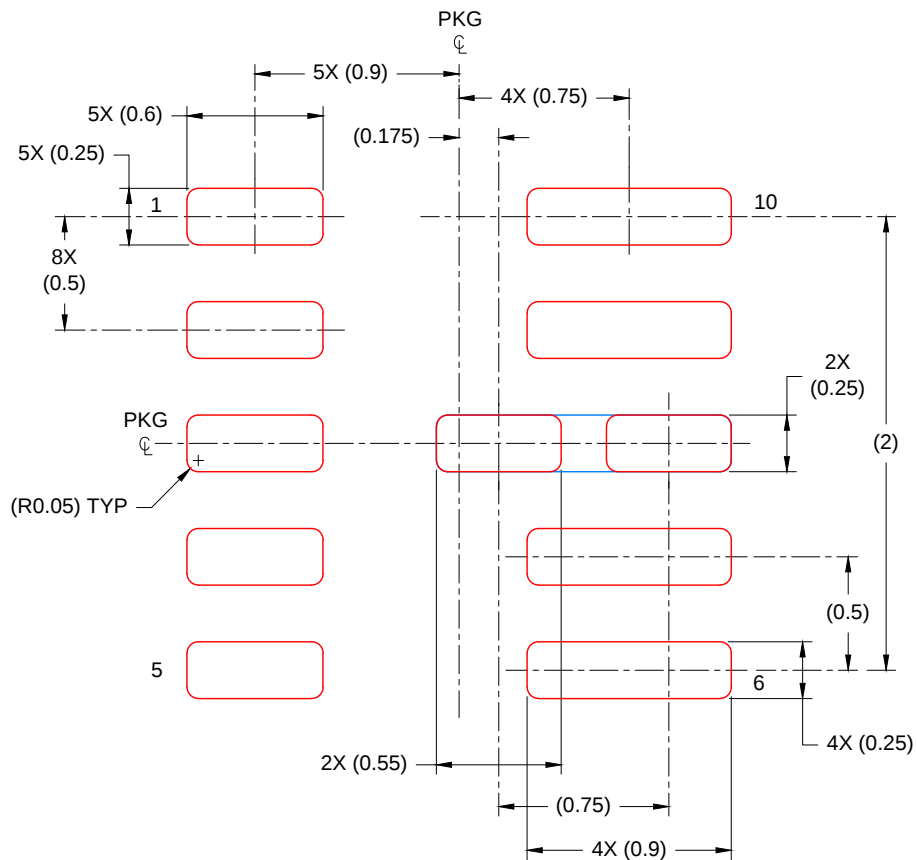


SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

PAD 8: 83%

SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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