参考資料

Texas Instruments

TPS650250 SoCおよびマルチレール・サブシステム用の電力管理IC (PMIC)

1 特長

- システム電圧(VDCDC1)用の1.6A、97%効率の降圧コンバータ
  - 3.3V、2.8V、または可変
- メモリ電圧用の0.8A、最高95%効率の降圧コンバータ(VDCDC2)
  - 1.8V、2.5V、または可変
- プロセッサ・コア用の0.8A、90%効率の降圧コンバータ(VDCDC3)
- VDCDC3の出力電圧は可変
- Vdd_alive用の30mA LDO
- 2×200mAの汎用LDO (LDO1およびLDO2)
- プロセッサ・コア用の動的電圧管理
- LDO1とLDO2の電圧は外部から変更可能
- 誘導性コンバータ用の独立したイネーブル・ピン
- スイッチング周波数: 2.25MHz
- 85µAの静止電流
- サーマル・シャットダウン保護機能

2 アプリケーション

- 携帯電話、スマートフォン
- GPS
- デジタル・スチル・カメラ
- 分離電源のDSPおよびµPソリューション
- Samsung製ARMベース・プロセッサ

3 概要

TPS650250デバイスは、複数の電源レールを必要とするアプリケーション向けの統合型電源管理ICです。TPS650250には、プロセッサ・ベースのシステムにおいてコア電圧、ペリフェラル、I/O、およびメモリ・レールを提供するため、3つの高効率な降圧コンバータが搭載されています。3つの降圧コンバータはすべてMODEピンにより制御され、軽負荷時には低消費電力モードに移行して最大の効率を維持するか、または強制的に固定周波数のPWMモードで動作します。

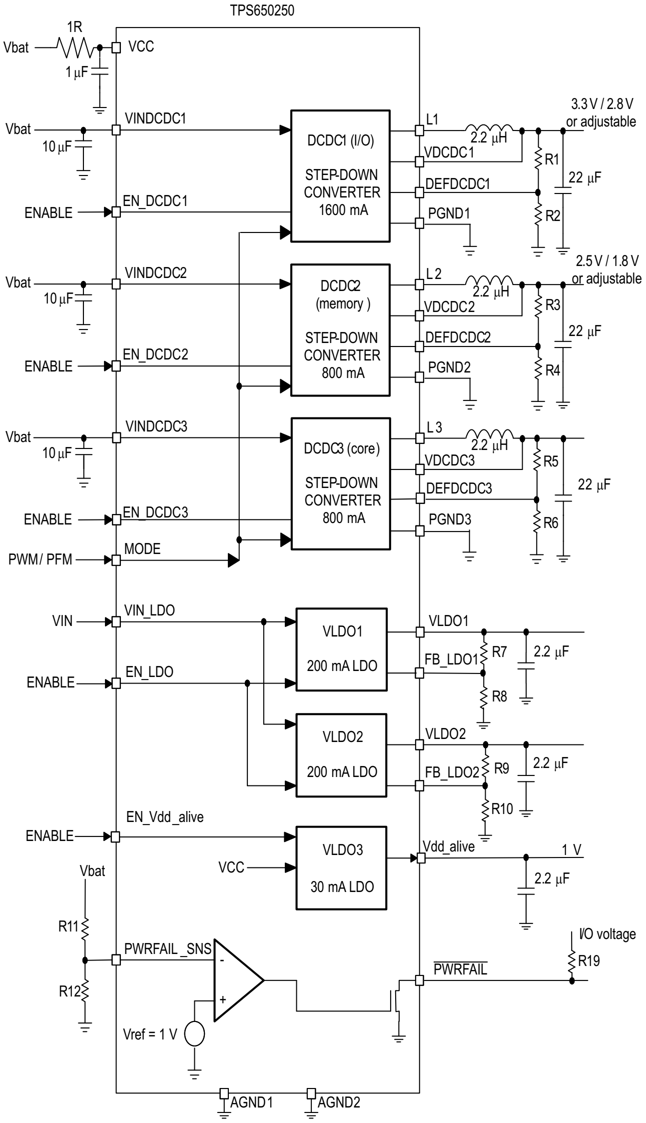
TPS650250デバイスには、2つの汎用200mA LDO電圧レギュレータが内蔵されています。どちらのLDOも1.5V～6.5Vの入力電圧範囲で動作し、降圧コンバータの1つから給電できます。すべてのレールの出力電圧は、外付けの分圧抵抗により設定でき、入力ピンによりイネーブルされます。さらに、常時オンのレールに電力を供給するため、一般に30mAのLDOが使用されます。

製品情報[(1)]

型番	パッケージ	本体サイズ(公称)
TPS650250	VQFN (32)	5.00mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

詳細ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2014) から Revision B に変更 **Page**

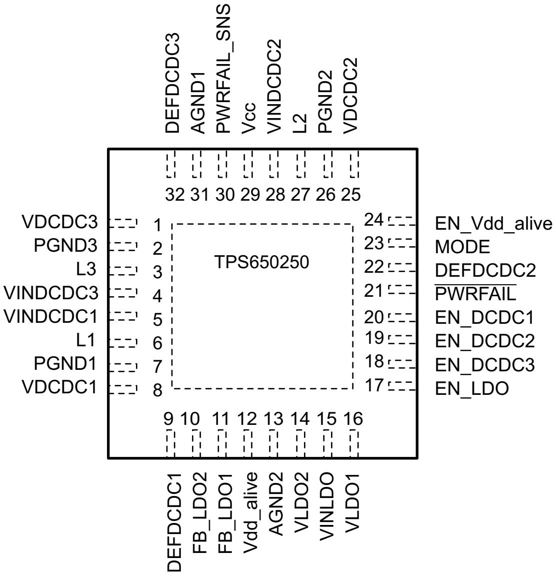
- データシートのタイトル 変更 1
- Changed the *Handling Ratings* table to *ESD Ratings* and moved the storage temperature to the *Absolute Maximum Ratings* table 4
- 追加「*開発サポート*」、「*ドキュメントのサポート*」、「*ドキュメントの更新通知を受け取る方法*」、「*コミュニティ・リソース*」セクション 26
- 変更「*静電気放電についての注意事項*」の記述 26

2008年12月発行のものから更新 **Page**

- 「*取り扱い定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 1

5 Pin Configuration and Functions

RHB Package
32-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCHING REGULATOR SECTION			
AGND1	31	—	Analog ground connection. All analog ground pins are connected internally on the chip.
AGND2	13	—	Analog ground connection. All analog ground pins are connected internally on the chip.
Thermal pad	—	—	Connect the power pad to analog ground.
VINDCDC1	5	I	Input voltage for VDCDC1 step-down converter. This must be connected to the same voltage supply as VINDCDC2, VINDCDC3 and VCC.
L1	6	—	Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
VDCDC1	8	I	VDCDC1 feedback voltage sense input, connect directly to VDCDC1.
PGND1	7	—	Power ground for VDCDC1 converter.
VINDCDC2	28	I	Input voltage for VDCDC2 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC3 and VCC.
L2	27	—	Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.
VDCDC2	25	I	VDCDC2 feedback voltage sense input, connect directly to VDCDC2.
PGND2	26	—	Power ground for VDCDC2 converter.
VINDCDC3	4	I	Input voltage for VDCDC3 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC2 and VCC.
L3	3	—	Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.
VDCDC3	1	I	VDCDC3 feedback voltage sense input, connect directly to VDCDC3.
PGND3	2	—	Power ground for VDCDC3 converter.
Vcc	29	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and DCDC3 DC-DC converters. This must be connected to the same voltage supply as VINDCDC3, VINDCDC1 and VINDCDC2.
DEFDCDC1	9	I	Input signal indicating default VDCDC1 voltage, 0 = 2.8V, 1 = 3.3V . This pin can also be connected to a resistor divider between VDCDC1 and GND. In this case the output voltage of the DCDC1 converter can be set in a range from 0.6V to VINDCDC1.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DEFDCDC2	22	I	Input signal indicating default VDCDC2 voltage, 0 = 1.8V, 1 = 2.5V . This pin can also be connected to a resistor divider between VDCDC2 and GND. In this case the output voltage of the DCDC2 converter can be set in a range from 0.6V to VINDCDC2.
DEFDCDC3	32	I	This pin must be connected to a resistor divider between VDCDC3 and GND. The output voltage of the DCDC3 converter can be set in a range from 0.6V to VINDCDC3.
EN_DCDC1	20	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.
EN_DCDC2	19	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.
EN_DCDC3	18	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.
LDO REGULATOR SECTION			
VINLDO	15	I	Input voltage for LDO1 and LDO2.
VLDO1	16	O	Output voltage of LDO1.
VLDO2	14	O	Output voltage of LDO2.
EN_LDO	17	I	Enable input for LDO1 and LDO2. Logic high enables the LDOs, logic low disables the LDOs.
EN_Vdd_alive	24	I	Enable input for Vdd_alive LDO. Logic high enables the LDO, logic low disables the LDO.
Vdd_alive	12	O	Output voltage for Vdd_alive.
FB_LDO1	11	I	Feedback pin for LDO1.
FB_LDO2	10	I	Feedback pin for LDO2.
CONTROL AND I2C SECTION			
MODE	23	I	Select between Power Safe Mode and forced PWM Mode for DCDC1, DCDC2 and DCDC3. In Power Safe Mode PFM is used at light loads, PWM for higher loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then Device operates in Power Safe Mode.
$\overline{\text{PWRFAIL}}$	21	O	Open drain output. Active low when PWRFAIL comparator indicates low VBAT condition.
PWRFAIL_SNS	30	I	Input for the comparator driving the /PWRFAIL output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Input voltage range on all pins except A/PGND pins with respect to AGND	–0.3	7	V
	Voltage range on pins VLDO1, VLDO2, FB_LDO1, FB_LDO2	–0.3	3.6	V
	Current at VINDCDC1, L1, PGND1, VINDCDC2, L2, PGND2, VINDCDC3, L3, PGND3	2000	2000	mA
	Peak current at all other pins	500	500	mA
	Continuous total power dissipation	See *Dissipation Ratings*		
T_A	Operating free-air temperature	–40	85	°C
T_J	Maximum junction temperature	125	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Input voltage range step-down converters, VINDCDC1, VINDCDC2, VINDCDC3	2.5		6.0	V
V_O	Output voltage range for step-down converter, VDCDC1 (1)	0.6		VINDCDC1	V
	Output voltage range for mem step-down converter, VDCDC2 (1)	0.6		VINDCDC2	V
	Output voltage range for core step-down converter, VDCDC3	0.6		VINDCDC3	V
V_I	Input voltage range for LDOs, VINLDO1, VINLDO2	1.5		6.5	V
V_O	Output voltage range for LDOs	1		3.3	V
I_O	Output current at L, V1DCDC1			1600	mA
L1	Inductor at L1 (2)	1.5	2.2		µH
C_I	Input capacitor at VINDCDC1 (2)	10			µF
C_O	Output capacitor at VDCDC1 (2)	10	22		µF
I_O	Output current at L2, VDCDC2			800	mA
L2	Inductor at L2 (2)	1.5	2.2		µH
C_I	Input capacitor at VINDCDC2 (2)	10			µF
C_O	Output capacitor at VDCDC2 (2)	10	22		µF
I_O	Output current at L3, VDCDC3			800	mA
L3	Inductor at L3 (2)	1.5	2.2		µH
C_I	Input capacitor at VINDCDC3 (2)	10			µF
C_O	Output capacitor at VDCDC3 (2)	10	22		µF
C_I	Input capacitor at VCC (2)	1			µF
C_I	Input capacitor at VINLDO (2)	1			µF
C_O	Output capacitor at VLDO1, VLDO2 (2)	2.2			µF
I_O	Output current at VLDO1, VLDO2			200	mA
C_O	Output capacitor at Vdd_alive (2)	2.2			µF
I_O	Output current at Vdd_alive			30	mA
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
R_{CC}	Resistor from VINDCDC3,VINDCDC2, VINDCDC1 to V_{CC} used for filtering (3)		1	10	Ω

(1) When using an external resistor divider at DEFDCDC2, DEFDCDC1.
(2) See applications section for more information, for V_O > 2.85V choose 3.3µH inductor.
(3) Up to 2.5mA can flow into V_{CC} when all 3 converters are running in PWM, this resistor will cause the UVLO threshold to be shifted accordingly.

6.4 Thermal Information

THERMAL METRIC (1)		TPS650250	UNIT
		RHB (VQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Dissipation Ratings

PACKAGE[1]	$R_{\theta JA}$	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RHB	35 K/W	2.85 W	28m W/K	1.57 W	1.14 W

(1) The thermal resistance junction to ambient of the RHB package is measured on a high K board. The thermal resistance junction to power pad is 1.5k/W.

6.6 Electrical Characteristics

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CONTROL SIGNALS: EN_DCDC1, EN_DCDC2, EN_DCDC3, EN_LDO, MODE, EN_VDD_ALIVE							
V_{IH}	High level input voltage			1.45		VCC	V
V_{IL}	Low level input voltage			0		0.4	V
I_H	Input bias current				0.01	0.1	μA
SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3							
$I_{(qPFM)}$	Operating quiescent current	PFM All 3 DCDC converters enabled, zero load and no switching, LDOs enabled	V_{CC} = 3.6V		135	170	μA
		PFM All 3 DCDC converters enabled, zero load and no switching, LDO1, LDO2 = OFF, Vdd_alive = ON			75	100	
		PFM DCDC1 and DCDC2 converters enabled, zero load and no switching, LDO1, LDO2 = OFF, Vdd_alive = ON			55	80	
		PFM DCDC1 converter enabled, zero load and no switching, LDO1, LDO2 = OFF, Vdd_alive = ON			40	60	
$I_{VCC(PWM)}$	Current into V_{CC}; PWM	All 3 DCDC converters enabled & running in PWM, LDOs off	V_{CC} = 3.6V		2		mA
		PWM DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off			1.5	2.5	
		PWM DCDC1 converter enabled and running in PWM, LDOs off			0.85	2	
I_q	Quiescent current	All converters disabled, LDO1, LDO2 = OFF, Vdd_alive = OFF	V_{CC} = 3.6V		16		μA
		All converters disabled, LDO1, LDO2 = OFF, Vdd_alive = ON			26		
VLDO1 AND VLDO2 LOW DROPOUT REGULATORS							
$I_{(q)}$	Operating quiescent current	Current per LDO into VINLDO			16	30	μA
$I_{(SD)}$	Shutdown current	Total current into VINLDO, VLDO = 0V			0.6	2	μA
V_I	Input voltage range for LDO1, LDO2			1.5		6.5	V
V_O	LDO1 output voltage range			1		3.3	V
	LDO2 output voltage range			1		3.3	V
VFB	LDO1 and LDO2 feedback voltage				1.0		V
I_O	Maximum output current for LDO1, LDO2	V_I = 1.8V, V_O = 1.3V		200			mA
I_O	Maximum output current for LDO1, LDO2	V_I = 1.5V; V_O = 1.3V			120		mA

Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC}	LDO1 and LDO2 short circuit current limit	V_{LDO1} = GND, V_{LDO2} = GND			400	mA
	Minimum voltage drop at LDO1, LDO2	I_O = 50mA, VINLDO = 1.8V			120	mV
	Minimum voltage drop at LDO1, LDO2	I_O = 50mA, VINLDO = 1.5V		65	150	mV
	Minimum voltage drop at LDO1, LDO2	I_O = 200mA, VINLDO = 1.8V			300	mV
	Output voltage accuracy for LDO1, LDO2	I_O = 10mA	–2%		1%	
	Line regulation for LDO1, LDO2	$V_{INLDO1,2}$ = $V_{LDO1,2}$ + 0.5V (min. 2.5V) to 6.5V, I_O = 10mA	–1%		1%	
	Load regulation for LDO1, LDO2	I_O = 0mA to 200mA	–1%		1%	
	Regulation time for LDO1, LDO2	Load change from 10% to 90%		10		μs
VDD_ALIVE LOW DROPOUT REGULATOR						
Vdd_alive	Vdd_alive LDO output voltage, TPS6502500 to TPS6502504	I_O = 0mA		1.0		V
I_O	Output current for Vdd_alive				30	mA
$I_{(SC)}$	Vdd_alive short circuit current limit	Vdd_alive = GND			100	mA
	Output voltage accuracy for Vdd_alive	I_O = 0mA	–1%		1 %	
	Line regulation for Vdd_alive	V_{CC} = Vdd_alive + 0.5 V to 6.5 V, I_O = 0mA	–1%		1 %	
	Regulation time for Vdd_alive	Load change from 10% to 90%		10		μs
ANALOGIC SIGNALS DEFDCDC1, DEFDCDC2, DEFDCDC3						
V_{IH}	High level input voltage		1.3		VCC	V
V_{IL}	Low level input voltage		0		0.1	V
I_H	Input bias current			0.001	0.05	μA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Increasing junction temperature		160		°C
	Thermal shudown hysteresis	Decreasing junction temperature		20		°C
INTERNAL UNDER VOLTAGE LOCK OUT						
UVLO	Internal UVLO	VCC falling	–3%	2.35	3%	V
V_{UVLO_HYST}	internal UVLO comparator hysteresis			120		mV
VOLTAGE DETECTOR COMPARATOR						
PWRFAIL_SNS	Comparator threshold	Falling threshold	–2%	1.0	2%	V
	Hysteresis		40	50	60	mV

Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Propagation delay	25mV overdrive			10	µs
V_{OL}	Power fail output low voltage	I_{OL} = 5 mA			0.3	V

6.7 Electrical Characteristics VDCDC1

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC1 STEP-DOWN CONVERTER							
V_I	Input voltage range,VINDCDC1			2.5		6	V
I_O	Maximum output current		V_O = 3.3V	1600			mA
I_{SD}	Shutdown supply current in VINDCDC1		EN_DCDC1 = GND		0.1	1	µA
$R_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC1 = VGS = 3.6V		125	261	mΩ
I_{LP}	P-channel leakage current		VINDCDC1 = 6V			2	µA
$R_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC1 = VGS = 3.6V		130	260	mΩ
I_{LN}	N-channel leakage current		V_{DS} = 6V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel)		2.5V < V_{INMAIN} < 6V	1.75	1.97	2.15	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
VDCDC1	Fixed output voltage MODE=0 (PWM/PFM)	2.8V	VINDCDC1 = 3.3V to 6V; 0 mA ≤ I_O ≤ 1.0A	–2%		2%	
		3.3V		–2%		2%	
	Fixed output voltage MODE=1 (PWM)	2.8V	VINDCDC1 = 3.7V to 6V; 0 mA ≤ I_O ≤ 1.0A	–1%		1%	
		3.3V		–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC1 MODE = 0 (PWM/PFM)		VINDCDC1 = VDCDC1 +0.4V (min 2.5V) to 6V; 0mA ≤ I_O ≤ 1.6A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC1; MODE = 1 (PWM)		VINDCDC1 = VDCDC1 +0.4V (min 2.5V) to 6V; 0mA ≤ I_O ≤ 1.6A	–1%		1%	
	Line regulation		VINDCDC1 = VDCDC1 + 0.3V (min. 2.5 V) to 6V; I_O = 10mA		0		%/V
	Load regulation		I_O = 10mA to 1.6A		0.25		%/A
t_{SS}	Soft start ramp time		VDCDC1 ramping from 5% to 95% of target value		750		µs
R(L1)	Internal resistance from L1 to GND				1		MΩ

6.8 Electrical Characteristics VDCDC2

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC2 STEP-DOWN CONVERTER						
V_I	Input voltage range, VINDCDC2		2.5		6	V
I_O	Maximum output current	V_O = 2.5V	800			mA
I_{SD}	Shutdown supply current in VINDCDC2	EN_DCDC2 = GND		0.1	1	µA
$R_{DS(on)}$	P-channel MOSFET on-resistance	VINDCDC2 = V_{GS} = 3.6V		140	300	mΩ
I_{LP}	P-channel leakage current	VINDCDC2 = 6.0V			2	µA
$R_{DS(on)}$	N-channel MOSFET on-resistance	VINDCDC2 = VGS = 3.6V		150	297	mΩ
I_{LN}	N-channel leakage current	V_{DS} = 6V		7	10	µA

Electrical Characteristics VDCDC2 (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMF}	Forward current limit (P- and N-channel)		2.5V < VINDCDC2 < 6V	1.05	1.16	1.29	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
VDCDC2	Fixed output voltage MODE = 0 (PWM/PFM)	1.8V	VINDCDC2 = 2.5V to 6V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
		2.5V	VINDCDC2 = 3V to 6V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
	Fixed output voltage MODE = 1 (PWM)	1.8V	VINDCDC2 = 2.5V to 6V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
		2.5V	VINDCDC2 = 3V to 6V; 0 mA ≤ I_O ≤ 1.6A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC2 MODE = 0 (PWM)		VINDCDC2 = VDCDC2 + 0.5V (min 2.5V) to 6V; 0mA ≤ I_O ≤ 1.6A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC2; MODE = 1 (PWM)		VINDCDC2 = VDCDC2 + 0.5V (min 2.5V) to 6V; 0mA ≤ I_O ≤ 1.6A	–1%		1%	
	Line regulation		VINDCDC2 = VDCDC2 + 0.3 V (min. 2.5 V) to 6V; I_O = 10mA		0.0		%/V
	Load regulation		I_O = 10mA to 1.6A		0.25		%/A
t_{SS}	Soft start ramp time		VDCDC2 ramping from 5% to 95% of target value		750		µs
R(L2)	Internal resistance from L2 to GND				1		MΩ

6.9 Electrical Characteristics VDCDC3

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC3 STEP-DOWN CONVERTER						
V_I	Input voltage range, VINDCDC3		2.5		6.0	V
I_O	Maximum output current	V_O = 1.6V	800			mA
I_{SD}	Shutdown supply current in VINDCDC3	EN_DCDC3 = GND		0.1	1	µA
$R_{DS(on)}$	P-channel MOSFET on-resistance	$V_{INDCDC3}$ = V_{GS} = 3.6V		310	698	mΩ
I_{LP}	P-channel leakage current	VINDCDC3 = 6V		0.1	2	µA
$R_{DS(on)}$	N-channel MOSFET on-resistance	$V_{INDCDC3}$ = V_{GS} = 3.6V		220	503	mΩ
I_{LN}	N-channel leakage current	V_{DS} = 6.0V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel)	2.5V < $V_{INDCDC3}$ < 6V	1.00	1.20	1.40	A
f_S	Oscillator frequency		1.95	2.25	2.55	MHz
VDCDC3	Adjustable output voltage with resistor divider at DEFDCDC2 MODE = 0 (PWM)	VINDCDC3 = VDCDC3 + 0.5V (min 2.5V) to 6V; 0mA ≤ I_O ≤ 0.8A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC2; MODE = 1 (PWM)	VINDCDC3 = VDCDC3 + 0.5V (min 2.5V) to 6V; 0mA ≤ I_O ≤ 0.8A	–1%		1%	
	Line regulation	VINDCDC3 = VDCDC3 + 0.3V (min. 2.5 V) to 6V; I_O = 10mA		0.0		%/V
	Load regulation	I_O = 10mA to 600mA		0.25		%/A
t_{SS}	Soft start ramp time	VDCDC3 ramping from 5% to 95% of target value		750		µs
R(L3)	Internal resistance from L3 to GND			1		MΩ

6.10 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
η	Efficiency VDCDC1	vs Load current PWM/PFM; V_O = 3.3V	Figure 1
η	Efficiency VDCDC1	vs Load current PWM; V_O = 3.3V	Figure 2
η	Efficiency VDCDC2	vs Load current PWM/PFM; V_O = 1.8V	Figure 3
η	Efficiency VDCDC2	vs Load current PWM; V_O = 1.8V	Figure 4
η	Efficiency VDCDC3	vs Load current PWM/PFM; V_O = 1.3V	Figure 5
η	Efficiency VDCDC3	vs Load current PWM; V_O = 1.3V	Figure 6

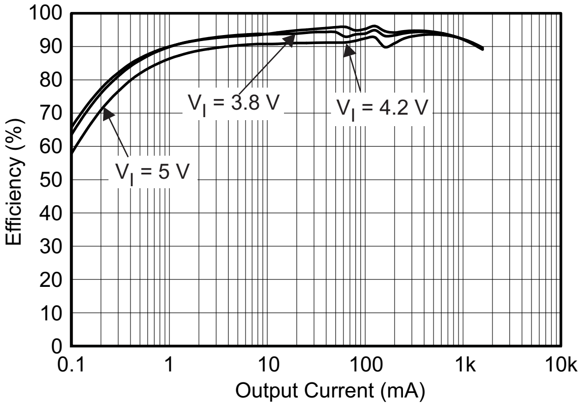


Figure 1. DCDC1: Efficiency vs Output Current

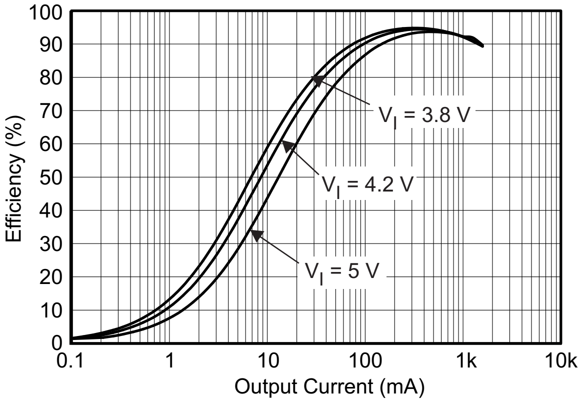


Figure 2. DCDC1: Efficiency vs Output Current

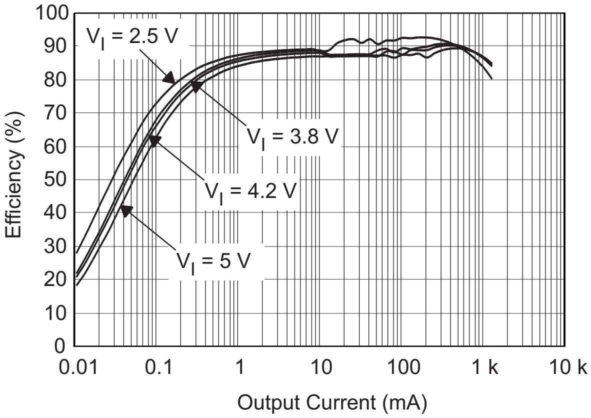


Figure 3. DCDC2: Efficiency vs Output Current

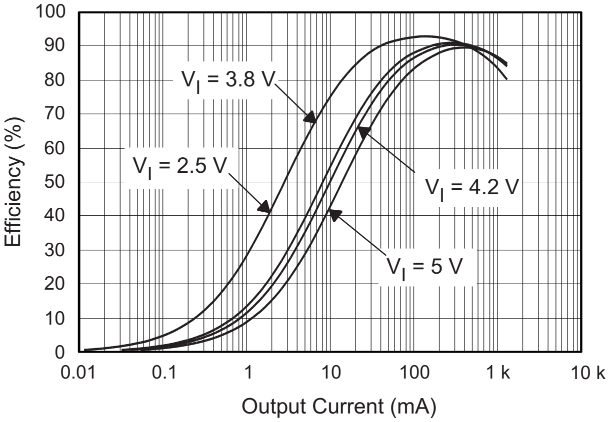


Figure 4. DCDC2: Efficiency vs Output Current

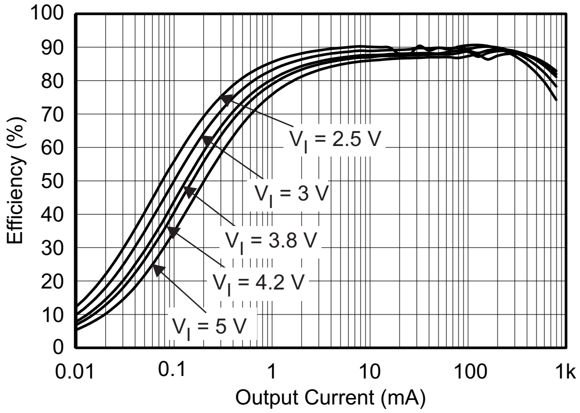


Figure 5. DCDC3: Efficiency vs Output Current

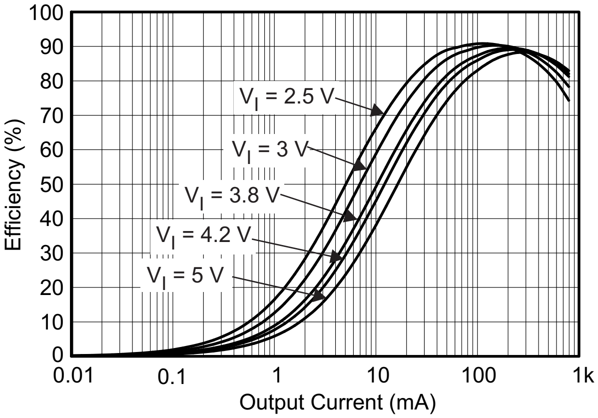


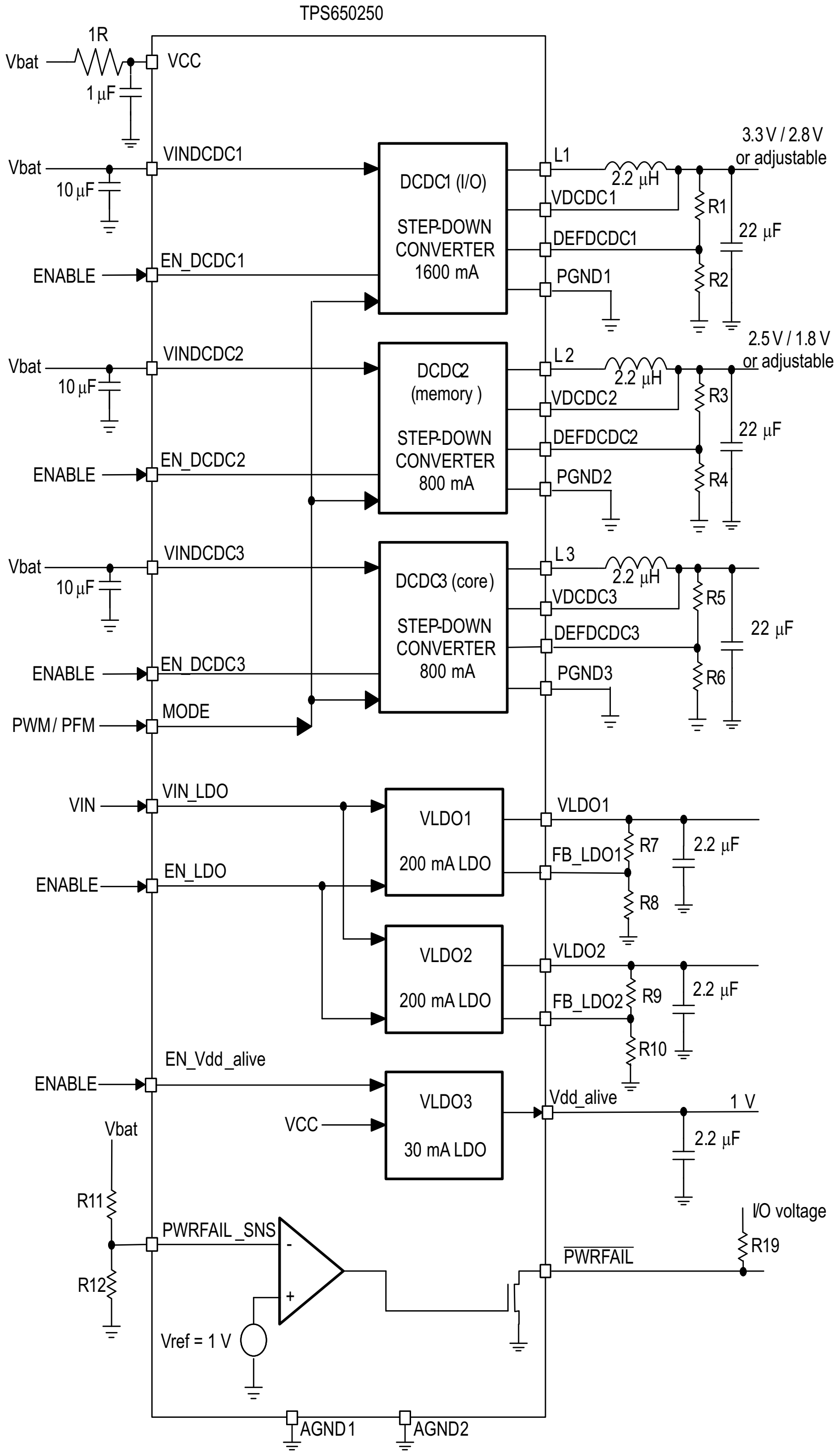
Figure 6. DCDC3: Efficiency vs Output Current

7 Detailed Description

7.1 Overview

The TPS650250 integrates three step-down converters, two general purpose LDOs and one always on low power LDO for applications powered by one LI-Ion or Li-Polymer cell or a single input voltage from 2.5 V to 6 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Step-Down Converters, VDCDC1, VDCDC2 AND VDCDC3

The TPS650250 incorporates three synchronous step-down converters operating typically at 2.25 MHz fixed frequency PWM (Pulse Width Modulation) at moderate to heavy load currents. At light load currents the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation). VDCDC1 delivers up to 1.6 A, VDCDC2 and VDCDC3 are capable of delivering up to 0.8 A of output current.

The converter output voltages can be programmed via the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. The pins can either be connected to GND, VCC or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 2.8 V or 3.3 V depending on the DEFDCDC1 configuration pin, if DEFDCDC1 is tied to ground the default is 2.80 V, if it is tied to VCC the default is 3.3 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC1 V. Reference the section on Output Voltage Selection for details on setting the output voltage range.

The VDCDC2 converter defaults to 1.8 V or 2.5 V depending on the DEFDCDC2 configuration pin, if DEFDCDC2 is tied to ground the default is 1.8 V, if it is tied to VCC the default is 2.5 V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC2 V.

On the DEFDCDC3 pin for the VDCDC3 converter, a resistor divider must be connected to set the output voltage. This pin does not accept a logic signal like DEFDCDC1 or DEFDCDC2. The value for the resistor divider can be changed during operation, so voltage scaling can be implemented by changing the resistor value.

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot through current, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC-DC converters operate synchronized to each other, with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turn on and the VDCDC2 and a further 90° shift to the VDCDC3 switch turn on decreases the input RMS current and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-Ion battery voltage of 3.7 V to 3.3 V, the VDCDC2 converter from 3.7 V to 2.5 V and the VDCDC3 converter from 3.7 V to 1.5 V.

7.3.2 Power Save Mode Operation

As the load current decreases, the converters enter Power Save Mode operation. During Power Save Mode the converters operate in a burst mode (PFM mode) with a frequency between 1.125 MHz and 2.25 MHz for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency, with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then Power Save Mode is entered. The typical threshold to enter Power Save Mode can be calculated as follows:

$$I_{PFMDCDC1enter} = \frac{VINDCDC\ 1}{24\ \Omega}$$

$$I_{PFMDCDC2enter} = \frac{VINDCDC\ 2}{26\ \Omega}$$

$$I_{PFMDCDC3leave} = \frac{VINDCDC\ 3}{39\ \Omega} \quad (1)$$

During Power Save Mode the output voltage is monitored with a comparator and by maximum skip burst width. As the output voltage falls below the threshold, set to the nominal V_O, the P-channel switch turns on and the converter effectively delivers a constant current as defined below.

Feature Description (continued)

$$I_{PFMDCDC1leave} = \frac{VINDCDC\ 1}{18\ \Omega}$$

$$I_{PFMDCDC2leave} = \frac{VINDCDC\ 2}{20\ \Omega}$$

$$I_{PFMDCDC3enter} = \frac{VINDCDC\ 3}{29\ \Omega} \tag{2}$$

If the load is below the delivered current then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power save mode is exited, and the converter returns to PWM mode if either of the following conditions are met:

1. The output voltage drops 2% below the nominal V_O due to increased load current
2. The PFM burst time exceeds 16 × 1/fs (7.1µs typical)

These control methods reduce the quiescent current to typically 14µA per converter and the switching activity to a minimum thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor values makes the output ripple tend to zero. Power Save Mode can be disabled by pulling the MODE pin high. This forces all DC-DC converters into fixed frequency PWM mode.

7.3.3 Soft Start

Each of the three converters has an internal soft start circuit that limits the inrush current during start-up. The soft start is realized by using a very low current to initially charge the internal compensation capacitor. The soft start time is typically 750 µs if the output voltage ramps from 5% to 95% of the final target value. If the output is already pre-charged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170µs between the converter being enabled and switching activity actually starting. This is to allow the converter to bias itself properly, to recognize if the output is pre-charged, and if so, to prevent discharging of the output while the internal soft start ramp catches up with the output voltage.

7.3.4 100% Duty Cycle Low Dropout Operation

The TPS650250x converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage and can be calculated as:

$$Vin_{min} = Vout_{min} + Iout_{max} \times \left(RDSon_{max} + R_L\right)$$

where

- $Iout_{max}$ = Maximum load current (note: ripple current in the inductor is zero under these conditions)
- $RDSon_{max}$ = Maximum P-channel switch RDSon
- R_L = DC resistance of the inductor
- $Vout_{min}$ = Nominal output voltage minus 2% tolerance limit (3)

7.3.5 Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to operate well with low value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 300 mV at the rated output current. Each LDO sports a current limit feature. Both LDOs are enabled by the EN_LDO pin. The LDOs also have reverse conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS650250 step-down and LDO voltage regulators automatically power down when the Vcc voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

Feature Description (continued)

7.3.6 Undervoltage Lockout

The undervoltage lockout circuit for the five regulators on the TPS650250x prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the Vcc pin; the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. Note that when any of the DC-DC converters are running there is an input current at the Vcc pin, which can be up to 3 mA when all three converters are running in PWM mode. This current needs to be taken into consideration if an external RC filter is used at the Vcc pin to remove switching noise from the TPS650250x internal analog circuitry supply. See the Vcc-Filter section for details on the external RC filter.

7.3.7 $\overline{\text{PWRFAIL}}$

The $\overline{\text{PWRFAIL}}$ signal is generated by a voltage detector at the PWRFAIL_SNS input. The input signal is compared to a 1 V threshold (falling edge) with 5% (50 mV) hysteresis. $\overline{\text{PWRFAIL}}$ is an open drain output which is actively low when the input voltage at PWRFAIL_SNS is below the threshold.

7.4 Device Functional Modes

The TPS650250x power-up sequencing is designed to be entirely flexible and customer driven; this is achieved simply by providing separate enable pins for each switch-mode converter and a common enable signal for LDO1 and LDO2. The relevant control pins are described in Table 2.

Table 2. Control Pins for DCDC Converters

PIN NAME	INPUT/ OUTPUT	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter set with an eternal resistor divider.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8V, DEFDCDC2 = VCC defaults VDCDC2 to 2.5V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 2.80V, DEFDCDC1 = VCC defaults VDCDC1 to 3.3V.
EN_DCDC3	I	Set EN_DCDC3 = 0 to disable or EN_DCDC3 = 1 to enable the VDCDC3 converter
EN_DCDC2	I	Set EN_DCDC2 = 0 to disable or EN_DCDC2 = 1 to enable the VDCDC2 converter
EN_DCDC1	I	Set EN_DCDC1 = 0 to disable or EN_DCDC1 = 1 to enable the VDCDC1 converter

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This device integrates three step-down converters and three LDOs which can be used to power the voltage rails needed by a processor. A typical configuration for using the TPS650250 PMIC to power the Samsung processor S3C6400-533MHz is shown in Figure 7.

8.2 Typical Application

8.2.1 Typical Configuration For The Samsung Processor S3C6400-533MHz

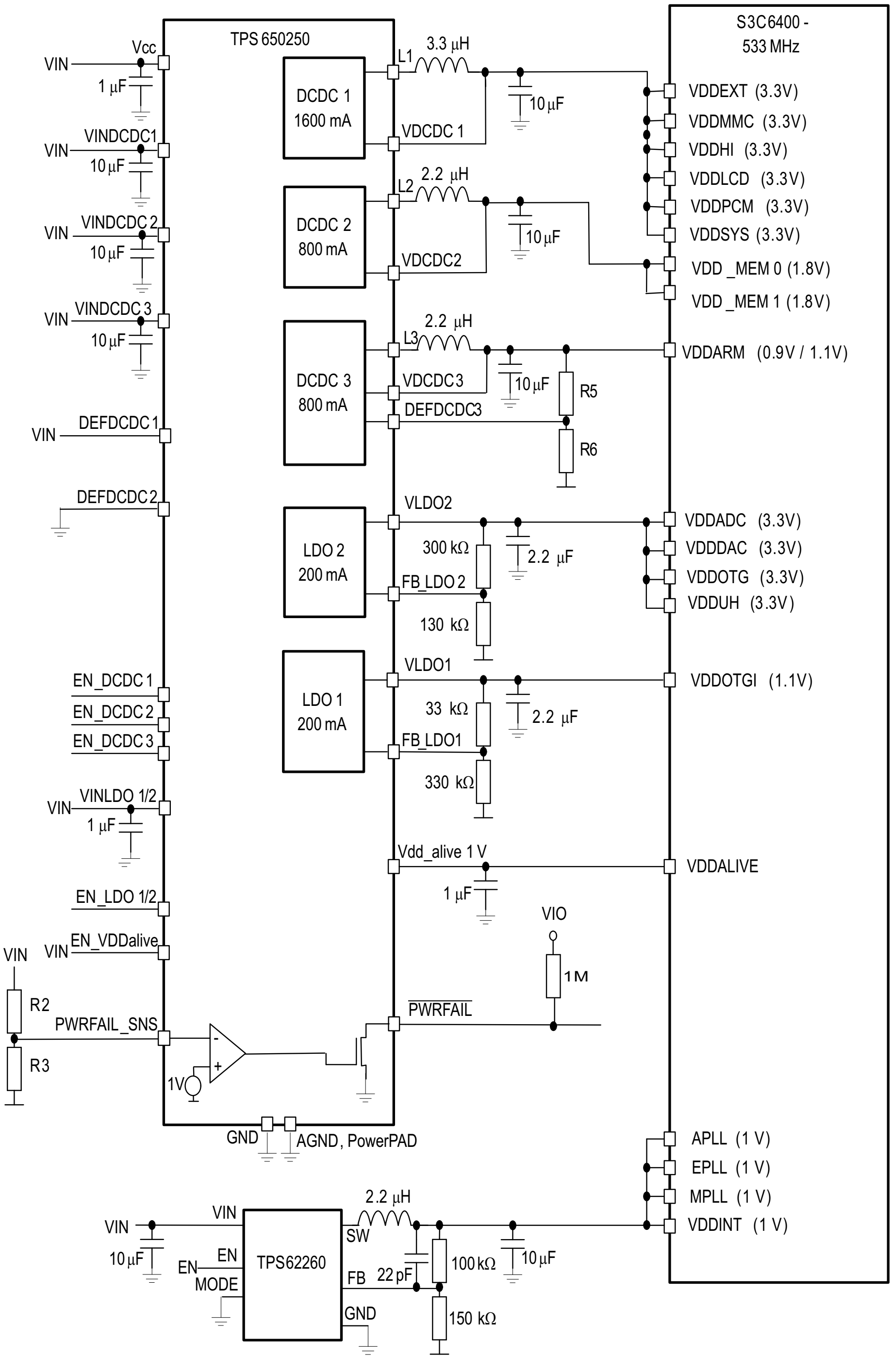


Figure 7. Samsung Processor Configuration

Typical Application (continued)

8.2.2 Design Requirements

The design parameters for the Samsung Processor Configuration are shown below.

Table 3. Design Parameters

Design Parameter	Value
Input Voltage Range	4.5 V to 5.5 V
DCDC1 Output Voltage	3.3 V
DCDC2 Output Voltage	1.8 V
DCDC3 Output Voltage	1.0 V
LDO1 Output Voltage	1.1 V
LDO2 Output Voltage	3.3 V

8.2.3 Detailed Design Procedure

This section describes the application design procedure for the TPS650250 PMIC.

8.2.3.1 Inductor Selection for the DCDC Converters

The three converters operate with 2.2 μH output inductors. Larger or smaller inductor values can be used to optimize performance of the device for specific conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductor influences directly the efficiency of the converter. Therefore, an inductor with the lowest DC resistance should be selected for the highest efficiency.

For a fast transient response, a 2.2 μH inductor in combination with a 22 μF output capacitor is recommended. For an output voltage above 2.8 V, an inductor value of 3.3 μH minimum is required. Lower values result in an increased output voltage ripple in PFM mode. The minimum inductor value is 1.5 μH, but an output capacitor of 22 μF minimum is needed in this case.

Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{L\,max} = I_{out\,max} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current (4)

The highest inductor current occurs at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consideration must be given to the difference in the core material from inductor to inductor which has an impact on efficiency especially at high switching frequencies. See Table 4 and the typical applications for possible inductors.

Table 4. Tested Inductors

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
DCDC3 Converter	3.3 μH	LPS3015-332 (output current up to 1 A)	Coilcraft
	2.2 μH	LPS3015-222 (output current up to 1 A)	Coilcraft
	3.3 μH	VLCF4020T-3R3N1R5	TDK
	2.2 μH	VLCF4020T-2R2N1R7	TDK
DCDC3 Converter	2.2 μH	LPS3010-222	Coilcraft
	2.2 μH	LPS3015-222	Coilcraft
	2.2 μH	VLCF4020-2R2	TDK

8.2.3.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the inductive converters implemented in the TPS650250x allows the use of small ceramic capacitors with a typical value of 10 µF for each converter, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. Refer to Table 5 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{RMSCout} = \text{Vout} \times \frac{1 - \frac{\text{Vout}}{\text{Vin}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{5}$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta\text{Vout} = \text{Vout} \times \frac{1 - \frac{\text{Vout}}{\text{Vin}}}{L \times f} \times \left(\frac{1}{8 \times \text{Cout} \times f} + \text{ESR} \right) \tag{6}$$

Where the highest output voltage ripple occurs at the highest input voltage, Vin.

At light load currents the converters operate in Power Save Mode and output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. Typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.3.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10 µF ceramic input capacitor on its input pin VINDCDCx. The input capacitor can be increased without any limit for better input voltage filtering. The Vcc pin should be separated from the input for the DC-DC converters. A filter resistor of up to 10 Ω and a 1 μF capacitor should be used for decoupling the Vcc pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow via this resistor into the Vcc pin when all converters are running in PWM mode.

Table 5. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER		COMMENTS
22 μF	1206	TDK	C3216X5R0J226M	Ceramic
22 μF	1206	Taiyo Yuden	JMK316BJ226ML	Ceramic
22 μF	0805	TDK	C2012X5R0J226MT	Ceramic
22 μF	0805	Taiyo Yuden	JMK212BJ226MG	Ceramic
10 μF	0805	Taiyo Yuden	JMK212BJ106M	Ceramic
10 μF	0805	TDK	C2012X5R0J106M	Ceramic

8.2.3.4 Output Voltage Selection

The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See Table 6 for the default voltages if the pins are pulled to GND or to Vcc.

Table 6. Voltage Options

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	VCC	3.3 V
	GND	2.80 V
DEFDCDC2	VCC	2.5 V
	GND	1.8 V
DEFDCDC3	external voltage divider	0.6 V to VinDCDC3

If a different voltage is needed, an external resistor divider can be added to the DEFDCDC1 or DEFDCDC2 pin as shown in Figure 8:

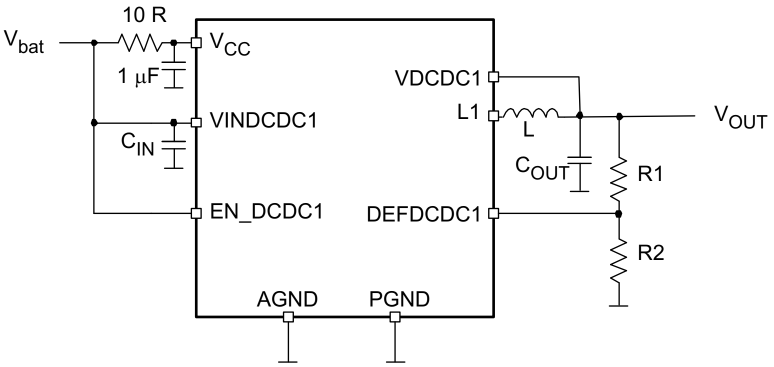


Figure 8. External Resistor Divider Added

When a resistor divider is connected to DEFDCDC1 or DEFDCDC2, the output voltage can be set from 0.6 V up to the input voltage V_{bat}. The total resistance (R1+R2) of the voltage divider should be kept in the 1 MΩ range in order to maintain a high efficiency at light load. $V_{DEFDCDCx} = 0.6V$

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1+R2}{R2}$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDCx}}\right) - R2$$

8.2.3.5 Voltage Change on VDCDC3

The output voltage of VDCDC3 is set with an external resistor divider at DEFDCDC3. This pin must not be connected to GND or VINDCDC3. The value of the resistor divider can be changed during operation to allow dynamic voltage scaling.

8.2.3.6 Vdd_alive Output

The Vdd_alive LDO is typically connected to the Vdd_alive input of the Samsung application processor. It provides an output voltage of 1 V at 30 mA. It is recommended to add a capacitor of 2.2 µF minimum to the Vdd_alive pin. The LDO can be disabled by pulling the EN_Vdd_alive pin to GND.

8.2.3.7 LDO1 and LDO2

The LDOs in the TPS650250 are general purpose LDOs which are stable using ceramics capacitors. The minimum output capacitor required is 2.2 µF. The LDOs output voltage can be changed to different voltages between 1 V and 3.3 V using an external resistor divider. Therefore they can also be used as general purpose LDOs in the application. The supply voltage for the LDOs needs to be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and therefore providing the highest efficiency.

The total resistance (R5+R6) of the voltage divider should be kept in the 1 MΩ range in order to maintain high efficiency at light load. V_{FBLDOx}= 1.0 V.

$$V_{OUT} = V_{FBLDOx} \times \frac{R5 + R6}{R6}$$

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FBLDOx}}\right) - R6$$

8.2.3.8 Vcc-Filter

An RC filter connected at the Vcc input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 1 Ω and 1 µF is used to filter the switching spikes, generated by the DC-DC converters. A larger resistor than 10 Ω should not be used because the current into Vcc of up to 2.5 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at Vcc internally to switch off too early.

8.2.4 Application Curves

The application curves were taken using the following inductor/output capacitor combinations

CONVERTER	INDUCTOR	OUTPUT CAPACITOR	OUTPUT CAPACITOR VALUE
DCDC1	VLCF4020-3R3	C2012X5R0J226M	22 µF
DCDC2	VLCF4020-2R2	C2012X5R0J226M	22 µF
DCDC3	LPS3010-222	C2012X5R0J226M	22 µF

Table 7. Table of Application Curves

			FIGURE
	Line transient response VDCDC1		Figure 9
	Line transient response VDCDC2		Figure 10
	Line transient response VDCDC3		Figure 11
	Load transient response VDCDC1		Figure 12
	Load transient response VDCDC2		Figure 13
	Load transient response VDCDC3		Figure 14
	Output voltage ripple DCDC2; PFM mode		Figure 15
	Output voltage ripple DCDC2; PWM mode		Figure 16
	Load regulation for Vdd_alive		Figure 17
	Start-up VDCDC1 to VDCDC3		Figure 18
	Start-up LDO1 and LDO2		Figure 19

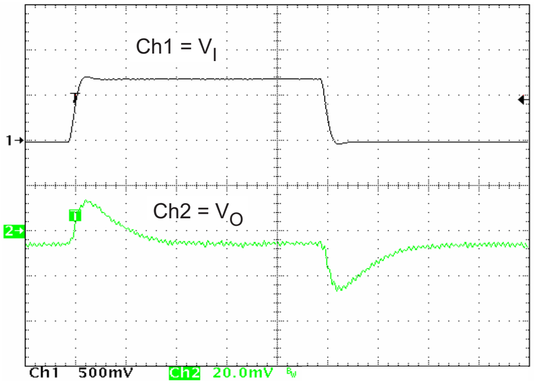


Figure 9. VDCDC1 Line Transient Response

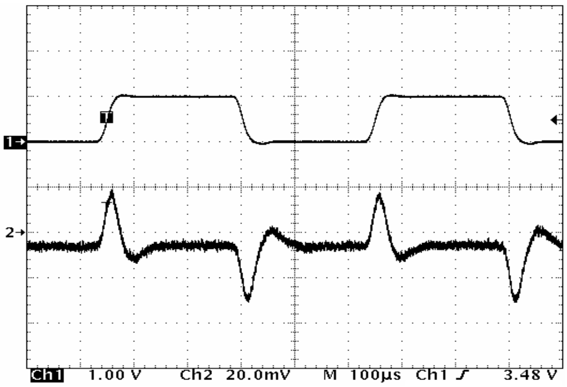


Figure 10. VDCDC2 Line Transient Response

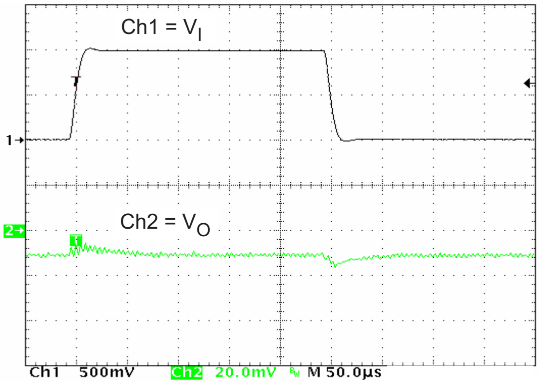


Figure 11. VDCDC3 Line Transient Response

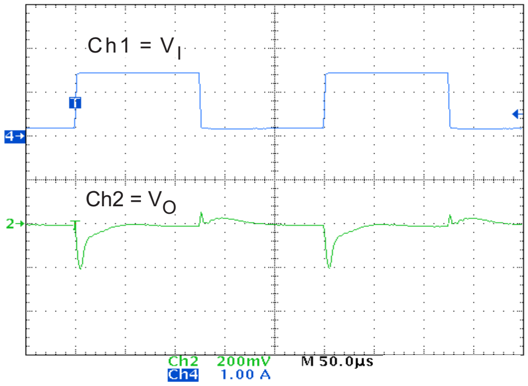


Figure 12. VDCDC1 Load Transient Response

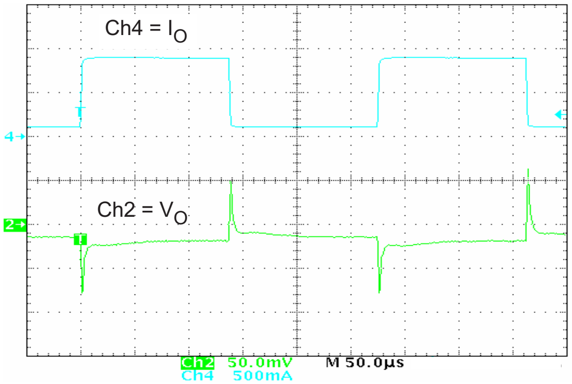


Figure 13. VDCDC2 Load Transient Response

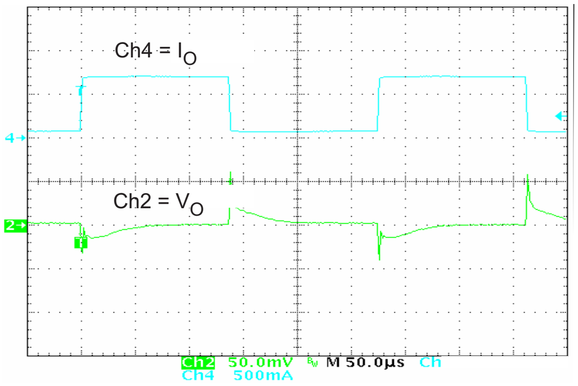


Figure 14. VDCDC3 Load Transient Response

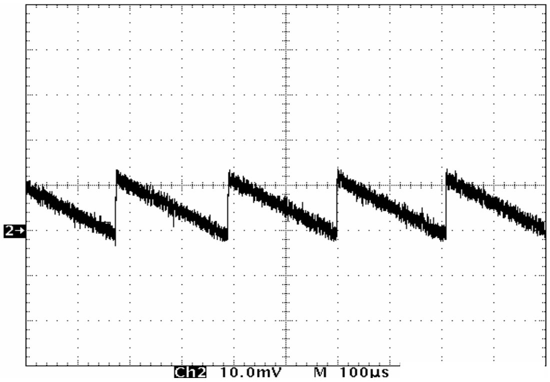


Figure 15. VDCDC2 Output Voltage Ripple

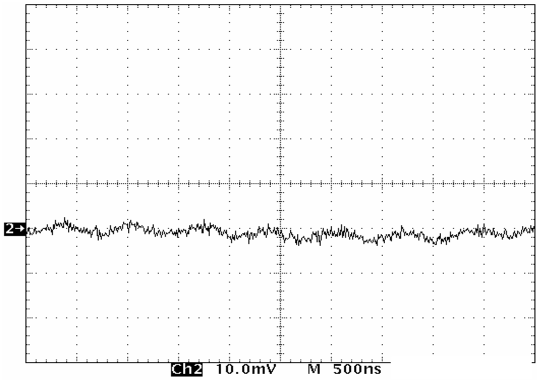


Figure 16. VDCDC2 Output Voltage Ripple

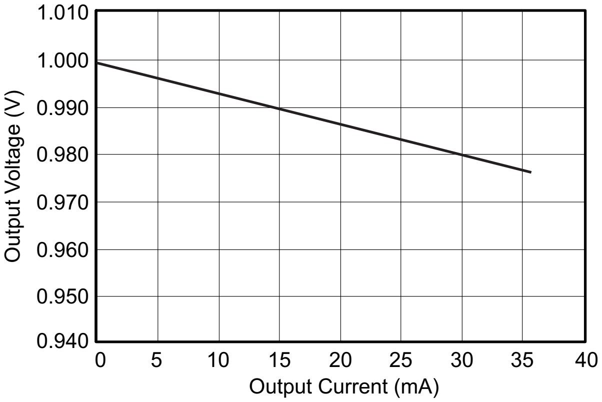


Figure 17. VDD_ALIVE Output Voltage vs Output Current

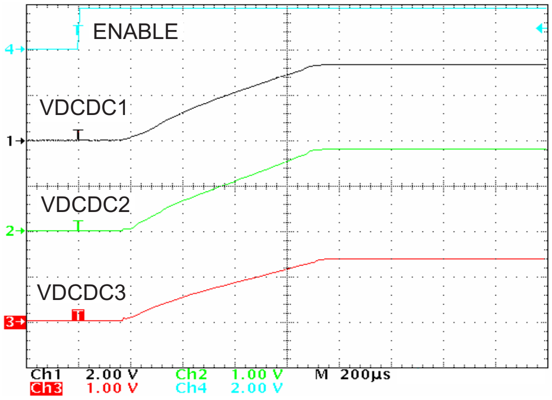


Figure 18. Startup VDCDC1, VDCDC2, VDCDC3

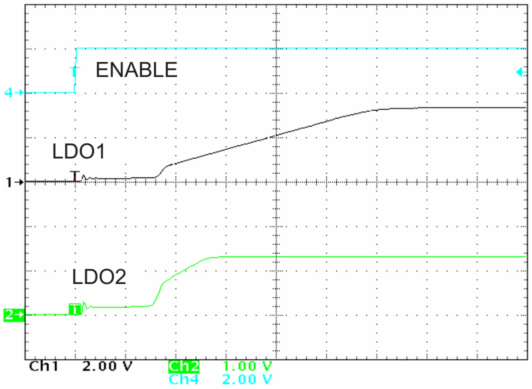


Figure 19. Startup LDO1 and LDO2

9 Power Supply Recommendations

The TPS650250 is designed to operate from an input voltage supply range between 3.5 V and 5.5 V. The input supply should be well regulated. If the input supply is located more than a few inches from the TPS650250, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- The VINDCDC1, VINDCDC2 and VINDCDC3 terminals should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 10 uF ceramic with a X5R or X7R dielectric.
- The VINLDO terminal should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 1 uF ceramic with a X5R or X7R dielectric.
- The optimum placement is closest to the individual voltage terminals and the AGNDx terminals.
- The AGNDx terminals should be tied to the pcb ground plane at the terminal of the IC.
- The cross sectional area loop from the input capacitor to the VINDCDCx input and corresponding PGNDx terminal should be minimized as much as possible.
- Route the feedback signal for each of the step-down converters next to the current path of the converter in order to decrease the cross sectional area of the feedback loop which minimizes noise injection into the loop.
- Do not route any noise sensitive signals under or next to any of the step-down inductors. Ensure a keepout region directly under the inductors or at least provide ground shielding.
- It is recommended to have the layer directly underneath the IC to be a solid copper ground plane.

10.2 Layout Example

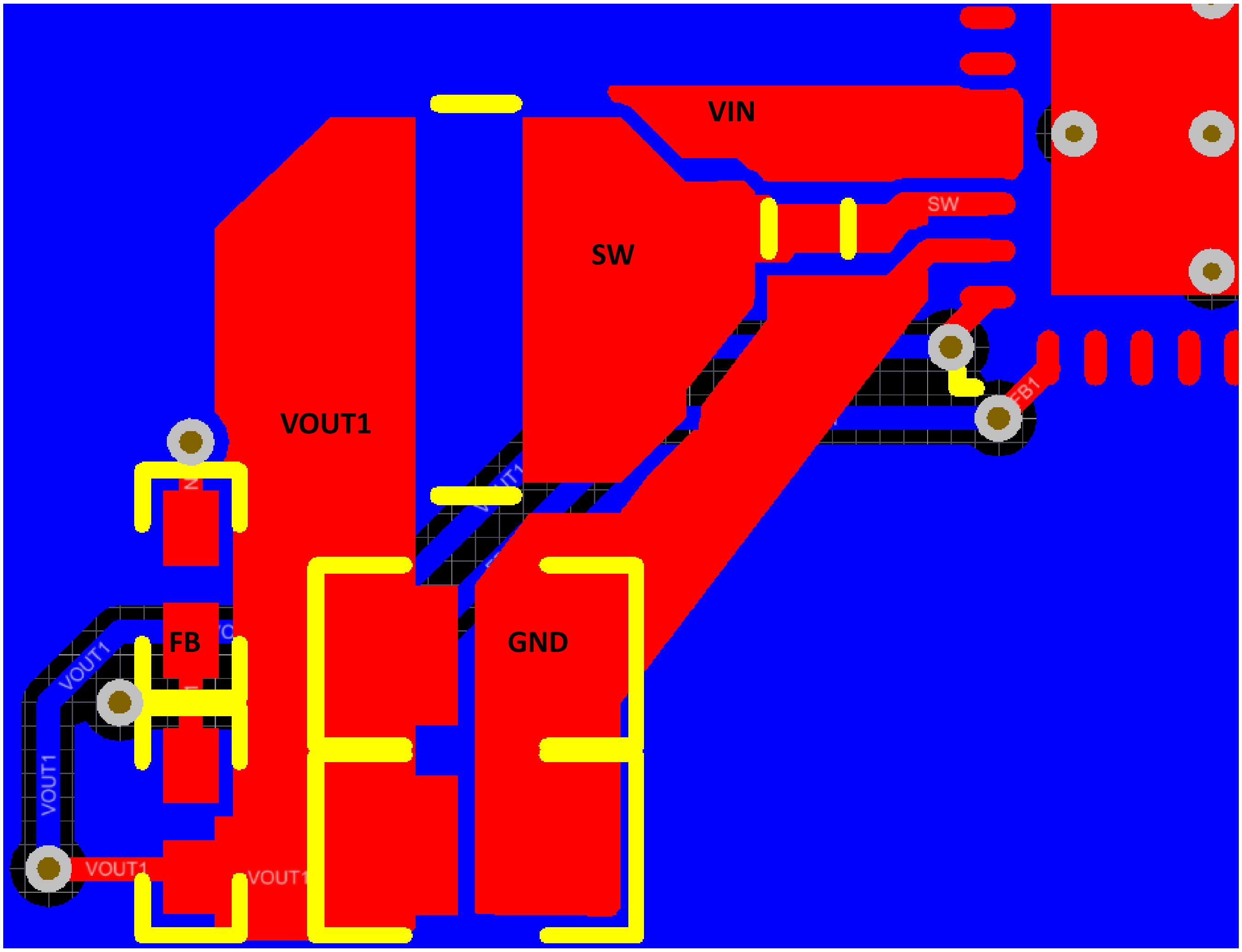


Figure 20. Layout Example of VDCDC1

The most important layout practice is the placement of the input capacitor. The input capacitor should be placed as close as possible to the VINDCDCx and GND pins of the converters inorder to minimize the parasitic inductance and loop.

The second most important layout practice is to minimize the feedback cross-sectional loop of the converters. Route the feedback trace along a close path of the VOUT and switch nodes.

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

開発サポートについては、次の資料を参照してください。

- AMIC110上のDDRレスEtherCAT®スレーブのリファレンス・デザイン
- EtherCATスレーブとマルチプロトコル産業用イーサネットのリファレンス・デザイン
- TPS650250を使用するXilinx Spartan 6 FPGA電源のリファレンス・デザイン
- PSRフライバックとコンパクトなDC/DC段を使用したPLC用ユニバーサル・ライン電源のリファレンス・デザイン
- スマート・ホームおよびエネルギー・ゲートウェイのリファレンス・デザイン
- ストリーミング・オーディオのリファレンス・デザイン

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『プロセッサ・アプリケーション向けパワー・マネージメントIC (PMIC)による設計の強化』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『コンパレータ入力における分圧抵抗の最適化』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『TPS650240 または TPS650250 を使用する Samsung™ s3c2416 用電源のリファレンス・デザイン』*
- テキサス・インスツルメンツ、*『TPS650250によるAM335xの電力供給』*ユーザー・ガイド
- テキサス・インスツルメンツ、*『リチウムイオン電池を使用するシステムでのTPS650250EVM電力管理ICの使用』*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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Samsung is a trademark of Samsung Semiconductor.
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11.6 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS650250RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650250
TPS650250RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650250
TPS650250RHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650250
TPS650250RHBRG4.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650250
TPS650250RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650250
TPS650250RHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 650250

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

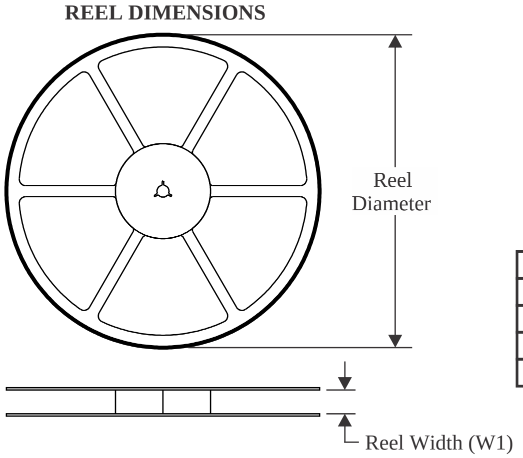
OTHER QUALIFIED VERSIONS OF TPS650250 :

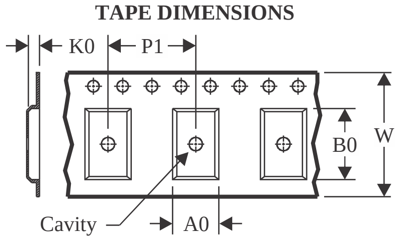
- Automotive : TPS650250-Q1

NOTE: Qualified Version Definitions:

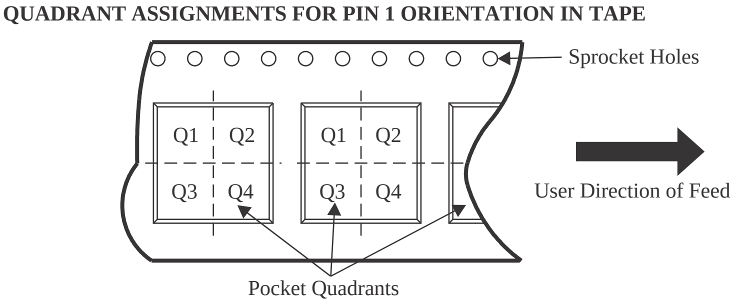
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





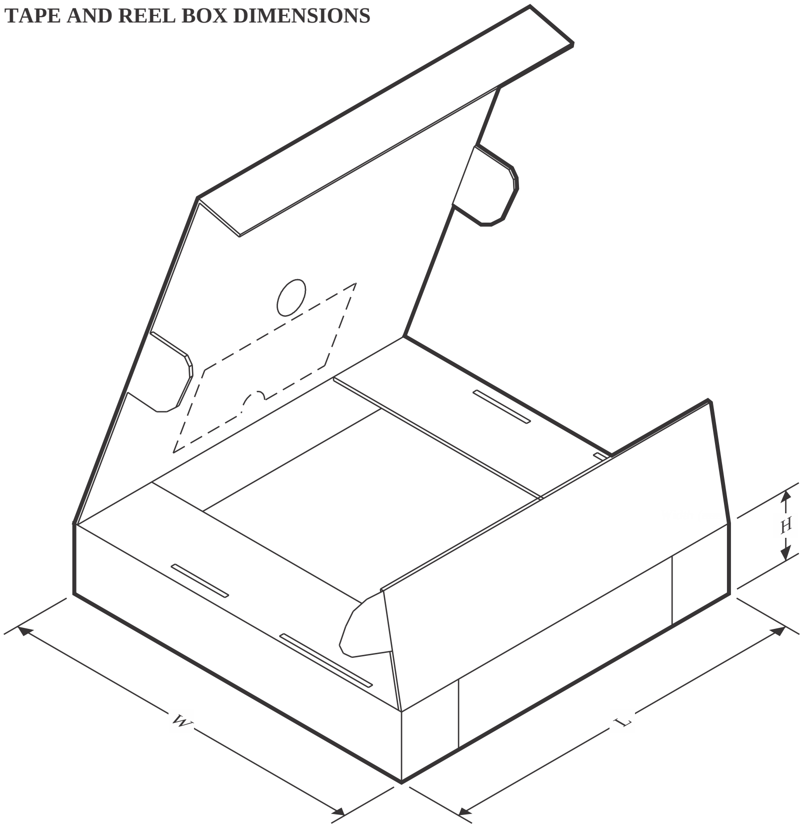
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650250RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650250RHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650250RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650250RHBR	VQFN	RHB	32	3000	353.0	353.0	32.0
TPS650250RHBRG4	VQFN	RHB	32	3000	353.0	353.0	32.0
TPS650250RHBT	VQFN	RHB	32	250	213.0	191.0	35.0

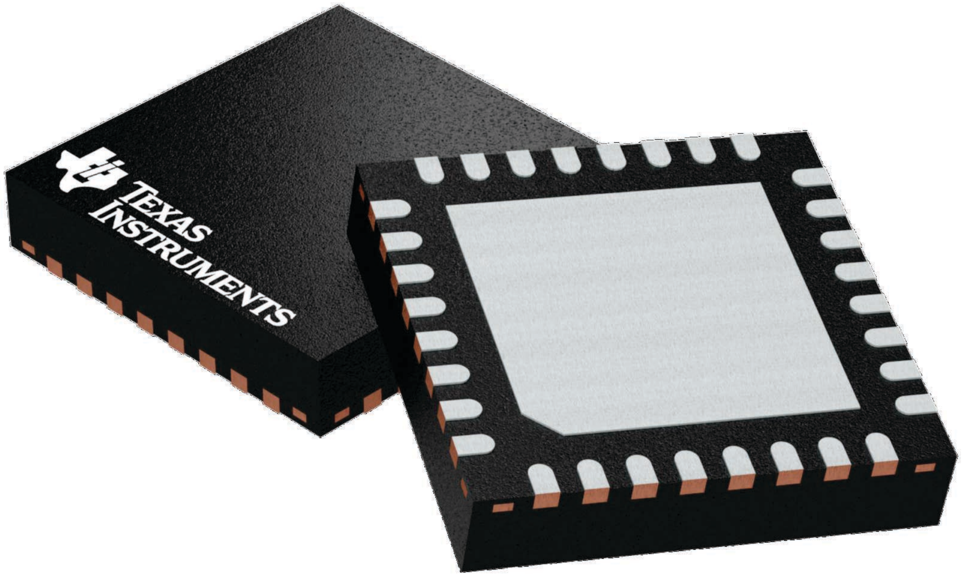
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

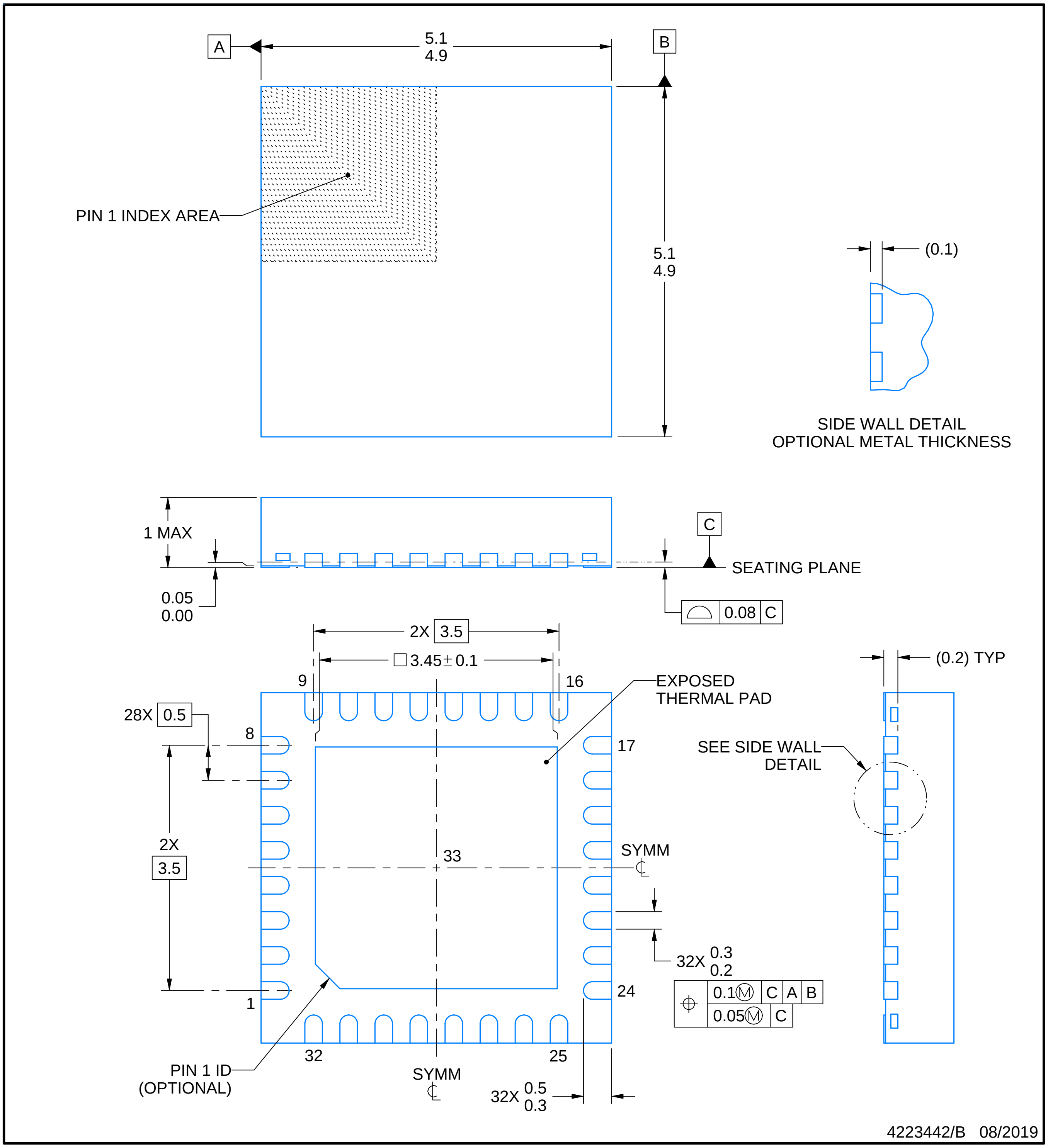
4224745/A

PACKAGE OUTLINE

RHB0032E

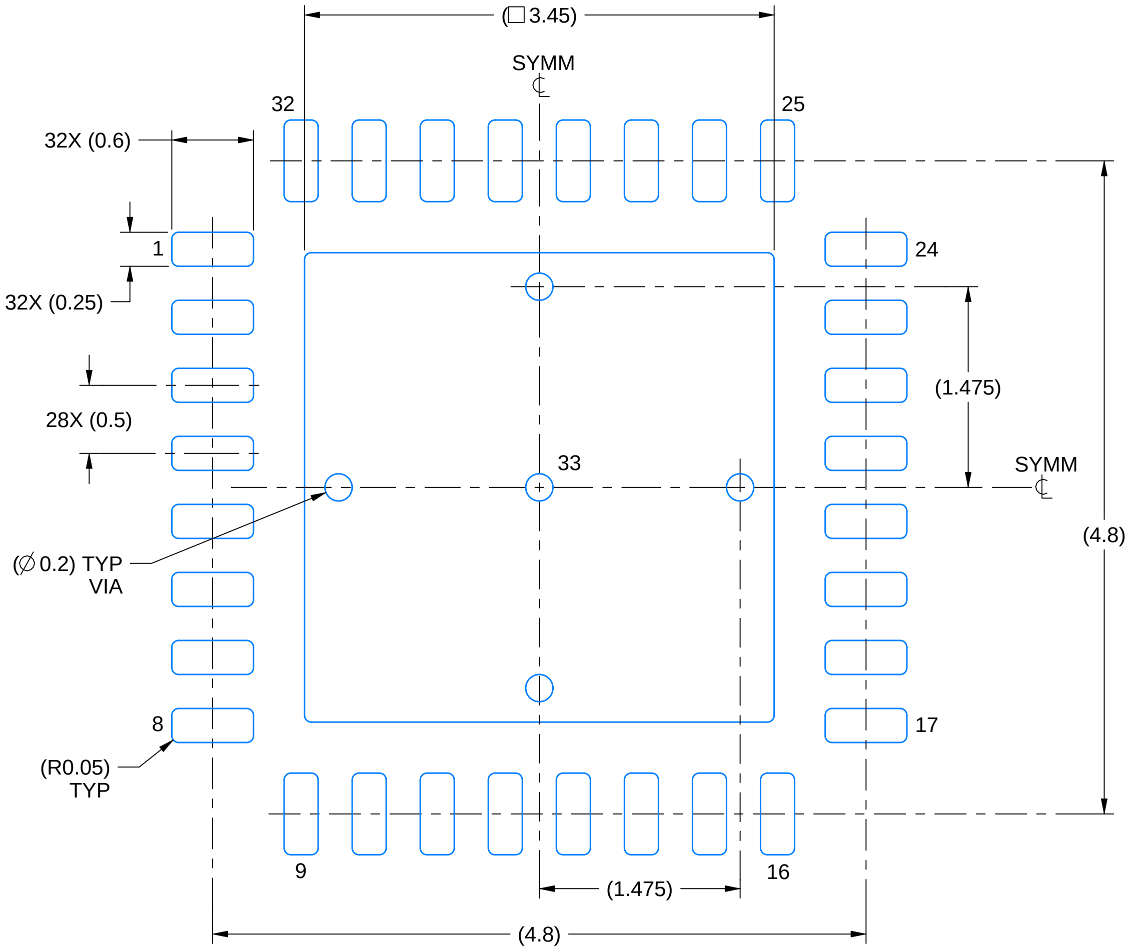
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

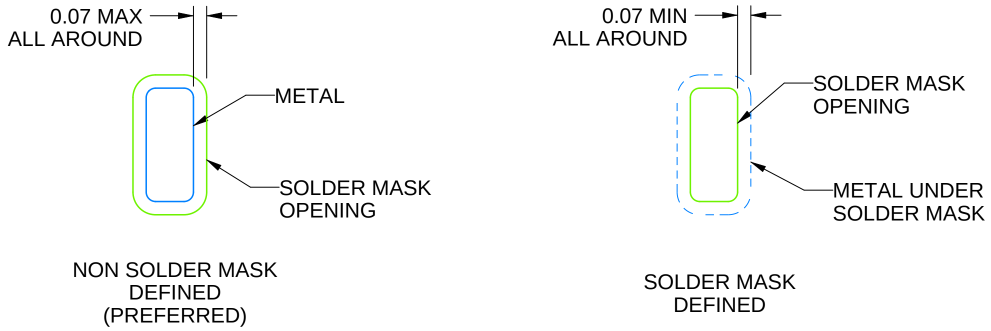


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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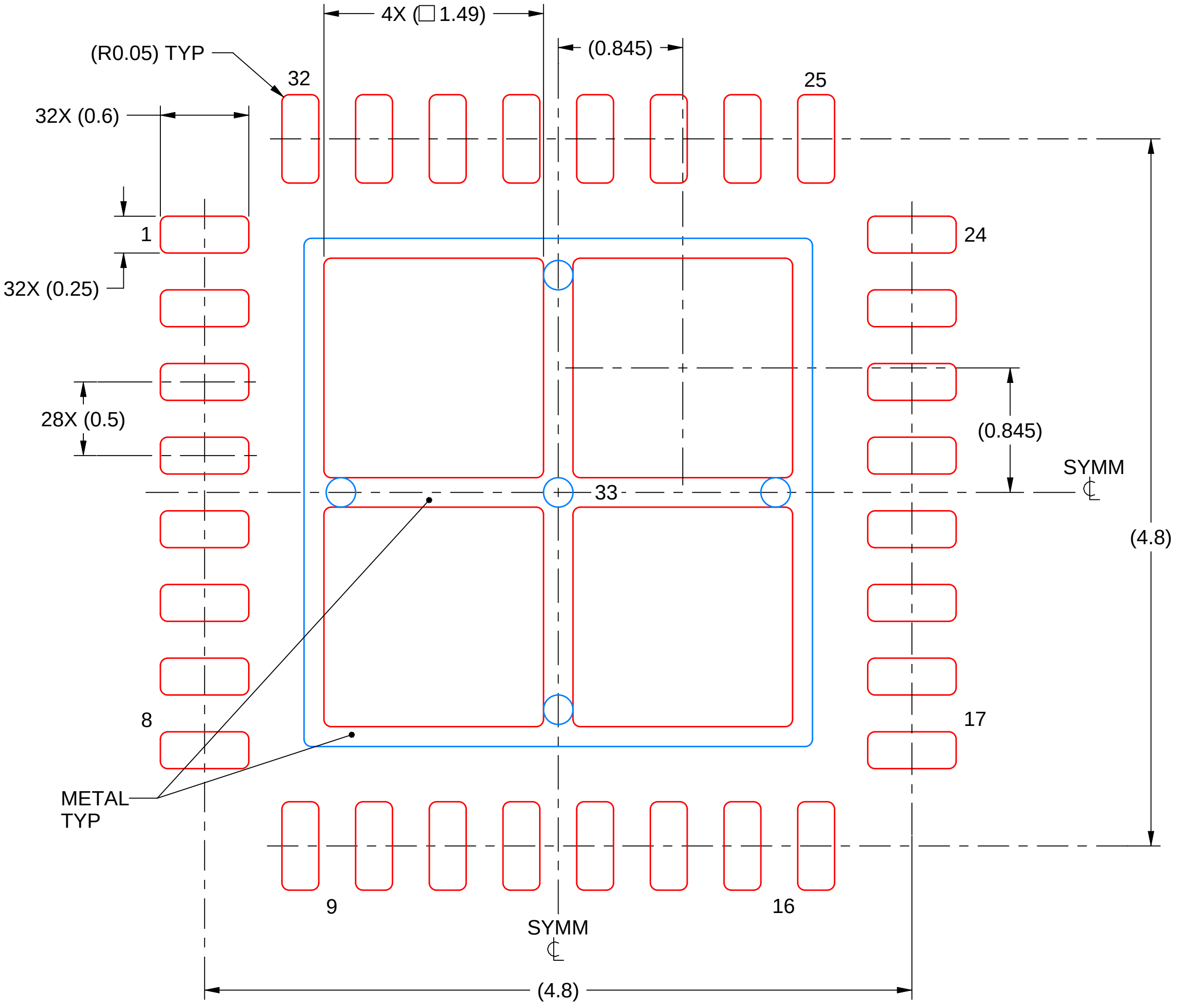
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

最終更新日：2025 年 10 月