TPS6513x デュアル、正 / 負出力 DC-DC コンバータ

1 特長

- 入力電圧範囲:2.7V～5.5V
- V_{POS} 昇圧コンバータの正電圧出力
  - 可変出力電圧:最大 15V
  - 2 つのスイッチ電流制限オプション:0.8A/2A
  - 変換効率:最大 89%
- V_{NEG} 反転昇降圧コンバータの負電圧出力
  - 可変出力電圧:最小 -15V
  - 2 つのスイッチ電流制限オプション:0.8A/2A
  - 変換効率:最大 81%
- 外部 P チャネル FET の制御出力により、バッテリからの完全な切断をサポート
- シャットダウン時電流:1µA
- 個別のイネーブル入力により、柔軟な出力シーケンシングが可能
- 保護機能
  - V_{POS} および V_{NEG} での過電圧保護機能
  - 入力低電圧誤動作防止機能
  - サーマル・シャットダウン保護機能
- 4mm × 4mm VQFN-24 パッケージ (RGE)

2 アプリケーション

- LCD および AMOLED ディスプレイ (約 4 インチ～17 インチ)
  - パーソナル・エレクトロニクス (ノート PC、モニタ、ゲーム)
  - ビル・オートメーション (エレベーター、サーモスタット)
  - ヘルスケア、フィットネス、EPOS、産業用 HMI、テストと測定
- 汎用分割レール電源
  - T&M、データ・アクイジション、DAC、ADC
  - 差動オーディオ PA 電源
  - ファクトリ・オートメーションおよび制御入力 / 出力モジュール
  - 差動オペアンプおよびコンパレータ電源

3 概要

TPS6513x デバイスはデュアル出力の DC-DC コンバータ電源で、最大 15V の正出力と、最低 -15V の負出力を生成します。このコンバータは低い出力電圧リップルを維持します。通常、最大出力電流は 200mA～500mA の範囲内で、入力電圧に対する出力電圧の比と電流制限オプションによって決まります。総合 (V_{POS} と V_{NEG}) 効率は 85%に達し、システムの温度上昇を防ぎ、バッテリ駆動時間を延長します。このデバイスの入力電圧範囲は 2.7V～5.5V と広いため、バッテリまたは固定 3.3V または 5V レールから電力を供給できます。

このコンバータは固定周波数の PWM 制御トポロジで動作します。パワー・セーブ・モードで動作する場合は、軽負荷電流時にパルス・スキップ・モードを使用します。このデバイスはわずか 500µA の静止時電流で動作します。

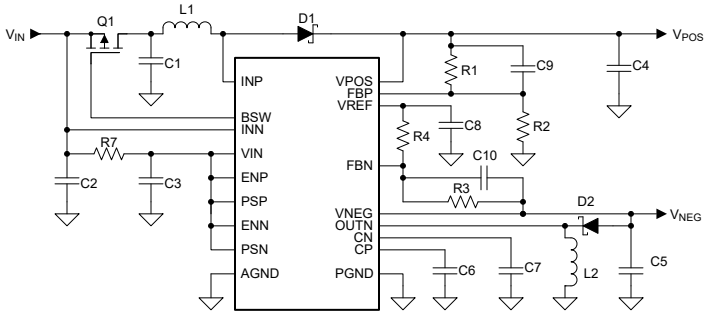
独立したイネーブル・ピンにより、いずれの出力でも柔軟なパワーアップ / パワーダウン・シーケンシングを実現できます。正と負の出力は独立して動作するため、非対称的な出力電圧および電流を供給できます。

このコンバータは内部電流制限、過電圧保護、サーマル・シャットダウン機能を備えており、障害状況で非常に高い信頼性を実現します。このコンバータは、4mm × 4mm の VQFN-24 パッケージで供給されます。ソリューション・サイズが小さく、最小スイッチング周波数が 1.25MHz であるため、インダクタを小型化でき、必要な他の外部部品の数も少なくて済みます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS65130	VQFN (24)	4.00mm × 4.00mm
TPS65131		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (January 2016) to Revision E (April 2022)	Page
• 文書全体の表、図、相互参照の採番方法を更新	1
• 最初のページのデバイスの説明を更新	1
• Changed ESD HBM specification from "±2000" to "±1000"	4
• Changed text string in セクション 8.2.2.1.1 description From "....to set the divider current at 5 µA or greater" To "...to set the divider current at 5 µA to 10 µA"	12
• Added セクション 8.2.3 description	15
• Corrected typographic error in x-axis labels for 図 8-39, 図 8-40, 図 8-41, 図 8-45, and 図 8-46	16

Changes from Revision C (June 2015) to Revision D (January 2016)	Page
• 「特長」の箇条書き項目「2.7V～5.5V の入力電圧範囲」をリストの先頭に移動し、「アプリケーション」の箇条書き一覧を変更	1

Changes from Revision B (September 2004) to Revision C (March 2015)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「熱に関する情報」、「電気的特性」、「詳細説明」セクション、「代表的特性」セクションを追加、更新、再編成。	1

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5 Pin Configuration and Functions

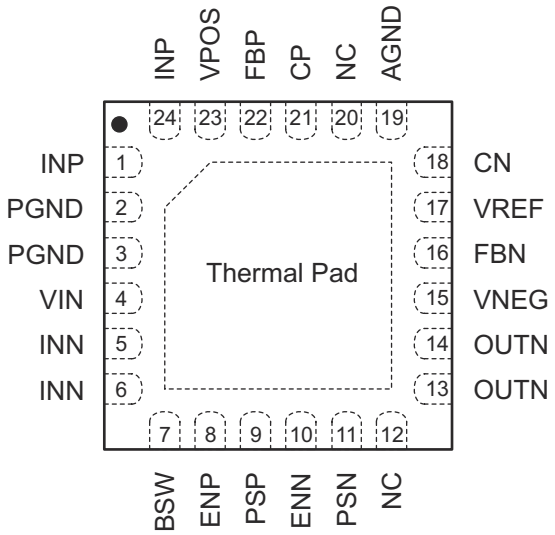


図 5-1. RGE Package, 24-PIN VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	19	—	Analog ground pin
BSW	7	O	Gate control pin for external battery switch. This pin goes low when ENP is set high.
CN	18	—	Compensation pin for inverting converter control
CP	21	—	Compensation pin for boost converter control
ENN	10	I	Enable pin for the negative output voltage (0 V: disabled, VIN: enabled)
ENP	8	I	Enable pin for the positive output voltage (0 V: disabled, VIN: enabled)
FBN	16	I	Feedback pin for the negative output voltage divider
FBP	22	I	Feedback pin for the positive output voltage divider
INN	5, 6	I	Inverting converter switch input
INP	1, 24	I	Boost converter switch input.
NC	12, 20	—	Not connected
OUTN	13, 14	O	Inverting converter switch output.
PGND	2, 3	—	Power ground pin
PSN	11	I	Power-save mode enable for inverter stage (0 V: disabled, VIN: enabled)
PSP	9	I	Power-save mode enable for boost converter stage (0 V: disabled, VIN: enabled)
VIN	4	I	Control supply input
VNEG	15	I	Negative output voltage sense input
VPOS	23	I	Positive output voltage sense input
VREF	17	O	Reference output voltage. Bypass this pin with a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
VIN, INN	Input voltage at pins (2)	–0.3	6	V
VPOS	Maximum voltage at pin (2)	–0.3	17	V
VNEG	Minimum voltage at pin (2)	–17	V_{IN} + 0.3	V
	Voltage at pins ENN, ENP, FBP, FBN, CN, CP, PSP, PSN, BSW (2)	–0.3	V_{IN} + 0.3	V
INP	Input voltage at pin (2)	–0.3	17	V
	Differential voltage between pins OUTN to V_{INN} (2)	–0.3	24	V
T_J	Operating virtual junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JEDEC JS-002.(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature, unless otherwise noted

		MIN	MAX	UNIT
V_I , V_{IN}, V_{INN}	Application input voltage range, input voltage range at VIN and INN pins	2.7	5.5	V
V_{POS}	Adjustable output voltage range for the boost converter	V_I + 0.5	15	V
V_{NEG}	Adjustable output voltage range for the inverting converter	–15	–2	V
V_{ENN}, V_{ENP}	Enable signals voltage	0	5.5	V
V_{PSN}, V_{PSP}	Power-save mode enable signals voltage	0	5.5	V
T_A	Operating free-air temperature range	–40	85	°C
T_J	Operating junction temperature range	–40	125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS65130x RGE Package (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over the full recommended input voltage range 2.7 V ≤ V_{IN} ≤ 5.5 V and over the temperature range –40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values apply for V_{IN} = 3.6 V and T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE (V_{POS}, V_{NEG})							
V_{POS}	Adjustable output voltage range			V_{IN}+ 0.5 V		15	V
V_{NEG}	Adjustable output voltage range			–15		–2	V
V_{REF}	Reference voltage		I_{REF} = 10 µA	1.2	1.213	1.225	V
I_{FBP}	Positive feedback input bias current		V_{FBP} = V_{REF}		50		nA
I_{FBN}	Negative feedback input bias current		V_{FBN} = 0.1 V_{REF}		50		nA
V_{FBP}	Positive feedback regulation voltage		V_{IN} = 2.7 V to 5.5 V	1.189	1.213	1.237	V
V_{FBN}	Negative feedback regulation voltage		V_{IN} = 2.7 V to 5.5 V	–0.024	0	0.024	V
	Total Output DC accuracy				3%		
$r_{DS(ON)(N)}$	Inverter switch ON-resistance		V_{IN} = 3.6 V		440	620	mΩ
			V_{IN} = 5 V		330	530	
I_{LIMN}	TPS65130 Inverter switch current limit		2.7 V < V_{IN} < 5.5 V	700	800	900	mA
I_{LIMN}	TPS65131 Inverter switch current limit		V_{IN} = 3.6 V	1800	1950	2200	mA
$r_{DS(ON)(P)}$	Boost switch ON-resistance		V_{POS} = 5 V		230	300	mΩ
			V_{POS} = 10 V		170	200	
I_{LIMP}	TPS65130 Boost switch current limit		2.7 V < V_{IN} < 5.5 V, V_{POS} = 8 V	700	800	900	mA
I_{LIMP}	TPS65131 Boost switch current limit		V_{IN} = 3.6 V, V_{POS} = 8 V	1800	1950	2200	mA
CONTROL STAGE							
V_{IH}	High level input voltage, ENP, ENN, PSP, PSN			1.4			V
V_{IL}	Low level input voltage, ENP, ENN, PSP, PSN					0.4	V
I_{IN}	Input current, ENP, ENN, PSP, PSN		ENP, ENN, PSP, PSN = GND or V_{IN}		0.01	0.1	µA
R_{BSW}	Output resistance				27		kΩ
V_{IN}	Input voltage range			2.7		5.5	V
I_Q	Quiescent current	VIN	V_{IN} = 3.6 V, I_{POS} = I_{NEG} = 0, ENP = ENN = PSP = PSN = V_{IN}, V_{POS} = 8 V, V_{NEG} = –5 V		300	500	µA
		VPOS			100	120	µA
		VNEG			100	120	µA
I_{SD}	Shutdown supply current		ENN = ENP = GND		0.2	1.5	µA
V_{UVLO}	Undervoltage lockout threshold			2.1	2.35	2.7	V

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over the full recommended input voltage range 2.7 V ≤ V_{IN} ≤ 5.5 V and over the temperature range –40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values apply for V_{IN} = 3.6 V and T_J = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown			150		°C
Thermal shutdown hysteresis	Junction temperature decreasing		5		°C

6.6 Switching Characteristics

over the full recommended input voltage range 2.7 V ≤ V_{IN} ≤ 5.5 V and over the temperature range –40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values apply for V_{IN} = 3.6 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY						
f_S	Oscillator frequency		1250	1380	1500	kHz
DUTY CYCLE						
D_{MAXP}	Maximum duty cycle boost converter			87.5%		
D_{MAXN}	Maximum duty cycle inverting converter			87.5%		
D_{MINP}	Minimum duty cycle boost converter			12.5%		
D_{MINN}	Minimum duty cycle inverting converter			12.5%		

6.7 Typical Characteristics

At 25°C, unless otherwise noted.

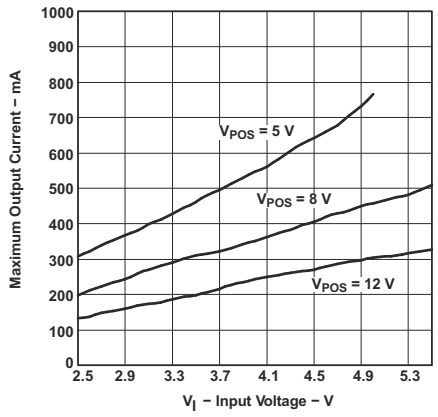


図 6-1. TPS65130 Maximum Output Current (V_{POS}) vs Input Voltage

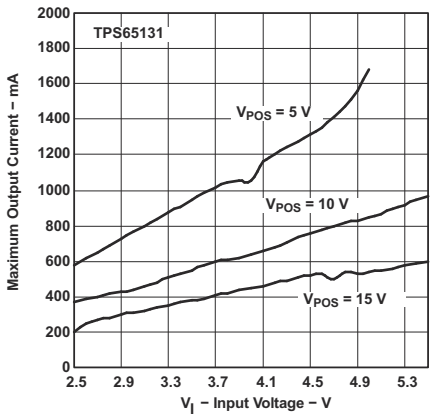


図 6-2. TPS65131 Maximum Output Current (V_{POS}) vs input Voltage

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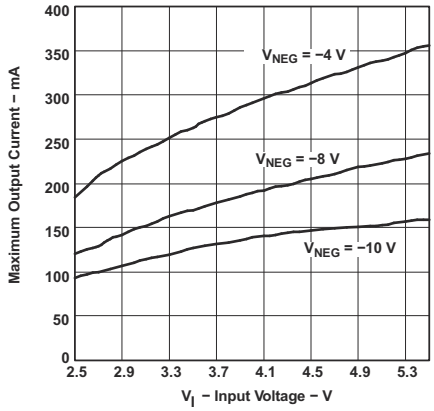


図 6-3. TPS65130 Maximum Output Current (V_{NEG}) vs Input Voltage

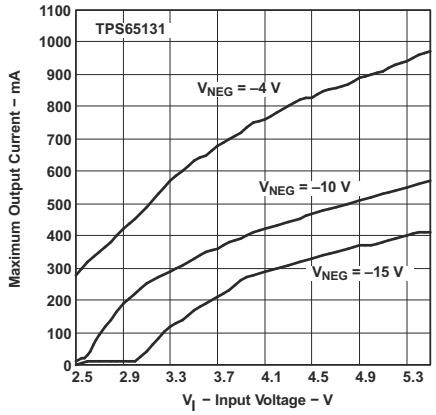


図 6-4. TPS65131 Maximum Output Current (V_{NEG}) vs Input Voltage

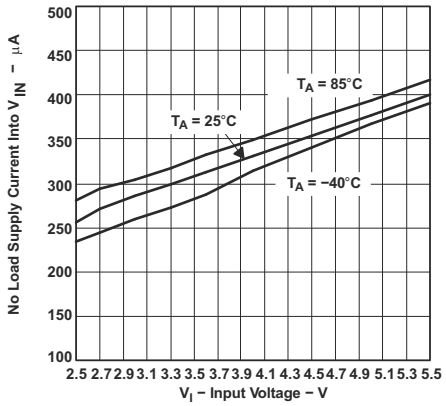


図 6-5. No Load Supply Current into V_{IN} vs Input Voltage

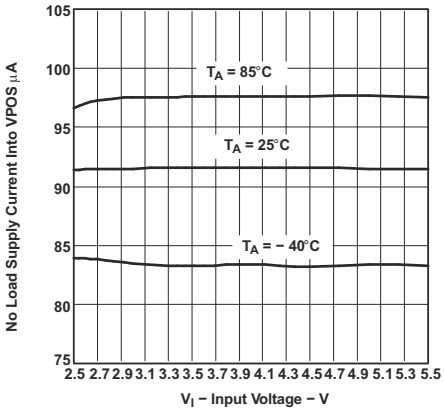


図 6-6. No Load Supply Current into V_{POS} vs Input Voltage

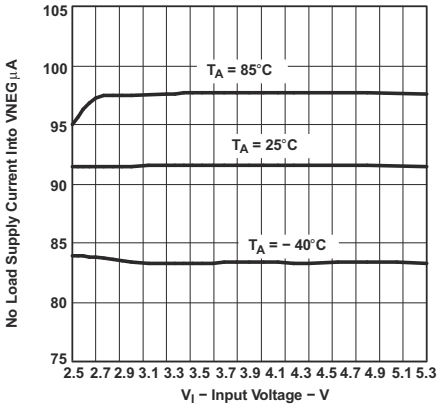


図 6-7. No Load Supply Current into V_{NEG} vs Input Voltage

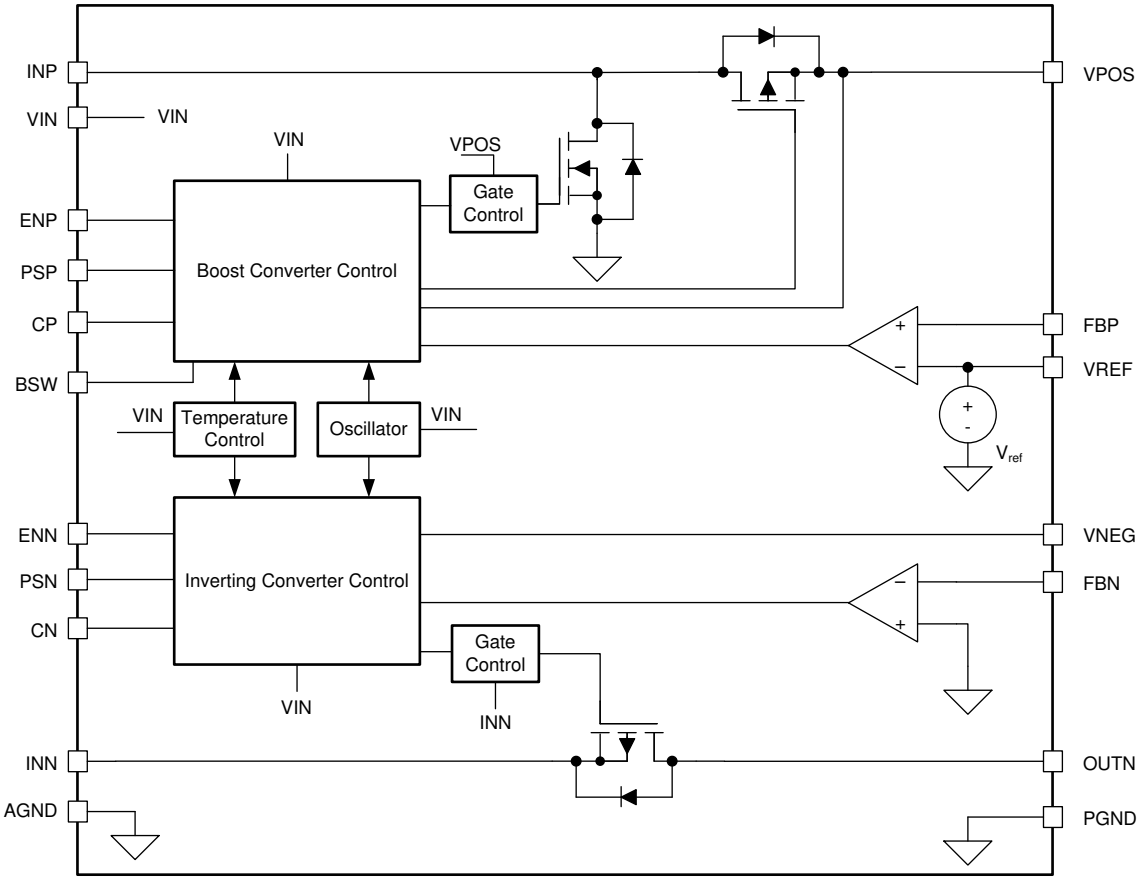
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7 Detailed Description

7.1 Overview

The TPS65130/1 operates with an input voltage range of 2.7 V to 5.5 V and can generate both a positive and negative output. Both converters work independently of each other. They only share a common clock and a common voltage reference. Both outputs are separately controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. In general, each converter operates at continuous conduction mode (CCM). At light loads, the negative converter can enter discontinuous conduction mode (DCM). As the load current decreases, the converters can enter a power-save mode if enabled. This works independently at both converters. Output voltages can go up to 15 V at the boost output and down to –15 V at the inverter output.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Power Conversion

Both converters operate in a fixed-frequency, PWM control scheme. So, the ON-time of the switches varies depending on input-to-output voltage ratio and the load. During this ON-time, the inductors connected to the converters charge with current. In the remaining time, the time period set by the fixed operating frequency, the inductors discharge into the output capacitors through the rectifier diodes. Usually at greater loads, the inductor currents are continuous. At lighter loads, the boost converter uses an additional internal switch to allow current flowing back to the input. This avoids inductor current becoming discontinuous in the boost converter. So, the boost converter is always controlled in a continuous current mode. At the inverting converter, during light loads, the inductor current can become discontinuous. In this case, the control circuit of the inverting controller output automatically takes care of these changing conditions to always operate with an optimum control setup.

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7.3.2 Control

The controller circuits of both converters employ a fixed-frequency, multiple-feedforward controller topology. The circuits monitor input voltage, output voltage, and voltage drop across the switches. Changes in the operating conditions of the converters directly affect the duty cycle and must not take the indirect and slow way through the output voltage control loops. Measurement errors in this feedforward system are corrected by a self-learning control system. An external capacitor damps the output to avoid output-voltage steps due to output changes of this selflearning control system.

The voltage loops, determined by the error amplifiers, must only handle small signal errors. The error amplifiers feature internal compensation. Their inputs are the feedback voltages on the FBP and FBN pins. The device uses a comparison of these voltages with the internal reference voltage to generate an accurate and stable output voltage.

7.3.3 Enable

Both converters can be enabled or disabled individually. Applying a logic HIGH signal at the enable pins (ENP for the boost converter, ENN for the inverting converter) enables the corresponding output. After enabling, internal circuitry necessary to operate the specific converter turns on followed by the soft-start period.

Applying a low signal at the enable ENP or ENN pin shuts down the corresponding converter. When both enable pins are low, the device enters shutdown mode, where all internal circuitry turns off. At this point, the device consumes shutdown current flowing into the VIN pin. The output loads of the converters can be disconnected from the input, see *セクション 7.3.4*.

7.3.4 Load Disconnect

The device supports completely disconnecting the load when the converters are disabled. For the inverting converter, the device turns off the internal PMOS switch. If the inverting converter is turned off, no DC current path remains which could discharge the battery or supply.

This is different for the boost converter. The external rectifying diode, together with the boost inductor, form a DC current path which could discharge the battery or supply if any load connects to the output. The device has no internal switch to prevent current from flowing. For this reason, the device offers a PMOS gate control output (BSW) to enable and disable a PMOS switch in this DC current path, ideally directly between the boost inductor and battery. To be able to fully disconnect the battery, the forward direction of the parasitic backgate diode of this switch must point to the battery or supply. The external PMOS switch, which connects to BSW, turns on when the boost converter is enabled and turns off when the boost converter is disabled.

7.3.5 Soft-Start

Both converters have implemented soft-start functions. When each converter is enabled, the implemented switch current limit ramps up slowly to its nominal programmed value in about 1 ms. Soft-start is implemented to limit the input current during start-up to avoid high peak currents at the battery which could interfere with other systems connected to the same battery. Without soft-start, the high input peak current could trigger the implemented switch current limit, which can lead to a significant voltage drops across the series resistance of the battery and its connections.

7.3.6 Overvoltage Protection

Both converters (boost and inverter) have implemented individual overvoltage protection. If the feedback voltage under normal operation exceeds the nominal value by typically 5%, the corresponding converter shuts down immediately to protect any connected circuitry from possible damage.

7.3.7 Undervoltage Lockout

An undervoltage lockout (UVLO) prevents the device from starting up and operating if the supply voltage at the VIN pin is lower than the undervoltage lockout threshold. For this case, the device automatically shuts down both converters when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown.

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7.3.8 Overtemperature Shutdown

The device automatically shuts down both converters if the implemented internal temperature sensor detects a chip temperature above the thermal shutdown temperature. It automatically starts operating again when the chip temperature falls below this thermal shutdown temperature. The built-in hysteresis avoids undefined operation caused by ringing from shutdown and prevents operating at a temperature close to the overtemperature shutdown threshold.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The power-save mode can improve efficiency at light loads. In power-save mode, the converter only operates when the output voltage falls below the threshold voltage that is internally set by the device. The converter ramps up the output voltage with one or several operating pulses and goes again into power-save mode once the inductor current becomes discontinuous.

The PSN and PSP logic level selects between power-save mode and continuous-conduction mode. If the specific pins (PSP for the boost converter, PSN for the inverting converter) are HIGH, the power-save mode for the corresponding converter operates at light loads. Similarly, a LOW on the PSP pin or PSN pin disables the power-save mode for the corresponding converter.

7.4.2 Full Operation with V_{IN} > 2.7 V

The recommended minimum input supply voltage for the TPS65130/1 device is 2.7 V. Above this voltage, the device achieves the performance described in this data sheet.

7.4.3 Limited Operation with V_{UVLO} < V_{IN} < 2.7 V

With input supply voltages between V_{UVLO} and 2.7 V, the device continues to operate. No functions are disabled, but full performance is not ensured.

7.4.4 No Operation with V_{IN} < V_{UVLO}

The TPS6513x enters an undervoltage lockout condition when the input supply voltage is below the UVLO threshold. In this mode, all device functions are disabled, and the input supply current consumption is minimized. See also セクション 7.3.7.

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8 Applications and Implementation

Note

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8.1 Application Information

The TPS6513x boost converter output voltage, V_{POS}, and the inverting converter output voltage, V_{NEG}, require external components to set the required output voltages. The valid output voltage ranges are as shown in *Recommended Operating Conditions*. The following sections show a typical application example with different output voltage settings and guidance for external component choices.

8.2 Typical Application

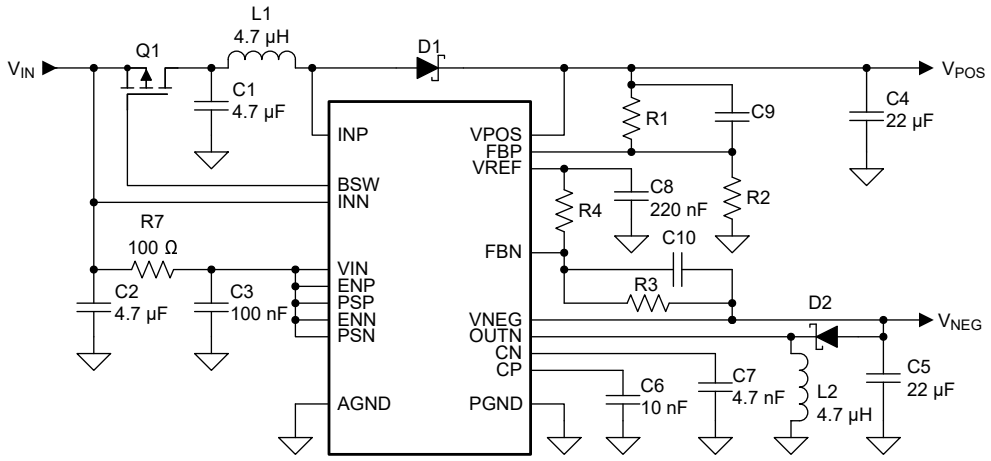


図 8-1. Typical Application

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8.2.1 Design Requirements

図 8-1 uses the following parameters:

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE	
Input voltage range	2.7 V to 5.5 V	
Boost converter output voltage, V_{POS}	R1 = 1 MΩ R2 = 130kΩ C9 = 6.8 pF	10.5 V
Inverting converter output voltage, V_{NEG}	R3 = 1 MΩ R4 = 121.2 kΩ C10 = 7.5 pF	–10 V

表 8-2. List of Components

REFERENCE	SETUP	VALUE, DESCRIPTION
C1, C2	—	4.7 µF, ceramic, 6.3 V, X5R
C3		0.1 µF, ceramic, 10 V, X5R
C4, C5		4 x 4.7 µF, ceramic, 25 V, X7R
C6		10 nF, ceramic, 16 V, X7R
C7		4.7 nF, 50 V, C0G
C8		220 nF, ceramic, 6.3 V, X5R
R1	V_{POS} = 10.5 V	1 MΩ
	V_{POS} = 15 V	975 kΩ
R2	V_{POS} = 10.5 V	130 kΩ
	V_{POS} = 15 V	85.8 kΩ
R3	V_{NEG} = –10 V	1 MΩ
	V_{NEG} = –15 V	1.3 MΩ
R4	V_{NEG} = –10 V	121.2 kΩ
	V_{NEG} = –15 V	104.8 kΩ
R7	—	100 Ω
D1, D2		Schottky, 1 A, 20 V, Onsemi MBRM120
L1, L2		Wurth Elektronik 7447789004 (TPS65130), EPCOS B82462-G4472 (TPS65131)
Q1		MOSFET, P-channel, 12 V, 4 A, Vishay Si2323DS

8.2.2 Detailed Design Procedure

The TPS65130/1 DC-DC converter is intended for systems typically powered by a single-cell Li-ion or Li-polymer battery with a terminal voltage from 2.7 V up to 4.2 V. Because the recommended input voltage goes up to 5.5 V, the device is also suitable for 3-cell alkaline, NiCd, or NiMH batteries, as well as any regulated supply voltages from 2.7 V to 5.5 V. It provides two independent output voltage rails which are programmed as follows.

8.2.2.1 Programming the Output Voltage

8.2.2.1.1 Boost Converter

The output voltage of the TPS65130/1 boost converter stage can be adjusted with an external resistor divider connected to the FBP pin. The typical value of the voltage at the FBP pin is the reference voltage, which is 1.213 V. The maximum recommended output voltage at the boost converter is 15 V. To achieve appropriate accuracy, the current through the feedback divider should be about 100 times greater than the current into the FBP pin. Typical current into the FBP pin is 0.05 µA, and the voltage across R2 is 1.213 V. Based on those values, the recommended value for R2 should be lower than 200 kΩ to set the divider current at 5 µA to 10 µA.

Calculate the value of resistor R1, as a function of the needed output voltage (V_{POS}), with 式 1:

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$$R1 = R2 \times \left(\frac{V_{POS}}{V_{ref}} - 1 \right) \quad (1)$$

In this example, with R2 = 130 kΩ, choose R1 = 1 MΩ to set V_{POS} = 10.5 V.

8.2.2.1.2 Inverting Converter

The output voltage of the inverting converter stage can also be adjusted with an external resistor divider. It must be connected to the FBN pin. Unlike the feedback divider at the boost converter, the reference point of the feedback divider is not GND but V_{REF}. So the typical value of the voltage at the FBN pin is 0 V. The minimum recommended output voltage at the inverting converter is –15 V. Feedback divider current considerations are similar to the considerations at the boost converter. For the same reasons, the feedback divider current should be in the range of 5 µA or greater. The voltage across R4 is 1.213 V. Based on those values, the recommended value for R4 should be lower than 200 kΩ to set the divider current at the required value.

Calculate the value of resistor R3, as a function of the needed output voltage (V_{NEG}), with 式 2:

$$R3 = -R4 \times \left(\frac{V_{NEG}}{V_{ref}} \right) \quad (2)$$

In this example, with R4 = 121.2 kΩ, choose R3 = 1 MΩ to set V_{NEG} = –10 V.

8.2.2.2 Inductor Selection

An inductive converter normally requires two main passive components for storing energy during the conversion. Therefore, each converter requires an inductor and a storage capacitor. In selecting the right inductor, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the switch for the boost converter and for the inverting converters is nominally 800 mA for the TPS65130 device and 1950 mA for TPS65131 device. The highest peak current through the switches and the inductor depend on the output load, the input voltage (V_{IN}), and the output voltages (V_{POS}, V_{NEG}). Use 式 3 to estimate the peak inductor current in the boost converter, I_{L_P}. 式 4 shows the corresponding formula for the inverting converter, I_{L_N}.

$$I_{(L-P)} = \frac{V_{POS}}{V_I \times 0.64} \times I_{POS} \quad (3)$$

$$I_{(L-N)} = \frac{V_I - V_{NEG}}{V_I \times 0.64} \times I_{NEG} \quad (4)$$

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the losses in the inductor, as well as output voltage ripple and EMI. But in the same way, output voltage regulation gets slower, causing greater voltage changes at fast load changes. In addition, a larger inductor usually increases the total system cost. Keep those parameters in mind and calculate the possible inductor value with 式 5 for the boost converter and 式 6 for the inverting converter.

$$L1 = \frac{V_I \times (V_{POS} - V_I)}{\Delta I_{(L-P)} \times f \times V_{POS}} \quad (5)$$

$$L2 = \frac{V_I \times V_{NEG}}{\Delta I_{(L-N)} \times f \times (V_{NEG} - V_I)} \quad (6)$$

Parameter f is the switching frequency. For the boost converter, ΔI_{L-P} is the ripple current in the inductor, that is, 20% of I_{L-P}. Accordingly, for the inverting converter, ΔI_{L-N} is the ripple current in the inductor, that is, 20% of I_{L-N}.

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V_I is the input voltage, which is 3.3 V in this example. So, the calculated inductance value for the boost inductor is 5.1 µH and for the inverting converter inductor is 5.1 µH. With these calculated values and the calculated currents, it is possible to choose a suitable inductor.

In typical applications, the recommendation is to choose a 4.7-µH inductor. The device is optimized to work with inductance values from 3.3 µH to 6.8 µH. Nevertheless, operation with greater inductance values may be possible in some applications. Perform detailed stability analysis in this case. Be aware of the possibility that load transients and losses in the circuit can lead to higher currents than estimated in 式 3 and 式 4. Also, the losses caused by magnetic hysteresis and conductor resistance are a major parameter for total circuit efficiency.

表 8-3 shows inductors from different suppliers used with the TPS65130/1 converter:

表 8-3. List of Inductors

VENDOR(1)	INDUCTOR SERIES
EPCOS	B8246284-G4
Wurth Elektronik	7447789XXX
	744031XXX
TDK	VLF3010
	VLF4012
Cooper Electronics Technologies	SD12

(1) See Third-party Products Disclaimer

8.2.2.3 Capacitor Selection

8.2.2.3.1 Input Capacitor

As a recommendation, choose an input capacitors of at least 4.7 µF for the input of the boost converter (INP) and accordingly for the input of the inverting converter (INN). This improves transient behavior of the regulators and EMI behavior of the total power-supply circuit. Choose a ceramic capacitor or a tantalum capacitor. For the use of a tantalum capacitor, an additional, smaller ceramic capacitor (100 nF) in parallel is required. Place the input capacitor(s) close to the input pins..

8.2.2.3.2 Output Capacitors

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero. Use 式 7 for the boost converter output capacitor (C4min) and 式 8 for the inverting converter output capacitor (C5min).

$$C4\,min = \frac{I_{POS} \times (V_{POS} - V_I)}{f \times \Delta V_{POS} \times V_{POS}} \tag{7}$$

$$C5\,min = \frac{I_{NEG} \times V_{NEG}}{f \times \Delta V_{NEG} \times (V_{NEG} - V_I)} \tag{8}$$

The parameter f is the switching frequency. ΔV_{POS} and ΔV_{NEG} are the maximum allowed ripple voltages for each converter. Choosing a ripple voltage in the range of 10 mV requires a minimum capacitance of 12 µF. The total ripple is larger due to the ESR of the output capacitor. Use 式 9 for he boost converter and 式 10 for the inverting converter to calculate this additional ripple component.

$$\Delta V_{(ESR-P)} = I_{POS} \times R_{(ESR-C4)} \tag{9}$$

$$\Delta V_{(ESR-N)} = I_{NEG} \times R_{(ESR-C5)} \tag{10}$$

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In this example, an additional ripple of 2 mV is the result of using a typical ceramic capacitor with an ESR in the 10-mΩ range. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 10 mV.

Load transients can create additional ripple. When the load current increases rapidly, the output capacitor must provide the additional current until the inductor current increases by the control loop which sets a higher ON-time (duty cycle) of the main switch. The higher duty cycle results in longer inductor charging periods. The inductance itself also limits the rate of increase of the inductor current. When the load current decreases rapidly, the output capacitor must store the excess energy (stored in the inductor) until the regulator has decreased the inductor current by reducing the duty cycle. TI recommends using greater capacitance values, as the foregoing calculations show.

8.2.2.4 Rectifier Diode Selection

Both converters (the boost and inverting converter) require rectifier diodes, D1 and D2. As a recommendation, to reduce losses, use Schottky diodes. The forward current rating needed is equal to the maximum output current. Consider that the maximum currents, I_{POS}max and I_{NEG}max, might differ for V_{POS} and V_{NEG} when choosing the diodes.

8.2.2.5 External PMOS Selection

During shutdown, when connected to a power supply, a path from the power supply to the positive output conducts through the inductor and an external diode. Optionally, to fully disconnect the positive output V_{POS} during shutdown, add an external PMOS (Q1). The BSW pin controls the gate of the PMOS. When choosing a proper PMOS, the V_{GS} and V_{GD} voltage ratings must cover the input voltage range, the drain current rating must not be lower than the maximum input current flowing into the application, and conditions of the PMOS operating area must fit.

If there is no intention to use an external PMOS, leave the BSW pin floating.

8.2.2.6 Stabilizing the Control Loop

8.2.2.6.1 Feedforward Capacitor

As a recommendation, to speed up the control loop, place feedforward capacitors in the feedback divider, parallel to R1 (boost converter) and R3 (inverting converter). 式 11 shows how to calculate the appropriate value for the boost converter, and 式 12 for the inverting converter.

$$C9 = \frac{6.8\ \mu s}{R1} \tag{11}$$

$$C10 = \frac{7.5\ \mu s}{R3} \tag{12}$$

To avoid coupling noise into the control loop from the feedforward capacitors, the feedforward effect can be bandwidth-limited by adding a series resistor. Any value from 10 kΩ to 100 kΩ is suitable. The greater the resistance, the lower the noise coupled into the control loop system.

8.2.2.6.2 Compensation Capacitors

The device features completely internally compensated control loops for both converters. The internal feedforward system has built-in error correction which requires external capacitors. As a recommendation, use a 10-nF capacitor at the CP pin of the boost converter and a 4.7-nF capacitor at the CN pin of the inverting converter.

8.2.3 Analog Supply Filter

To ensure a noise free voltage supply of the IC, it is recommended to add an RC or LC filter between INN and VIN pins.

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8.2.3.1 RC-Filter

For most applications an RC filter can be used with a resistance value of 100 Ω minimum and capacitor value of 0.1 µF as in the application example 図 8-1.

8.2.3.2 LC-Filter

For applications where input voltages V_I with a fast rising edge (slew rate ≥ 275 mV/µs) are expected, it is recommended to replace the resistor R7 with a ferrite bead to minimize the delay between the signals on the INN pin and VIN pin. Select a ferrite bead with the lowest possible DCR and a proper current rating, such as BLM18KG101TN1 for example. A conservative approach for the current rating specification is to set it at 1.5 times or twice the maximum input current.

表 8-4. List of Ferrite Beads

VENDOR	FERRITE BEAD SERIES
Murata	BLMxKG

8.2.4 Application Curves

表 8-5. Table of Figures

FIGURE	DESCRIPTION
図 8-2	TPS65130 efficiency versus output current, V_{POS}= 5 V
図 8-3	TPS65131 efficiency versus output current, V_{POS}= 5 V
図 8-4	TPS65130 efficiency versus output current, V_{POS}= 8 V
図 8-5	TPS65131 efficiency versus output current, V_{POS}= 10 V
図 8-6	TPS65130 efficiency versus output current, V_{POS}= 12 V
図 8-7	TPS65131 efficiency versus output current, V_{POS}= 15 V
図 8-8	TPS65130 efficiency versus output current, V_{NEG}= –4 V, (V_{IN} = 4 V, 3 V)
図 8-9	TPS65131 efficiency versus output current, V_{NEG}= –4 V, (V_{IN} = 5 V, 3 V)
図 8-10	TPS65130 efficiency versus output current, V_{NEG}= –8 V, (V_{IN} = 4.2 V, 3 V)
図 8-11	TPS65131 efficiency versus output current, V_{NEG}= –10 V, (V_{IN} = 5 V, 3 V)
図 8-12	TPS65130 efficiency versus output current, V_{NEG}= –10 V, (V_{IN} = 4.2 V, 3 V)
図 8-13	TPS65131 efficiency versus output current, V_{NEG}= –15 V, (V_{IN} = 5 V, 3 V)
図 8-14	TPS65130 efficiency versus input voltage, V_{POS}= 5 V in power-save mode
図 8-15	TPS65130 efficiency versus input voltage, V_{POS}= 8 V in power-save mode
図 8-16	TPS65130 efficiency versus input voltage, V_{POS}= 12 V in power-save mode
図 8-17	TPS65130 efficiency versus input voltage, V_{NEG}= –4 V in power-save mode
図 8-18	TPS65130 efficiency versus input voltage, V_{NEG}= –8 V in power-save mode
図 8-19	TPS65130 efficiency versus input voltage, V_{NEG}= –10 V in power-save mode
図 8-20	TPS65130 efficiency versus output current, V_O= 13.5 V (+9 V, –4.5 V), (V_{IN} = 4.2 V, 3 V)
図 8-21	TPS65131 efficiency versus output current, V_O= 30 V (±15 V, (V_{IN} 5 V, 3 V)
図 8-22	TPS65130 efficiency versus input voltage, V_O= 13.5 V (9 V, –4.5 V) in power save mode
図 8-23	TPS65130 output voltage versus output current, V_{POS}= 5 V, V_{IN} = 3 V
図 8-24	TPS65131 output voltage versus output current, V_{POS}= 5 V, V_{IN} = 4.2 V
図 8-25	TPS65130 output voltage versus output current, V_{POS}= 8 V, V_{IN} = 3 V
図 8-26	TPS65131 output voltage versus output current, V_{POS}= 10 V, V_{IN} = 5 V
図 8-27	TPS65130 output voltage versus output current, V_{POS}= 12 V (V_{IN} = 3 V)
図 8-28	TPS65131 output voltage versus output current, V_{POS}= 15 V (V_{IN} = 5 V)
図 8-29	TPS65130 output voltage versus output current, V_{NEG}= –4 V, V_{IN} = 3 V
図 8-30	TPS65131 output voltage versus output current, V_{NEG}= –4 V, V_{IN} = 5 V

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表 8-5. Table of Figures (continued)

FIGURE	DESCRIPTION
図 8-31	TPS65130 output voltage versus output current, V_{NEG}= –8 V, V_{IN} = 3 V
図 8-32	TPS65131 output voltage versus output current, V_{NEG}= –10 V, V_{IN} = 5 V
図 8-33	TPS65130 output voltage versus output current, V_{NEG}= –10 V, V_{IN} = 3 V
図 8-34	TPS65131 output voltage versus output current, V_{NEG}= –15 V, V_{IN} = 5 V
図 8-35	Positive output voltage in continuous current mode
図 8-36	Negative output voltage in continuous current mode
図 8-37	Positive output voltage at power-save mode disabled
図 8-38	Negative output voltage at power-save mode disabled
図 8-39	Positive output voltage in power-save mode, V_I = 3.6 V, V_{POS} = 5.5 V
図 8-40	Negative output voltage in power-save mode, V_I = 3.6 V, V_{NEG} = –8 V
図 8-41	Load transient response, V_I = 3.6 V, V_{POS} = 8 V
図 8-42	Load transient response, V_I = 3.6 V, V_{NEG} = –8 V
図 8-43	Line transient response, V_I = 3.6 V to 4.2 V, V_{POS} = 8 V
図 8-44	Line transient response, V_I = 3.6 V to 4.2 V, V_{NEG} = –8 V
図 8-45	Start-up after enable, V_{POS} = 8 V, V_I = 3.6 V
図 8-46	Start-up after enable, V_{NEG} = –8 V, V_I = 3.6 V

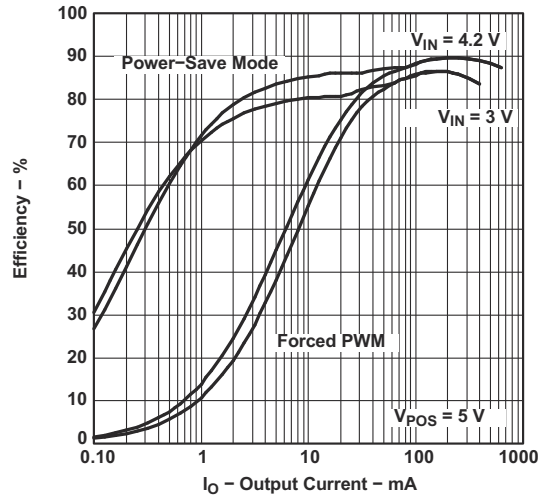


図 8-2. TPS65130 Efficiency vs Output Current

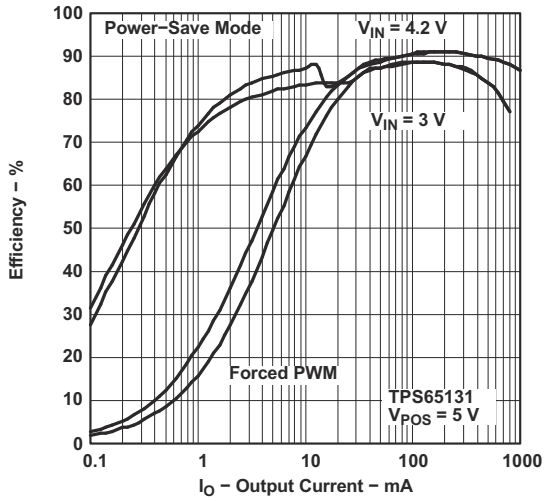


図 8-3. TPS65131 Efficiency vs Output Current

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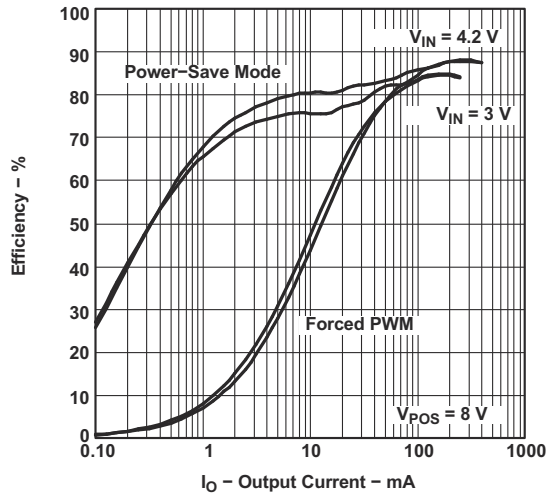


図 8-4. TPS65130 Efficiency vs Output Current

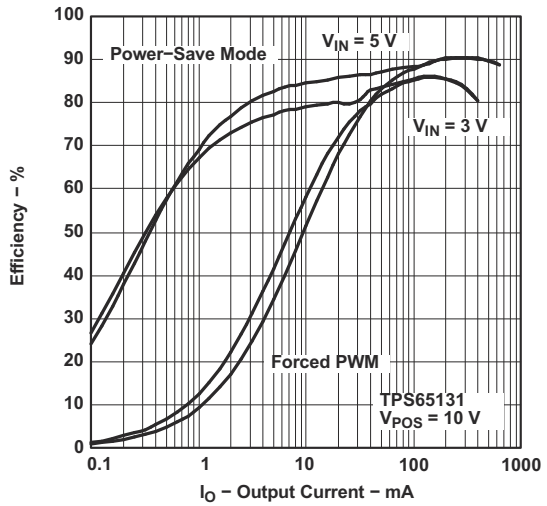


図 8-5. TPS65131 Efficiency vs Output Current

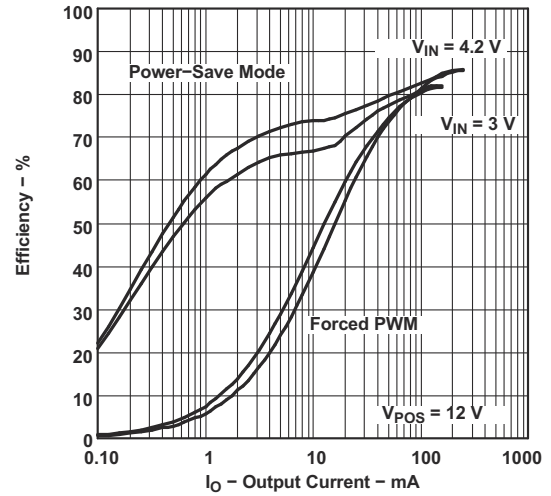


図 8-6. TPS65130 Efficiency vs Output Current

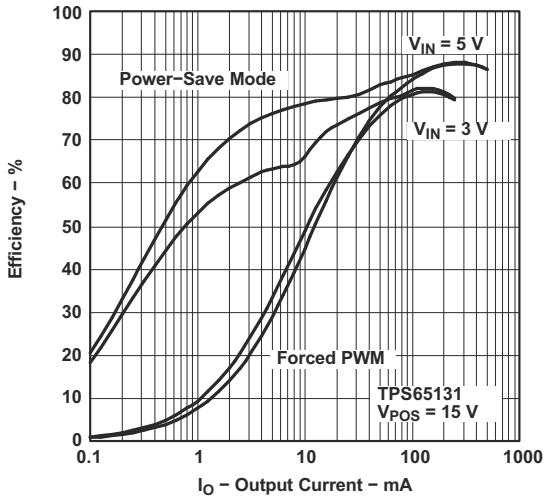


図 8-7. TPS65131 Efficiency vs Output Current

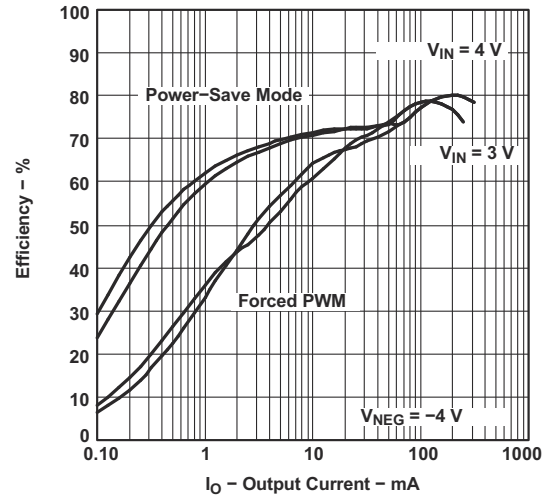


図 8-8. TPS65130 Efficiency vs Output Current

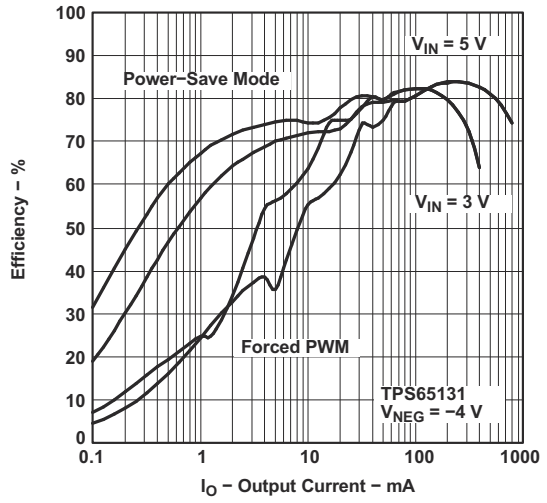


図 8-9. TPS65131 Efficiency vs Output Current

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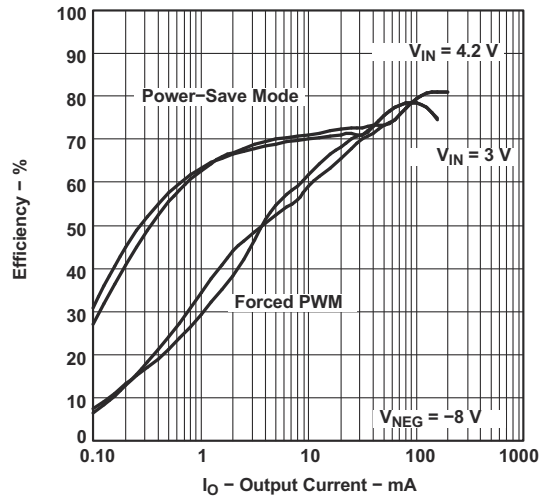


図 8-10. TPS65130 Efficiency vs Output Current

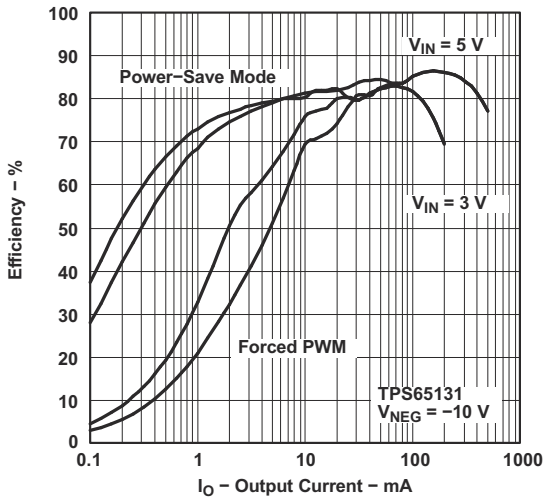


図 8-11. TPS65131 Efficiency vs Output Current

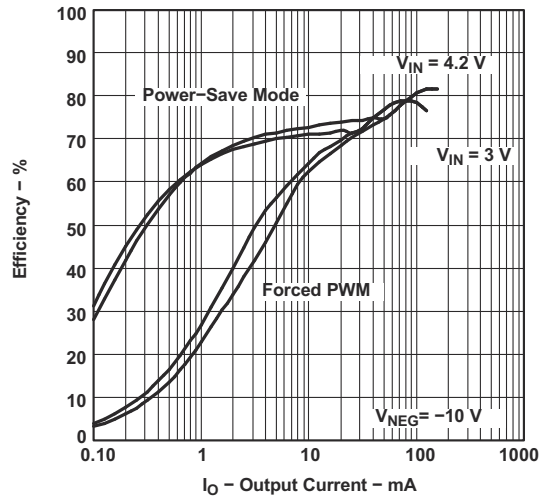


図 8-12. TPS65130 Efficiency vs Output Current

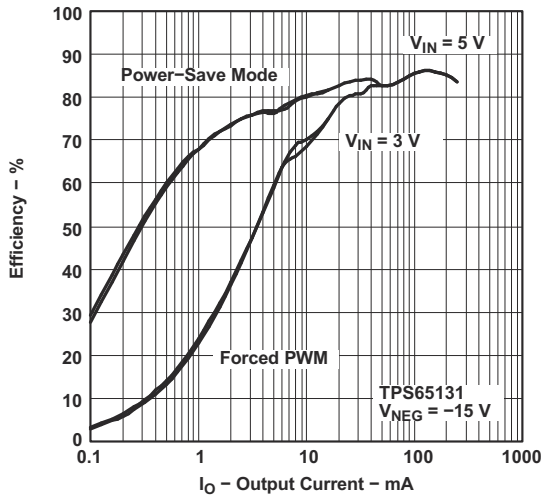


図 8-13. TPS65131 Efficiency vs Output Current

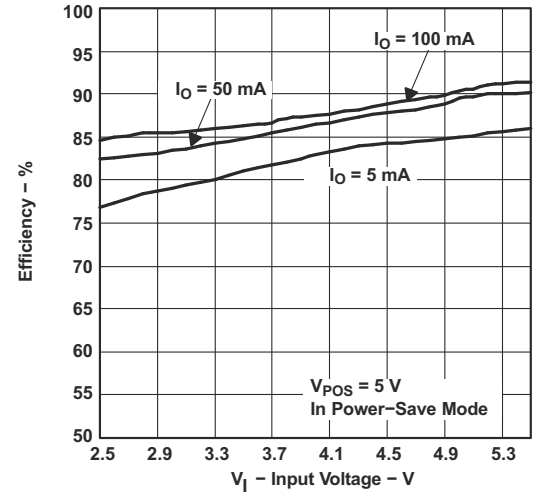


図 8-14. TPS65130 Efficiency vs Input Voltage

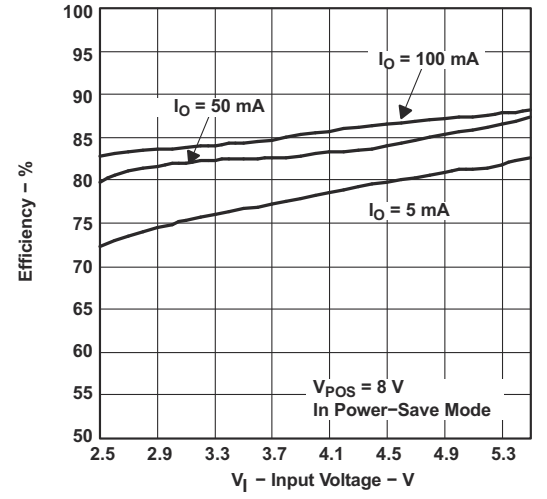


図 8-15. TPS65130 Efficiency vs Input Voltage

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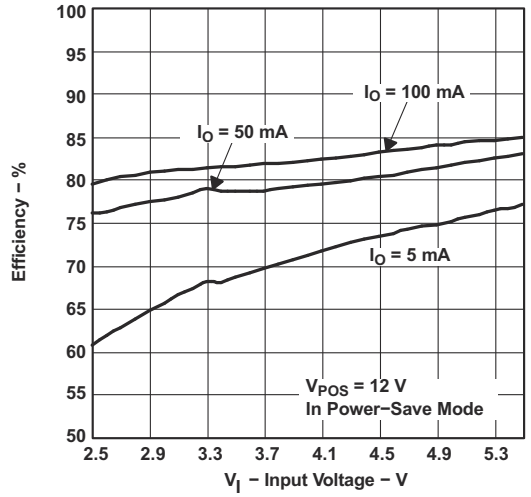


図 8-16. TPS65130 Efficiency vs Input Voltage

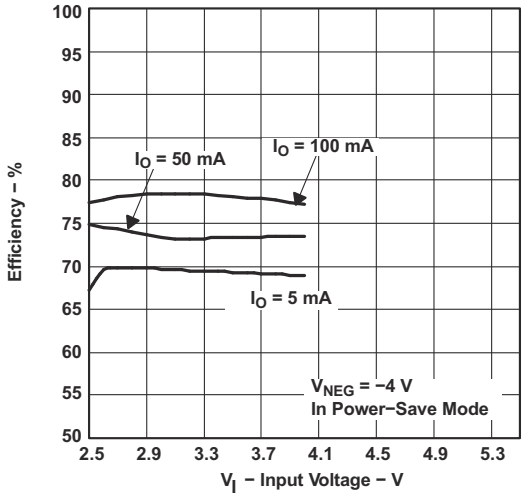


図 8-17. TPS65130 Efficiency vs Input Voltage

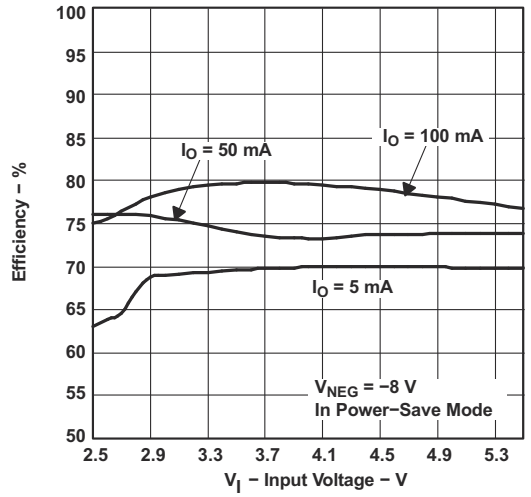


図 8-18. TPS65130 Efficiency vs Input Voltage

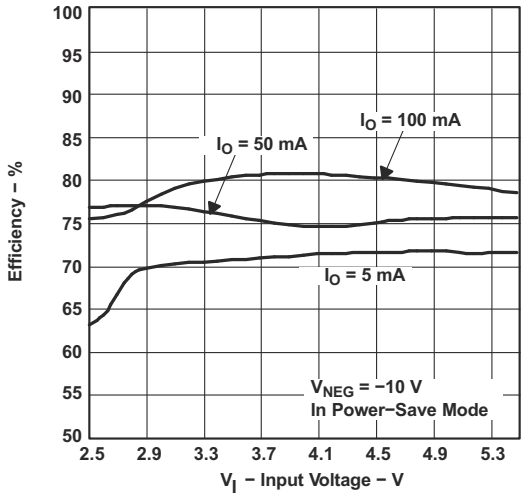


図 8-19. TPS65130 Efficiency vs Input Voltage

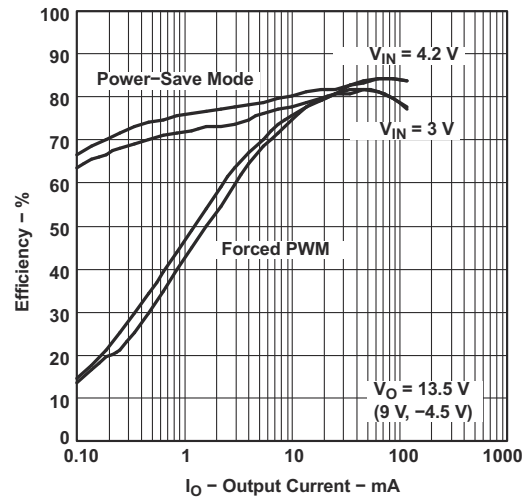


図 8-20. TPS65130 Combined Efficiency vs Output Current

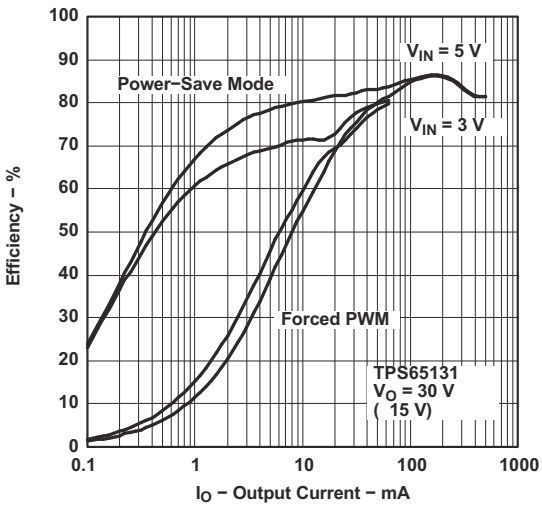


図 8-21. TPS65131 Combined Efficiency vs Output Current

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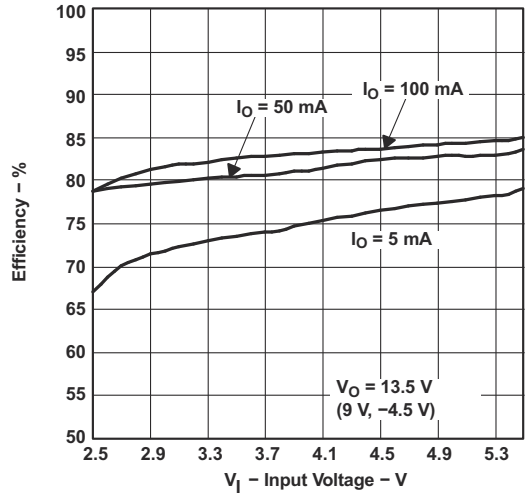


図 8-22. TPS65130 Combined Efficiency vs Input Voltage

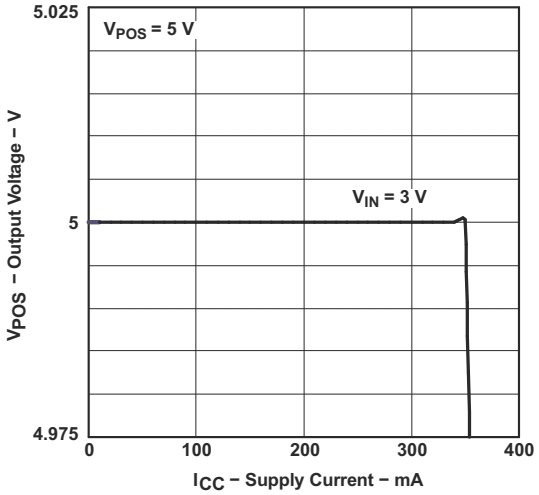


図 8-23. TPS65130 Output Voltage vs Output Current

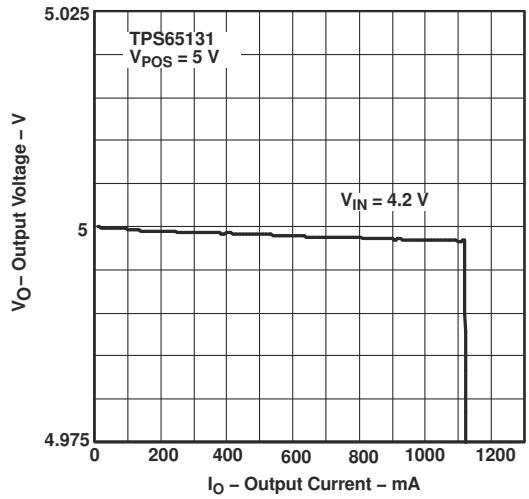


図 8-24. TPS65131 Output Voltage vs Output Current

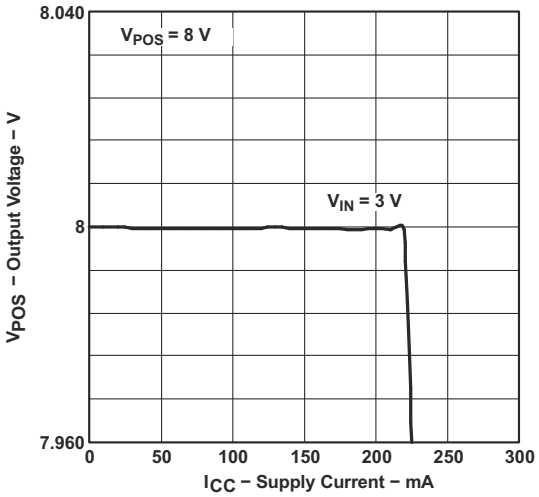


図 8-25. TPS65130 Output Voltage vs Output Current

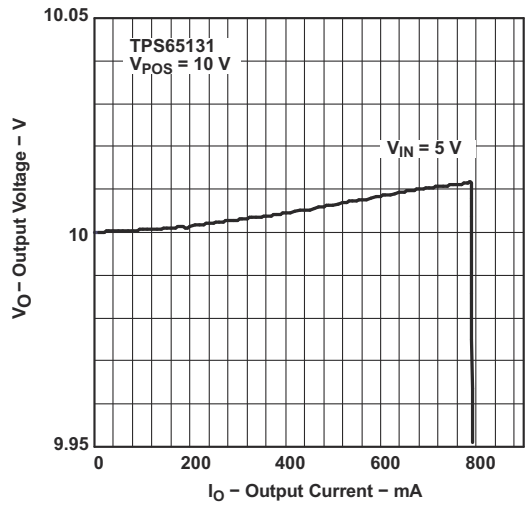


図 8-26. TPS65131 Output Voltage vs Output Current

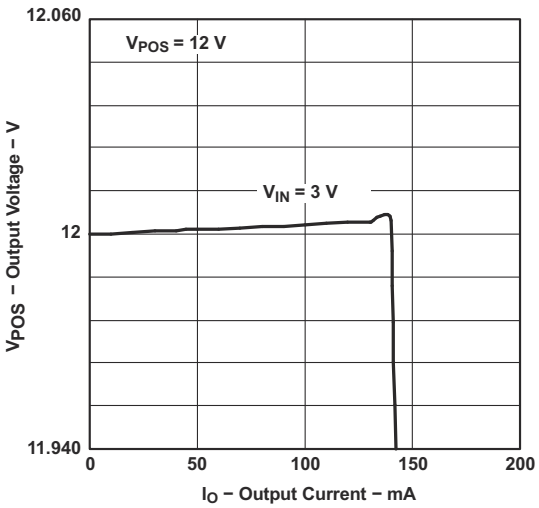


図 8-27. TPS65130 Output Voltage vs Output Current

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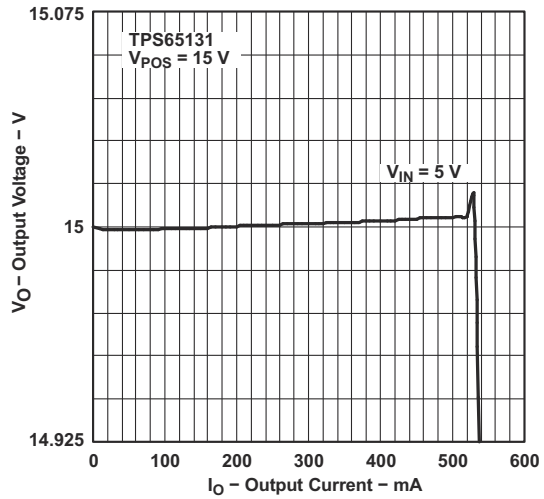


図 8-28. TPS65131 Output Voltage vs Output Current

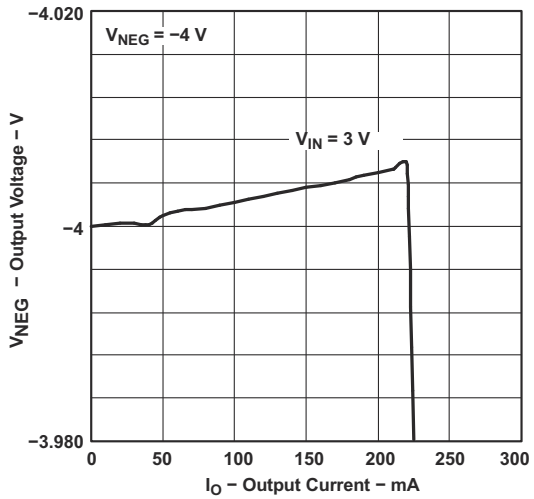


図 8-29. TPS65130 Output Voltage vs Output Current

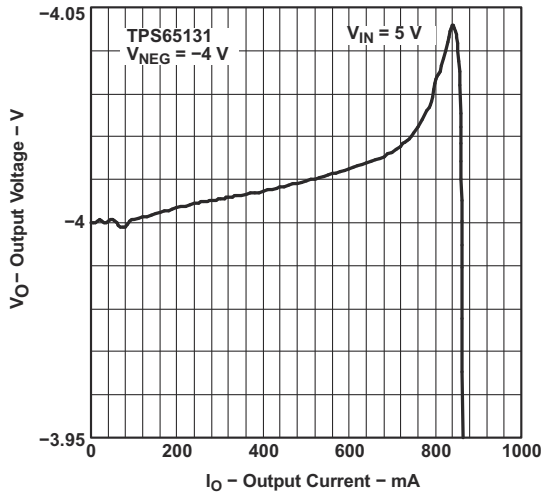


図 8-30. TPS65131 Output Voltage vs Output Current

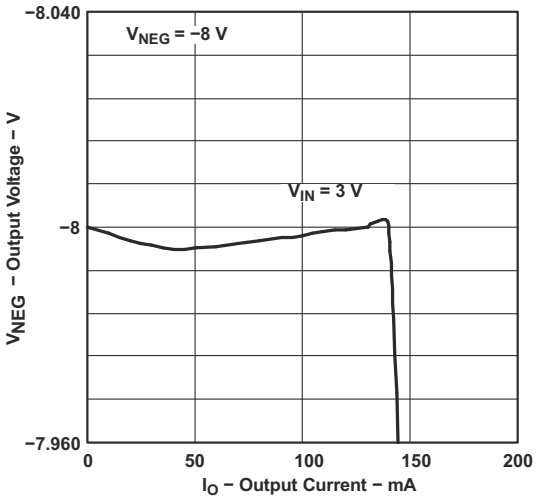


図 8-31. TPS65130 Output Voltage vs Output Current

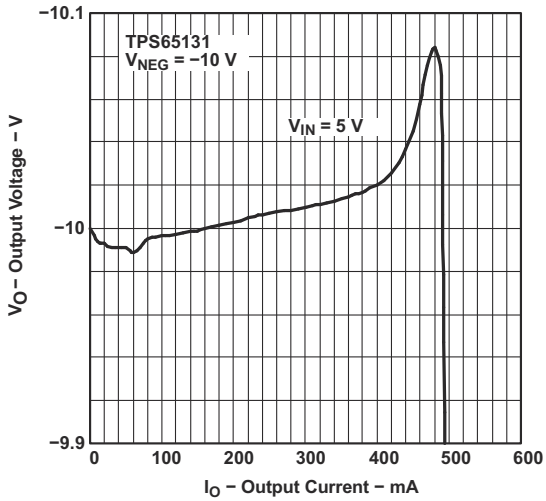


図 8-32. TPS65131 Output Voltage vs Output Current

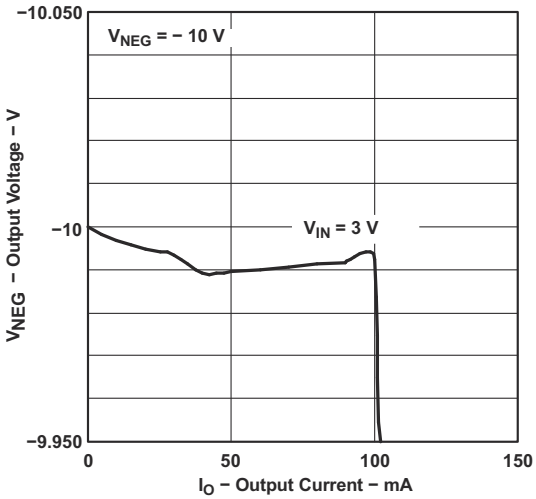


図 8-33. TPS65130 Output Voltage vs Output Current

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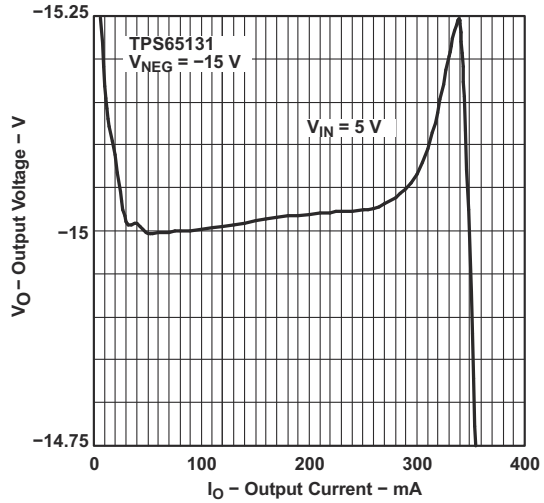


図 8-34. TPS65131 Output Voltage vs Output Current

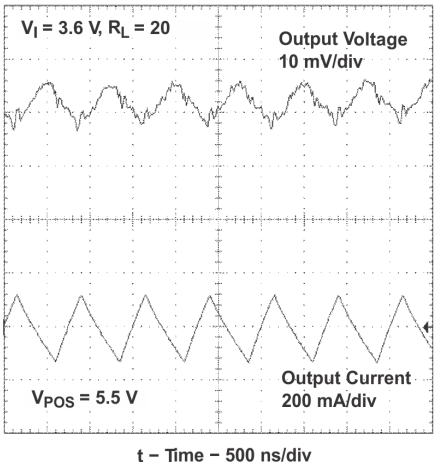


図 8-35. V_{POS} in Continuous Current Mode

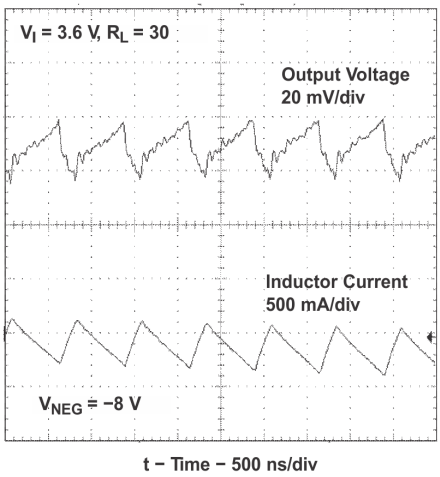


図 8-36. V_{NEG} in Continuous Current Mode

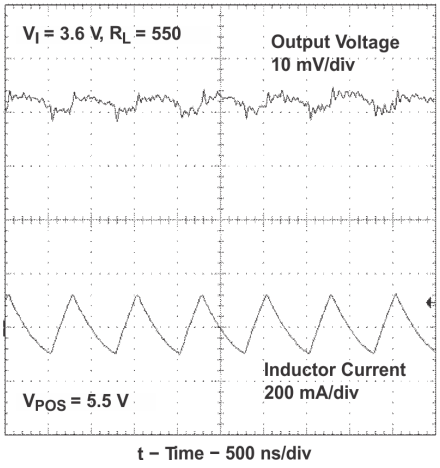


図 8-37. V_{POS} at Power-Save Mode Disabled

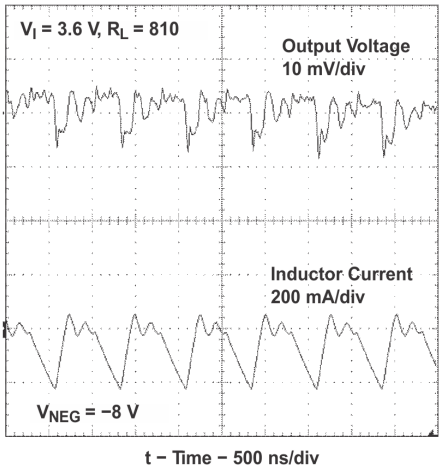


図 8-38. V_{NEG} at Power-Save Mode Disabled

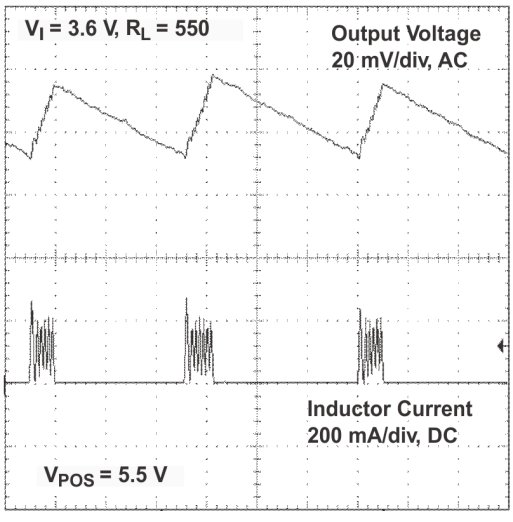


図 8-39. V_{POS} in Power-Save Mode

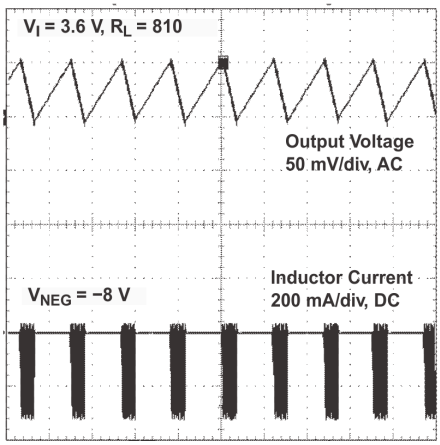


図 8-40. V_{NEG} in Power-Save Mode

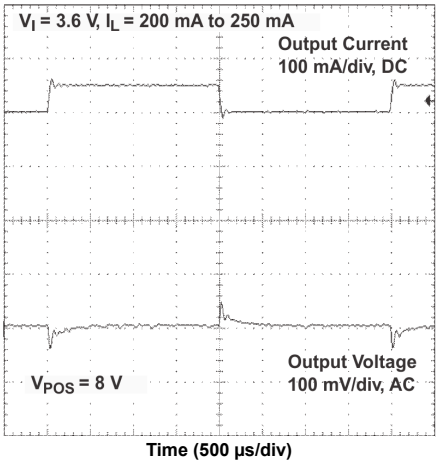


図 8-41. Load Transient Response

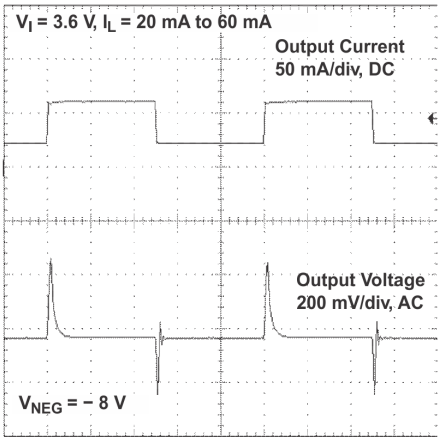


図 8-42. Load Transient Response

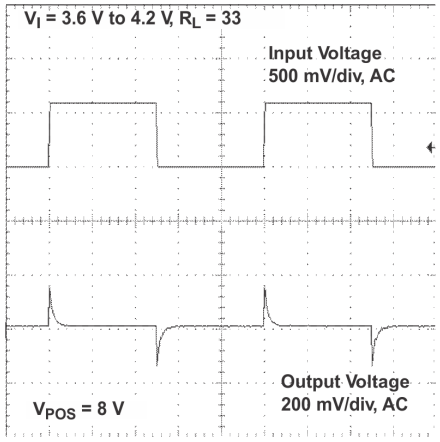


図 8-43. Line Transient Response

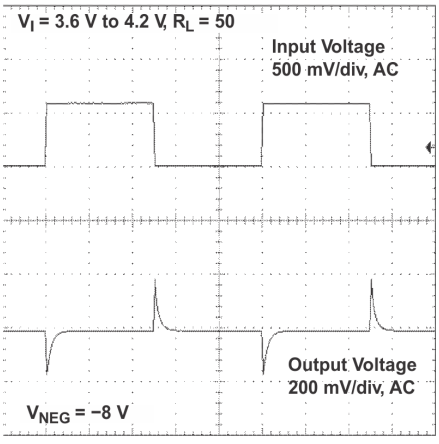


図 8-44. Line Transient Response

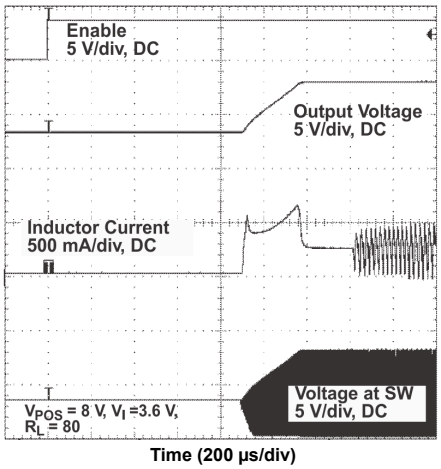


図 8-45. Start-up After Enable

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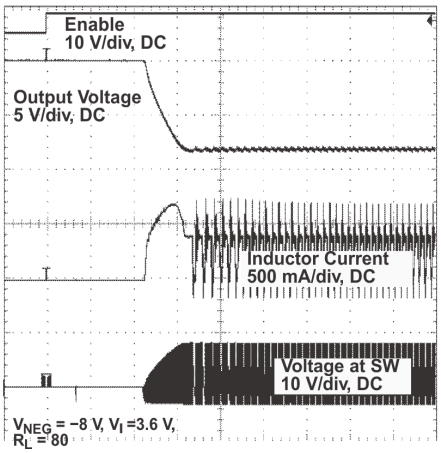


図 8-46. Start-up After Enable

Power Supply Recommendations

The input voltage ranges from 2.7 V to 5.5 V for the TPS6513x. Consequently, the supply can come, for example, from a 3.3-V or 5-V rail. If the device starts into load during the soft-start phase, the drawn input current can be higher than during post-start operation. Consider the application requirements when selecting the power supply. To avoid unintended toggling of the undervoltage lockout protection, connect the TPS6513x device through a low-impedance path to the power supply.

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9 Layout

9.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. Therefore, use wide and short traces for the main current paths and for the power ground tracks. The input capacitors (C1, C2, C3), output capacitors (C4, C5), the inductors (L1, L2), and the rectifying diodes (D1, D2) should be placed as close as possible to the IC to keep parasitic inductances low. Use a wide power ground (PGND) plane. Connect the analog ground pin (AGND) to the PGND plane. Further, connect the PGND plane with the exposed thermal pad. Place the feedback dividers as close as possible to the control pin (boost converter) or the VREF pin (inverting converter) of the IC.

9.2 Layout Example

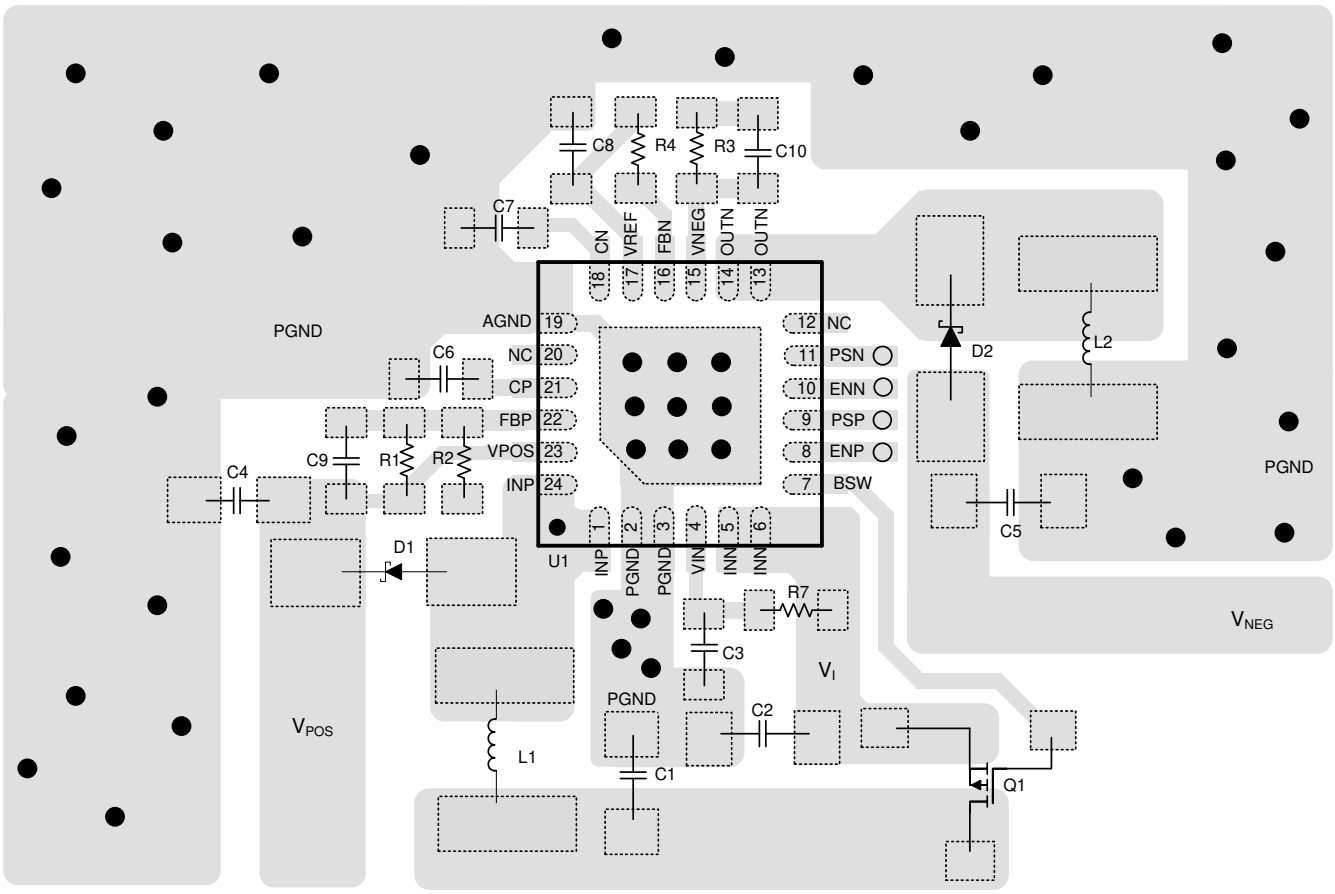


図 9-1. Layout Recommendation (TPS65130 and TPS65131)

9.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heatsinks and convection surfaces, and the presence of heat-generating components affect the power-dissipation limits of a given component.

These three basic approaches enhance thermal performance:

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow to the system.

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The recommended device junction temperature range, T_J, is –40°C to 125°C. The thermal resistance of the 24-pin QFN, 4–mm × 4–mm package (RGE) is $R_{\theta JA}$ = 34.1°C/W. The recommended operating ambient temperature range for the device is T_A = –40°C to 85°C. Use 式 13 to calculate the maximum power dissipation, $P_D$max, as a function of T_A. In this equation, use T_J = 125°C to operate the device within the recommended temperature range, use $T_J = T_{TS}$ to determine the absolute maximum threshold when the device might go into thermal shutdown. If the maximum ambient temperature of the application is lower, more heat dissipation is possible.

$$P_D\,\text{max} = \frac{T_J - T_A}{R_{\theta JA}} \tag{13}$$

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10 Device and Documentation Support

10.1 Device Support

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

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10.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65130RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 5130
TPS65130RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 5130
TPS65130RGET	Obsolete	Production	VQFN (RGE) | 24	-	-	Call TI	Call TI	-40 to 85	TPS6 5130
TPS65131RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 5131
TPS65131RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 5131
TPS65131RGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 5131

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS65131 :

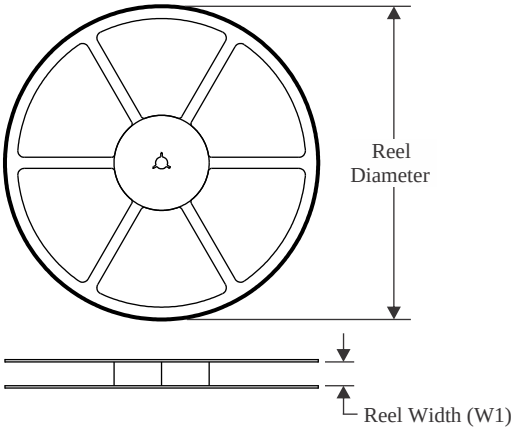
- Automotive : TPS65131-Q1

NOTE: Qualified Version Definitions:

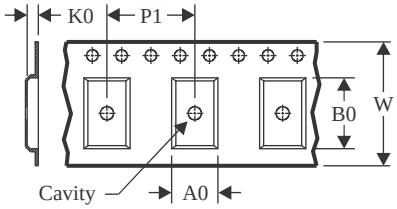
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

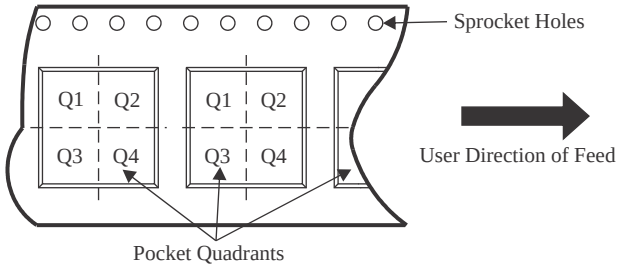


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

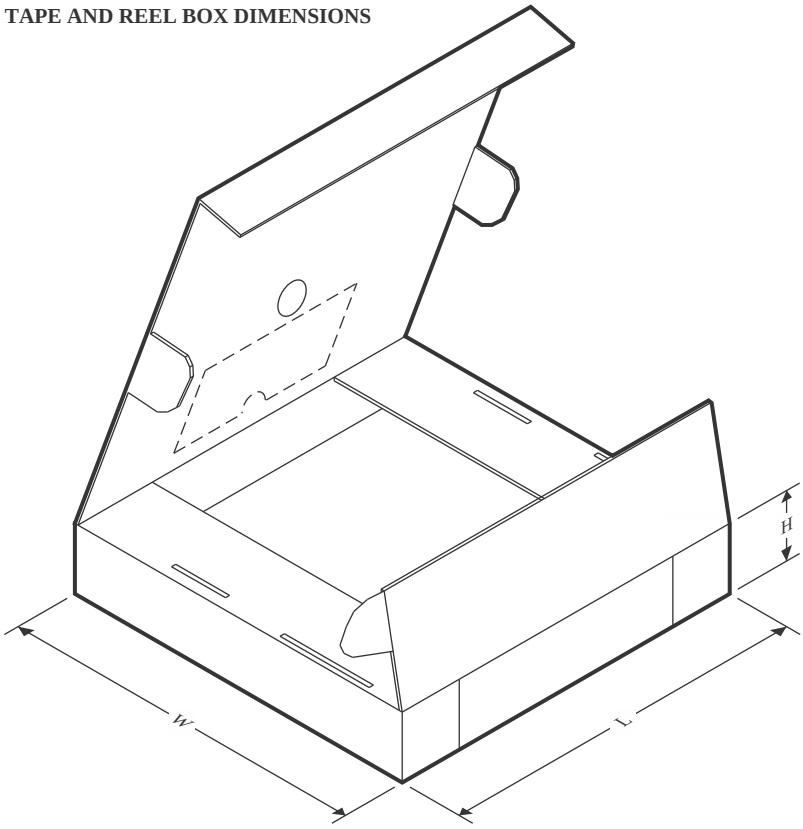
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65130RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65131RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

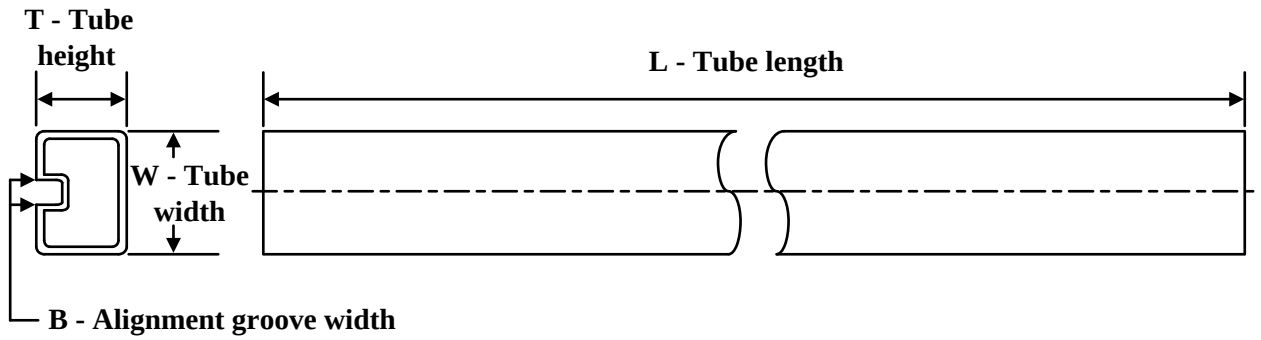
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65130RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS65131RGER	VQFN	RGE	24	3000	552.0	346.0	36.0

TUBE



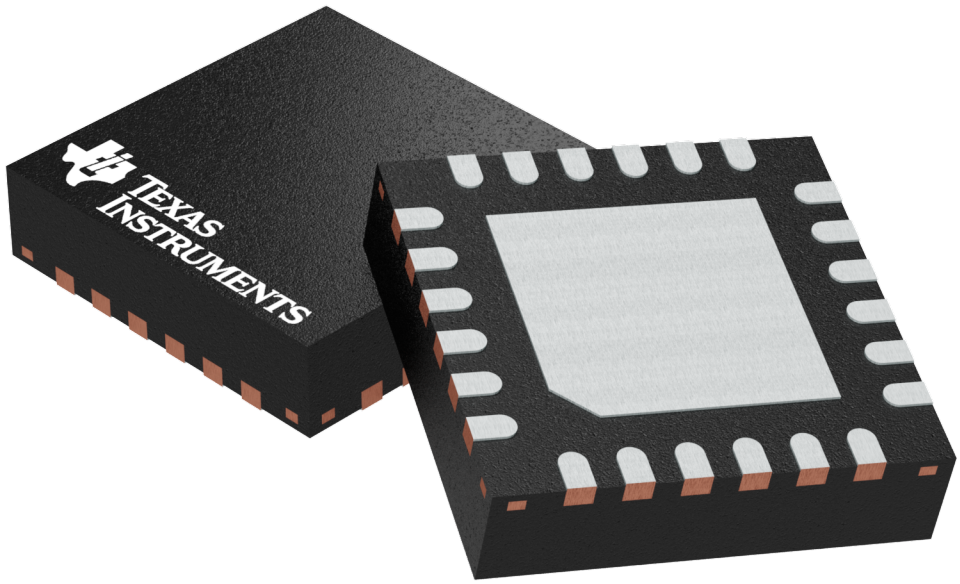
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS65131RGER	RGE	VQFN	24	3000	381	5.79	2286	0
TPS65131RGER.A	RGE	VQFN	24	3000	381	5.79	2286	0
TPS65131RGERG4	RGE	VQFN	24	3000	381	5.79	2286	0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

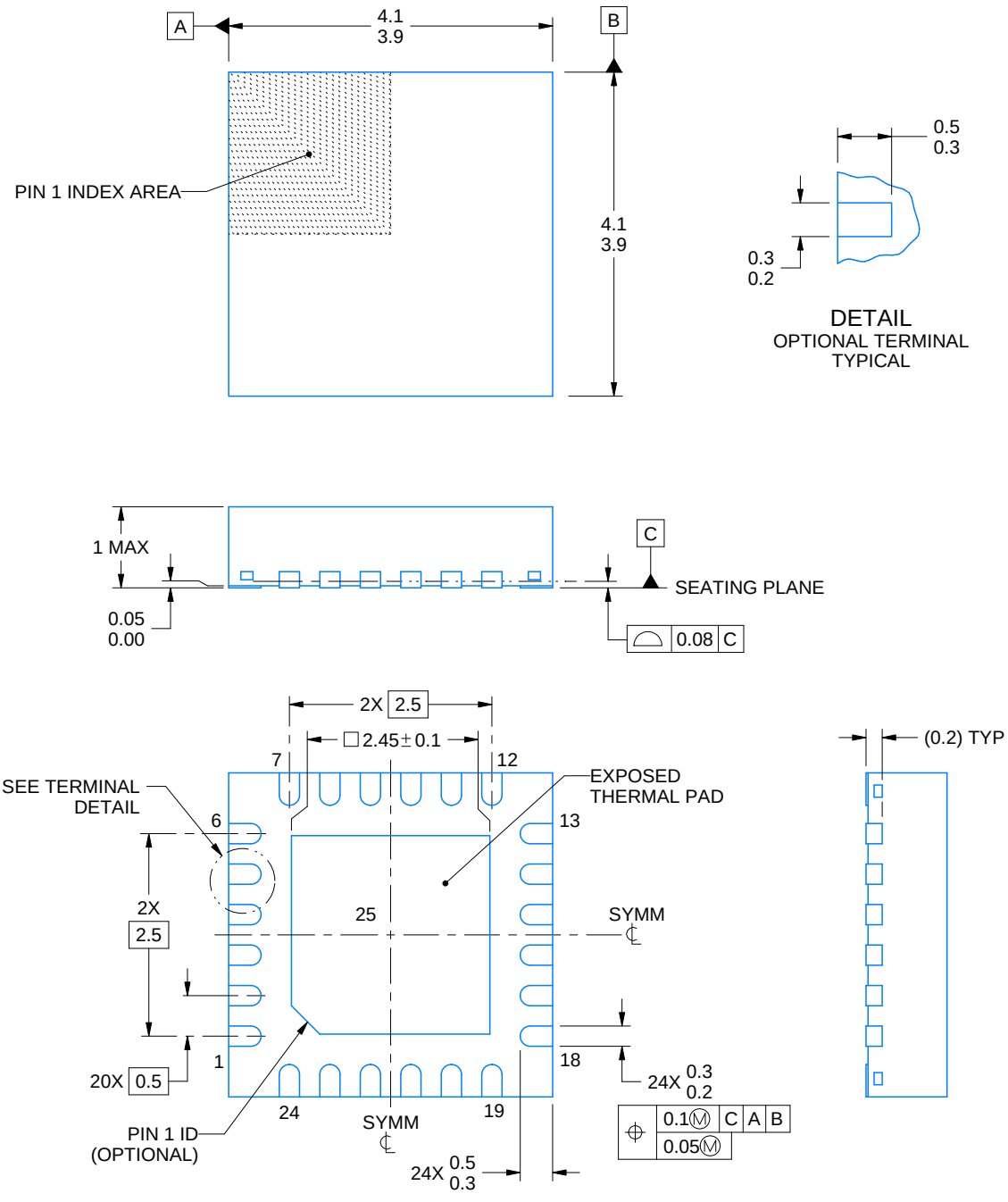
4204104/H

PACKAGE OUTLINE

RGE0024B

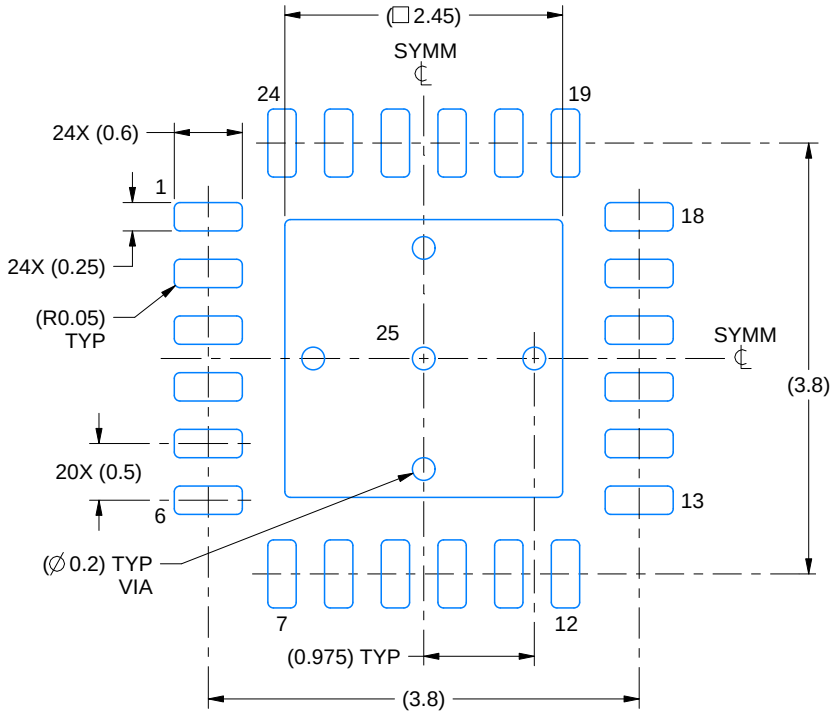
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

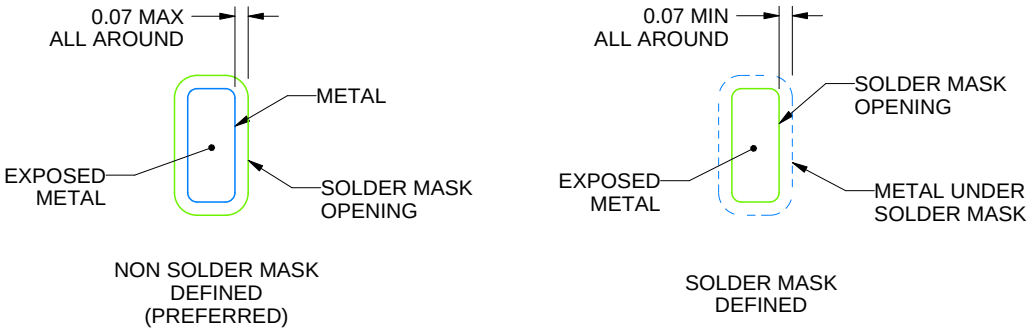


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

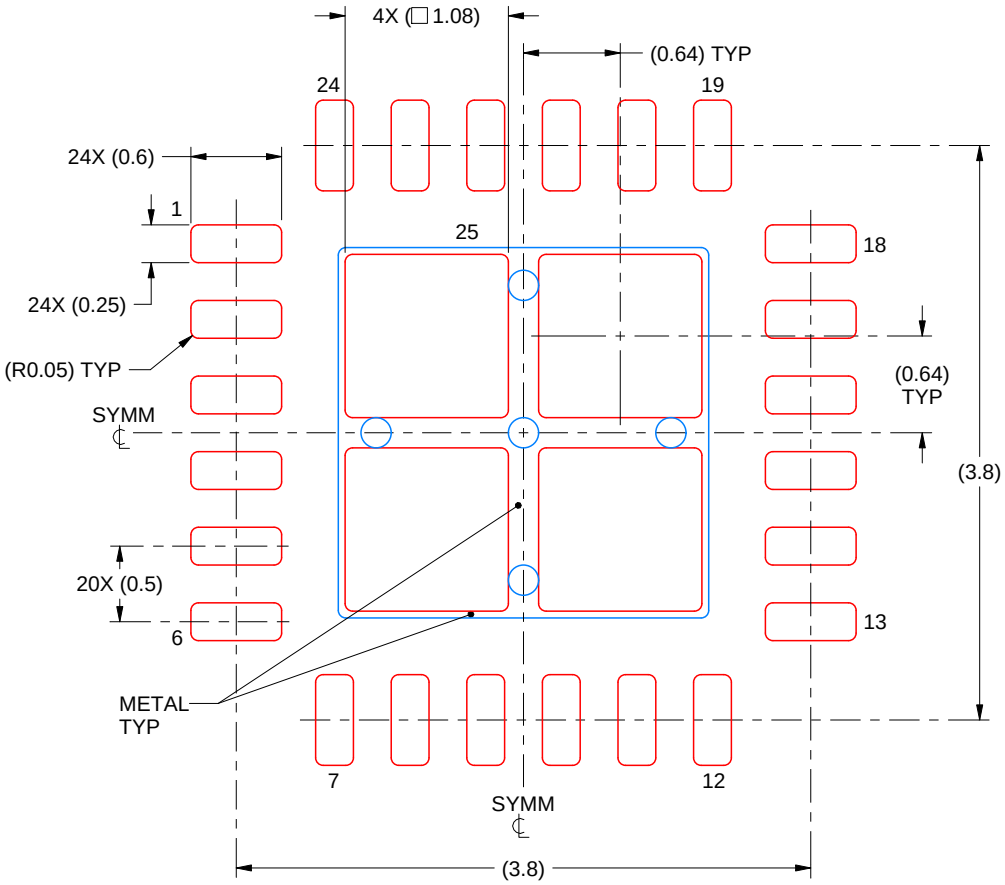


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月