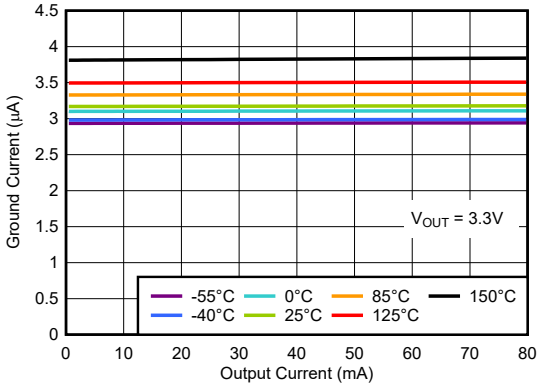
TPS714 80mA、10V、3.2µA 静止電流、低ドロップアウト リニア レギュレータ

1 特長

- 入力電圧範囲:2.5V～10V
- 選択可能な出力電圧:
  - 固定:1.8V～5V
  - 可変:1.205V～8.8V
- 出力電流:最大 80mA
- 超低 I_Q:80mA の負荷電流で 3.2µA
- ドロップアウト電圧:415mV (50mA 負荷の場合)
- 過電流保護
- 動作時接合部温度:-40℃～+125℃
- パッケージ:
  - 2mm × 1.25mm SC-70 (DCK)
  - 2mm × 2mm WSON (DRV)
- MSP430 固有の出力電圧については、TPS715 を参照してください

2 アプリケーション

- ホーム / ビルディング・オートメーション
- リテール・オートメーションおよびペイメント
- グリッド・インフラ
- 医療用アプリケーション
- 照明アプリケーション



静止電流と負荷電流との関係 (新チップ)

3 概要

TPS714 低ドロップアウト (LDO) リニア電圧レギュレータは、広い入力電圧範囲と低消費電力動作の利点を小型パッケージで実現する、低静止電流のデバイスです。このため、TPS714 はバッテリ駆動アプリケーションや、低消費電力マイコンの電力管理外付け機能用に設計されています。

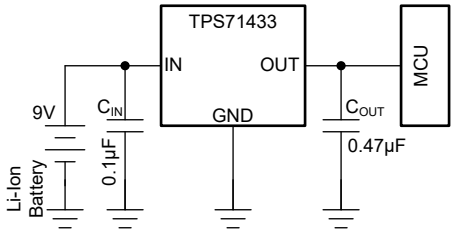
TPS714 には、固定電圧と可変電圧のバージョンがあります。より高い柔軟性またはより高い出力電圧を実現するために、調整可能バージョンでは、外付け帰還抵抗を使用して出力電圧を 1.205V～8.8V に設定します。TPS714 の LDO は、80mA の負荷電流で 650mV (標準値) の低ドロップアウトをサポートしています。静止電流が低く (標準値 3.2µA)、出力負荷電流の全範囲 (0mA～80mA) にわたって安定しています。また、TPS714 (新チップのみ) には、内部ソフトスタートが搭載されており、突入電流を低減できます。過電流制限機能が組み込まれているため、負荷の短絡やフォルトが発生してもレギュレータが保護されます。

TPS714 は、高消費電力アプリケーション向けの 2mm × 2mm パッケージで供給され、SC70-5 パッケージはハンドヘルドおよび超ポータブル アプリケーション向けに設計されています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
TPS714	DRV (WSON、6)	2mm × 2mm
	DCK (SC70、5)	2mm × 2.1mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

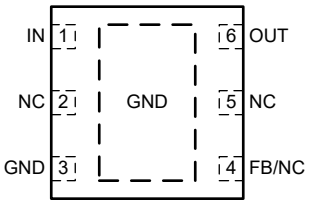


図 4-1. DRV Package, 6-Pin WSON (Top View)

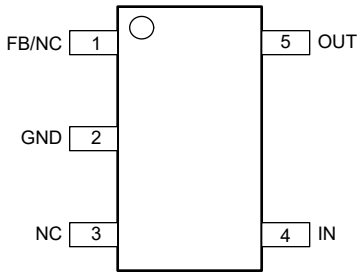


図 4-2. DCK Package, 5-Pin SC70 (Top View)

Pin Functions

TPS714					
	DCK		DRV		
NAME	FIXED	ADJ.	FIXED	ADJ.	DESCRIPTION
FB	—	1	—	4	In the adjustable configuration, this pin sets the output voltage with the help of the external feedback divider.
GND	2	2	3, Pad	3, Pad	Ground pin.
NC	1,3	3	2, 4, 5	2, 5	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.
IN	4	4	1	1	Input supply pin. Use a capacitor with a value of 0.1 µF or larger from this pin to ground.(2) See the *Input and Output Capacitor Requirements* section for more information.
OUT	5	5	6	6	Output of the regulator. For the new chip, a capacitor with a value of 1 µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Requirements* section for more information.

(1) The nominal output capacitance must be greater than 0.47 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47 µF. The legacy chip is stable for any capacitor value ≥ 0.47 µF.
(2) For the legacy chip, use a capacitor with a value of 0.047 µF or larger from IN to ground.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Voltage	V_{IN} (for legacy chip only)	–0.3	24	V
	V_{IN} (for new chip only)	–0.3	30	
	V_{OUT} (for fixed output new chip only)	–0.3	2 × $V_{OUT(typ)}$ or V_{IN} + 0.3 or 5.5 (whichever is lower)	
Voltage	V_{OUT} (for legacy chip only)	–0.3	9.9	V
Voltage	V_{OUT} (for adjustable output new chip only)	–0.3	V_{IN} + 0.3	V
	V_{FB} (for adjustable output new chip only)		2.4	
	V_{FB} (for adjustable output legacy chip only)	–0.3	4.5	
Current	Peak output current	Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		10	V
V_{OUT}	Output voltage	1.205		8.8	V
I_{OUT}	Output current	0		80	mA
C_{IN}	Input capacitor(2)	0	0.047		μF
C_{OUT}	Output capacitor (for legacy chip only)	0.47	1		
	Output capacitor (for new chip only) (3)	1			
T_J	Operating junction temperature	-40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.047 μF is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 0.47 μF minimum for the stability.

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5.4 Thermal Information

THERMAL METRIC		TPS714				UNIT
		DCK (SC-70) 5 Pins		DRV (WSON) 6 Pins		
		Legacy chip	New chip	Legacy chip	New chip	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.8	195.7	79.5	69.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	88.2	110.5	108.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.6	40.7	48.9	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	11.2	5.2	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.9	40.5	49.3	35.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	18.3	7.2	°C/W

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5.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range (1)		I_O = 10 mA	2.5		10	V
			I_O = 80mA	3		10	
V_{OUT}	Output voltage range (TPS71401)(1)			V_{FB}		8.8	V
V_{FB}	Internal reference (legacy chip) (TPS71401)(1)			1.12	1.2	1.24	V
	Internal reference (new chip) (TPS71401)(1)			1.16	1.2	1.24	
V_{OUT}	Accuracy (1)	TPS71433 over V_{IN}, I_{OUT} and Temp	4.3 V ≤ V_{IN} ≤ 10 V, 1 mA ≤ I_{OUT} ≤ 80 mA	3.135	3.3	3.465	V
I_{GND}	Ground pin current (legacy chip)(3)		1 mA ≤ I_{OUT} ≤ 80mA, T_J = –40°C to 85°C		3.2	4.2	µA
			1 mA ≤ I_{OUT} ≤ 80mA		3.2	5.8	
			1 mA ≤ I_{OUT} ≤ 80mA, V_{IN} = 10 V			7.4	
	Ground pin current (new chip) (3)		1 mA ≤ I_{OUT} ≤ 80mA, T_J = –40°C to 85°C		3.2	4.1	
			1 mA ≤ I_{OUT} ≤ 80mA		3.2	4.3	
			1 mA ≤ I_{OUT} ≤ 80mA, V_{IN} = 10 V			4.5	
ΔV_{OUT} (ΔIOUT)	Load regulation		I_{OUT} = 1 mA to 80 mA		30		mV
ΔV_{OUT} (ΔVIN)	Output voltage line regulation (1)		V_{OUT} + 1 V < V_{IN} ≤ 10 V		5		mV
$I_{FB\ BIAS}$	Feedback pin bias current		I_{OUT} = 0 mA, V_{IN} = 3V to 10V, V_{OUT} = 1.2V		2		nA
V_n	Output noise voltage (legacy chip)		BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
	Output noise voltage (new chip)		BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		425		
I_{CL}	Output current limit (legacy chip)		V_{OUT} = 0 V	100		1100	mA
	Output current limit (new chip)		V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	160		500	
	Output current limit (new chip)		V_{OUT} = 0 V, V_{IN} < 3.5 V	90		500	
V_{DO}	Dropout voltage (legacy chip)		V_{IN} = $V_{OUT(nom)}$ – 0.1 V, I_{OUT} = 80 mA		670	1300	mV
	Dropout voltage (new chip)		V_{IN} = $V_{OUT(nom)}$ – 0.1 V, I_{OUT} = 80 mA		670	900	

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) This device employs a leakage null control circuit. This circuit is active only if output current is less than pass transistor leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.

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5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

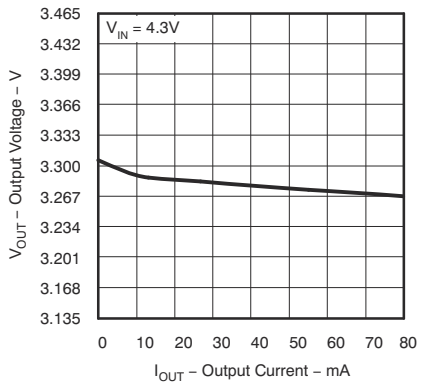


図 5-1. TPS71433 Output Voltage vs Output Current (Legacy Chip)

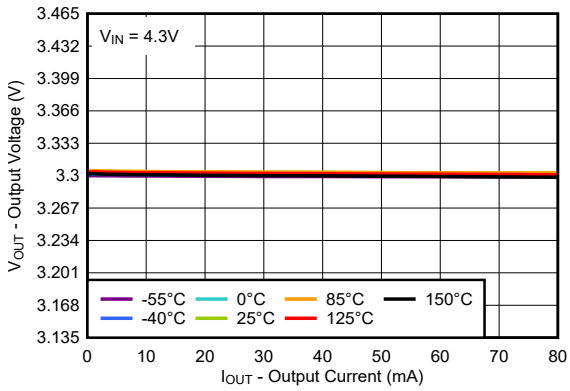


図 5-2. TPS71433 Output Voltage vs Output Current (New Chip)

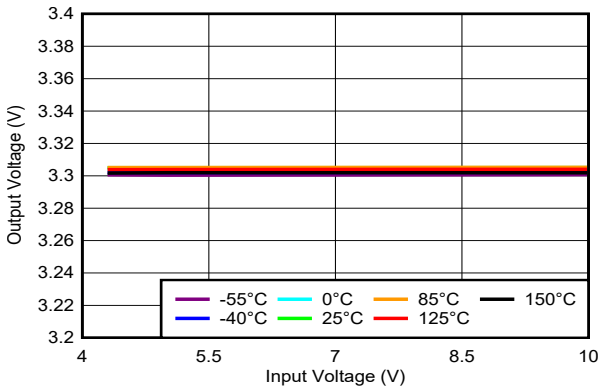


図 5-3. TPS71433 Output Voltage vs Input Voltage (New Chip)

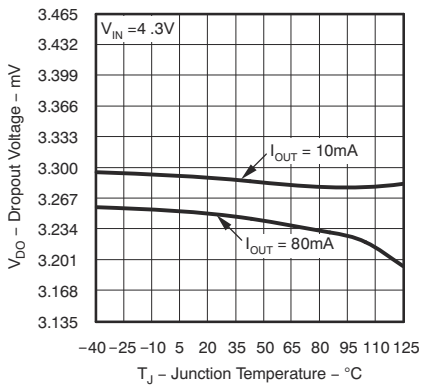


図 5-4. TPS71433 Output Voltage vs Junction Temperature (Legacy Chip)

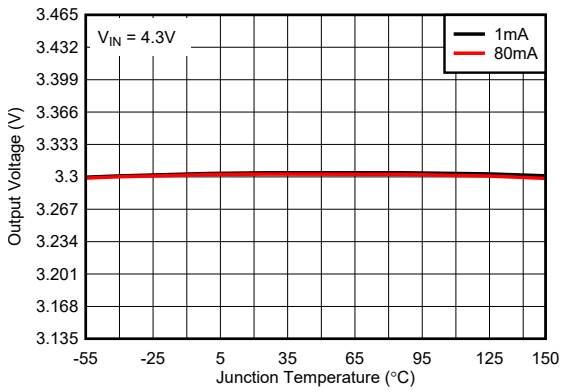


図 5-5. TPS71433 Output Voltage vs Junction Temperature (New Chip)

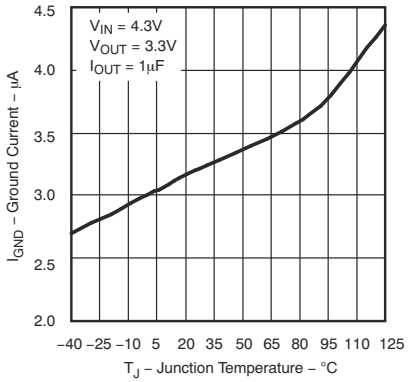


図 5-6. TPS71433 Quiescent Current vs Junction Temperature (Legacy Chip)

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5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

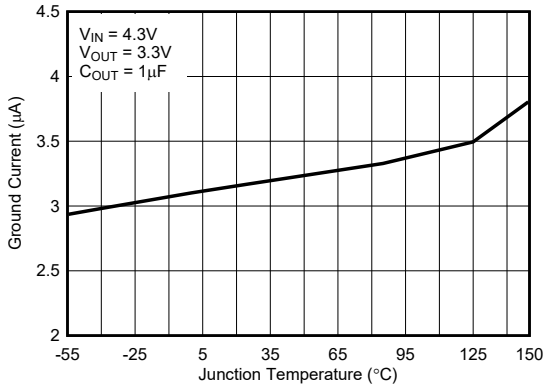


図 5-7. TPS71433 Quiescent Current vs Junction Temperature (New Chip)

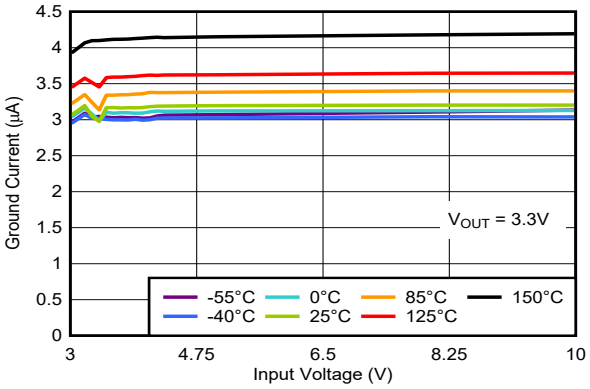


図 5-8. TPS71433 Quiescent Current vs Input Voltage (New Chip)

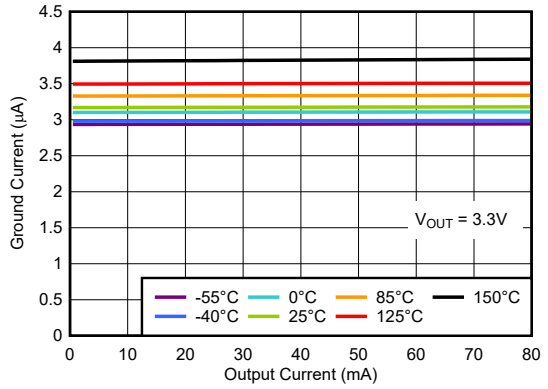


図 5-9. TPS71433 Quiescent Current vs Load Current (New Chip)

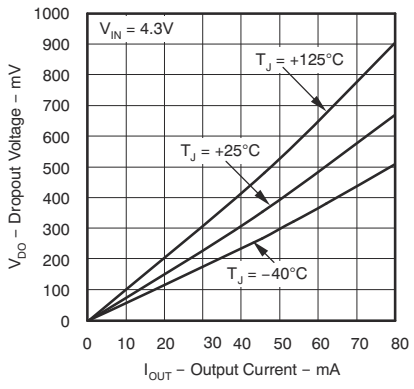


図 5-10. TPS71433 Dropout Voltage vs Output Current (Legacy Chip)

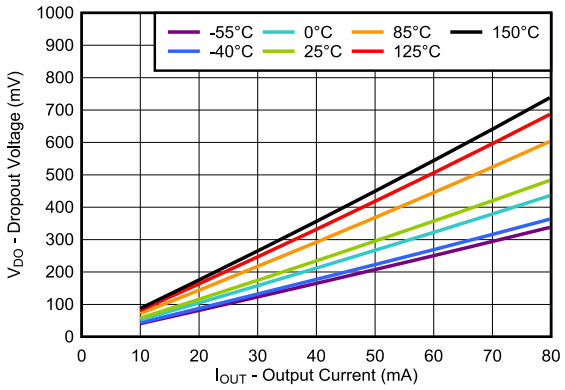


図 5-11. TPS71433 Dropout Voltage vs Output Current (New Chip)

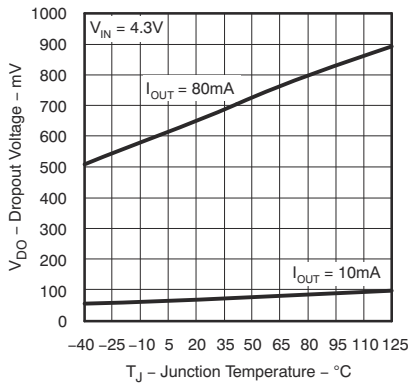


図 5-12. TPS71433 Dropout Voltage vs Junction Temperature (Legacy Chip)

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5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

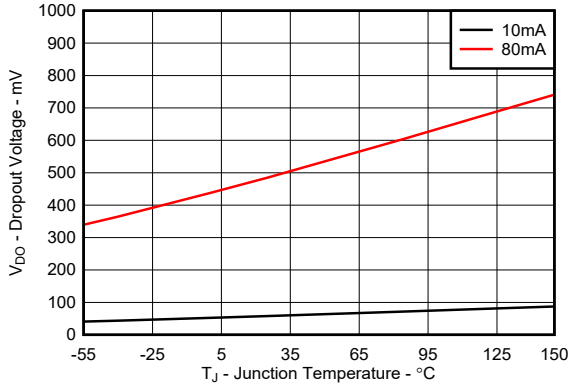


図 5-13. TPS71433 Dropout Voltage vs Junction Temperature (New Chip)

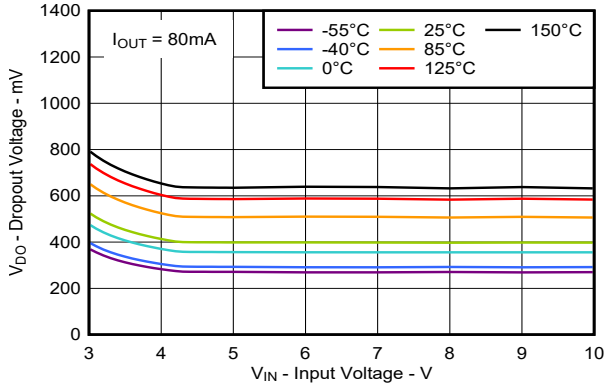


図 5-14. TPS71401 Dropout Voltage vs Input Voltage (New Chip)

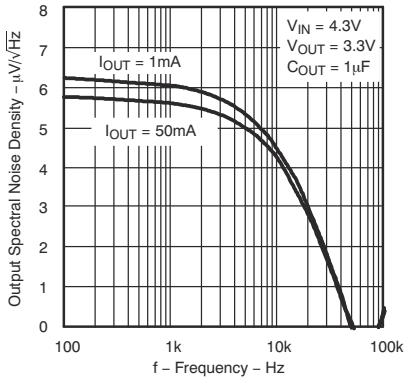


図 5-15. TPS71433 Output Spectral Noise Density vs Frequency (Legacy Chip)

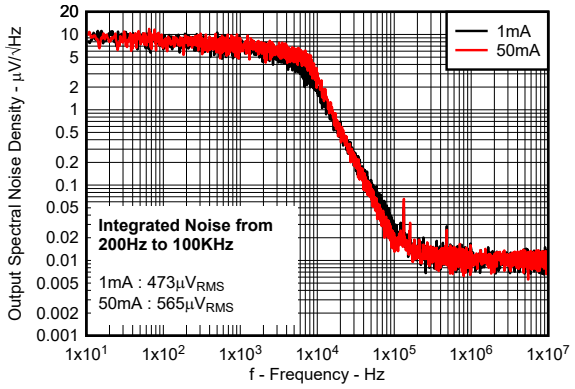


図 5-16. TPS71433 Output Spectral Noise Density vs Frequency (New Chip)

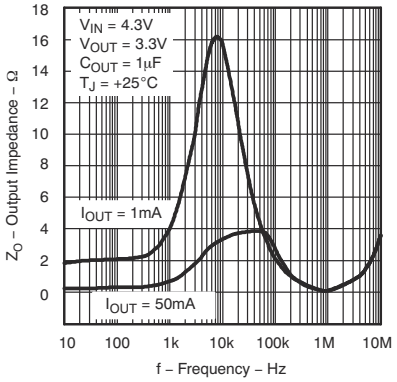


図 5-17. TPS71433 Output Impedance vs Frequency (Legacy Chip)

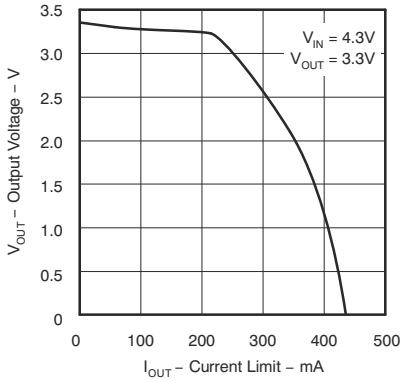


図 5-18. TPS71433 V_{OUT} vs Current Limit (Legacy Chip)

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5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

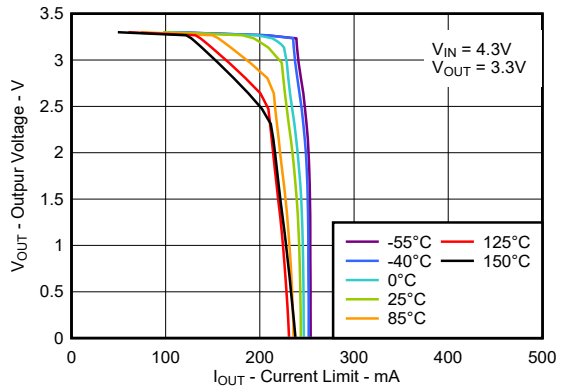


図 5-19. TPS71433 V_{OUT} vs Current Limit (New Chip)

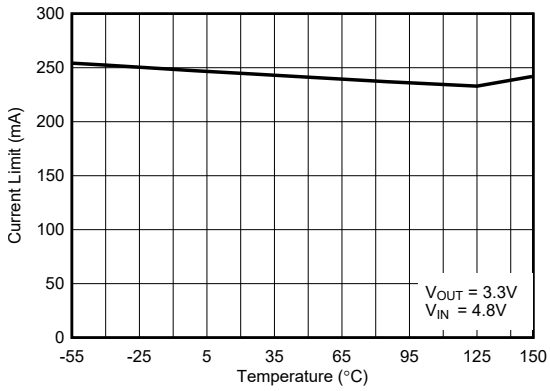


図 5-20. TPS71433 Current Limit vs Junction Temperature (New Chip)

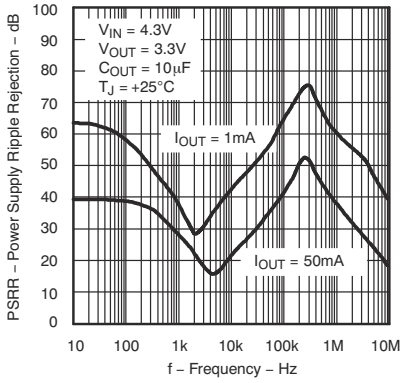


図 5-21. TPS71433 Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

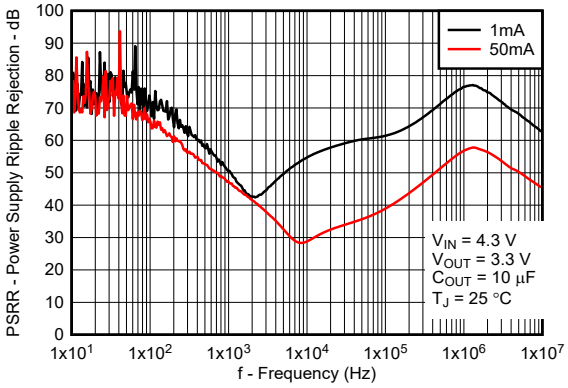


図 5-22. TPS71433 Power-Supply Ripple Rejection vs Frequency (New Chip)

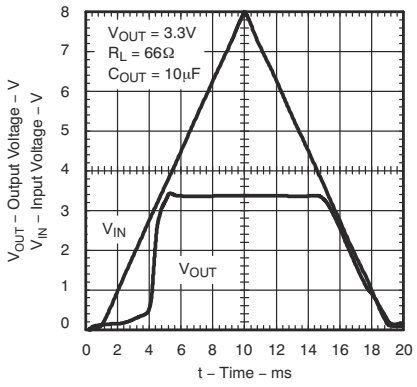


図 5-23. TPS71433 Power-Up, Power-Down (Legacy Chip)

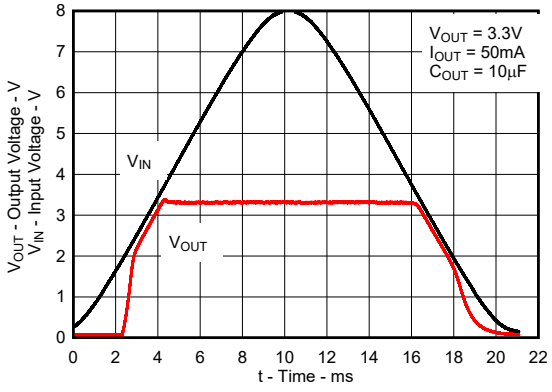


図 5-24. TPS71433 Power-Up, Power-Down (New Chip)

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5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

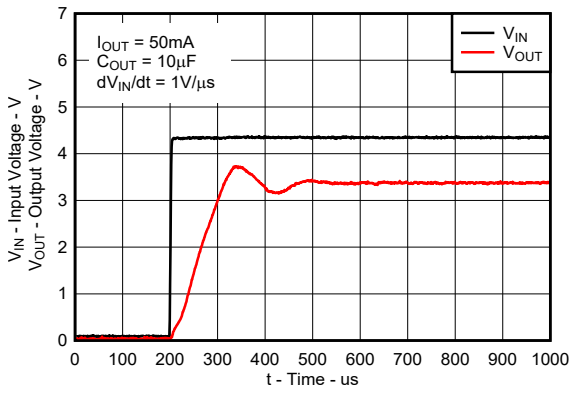


図 5-25. TPS71433 Fast Power-Up (Legacy Chip)

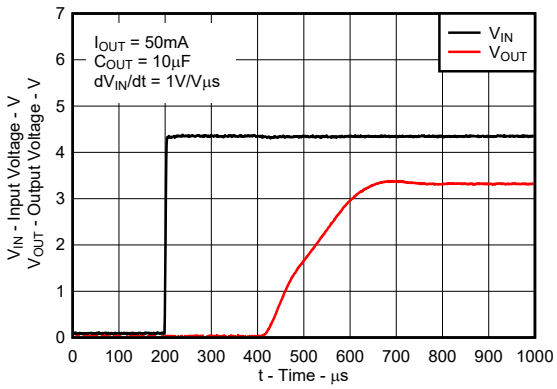


図 5-26. TPS71433 Fast Power-Up (New Chip)

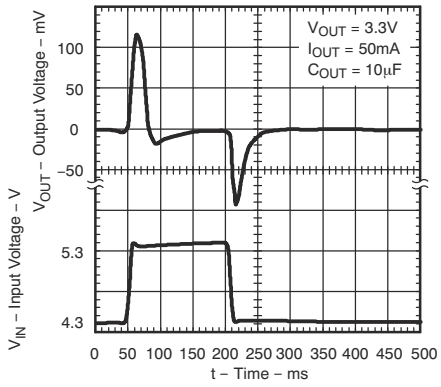


図 5-27. TPS71433 Line Transient Response (Legacy Chip)

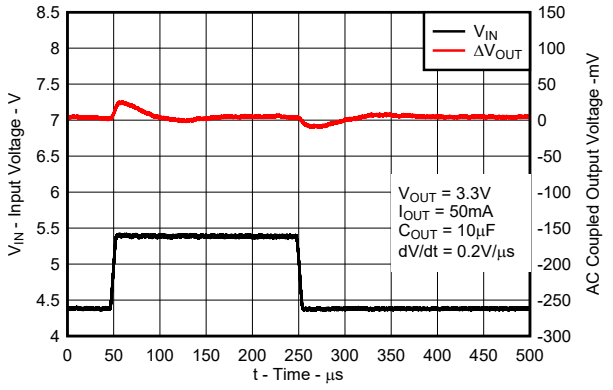


図 5-28. TPS71433 Line Transient Response (New Chip)

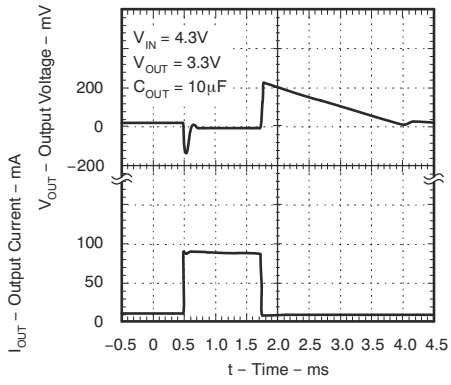


図 5-29. TPS71433 Load Transient Response (Legacy Chip)

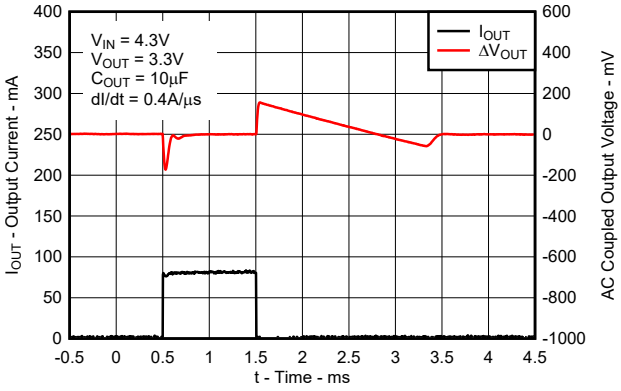


図 5-30. TPS71433 Load Transient Response (New Chip)

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6 Detailed Description

6.1 Overview

The TPS714 low-dropout regulator (LDO) consumes only 3.2 µA (typ) of quiescent current across the entire output current range, while offering a wide input voltage range and low-dropout voltage in small packaging. The device, which operates over an input range of 2.5 V to 10 V, is stable with any output capacitance greater than or equal to 0.47 µF. The low quiescent current across the complete load current range makes the TPS714 designed for powering battery-operated applications. The TPS714 (new chip only) has an internal soft-start to control inrush current into the output capacitor. This LDO also has overcurrent protection during a load-short or fault condition on the output.

6.2 Functional Block Diagrams

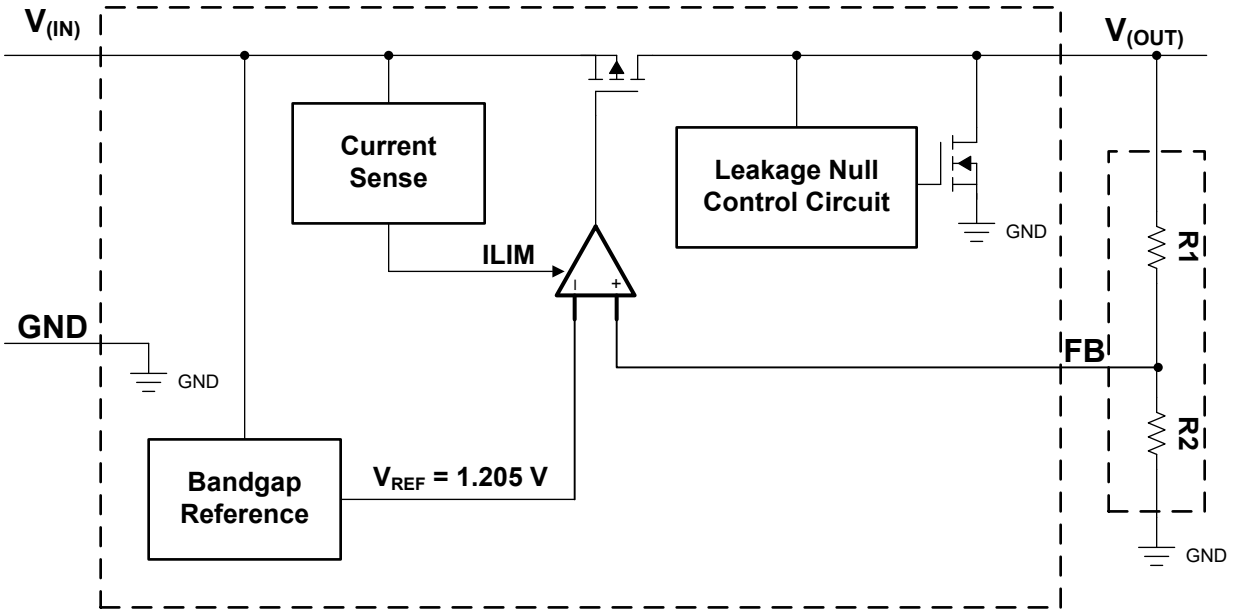


図 6-1. Adjustable Voltage Version

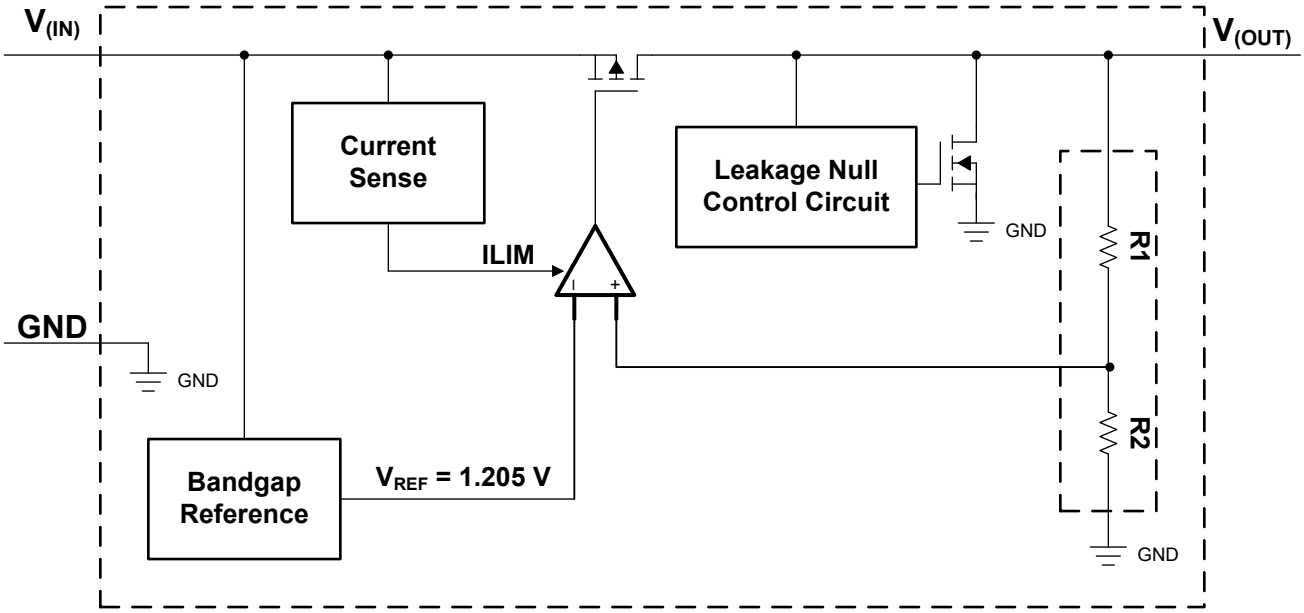


図 6-2. Fixed Voltage Version

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6.3 Feature Description

6.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 10 V, allowing for a wide range of applications. This wide supply range is ideal for applications that have either large transients or high dc voltage supplies.

6.3.2 Low Supply Current

This device only requires 3.2 µA (typical) of quiescent current across the complete load current range (0 mA to 80 mA) and has a maximum current consumption of 4.8 µA (for new device only) at –40°C to +125°C.

6.3.3 Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note. The LDO is not designed to operate in a steady-state current limit.

図 6-3 shows a diagram of the current limit.

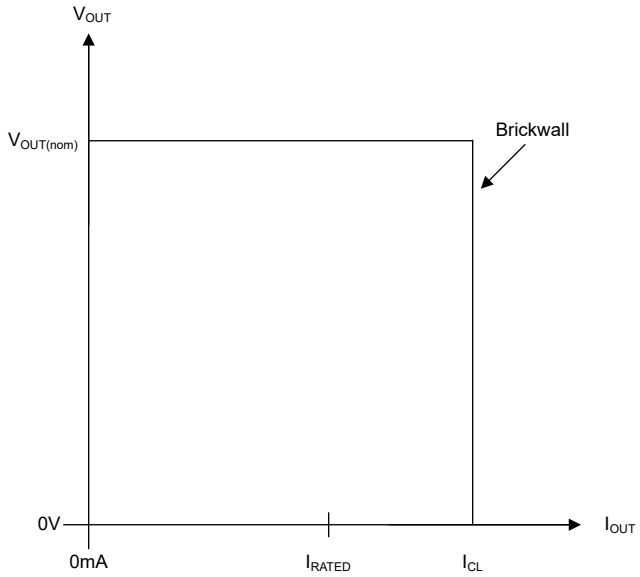


図 6-3. Current Limit

6.3.4 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use 式 1 to calculate the $R_{DS(ON)}$ of the device.

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$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.4 Device Functional Modes

表 6-1 provides a quick comparison between the normal and dropout modes of operation.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

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7 Application and Implementation

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7.1 Application Information

The TPS714 LDO regulator is designed for battery-powered applications and is a good supply for low-power microcontrollers (such as the MSP430) because of the device low I_Q performance across load current range. The ultra-low-supply current of the TPS714 maximizes efficiency at light loads, and the high input voltage range and flexibility of output voltage selection in the adjustable configuration and fixed output levels makes the device an optimal supply for building automation and power tools.

7.2 Typical Applications

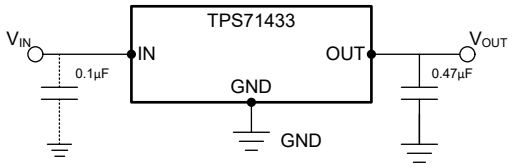
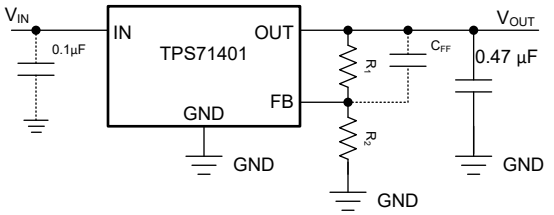


図 7-1. Typical Application Circuit (Fixed-Voltage Version)



Output Voltage	R1	R2
1.8V	0.499 MΩ	1MΩ
2.8V	1.33 MΩ	1MΩ
5.0V	3.16 MΩ	1MΩ

図 7-2. TPS714 Adjustable LDO Regulator Programming

7.2.1 Design Requirements

The minimum output capacitor (C_{OUT}) value for stability is needed, as suggested in the *Recommended Operating Conditions*.

表 7-1 summarizes the design requirements for this application.

表 7-1. Design Parameters

PARAMETER	VALUE
Input voltage	4.3 V
Output voltage	3.3 V
Output current	50 mA

7.2.2 Detailed Design Procedure

7.2.2.1 Setting V_{OUT} for the TPS71401 Adjustable LDO

The TPS714 contains an adjustable version, the TPS71401, which sets the output voltage using an external resistor divider, as shown in 図 7-2. The output voltage operating range is 1.205 V to 8.8 V, and is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where:

- V_{REF} = 1.205 V (typical)

Choosing resistors R1 and R2 allows approximately 1.5 µA of current through the resistor divider. Lower value resistors can be used for improved noise performance, but consume more power. Avoid higher resistor values because leakage current into or out of FB across R1 / R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using 式 3:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (3)$$

図 7-2 depicts this configuration.

7.2.2.2 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value. For the legacy chip, Any capacitor (including ceramic and tantalum) greater than or equal to 0.47 µF properly stabilizes the output regulation loop.

Although not required, a 0.1-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, improves transient response and noise rejection of the power supply as a whole. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

7.2.2.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.2.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN}$ + 0.3 V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

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If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

図 7-3 shows one approach for protecting the device.

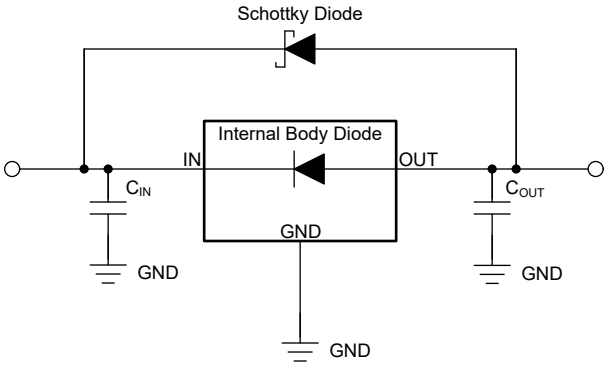


図 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however,the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 µA. 式 6 calculates the feedback divider current.

$$I_{FB_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 1.205 V with the FB pin tied to the OUT pin, no C_{FF} is used.

7.2.2.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (7)$$

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Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.2.2.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

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7.2.3 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

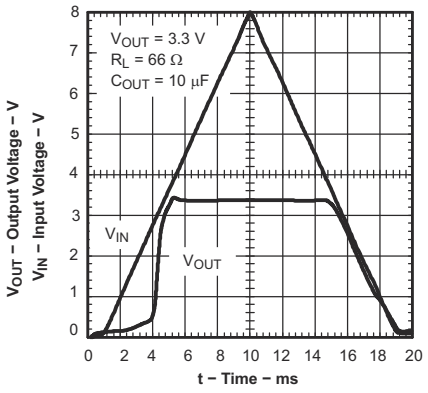


図 7-4. Power-Up and Power-Down (Legacy Chip)

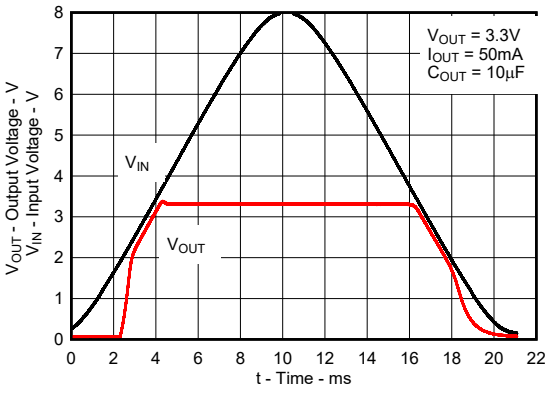


図 7-5. Power-Up and Power-Down (New Chip)

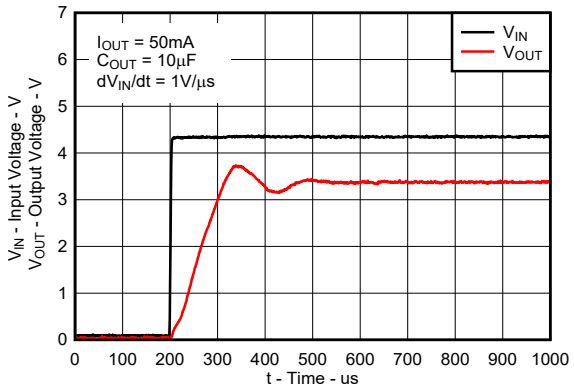


図 7-6. TPS71433 Fast Power-Up (Legacy Chip)

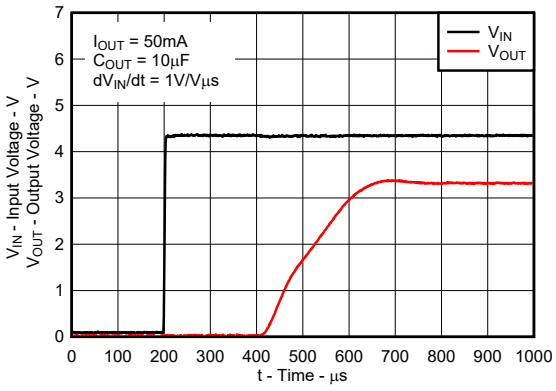


図 7-7. TPS71433 Fast Power-Up (New Chip)

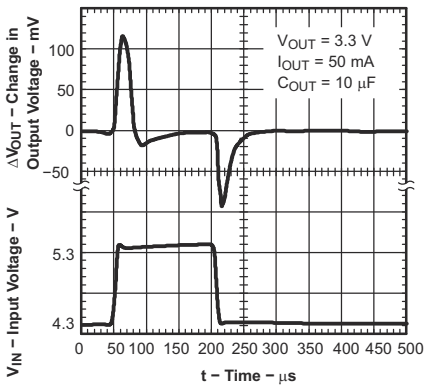


図 7-8. Line Transient Response (Legacy Chip)

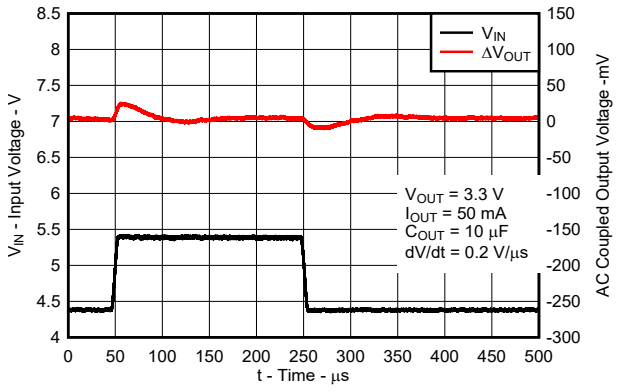


図 7-9. Line Transient Response (New Chip)

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7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

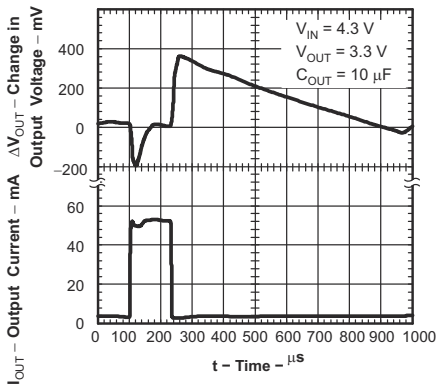


図 7-10. Load Transient Response (Legacy Chip)

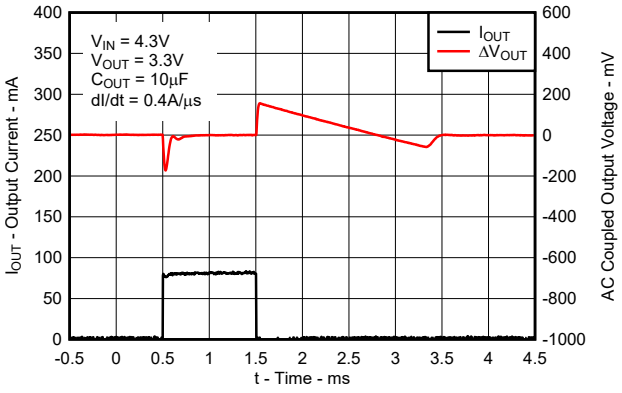


図 7-11. Load Transient Response (New Chip)

7.3 Power Supply Recommendations

The TPS714 is designed to operate from an input voltage supply range between 2.5 V and 10 V. The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Avoid using vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because doing so negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is recommended to be embedded either in the PCB or located on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage and shields the LDO from noise.

7.4.1.1 Power Dissipation

To provide reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using 式 11.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \tag{11}$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

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The regulator power dissipation is calculated using 式 12.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (12)$$

For wider input range requirement, see the TPS715A.

7.4.2 Layout Example

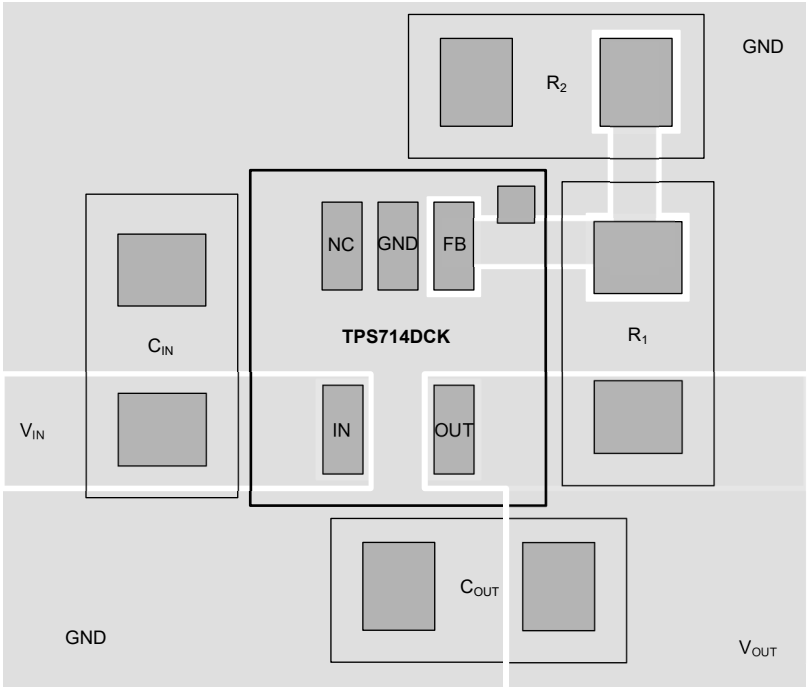


図 7-12. Example Layout for the TPS714DCK

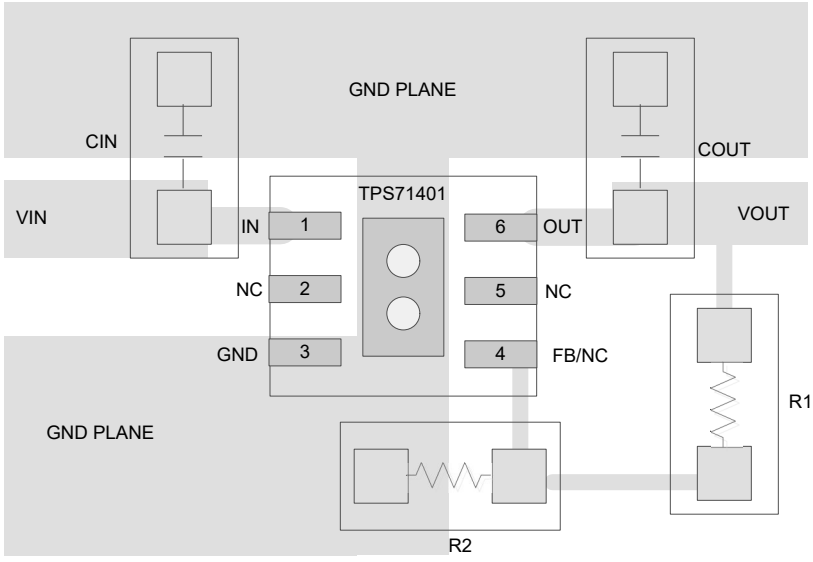


図 7-13. Example Layout for the TPS714DRV

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Device Information(1)

PRODUCT	V_{OUT} (2)
TPS714**xxyyyz**	**XX** is nominal output voltage (for example 33 = 3.3 V, 01 = adjustable). **YYY** is package designator. **Z** is package quantity.
TPS714**xxyyyz M3**	**xx** is nominal output voltage (for example 33 = 3.3V, 01 = adjustable) **yyy** is package designator **z** is package quantity **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Custom output voltages are available on a quick-turn basis for prototyping. Production quantities are available; minimum package order quantities apply. Contact factory for details and availability.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (March 2011) to Revision D (November 2023) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- 「製品情報」表、ページ 1 の図、「ESD 定格」、「推奨動作条件」、「熱に関する情報」、「概要」、「機能説明」、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- ドキュメント全体で「SON」を「WSON」に変更 1
- 「特長」、「アプリケーション」、「概要」セクションを変更 1
- Changed *Description* column of *Pin Functions* table and added table footnotes 3
- Added curves for new chip to *Typical Characteristics* section 7

Changes from Revision B (December 2009) to Revision C (March 2011) **Page**

- Changed *Ground pin current* maximum specifications in *Electrical Characteristics* table 4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71401DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DRVRM3	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DRVRM3.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71401DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVG
TPS71433DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DCKT	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	CVH
TPS71433DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH
TPS71433DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

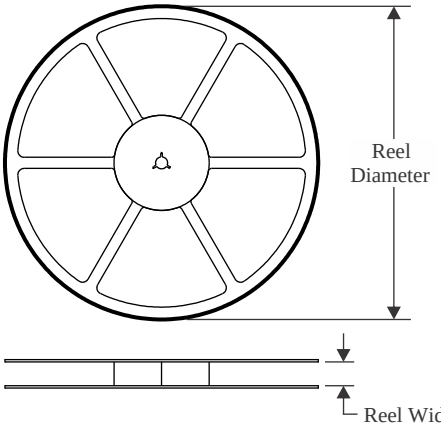
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

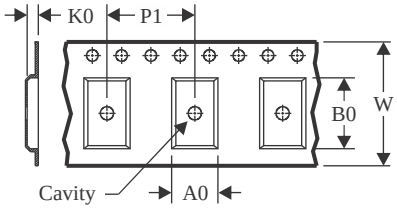
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

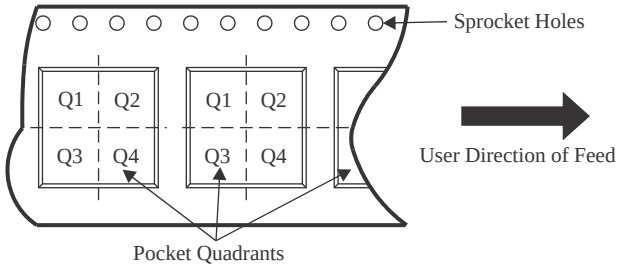


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

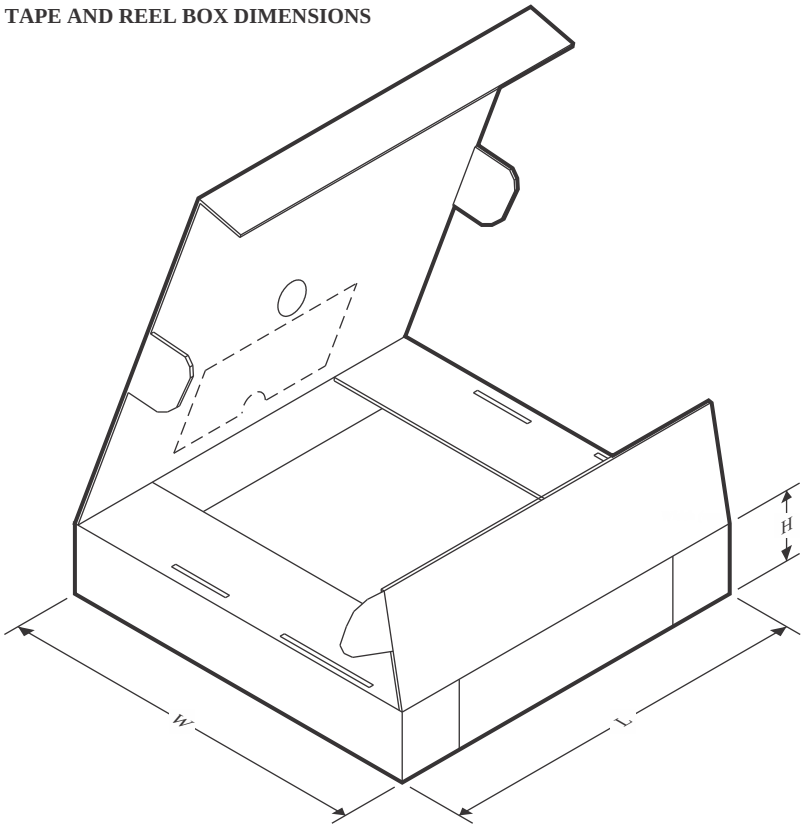
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71401DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71401DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71401DCKT	SC70	DCK	5	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71401DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS71401DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS71401DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71433DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71433DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71433DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71433DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

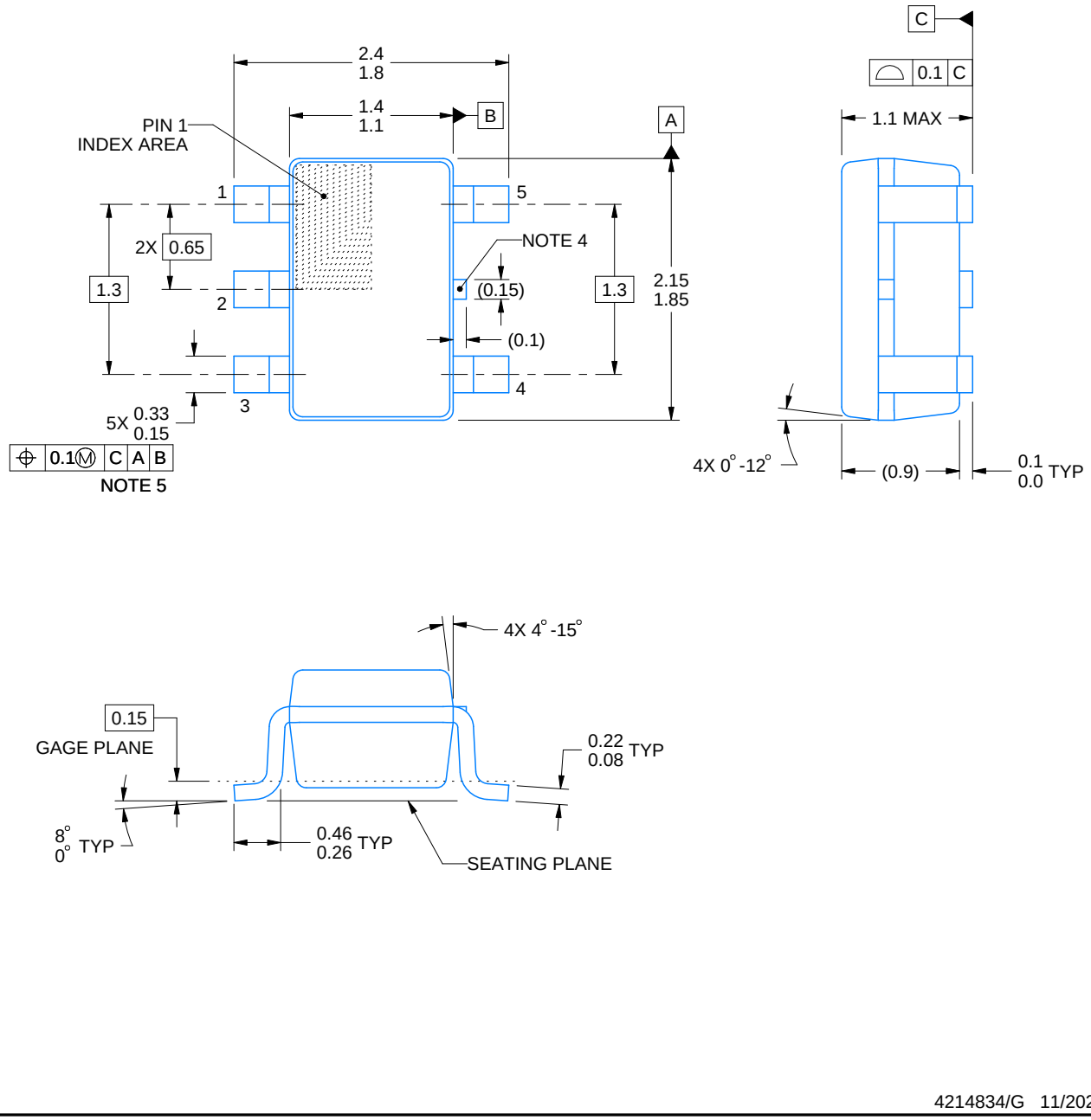
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71401DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71401DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71401DCKT	SC70	DCK	5	250	183.0	183.0	20.0
TPS71401DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS71401DRVRM3	WSON	DRV	6	3000	210.0	185.0	35.0
TPS71401DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS71433DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71433DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71433DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71433DRVT	WSON	DRV	6	250	203.0	203.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

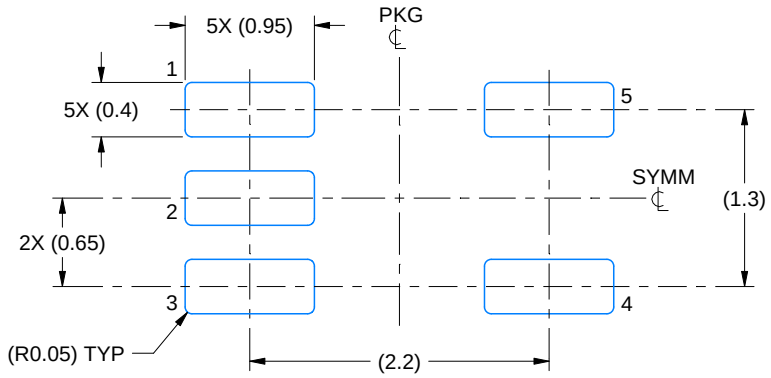
SMALL OUTLINE TRANSISTOR



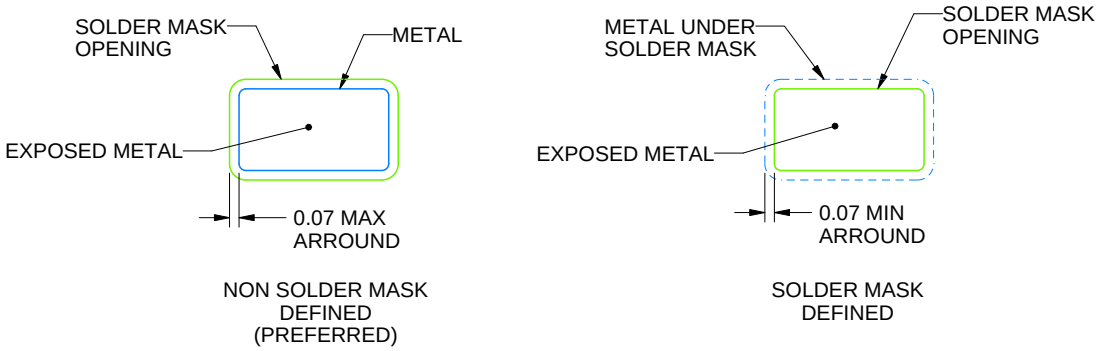
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

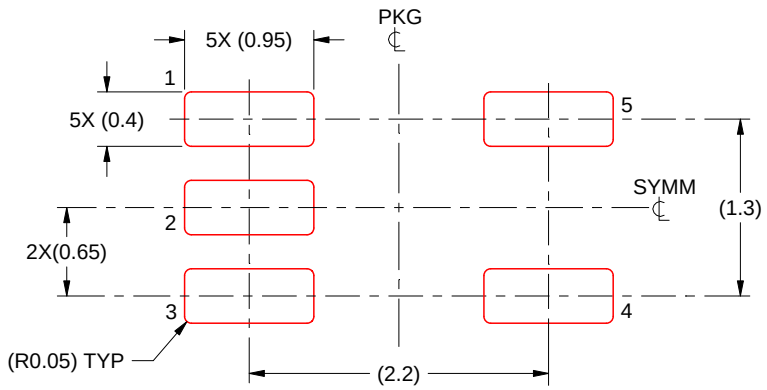


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

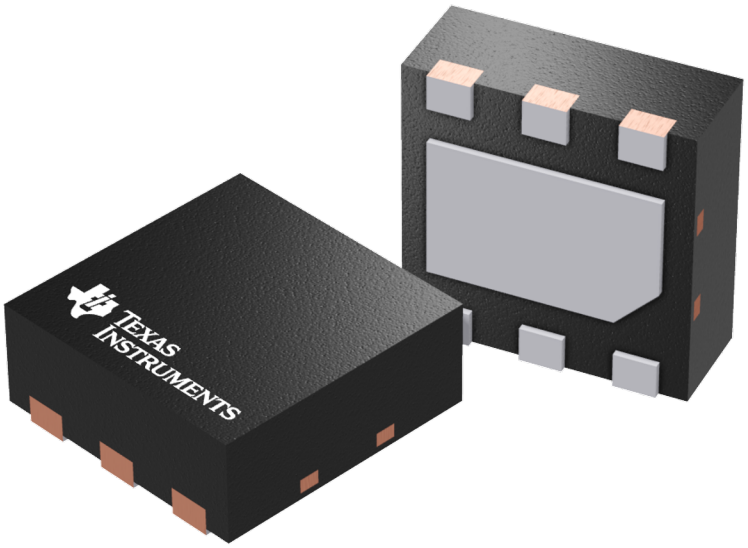
4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



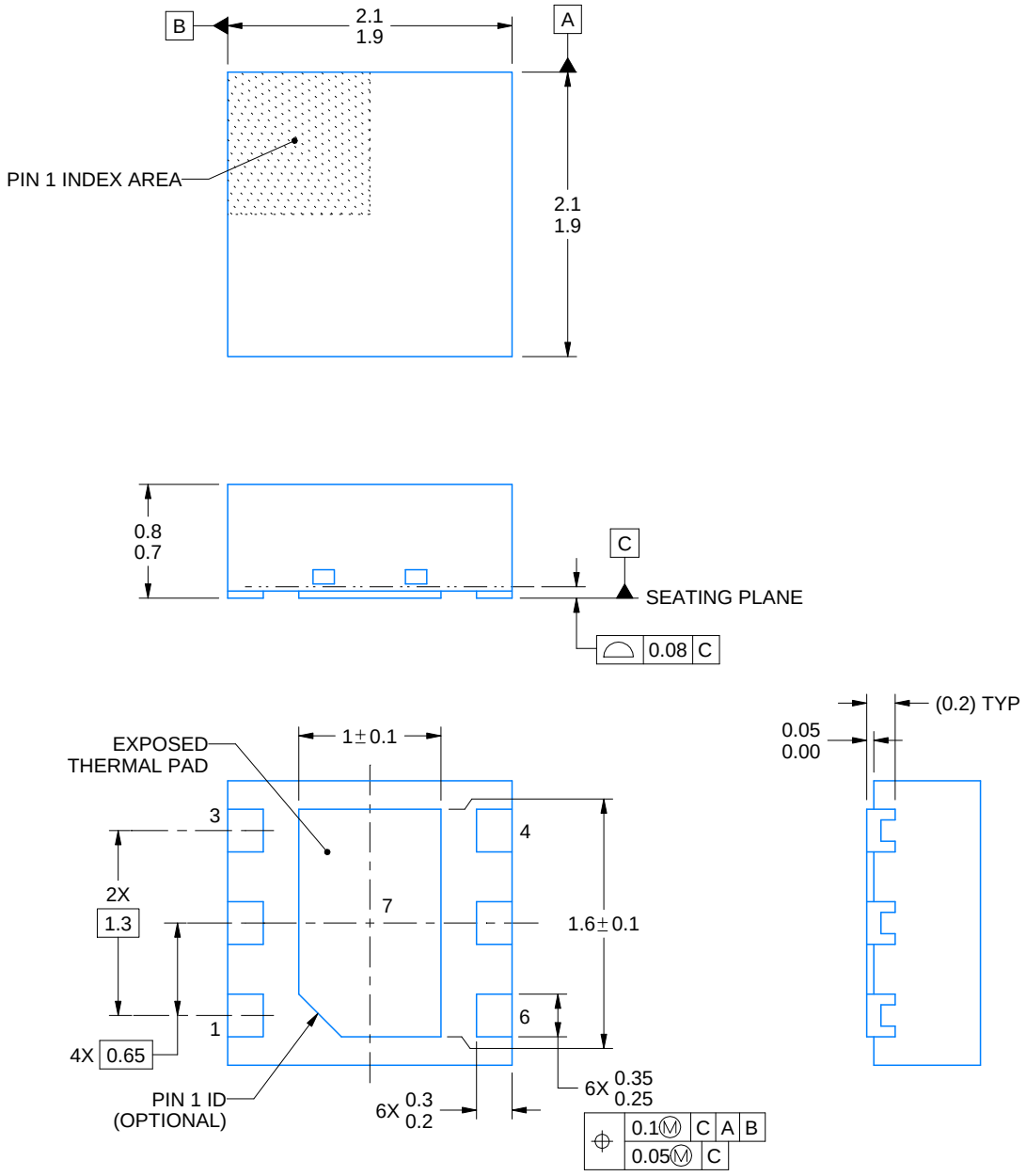
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

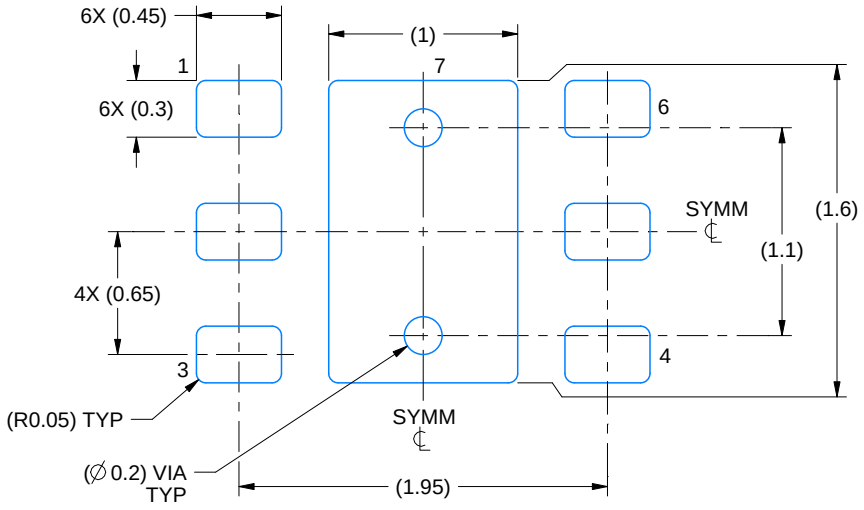
PLASTIC SMALL OUTLINE - NO LEAD



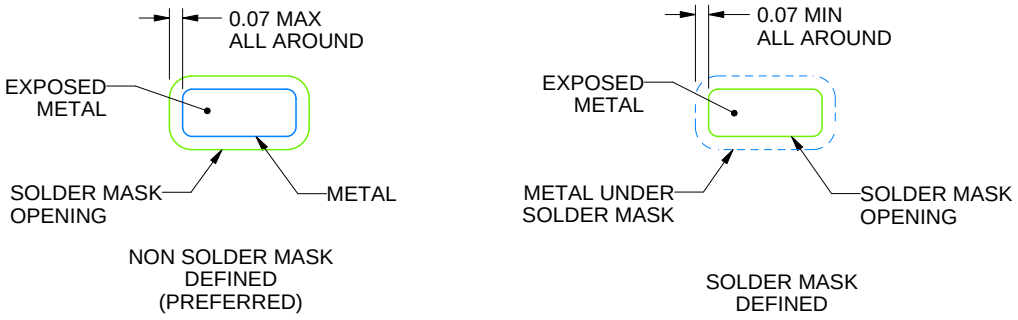
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

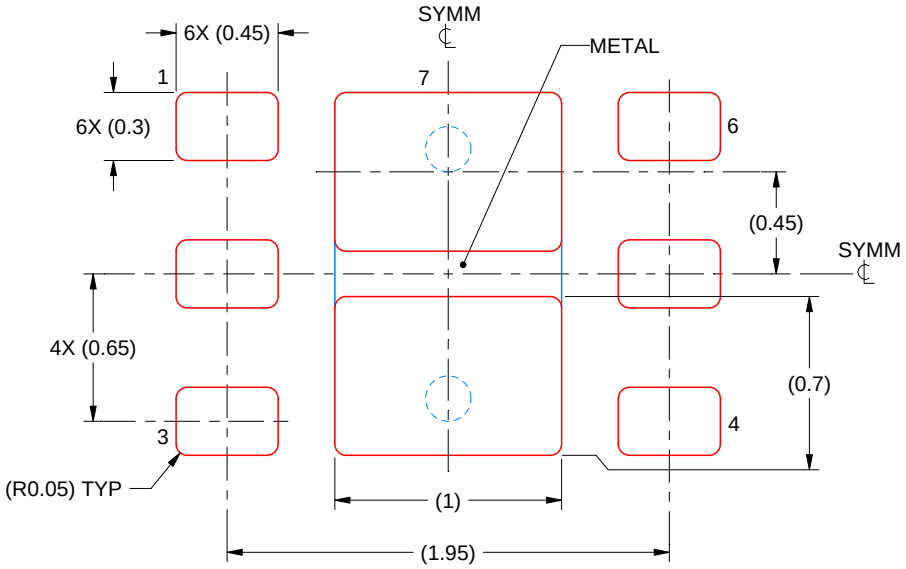


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



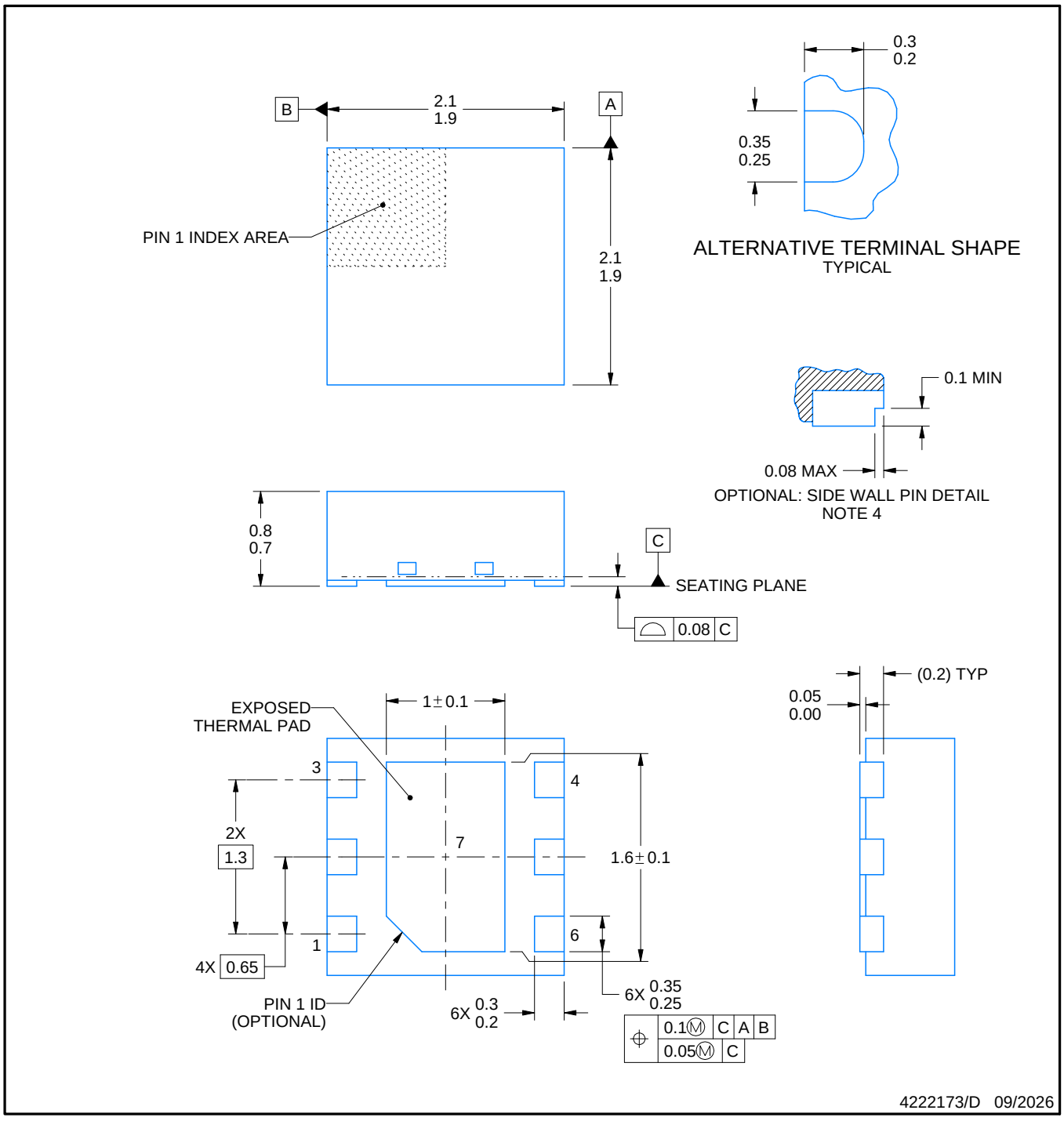
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

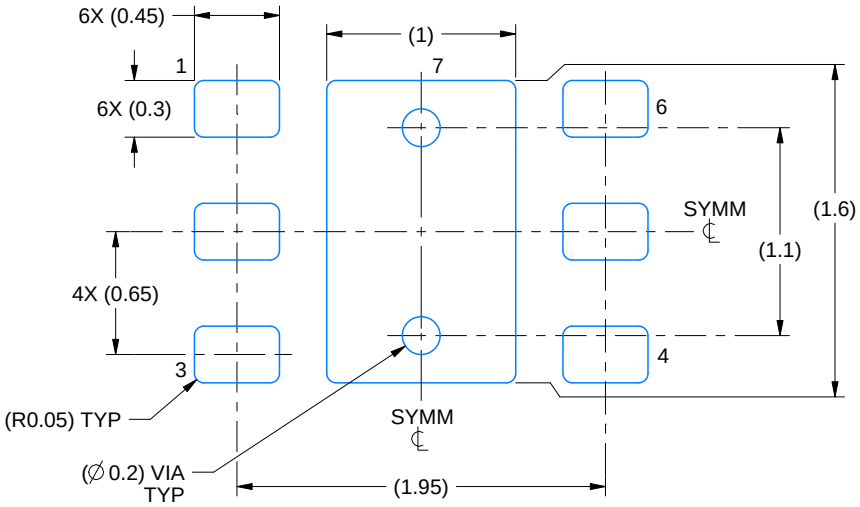
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

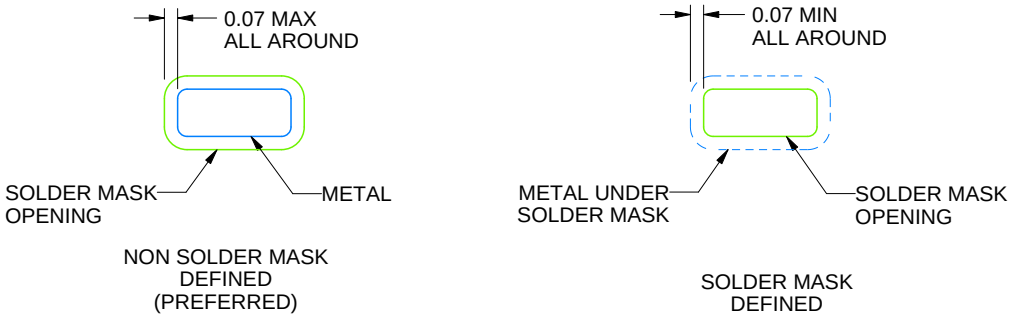


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

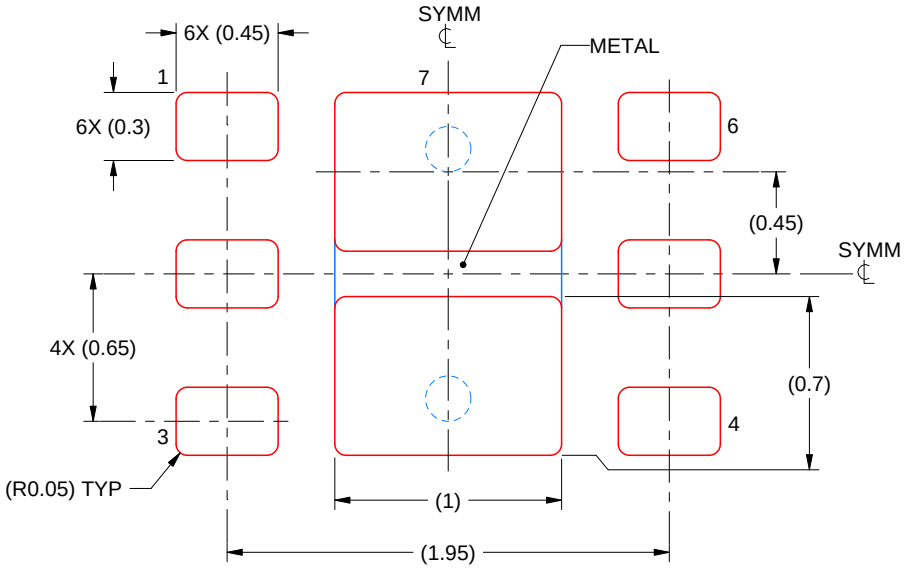


SOLDER MASK DETAILS

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NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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