TPS735 500mA、低静止電流、低ノイズ、高PSRR、低ドロップアウトのリニア・レギュレータ

1 特長

- 入力電圧: 2.7V～6.5V
- ENを備えた500mA低ドロップアウト・レギュレータ
- 低いI_Q: 45µA
- 複数の出力電圧バージョンを利用可能:
  - 1.2V～4.3Vの固定出力
  - 1.25V～6Vの可変出力
- 高いPSRR: 1kHzにおいて68dB
- 低ノイズ: 13.2µV_{RMS}
- 短いスタートアップ時間: 45µs
- セラミック、2.2µF、低ESRの出力コンデンサで安定
- 非常に優れた負荷/ライン過渡応答
- 総合精度2% (負荷、ライン、および温度、V_{OUT} > 2.2V)
- 非常に低いドロップアウト: 500mAにおいて280mV
- 2mm×2mmのWSON-6および3mm×3mmのSON-8パッケージ

2 アプリケーション

- DC-DCコンバータ後のリップル・フィルタリング
- IPネットワーク・カメラ
- マクロ基地局
- サーモスタット

3 概要

TPS735低ドロップアウト(LDO)低消費電力リニア・レギュレータは、極めて低いグランド電流で優れたAC性能を提供します。高い電源除去比(PSRR)、低ノイズ、高速スタートアップ、優れたライン/負荷過渡応答を実現しながら、消費するグランド電流はわずか45µA (標準値)です。

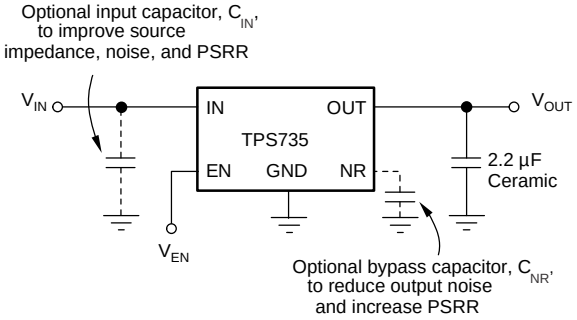
TPS735デバイスはセラミック・コンデンサで安定動作し、先進のBiCMOS製造プロセスを使用しているため、500mA出力で標準280mVのドロップアウト電圧を実現しています。TPS735デバイスは、高性能な電圧リファレンスと帰還ループにより、すべての負荷、ライン、製造プロセス、および温度変化に対して2% (V_{OUT} > 2.2V)の総合精度を達成できます。このデバイスはT_J = -40℃～+125℃で完全に動作が規定されており、薄型の3mm×3mm SON-8パッケージおよび2mm×2mm WSON-6パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS735	WSON (6)	2.00mm×2.00mm
	SON (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision L (January 2015) から Revision M に変更 **Page**

- 最新のデータシートおよび翻訳標準に合わせてデータシートを更新 ... 1
- ドキュメントのタイトルで「超低ノイズ」を「低ノイズ」に 変更 ... 1
- 「*特長*」、「*概要*」、「*アプリケーション情報*」セクションで、低I_Qを46µAから45µAに 変更 ... 1
- 「*特長*」箇条書きの「標準」を「セラミック」に 変更 ... 1
- 「*特長*」箇条書きの6ピン・パッケージを「SON」から「WSON」に 変更 ... 1
- 「*アプリケーション*」セクションからプリンタ、WiFi®、WiMaxモジュール、携帯電話、スマートフォン、マイクロプロセッサの電源を削除 ... 1
- 「*アプリケーション*」セクションにDC/DC後のリップル・フィルタリング、IPネットワーク・カメラ、マクロ基地局、サーモスタットを 追加 ... 1
- 「*概要*」セクションでT_AをT_Jに 変更 ... 1
- 「*概要*」セクションで6ピンのパッケージを「SON」から「WSON」に 変更 ... 1
- 「*製品情報*」表のパッケージをVSON (6)からWSON (6)に 変更 ... 1
- Changed 6-pin DRB package designator from "VSON" to "SON" in *Pin Configurations and Functions* section ... 4
- Changed 6-pin DRV package designator from "VSON" to "WSON" in *Pin Configurations and Functions* section ... 4
- Added "feedback resistor" parameter to *Recommended Operating Conditions* table ... 5
- Changed DRV package designator from "VSON" to "WSON" in *Thermal Information* table ... 6
- Changed DRB package designator from "VSON" to "SON" in *Thermal Information* table ... 6
- 変更 *TPS735 Ground Pin Current (Disable) vs Temperature* in *Typical Characteristics* section ... 8
- 変更 *TPS735 Dropout Voltage vs Output Current* in *Typical Characteristics* section ... 8
- Updated Equation 1 ... 14
- 変更 x-axis scale from "10 ms/div" to "10 µs/div" in 図 17 ... 15
- 変更 x-axis scale from "10 ms/div" to "10 µs/div" in 図 18 ... 15
- 変更 V_{OUT} starting value to 0 V in 図 19 ... 15
- Updated Equation 2 ... 17
- Updated Equation 3 ... 17
- 変更 DRV package designator from "SON" to "WSON" in *Measuring Points for T_T and T_B* ... 19
- 削除「*関連資料*」セクションのサーマル情報ドキュメントへの参照 ... 20

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改訂履歴 (continued)

Revision K (August, 2013) から Revision L に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 1
- 「*特長*」箇条書きの最初の項目 追加 1
- 「*特長*」箇条書きの4番目の項目を「1.2Vの固定出力」に 変更 1
- 「*特長*」箇条書きの8番目の項目 変更 1
- 「*特長*」箇条書きの最後の項目 変更 1
- 「*アプリケーション*」箇条書きの最後の項目 変更 1
- Changed *Pin Configuration and Functions* section; updated table format and pin descriptions to meet new standards 4
- Changed C_{NR} value notation from 0.01 µF to 10 nF throughout *Electrical Characteristics* 7
- Changed feedback voltage parameter values and measured test conditions 7
- Changed output current limit maximum specified value 7
- Changed power-supply rejection ratio typical specified values for 100 Hz, 10 kHz, and 100 kHz frequency test conditions 7
- 追加 note (1) to 図 1 8
- 変更 y-axis title for 図 6 8
- 変更 y-axis title for 図 7 8
- 変更 footnote for 図 13 10
- 変更 reference to noise-reduction capacitor (C_{NR}) to feed-forward capacitor (C_{FF}) in Transient Response 11
- 変更 noise-reduction capacitor to feed-forward capacitor in 図 16 13
- 変更 references to "noise-reduction capacitor" (C_{NR}) to "feed-forward capacitor" (C_{FF}) and section title from "Feedback Capacitor Requirements" to "Feed-forward Capacitor Requirements" in *Feed-Forward Capacitor Requirements* section 14
- 変更 C_{NR} value notation from 0.01 µF to 10 nF in *Output Noise* section 14

Revision J (May, 2011) から Revision K に変更 **Page**

- 追加 last sentence to first paragraph of *Startup and Noise Reduction Capacitor* section 11

Revision I (April, 2011) から Revision J に変更 **Page**

- Replaced the *Dissipation Ratings* with *Thermal Information* 6
- Revised conditions for *Typical Characteristics* to include statement about TPS73525 device availability 8
- 追加 *Estimating Junction Temperature* section 18
- Updated *Power Dissipation* section 19

Revision H (November, 2009) から Revision I に変更 **Page**

- Corrected typo in *Electrical Characteristics* table for V_{OUT} specification, DRV package test conditions, $V_{OUT} \leq 2.2V$ 7

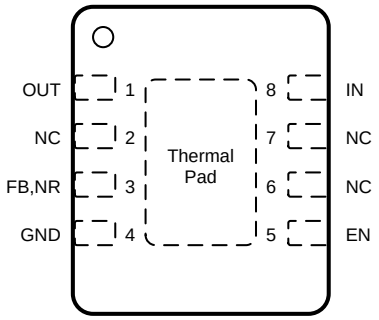
Revision G (March 2009) から Revision H に変更 **Page**

- 「*特長*」箇条書きの項目を変更し、280mVの非常に低いドロップアウトについて記載 1
- Changed dropout voltage typical specification from 250mV to 280mV 7

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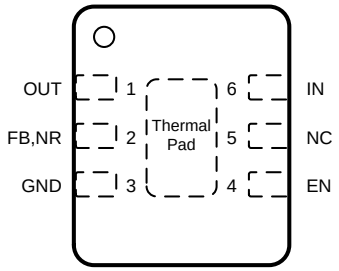
5 Pin Configuration and Functions

DRB Package
8-Pin SON With Exposed Thermal Pad
Top View



Not to scale

DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

NC - No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO			
	DRV	DRB		
IN	6	8	I	Input supply. A 0.1-µF to 1-µF, low ESR capacitor must be placed from this pin to ground near the device.
GND	3	4	—	Ground. The pad must be tied to GND.
EN	4	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. The EN pin can be connected to the IN pin if not used.
NR	2	3	—	This pin is only available for the fixed voltage versions. Connecting an external capacitor to this pin bypasses noise that is generated by the internal band gap and allows the output noise to be reduced to very low levels. The maximum recommended capacitor is 0.01 µF.
FB	2	3	I	This pin is only available for the adjustable version. The FB pin is the input to the control-loop error amplifier, and is used to set the output voltage of the device. This pin must not be left floating.
OUT	1	1	O	This pin is the output of the regulator. A small, 2.2-µF ceramic capacitor is required from this pin to ground to assure stability. The minimum output capacitance required for stability is 2 µF.
NC	5	2, 6, 7	—	Not internally connected.
Thermal pad			—	

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6 Specifications

6.1 Absolute Maximum Ratings

at –40°C ≤ T_J and T_A ≤ +125°C (unless otherwise noted). All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
V_{IN}	Voltage	–0.3	7	V
V_{EN}		–0.3	V_{IN} + 0.3	V
V_{FB}		–0.3	1.6	V
V_{OUT}		–0.3	V_{IN} + 0.3	V
I_{OUT}	Current	Internally limited		A
$P_{D(tot)}$	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed as *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
V_{OUT}	Output voltage	V_{FB}		6	V
I_{OUT}	Output current(1)	0		500	mA
T_A	Operating free-air temperature	–40		125	°C
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor		2		µF
C_{NR}	Noise reduction capacitor		10		nF
C_{FF}	Feed-forward capacitor (2)	3	22	1000	pF
R_2	Feedback resistor (2)		110		kΩ

(1) When operating at T_J near 125°C, $I_{OUT(min)}$ is 500 µA.
(2) Adjustable version only.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS735 (2)		UNIT
		DRB (SON)	DRV (WSON)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3)	52.2	65.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (4)	59.4	85.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	34.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter (5)	2	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter (6)	19.3	35.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (7)	11.8	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array.
  ii. DRV: The exposed pad is connected to the PCB ground layer through a 2 x 2 thermal via array. Due to size limitation of thermal pad, 0.8-mm pitch array is used which is off the JEDEC standard.
  (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  ii DRV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-in × 3-in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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6.5 Electrical Characteristics

over operating temperature range (–40°C ≤ T_J ≤ 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 10 nF (unless otherwise noted). For the adjustable version (TPS73501), V_{OUT} = 3 V. Typical values are at T_A = 25°C.

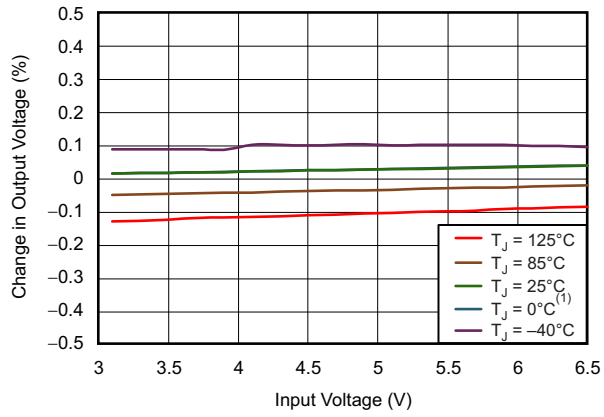
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)			2.7		6.5	V
V_{FB}	Internal reference (adjustable version only)	T_J = 25°C		1.196	1.208	1.220	V
V_{OUT}	Output voltage range (adjustable version only)			V_{FB}		6	V
	DC output accuracy(1)	1 mA ≤ I_{OUT} ≤ 500 mA, V_{OUT} + 0.5 V ≤ V_{IN} < 6.5 V	V_{OUT} > 2.2 V	–2%	±1%	2%	
			V_{OUT} ≤ 2.2 V	–3%	±1%	3%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	500 µA ≤ I_{OUT} ≤ 500 mA			0.005		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)	I_{OUT} = 500 mA			280	500	mV
I_{LIM}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 0.9 V V_{IN} ≥ 2.7 V		800	1170	1900	mA
I_{GND}	Ground pin current	10 mA ≤ I_{OUT} ≤ 500 mA			45	65	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0 V			0.15	1	µA
I_{FB}	Feedback pin current (adjustable version only)	$V_{OUT(nom)}$ = 1.2 V		–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V V_{OUT} = 2.85 V C_{NR} = 0.01 µF I_{OUT} = 100 mA	f = 100 Hz		66		dB
			f = 1k Hz		68		
			f = 10 kHz		44		
			f = 100 kHz		22		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	C_{NR} = 10 nF		11 × V_{OUT}		μV_{RMS}
			C_{NR} = none		95 × V_{OUT}		
t_{STR}	Start-up time	C_{NR} = none			45		µs
		C_{NR} = 1 nF			45		
		C_{NR} = 10 nF			50		
		C_{NR} = 47 nF			50		
$V_{EN(HI)}$	Enable high (enabled)			1.2			V
$V_{EN(LO)}$	Enable low (shutdown)					0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		
UVLO	Undervoltage lockout	V_{IN} rising		1.9	2.2	2.65	V
V_{hys}	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for this family of devices with $V_{OUT(nom)}$ < 2.8 V because the minimum V_{IN} = 2.7 V.

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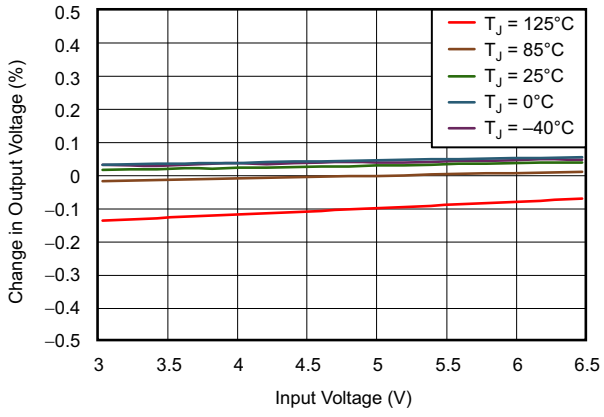
6.6 Typical Characteristics

over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN},C_{OUT} = 2.2 µF, C_{NR} = 10 nF. Typical values are at T_J = 25°C, (unless otherwise noted).



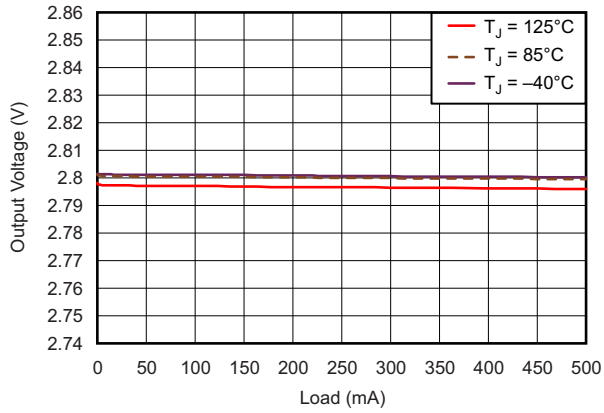
I_{OUT} = 100 mA

図 1. TPS735 Line Regulation



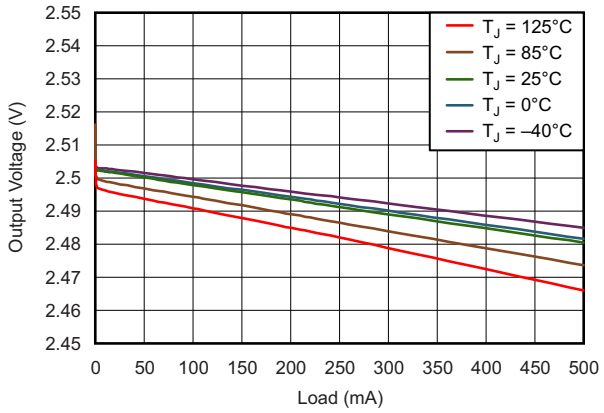
I_{OUT} = 100 mA

図 2. TPS735 Line Regulation



The y-axis range is ±2% of 2.8 V

図 3. TPS735 Load Regulation



The y-axis range is ±2% of 2.5 V

図 4. TPS735 Load Regulation

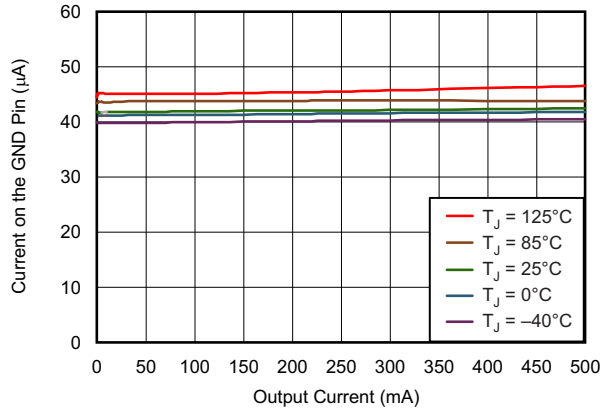


図 5. TPS735 Ground Pin Current vs Output Current

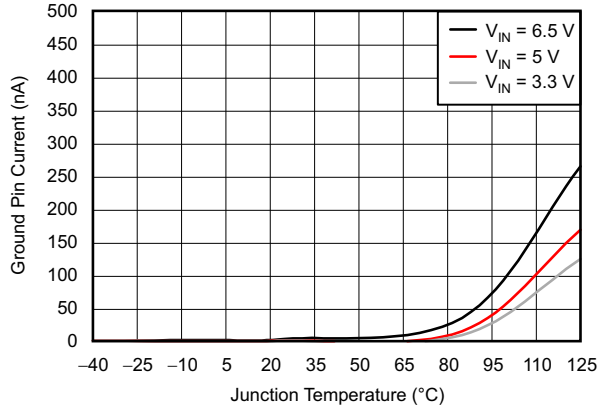


図 6. TPS735 Ground Pin Current (Disable) vs Temperature

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Typical Characteristics (continued)

over operating temperature range (T_J= –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN},C_{OUT} = 2.2 µF, C_{NR} = 10 nF. Typical values are at T_J = 25°C, (unless otherwise noted).

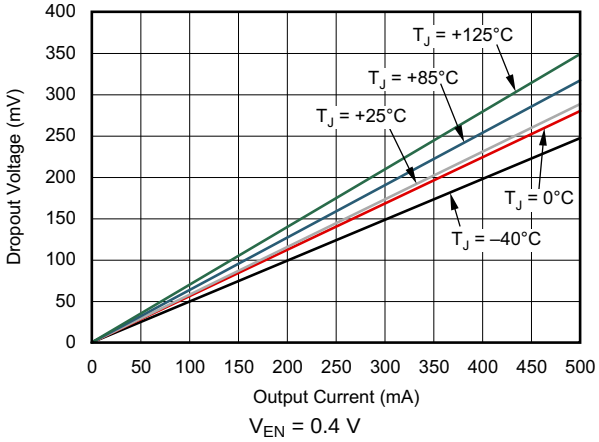


図 7. TPS735 Dropout Voltage vs Output Current

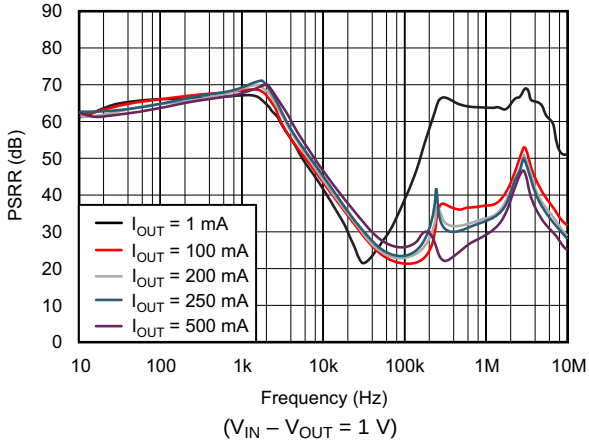


図 8. Power-Supply Ripple Rejection vs Frequency

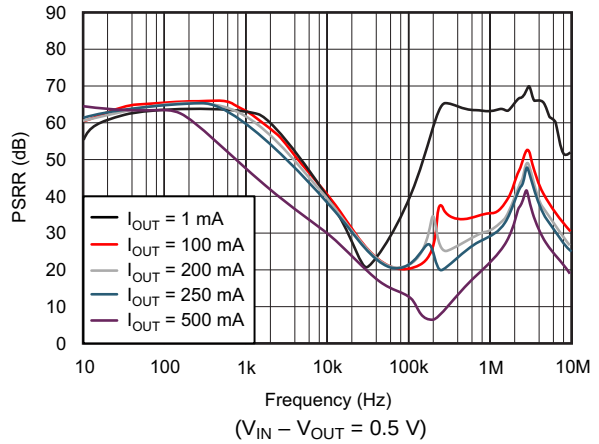


図 9. Power-Supply Ripple Rejection vs Frequency

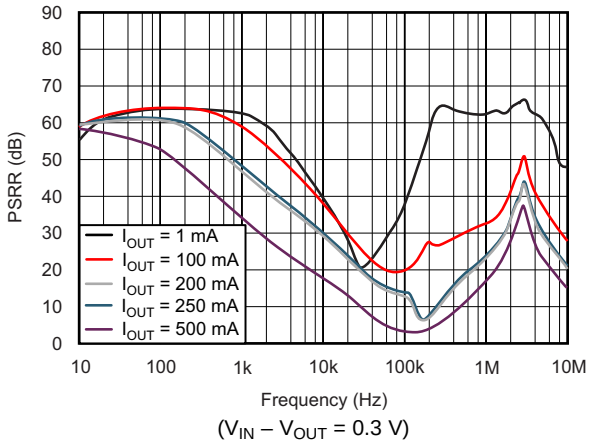


図 10. Power-Supply Ripple Rejection vs Frequency

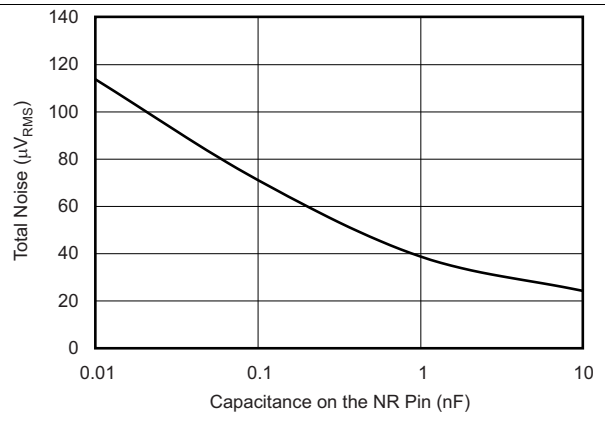


図 11. TPS73525 RMS Noise vs C_{NR}

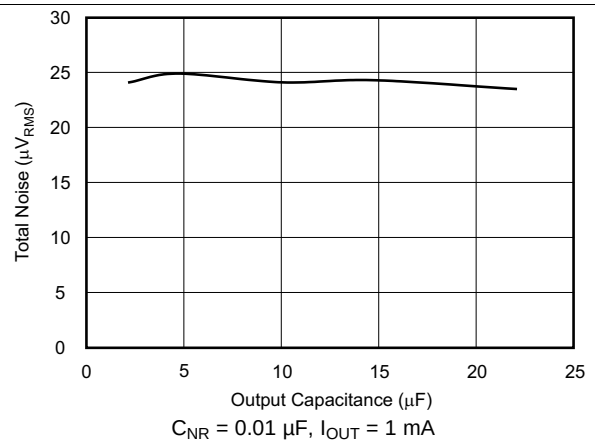


図 12. TPS735 RMS Noise vs C_{OUT}

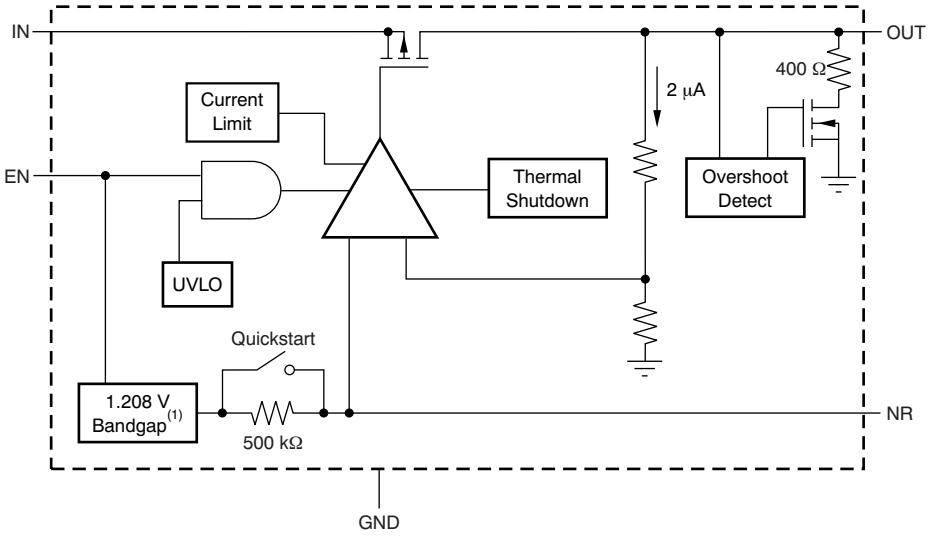
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7 Detailed Description

7.1 Overview

The TPS735 of low dropout (LDO) regulator combines the high performance required by radio frequency (RF) and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection and very low headroom ($V_{IN} – V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise that is generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at start-up. The combination of high performance and low ground current make the TPS735 device designed for portable applications. All versions have thermal and overcurrent protection and are specified from –40°C ≤ T_J ≤ +125°C.

7.2 Functional Block Diagrams



(1) The 1.2-V fixed voltage version has a 1-V band gap instead of a 1.208-V circuit.

図 13. Fixed Voltage Versions

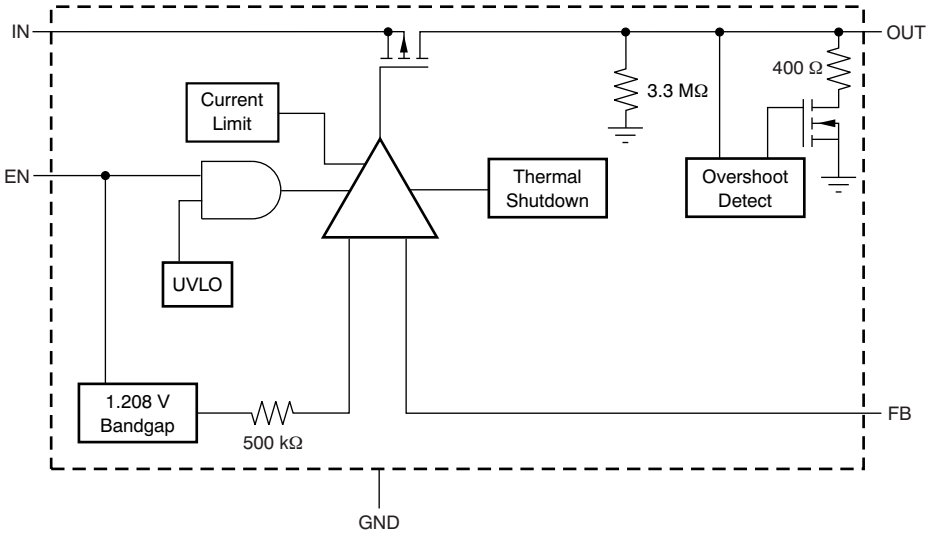


図 14. Adjustable Voltage Versions

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7.3 Feature Description

7.3.1 Internal Current Limit

The TPS735 internal current limit protects the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is independent of the output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

The PMOS pass element in the TPS735 device contains a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is expected, external limiting is appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can connect to the IN pin.

7.3.3 Dropout Voltage

The TPS735 device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance ($R_{(IN/OUT)}$) of the PMOS pass element. V_{DO} scales with the output current because the PMOS device operates like a resistor in dropout.

As with any linear regulator, PSRR and transient response degrades as (V_{IN} – V_{OUT}) approaches dropout. *Typical Characteristics* shows this effect; (see 図 8 through 図 10).

7.3.4 Start-Up and Noise Reduction Capacitor

Fixed voltage versions of the TPS735 use a quick-start circuit to charge the noise reduction (NR) capacitor (C_{NR}) if present (see *Functional Block Diagrams*). This architecture allows the combination of low output noise and fast start-up times. The NR pin is high impedance so a low-leakage C_{NR} capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, COG-type (NPO) dielectric ceramic capacitor is recommended for C_{NR} when used in environments where abrupt changes in temperature can occur.

For the fastest start-up, first apply V_{IN} , then drive the enable (EN) pin high. If EN is tied to IN, start-up is slower. See *Typical Applications* . The quick-start switch closes for approximately 135 μs. To ensure that C_{NR} is charged during the quick-start time, use a capacitor with a value of no more than 0.01 μF.

7.3.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the transient response duration. In the adjustable version, adding C_{FF} between the OUT and FB pins improves stability and transient response performance. The transient response of the TPS735 device is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. The pull-down device operates like a 400-Ω resistor to ground when enabled.

7.3.6 Undervoltage Lockout

The TPS735 device uses an undervoltage lockout circuit to disable the output until the internal circuitry is operates properly. The UVLO circuit contains a deglitch feature so that the UVLO ignores undershoot transients on the input if the transients are less than 50 μs in duration.

7.3.7 Minimum Load

The TPS735 device is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. If the output is below 500 μA and if the junction temperature is approximately 125°C, the output can increase enough to turn on the output pulldown. The output pulldown limits voltage drift to 5% (typically) but ground current can increase by approximately 50 μA. In most applications, the junction does not reach high temperatures at light loads because little power is dissipated. As a result, the specified ground current is valid at no load in most applications.

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Feature Description (continued)

7.3.8 Thermal Protection

Thermal protection disables the output when the junction temperature increases to approximately 165°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits the dissipation of the regulator and protects the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the thermal margin in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For reliable operation, trigger thermal protection at least 40°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS735 protects against overload conditions. This protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS735 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage previously exceeded the UVLO voltage and did not decrease below the UVLO threshold minus V_{hys}.
- The input voltage is greater than the nominal output voltage that is added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is within the specified range.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is equal to the input voltage minus the dropout voltage. The transient performance of the device degrades because the pass device is in a triode state and the LDO operates like a resistor. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{hys}, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

表 1 lists the conditions that result in different modes of operation.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUTnom} + V_{DO}$ and $V_{IN} >$ UVLO	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	UVLO $< V_{IN} < V_{OUTnom} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 165°C$
Disabled mode (any true condition disables the device)	$V_{IN} <$ UVLO $- V_{hys}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 165°C$

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS735 LDO regulator provides a design with an ultra-low noise, high PSRR, low-dropout linear regulation with a very small ground current (5 µA, typical).

The devices are stable with ceramic capacitors and have a dropout voltage of 280 mV at the full output rating of 500 mA. The features of the TPS735 device enables the LDO regulators to be used in a wide variety of applications with minimal design complexity.

8.2 Typical Applications

図 15 shows the basic circuit connections for fixed-voltage models. 図 16 shows the connections for the adjustable output version. R_1 and R_2 can be calculated for any output voltage using the formula in 図 16.

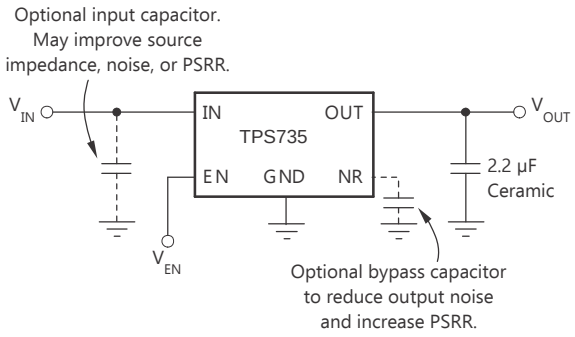


図 15. Typical Application Circuit for Fixed-Voltage Versions

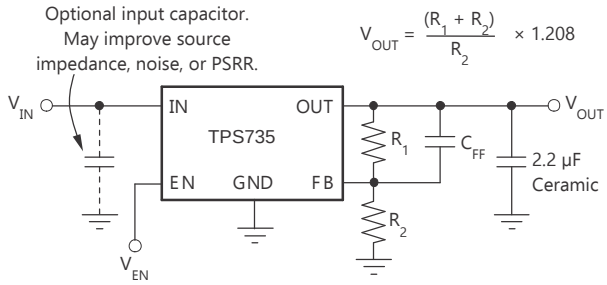


図 16. Typical Application Circuit for Adjustable-Voltage Versions

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Typical Applications (continued)

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1-μF to 1-μF low-equivalent series-resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher-value capacitor may be required if large, fast, rise-time load transients are expected, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be required to ensure stability.

TheTPS735 device is designed to be stable with standard ceramic output capacitors of values 2 μF or larger. X5R- and X7R-type capacitors are best because these capacitors feature minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor is < 1 Ω and, therefore, the output capacitor type must be ceramic or conductive polymer electrolytic.

8.2.1.2 Feed-Forward Capacitor Requirements

The feed-forward capacitor (C_{FF}), shown in 図 16, is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value between 3 pF to 1 nF can be used. Fixed-voltage versions have an internal 30-pF feed-forward capacitor that is quick-charged at start-up. Larger value capacitors improve noise slightly. The TPS735 device is stable in unity-gain configurations (the OUT pin is tied to the FB pin) without C_{FF}.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Noise

In most LDO regulators, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS735 device, the band gap does not contribute significantly to noise. Noise is dominated by the output resistor divider and the error-amplifier input. To minimize noise in a given application, use a 10-nF noise reduction capacitor. For the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that produces 2 μA of divider current has the same noise performance as a fixed voltage version with a C_{NR}. To further optimize noise, set the ESR of the output capacitor to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, which reduces the total output noise up to 10%. TI recommends a maximum capacitor value of 10 nF.

式 1 calculates the approximate integrated output noise from 10 Hz to 100 kHz with a C_{NR} value of 10 nF.

$$V_n\ (\mu V_{RMS}) = 11\,(\mu V_{RMS}\ /\ V) \times V_{OUT}\ (V) \tag{1}$$

The TPS735adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise is minimized according to the previously listed recommendations.

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Typical Applications (continued)

8.2.3 Application Curves

at $V_{IN} = V_{OUT(nom)} + 0.5$ V or 2.7 V, whichever is greater; $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2$ µF, $C_{NR} = 10$ nF, and $T_J = 25°C$ (unless otherwise noted)

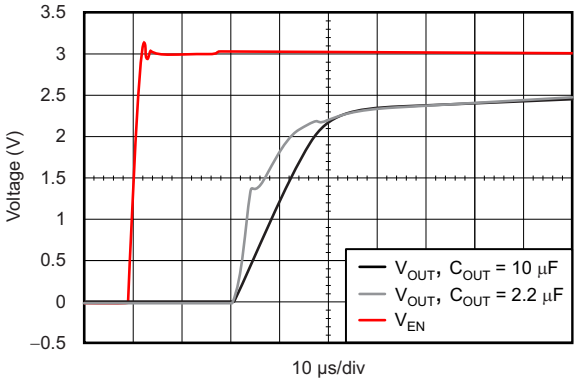


図 17. TPS735 Turnon Response ($V_{IN} = V_{EN}$)

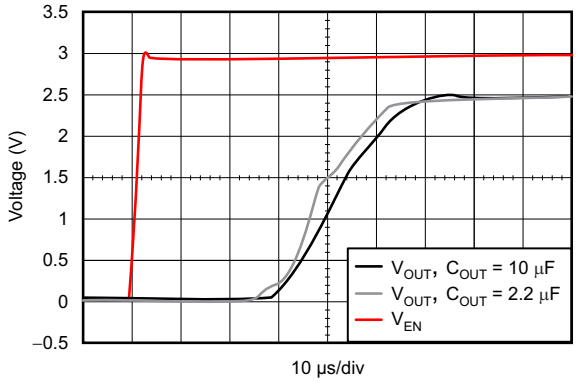


図 18. TPS735 Turnon Response Using EN

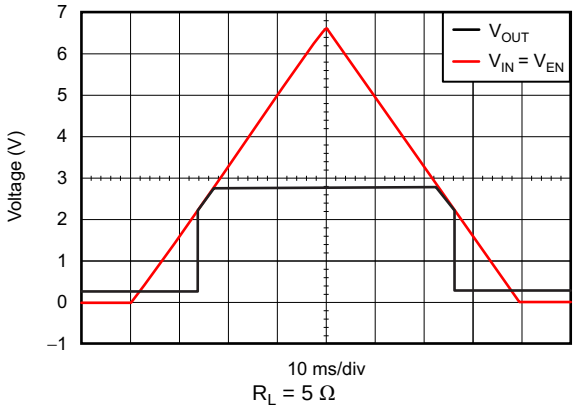


図 19. TPS73525 Power-Up and Power-Down ($V_{IN} = V_{EN}$)

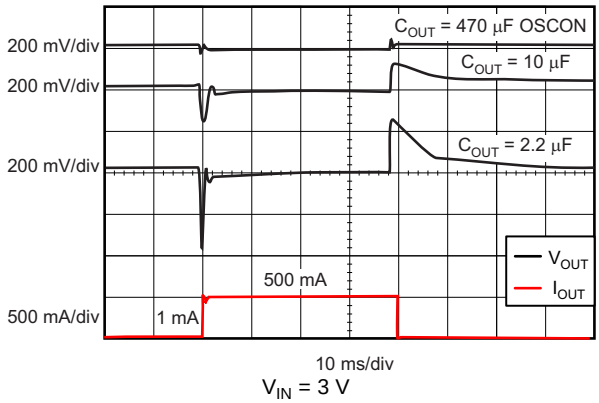


図 20. TPS735 Load Transient Response

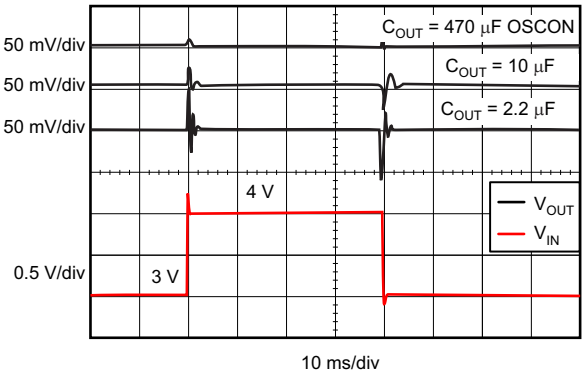


図 21. TPS735 Line Transient Response

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

10 Layout

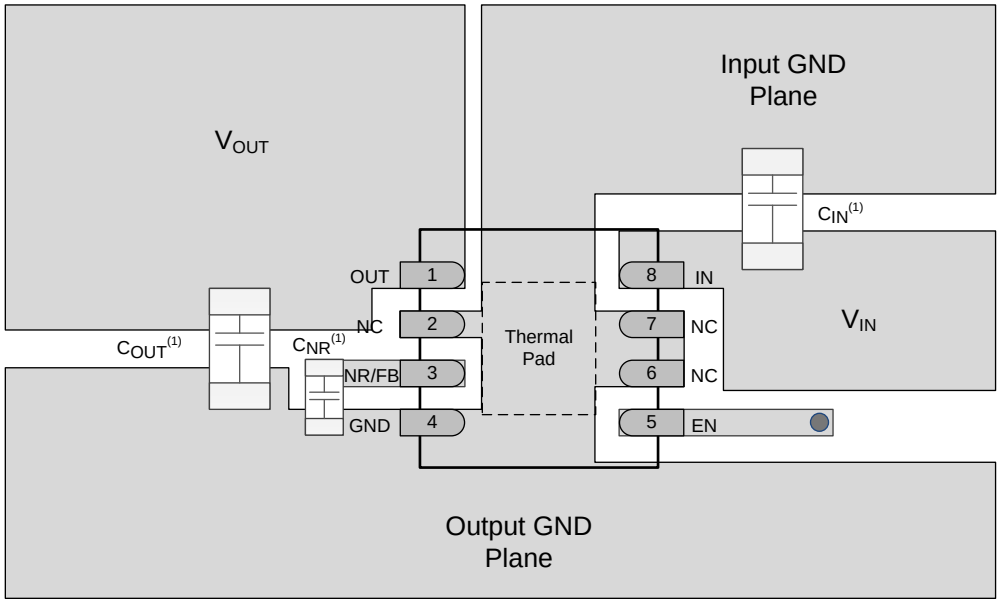
10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near to the respective LDO pin connections as possible. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and as a result, reduces load-current transients, minimizes noise, and increases circuit stability. TI recommends using a ground reference plane, and is embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane ensures accuracy of the output voltage, shields the LDO from noise, and operates similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is required to meet thermal requirements.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

10.2 Layout Example



(1) C_{IN} and C_{OUT} are 0603 capacitors and C_{NR} is a 0402 capacitor. The footprint is shown to scale with package size.

図 22. TPS735 Fixed Version Layout Reference Diagram

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10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, which presents different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* section. Heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation can be approximated by the product of the output current and the voltage drop across the output pass element, as 式 2 shows.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

注

When the device is used in a condition of high input and low output voltages, P_D can exceed the junction temperature rating even when the ambient temperature is at room temperature.

式 3 is an example calculation for the power dissipation (P_D) of the DRB package.

$$P_D = (6.5\ V - 1.2\ V) \times 500\ mA = 2.65\ W \quad (3)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output performance.

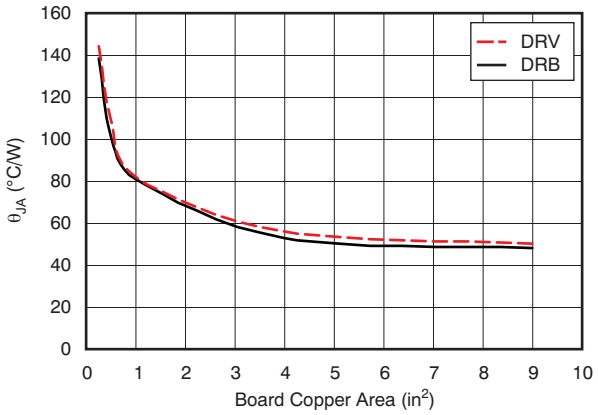
On the DRB package, the primary conduction path for heat is through the exposed thermal pad to the PCB. The pad can be connected to ground or left floating. The pad must be attached to an appropriate amount of copper PCB area to ensure that the device does not overheat. The maximum allowable junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. 式 4 calculates the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(125°C - T_A)}{P_D} \quad (4)$$

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Power Dissipation (continued)

図 23 estimates the maximum $R_{\theta JA}$ and the minimum amount of PCB copper area required to heat sink.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

図 23. θ_{JA} vs Board Size

図 23 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and must not be used to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

10.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as the table shows, the junction temperature can be estimated with corresponding formulas (式 5), which are more accurate than the value of T_J through calculation with θ_{JA}.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

where:

- P_D is the power dissipation calculated with 式 2,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface (as shown in 図 25). (5)

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see *Using New Thermal Metrics*, available for download at www.ti.com.

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Estimating Junction Temperature (continued)

According to 図 24, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) do not depend on the copper area. Using Ψ_{JT} or Ψ_{JB} with 式 5 can estimate T_J by measuring T_T or T_B on an application board.

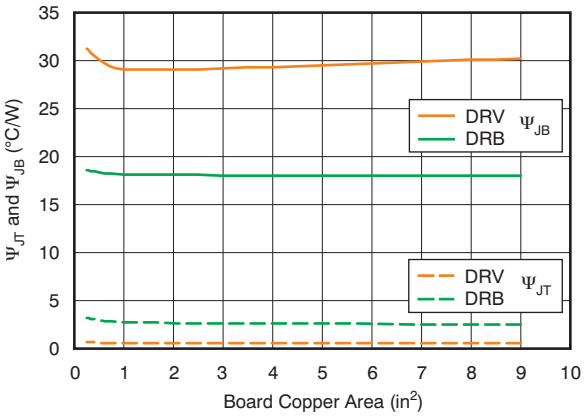
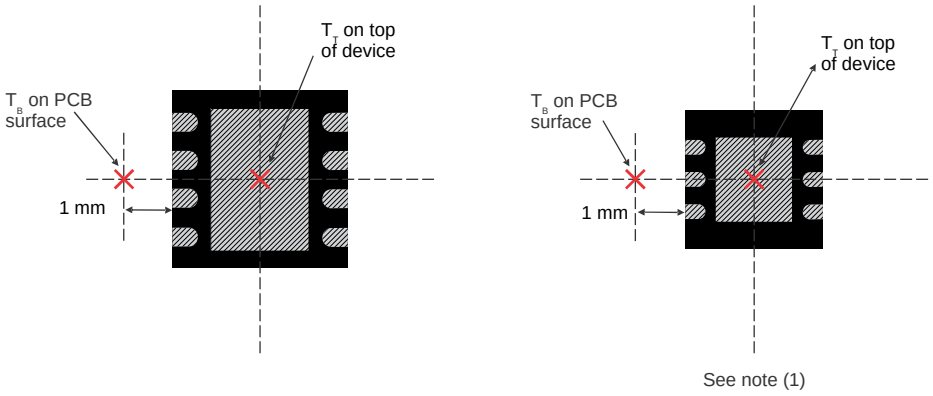


図 24. Ψ_{JT} and Ψ_{JB} vs Board Size



(a) Example DRB (SON) Package Measurement (b) Example DRV (WSON) Package Measurement

(1) Power dissipation may limit operating range. See *Thermal Information* .

図 25. Measuring Points for T_T and T_B

10.5 Package Mounting

Solder pad footprint recommendations for the TPS735 device is available from the TI website at www.ti.com.

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS735を使用する回路の性能の初期評価に役立てるため、2つの評価モジュール(EVM)を利用可能です。TPS73501EVM-276評価モジュールおよびTPS73525EVM-276評価モジュール(および関連するユーザー・ガイド)は、TI Webサイトのプロダクト・フォルダから請求するか、TI eStoreから直接お求めになれます。

11.1.2 デバイスの項目表記

表 2. デバイスの項目表記(1)

製品名	V_{OUT}
TPS735**xx(x)** ***yyy z***	**xx(x)**は公称出力電圧です。出力電圧の分解能が100mVの場合、注文番号に2桁が使用されます。それ以外の場合は3桁が使用されます(例: 33 = 3.3V、125 = 1.25V)。 **yyy**はパッケージ指定子です。 **Z**はテープ・アンド・リール数量です(R = 3,000、T = 250)。 **01**は可変出力バージョンです。

(1) 最新のパッケージおよび発注情報については、このデータシートの末尾にあるパッケージ・オプションについての付録を参照するか、TIのWebサイト(www.ti.com)をご覧ください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『TPS735EVM-276ユーザー・ガイド』*

11.3 商標

All trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73501DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK
TPS73501DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK
TPS73501DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK
TPS73501DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK
TPS73501DRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK
TPS73501DRBTG4.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK
TPS73501DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SDR
TPS73501DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SDR
TPS73501DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SDR
TPS73501DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SDR
TPS73501DRVTG4.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS73512DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT
TPS73512DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT
TPS73512DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT
TPS73512DRBRG4.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT
TPS73512DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT
TPS73512DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT
TPS73515DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH
TPS73515DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH
TPS73515DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH
TPS73515DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH
TPS73515DRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH
TPS73515DRBTG4.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH
TPS73525DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM
TPS73525DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM
TPS73525DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM
TPS73525DRBRG4.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM
TPS73525DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM
TPS73525DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73525DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NSW
TPS73525DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NSW
TPS73525DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NSW
TPS73525DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NSW
TPS73527DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK
TPS73527DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK
TPS73527DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK
TPS73527DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK
TPS73527DRVTG4.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS735285DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAW
TPS735285DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAW
TPS735285DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAW
TPS735285DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAW
TPS73533DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY
TPS73533DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY
TPS73533DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY
TPS73533DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY
TPS73533DRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY
TPS73533DRBTG4.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY
TPS73533DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVY
TPS73533DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVY
TPS73533DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVY
TPS73533DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVY
TPS73534DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTU
TPS73534DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTU
TPS73534DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTU
TPS73534DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS735 :

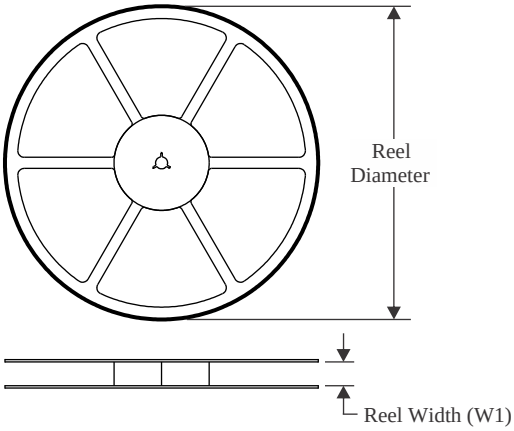
- Automotive : TPS735-Q1

NOTE: Qualified Version Definitions:

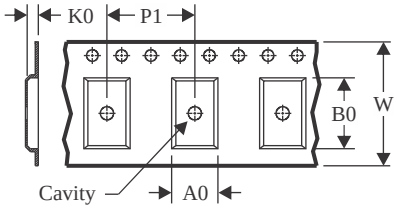
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

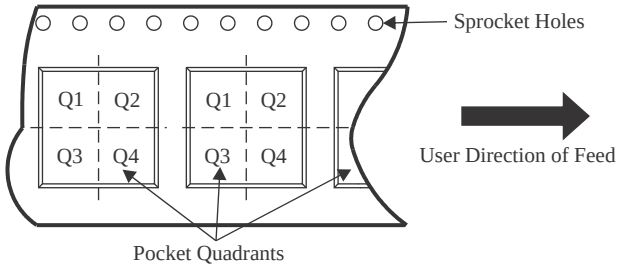


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

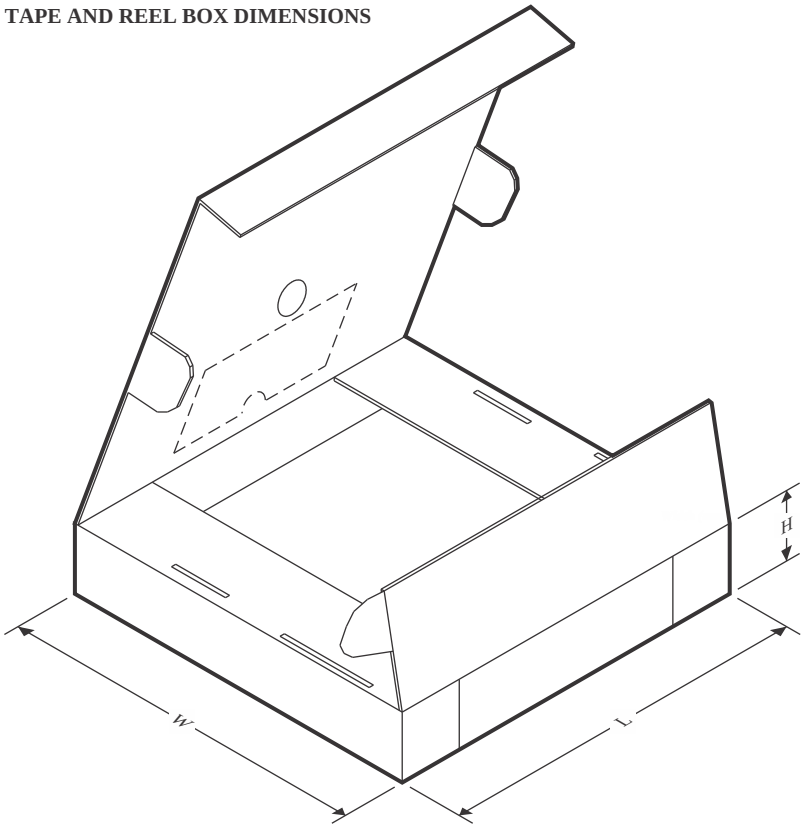


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73501DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRBTG4	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73501DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73501DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73512DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73512DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73512DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBTG4	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73525DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73527DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73527DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS735285DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS735285DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73533DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRBTG4	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73533DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73533DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73534DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73534DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



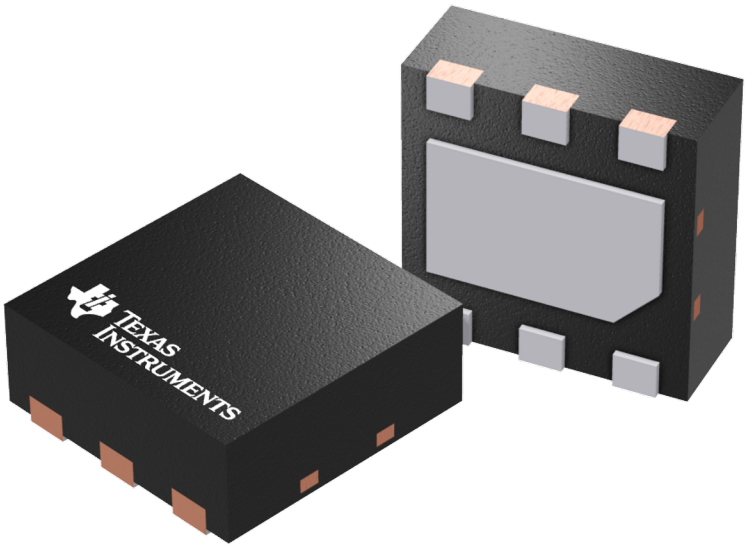
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73501DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS73501DRBT	SON	DRB	8	250	338.0	355.0	35.0
TPS73501DRBTG4	SON	DRB	8	250	338.0	355.0	35.0
TPS73501DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73501DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS73501DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS73512DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS73512DRBRG4	SON	DRB	8	3000	353.0	353.0	32.0
TPS73512DRBT	SON	DRB	8	250	213.0	191.0	35.0
TPS73515DRBR	SON	DRB	8	3000	338.0	355.0	35.0
TPS73515DRBT	SON	DRB	8	250	338.0	355.0	35.0
TPS73515DRBTG4	SON	DRB	8	250	338.0	355.0	35.0
TPS73525DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS73525DRBRG4	SON	DRB	8	3000	353.0	353.0	32.0
TPS73525DRBT	SON	DRB	8	250	338.0	355.0	35.0
TPS73525DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73525DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS73527DRVR	WSON	DRV	6	3000	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73527DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS735285DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS735285DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73533DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS73533DRBT	SON	DRB	8	250	338.0	355.0	35.0
TPS73533DRBTG4	SON	DRB	8	250	338.0	355.0	35.0
TPS73533DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73533DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS73533DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73534DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS73534DRBT	SON	DRB	8	250	213.0	191.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



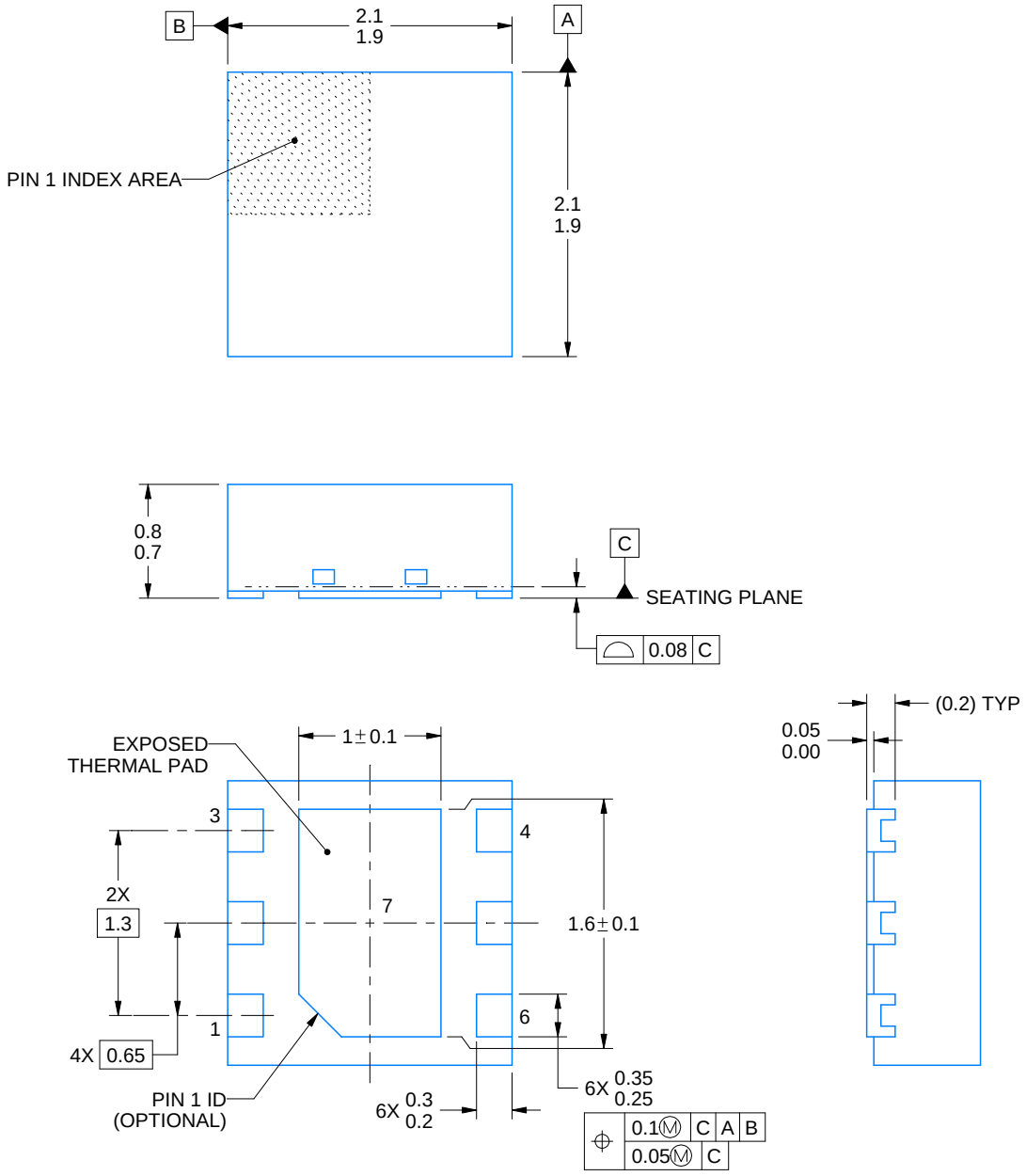
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

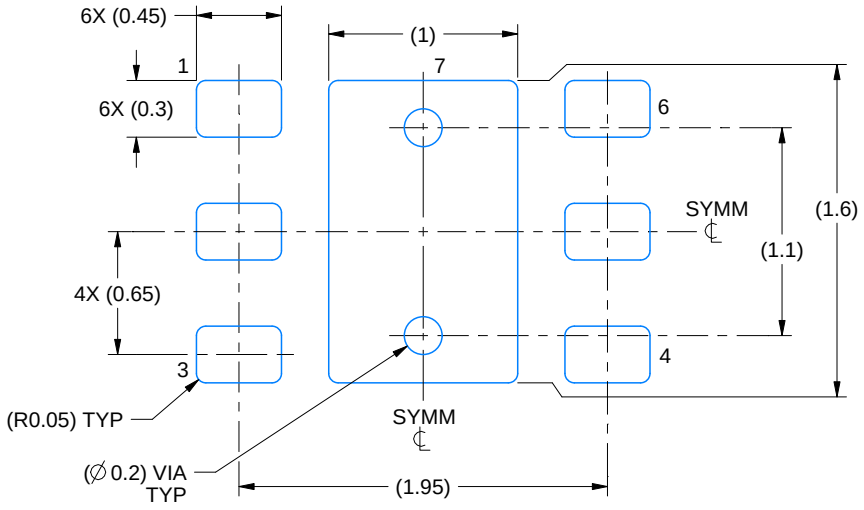
PLASTIC SMALL OUTLINE - NO LEAD



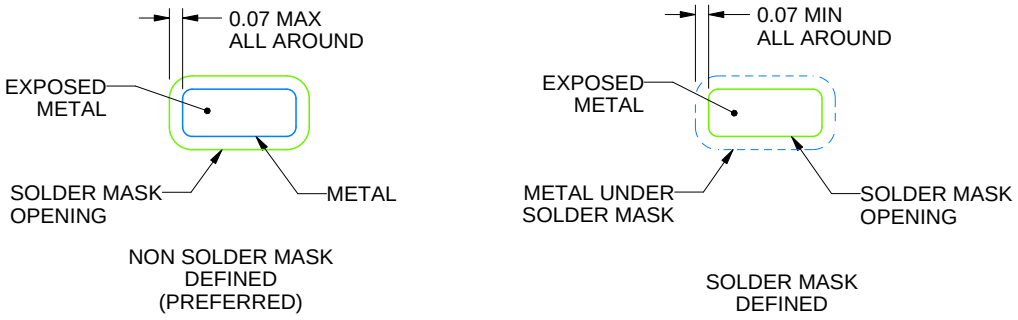
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

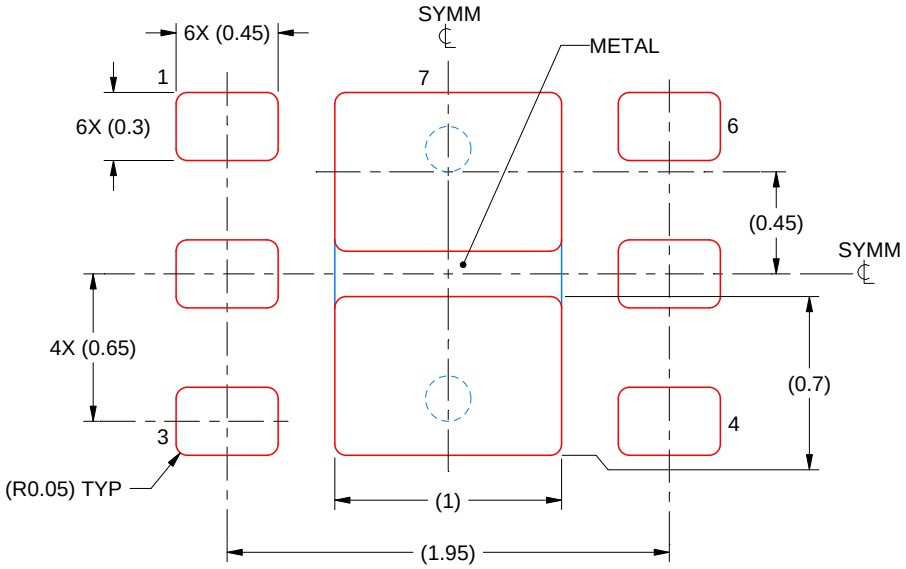


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

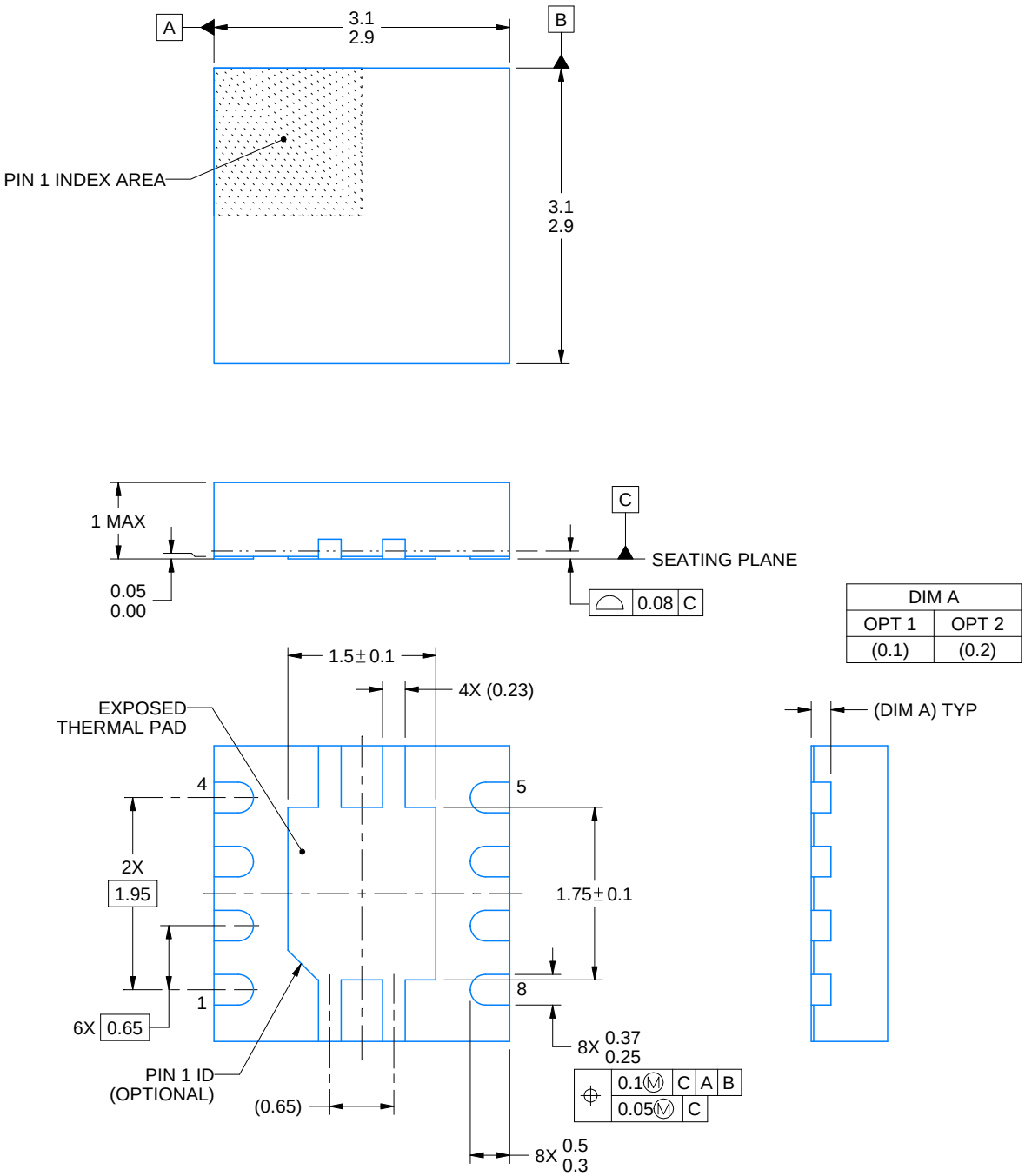
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

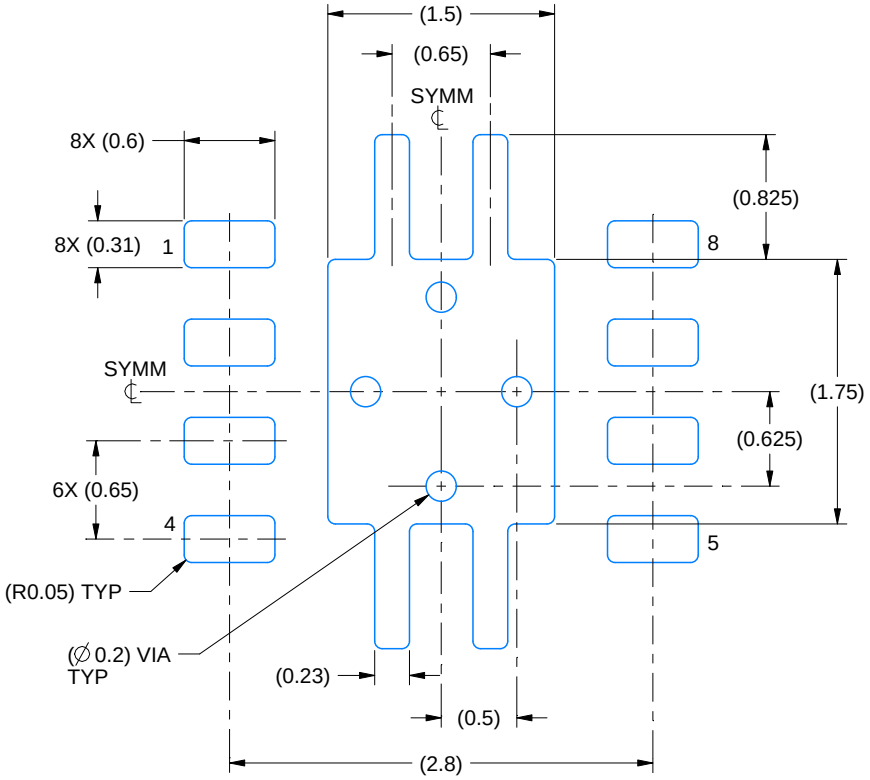
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

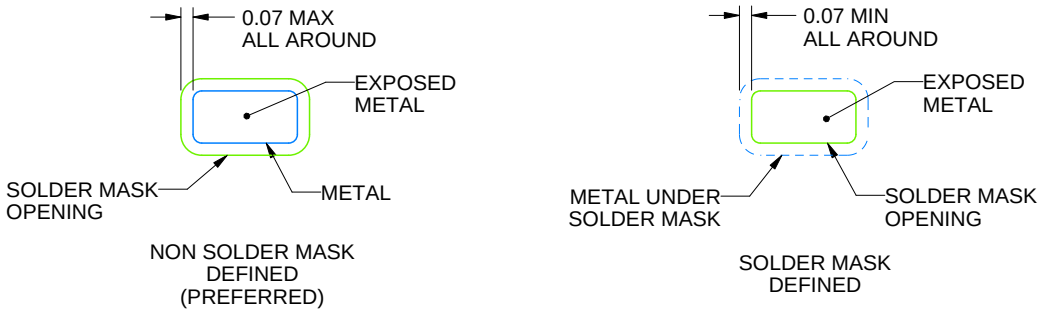
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

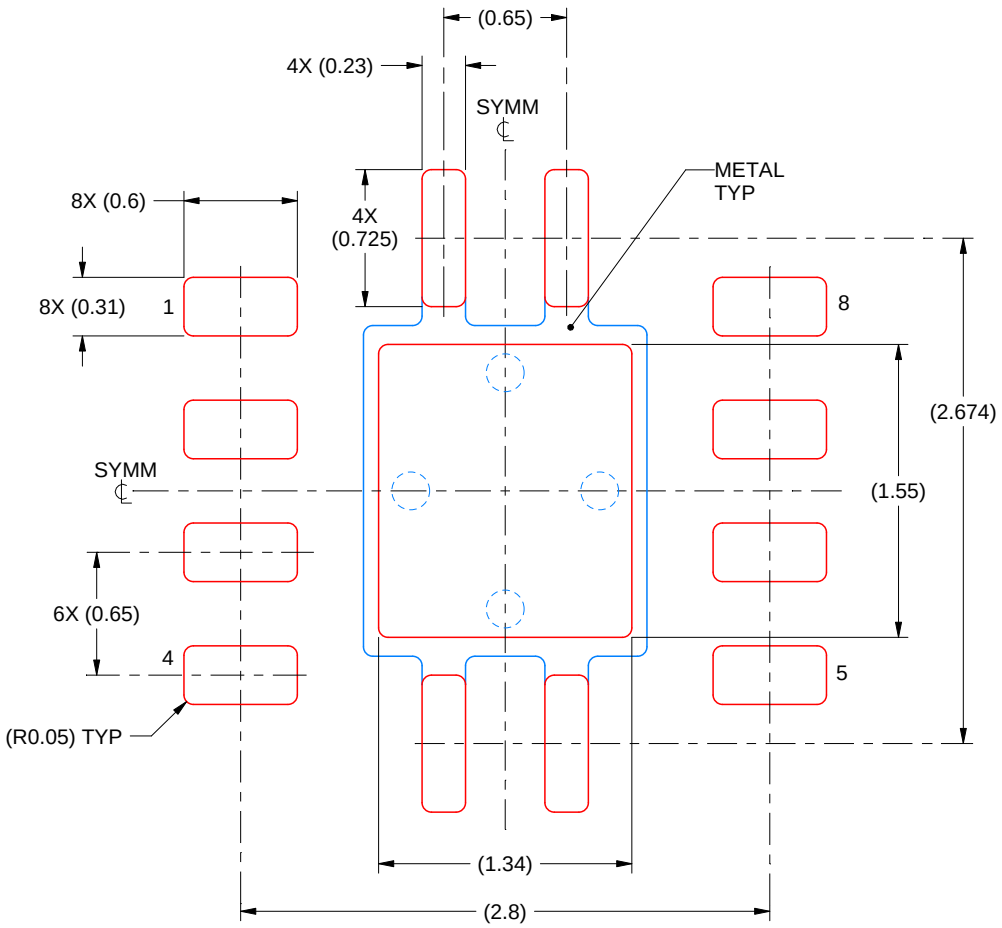


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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