TEXAS INSTRUMENTS
TPS745
JAJSF57A – APRIL 2018 – REVISED DECEMBER 2018

# TPS745 小型パッケージで500mA、高精度、パワー・グッド出力搭載の可変LDO

## 1 特長

- 入力電圧範囲: 1.5V～6.0V
- 可変出力電圧
  - 0.55V～5.5V
- 非常に低いドロップアウト
  - 500mAで130mV（最大値）($3.3V_{OUT}$)
- 高い出力精度：0.7%（標準値）および1%（全温度範囲での最大値）
- オープン・ドレインのパワー・グット出力
- $I_Q$: 25µA (標準値)
- $V_{OUT}$が単調増加するソフトスタートを内蔵
- パッケージ
  - 2mm×2mm WSON-6 (DRV)
- アクティブ出力放電

## 2 アプリケーション

- セットトップ・ボックス、ゲーム機
- ホーム・シアターおよびエンターテインメント
- デスクトップ、ノートブック、ウルトラブック
- プリンタ
- サーバー
- サーモスタットおよび照明制御
- 電子POS (EPOS)

## 3 概要

TPS745は可変の500mA低ドロップアウト(LDO)レギュレータで、パワー・グッド機能が搭載されています。このデバイスは、小型の6ピン、2mm×2mmのWSONパッケージで供給され、静止電流が非常に少なく、ラインおよび負荷の過渡特性が高速です。TPS745はドロップアウトが500mAで130mVと非常に低く、システムの電力効率向上に役立ちます。

TPS745は1.5V～6.0Vの入力電圧範囲に対応し、出力電圧を外部から0.55V～5.5Vの範囲で変更でき、広範なアプリケーション用に最適化されています。出力電圧が低いため、このLDOはコア電圧が低い現代のマイクロコントローラの電源として使用できます。

TPS745にはパワー・グッド出力(PG)があり、フィードバック・ピンの電圧を監視して、出力電圧のステータスを表示します。EN入力およびPG出力を使用して、システムの複数の電源をシーケンシングできます。

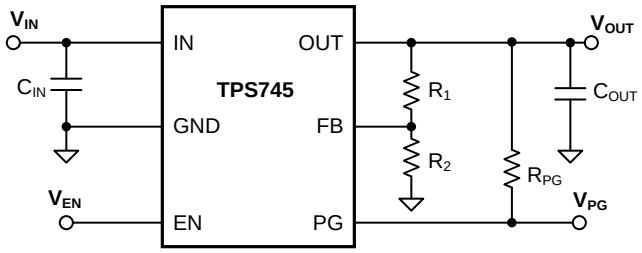
TPS745は小さなセラミック出力コンデンサで安定するため、ソリューション全体のサイズを小さくできます。高精度のバンドギャップおよびエラー・アンプにより、25°Cで0.7%（最大値）、全温度範囲(85°C)で1%（最大値）の高精度を実現しています。このデバイスにはサーマル・シャットダウン、電流制限、低電圧誤動作防止(UVLO)機能が内蔵されています。TPS745には内部フォールドバック電流制限があり、短絡発生時の熱発散を低減するため役立ちます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ（公称） |
|---|---|---|
| TPS745 | WSON (6) | 2.00mm×2.00mm |

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

**代表的なアプリケーション**




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# 目次

**1** 特長 ... 1
**2** アプリケーション ... 1
**3** 概要 ... 1
**4** 改訂履歴 ... 2
**5** **Pin Configuration and Functions** ... 3
**6** **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Typical Characteristics ... 7
**7** **Detailed Description** ... 14
7.1 Overview ... 14
7.2 Functional Block Diagram ... 14
7.3 Feature Description ... 14
7.4 Device Functional Modes ... 16
**8** **Application and Implementation** ... 17
8.1 Application Information ... 17
8.2 Typical Application ... 22
**9** **Power Supply Recommendations** ... 24
**10** **Layout** ... 24
10.1 Layout Guidelines ... 24
10.2 Layout Example ... 24
**11** デバイスおよびドキュメントのサポート ... 25
11.1 ドキュメントのサポート ... 25
11.2 ドキュメントの更新通知を受け取る方法 ... 25
11.3 コミュニティ・リソース ... 25
11.4 商標 ... 25
11.5 静電気放電に関する注意事項 ... 25
11.6 Glossary ... 25
**12** メカニカル、パッケージ、および注文情報 ... 25

## 4 改訂履歴

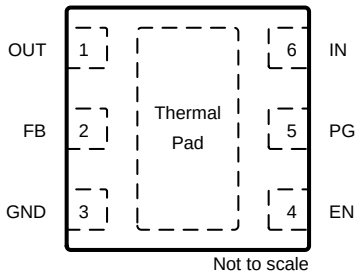
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- ドキュメントのステータスを「事前情報」から「量産データ」に 変更 ... 1


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# 5 Pin Configuration and Functions

**DRV Package**
**6-Pin Adjustable WSON**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 4 | Input | Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the LDO into shutdown mode. |
| FB | 2 | — | This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO. |
| GND | 3 | — | Ground pin |
| IN | 6 | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the output of the device as possible. |
| OUT | 1 | Output | Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible. |
| PG | 5 | Output | Power-good output |
| Thermal pad | Pad | — | Connect the thermal pad to a large area GND plane for improved thermal performance. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply, $V_{IN}$ | –0.3 | 6.5 | V |
| | Enable, $V_{EN}$ | –0.3 | 6.5 | |
| | Feedback, $V_{FB}$ | –0.3 | 2 | |
| | Power-good, $V_{PG}$ | –0.3 | 6.5 | |
| | Output, $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3(2) | |
| Current | Power-good current | | ±10 | mA |
| Temperature | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) The absolute maximum rating is $V_{IN}$ + 0.3V or 6.5 V, whichever is smaller.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM ispossible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM ispossible with the necessary precautions.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 1.5 | | 6.0 | V |
| $V_{OUT}$ | Output voltage | 0.55 | | 5.5 | V |
| $I_{OUT}$ | Output current | 0 | | 500 | mA |
| $C_{IN}$ | Input capacitor | 1 | | | µF |
| $C_{OUT}$ | Output capacitor(1) | 1 | | 220 | µF |
| $V_{EN}$ | Enable voltage | 0 | | 6.0 | V |
| $f_{EN}$ | Enable toggle frequency | | | 10 | kHz |
| $V_{PG}$ | PG voltage | 0 | | 6.0 | V |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

(1) Minimum derated capacitance of 0.47 µF is required for stability


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## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS745 DRV (WSON) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 80.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 98.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 45.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 20.8 | °C/W |

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at operating temperature range ($T_J$ = –40°C to +125°C),$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever isgreater), $I_{OUT}$ = 1 mA, $V_{EN}$ =$V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 uF(unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback voltage | $T_J$ = 25°C | | | 0.55 | | V |
| | Output accuracy(1) | $T_J$ = 25°C | | –0.7% | | 0.7% | |
| | | –40°C ≤ $T_J$ ≤ +85°C | | –1% | | 1% | |
| | | –40°C ≤ $T_J$ ≤ +125°C | | –1.5% | | 1.5% | |
| | Line regulation | $V_{OUT(NOM)}$ + 0.5 V(2) ≤ $V_{I N}$ ≤ 6.0 V | | | 2 | 7.5 | mV |
| | Load regulation | 0.1 mA ≤ $I_{OUT}$ ≤ 500 mA, $V_{IN}$ ≥ 2.0 V | | | 0.030 | | V/A |
| $I_{GND}$ | Ground current | $I_{OUT}$ = 0 mA | $T_J$ = 25°C | 10 | 25 | 31 | µA |
| $I_{GND}$ | Ground current | | –40°C ≤ $T_J$ ≤ +125°C | | | 35 | µA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ ≤ 0.3 V, 1.5 V ≤ $V_{IN}$ ≤ 6.0 V | | | 0.1 | 1 | µA |
| $I_{FB}$ | Feedback pin current | | | | 0.01 | 0.1 | µA |
| $I_{CL}$ | Output current limit | $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V | $V_{OUT}$ = $V_{OUT(NOM)}$ – 0.2 V, $V_{OUT}$ < 1.5 V | 530 | 720 | 865 | mA |
| | | | $V_{OUT}$ = 0.9 V × $V_{OUT(NOM)}$, $V_{OUT}$ ≥ 1.5 V | 530 | 720 | 865 | |
| $I_{SC}$ | Short-circuit current limit | $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V | $V_{OUT}$ = 0 V | | 350 | | mA |
| $V_{DO}$ | Dropout voltage | $I_{OUT}$ = 500 mA, –40°C ≤ $T_J$ ≤ +125°C, $V_{OUT}$ = 0.95 × $V_{OUT(NOM)}$ | 0.65 V ≤ $V_{OUT}$ < 0.8 V | | 720 | 880 | mV |
| | | | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | 585 | 750 | |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | 420 | 570 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | 285 | 400 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | 180 | 235 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | 140 | 185 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | 102 | 140 | |
| | | | 3.3 V ≤ $V_{OUT}$ ≤ 5.5 V | | 95 | 130 | |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V, $I_{OUT}$ = 50 mA | f = 1 kHz | | 50 | | dB |
| | | | f = 100 kHz | | 45 | | |
| | | | f = 1 MHz | | 30 | | |
| $V_n$ | Output noise voltage | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 0.9 V | | | 53 | | $\mu V_{RMS}$ |
| $V_{UVLO}$ | Undervoltage lockout | $V_{IN}$ rising | | 1.21 | 1.33 | 1.47 | V |
| | | $V_{IN}$ falling | | 1.17 | 1.29 | 1.42 | V |
| $V_{UVLO, HYST}$ | Undervoltage lockout hysteresis | $V_{IN}$ Hysteresis | | | 40 | | mV |
| $t_{STR}$ | Startup time | From EN low-to-high transition to $V_{OUT}$ = $V_{OUT(NOM)}$ × 95% | | | 500 | | µs |

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included
(2) $V_{IN}$ = 1.5V for $V_{OUT}$ < 1.0 V

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## Electrical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C),$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever isgreater), $I_{OUT}$ = 1 mA, $V_{EN}$ =$V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 uF(unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{EN(HI)}$ | EN pin high voltage | | 1.0 | | | V |
| $V_{EN(LO)}$ | EN pin low voltage | | | | 0.3 | V |
| $I_{EN}$ | Enable pin current | $V_{IN}$ = EN = 6.0 V | | 10 | | nA |
| $R_{PULL\ DOWN}$ | Pulldown resistance | $V_{IN}$ = 6.0 V | | 95 | | Ω |
| $PG_{HTH}$ | PG high threshold | $V_{OUT}$ increasing | 89 | 94 | 95 | %$V_{OUT}$ |
| $PG_{LTH}$ | PG low threshold | $V_{OUT}$ decreasing | 87 | 92 | 93 | %$V_{OUT}$ |
| $V_{OL(PG)}$ | PG pin low-level output voltage | $V_{IN}$ ≥ 1.5 V, $I_{SINK}$ = 1 mA | | | 300 | mV |
| $V_{OL(PG)}$ | PG pin low-level output voltage | $V_{IN}$ ≥ 2.75 V, $I_{SINK}$ = 2 mA | | | 300 | |
| $I_{lkg(PG)}$ | PG pin leakage current | $V_{OUT}$ > $PG_{HTH}$, $V_{PG}$ = 6.0 V | | | 300 | nA |
| $T_{SD}$ | Thermal shutdown | Shutdown, temperature increasing | | 170 | | °C |
| | | Reset, temperature decreasing | | 155 | | |

## 6.6 Timing Requirements

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PGDH}$ | PG delay time rising(1) | Time from 92% VOUT to 20% of PG | 135 | 165 | 178 | µs |
| $t_{PGDL}$ | PG delay time falling(1) | Time from 90% $V_{OUT}$ to 80% of PG | 1.5 | 7 | 10 | µs |

(1) Output overdrive = 10%


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## 6.7 Typical Characteristics

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)

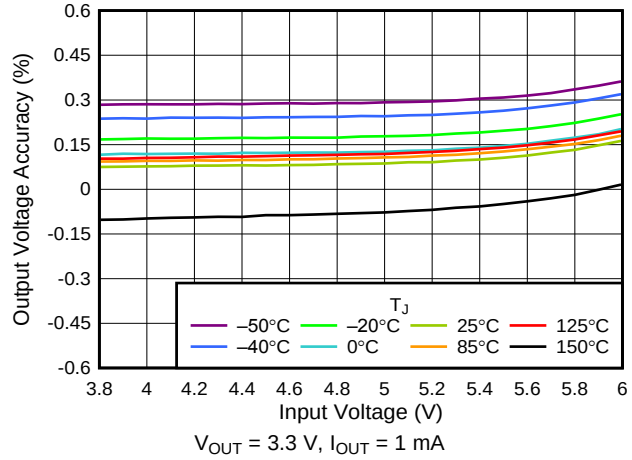



**図 1. 3.3-V Line Regulation vs $V_{IN}$**

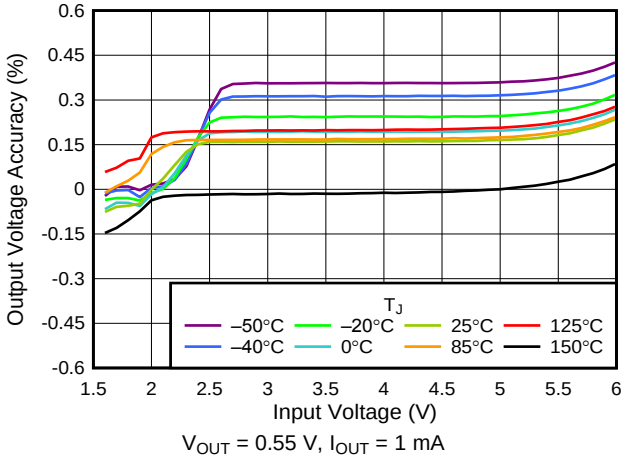



**図 2. 0.55-V Line Regulation vs $V_{IN}$**

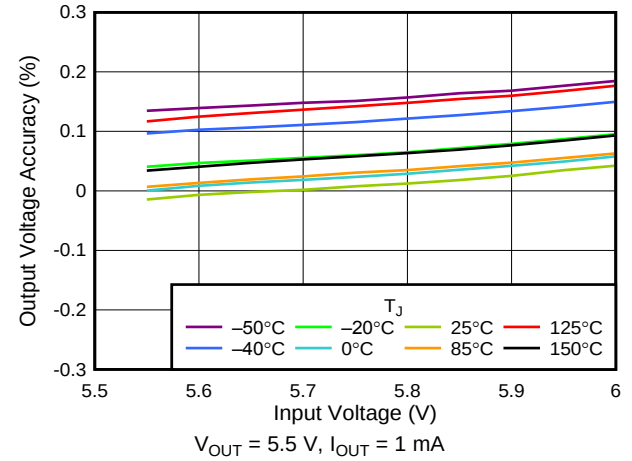



**図 3. 5.5-V Line Regulation vs $V_{IN}$**

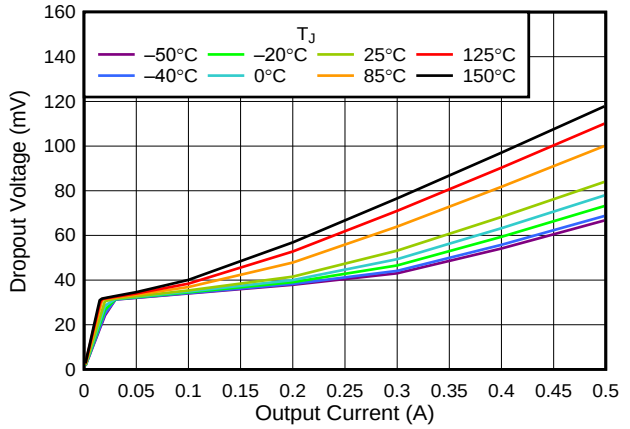



**図 4. 3.3-V Dropout Voltage vs $I_{OUT}$**

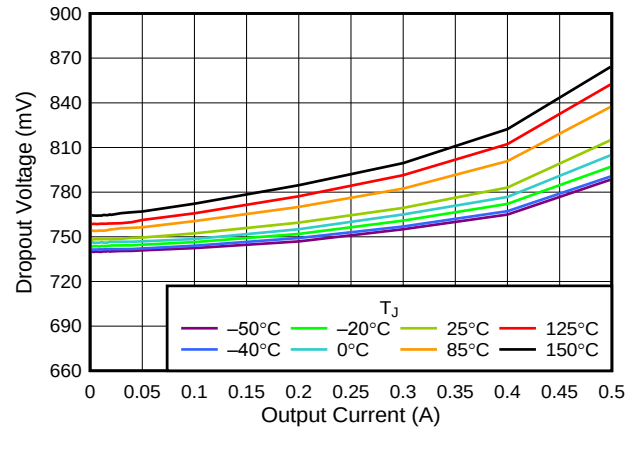



**図 5. 0.55-V Dropout Voltage vs $I_{OUT}$**

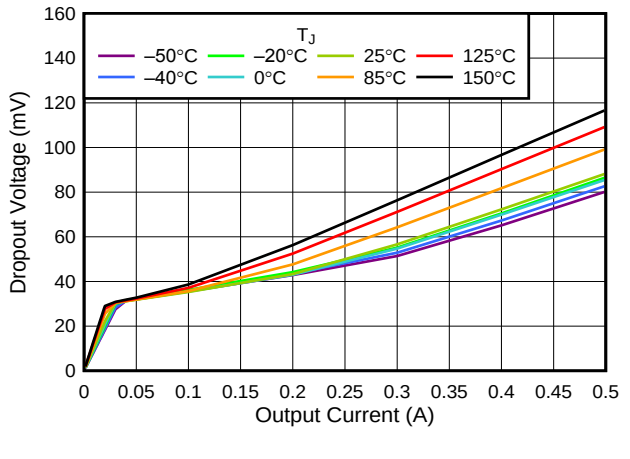



**図 6. 5.5-V Dropout Voltage vs $I_{OUT}$**

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## Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)

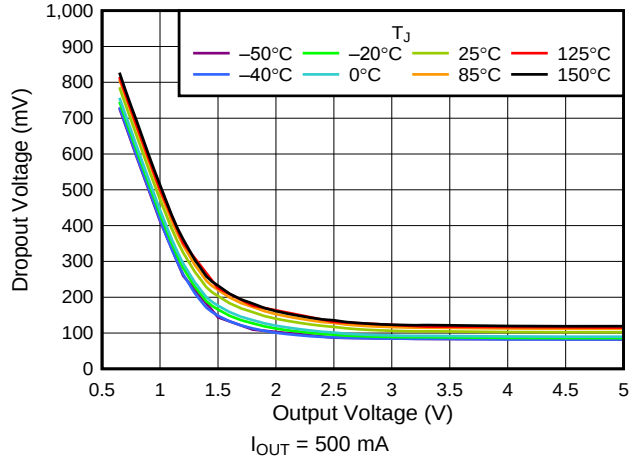



**図 7. $V_{DO}$ vs $V_{OUT}$**

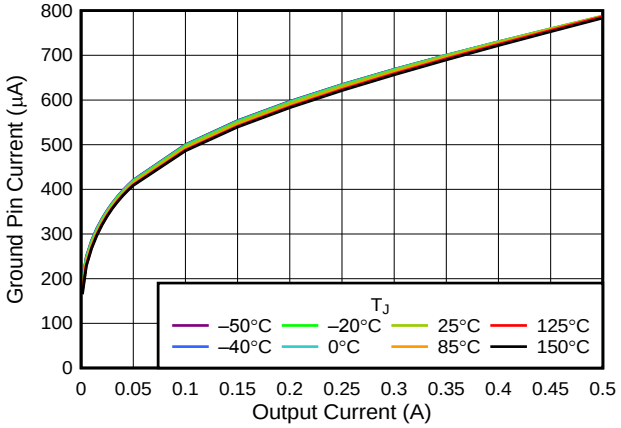



**図 8. $I_{GND}$ vs $I_{OUT}$**

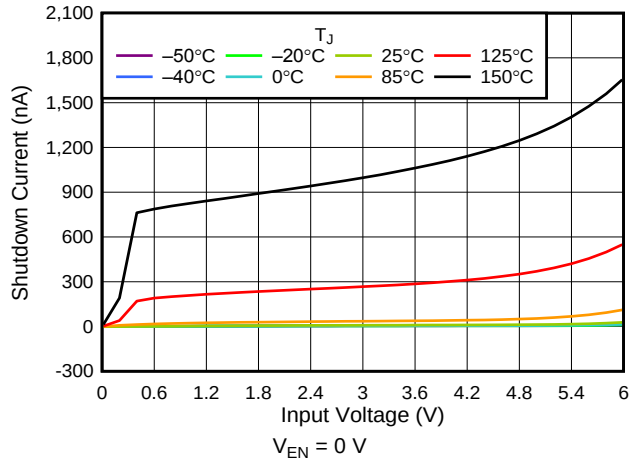



**図 9. $I_{SHDN}$ vs $V_{IN}$**

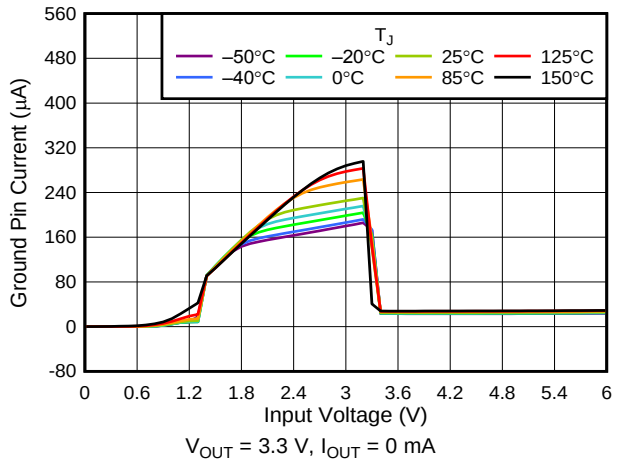



**図 10. $I_Q$ vs $V_{IN}$**

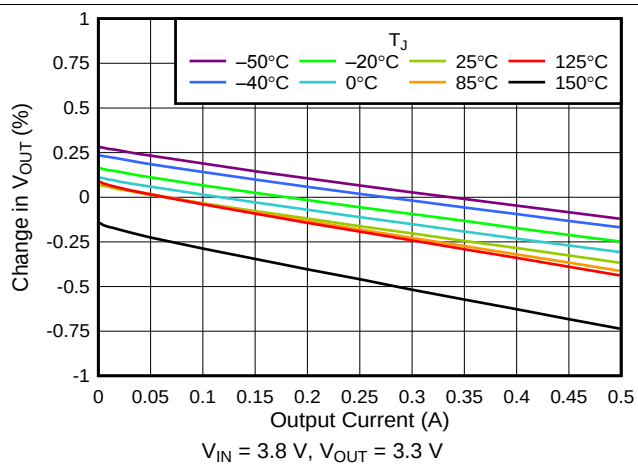



**図 11. 3.3-V Load Regulation vs $I_{OUT}$**

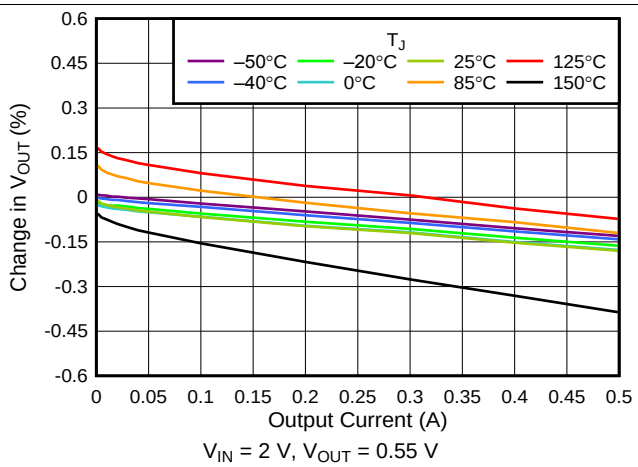



**図 12. 0.55-V Load Regulation vs $I_{OUT}$**


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## Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)

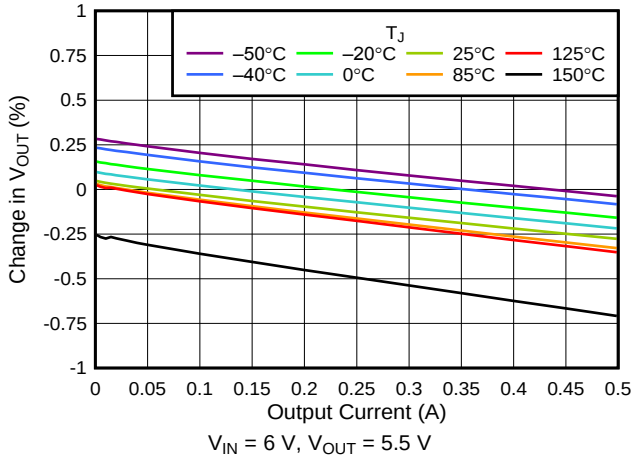



図 13. 5-V Load Regulation vs $I_{OUT}$

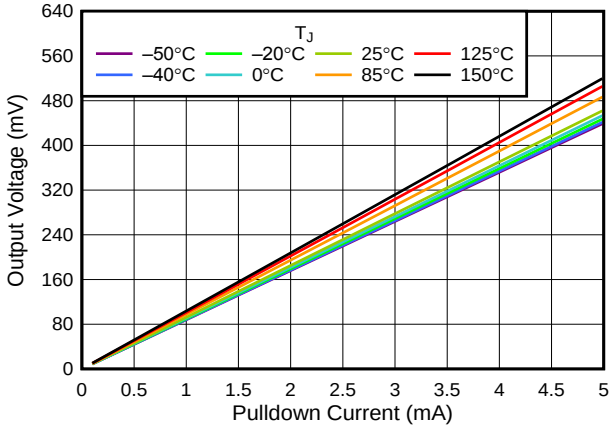



図 14. $V_{OUT}$ vs $I_{OUT}$ Pulldown Resistor

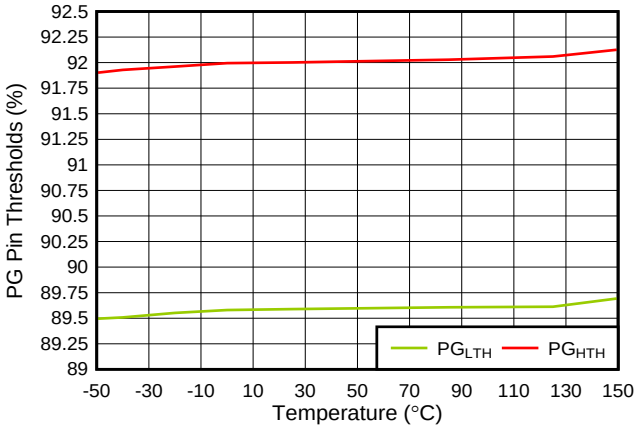



図 15. $PG_{LTH}$ and $PG_{HTH}$ vs Temperature

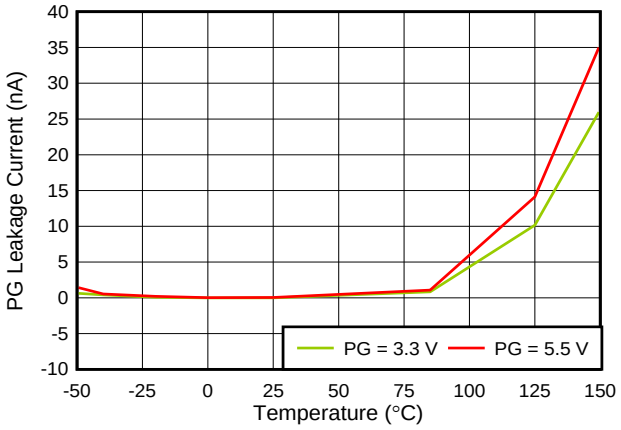



図 16. $I_{lkg(PG)}$ vs Temperature and PG Pin Voltage

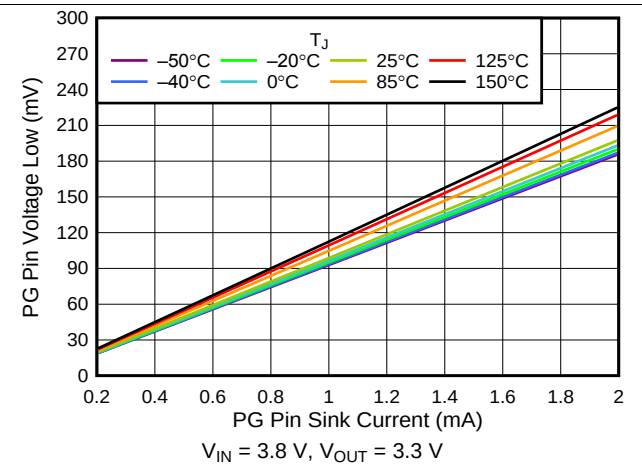



図 17. $V_{OL(PG)}$ vs PG Pin Sink Current

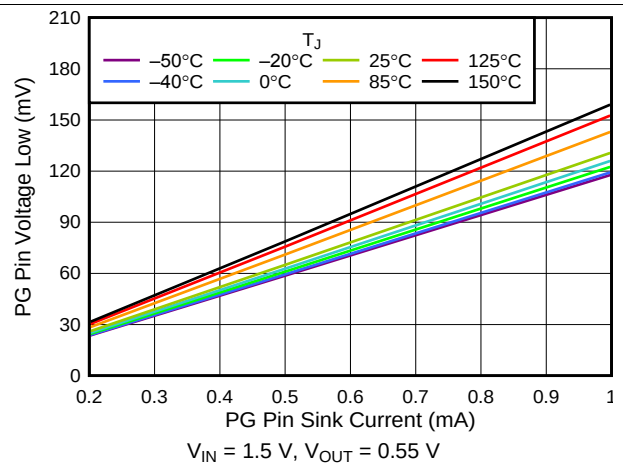



図 18. $V_{OL(PG)}$ vs PG Pin Sink Current

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## Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)

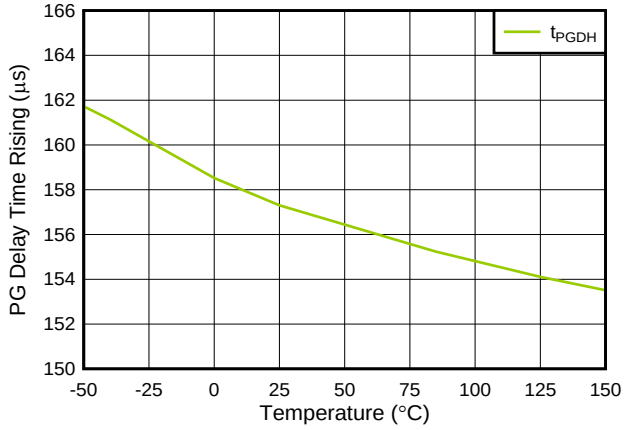



**図 19. $t_{PGDH}$ vs Temperature**

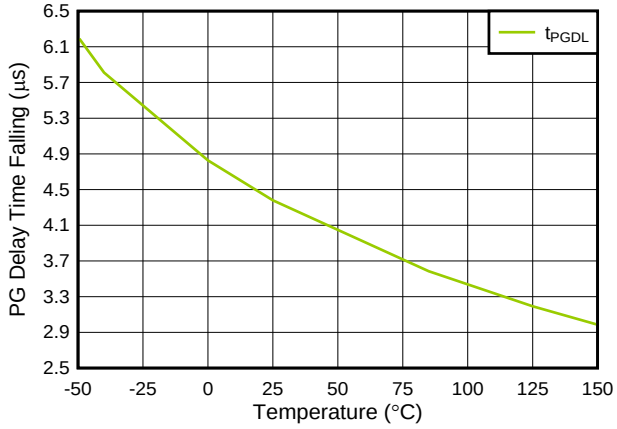



**図 20. $t_{PGDL}$ vs Temperature**

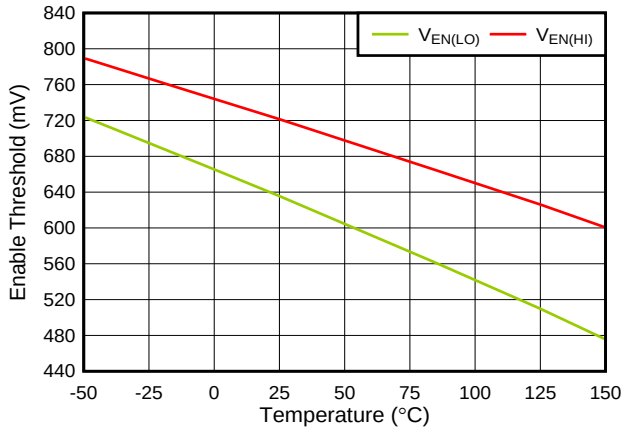



**図 21. $V_{EN(HI)}$ and $V_{EN(LO)}$ vs Temperature**

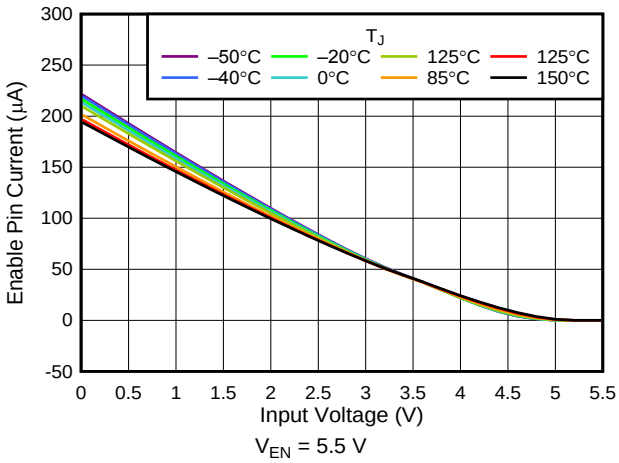



**図 22. $I_{EN}$ vs $V_{IN}$**

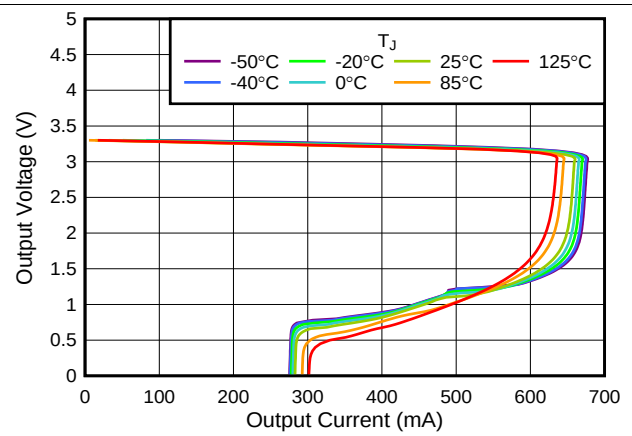



**図 23. 3.3-V Foldback Current Limit vs $I_{OUT}$**

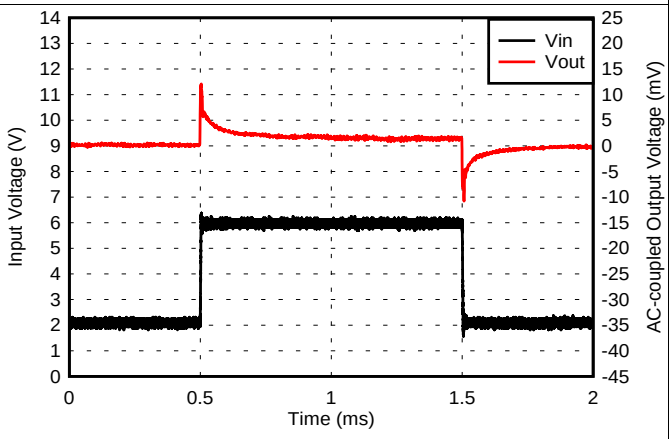
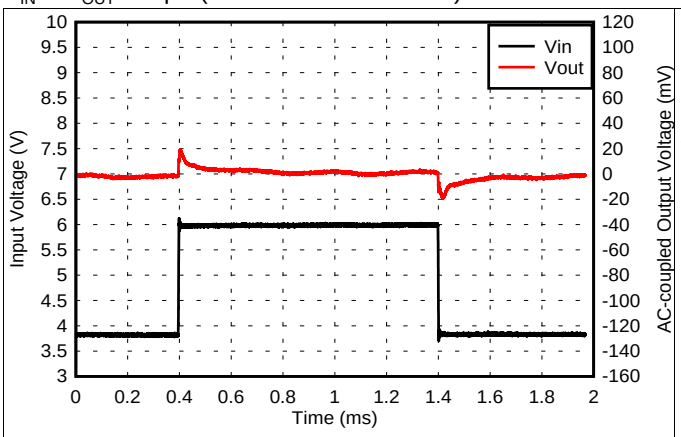



**図 24. 0.55-V Line Transient**


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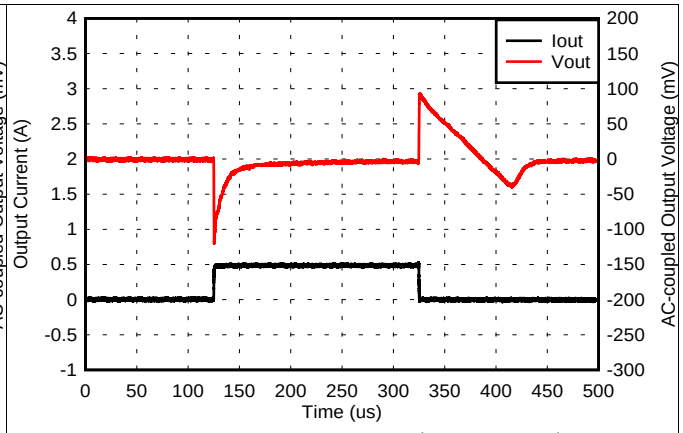
## Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



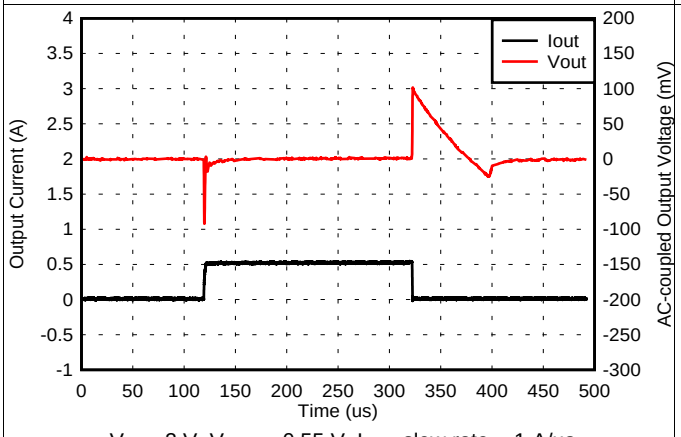

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA, $V_{IN}$ slew rate = 1 V/µs

**図 25. 3.3-V Line Transient**



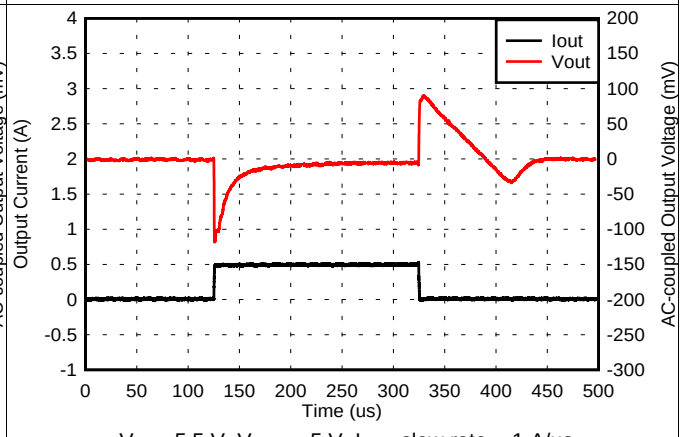

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 1 A/µs

**図 26. 3.3-V, 1-mA to 500-mA Load Transient**



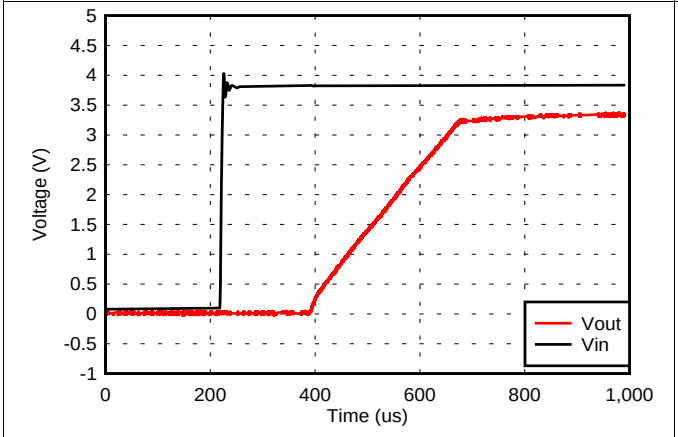

$V_{IN}$ = 2 V, $V_{OUT}$ = 0.55 V, $I_{OUT}$ slew rate = 1 A/µs

**図 27. 0.55-V, 1-mA to 500-mA Load Transient**



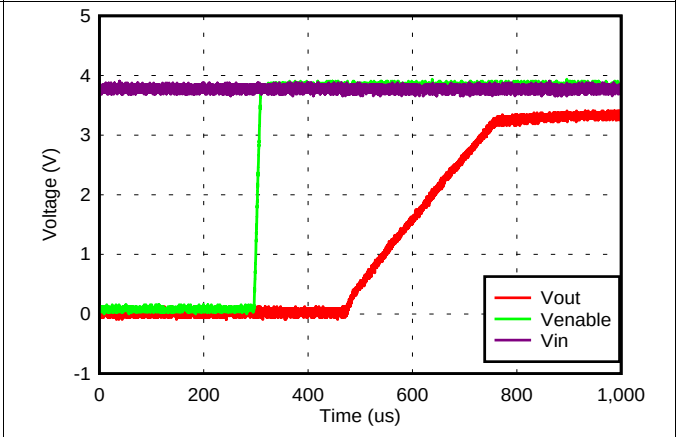

$V_{IN}$ = 5.5 V, $V_{OUT}$ = 5 V, $I_{OUT}$ slew rate = 1 A/µs

**図 28. 5-V, 1-mA to 500-mA Load Transient**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA

**図 29. $V_{IN}$ Power-Up**



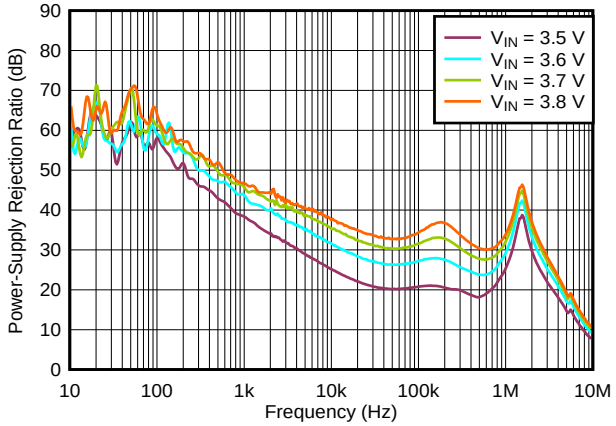

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA

**図 30. Startup With EN**

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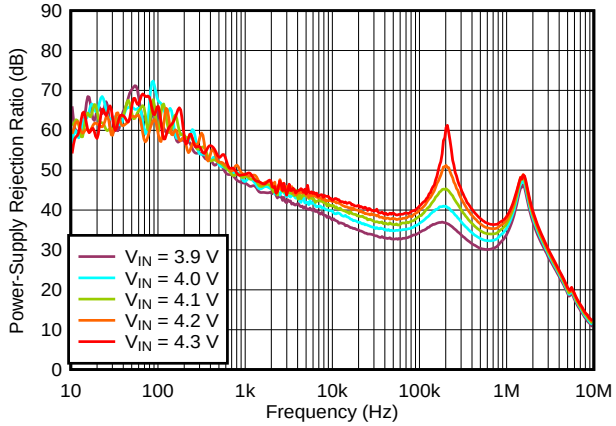
## Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



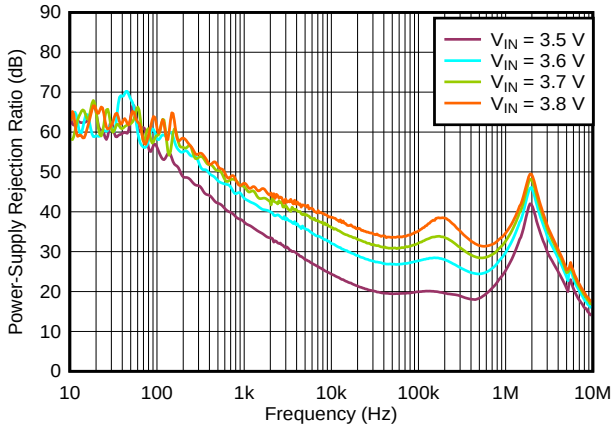

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF

**図 31. PSRR vs Frequency and $V_{IN}$**



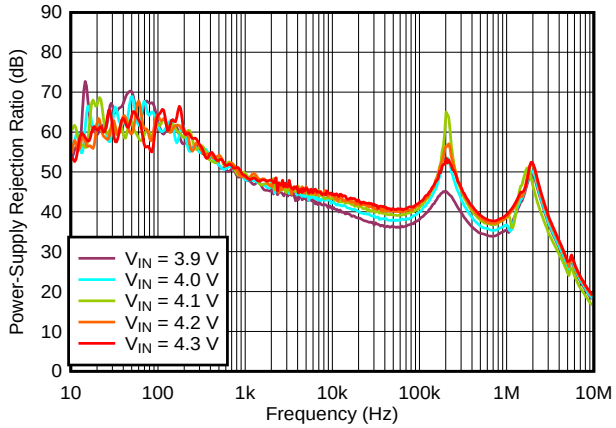

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF

**図 32. PSRR vs Frequency and $V_{IN}$**



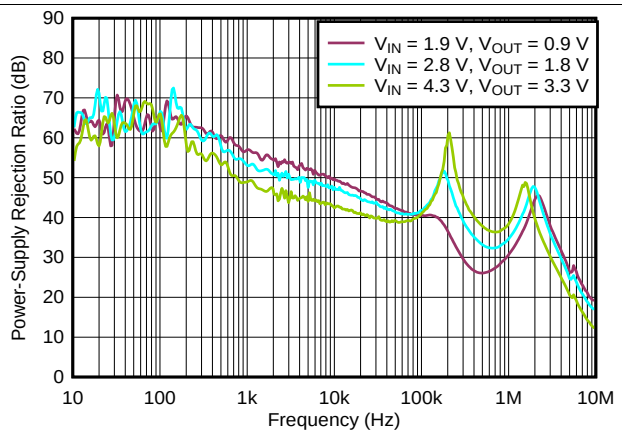

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 250 mA, $C_{OUT}$ = 2.2 µF

**図 33. PSRR vs Frequency and $V_{IN}$**



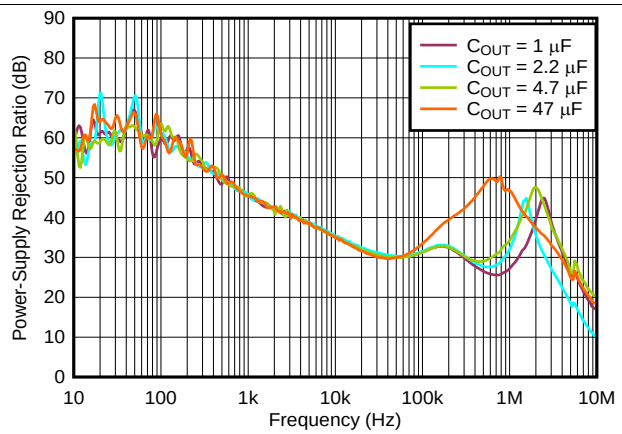

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 250 mA, $C_{OUT}$ = 2.2 µF

**図 34. PSRR vs Frequency and $V_{IN}$**




$I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF

**図 35. PSRR vs Frequency**



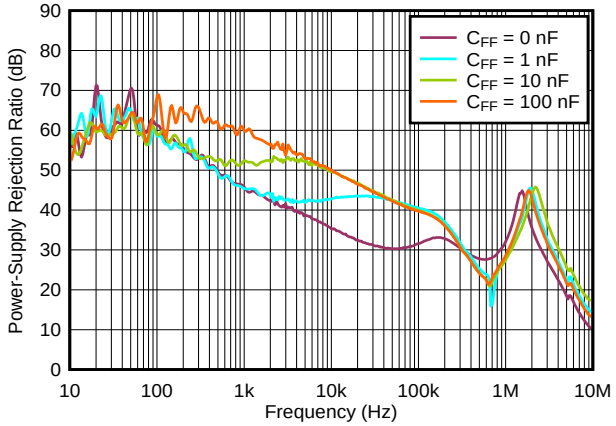

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA

**図 36. PSRR vs Frequency and $C_{OUT}$**


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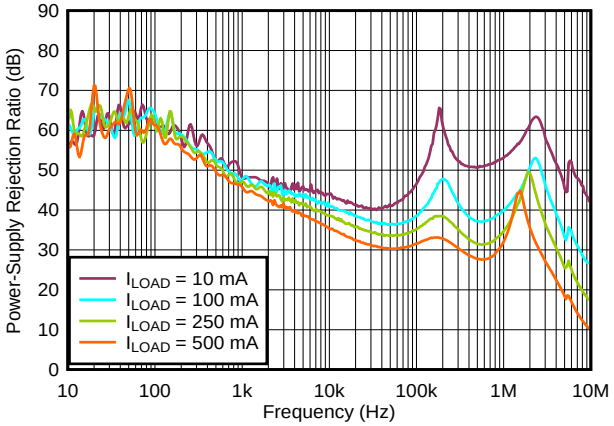
## Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



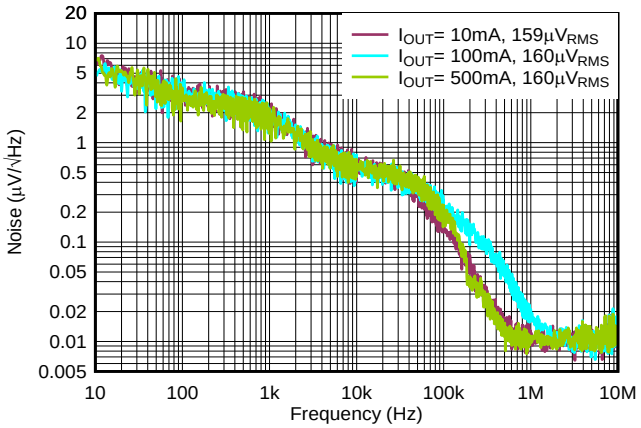

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA

**図 37. PSRR vs Frequency and $C_{FF}$**



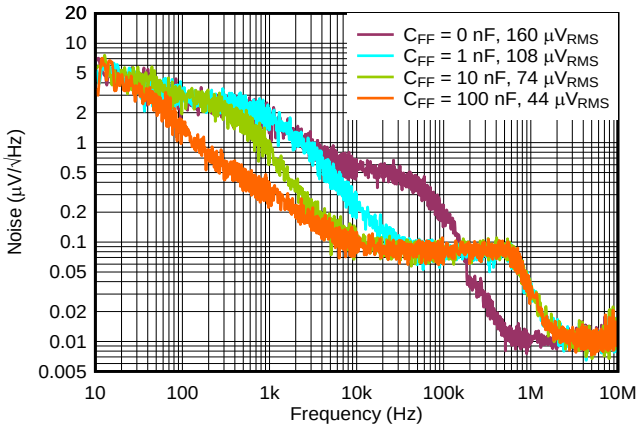

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 2.2 µF

**図 38. PSRR vs Frequency and $I_{LOAD}$**



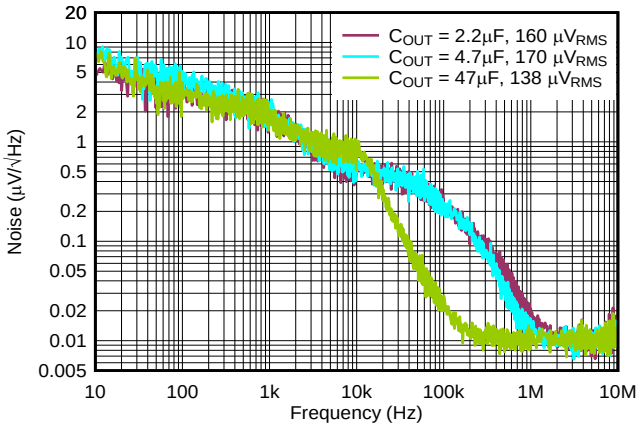

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 2.2 µF,
$V_{RMS}$ BW = 10 Hz to 100 kHz

**図 39. Output Spectral Noise Density**



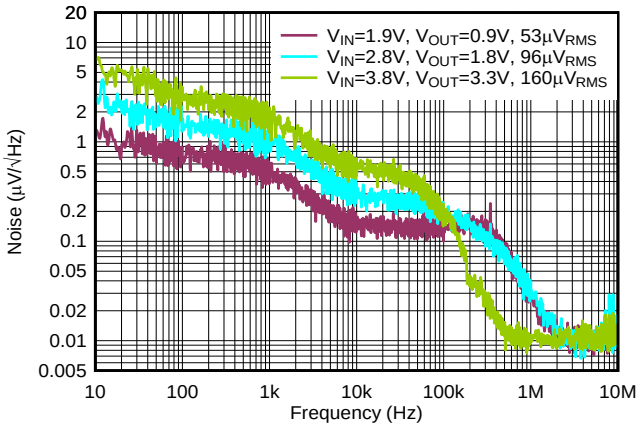

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF,
$V_{RMS}$ BW = 10 Hz to 100 kHz

**図 40. Output Spectral Noise Density vs Frequency and $C_{FF}$**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 mA, $C_{FF}$ = 0 µF,
$V_{RMS}$ BW = 10 Hz to 100 kHz

**図 41. Output Spectral Noise Density vs Frequency and $C_{OUT}$**




$I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF, $V_{RMS}$ BW = 10 Hz to 100 kHz

**図 42. Output Spectral Noise Density vs Frequency**

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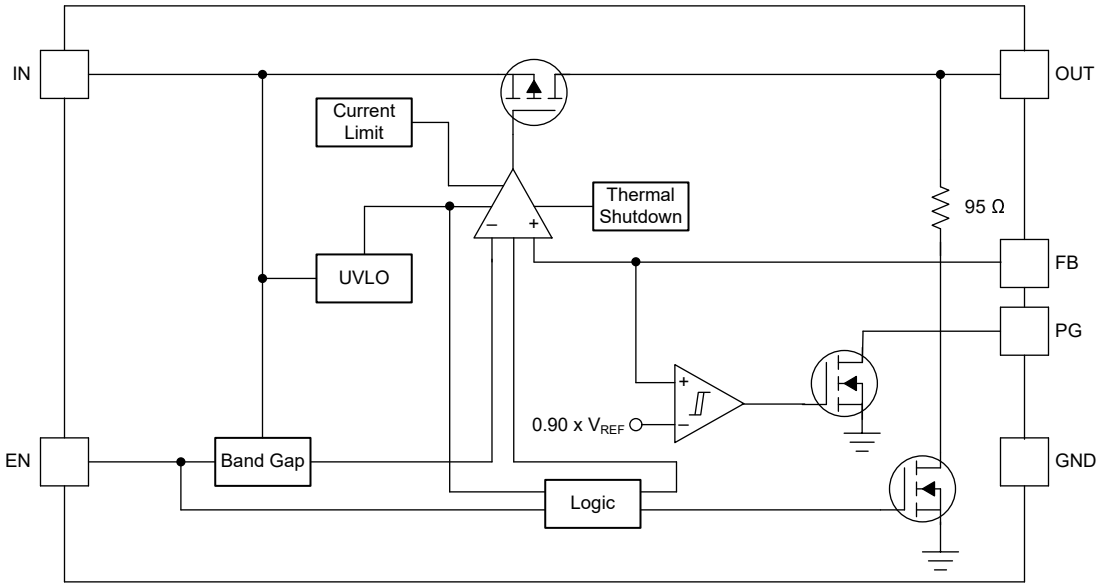
# 7 Detailed Description

## 7.1 Overview

The TPS745 low-dropout regulators (LDO) consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device ideal for portable consumer applications. The internal power-good detection circuit allows the down-stream supplies to be sequenced and alerts if the output voltage is below a regulation threshold.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Undervoltage Lockout (UVLO)

The TPS745 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage ($V_{UVLO}$). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When $V_{IN}$ is less than $V_{UVLO}$, the output is connected to ground with a pulldown resistor ($R_{PULLDOWN}$). When the device enters UVLO, the PG output is pulled low.

### 7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$. Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN.When the device is disabled, the PG output pin is pulled low.

The TPS745 has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance ($C_{OUT}$) and the load resistance ($R_L$) in parallel with the pulldown resistor ($R_{PULLDOWN}$). 式 1 calculates the time constant:

$$\tau = ( R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$


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## Feature Description (continued)

### 7.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4\ V \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 43 shows a diagram of the foldback current limit.

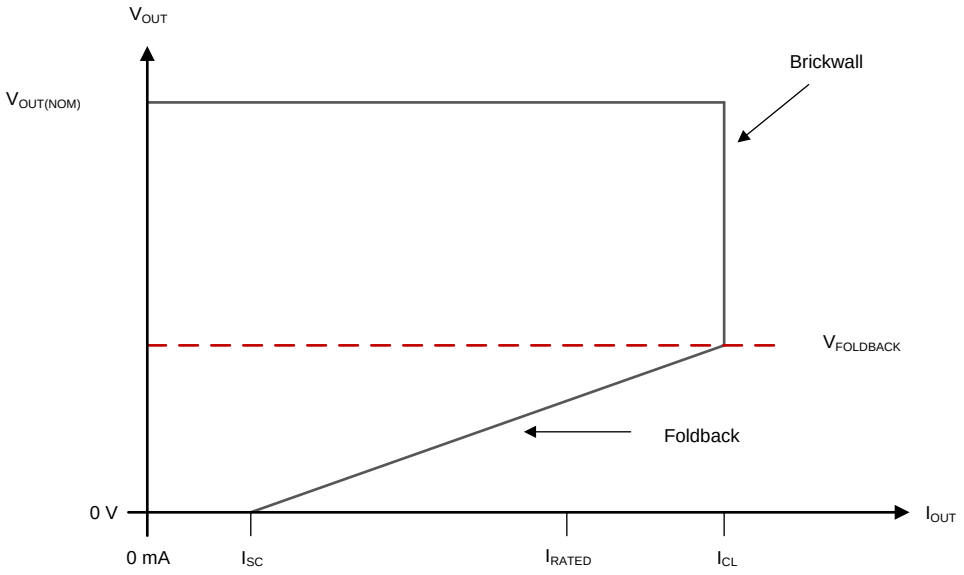



**Figure 43. Foldback Current Limit**

### 7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN} – V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

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## Feature Description (continued)

The TPS745 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS745 into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.


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# 8 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Adjustable Device Feedback Resistors

図 44 shows that the output voltage of the TPS745 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

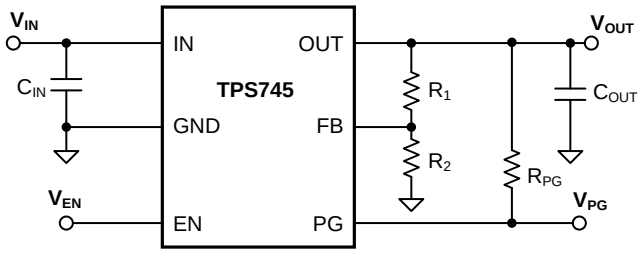



**図 44. Adjustable Operation**

The adjustable-version device requires external feedback divider resistors to set the output voltage. $V_{OUT}$ is set using the feedback divider resistors, $R_1$ and $R_2$, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

For this device, $V_{FB}$ = 0.55 V.

To ignore the FB pin current error term in the $V_{OUT}$ equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

For this device, $I_{FB}$ = 10 nA.

### 8.1.2 Input and Output Capacitor Selection

The TPS745 requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

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## Application Information (continued)

### 8.1.3 Dropout Voltage

The TPS745 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{IN}$ – $V_{OUT}$) approaches dropout operation.

### 8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on $V_{IN}$ during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in 図 45, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

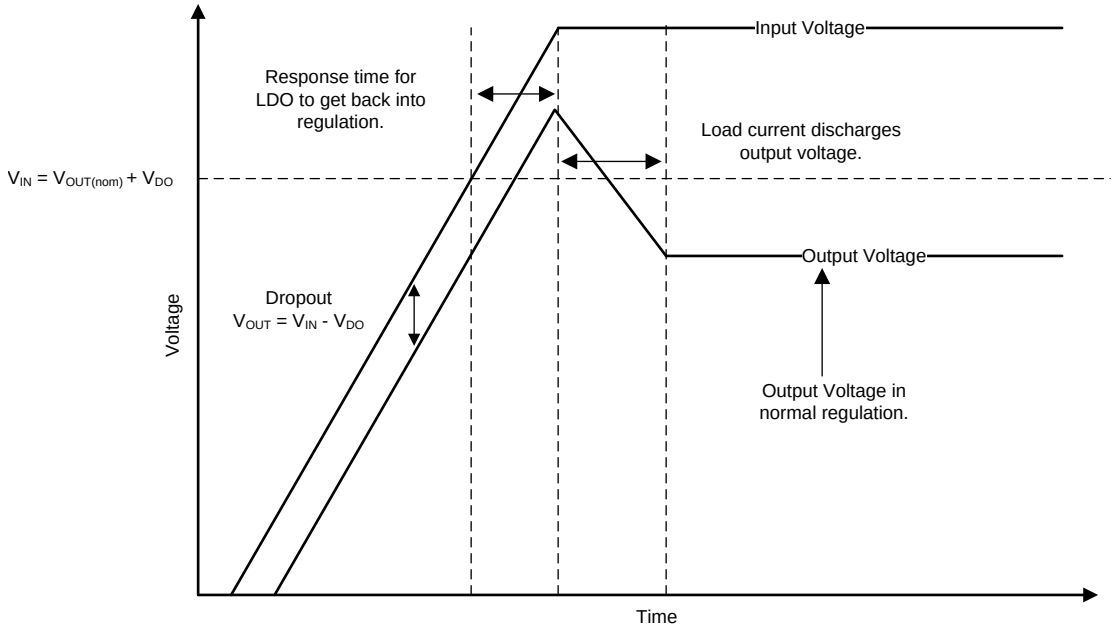



**図 45. Startup Into Dropout**

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 図 46 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.


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## Application Information (continued)

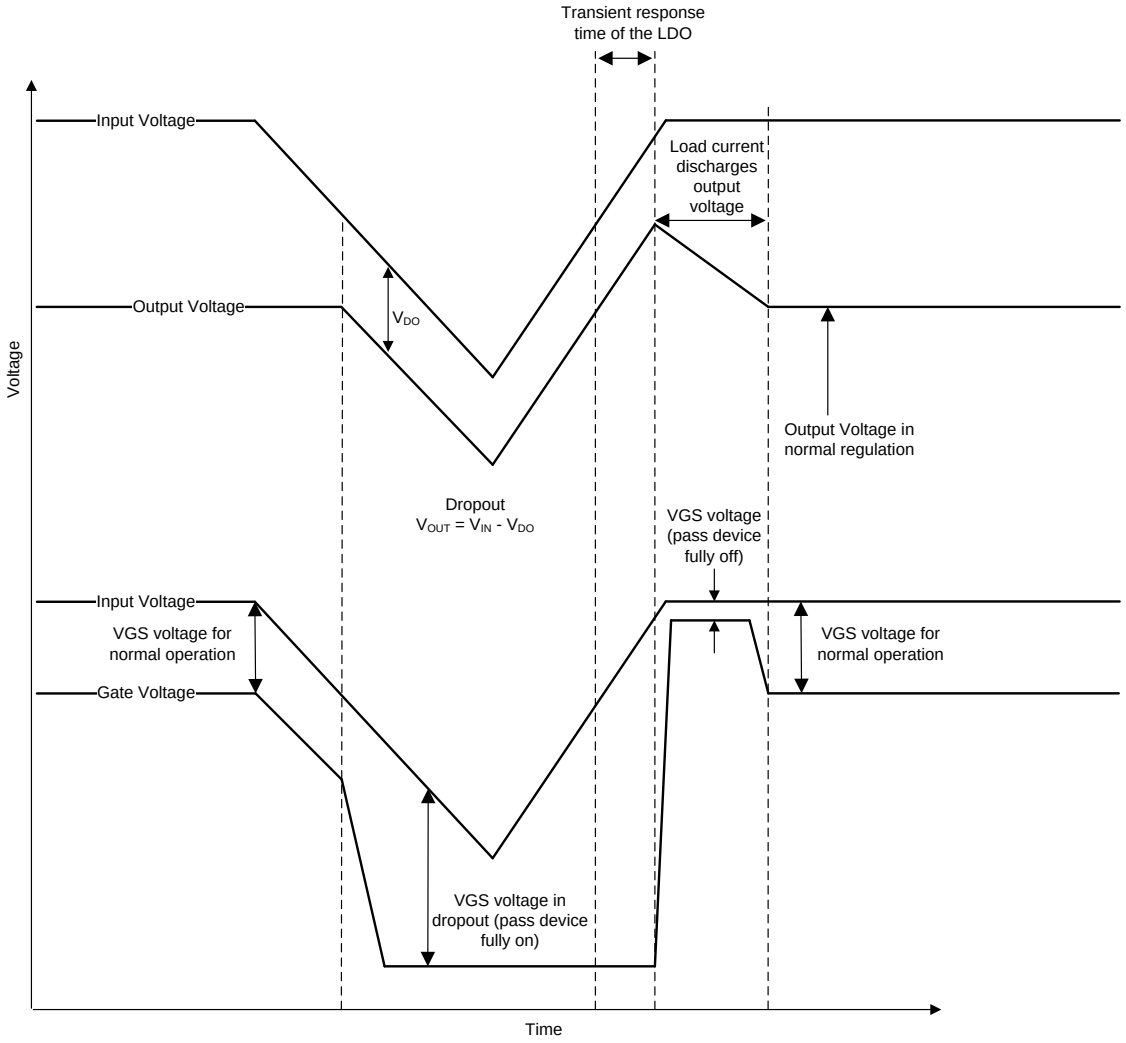



**図 46. Line Transients From Dropout**

### 8.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

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## Application Information (continued)

If reverse current flow is expected in the application, external protection must be used to protect the device. 図 47 shows one approach of protecting the device.

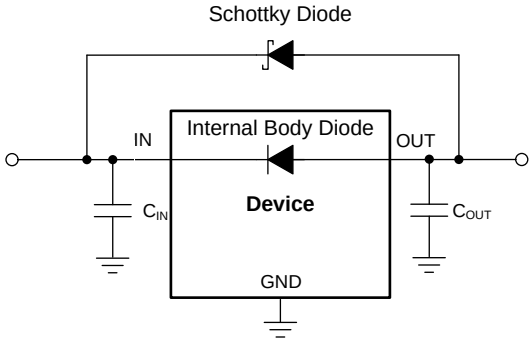



**図 47. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 8.1.6 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation ($P_D$).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (4)$$

**NOTE**

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

### 8.1.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage ($PG_{LTH}$), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds $PG_{HTH}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.


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## Application Information (continued)

When using a feed-forward capacitor ($C_{FF}$), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

The state of PG is only valid when the device operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

### 8.1.8 Feed-Forward Capacitor ($C_{FF}$)

For the adjustable-voltage version device, a feed-forward capacitor ($C_{FF}$) can be connected from the OUT pin to the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended $C_{FF}$ values are listed in the *Recommended Operating Conditions* table. A higher capacitance $C_{FF}$ can be used; however, the startup time increases. For a detailed description of $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

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## 8.2 Typical Application

図 48 shows the typical application circuit for the TPS745. Input and output capacitances must be at least 1 µF.

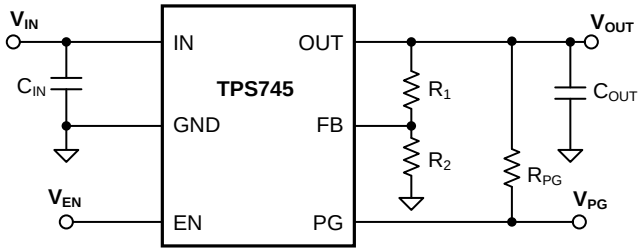



**図 48. TPS745 Typical Application**

### 8.2.1 Design Requirements

Use the parameters listed in 表 2 for typical linear regulator applications.

**表 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 3.8 V |
| Output voltage | 3.3 V, ±1% |
| Input current | 500 mA (maximum) |
| Output load | 500-mA DC |
| Maximum ambient temperature | 70°C |

### 8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

図 44 illustrates the output voltage of the TPS745. Set the output voltage using the resistor divider; see the section for details.

#### *8.2.2.1 Input Current*

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use 式 6 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (6)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the $V_{OUT}$ ramp
- $R_{LOAD}$ is the resistive load impedance

#### *8.2.2.2 Thermal Dissipation*

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation ($P_D$). Use 式 7 to calculate the power dissipation. Multiply $P_D$ by $R_{\theta JA}$ as 式 8 shows and add the ambient temperature ($T_A$) to calculate the junction temperature ($T_J$).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (7)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (8)$$

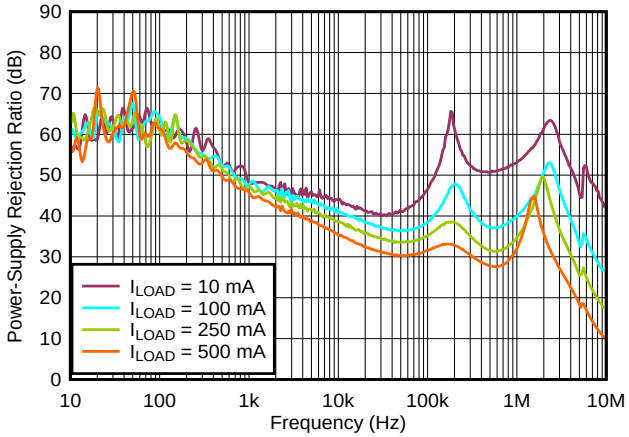
Calculate the maximum ambient temperature as 式 9 shows if the ($T_{J(MAX)}$) value does not exceed 125°C. 式 10 calculates the maximum ambient temperature with a value of 104.93°C.


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$$T_{A(MAX)} = T_{J(MAX)} – R_{\theta JA} \times P_D \quad (9)$$

$$T_{A(MAX)} = 125°C – 80.3°C/W \times (3.8\ V – 3.3\ V) \times (0.5\ A) = 104.93°C \quad (10)$$

### 8.2.3 Application Curve




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 2.2 µF

**図 49. PSRR vs Frequency and $I_{LOAD}$**

# 9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TPS745.

# 10 Layout

## 10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

## 10.2 Layout Example

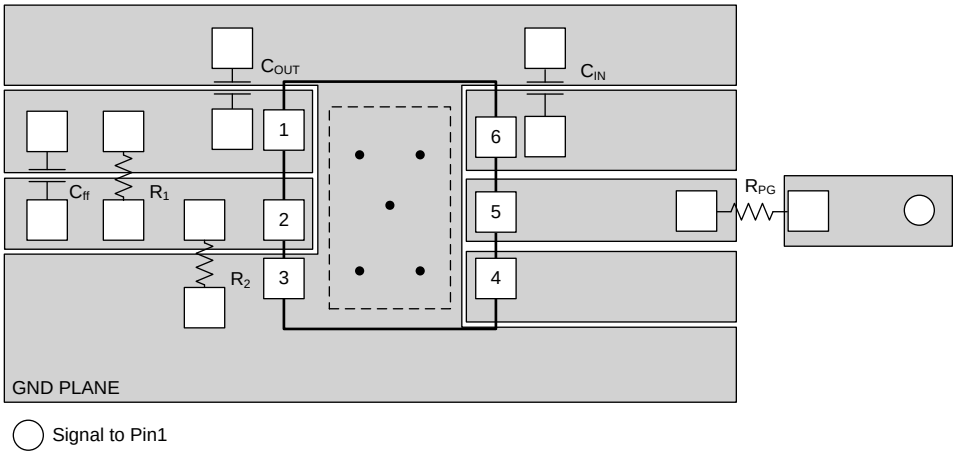



**図 50. DRV Package Layout Example**


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# 11 デバイスおよびドキュメントのサポート

## 11.1 ドキュメントのサポート

### 11.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、*『低ドロップアウト・レギュレータでフィードフォワード・コンデンサを使用することの長所と短所』アプリケーション・レポート*

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## 11.3 コミュニティ・リソース

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## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS74501PDRVR | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MEH |
| TPS74501PDRVR.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MEH |
| TPS74501PDRVRG4 | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MEH |
| TPS74501PDRVRG4.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MEH |
| TPS74501PDRVT | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MEH |
| TPS74501PDRVT.A | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MEH |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS745 :**

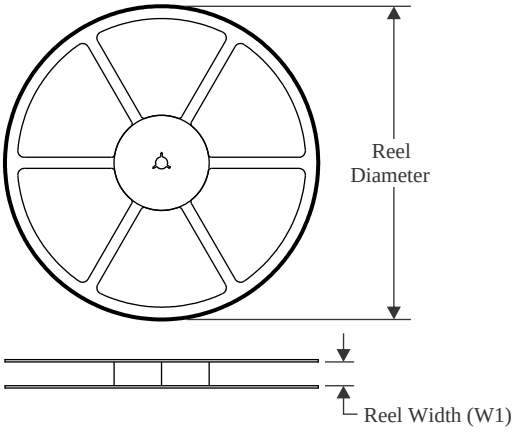
- Automotive : TPS745-Q1

NOTE: Qualified Version Definitions:

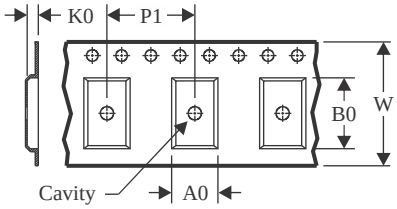
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

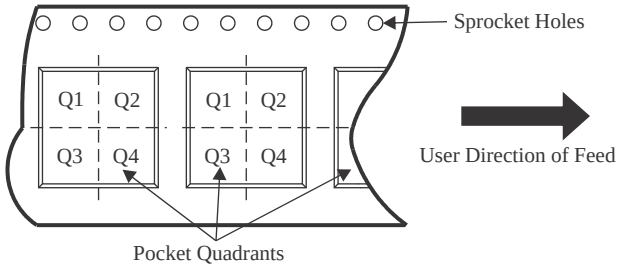



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

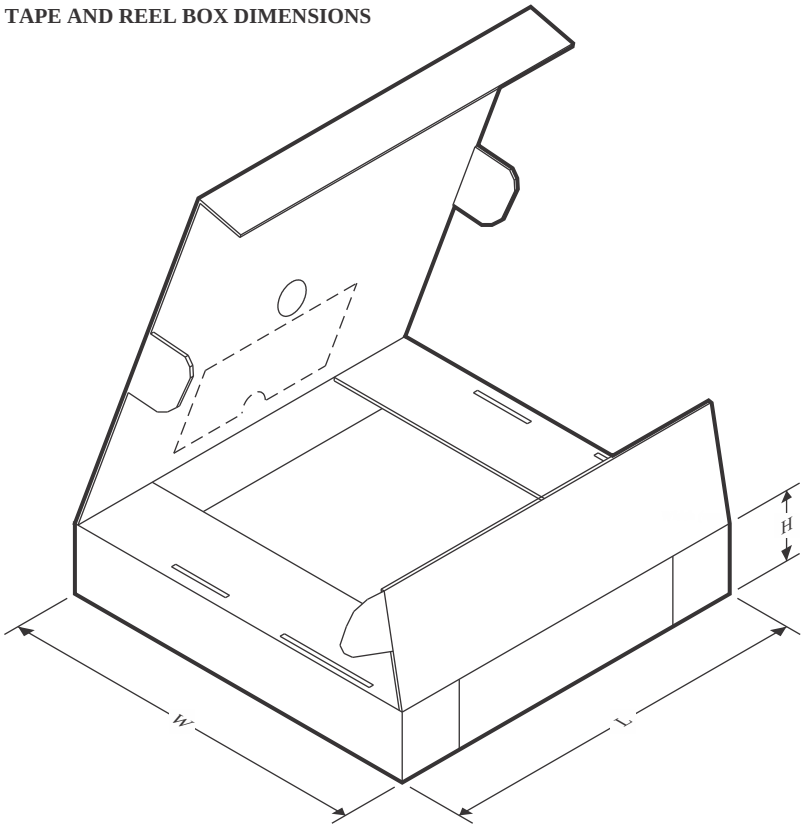
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS74501PDRVR | WSON | DRV | 6 | 3000 | 178.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS74501PDRVRG4 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS74501PDRVT | WSON | DRV | 6 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

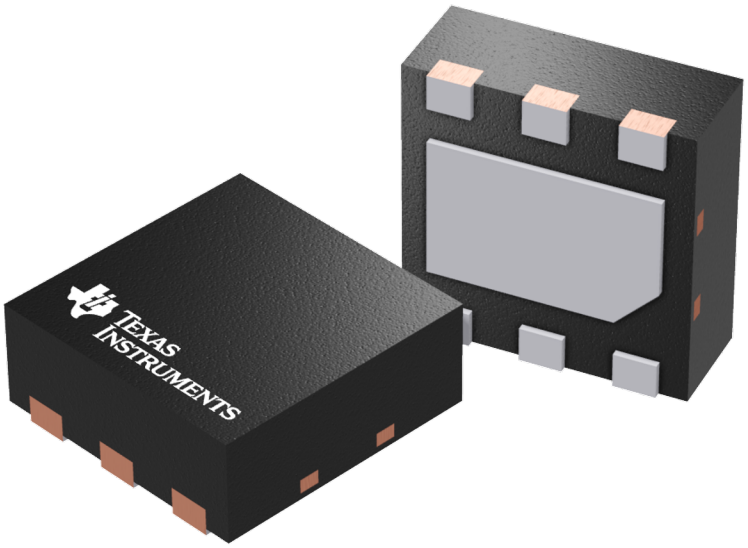



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS74501PDRVR | WSON | DRV | 6 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS74501PDRVRG4 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS74501PDRVT | WSON | DRV | 6 | 250 | 210.0 | 185.0 | 35.0 |

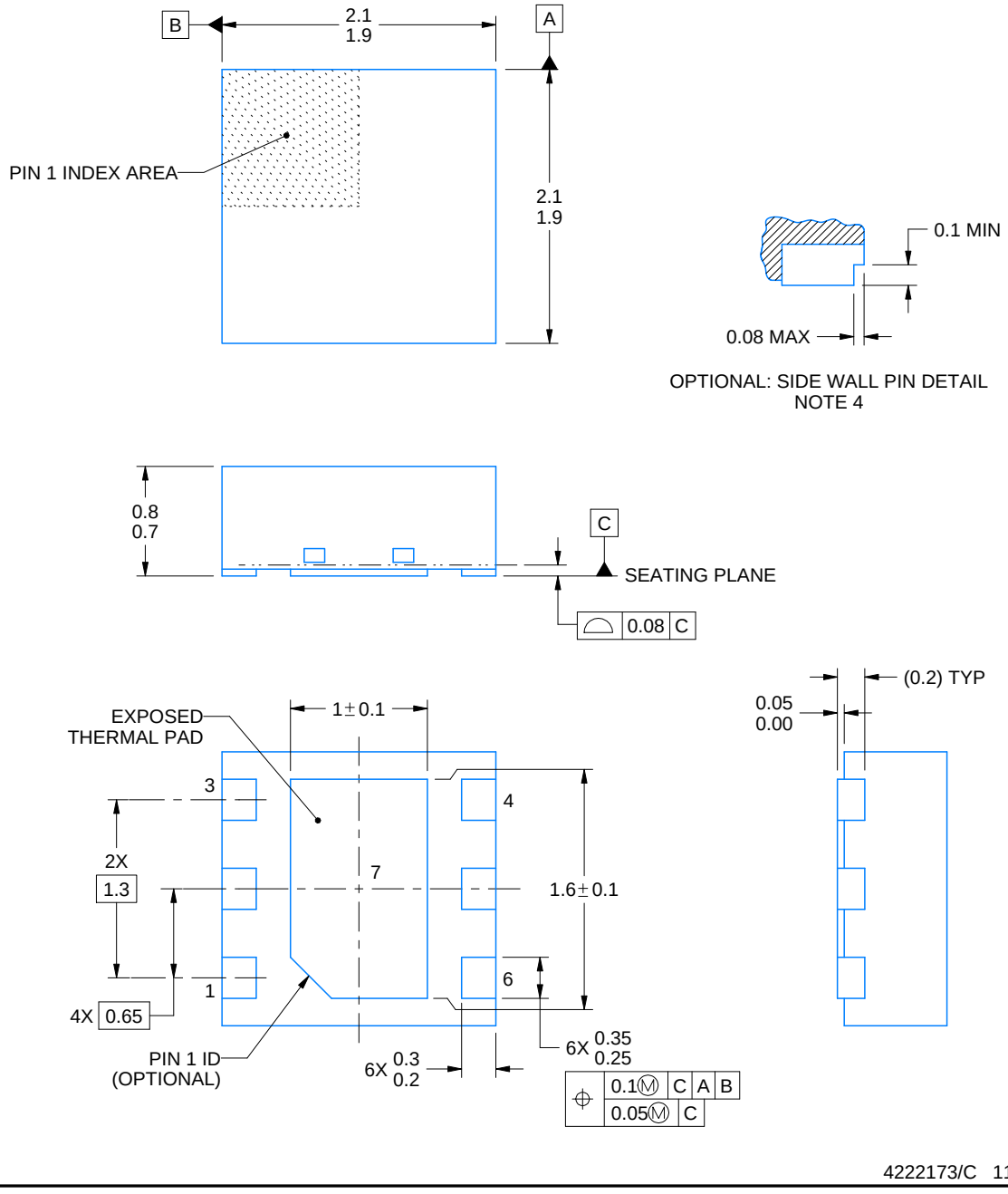
# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



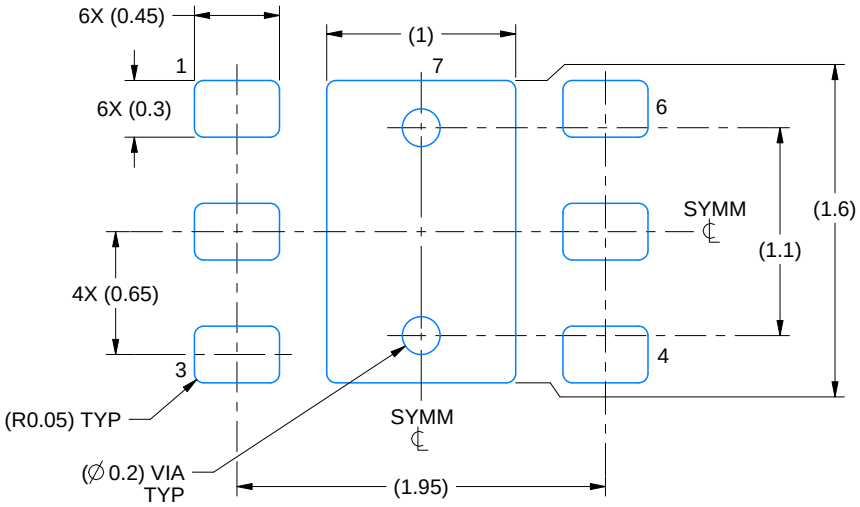

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

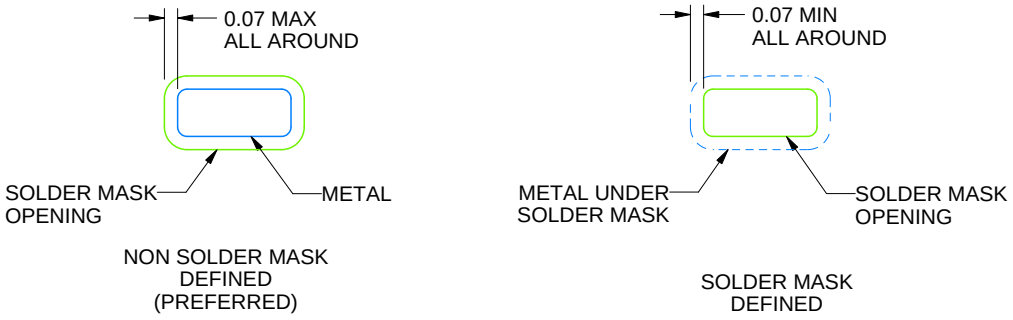



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.




LAND PATTERN EXAMPLE
SCALE:25X

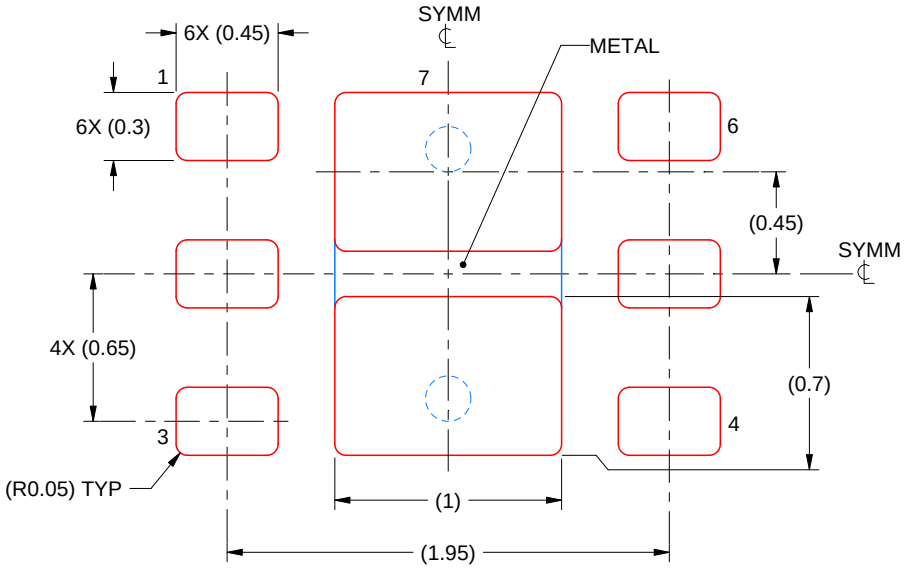



SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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