

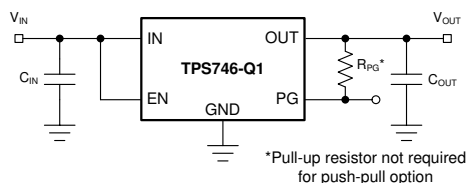
# TPS746-Q1 小型ウェットブル フランク パッケージ封止のパワーグッド機能 搭載、車載用 1A LDO

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ,  $T_A$
- デバイスの動作時の接合部温度範囲
  - $-40^{\circ}\text{C} \sim +150^{\circ}\text{C}$
- パッケージ:
  - 2mm x 2mm ウェットブル フランク WSON
  - 3mm x 3mm ウェットブル フランク VSON
- 入力電圧範囲: 1.5V ~ 6.0V
- 出力電圧範囲:
  - 固定オプション: 0.65V ~ 5.0V
  - 可変オプション: 0.55V ~ 5.5V
- 高 PSRR: 100kHz 時に 38dB
- 出力精度: 標準値  $\pm 0.85\%$ 、最大値  $\pm 1.5\%$
- パワーグッド出力オプション
  - オープンドレインまたはプッシュプル
- 非常に低いドロップアウト:
  - 1A で 265mV (最大値) ( $3.3V_{\text{OUT}}$ )
- 1 $\mu\text{F}$  以上のコンデンサで安定
- 低  $I_Q$ : 25 $\mu\text{A}$  (標準値)
- アクティブ出力放電
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 低い熱抵抗:
  - DRV (6ピン WSON)、 $R_{\theta\text{JA}} = 80.3^{\circ}\text{C/W}$
  - DRB (8ピン VSON)、 $R_{\theta\text{JA}} = 55.5^{\circ}\text{C/W}$

## 2 アプリケーション

- 車載ヘッド・ユニット
- 前方および後方カメラ
- 車載クラスター・ディスプレイ
- テレマティクス制御ユニット
- 中距離 / 短距離レーダー



代表的なアプリケーション：固定電圧バージョン

## 3 説明

TPS746-Q1 は、パワーグッド機能を持つ 1A の超低ドロップアウトレギュレータ (LDO) です。小型の 6 ピン、2mm × 2mm WSON パッケージ、および小型の 8 ピン、3mm × 3mm VSON パッケージ (ウェットブル フランク付き) で供給されるため、光学検査を容易に行えます。TPS746-Q1 は静止電流が小さく、ラインおよび負荷の過渡性能が高速です。

TPS746-Q1 は、1.5V~6.0V の入力電圧範囲と外部から調整可能な 0.55V~5.5V の出力範囲に対応しているため、ポストレギュレーションに柔軟に使用できます。本デバイスは、一般的な電圧レールに給電するための固定出力電圧にも対応しています。

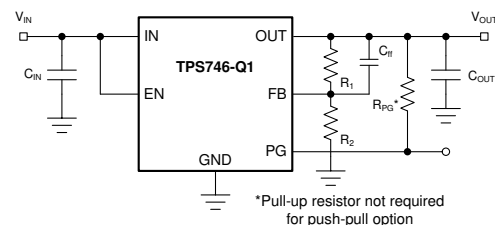
TPS746-Q1 は、フィードバックピンの電圧を監視して出力電圧のステータスを表示するパワーグッド出力 (PG) を備えています。EN 入力および PG 出力を使用して、システムの複数の電源をシーケンシングできます。

TPS746-Q1 は小さなセラミック出力コンデンサでも安定に動作するため、ソリューション全体を小型化できます。高精度のバンドギャップおよびエラーアンプにより、 $25^{\circ}\text{C}$  で  $\pm 0.85\%$  (最大値)、全温度範囲で  $\pm 1.5\%$  (最大値) の高精度を実現しています。このデバイスはサーマルシャットダウン、電流制限、低電圧誤動作防止 (UVLO) 機能を内蔵しています。TPS746-Q1 は、短絡発生時の発熱を低減するのに役立つ内部フォールドバック電流制限機能を備えています。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TPS746-Q1	DRV (ウェットブル フランク WSON 6)	2mm × 2mm
	DRB (ウェットブル フランク VSON 8)	3mm × 3mm

- 詳細については、[メカニカル](#)、[パッケージ](#)、および[注文情報](#)をご覧ください。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション：可変電圧バージョン



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## 4 Pin Configuration and Functions

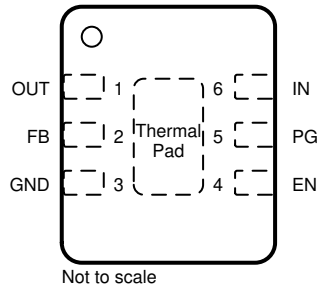


图 4-1. DRV Package, 6-Pin Adjustable WSON (Top View)

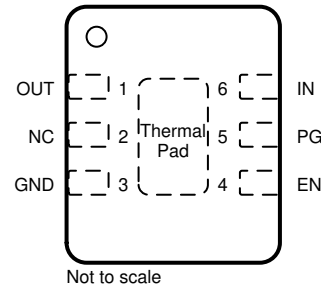


图 4-2. DRV Package, 6-Pin Fixed WSON (Top View)

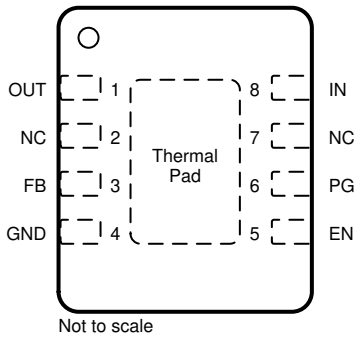


图 4-3. DRB Package, 8-Pin Adjustable VSON (Top View)

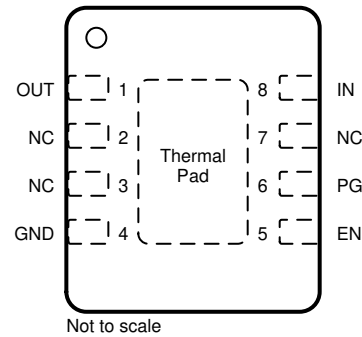


图 4-4. DRB Package, 8-Pin Fixed VSON (Top View)

表 4-1. Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DRV (Fixed)	DRV (Adjust)	DRB (Fixed)	DRB (Adjust)		
EN	4	4	5	5	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
FB	—	2	—	3	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	3	4	4	—	Ground pin.
IN	6	6	8	8	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the <a href="#">Recommended Operating Conditions</a> table and the <a href="#">Input and Output Capacitor Selection</a> section. Place the input capacitor as close to the output of the device as possible.
NC	2	—	2, 3, 7	2, 7	—	No internal connection. Ground this pin for better thermal performance.
OUT	1	1	1	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the <a href="#">Recommended Operating Conditions</a> table and the <a href="#">Input and Output Capacitor Selection</a> section. Place the output capacitor as close to the output of the device as possible.
PG	5	5	6	6	Output	Power-good output. Available in open-drain and push-pull topologies. A pullup resistor is required for the open-drain version. For the open-drain version, if the power-good functionality is not being used, ground this pin or leave floating. For the push-pull version, if the power-good functionality is not being used, leave this pin floating.
Thermal Pad					—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply, $V_{IN}$	-0.3	6.5	V
	Enable, $V_{EN}$	-0.3	6.5	
	Feedback, $V_{FB}$	-0.3	2.0	
	Power-good, $V_{PG}$	-0.3	6.5	
	Output, $V_{OUT}$	-0.3	$V_{IN} + 0.3$ <sup>(2)</sup>	
Current	Output, $I_{OUT}$	Internally limited		
	Power-good, $I_{PG}$		±10	mA
Temperature	Operating junction, $T_J$	-40	150	°C
	Storage, $T_{stg}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The absolute maximum rating is  $V_{IN} + 0.3$  V or 6.0 V, whichever is smaller.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011, corner pins	±750
		Charged-device model (CDM), per AEC Q100-011, other pins	±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	1.5		6.0	V
$V_{OUT}$	Output voltage	Adjustable version		5.5	V
		Fixed version	0.65	5.0	
$I_{OUT}$	Output current	0		1	A
$C_{IN}$	Input capacitor	1			µF
$C_{OUT}$	Output capacitor <sup>(1)</sup>	1		220	µF
$C_{FF}$	Feed-forward capacitor		10		nF
$V_{EN}$	Enable voltage	0		6.0	V
$f_{EN}$	Enable toggle frequency			10	kHz
$V_{PG}$	PG voltage	0		6.0	V
$T_J$	Junction temperature	-40		150	°C

- (1) Minimum derated capacitance of 0.47 µF is required for stability.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS746-Q1		UNIT
		DRV (WSON)	DRB (VSON)	
		6 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	80.3	55.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	98.7	70.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	44.8	28.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.1	4.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	45.0	28.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	20.8	10.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

at operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted); all typical values at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>FB</sub>	Feedback voltage			0.55			V
	Output accuracy <sup>(1)</sup>	T <sub>J</sub> = 25°C		-0.85%		0.85%	
		-40°C ≤ T <sub>J</sub> ≤ 85°C		-1.00%		1.00%	
		-40°C ≤ T <sub>J</sub> ≤ 150°C		-1.50%		1.50%	
	Line regulation	V <sub>OUT(NOM)</sub> + 0.5 V <sup>(2)</sup> ≤ V <sub>IN</sub> ≤ 6.0 V			2	7.5	mV
	Load regulation	0.1 mA ≤ I <sub>OUT</sub> ≤ 1 A, V <sub>IN</sub> ≥ 2.0 V			0.030		V/A
I <sub>GND</sub>	Ground current	I <sub>OUT</sub> = 0 mA	T <sub>J</sub> = 25°C		25	32	μA
			-40°C ≤ T <sub>J</sub> ≤ 150°C		25	36	
I <sub>SHDN</sub>	Shutdown current	V <sub>EN</sub> ≤ 0.3 V, 1.5 V ≤ V <sub>IN</sub> ≤ 6.0 V	-40°C ≤ T <sub>J</sub> ≤ 125°C		0.1	1	μA
			-40°C ≤ T <sub>J</sub> ≤ 150°C		0.1	1.55	
I <sub>FB</sub>	Feedback pin current	Adjustable only			0.01	0.1	μA
I <sub>CL</sub>	Output current limit	V <sub>OUT(NOM)</sub> < 1 V, V <sub>OUT</sub> = V <sub>OUT(NOM)</sub> - 0.2 V, V <sub>IN</sub> = 2.0 V		1.22	1.5	1.83	A
		V <sub>OUT(NOM)</sub> ≥ 1 V, V <sub>OUT</sub> = V <sub>OUT(NOM)</sub> × 0.85, V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 1.0 V					
I <sub>SC</sub>	Short-circuit current limit	V <sub>OUT</sub> = 0 V	V <sub>OUT(NOM)</sub> < 1 V, V <sub>IN</sub> = 2.0 V	500	680	850	mA
			V <sub>OUT(NOM)</sub> ≥ 1 V, V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 1.0 V				
V <sub>DO</sub>	Dropout voltage	I <sub>OUT</sub> = 1 A, V <sub>OUT</sub> = 0.95 × V <sub>OUT(NOM)</sub>	0.65 V ≤ V <sub>OUT</sub> < 0.8 V <sup>(3)</sup>		895	1090	mV
			0.8 V ≤ V <sub>OUT</sub> < 0.9 V		765	960	
			0.9 V ≤ V <sub>OUT</sub> < 1.0 V		700	890	
			1.0 V ≤ V <sub>OUT</sub> < 1.2 V		600	790	
			1.2 V ≤ V <sub>OUT</sub> < 1.5 V		465	625	
			1.5 V ≤ V <sub>OUT</sub> < 1.8 V		335	480	
			1.8 V ≤ V <sub>OUT</sub> < 2.5 V		265	400	
			2.5 V ≤ V <sub>OUT</sub> < 3.3 V		195	310	
		3.3 V ≤ V <sub>OUT</sub> ≤ 5.5 V		160	265		
PSRR	Power-supply rejection ratio	V <sub>OUT</sub> = 1.8 V, V <sub>IN</sub> = 2.8 V, I <sub>OUT</sub> = 1 A, C <sub>OUT</sub> = 2.2 μF	f = 1 kHz		53		dB
			f = 100 kHz		38		
			f = 1 MHz		30		
V <sub>N</sub>	Output noise voltage	BW = 10 Hz to 100 kHz, V <sub>OUT</sub> = 0.9 V, V <sub>IN</sub> = 1.9 V			53		μV <sub>RMS</sub>
V <sub>UVLO</sub>	Undervoltage lockout	V <sub>IN</sub> rising		1.21	1.33	1.47	V
		V <sub>IN</sub> falling		1.17	1.29	1.42	

## 5.5 Electrical Characteristics (続き)

at operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted); all typical values at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO,HYST}$	Undervoltage lockout hysteresis	$V_{IN}$ hysteresis		40		mV
$t_{STR}$	Startup time	From EN low-to-high transition to $V_{OUT} = V_{OUT(NOM)} \times 95\%$	200	500	650	$\mu\text{s}$
$V_{HI}$	EN pin high voltage (enabled)		1.0			V
$V_{LO}$	EN pin low voltage (disabled)				0.3	V
$V_{LO}$	EN pin low voltage (disabled)	TPS74601PQWDRBRQ1 only			0.4	V
$I_{EN}$	Enable pin current	$V_{IN} = V_{EN} = 6.0\text{ V}$		10		nA
$R_{PULLDOWN}$	Pulldown resistance	$V_{IN} = 6.0\text{ V}$		95		$\Omega$
$PG_{HHTH}$	PG high threshold	$V_{OUT}$ increasing	89	92	96	$\%V_{OUT}$
$PG_{LHTH}$	PG low threshold	$V_{OUT}$ decreasing	86	90	93	$\%V_{OUT}$
$PG_{HYST}$	PG hysteresis			2		$\%V_{OUT}$
$V_{OL(PG)}$	PG pin low-level output voltage	$V_{IN} \geq 1.5\text{ V}$ , $I_{SINK} = 1\text{ mA}$ $V_{IN} \geq 2.75\text{ V}$ , $I_{SINK} = 2\text{ mA}$			300	mV
$V_{OH(PG)}$	PG pin high-level output voltage <sup>(4)</sup>	$V_{OUT} \geq 1.0\text{ V}$ , $I_{SOURCE} = 0.04\text{ mA}$ $V_{OUT} \geq 1.4\text{ V}$ , $I_{SOURCE} = 0.2\text{ mA}$ $V_{OUT} \geq 2.5\text{ V}$ , $I_{SOURCE} = 0.5\text{ mA}$ $V_{OUT} \geq 4.5\text{ V}$ , $I_{SOURCE} = 1.0\text{ mA}$	0.8 × $V_{OUT}$			V
$I_{kG(PG)}$	PG pin leakage current <sup>(5)</sup>	$V_{OUT} > PG_{HHTH}$ , $V_{PG} = 6.0\text{ V}$		7	50	nA
$T_{SD}$	Thermal shutdown	Shutdown, temperature increasing Reset, temperature decreasing		170		$^\circ\text{C}$
				155		

- (1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
- (2)  $V_{IN} = 1.5\text{ V}$  for  $V_{OUT} < 1.0\text{ V}$
- (3) Dropout is not tested for nominal output voltages below 0.65 V since the input voltage may be below UVLO.
- (4) Push-pull version only. The push-pull option is supported only for  $V_{OUT} \geq 1.0\text{ V}$ .
- (5) Open-drain version only.

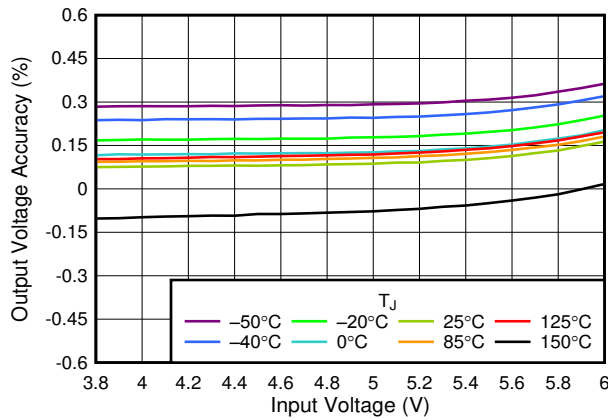
## 5.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
$t_{PGDH}$	PG delay time rising, time from 92% $V_{OUT}$ to 20% of PG <sup>(1)</sup>	135	165	178	$\mu\text{s}$
	'B' version <sup>(2)</sup>	4.5	5	5.5	ms
$t_{PGDL}$	PG delay time falling, time from 90% $V_{OUT}$ to 80% of PG <sup>(1)</sup>	1.5	7	10	$\mu\text{s}$

- (1) Output overdrive = 10%.
- (2) See the Device Nomenclature table for more information on available PG timings.

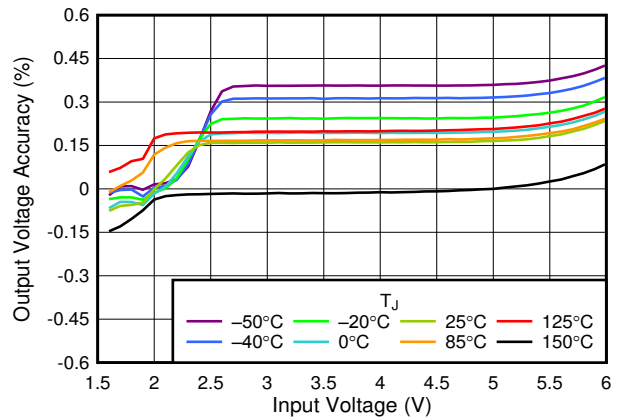
## 5.7 Typical Characteristics

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)



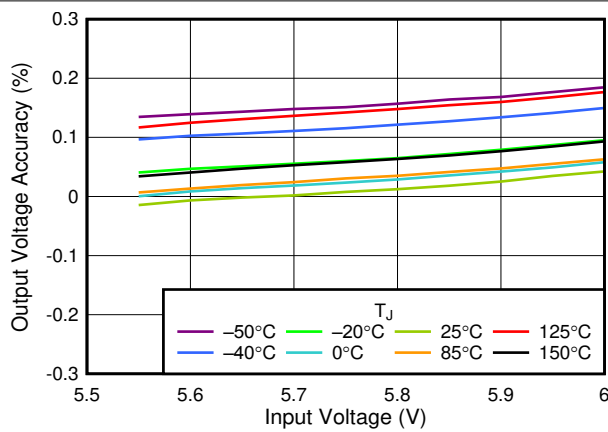
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$

5-1. 3.3-V Line Regulation vs  $V_{IN}$



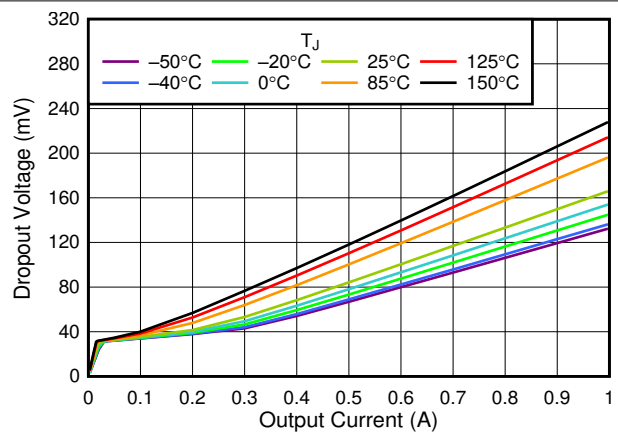
$V_{OUT} = 0.55\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$

5-2. 0.55-V Line Regulation vs  $V_{IN}$

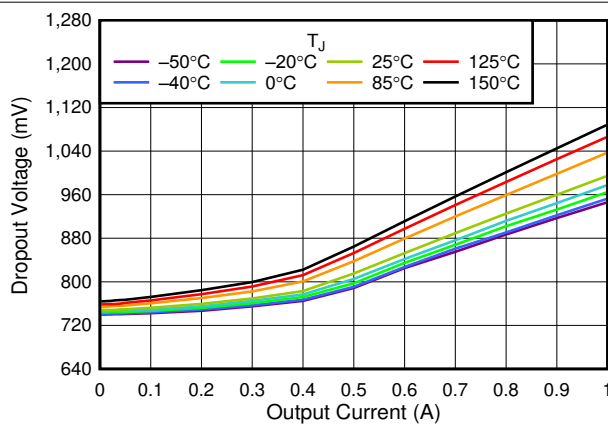


$V_{OUT} = 5.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$

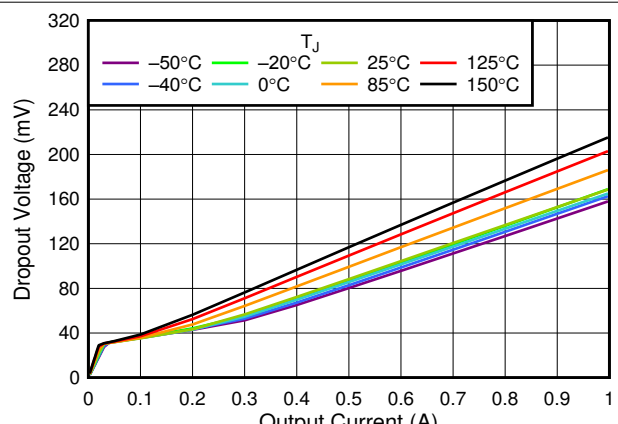
5-3. 5.5-V Line Regulation vs  $V_{IN}$



5-4. 3.3-V Dropout Voltage vs  $I_{OUT}$



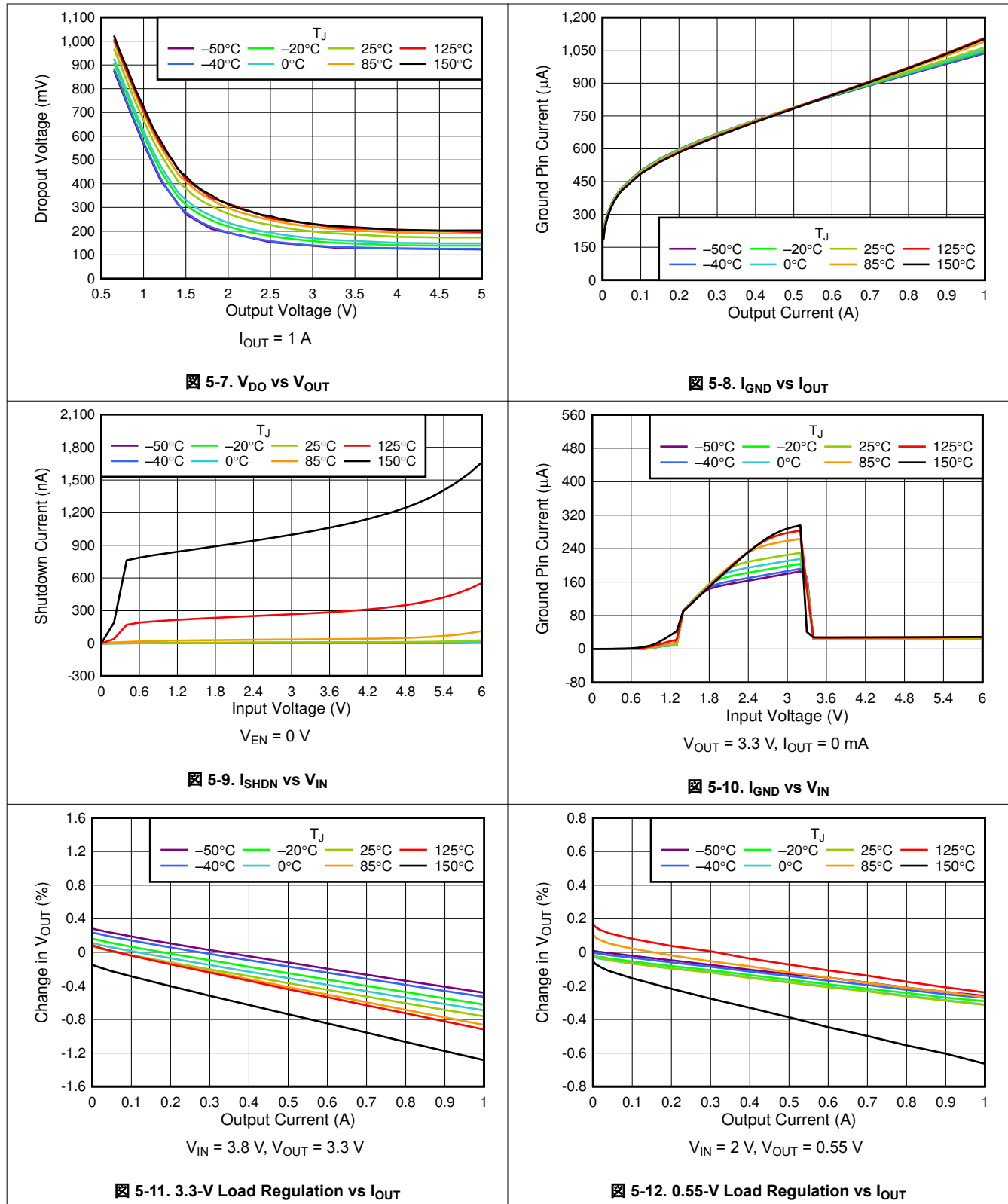
5-5. 0.55-V Dropout Voltage vs  $I_{OUT}$



5-6. 5.5-V Dropout Voltage vs  $I_{OUT}$

### 5.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)



### 5.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted)

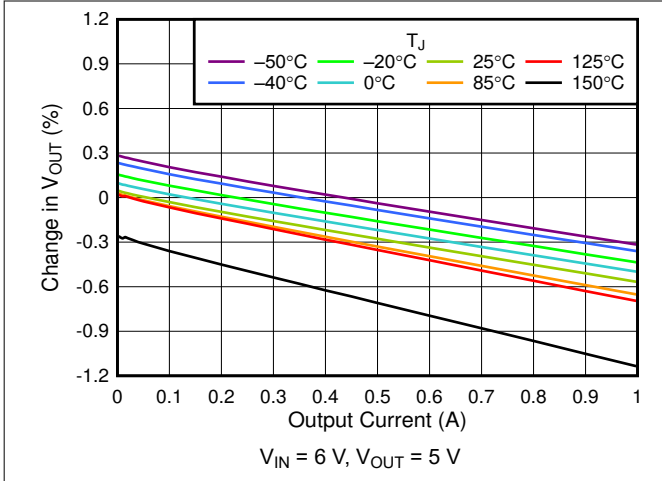


图 5-13. 5-V Load Regulation vs  $I_{OUT}$

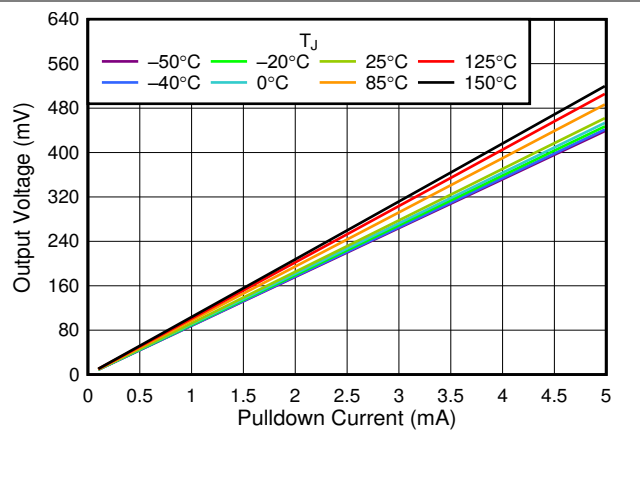


图 5-14.  $V_{OUT}$  vs  $I_{OUT}$  Pulldown Resistor

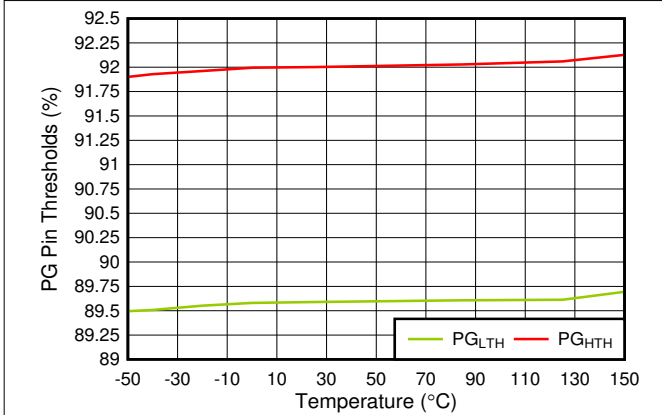


图 5-15.  $PGL_{TH}$  and  $PGH_{HTH}$  vs Temperature

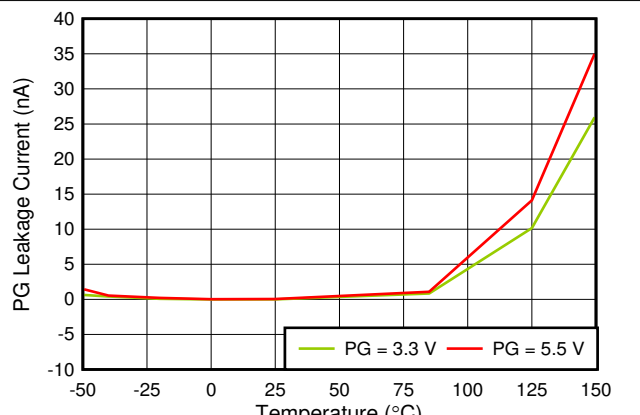
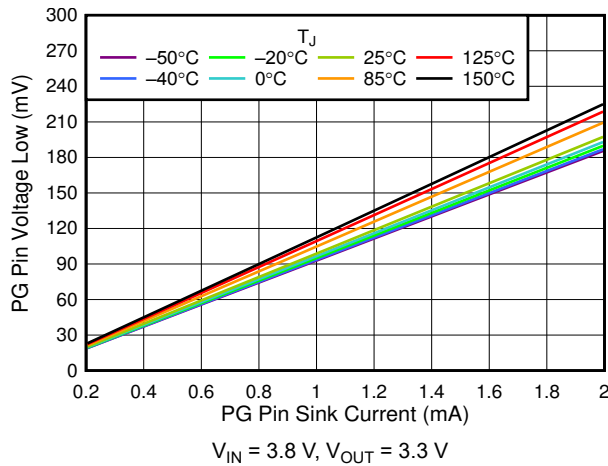


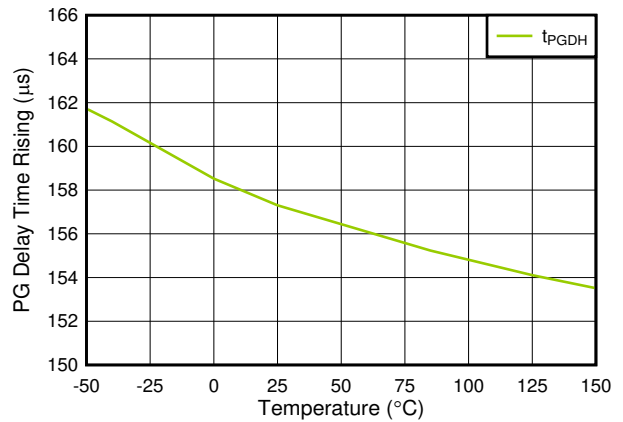
图 5-16.  $I_{kg(PG)}$  vs Temperature and PG Pin Voltage

### 5.7 Typical Characteristics (continued)

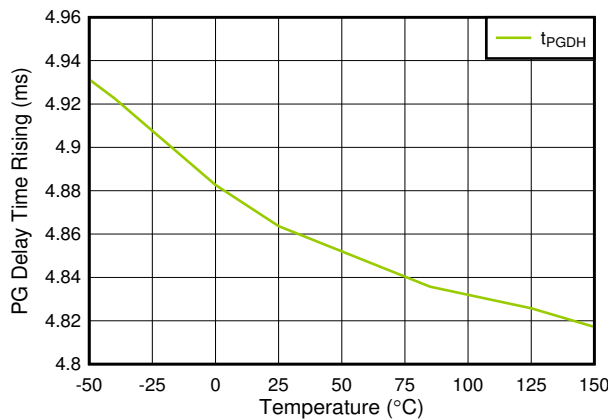
at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)



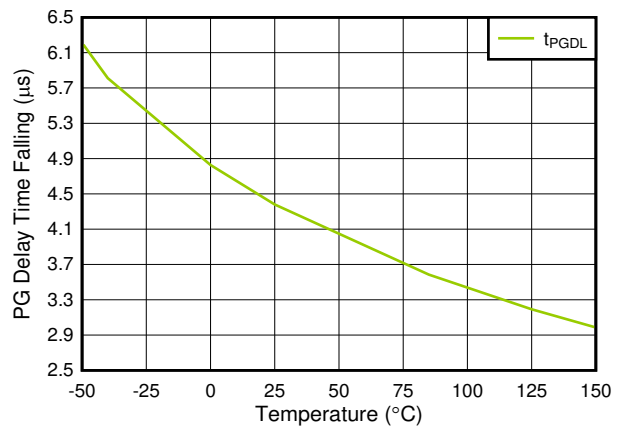
5-17.  $V_{OL(PG)}$  vs PG Pin Sink Current



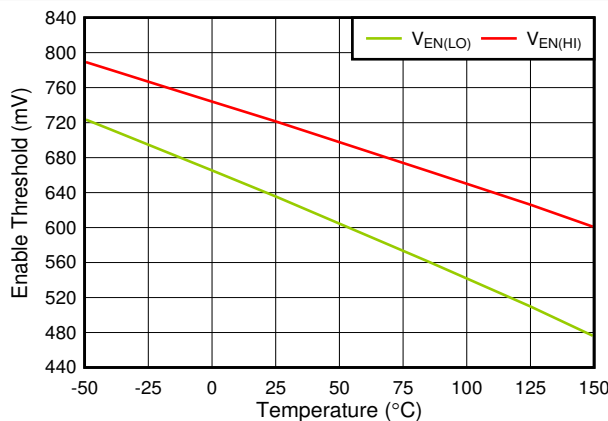
5-18.  $t_{PGDH}$  vs Temperature



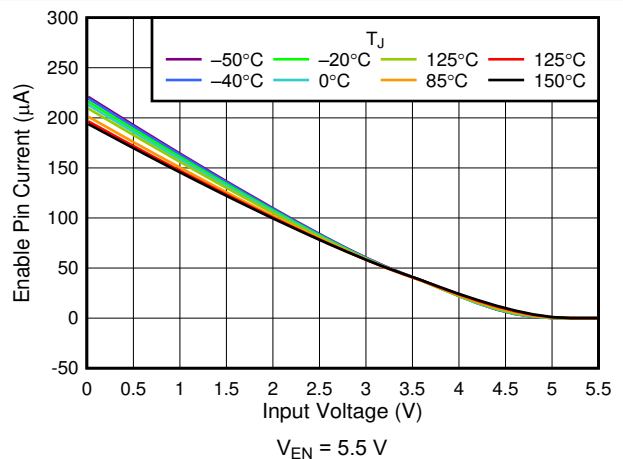
5-19.  $t_{PGDH}$  vs Temperature (For TPS746B Only)



5-20.  $t_{PGDL}$  vs Temperature



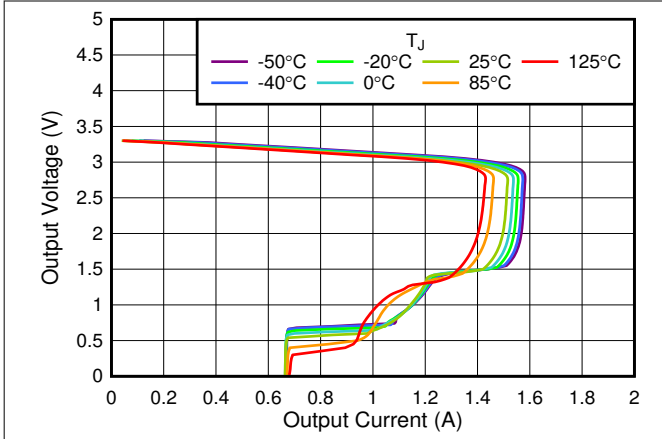
5-21.  $V_{EN(HI)}$  and  $V_{EN(LO)}$  vs Temperature



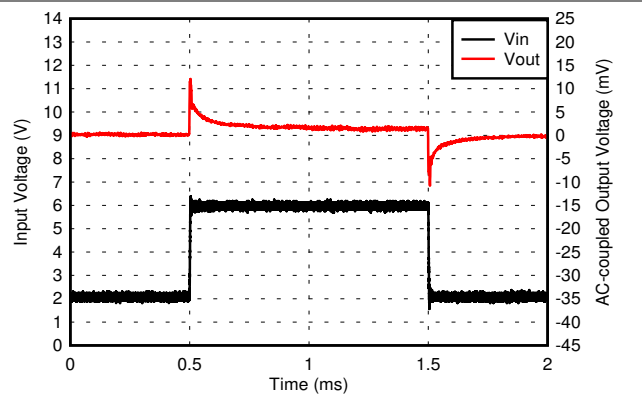
5-22.  $I_{EN}$  vs  $V_{IN}$

### 5.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)

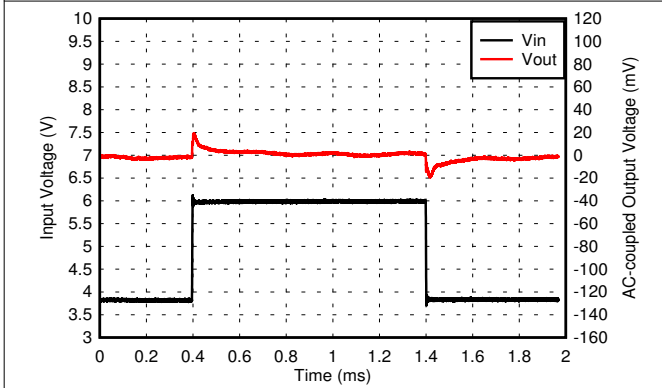


5-23. 3.3-V Foldback Current Limit vs  $I_{OUT}$



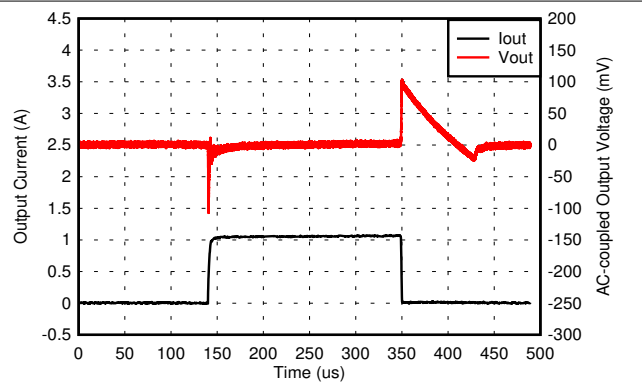
$V_{OUT} = 0.55\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{IN}$  slew rate =  $1\text{ V}/\mu\text{s}$

5-24. 0.55-V Line Transient



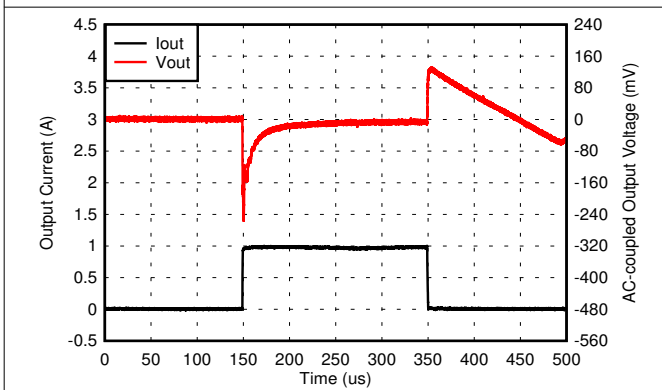
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{IN}$  slew rate =  $1\text{ V}/\mu\text{s}$

5-25. 3.3-V Line Transient



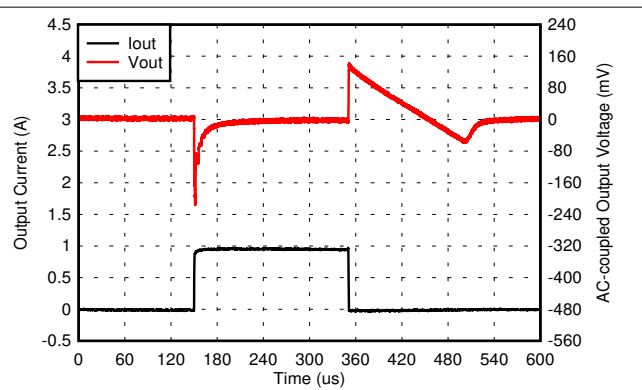
$V_{OUT} = 0.55\text{ V}$ ,  $V_{IN} = 2\text{ V}$ ,  $I_{OUT}$  slew rate =  $1\text{ A}/\mu\text{s}$

5-26. 1-mA to 1-A Load Transient (0.55 V)



$V_{OUT} = 5\text{ V}$ ,  $V_{IN} = 5.5\text{ V}$ ,  $I_{OUT}$  slew rate =  $1\text{ A}/\mu\text{s}$

5-27. 1-mA to 1-A Load Transient (5 V)

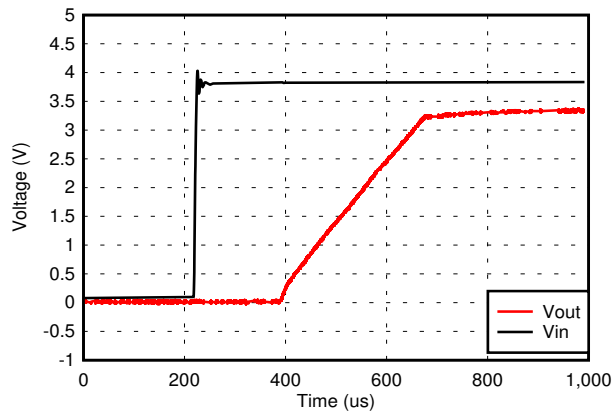


$V_{OUT} = 3.3\text{ V}$ ,  $V_{IN} = 3.8\text{ V}$ ,  $I_{OUT}$  slew rate =  $1\text{ A}/\mu\text{s}$

5-28. 1-mA to 1-A Load Transient (3.3 V)

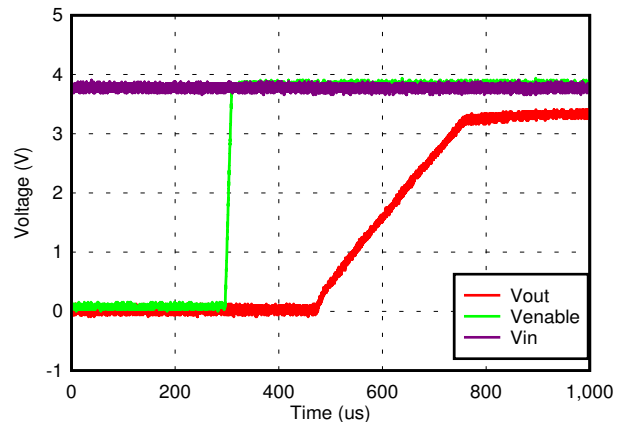
## 5.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)



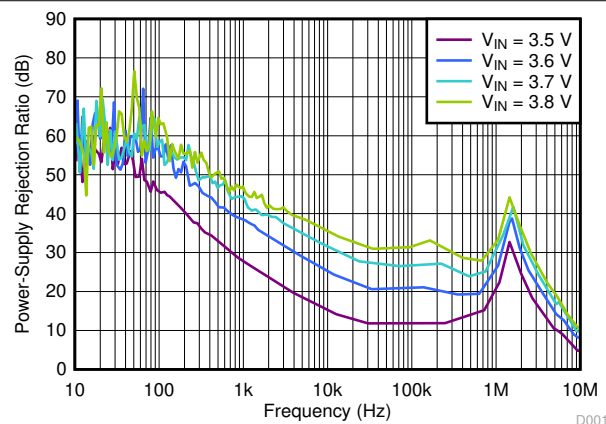
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$

Figure 5-29.  $V_{IN}$  Power-Up



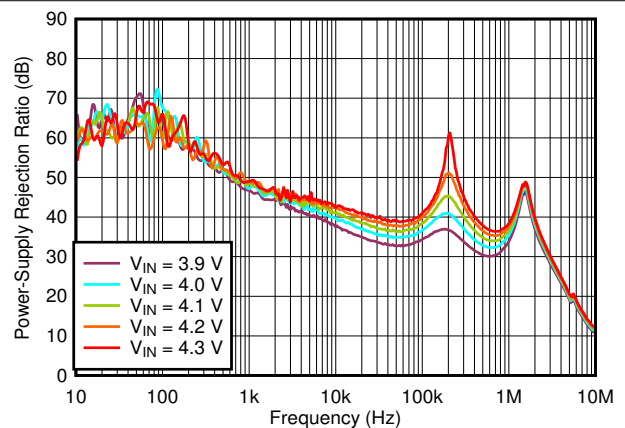
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$

Figure 5-30. Startup With EN



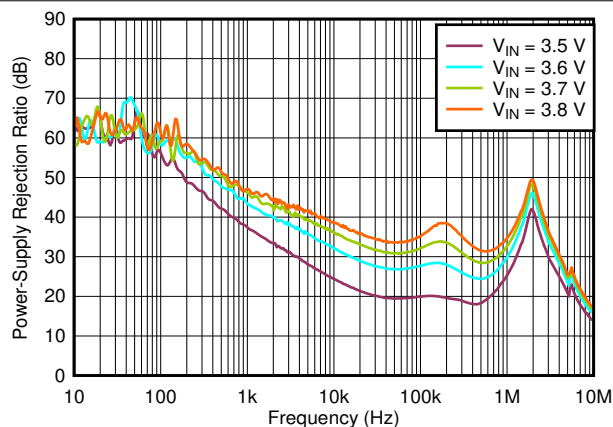
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$

Figure 5-31. PSRR vs Frequency and  $V_{IN}$



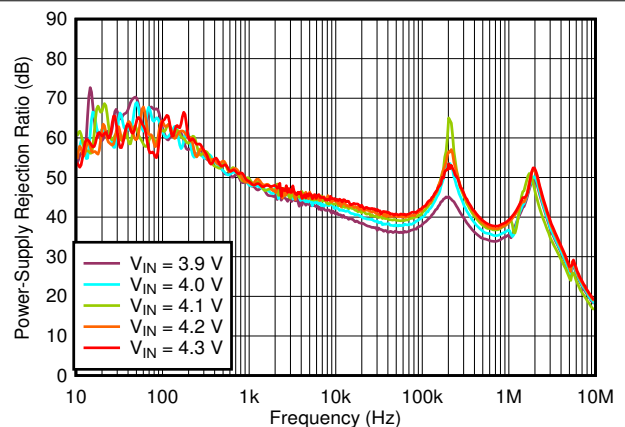
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$

Figure 5-32. PSRR vs Frequency and  $V_{IN}$



$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 250\text{ mA}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$

Figure 5-33. PSRR vs Frequency and  $V_{IN}$

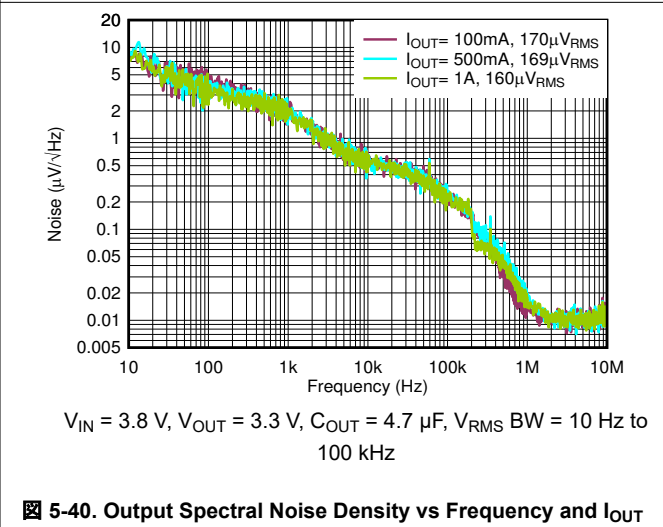
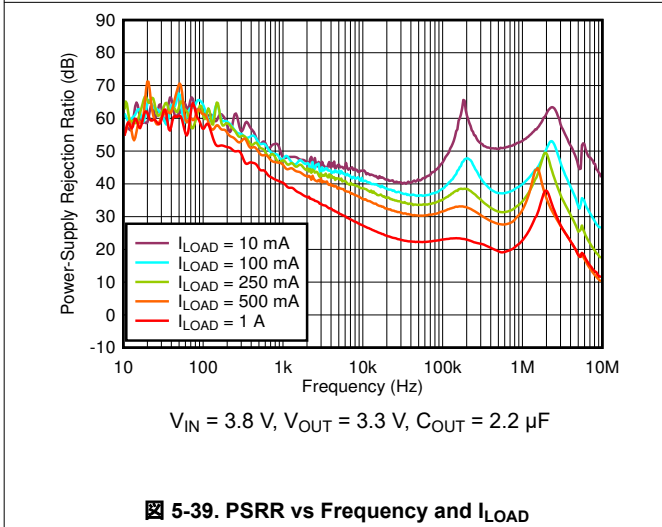
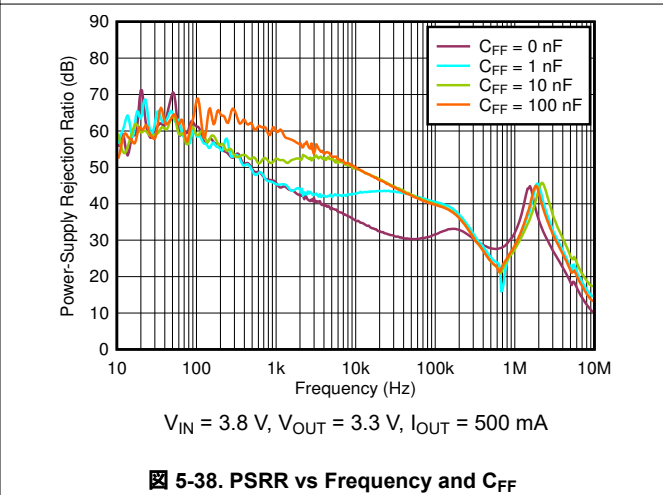
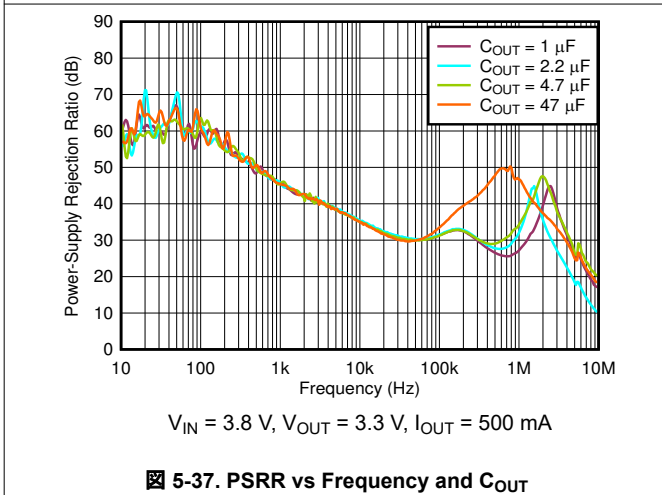
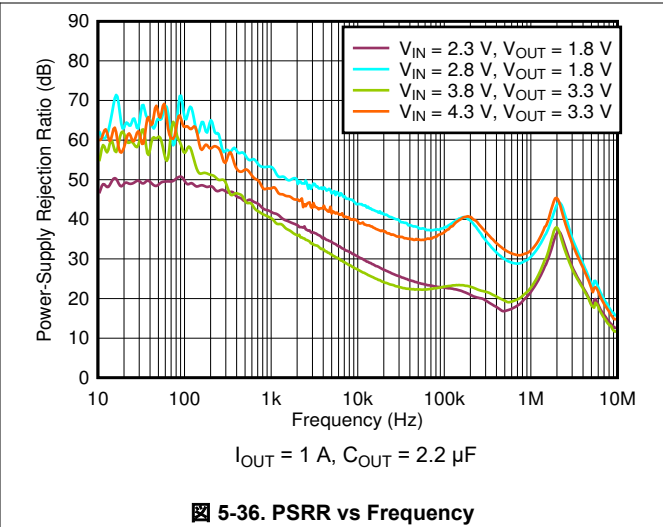
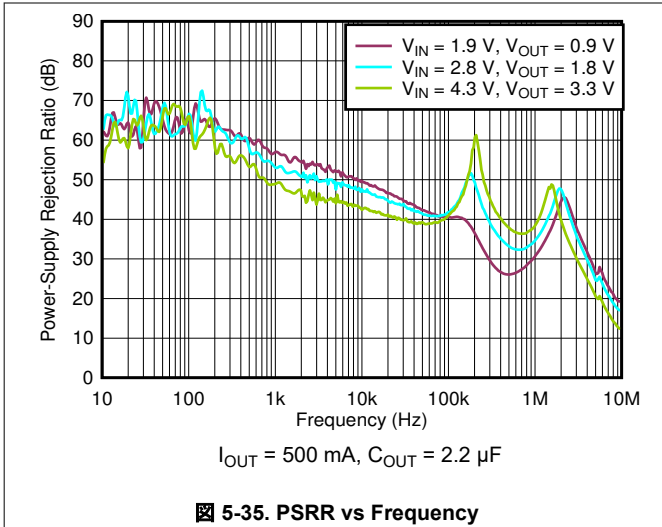


$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 250\text{ mA}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$

Figure 5-34. PSRR vs Frequency and  $V_{IN}$

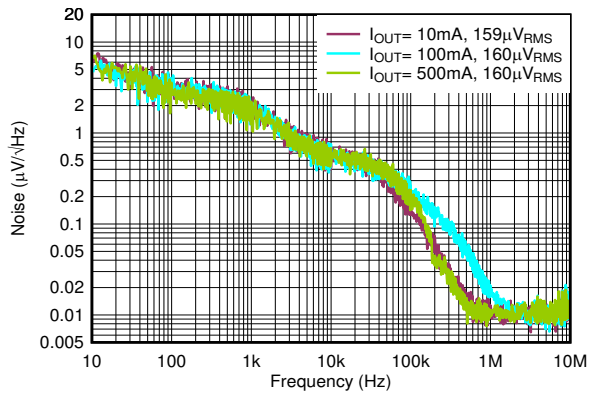
### 5.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted)



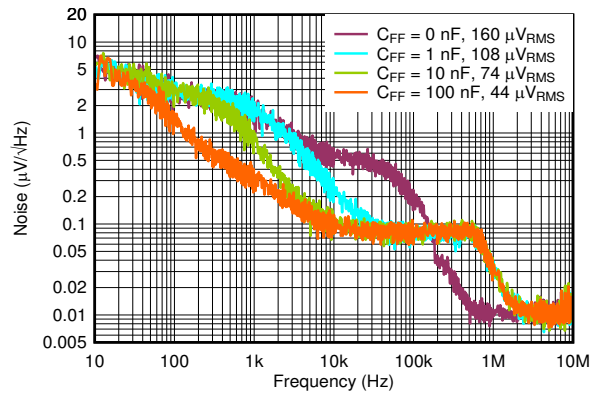
### 5.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted)



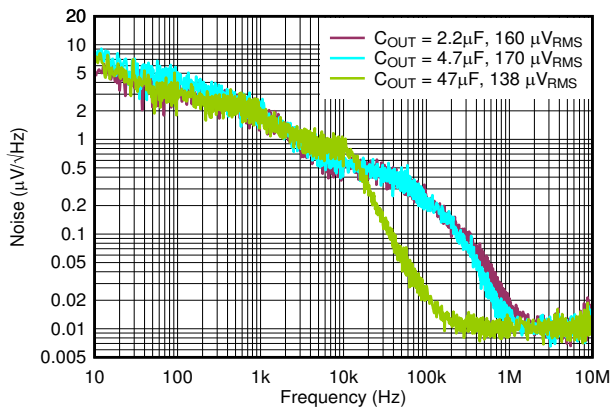
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

Figure 5-41. Output Spectral Noise Density vs Frequency and  $I_{OUT}$



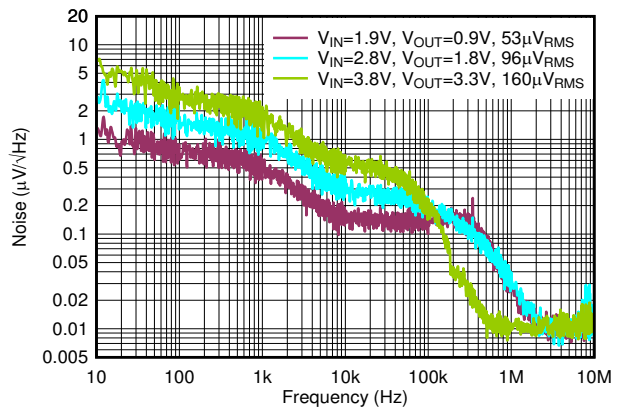
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

Figure 5-42. Output Spectral Noise Density vs Frequency and  $C_{FF}$



$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$ ,  $C_{FF} = 0\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

Figure 5-43. Output Spectral Noise Density vs Frequency and  $C_{OUT}$



$I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

Figure 5-44. Output Spectral Noise Density vs Frequency

## 6 Detailed Description

### 6.1 Overview

The TPS746-Q1 is a low-dropout regulator (LDO) that consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device ideal for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ .

### 6.2 Functional Block Diagrams

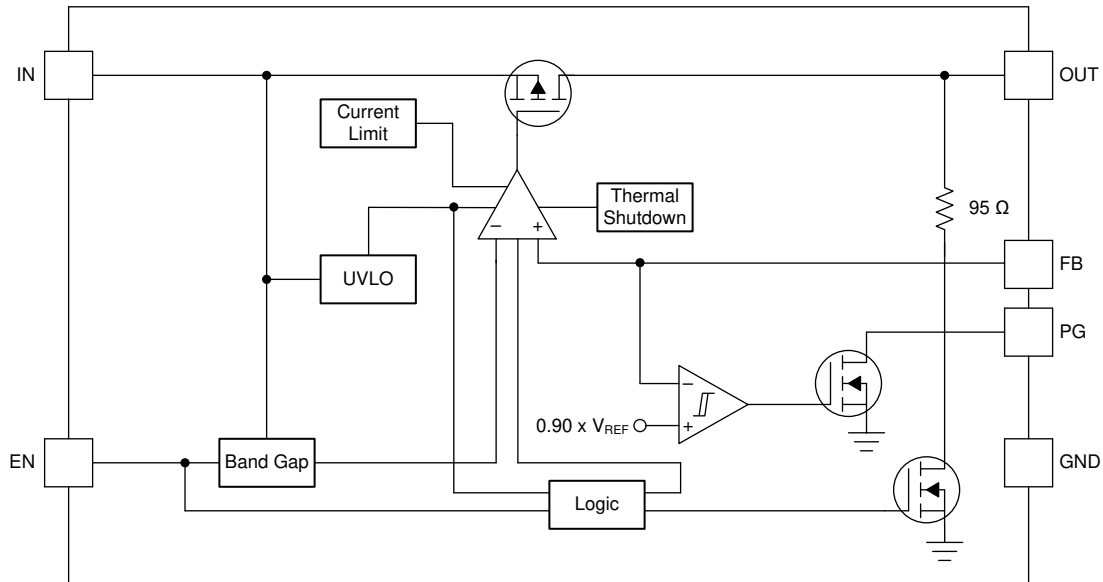


図 6-1. Adjustable Version With Open-Drain Power-Good

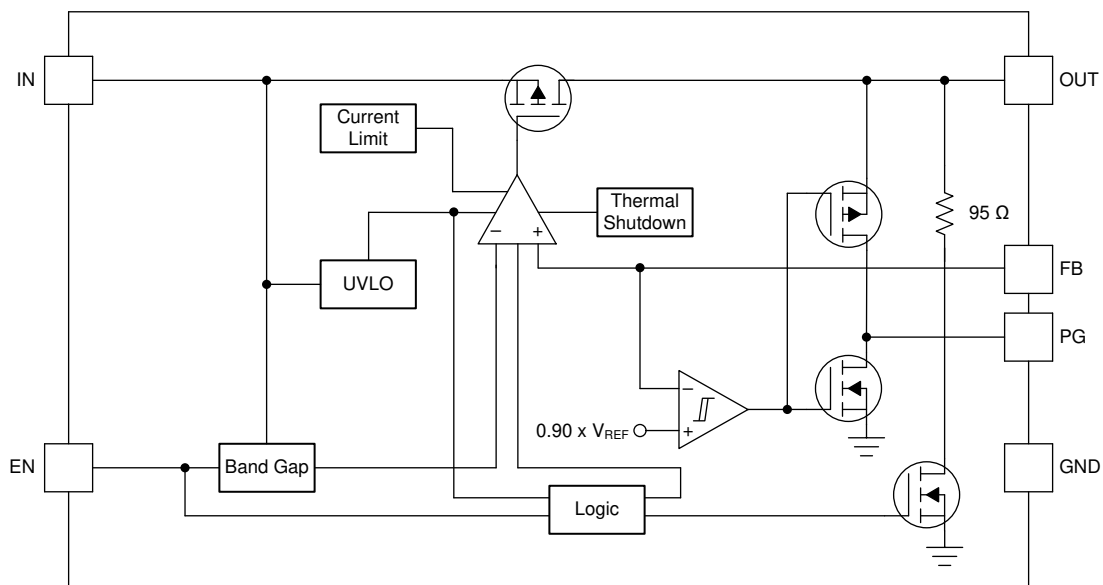


図 6-2. Adjustable Version With Push-Pull Power-Good

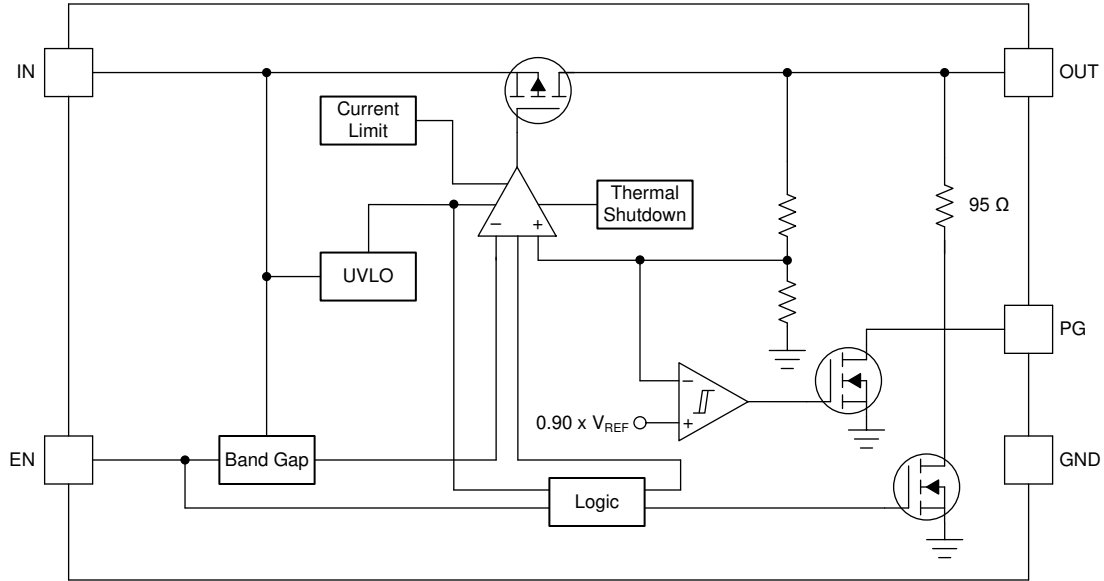


図 6-3. Fixed Voltage Version With Open-Drain Power-Good

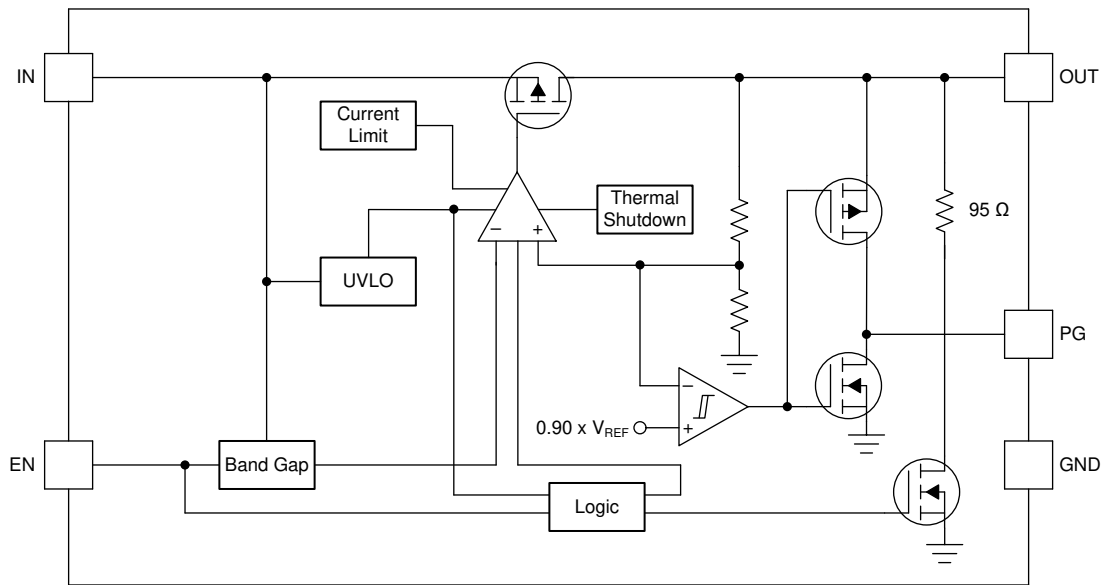


図 6-4. Fixed Voltage Version With Push-Pull Power-Good

## 6.3 Feature Description

### 6.3.1 Undervoltage Lockout (UVLO)

The TPS746-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage ( $V_{UVLO}$ ). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When  $V_{IN}$  is less than  $V_{UVLO}$ , the output is connected to ground with a pulldown resistor ( $R_{PULLDOWN}$ ).

### 6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed  $V_{EN(HI)}$ . Turn off the device by forcing the EN pin to drop below  $V_{EN(LO)}$ . If shutdown capability is not required, connect EN to IN.

The TPS746-Q1 has an internal pulldown MOSFET that connects an  $R_{PULLDOWN}$  resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance ( $C_{OUT}$ ) and the load resistance ( $R_L$ ) in parallel with the pulldown resistor ( $R_{PULLDOWN}$ ). [式 1](#) calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$

### 6.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ( $V_{FOLDBACK}$ ). In a high-load current fault with the output voltage above  $V_{FOLDBACK}$ , the brick-wall scheme limits the output current to the current limit ( $I_{CL}$ ). When the voltage drops below  $V_{FOLDBACK}$ , a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ( $I_{SC}$ ).  $I_{CL}$  and  $I_{SC}$  are listed in the *Electrical Characteristics* table.

For this device,  $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$ .

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{CL}]$ . When the device output is shorted and the output is below  $V_{FOLDBACK}$ , the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{SC}]$ . If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application note](#).

Figure 6-5 shows a diagram of the foldback current limit.

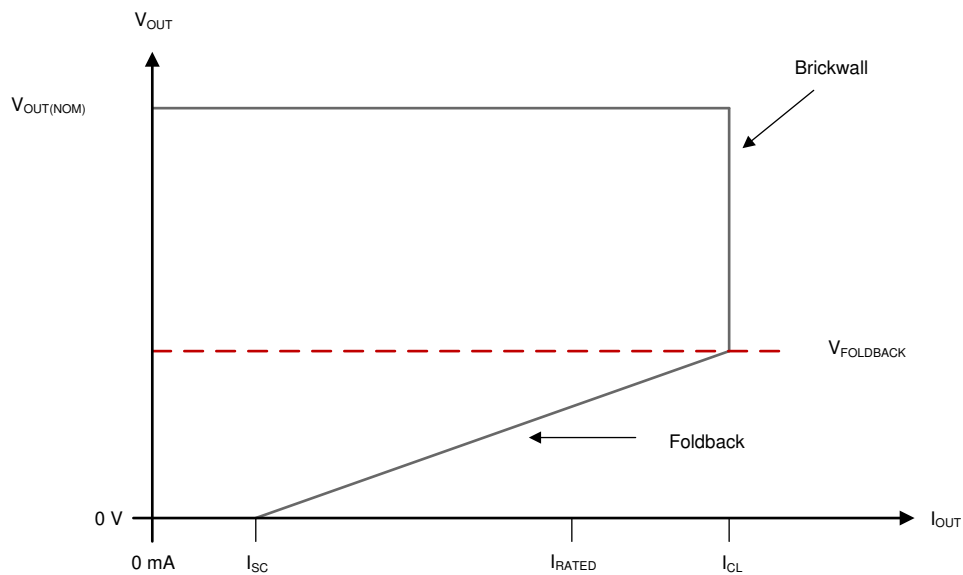


Figure 6-5. Foldback Current Limit

### 6.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately  $170^{\circ}\text{C}$ . Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately  $155^{\circ}\text{C}$ , the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the  $(V_{IN} - V_{OUT})$  voltage and the load current. For reliable operation limit junction temperature to  $125^{\circ}\text{C}$ , maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS746-Q1 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS746-Q1 into thermal shutdown degrades device reliability.

## 6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**表 6-1. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER			
	$V_{IN}$	$V_{EN}$	$I_{OUT}$	$T_J$
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ( $V_{OUT(nom)} + V_{DO}$ )
- The output current is less than the current limit ( $I_{OUT} < I_{CL}$ )
- The device junction temperature is less than the thermal shutdown temperature ( $T_J < T_{SD}$ )
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout,  $V_{IN} < V_{OUT(NOM)} + V_{DO}$ , directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ( $V_{OUT(NOM)} + V_{DO}$ ), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 6.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Application Information

#### 7.1.1 Adjustable Device Feedback Resistors

図 7-1 shows that the output voltage of the TPS746P-Q1 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

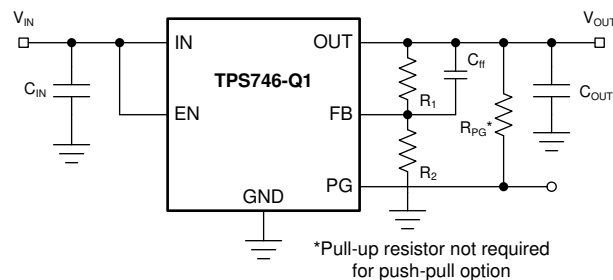


図 7-1. Adjustable Operation

The adjustable-version device requires external feedback divider resistors to set the output voltage.  $V_{OUT}$  is set using the feedback divider resistors,  $R_1$  and  $R_2$ , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the  $V_{OUT}$  equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

#### 7.1.2 Input and Output Capacitor Selection

The TPS746-Q1 requires an output capacitance of 0.47  $\mu\text{F}$  or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220  $\mu\text{F}$ .

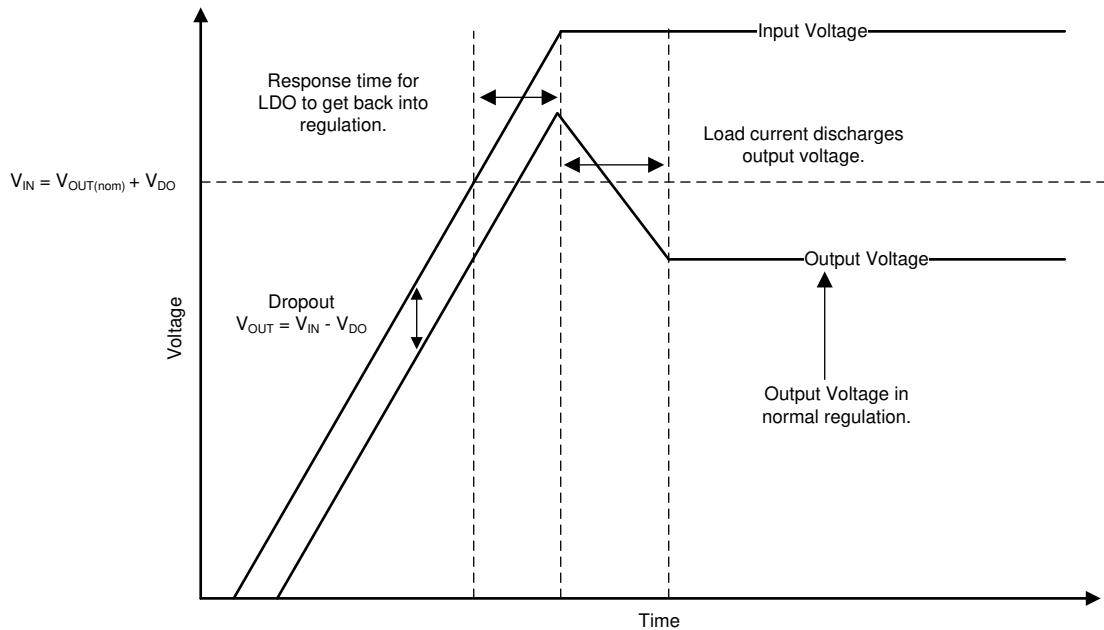
Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

### 7.1.3 Dropout Voltage

The TPS746-Q1 uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as  $(V_{IN} - V_{OUT})$  approaches dropout operation.

### 7.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on  $V_{IN}$  during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in [Figure 7-2](#), when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.



**Figure 7-2. Start-Up Into Dropout**

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. [Figure 7-3](#) illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage ( $V_{GS}$ ) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

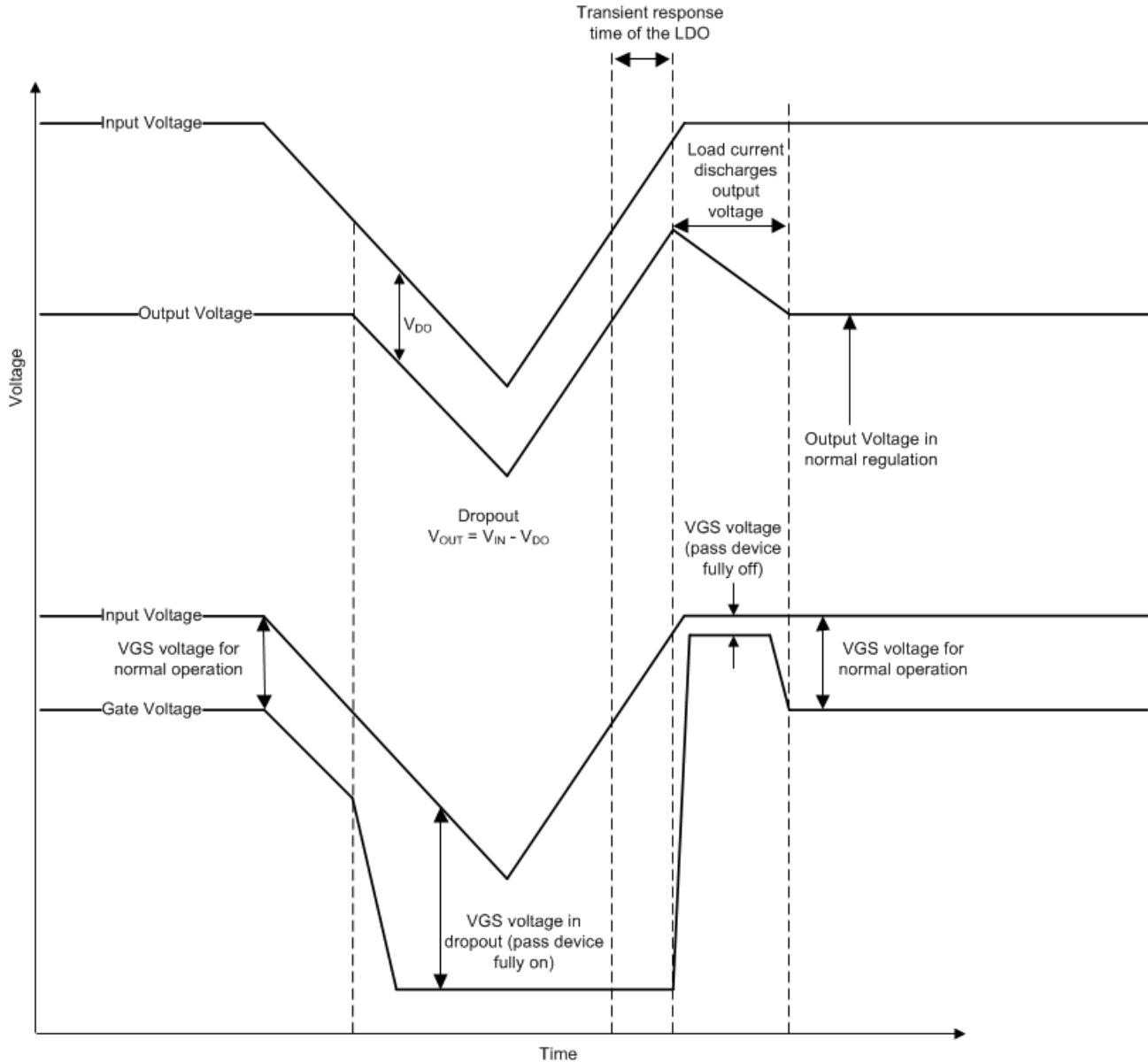


图 7-3. Line Transients From Dropout

### 7.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.


Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

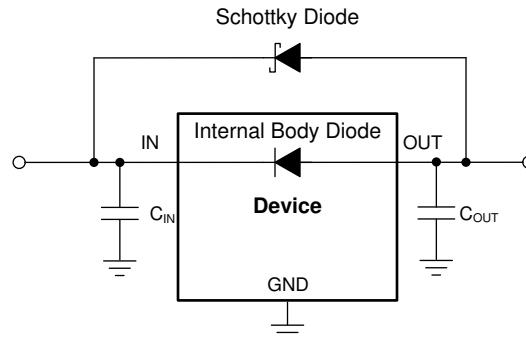
- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of  $V_{OUT} > V_{IN} + 0.3\text{ V}$ :

- If the device has a large  $C_{OUT}$  and the input supply collapses with little or no load current

- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device.  7-4 shows one approach of protecting the device.



**図 7-4. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 7.1.6 Power Dissipation ( $P_D$ )

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 式 4 calculates power dissipation ( $P_D$ ).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

#### 注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ( $T_A$ ) for the device. According to 式 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ( $R_{\theta JA}$ ) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

Figure 7-5 and Figure 7-6 show the functions of  $R_{\theta JA}$  and  $\psi_{JB}$  versus copper area and thickness. These plots are generated with a 101.6-mm × 101.6-mm × 1.6-mm PCB of two and four layers. For the four layer board, the inner planes use 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 2 x 1 array of thermal vias of 300- $\mu$ m drill diameter and 25- $\mu$ m copper (Cu) plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area, as shown in Figure 7-7.

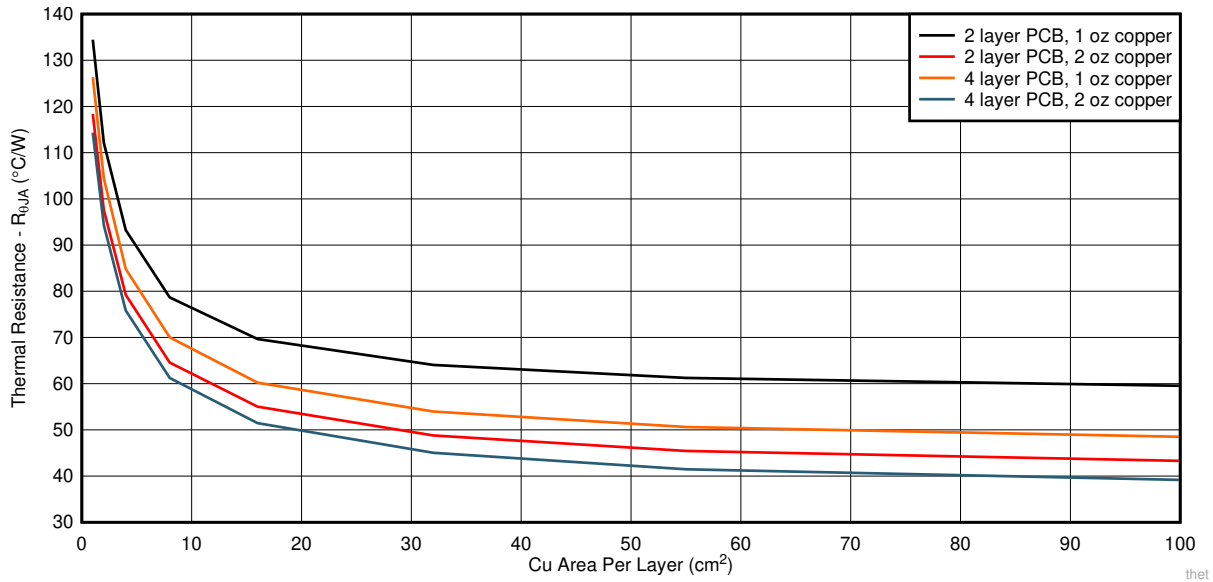


Figure 7-5.  $R_{\theta JA}$  versus Cu Area for the WSON (DRV) Package

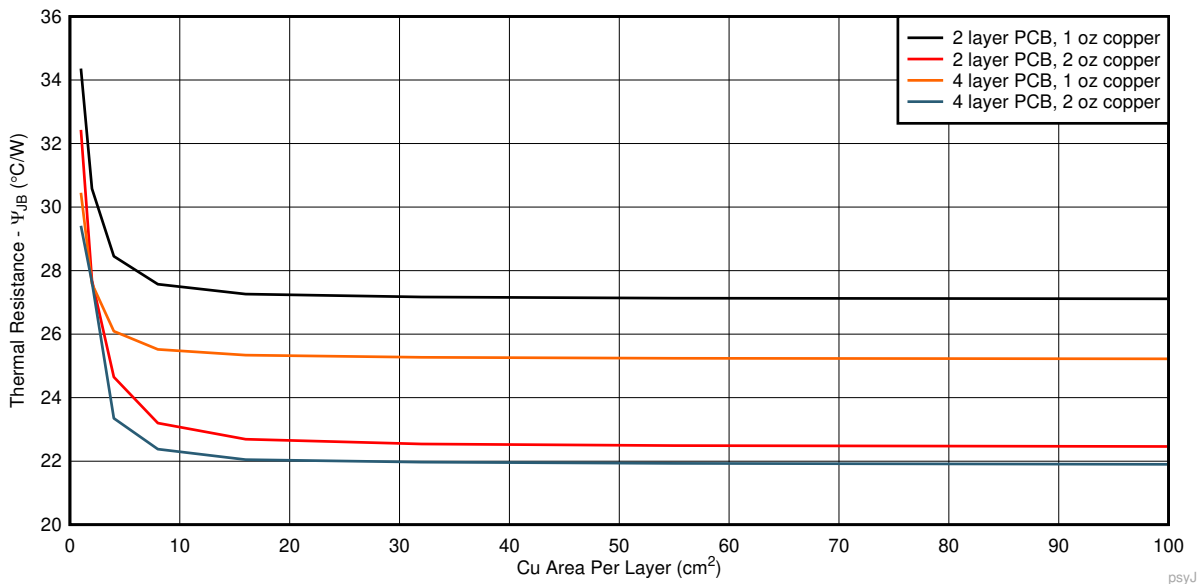
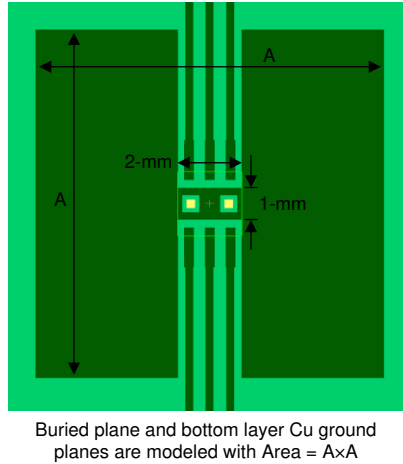


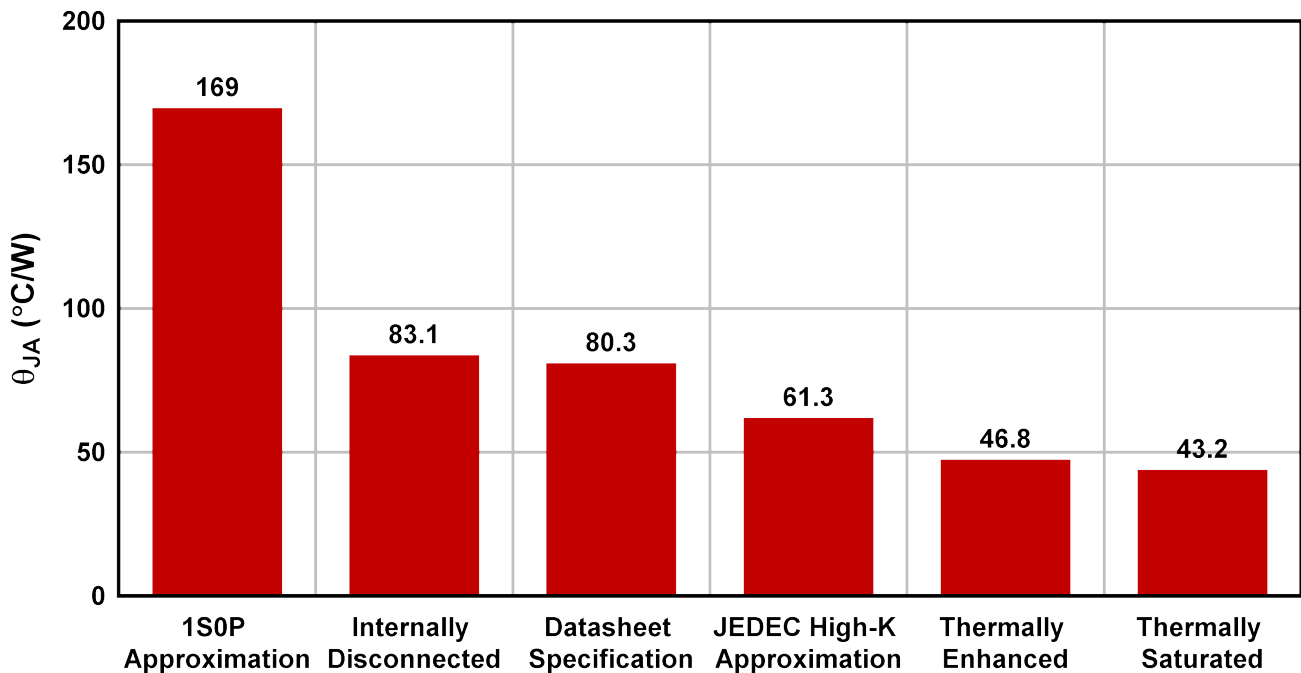
Figure 7-6.  $\psi_{JB}$  versus Cu Area for the WSON (DRV) Package

As shown in 7-7, each of the layers has a copper plane of equal area.



7-7. Board Parameters Used for Simulation

For a more comprehensive study of how thermal resistance varies with copper area and thickness, see the [An Empirical Analysis of the Impact of Board Layout on LDO Thermal Performance application note](#). As shown in 7-8, modifying board layout to be more thermally enhanced can lower the  $R_{\theta JA}$  value from 80.3°C/W to 46.8°C/W or better.



7-8. TPS746-Q1 (WSO)  $R_{\theta JA}$  vs Board Layout

### 7.1.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage ( $PG_{LTH}$ ), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds  $PG_{HTH}$ , the PG pin becomes high impedance. The open-drain output requires a pullup resistor. By connecting a pullup resistor to an external

supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Additionally, the open-drain output can be tied to other open-drain outputs to implement AND logic. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 k $\Omega$  to 100 k $\Omega$  is recommended. The push-pull power-good output option does not require the pullup resistor and instead has a high logic signal that correlates with the output voltage of the device. The push-pull option is supported only for  $V_{OUT} \geq 1.0$  V. Do not tie the push-pull output to other logic outputs.

When using a feed-forward capacitor ( $C_{FF}$ ), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note](#).

The state of PG is only valid when the device operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

#### 7.1.8 Feed-Forward Capacitor ( $C_{FF}$ )

For the adjustable-voltage version device, a feed-forward capacitor ( $C_{FF}$ ) can be connected from the OUT pin to the FB pin.  $C_{FF}$  improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended  $C_{FF}$  values are listed in the *Recommended Operating Conditions* table. A higher capacitance  $C_{FF}$  can be used; however, the startup time increases. For a detailed description of  $C_{FF}$  tradeoffs, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note](#).

#### 7.1.9 Start-Up Sequencing

If  $V_{EN}$  is greater than  $V_{UVLO}$  rising (min), the input pin (IN) must sink 1 mA of current to avoid the device being turned on with a floating input pin.

## 7.2 Typical Application

Figure 7-9 shows the typical application circuit for the TPS746P-Q1. Input and output capacitances must be at least 1  $\mu\text{F}$ .

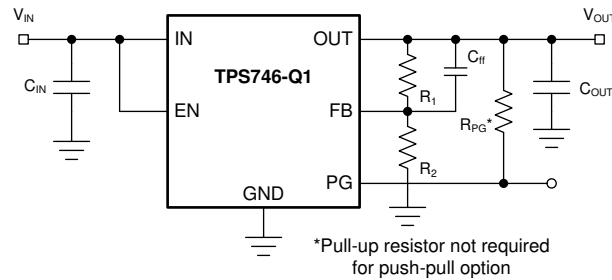


Figure 7-9. TPS746-Q1 Typical Application

### 7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for typical linear regulator applications.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	3.3 V, $\pm 1\%$
Input current	1.2 A (maximum)
Output load	1-A DC
Maximum ambient temperature	70°C

### 7.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2  $\mu\text{F}$  are selected to give the maximum output capacitance in a small, low-cost package; see the [Input and Output Capacitor Selection](#) section for details.

Figure 7-1 illustrates the output voltage of the TPS746-Q1. Set the output voltage using the resistor divider; see the [Adjustable Device Feedback Resistors](#) section for details.

#### 7.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 6 to calculate the current through the input.

$$I_{OUT(t)} = \left[ \frac{C_{OUT} \times dV_{OUT(t)}}{dt} \right] + \left[ \frac{V_{OUT(t)}}{R_{LOAD}} \right] \quad (6)$$

where:

- $V_{OUT(t)}$  is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT(t)} / dt$  is the slope of the  $V_{OUT}$  ramp
- $R_{LOAD}$  is the resistive load impedance

### 7.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) and the total power dissipation ( $P_D$ ). Use 式 7 to calculate the power dissipation. Multiply  $P_D$  by  $R_{\theta JA}$  as 式 8 shows and add the ambient temperature ( $T_A$ ) to calculate the junction temperature ( $T_J$ ).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (7)$$

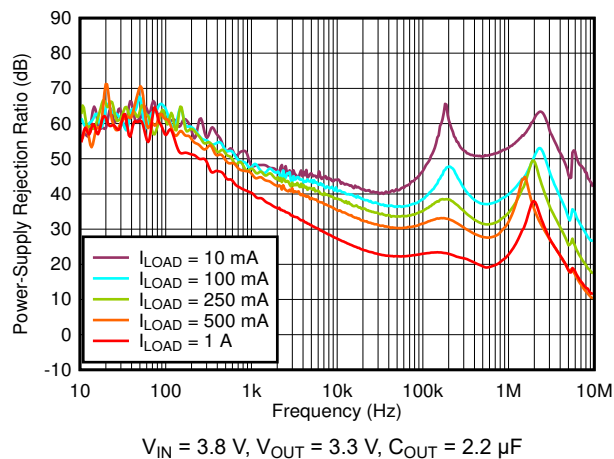
$$T_J = R_{\theta JA} \times P_D + T_A \quad (8)$$

Calculate the maximum ambient temperature as 式 9 shows if the ( $T_{J(MAX)}$ ) value does not exceed 125°C. 式 10 calculates the maximum ambient temperature with a value of 109.85°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (9)$$

$$T_{A(MAX)} = 150^\circ\text{C} - 80.3^\circ\text{C/W} \times (3.8\text{ V} - 3.3\text{ V}) \times (1\text{ A}) = 109.85^\circ\text{C} \quad (10)$$

### 7.2.3 Application Curve



7-10. PSRR vs Frequency and  $I_{LOAD}$

## 7.3 Power Supply Recommendations

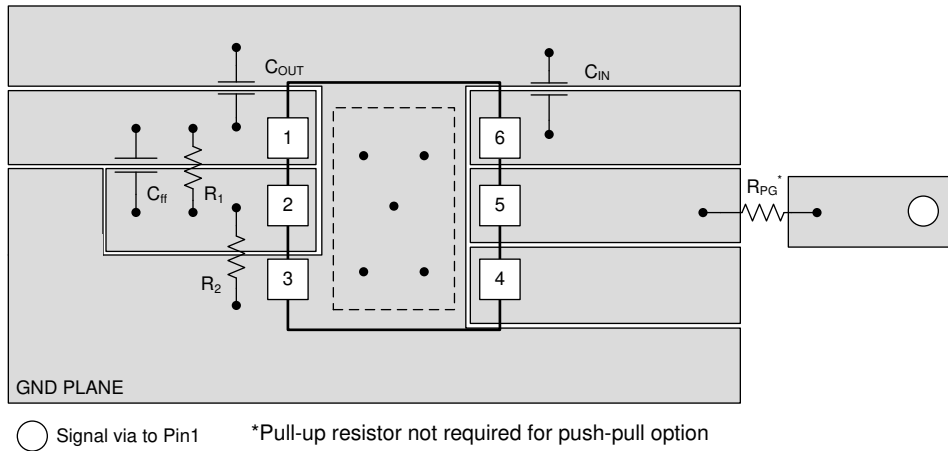
The TPS746-Q1 is designed to operate from an input voltage supply range from 1.5 V to 6.0 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR may help improve output noise performance. Connect a low output impedance power supply directly to the IN pin of the TPS746-Q1.

## 7.4 Layout

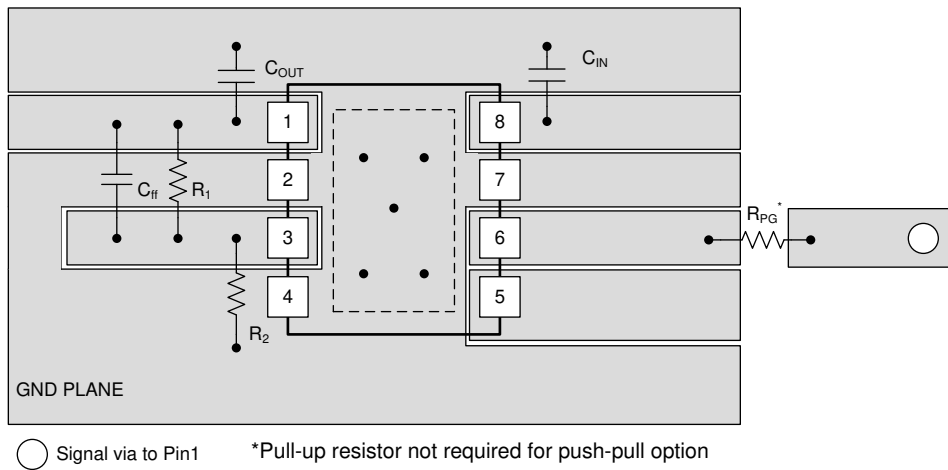
### 7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Place a tented thermal via directly beneath the thermal pad of the DRV or DRB package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

### 7.4.2 Layout Examples



**7-11. Layout Example for the DRV Package**



**7-12. Layout Example for the DRB package**

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Device Nomenclature

表 8-1. Device Nomenclature (1) (2)

PRODUCT	V <sub>OUT</sub>
TPS746)xx(x)PvQWyyyzQ1	<p><b>xx(x)</b> is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V; 01 = adjustable).</p> <p><b>P</b> indicates an active output discharge feature. All members of the TPS746 family will actively discharge the output when the device is disabled.</p> <p><b>v</b> indicates the topology of the power-good output and the timing associated with the power-good delay.</p> <ul style="list-style-type: none"> <li>If unused, indicates an open-drain power-good output with a 150-<math>\mu</math>s delay.</li> <li>If <b>B</b>, indicates an open-drain, power-good output with a 5-ms delay.</li> <li>If <b>C</b>, indicates a push-pull, power-good output with a 150-<math>\mu</math>s delay.</li> </ul> <p><b>Q</b> indicates that this device is a Grade-1 device in accordance with the AEC-Q100 standard.</p> <p><b>W</b> indicates the package has wettable flanks.</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity. R is for reel (3000 pieces).</p> <p><b>Q1</b> indicates that this device is an automotive grade (AEC-Q100) device.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).
- (2) Output voltages from 0.65 V to 5.0 V in 50-mV increments are available. Contact the factory for details and availability.

### 8.2 Documentation Support

#### 8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note](#)
- Texas Instruments, [An Empirical Analysis of the Impact of Board Layout on LDO Thermal Performance application note](#)

### 8.3 ドキュメントの更新通知を受け取る方法

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## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (May 2022) to Revision D (April 2025)	Page
• Added new VLO spec line for TPS74601PQWDRBRQ1.....	5

Changes from Revision B (January 2021) to Revision C (May 2022)	Page
• DRB $R_{\theta JA}$ を 62.0°C/W から 55.5°C/W に変更し、機能安全の箇条書き項目を追加 .....	1
• ドキュメント全体で、DRB パッケージについて WSON を VSON に変更 .....	1
• Updated thermal table to reflect correct values and package name.....	5

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS74601PBQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1S46
TPS74601PBQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1S46
<a href="#">TPS74601PCQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1OZ6
TPS74601PCQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1OZ6
<a href="#">TPS74601PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74601P
TPS74601PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74601P
<a href="#">TPS74601PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1OW6
TPS74601PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1OW6
<a href="#">TPS74610PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74610P
TPS74610PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74610P
<a href="#">TPS74610PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SG6
TPS74610PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SG6
<a href="#">TPS746115PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	746115
TPS746115PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	746115
<a href="#">TPS74611PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74611P
TPS74611PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74611P
<a href="#">TPS74611PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SH6
TPS74611PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SH6
<a href="#">TPS746125PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	746125
TPS746125PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	746125
<a href="#">TPS74612PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74612P
TPS74612PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74612P
<a href="#">TPS74612PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1S16
TPS74612PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1S16
<a href="#">TPS746135PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	746135
TPS746135PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	746135
<a href="#">TPS74613PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74613P
TPS74613PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74613P
<a href="#">TPS74615PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74615P

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74615PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74615P
<a href="#">TPS74615PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SJ6
TPS74615PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SJ6
<a href="#">TPS74617PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74617P
TPS74617PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74617P
<a href="#">TPS74618PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74618P
TPS74618PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74618P
<a href="#">TPS74618PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SK6
TPS74618PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SK6
<a href="#">TPS74625PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74625P
TPS74625PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74625P
<a href="#">TPS74625PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SL6
TPS74625PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SL6
<a href="#">TPS74628PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SM6
TPS74628PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SM6
<a href="#">TPS74629PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SN6
TPS74629PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SN6
<a href="#">TPS74630PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74630P
TPS74630PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74630P
<a href="#">TPS74633PCQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1P16
TPS74633PCQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1P16
<a href="#">TPS74633PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74633P
TPS74633PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74633P
<a href="#">TPS74633PQWDRVRQ1</a>	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1OX6
TPS74633PQWDRVRQ1.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1OX6
<a href="#">TPS74634PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74634P
TPS74634PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74634P
<a href="#">TPS74650PQWDRBRQ1</a>	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74650P
TPS74650PQWDRBRQ1.A	Active	Production	SON (DRB)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74650P

(1) **Status:** For more details on status, see our [product life cycle](#).

- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS746-Q1 :**

- Catalog : [TPS746](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74601PBQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74601PCQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74601PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74601PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74610PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74610PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS746115PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74611PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74611PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS746125PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74612PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74612PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS746135PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74613PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74615PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74615PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74617PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74618PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74618PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74625PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74625PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74628PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74629PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74630PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74633PCWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74633PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74633PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74634PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74650PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74601PBQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74601PCQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74601PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74601PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74610PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74610PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS746115PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74611PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74611PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS746125PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74612PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74612PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS746135PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74613PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74615PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74615PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74617PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74618PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74618PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74625PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74625PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74628PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74629PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74630PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74633PCQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74633PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74633PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74634PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74650PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

DRV 6

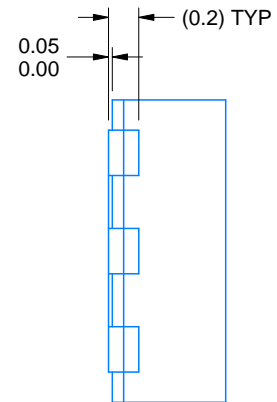
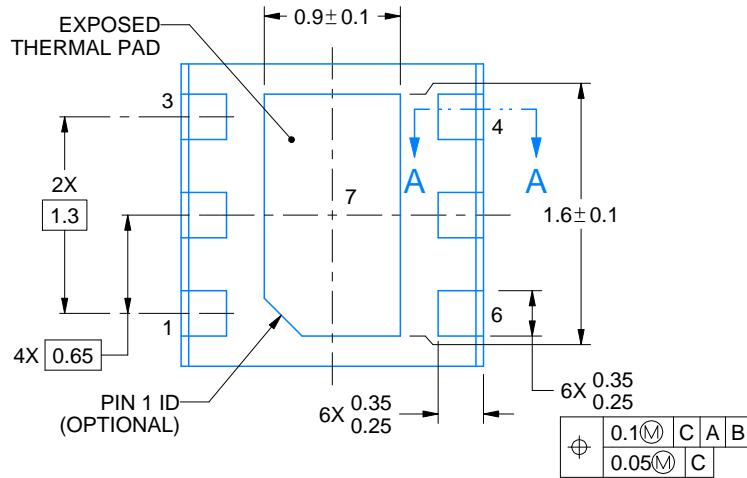
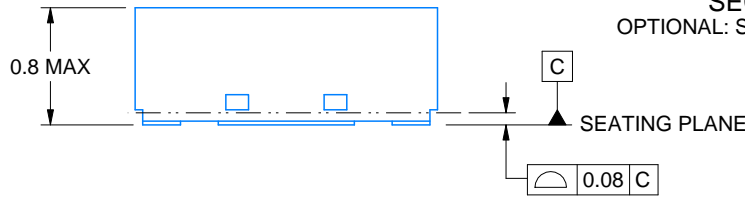
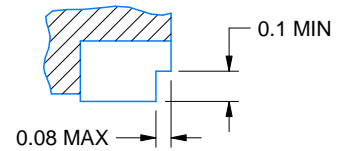
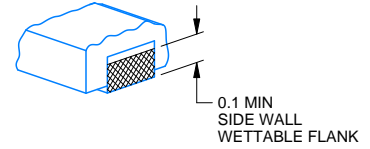
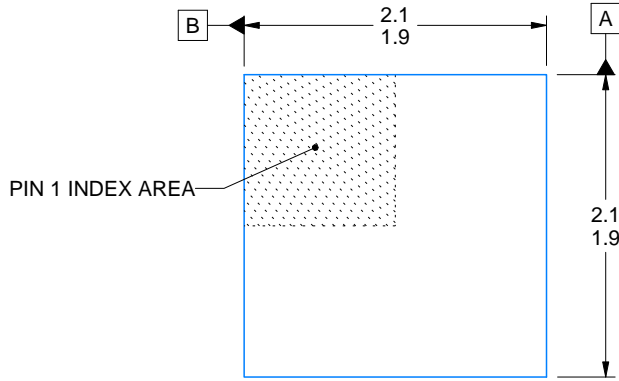
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



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NOTES:

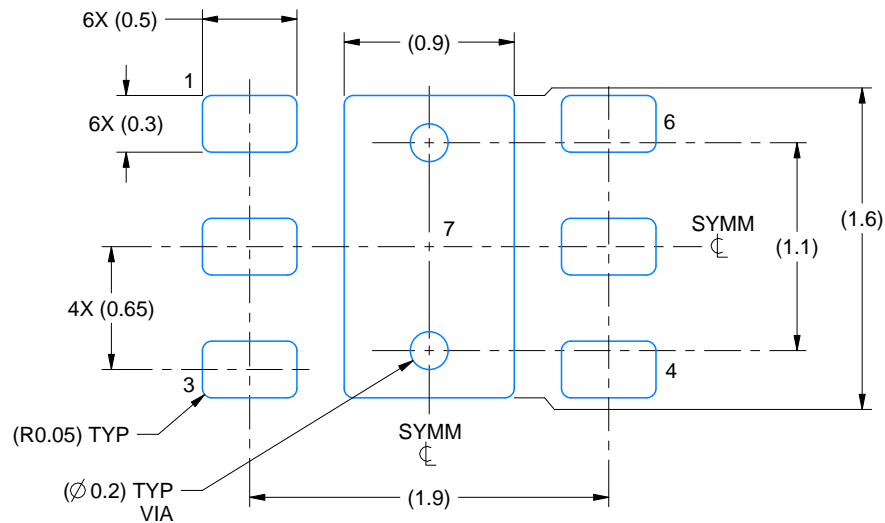
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

# EXAMPLE BOARD LAYOUT

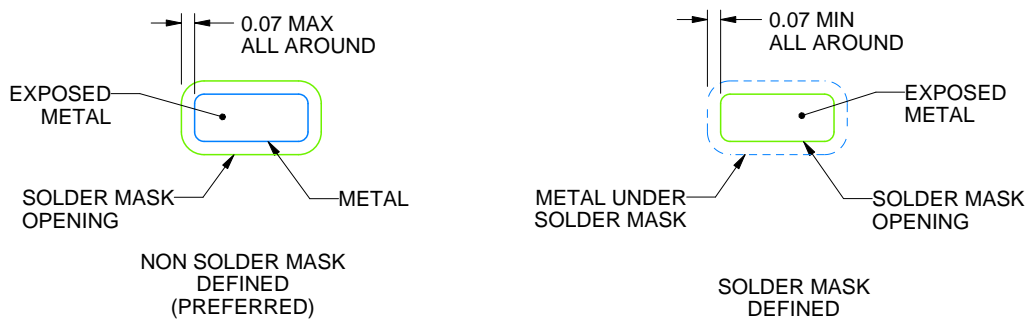
DRV0006C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:25X



**SOLDER MASK DETAILS**

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NOTES: (continued)

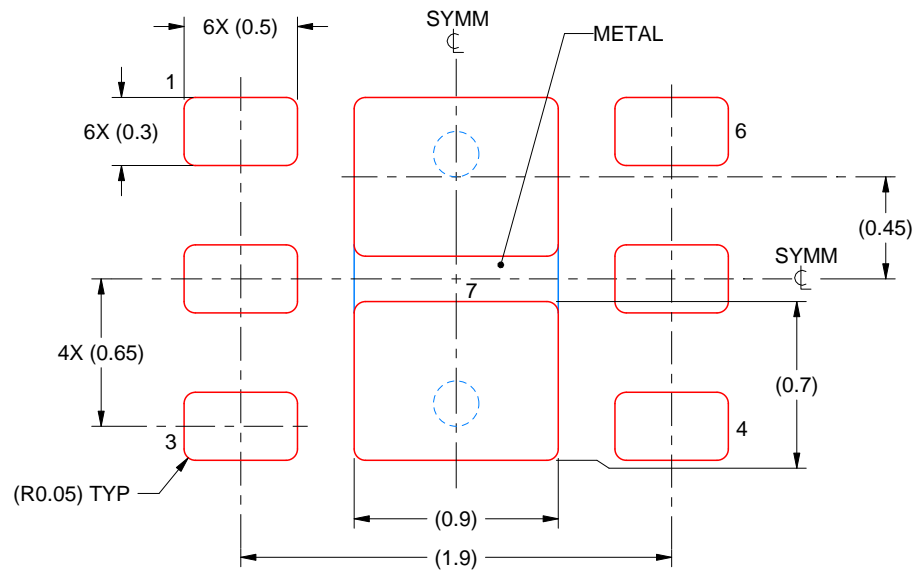
4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRV0006C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7:  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

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NOTES: (continued)

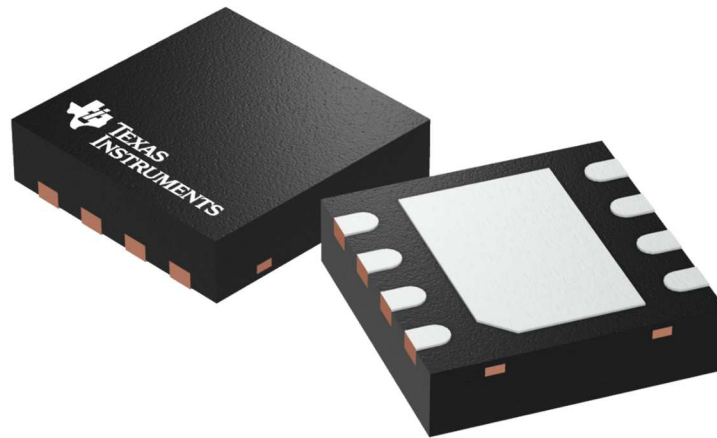
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**DRB 8**

**GENERIC PACKAGE VIEW**

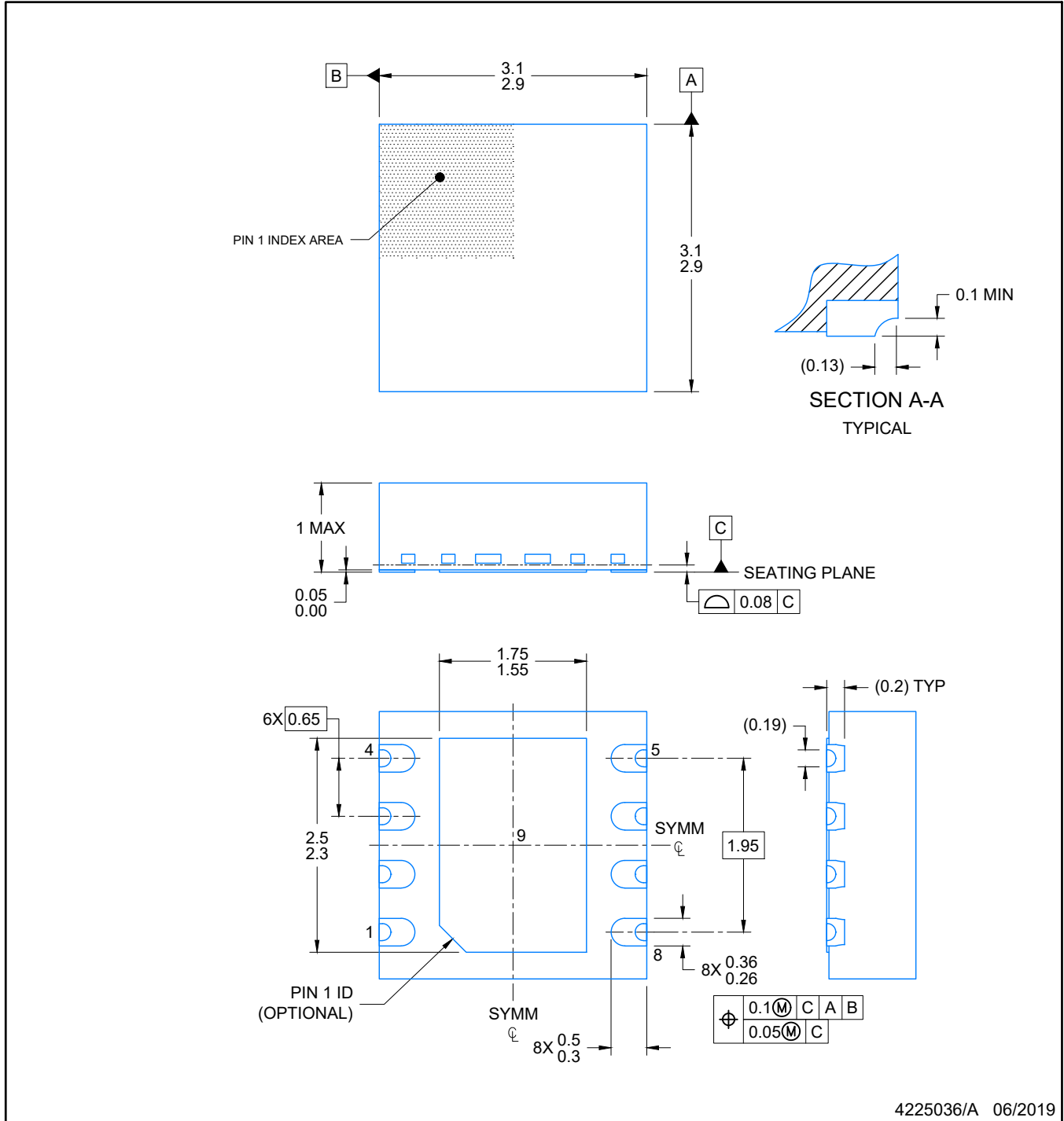
**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

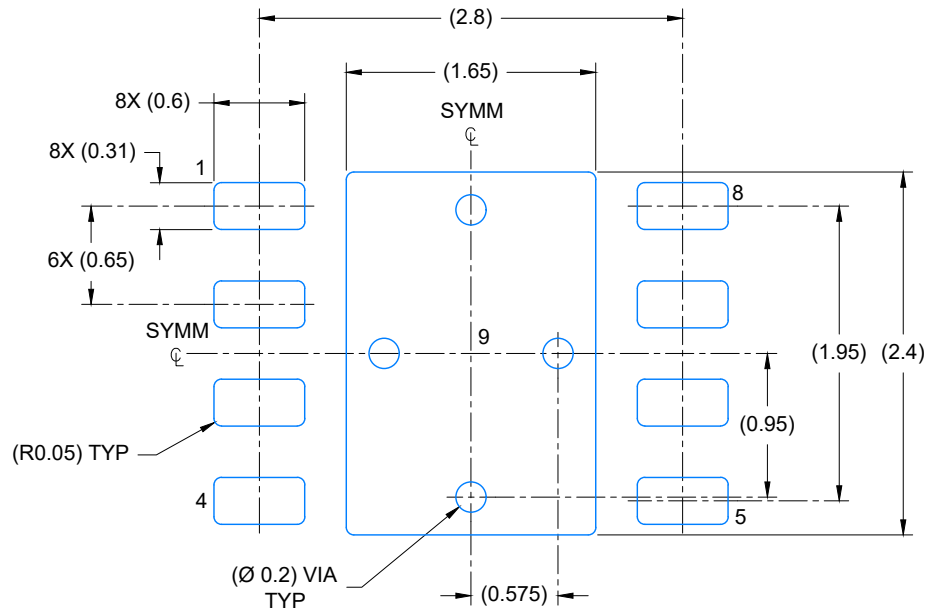
4203482/L



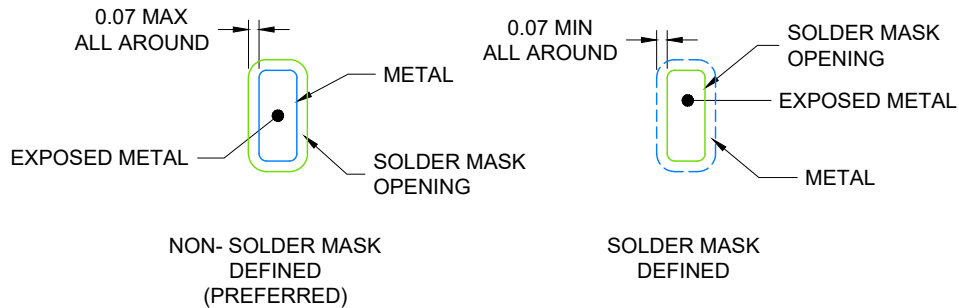
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

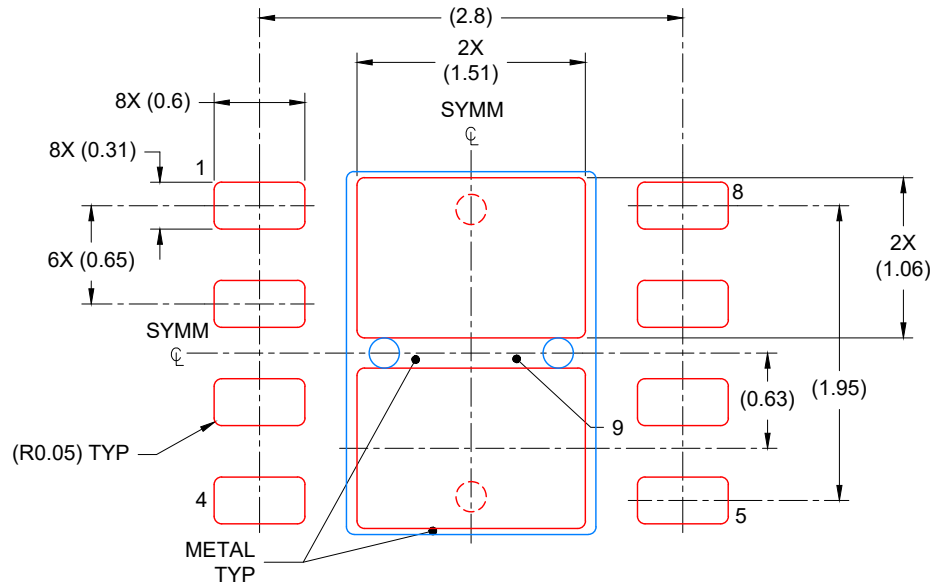


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 81% PRINTED COVERAGE BY AREA  
 SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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