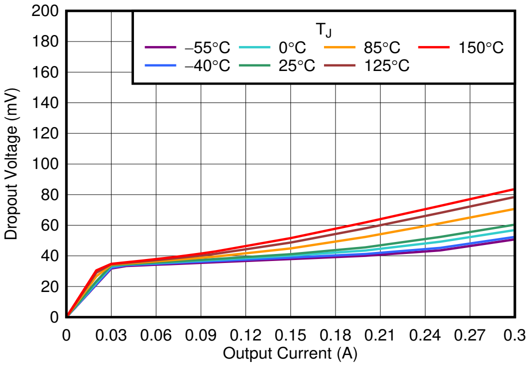
TPS784-Q1 車載用、300mA、高 PSRR、高精度、低ドロップアウト電圧レギュレータ、イネーブル付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1:–40℃～+125℃、T_A
- デバイスの接合部温度:–40℃～+150℃、T_J
- 入力電圧範囲:1.65V～6.0V
- 利用可能な出力電圧:
  - 可変オプション:1.2V～5.5V
  - 固定オプション:0.65V～5.0V
- 出力精度:標準値 0.5%、最大値 1.7%
- 50dB の PSRR (100kHz 時)
- 低 I_Q:25μA (標準値):
- 非常に低いドロップアウト:
  - 3.3V_{OUT}、300mA 時に 115mV (最大値)
- 500μs の内部ソフトスタートにより突入電流を低減
- アクティブ出力放電
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- パッケージ
  - 3mm × 3mm のウェッタブル・フランク VSON (8)
  - 5 ピン SOT-23

2 アプリケーション

- 車載ヘッド・ユニット
- ハイブリッド・インストルメント・クラスタ
- テレマティクス制御ユニット
- DC/DC コンバータ



5.0V でのドロップアウトと I_{OUT} との関係

3 概要

TPS784-Q1 超低ドロップアウト・レギュレータ (LDO) は、非常に優れたラインおよび負荷過渡性能で 300mA を供給できる小型低静止電流 LDO です。

出力ノイズが小さく PSRR 特性が優れているため、このデバイスは電力の制約が厳しいアナログ負荷に適しています。TPS784-Q1 は 1.65V～6.0V の入力電圧範囲に対応しており、出力を 1.2V～5.5V の範囲で調整できるため、ポスト・レギュレーション用デバイスとして柔軟に使用できます。本デバイスは、一般的な電圧レールに給電するための 0.65V～5.0V の固定出力電圧にも対応しています。

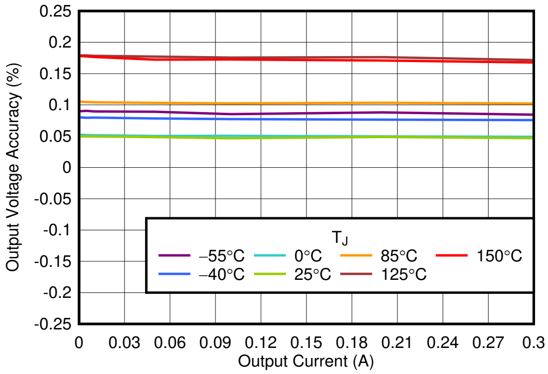
TPS784-Q1 は、過電流条件の際に消費電力を低減するため、フォールドバック電流制限機能を備えています。EN 入力は、システムの電源シーケンス要件を満たすのに役立ちます。内部ソフトスタートにより制御された起動を実現できるため、突入電流が少なくなり、小さい容量の入力コンデンサを使用できます。

TPS784-Q1 は、ディセーブル時に出力負荷を迅速に放電するためのアクティブ・プルダウン回路を備えています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS784-Q1	ウェッタブル・フランク VSON (8)	3.00mm × 3.00mm
	SOT-23 (5)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



5.0V での出力精度と I_{OUT} との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from May 16, 2021 to January 11, 2022 (from Revision B (April 2021) to Revision C (January 2022))

Page

- VSON パッケージをプレビューから量産データに変更........ 1
- Added B version DRB package (VSON) to the *Pin Configuration and Functions* section........ 3
- Changed *Device Nomenclature* table........ 39

Changes from Revision A (November 2020) to Revision B (April 2021)

Page

- Reworded the VIN conditions to have more clarity on what 1.65 V or whichever is greater applies to........ 7
- Added line item for 1.2 V ≤ V_{OUT} < 1.5 V dropout voltage in the DRB package. 7

5 Pin Configuration and Functions

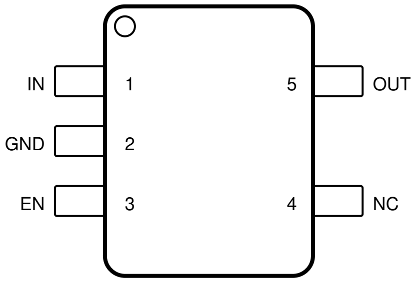

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図 5-1. DBV Package (Fixed), 5-Pin SOT-23, Top View

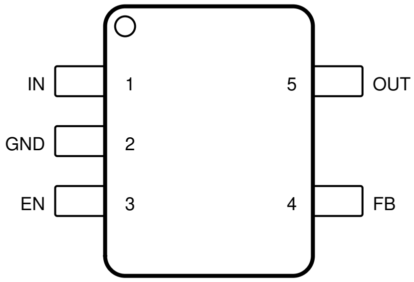

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図 5-2. DBV Package (Adjustable), 5-Pin SOT-23, Top View

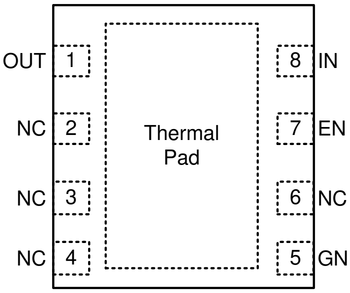

図 5-3. DRB Package (Fixed), 8-Pin VSON, Top View

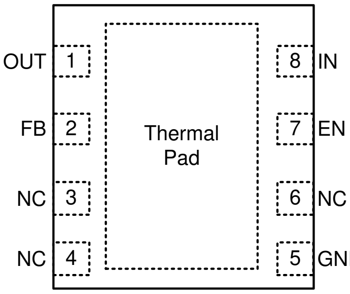

図 5-4. DRB Package (Adjustable), 8-Pin VSON, Top View

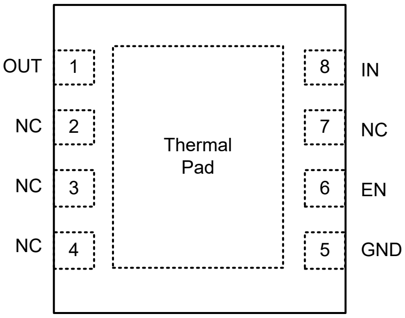

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図 5-5. DRB Package (Fixed) B Version, 8-Pin VSON, Top View

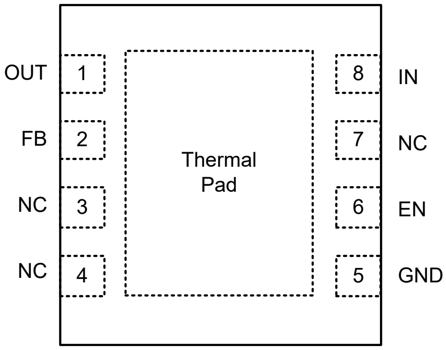

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図 5-6. DRB Package (Adjustable) B Version, 8-Pin VSON, Top View

表 5-1. Pin Functions

PIN							I/O	DESCRIPTION
NAME	DBV (Adjustable)	DBV (Fixed)	DRB (Adjustable)	DRB (Fixed)	DRB (Adjustable) B Version	DRB (Fixed) B Version		
EN	3	3	7	7	6	6	Input	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. Do not float this pin. If not used, connect EN to IN.
FB	4	—	2	—	2	—	Input	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. Do not float this pin. For adjustable-voltage version devices only.
GND	2	2	5	5	5	5	—	Ground pin. This pin must be connected to ground on the board.
IN	1	1	8	8	8	8	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible.
NC	—	4	3, 4, 6	2, 3, 4, 6	3, 4, 7	2, 3, 4, 7	—	No connect pin. This pin is not internally connected. Connect to ground for best thermal performance or leave floating.
OUT	5	5	1	1	1	1	Output	A 0.47-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table.
Thermal Pad	N/A	N/A	Pad	Pad	Pad	Pad	—	The thermal pad is electrically connected to the GND pin. Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	6.5	V
	Enable, V_{EN}	–0.3	6.5	V
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	V
	Feedback, V_{FB}	–0.3	2	V
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		1.65		6.0	V
V_{OUT}	Output voltage	Adjustable output	1.2		5.5	V
		Fixed output	0.65		5.0	
C_{IN}	Input capacitor		0.1	1		µF
C_{OUT}	Output capacitor		1(1)		200	µF
C_{FF}	Feed-forward capacitor(2)		0	10	100	nF
I_{OUT}	Output current		0		300	mA
$C_{OUT,ESR}$	Output capacitor ESR		0.001		1	Ω
V_{EN}	Enable voltage		0		6	V
F_{EN}	Enable toggle frequency				10	kHz
T_J	Junction temperature		–40		150	°C

(1) The minimum effective capacitance is 0.47 µF.
(2) Feed-forward capacitor is optional and not required for stability.

6.4 Thermal Information

THERMAL METRIC(1)		TPS784-Q1		UNIT
		DRB (VSON)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.8(2)	170.8(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.1	93.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	10.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.2	17.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.1	40	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.1	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The 1s0p $R_{\theta JA}$ value (based on JEDEC 51-3) is 226.5 ℃/W for the DRB package.
(3) The 1s0p $R_{\theta JA}$ value (based on JEDEC 51-3) is 277.3 ℃/W for the DBV package.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +150°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.65		6.0	V
V_{OUT}	Output voltage	Adjustable output		1.2		5.5	V
		Fixed output		0.65		5.0	
V_{OUT}	Output accuracy(1)	1 mA ≤ I_{OUT} ≤ 300 mA, $V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater) ≤ V_{IN} ≤ 6.0 V	T_J = 25°C	–0.5		0.5	%
			–40°C ≤ T_J ≤ 85°C	–1		1	
			–40°C ≤ T_J ≤ 150°C	–1.7		1.7	
V_{OUT}	Line regulation	$V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater) ≤ V_{IN} ≤ 6.0 V			0.3		mV
V_{OUT}	Load regulation	0.1 mA ≤ I_{OUT} ≤ 300 mA	–40°C ≤ T_J ≤ 85°C	–5		5	mV
			–40°C ≤ T_J ≤ 150°C	–5		10	
ΔV_{OUT}	Load transient response settling time(2) (3)	C_{OUT} = 10 µF				10	µs
	Load transient response overshoot, undershoot (3) (5)	t_R = t_F = 1 µs, C_{OUT} = 10 µF	I_{OUT} = 90 mA to 210 mA	–2%			%V_{OUT}
			I_{OUT} = 210 mA to 90 mA			10%	
			I_{OUT} = 0 mA to 300 mA	–10%			
I_{GND}	Ground current	I_{OUT} = 0 mA $V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater) ≤ V_{IN} ≤ 6.0 V	T_J = 25°C	15	25	30	µA
			–40°C ≤ T_J ≤ 85°C			33	
			–40°C ≤ T_J ≤ 150°C			40	
		I_{OUT} = 500 µA $V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater) ≤ V_{IN} ≤ 6.0 V	T_J = 25°C		33	43	
			–40°C ≤ T_J ≤ 85°C			45	
			–40°C ≤ T_J ≤ 150°C			48	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.3 V $V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater) ≤ V_{IN} ≤ 6.0 V	T_J = 25°C		0.01	0.05	µA
			–40°C ≤ T_J ≤ 85°C			0.25	
			–40°C ≤ T_J ≤ 150°C			3	
V_{FB}	Feedback voltage	Adjustable output only		1.182	1.2	1.218	V
I_{FB}	Feedback pin current	Adjustable output only		–0.05	0.01	0.05	µA
I_{CL}	Output current limit	V_{IN} = $V_{OUT(nom)}$ + 1 V, V_{OUT} = 0.9 x $V_{OUT(nom)}$ (4)		320		420	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			162.5		mA
V_{DO}	Dropout voltage	I_{OUT} = 300 mA, V_{OUT} = 0.95 x $V_{OUT(nom)}$	0.65 V ≤ V_{OUT} < 0.8 V			900	mV
			0.8 V ≤ V_{OUT} < 1.2 V			775	
			1.2 V ≤ V_{OUT} < 1.5 V			300	
			1.5 V ≤ V_{OUT} < 1.8 V			175	
			1.8 V ≤ V_{OUT} < 2.5 V			140	
			2.5 V ≤ V_{OUT} ≤ 5.0 V			115	
			1.2 V ≤ V_{OUT} < 1.5 V, DRB Package only			320	
PSRR	Power-supply rejection ratio	I_{OUT} = 300 mA , V_{IN} = V_{OUT} + 1 V	f = 1 kHz		60		dB
			f = 100 kHz		45		
			f = 1 MHz		30		
Vn	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.2 V			30		μV_{RMS}
V_{UVLO}	UVLO threshold	V_{IN} rising		1.32	1.42	1.6	V
		V_{IN} falling		1.17	1.29	1.42	
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{IN} hysteresis			130		mV
t_{STR}	Start-up time	From EN low-to-high transition to V_{OUT} = $V_{OUT(nom)}$ x 95%		280	500	780	µs
$V_{EN(HI)}$	EN pin logic high voltage			0.85			V
$V_{EN(LOW)}$	EN pin logic low voltage					0.425	

6.5 Electrical Characteristics (continued)

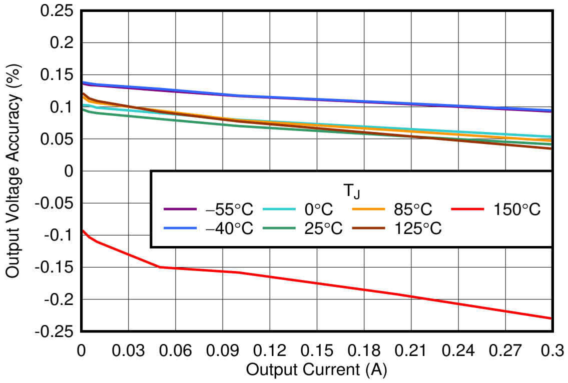
at operating temperature range (T_J = –40°C to +150°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 1.65 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 6.0 V		10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 3.3 V		120		Ω
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		155		

(1) Resistor tolerance is not included in overall accuracy in the adjustable version.
(2) The settling time is measured from when I_{OUT} is stepped from 90 mA to 210 mA to when the output voltage recovers to V_{OUT} = $V_{OUT(nom)}$ - 5 mV.
(3) This specification is verified by design.
(4) The output is being forced to 90% of the nominal V_{OUT} value.
(5) This specification is in relation to the change from the nominal output voltage ($V_{OUT(nom)}$).

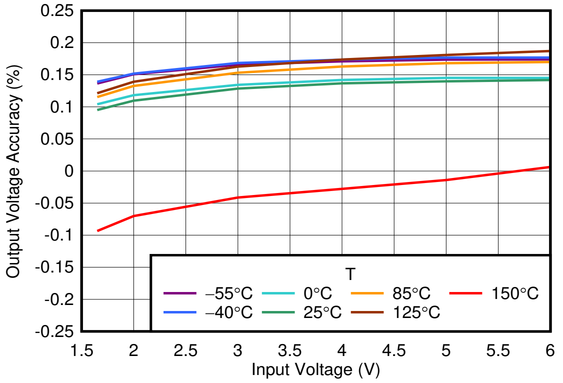
6.6 Typical Characteristics

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



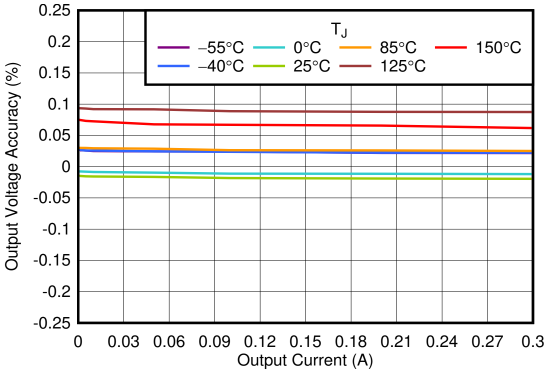
V_{OUT} = 0.65 V

図 6-1. Output Accuracy vs I_{OUT}



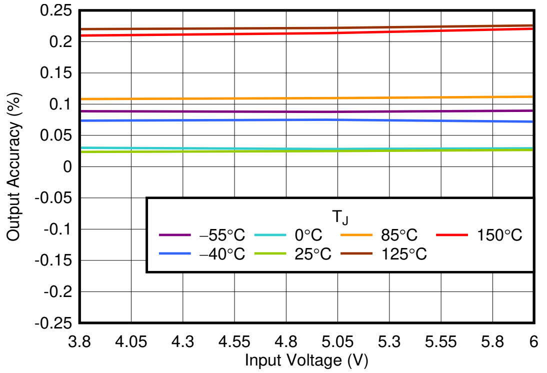
V_{OUT} = 0.65 V

図 6-2. Output Accuracy vs V_{IN}



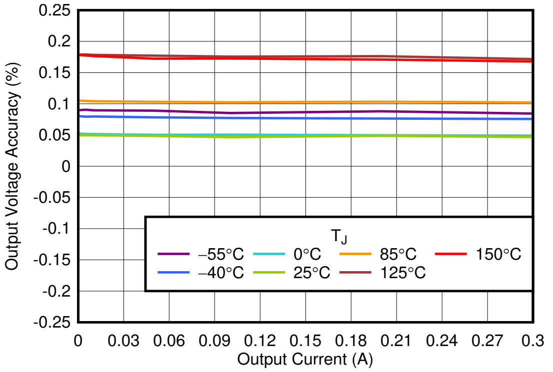
V_{OUT} = 1.2 V

図 6-3. Output Accuracy vs I_{OUT}



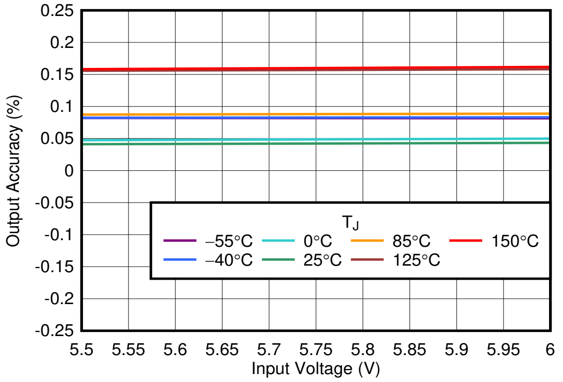
V_{OUT} = 3.3 V

図 6-4. Output Accuracy vs V_{IN}



V_{OUT} = 5.0 V

図 6-5. Output Accuracy vs I_{OUT}

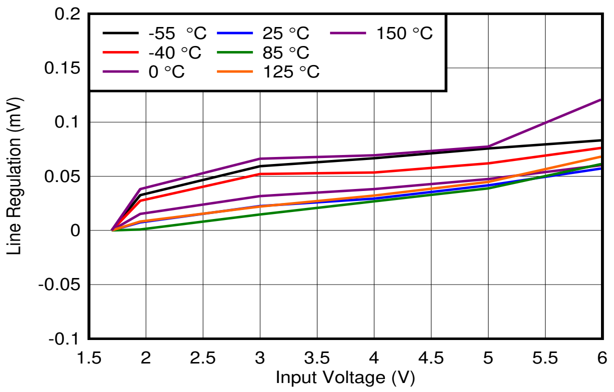


V_{OUT} = 5.0 V

図 6-6. Output Accuracy vs V_{IN}

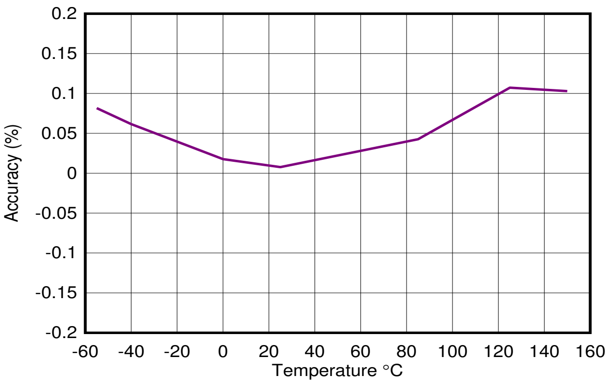
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



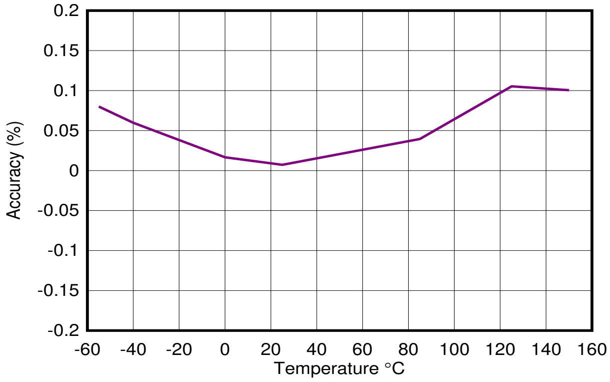
V_{OUT} = 1.2 V, I_{OUT} = 50 mA

図 6-7. 50-mA Line Regulation



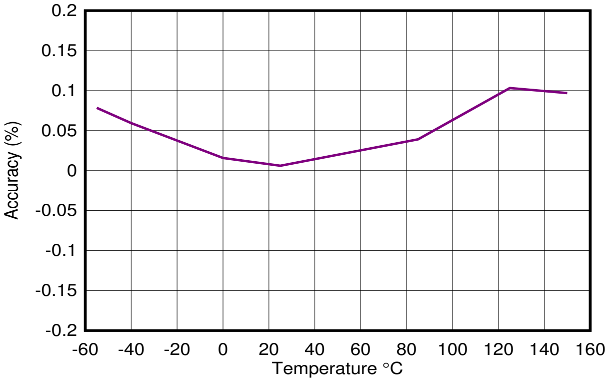
V_{OUT} = 1.2 V, I_{OUT} = 50 mA

図 6-8. Accuracy vs Temperature



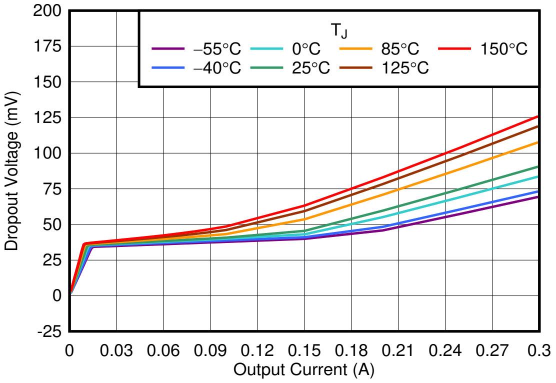
V_{OUT} = 1.2 V, I_{OUT} = 100 mA

図 6-9. Accuracy vs Temperature



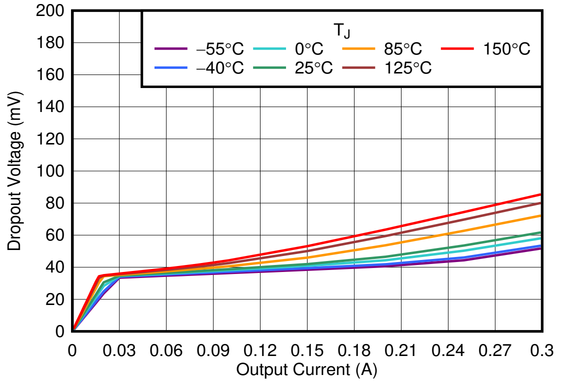
V_{OUT} = 1.2 V, I_{OUT} = 300 mA

図 6-10. Accuracy vs Temperature



V_{OUT} = 1.8 V

図 6-11. Dropout Voltage vs I_{OUT}

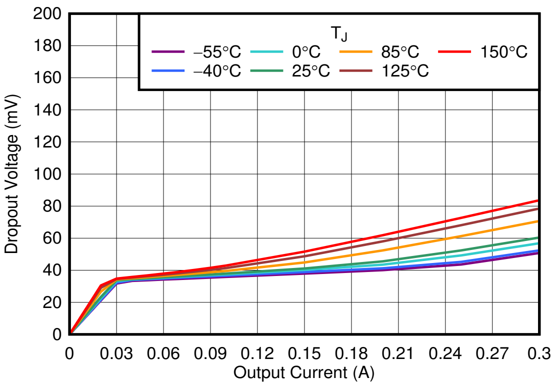


V_{OUT} = 3.3 V

図 6-12. Dropout Voltage vs I_{OUT}

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



V_{OUT} = 5.0 V

図 6-13. Dropout Voltage vs I_{OUT}

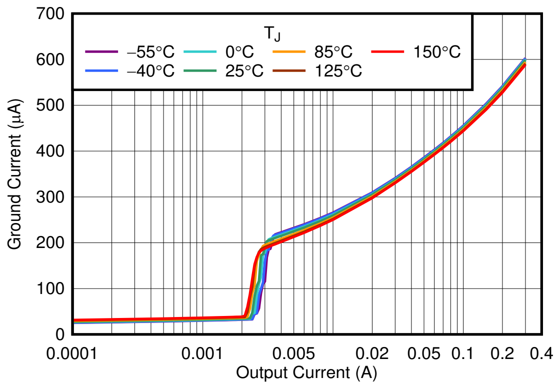
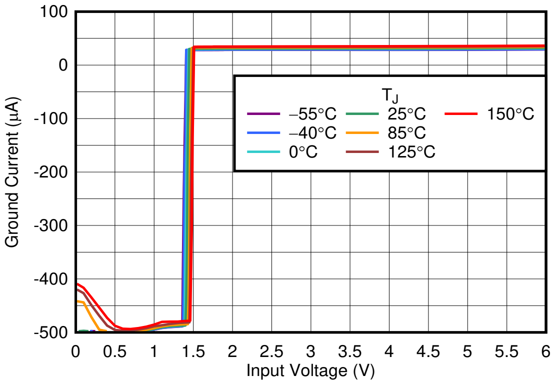
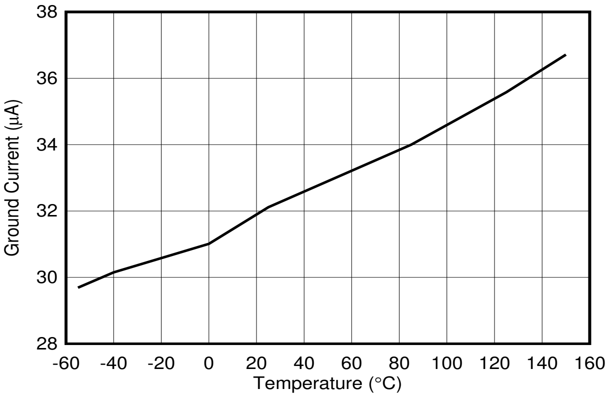


図 6-14. I_{GND} vs I_{OUT}



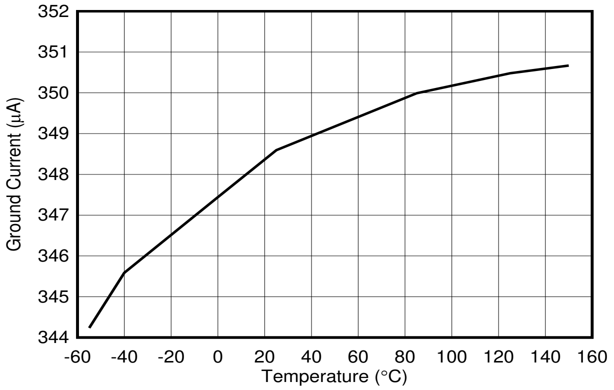
I_{OUT} = 500 µA

図 6-15. I_{GND} vs V_{IN}



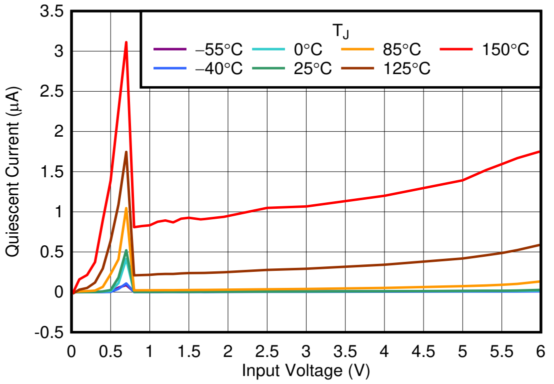
I_{OUT} = 500 µA

図 6-16. 500-µA Ground Current vs Temperature



I_{OUT} = 50 mA

図 6-17. 50-mA Ground Current vs Temperature

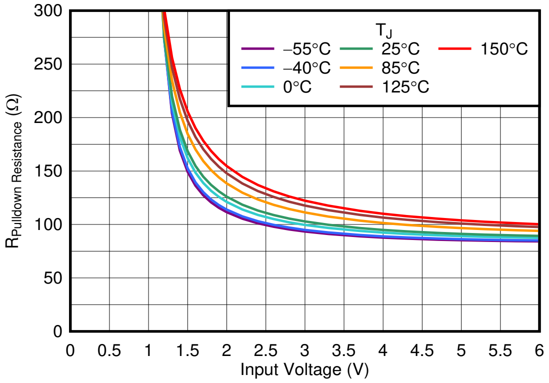


V_{EN} = 0.3 V

図 6-18. I_{SHDN} vs V_{IN}

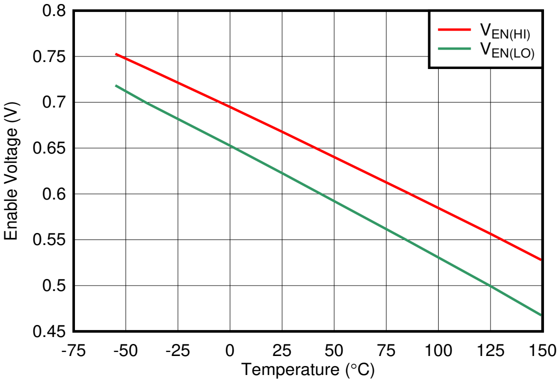
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



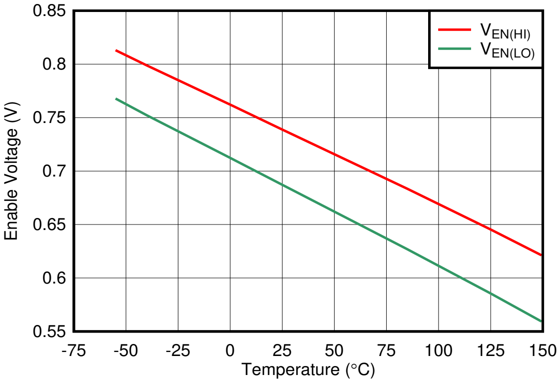
V_{EN} = 0.3 V

図 6-19. Pulldown Resistor ($R_{Pulldown}$) vs V_{IN}



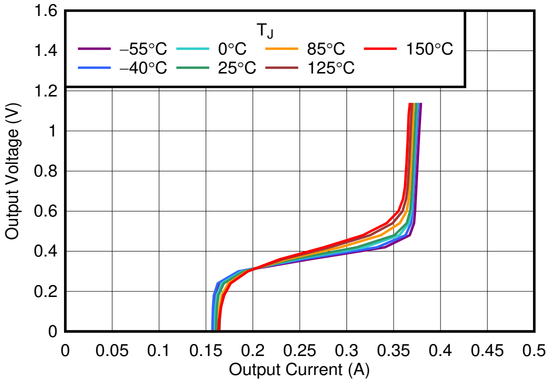
V_{IN} = 2 V

図 6-20. $V_{EN(HI)}$ and $V_{EN(LOW)}$ Thresholds vs Temperature



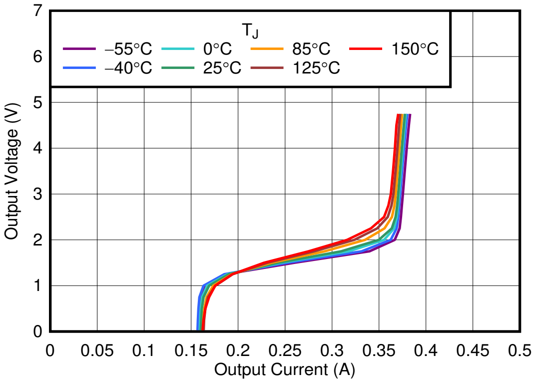
V_{IN} = 6 V

図 6-21. $V_{EN(HI)}$ and $V_{EN(LOW)}$ Thresholds vs Temperature



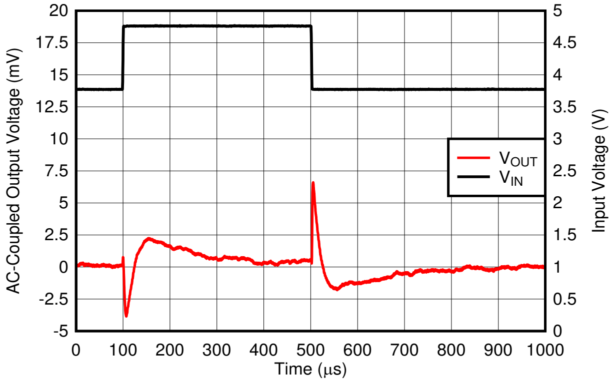
V_{OUT} = 1.2 V

図 6-22. Foldback Current Limit vs I_{OUT} and Temperature



V_{OUT} = 5.0 V

図 6-23. Foldback Current Limit vs I_{OUT} and Temperature

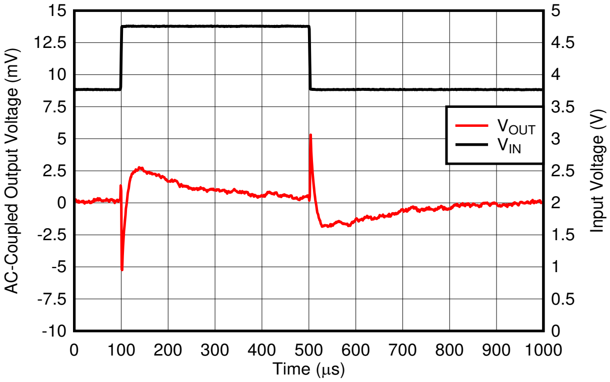


V_{OUT} = 3.3 V, I_{OUT} = 1 mA, slew rate = 1 V/µs

図 6-24. Line Transient

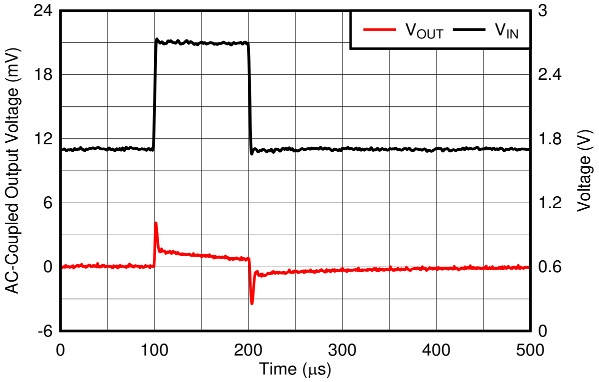
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



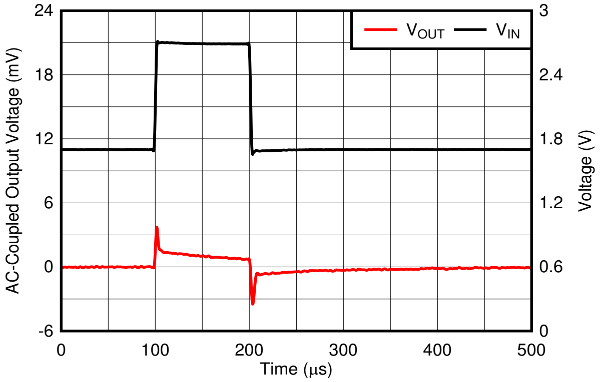
V_{OUT} = 3.3 V, I_{OUT} = 300 mA, slew rate = 1 V/µs

図 6-25. Line Transient



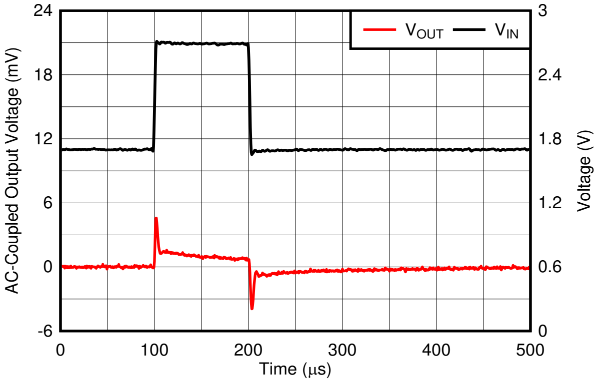
V_{OUT} = 1.2 V, I_{OUT} = 50 mA, slew rate = 1 V/µs, T_J = 25°C

図 6-26. Line Transient



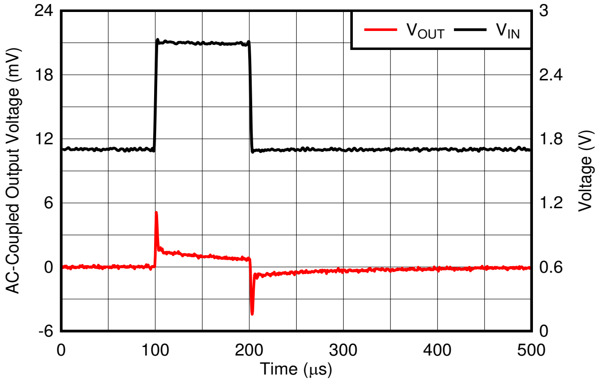
V_{OUT} = 1.2 V, I_{OUT} = 50 mA, slew rate = 1 V/µs, T_J = -40℃

図 6-27. Line Transient



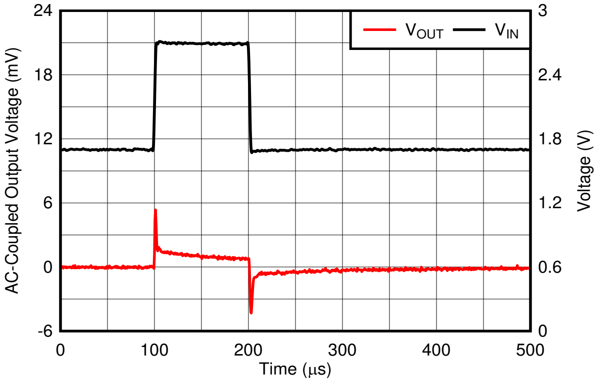
V_{OUT} = 1.2 V, I_{OUT} = 50 mA, slew rate = 1 V/µs, T_J = 150℃

図 6-28. Line Transient



V_{OUT} = 1.2 V, I_{OUT} = 100 mA, slew rate = 1 V/µs, T_J = 25℃

図 6-29. Line Transient

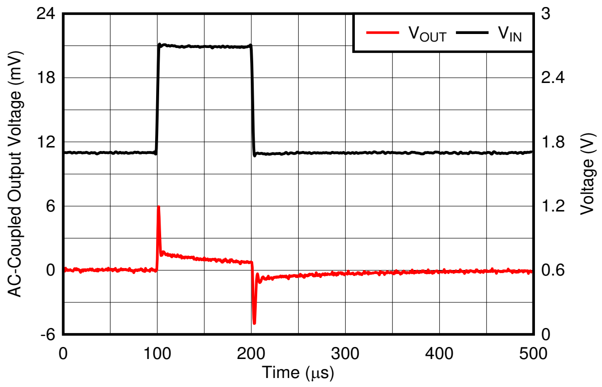


V_{OUT} = 1.2 V, I_{OUT} = 100 mA, slew rate = 1 V/µs, T_J = -40℃

図 6-30. Line Transient

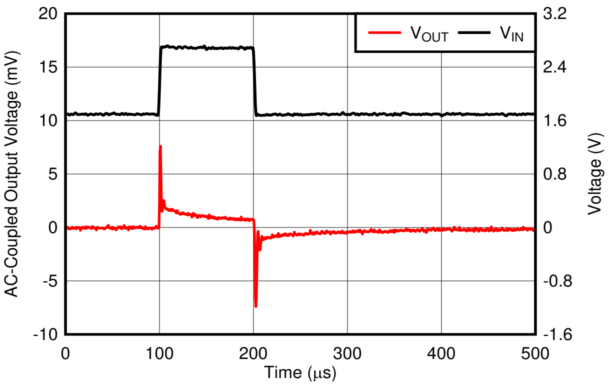
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



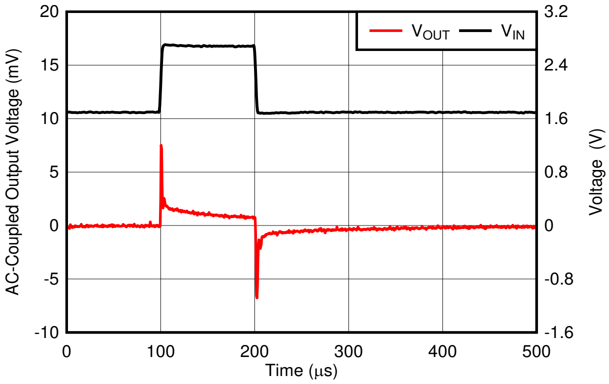
V_{OUT} = 1.2 V, I_{OUT} = 100 mA, slew rate = 1 V/µs, T_J = 150℃

図 6-31. Line Transient



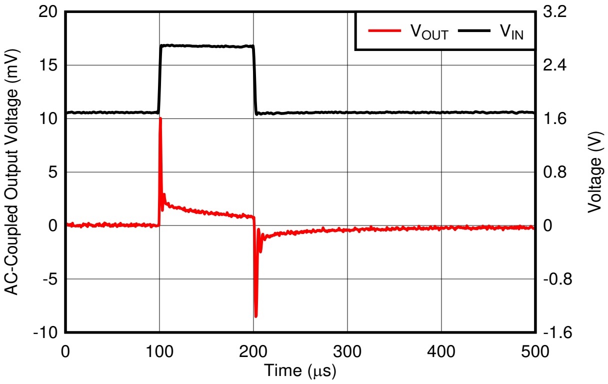
V_{OUT} = 1.2 V, I_{OUT} = 300 mA, slew rate = 1 V/µs, T_J = 25℃

図 6-32. Line Transient



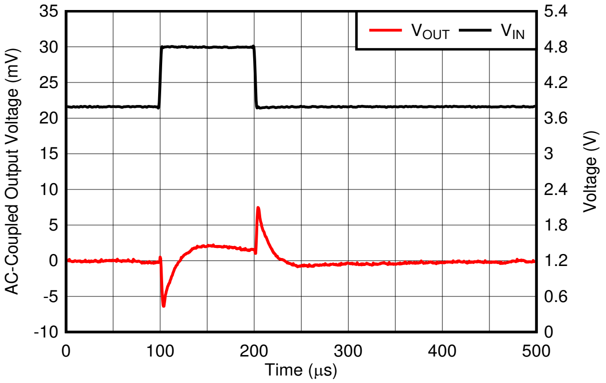
V_{OUT} = 1.2 V, I_{OUT} = 300 mA, slew rate = 1 V/µs, T_J = -40℃

図 6-33. Line Transient



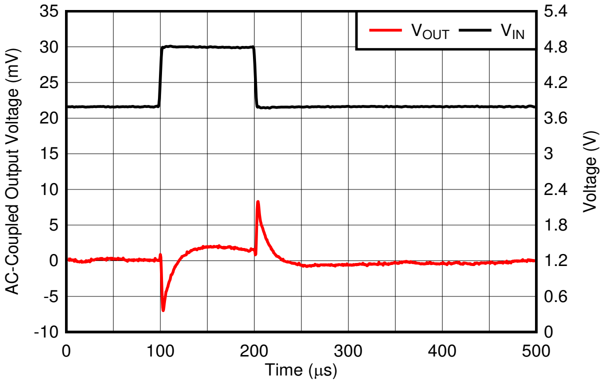
V_{OUT} = 1.2 V, I_{OUT} = 300 mA, slew rate = 1 V/µs, T_J = 150℃

図 6-34. Line Transient



V_{OUT} = 3.3 V, I_{OUT} = 50 mA, slew rate = 1 V/µs, T_J = 25℃

図 6-35. Line Transient

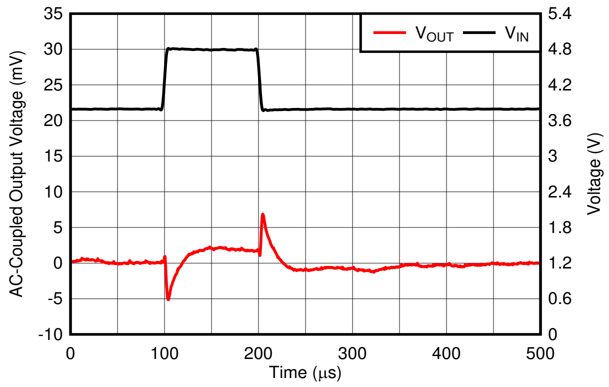


V_{OUT} = 3.3 V, I_{OUT} = 50 mA, slew rate = 1 V/µs, T_J = -40℃

図 6-36. Line Transient

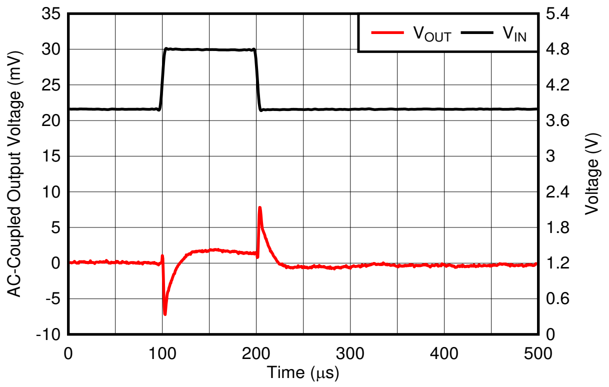
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



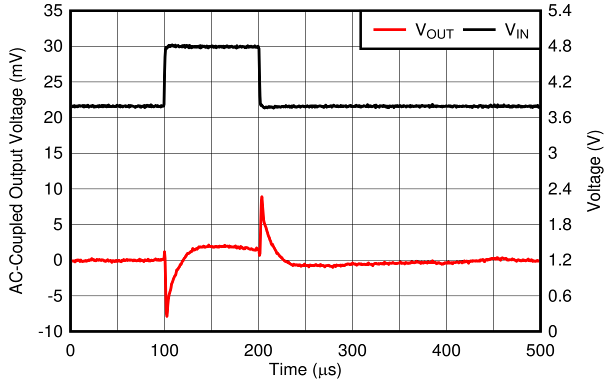
V_{OUT} = 3.3 V, I_{OUT} = 50 mA, slew rate = 1 V/µs, T_J = 150℃

図 6-37. Line Transient



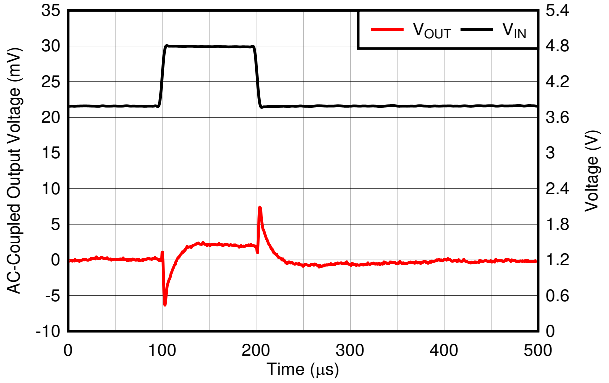
V_{OUT} = 3.3 V, I_{OUT} = 100 mA, slew rate = 1 V/µs, T_J = 25℃

図 6-38. Line Transient



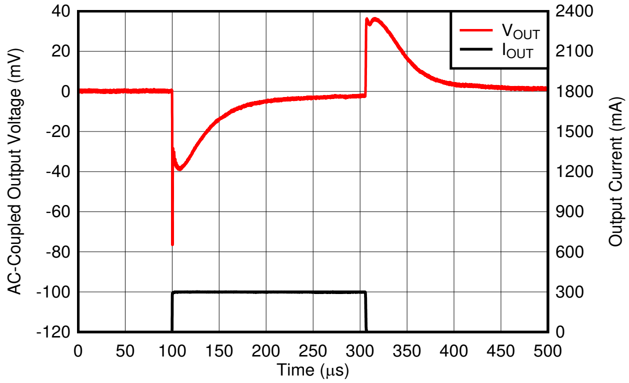
V_{OUT} = 3.3 V, I_{OUT} = 100 mA, slew rate = 1 V/µs, T_J = -40℃

図 6-39. Line Transient



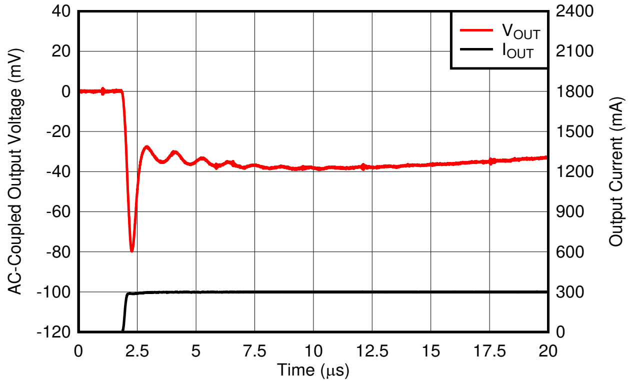
V_{OUT} = 3.3 V, I_{OUT} = 100 mA, slew rate = 1 V/µs, T_J = 150℃

図 6-40. Line Transient



V_{IN} = 5.5 V, V_{OUT} = 5.0 V, I_{OUT} slew rate = 1 A/µs

図 6-41. I_{OUT} Transient From 1 mA to 300 mA

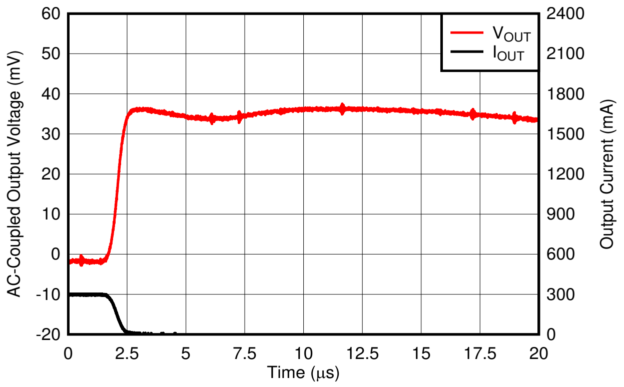


V_{IN} = 5.5 V, V_{OUT} = 5.0 V, I_{OUT} slew rate = 1 A/µs

図 6-42. I_{OUT} Transient From 1 mA to 300 mA

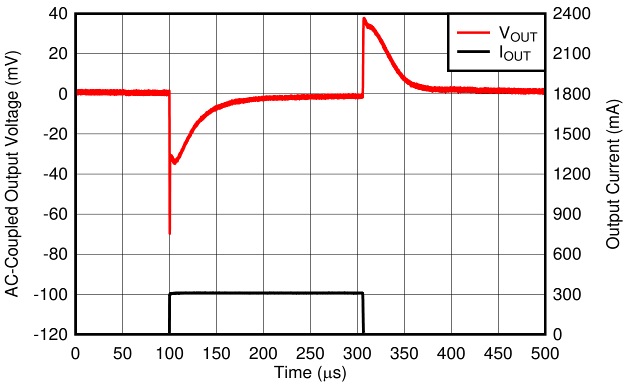
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



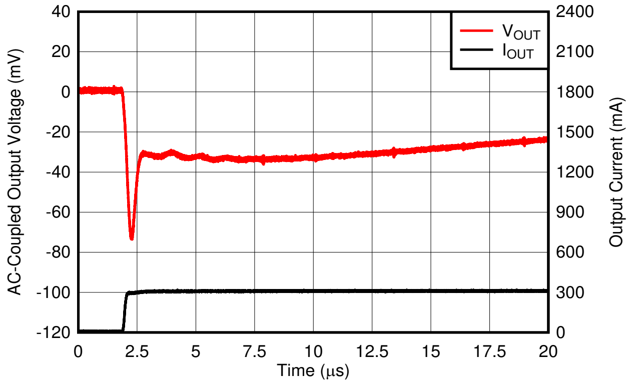
V_{IN} = 5.5 V, V_{OUT} = 5.0 V, I_{OUT} slew rate = 1 A/µs

図 6-43. I_{OUT} Transient From 300 mA to 1 mA



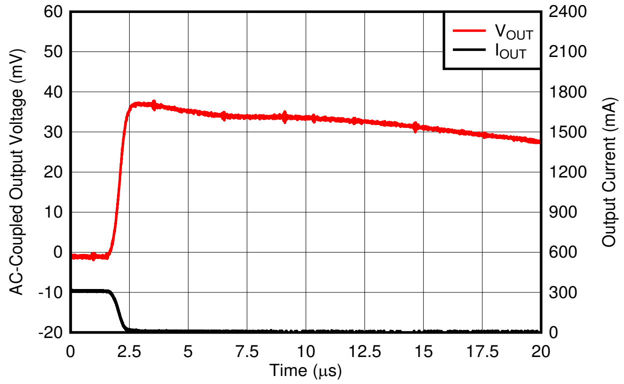
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} slew rate = 1 A/µs

図 6-44. I_{OUT} Transient From 1 mA to 300 mA



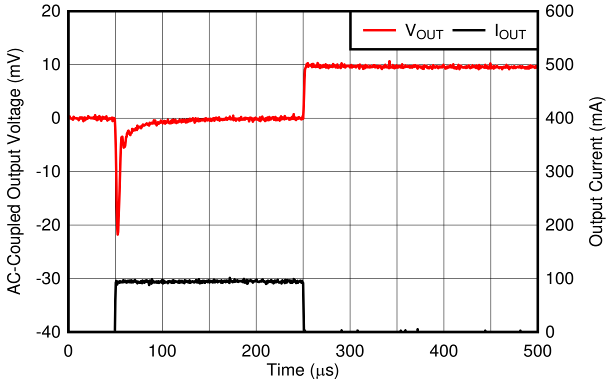
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} slew rate = 1 A/µs

図 6-45. I_{OUT} Transient From 1-mA to 300-mA Rising Edge



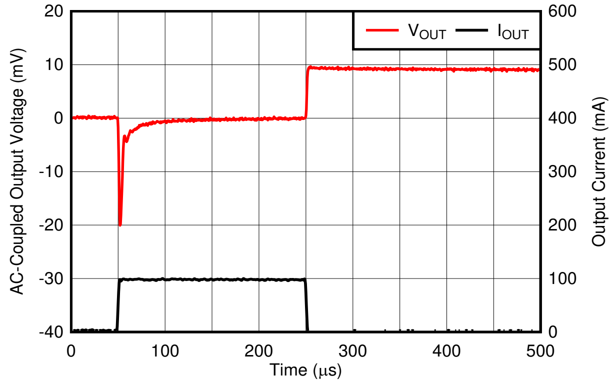
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} slew rate = 0.5 A/µs

図 6-46. I_{OUT} Transient From 1-mA to 300-mA Falling Edge



V_{OUT} = 1.2 V, I_{OUT} = 0 mA to 100 mA , I_{OUT} slew rate = 1 A/µs,
T_J = 25℃

図 6-47. Load Transient

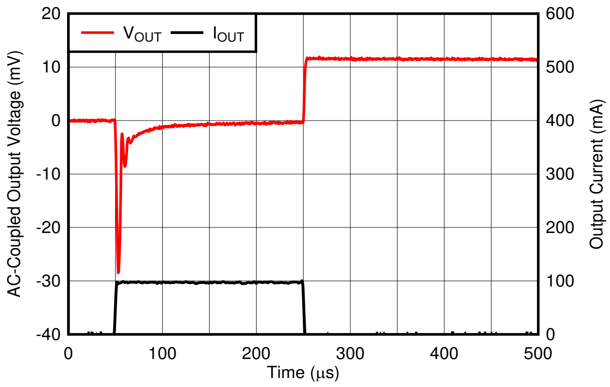


V_{OUT} = 1.2 V, I_{OUT} = 0 mA to 100 mA , I_{OUT} slew rate = 1 A/µs,
T_J = -40℃

図 6-48. Load Transient

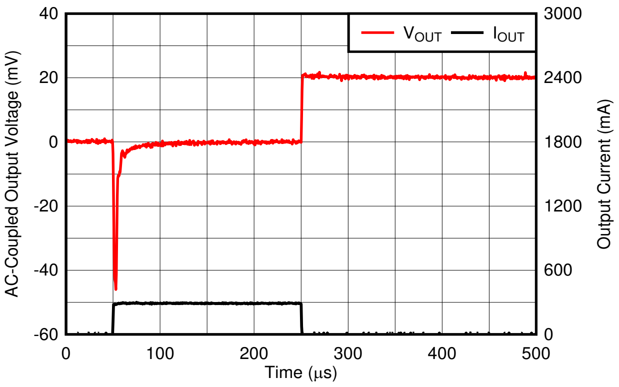
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



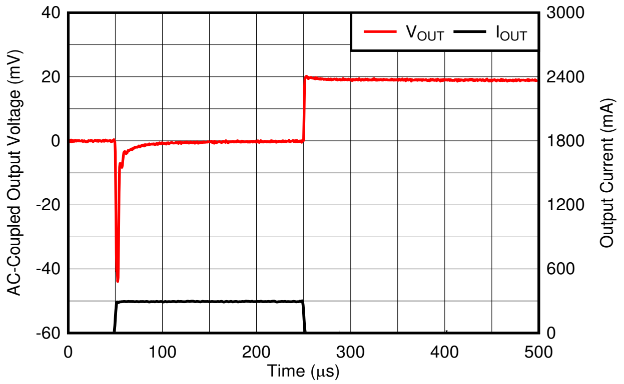
V_{OUT} = 1.2 V, I_{OUT} = 0 mA to 100 mA , I_{OUT} slew rate = 1 A/µs, T_J = 150°C

図 6-49. Load Transient



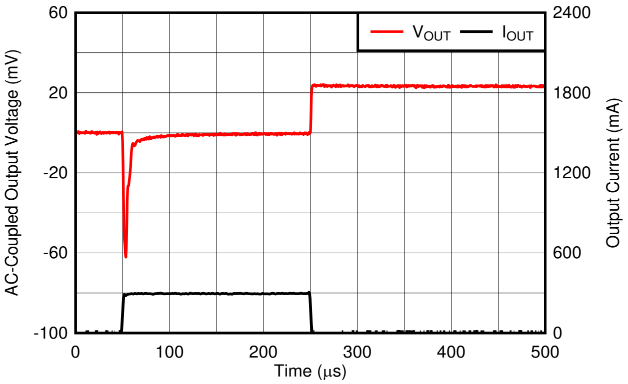
V_{OUT} = 1.2 V, I_{OUT} = 0 mA to 300 mA , I_{OUT} slew rate = 1 A/µs, T_J = 25°C

図 6-50. Load Transient



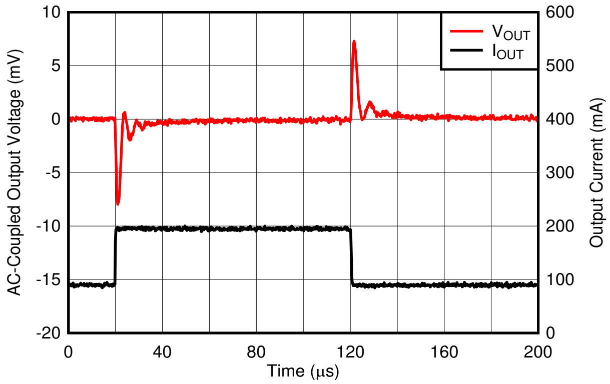
V_{OUT} = 1.2 V, I_{OUT} = 0 mA to 300 mA , I_{OUT} slew rate = 1 A/µs, T_J = -40°C

図 6-51. Load Transient



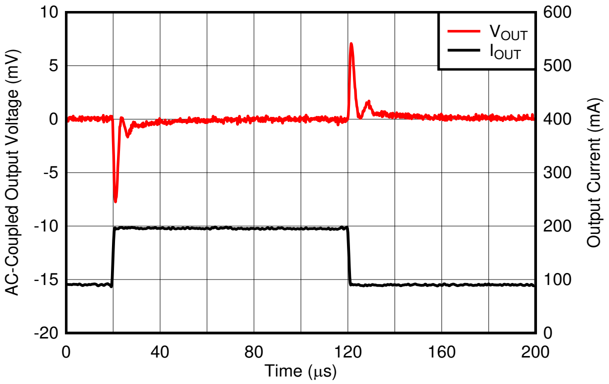
V_{OUT} = 1.2 V, I_{OUT} = 0 mA to 300 mA , I_{OUT} slew rate = 1 A/µs, T_J = 150°C

図 6-52. Load Transient



V_{OUT} = 1.2 V, I_{OUT} = 90 mA to 200 mA, I_{OUT} slew rate = 1 A/µs, T_J = 25°C

図 6-53. Load Transient

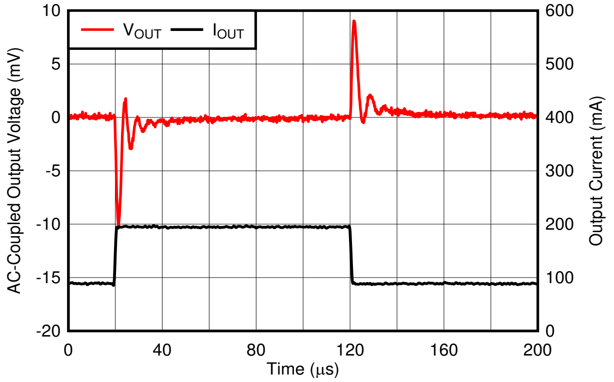


V_{OUT} = 1.2 V, I_{OUT} = 90 mA to 200 mA, I_{OUT} slew rate = 1 A/µs, T_J = -40°C

図 6-54. Load Transient

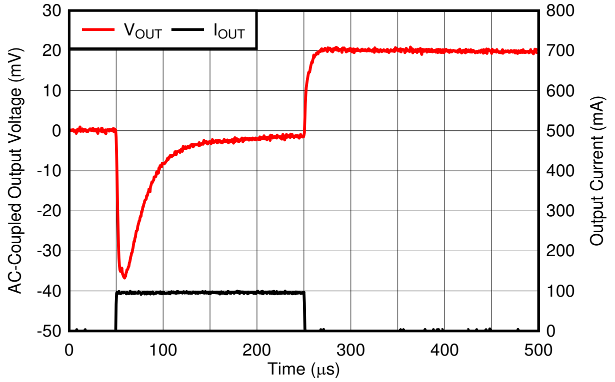
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



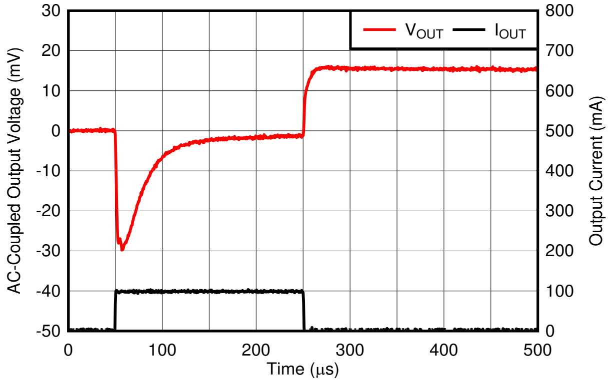
V_{OUT} = 1.2 V, I_{OUT} = 90 mA to 200 mA, I_{OUT} slew rate = 1 A/µs, T_J = 150℃

図 6-55. Load Transient



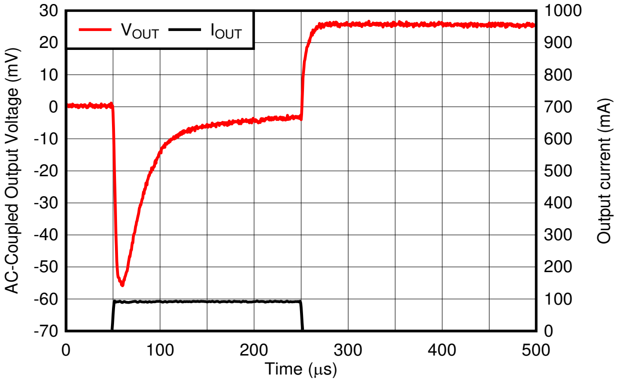
V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 100 mA, I_{OUT} slew rate = 1 A/µs, T_J = 25℃

図 6-56. Load Transient



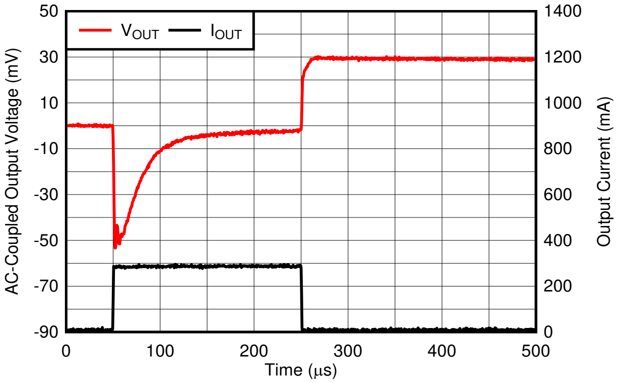
V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 100 mA, I_{OUT} slew rate = 1 A/µs, T_J = -40℃

図 6-57. Load Transient



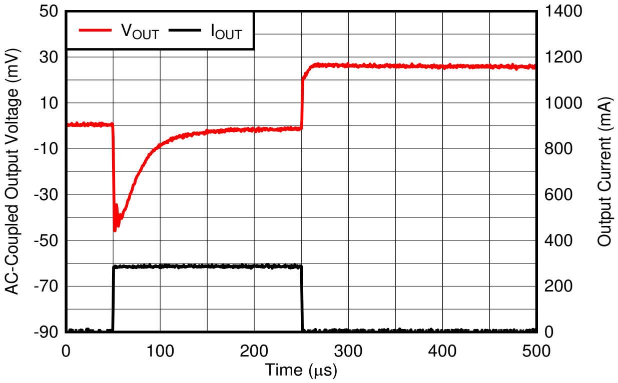
V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 100 mA, I_{OUT} slew rate = 1 A/µs, T_J = 150℃

図 6-58. Load Transient



V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 300 mA, I_{OUT} slew rate = 1 A/µs, T_J = 25℃

図 6-59. Load Transient

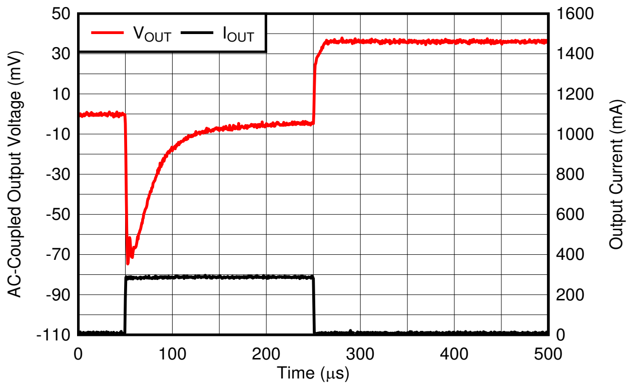


V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 300 mA, I_{OUT} slew rate = 1 A/µs, T_J = -40℃

図 6-60. Load Transient

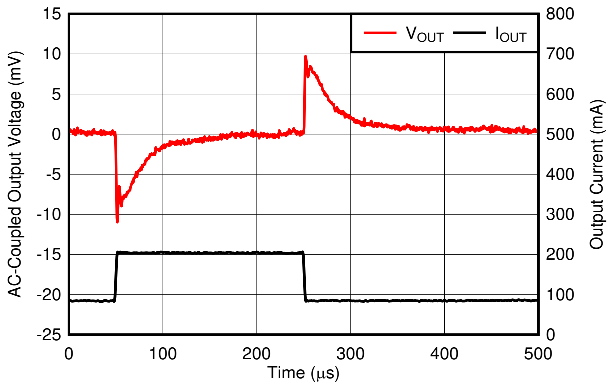
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



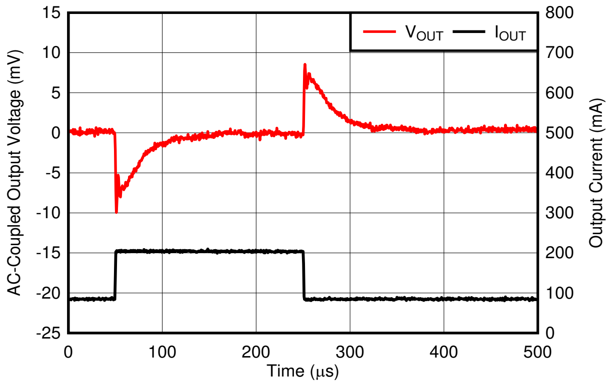
V_{OUT} = 3.3 V, I_{OUT} = 0 mA to 300 mA, I_{OUT} slew rate = 1 A/µs, T_J = 150℃

図 6-61. Load Transient



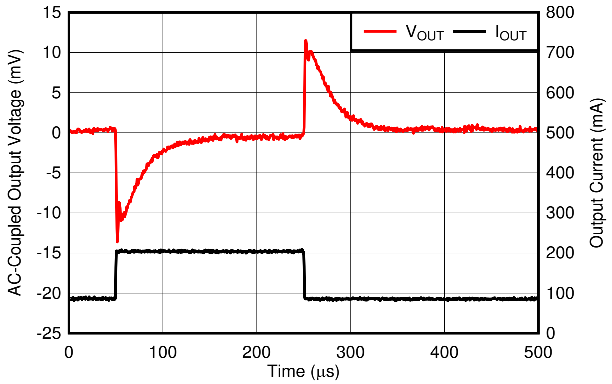
V_{OUT} = 3.3 V, I_{OUT} = 90 mA to 200 mA, I_{OUT} slew rate = 1 A/µs, T_J = 25℃

図 6-62. Load Transient



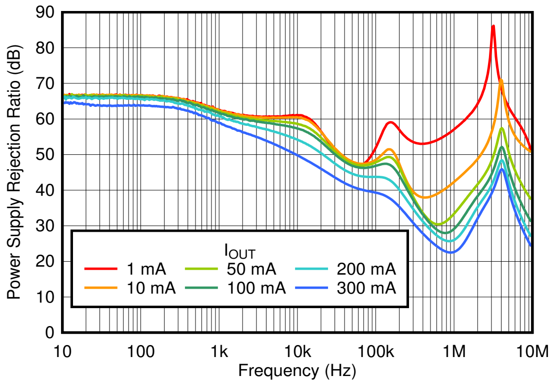
V_{OUT} = 3.3 V, I_{OUT} = 90 mA to 200 mA, I_{OUT} slew rate = 1 A/µs, T_J = -40℃

図 6-63. Load Transient



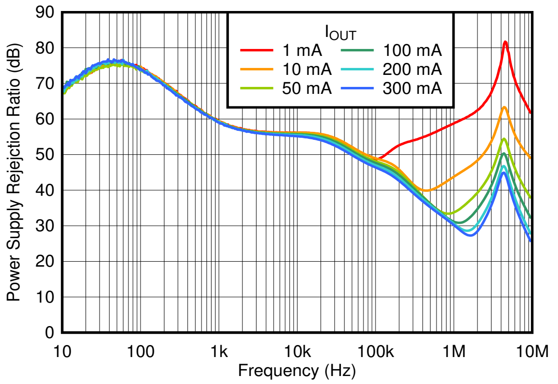
V_{OUT} = 3.3 V, I_{OUT} = 90 mA to 200 mA, I_{OUT} slew rate = 1 A/µs, T_J = 150℃

図 6-64. Load Transient



V_{IN} = 1.65 V, C_{IN} = 0 µF, V_{OUT} = 0.65 V

図 6-65. PSRR vs Frequency and I_{OUT}

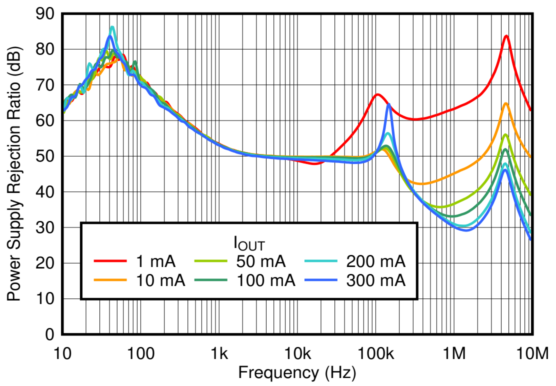


V_{IN} = 2.2 V, C_{IN} = 0 µF, V_{OUT} = 1.2 V

図 6-66. PSRR vs Frequency and I_{OUT}

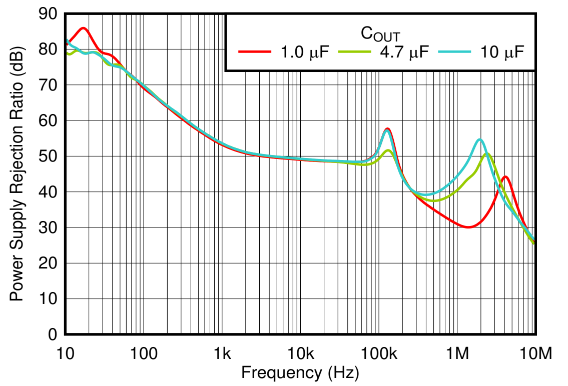
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



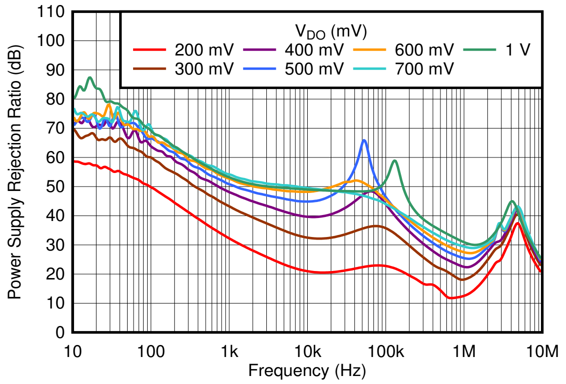
V_{IN} = 4.3 V, C_{IN} = 0 µF, V_{OUT} = 3.3 V

図 6-67. PSRR vs Frequency and I_{OUT}



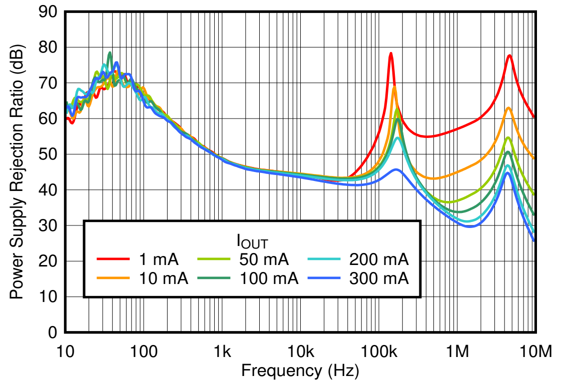
V_{IN} = 4.3 V, C_{IN} = 0 µF, V_{OUT} = 3.3 V, I_{OUT} = 300 mA

図 6-68. PSRR vs Frequency and C_{OUT}



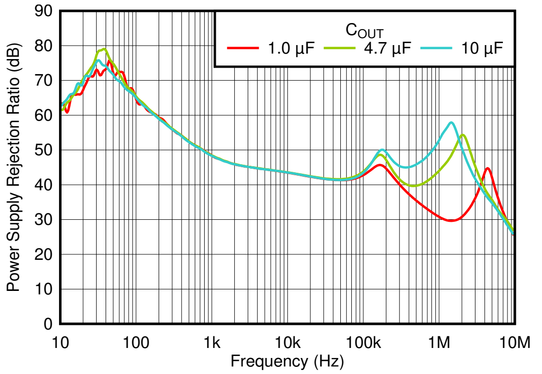
C_{IN} = 0 µF, V_{OUT} = 3.3 V, I_{OUT} = 300 mA

図 6-69. PSRR vs Frequency and V_{DO}



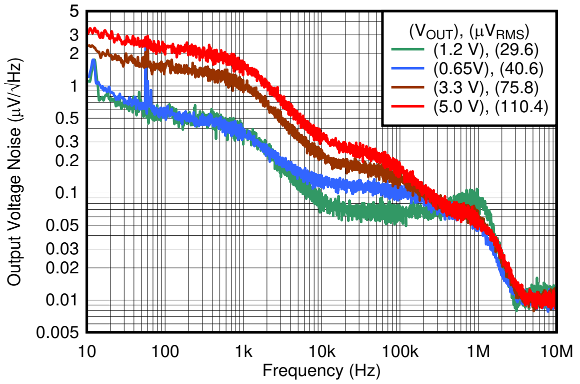
V_{IN} = 6 V, C_{IN} = 0 µF, V_{OUT} = 5.0 V

図 6-70. PSRR vs Frequency and I_{OUT}



V_{IN} = 6 V, C_{IN} = 0 µF, V_{OUT} = 5.0 V, I_{OUT} = 300 mA

図 6-71. PSRR vs Frequency and C_{OUT}

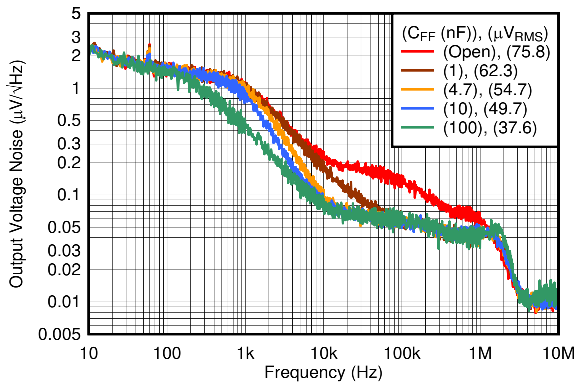


V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 300 mA,
V_{RMS} BW = 10 Hz to 100 kHz

図 6-72. Output Noise vs Frequency and V_{OUT}

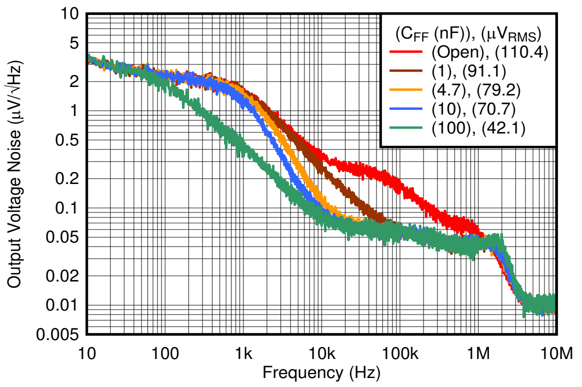
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and $V_{IN} = V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



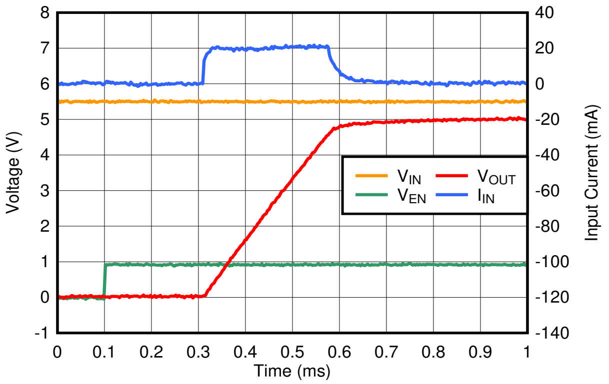
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 300 mA,
V_{RMS} BW = 10 Hz to 100 kHz

図 6-73. Output Noise vs Frequency and C_{FF}



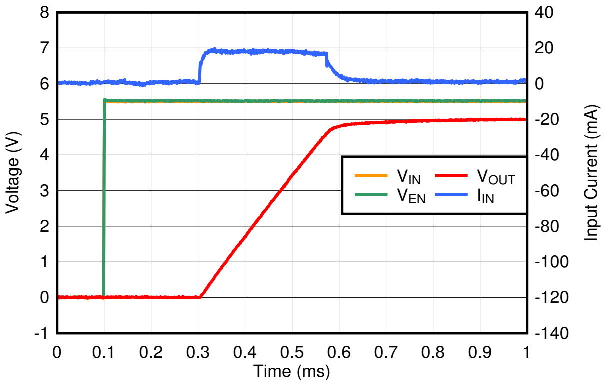
V_{IN} = 6 V, V_{OUT} = 5.0 V, I_{OUT} = 300 mA,
V_{RMS} BW = 10 Hz to 100 kHz

図 6-74. Output Noise vs Frequency and C_{FF}



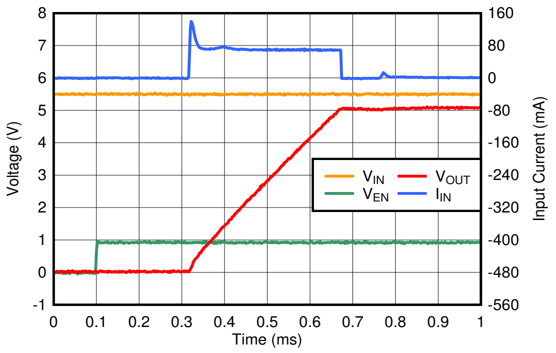
V_{IN} = 5.5 V, C_{IN} = 0 µF, C_{OUT} = 1 µF, V_{OUT} = 5.0 V,
I_{OUT} = 0 mA

図 6-75. Start-Up Inrush Current With C_{OUT} = 1 µF



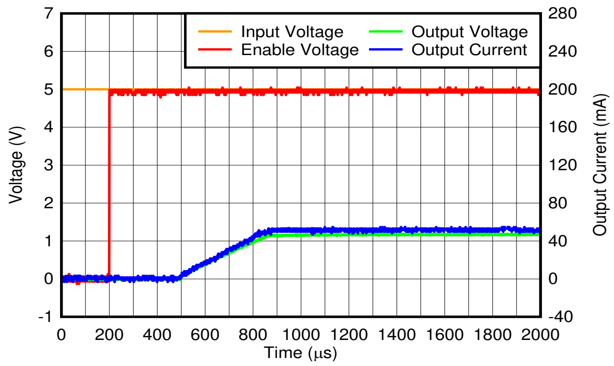
V_{IN} = V_{EN} = 5.5 V, C_{IN} = 0 µF, C_{OUT} = 1 µF, V_{OUT} = 5.0 V,
I_{OUT} = 0 mA

図 6-76. Start-Up Inrush Current With C_{OUT} = 1 µF



V_{IN} = 5.5 V, C_{IN} = 0 µF, C_{OUT} = 4.7 µF, V_{OUT} = 5.0 V,
I_{OUT} = 0 mA

図 6-77. Start-Up Inrush Current With C_{OUT} = 4.7 µF

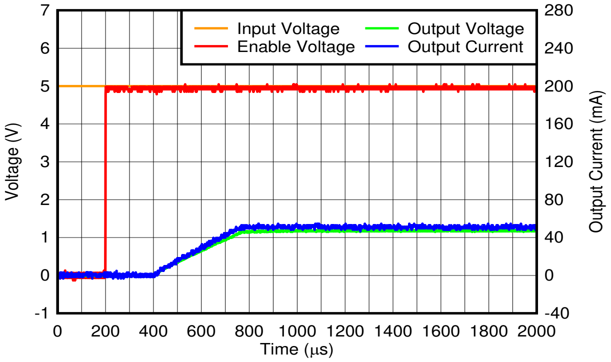


V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 10 µF, V_{OUT} = 1.2 V,
I_{OUT} = 500 mA

図 6-78. Start Up at –40°C

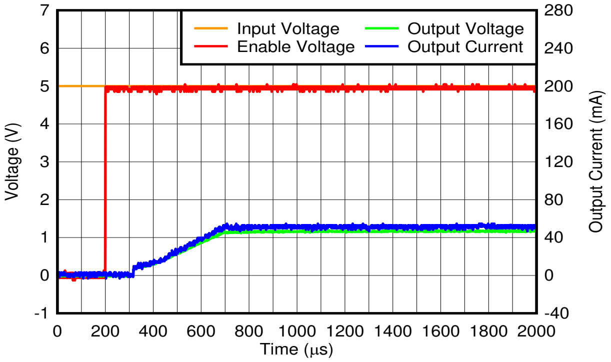
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF, and V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



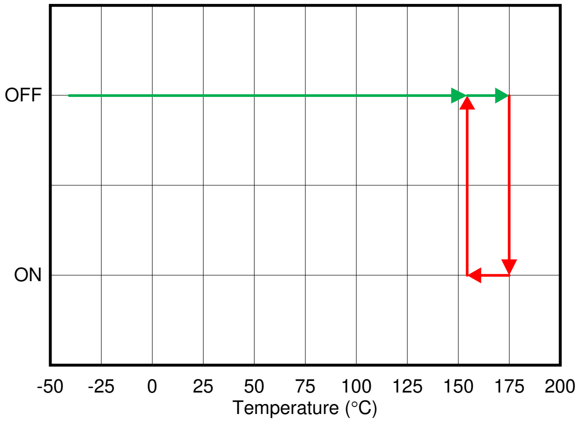
V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 10 µF, V_{OUT} = 1.2 V, I_{OUT} = 500 mA

図 6-79. Start Up at 25°C



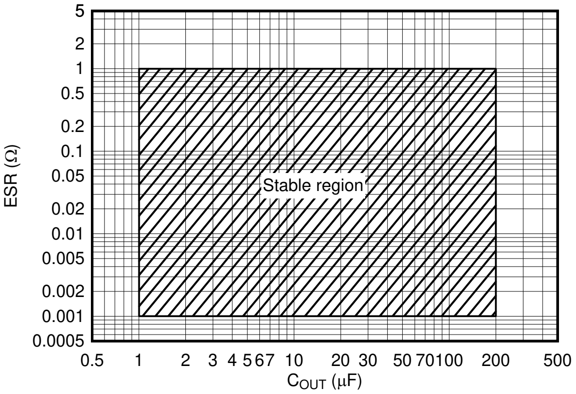
V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 10 µF, V_{OUT} = 1.2 V, I_{OUT} = 500 mA

図 6-80. Start Up at 150°C



V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 10 µF, V_{OUT} = 1.2 V, I_{OUT} = 500 mA

図 6-81. Thermal Shutdown Activation



C_{OUT} denotes nominal capacitor size (not effective capacitance)

図 6-82. ESR vs C_{OUT}

7 Detailed Description

7.1 Overview

The TPS784-Q1 is an ultra low-dropout, high PSRR, high-accuracy linear voltage regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most automotive applications.

This regulator offers foldback current limit, output enable, active discharge, undervoltage lockout (UVLO), and thermal protection.

7.2 Functional Block Diagrams

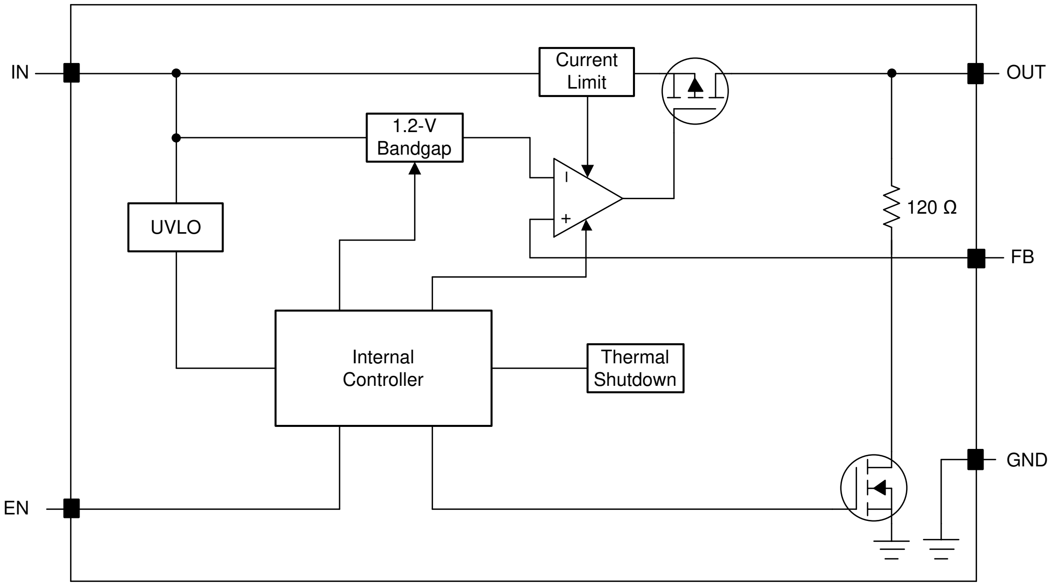


図 7-1. Adjustable Version Block Diagram

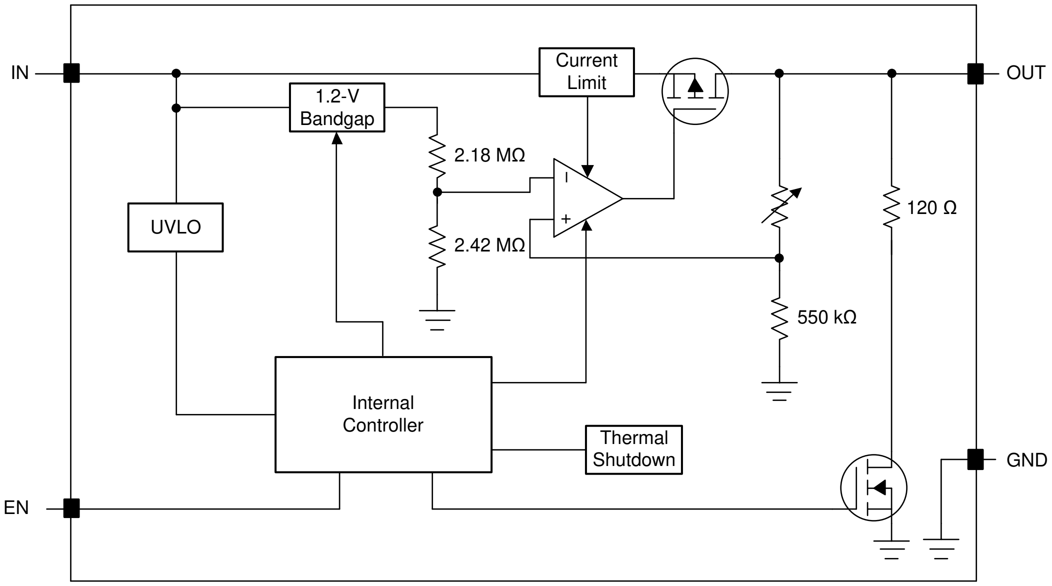


図 7-2. Fixed Version Block Diagram

7.3 Feature Description

7.3.1 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

図 7-3 shows a diagram of the foldback current limit.

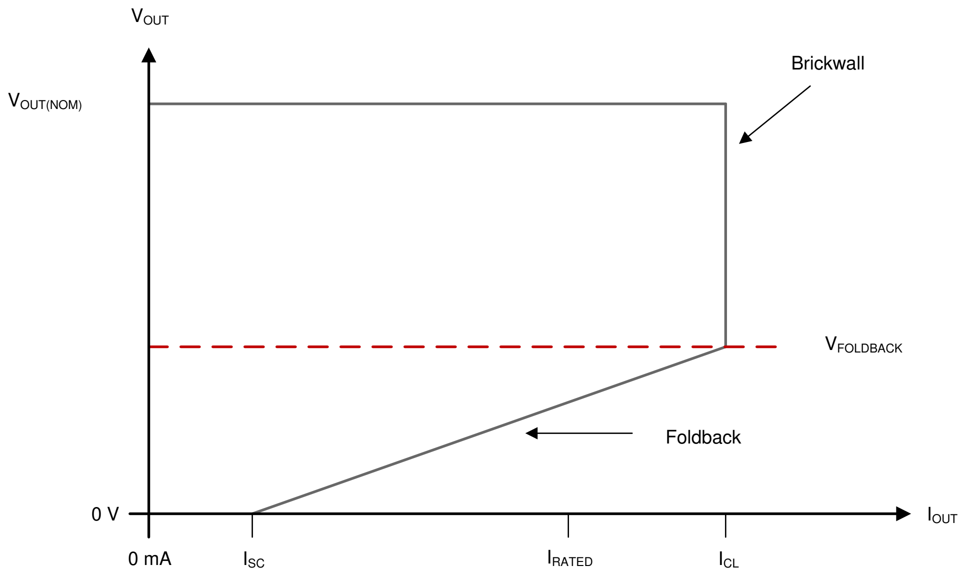


図 7-3. Foldback Current Limit

7.3.2 Output Enable

The enable pin (EN) is active high. Enable the device by forcing the voltage of the enable pin to exceed the minimum EN pin high-level input voltage (see the *Electrical Characteristics* table). Turn off the device by forcing the voltage of the enable pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

7.3.3 Active Discharge

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit to discharge the output voltage after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device, especially when a large output capacitor is used. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.3.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. 図 7-4 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

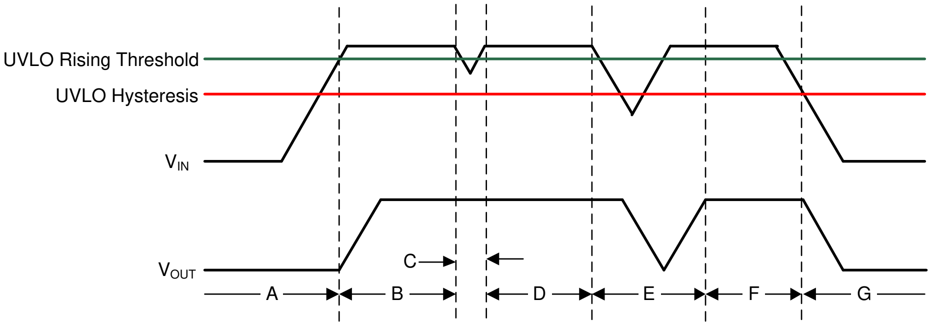


図 7-4. Typical UVLO Operation

7.3.5 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

The device requires an input capacitor of 1.0 µF or larger as specified in the *Recommended Operating Conditions* table for stability. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

The device also requires an output capacitor of 1.0 µF or larger as specified in the *Recommended Operating Conditions* table for stability. Dynamic performance of the device is improved by using a higher capacitor than the minimum output capacitor.

8.1.3 Adjustable Device Feedback Resistors

The device requires external feedback divider resistors to set the output voltage. 図 8-1 shows how the output voltage of an adjustable device can be configured from 1.2 V to 5.5 V by using a resistor divider network.

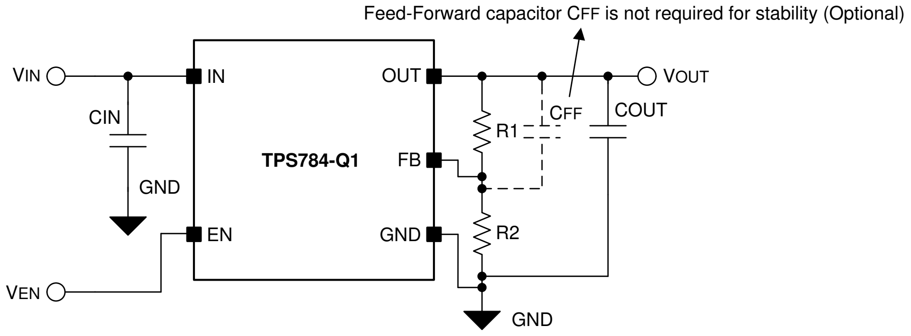


図 8-1. Adjustable Operation

式 2 calculates the values of the R_1 and R_2 resistors to set the output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) + I_{FB} \times R_1 \tag{2}$$

To disregard the effect of the FB pin current error term in 式 2 and to achieve best accuracy, choose R_2 to be equal to or smaller than 550 kΩ so that the current flowing through R_1 and R_2 is at least 100 times larger than the I_{FB} current listed in the *Electrical Characteristics* table. Lowering the value of R_2 increases the immunity against noise injection. Increasing the value of R_2 reduces the quiescent current for achieving higher efficiency at low load currents. 式 3 calculates the setting that provides the maximum feedback divider series resistance.

$$(R_1 + R_2) \leq V_{OUT} / (I_{FB} \times 100) \tag{3}$$

8.1.4 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 図 8-2 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

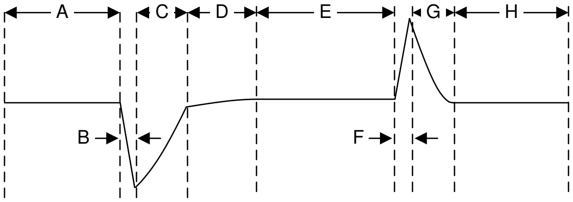


図 8-2. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.5 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in 図 8-3, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

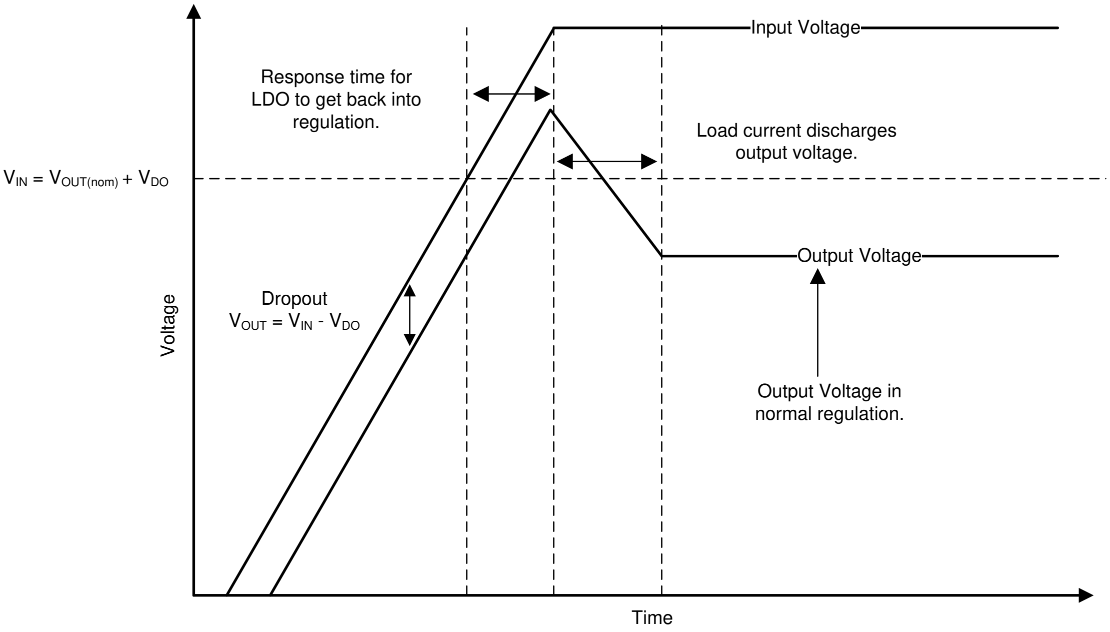


図 8-3. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 図 8-4 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

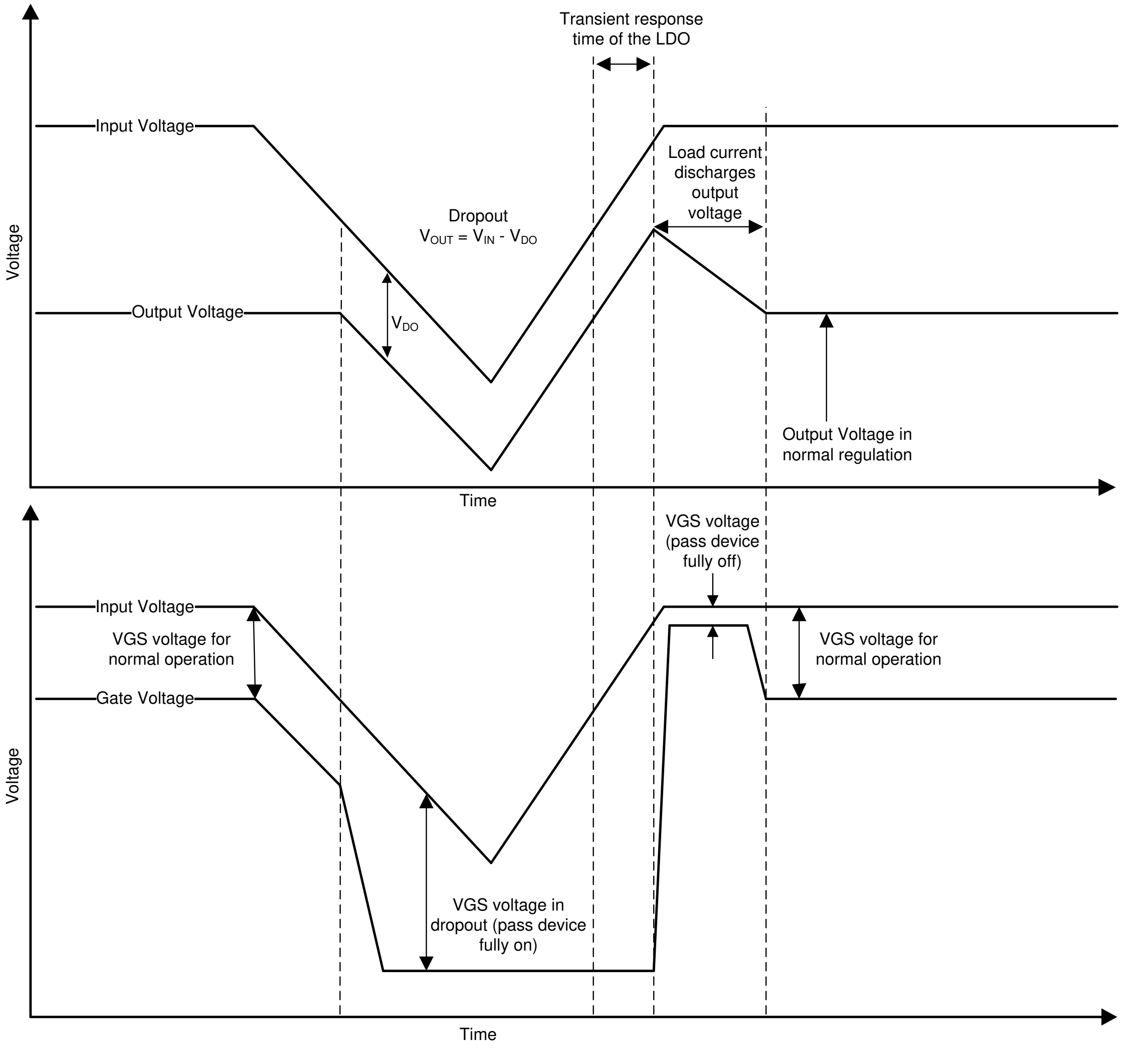


図 8-4. Line Transients From Dropout

8.1.6 Dropout Voltage

The device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

8.1.7 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. 図 8-5 shows one approach of protecting the device.

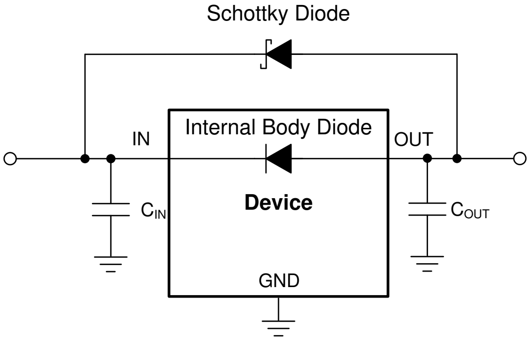


図 8-5. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.8 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

8.1.9 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 4 to approximate P_D:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS784-Q1 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 式 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). 式 6 rearranges 式 5 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{5}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{6}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Recommended Operating Conditions* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the VSON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.9.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 7 and are given in the *Recommended Operating Conditions* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (7)$$

where:

- P_D is the power dissipated as explained in 式 4
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.9.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 図 8-6 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output (V_{IN} – V_{OUT}) at a given output current level. See the *Dropout Voltage* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 式 6. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when V_{IN} – V_{OUT} increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of V_{IN} – V_{OUT}.

図 8-6 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Recommended Operating Conditions* table.

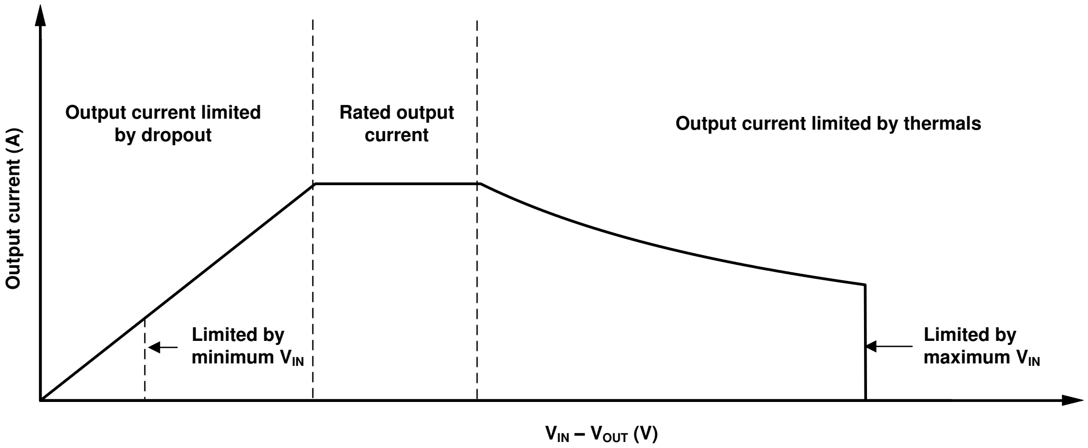


図 8-6. Region Description of Continuous Operation Regime

8.1.9.3 Power Dissipation versus Ambient Temperature

図 8-7 is based off of a JESD51-7 four-layer high-K board. The allowable power dissipation was estimated using the following equation. As disscussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application report, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%.

$$T_A + R_{\theta JA}\, x\, P_D \leq 150\ °C \tag{8}$$

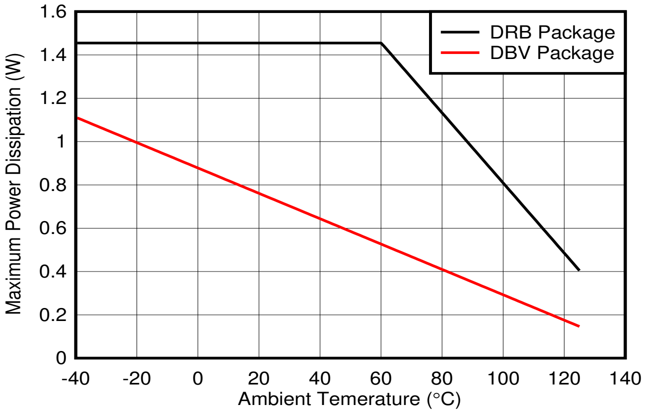


図 8-7. Allowable Power Dissipation

8.2 Typical Application

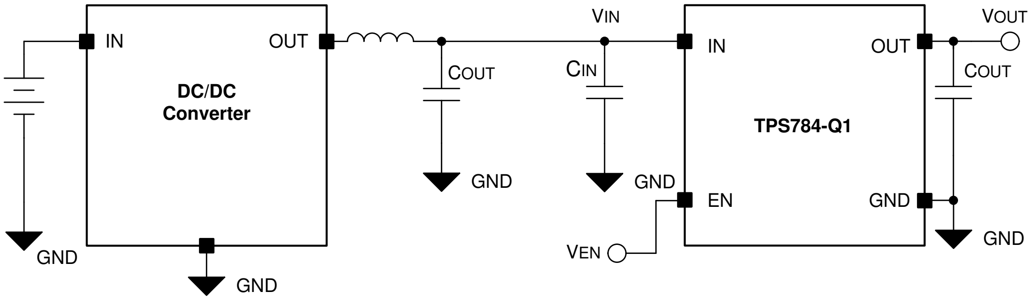


図 8-8. Operation From a DC/DC Converter

8.2.1 Design Requirements

表 8-1 summarizes the design requirement for this application.

表 8-1. Design Parameters

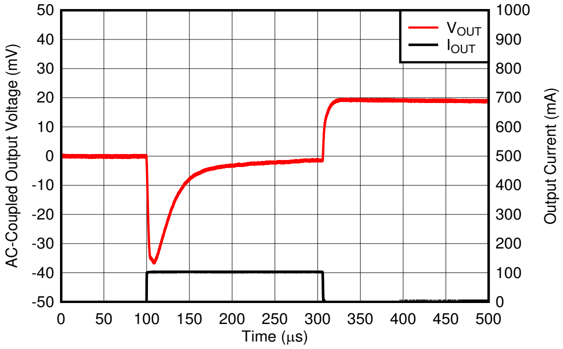
PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	3.3 V, ±1.5%
Output load	100 mA
Output capacitor	10 µF
Maximum ambient temperature	85°C

8.2.2 Detailed Design Procedure

For this design example, the 3.3-V, fixed-version device is selected. The device is powered of a DC/DC converter connected to a battery. A 500-mV headroom between V_{IN} and V_{OUT} is used to keep the device within the dropout voltage specification and to ensure the device stays in regulation under all load and temperature conditions for this design.

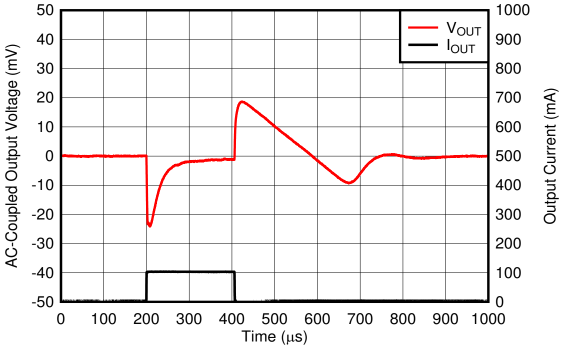
8.2.3 Application Curves

A 10-µF capacitor is used to reduce overshoot and undershoot of output voltage during load transients with ramps rates greater than 0.5 A/µs. 図 8-9 and 図 8-10 show captures of load transient behavior for this application.



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF,
I_{OUT} slew rate = 1 A/µs

図 8-9. I_{OUT} Transient From 0 mA to 100 mA



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF,
I_{OUT} slew rate = 1 A/µs

図 8-10. I_{OUT} Transient From 1 mA to 100 mA

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.65 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V. TI requires using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

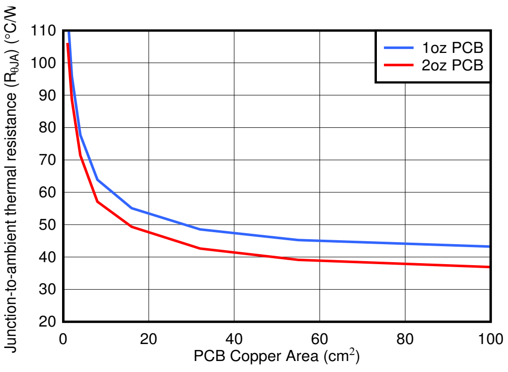
10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Only place tented thermal vias directly beneath the thermal pad of the DRB package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

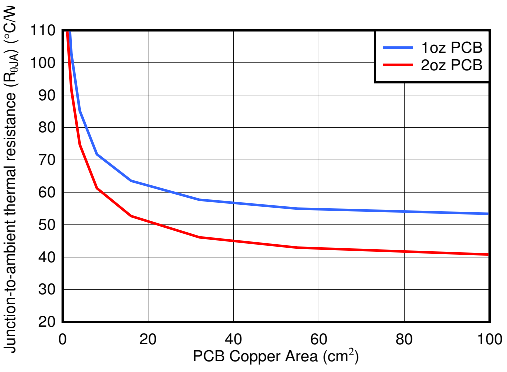
10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends using a fixed-voltage version of the device, or isolating the FB node by placing a copper ground plane on the layer directly underneath the LDO circuitry and FB pin to minimize any undesirable signal coupling.



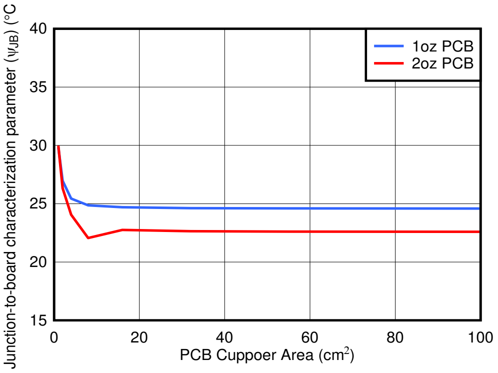
4-layer PCB

図 10-1. Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$) vs PCB Copper Area



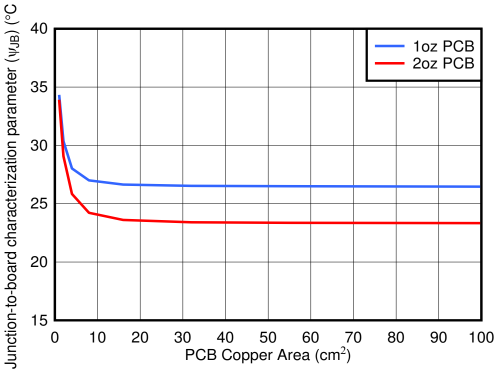
2-layer PCB

図 10-2. Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$) vs PCB Copper Area



4-layer PCB

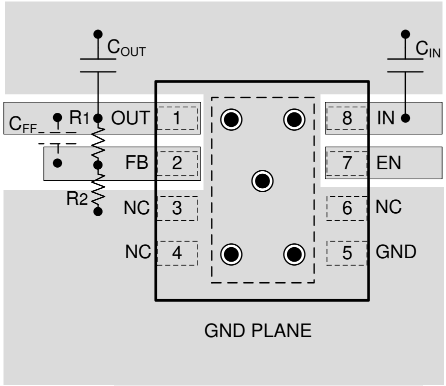
図 10-3. Junction-to-Board Characterization Parameter (ψ_{JB}) vs PCB Copper Area



2-layer PCB

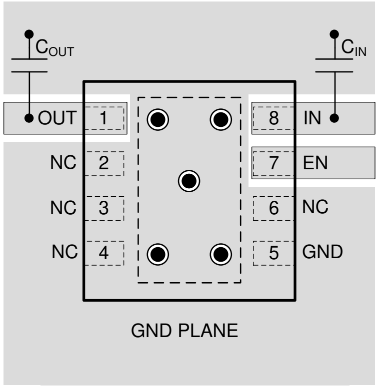
図 10-4. Junction-to-Board Characterization Parameter (ψ_{JB}) vs PCB Copper Area

10.2 Layout Examples



● Represents a thermal via

図 10-5. Layout Example for the DRB Package Adjustable Version



● Represents a thermal via

図 10-6. Layout Example for the DRB Package Fixed Version

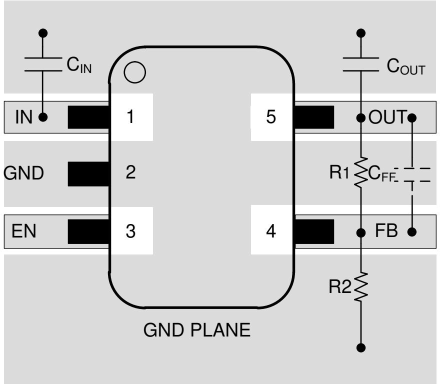


図 10-7. Layout Example for the DBV Package Adjustable Version

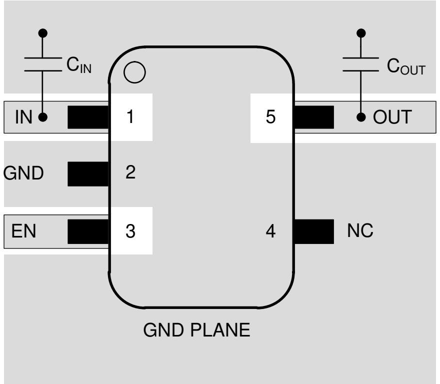


図 10-8. Layout Example for the DBV Package Fixed Version

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

表 11-1. Device Nomenclature

PRODUCT(1) (2)	V_{OUT}
TPS784**xx(x)ZQ(W)yyyRQ1**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 285 = 2.85 V). **Z** indicates the pinout of the device. If no letter is present, the EN pin is pin 7, if the B version is used, EN is now pin 6. **yyy** is the package designator. **W** is used to denote a wettable flank package.

(1) For the most current package and ordering information see the *Package Option Addendum* at the end of this document, or visit the device product folder on www.ti.com.

(2) Output voltages from 0.65 V to 5.5 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Universal Low-Dropout (LDO) Linear Voltage Regulator MultiPkgLDOEVM-823 Evaluation Module user's guide*
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report*
- Texas Instruments, *An empirical analysis of the impact of board layout on LDO thermal performance application report*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS78401BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8401BQ
TPS78401BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8401BQ
TPS78401QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23JF
TPS78401QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23JF
TPS78401QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8401WQ
TPS78401QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8401WQ
TPS784075QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	84075W
TPS784075QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	84075W
TPS784085BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	4085BQ
TPS784085BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	4085BQ
TPS78408BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8408BQ
TPS78408BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8408BQ
TPS78408QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2BGF
TPS78408QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2BGF
TPS784105QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	84105W
TPS784105QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	84105W
TPS78410QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8410WQ
TPS78410QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8410WQ
TPS78411QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8411WQ
TPS78411QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8411WQ
TPS78412BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8412BQ
TPS78412BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8412BQ
TPS78412QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23KF
TPS78412QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23KF
TPS78412QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8412WQ
TPS78412QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8412WQ
TPS78415QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	23LF
TPS78415QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23LF
TPS78415QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8415WQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS78415QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8415WQ
TPS78417QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	2BHF
TPS78417QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2BHF
TPS78418BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8418BQ
TPS78418BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8418BQ
TPS78418QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23MF
TPS78418QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23MF
TPS78418QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8418WQ
TPS78418QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8418WQ
TPS78425BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8425BQ
TPS78425BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8425BQ
TPS78425QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23NF
TPS78425QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23NF
TPS78425QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8425WQ
TPS78425QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8425WQ
TPS78428QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	23OF
TPS78428QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23OF
TPS78429QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	23PF
TPS78429QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23PF
TPS78430QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	23QF
TPS78430QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23QF
TPS78430QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8430WQ
TPS78430QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8430WQ
TPS78433BQWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8433BQ
TPS78433BQWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8433BQ
TPS78433QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23RF
TPS78433QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	23RF
TPS78433QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8433WQ
TPS78433QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8433WQ
TPS78450QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	2BIF
TPS78450QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2BIF

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS78450QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8450WQ
TPS78450QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	8450WQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS784-Q1 :

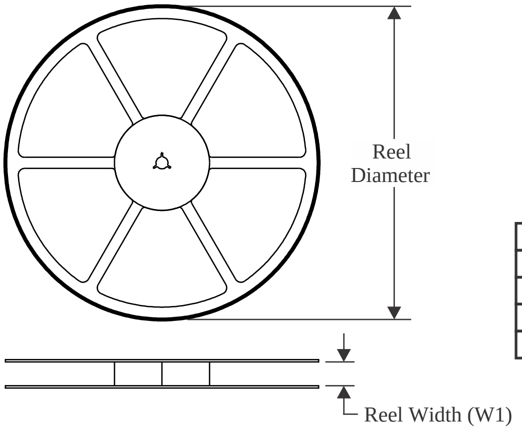
- Catalog : TPS784

NOTE: Qualified Version Definitions:

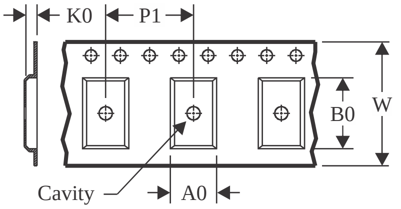
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

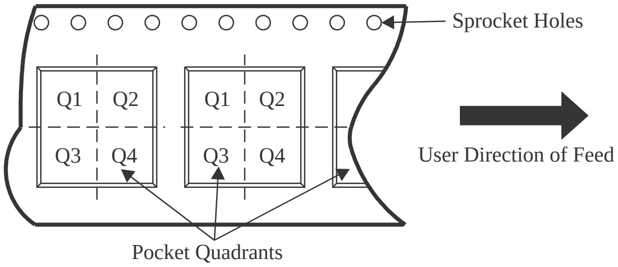


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

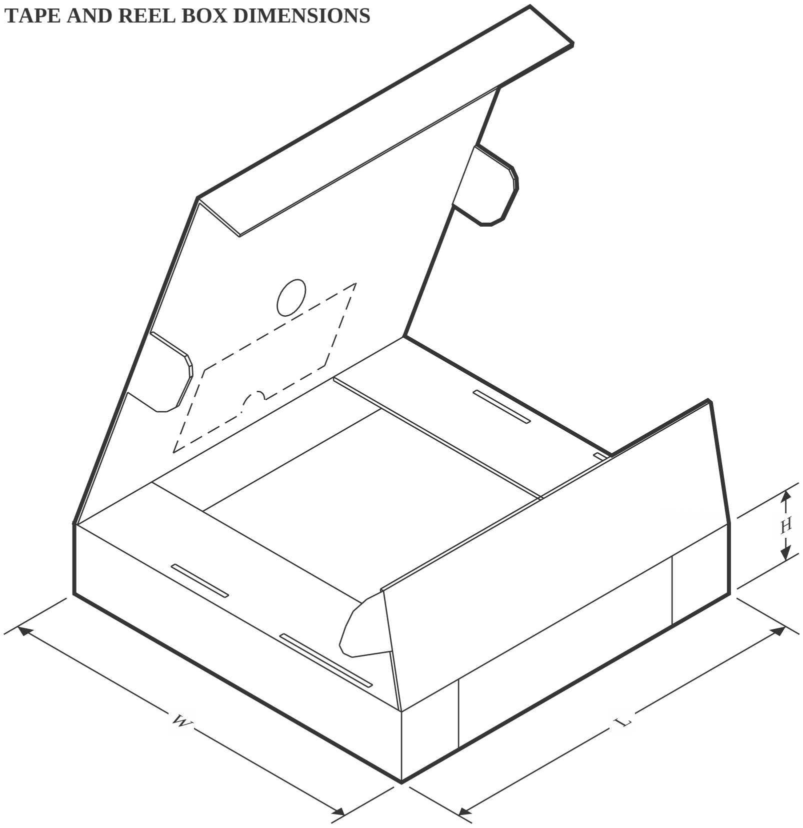


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78401BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78401QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78401QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS784075QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS784085BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78408BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78408QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78408QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS784105QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78410QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78411QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78412BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78412QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78412QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78412QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78415QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78415QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78417QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78417QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78418BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78418QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78418QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78418QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78425BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78425QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78425QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78425QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78428QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78429QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78430QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78430QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78433BQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78433QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78433QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78433QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3
TPS78450QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78450QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q3

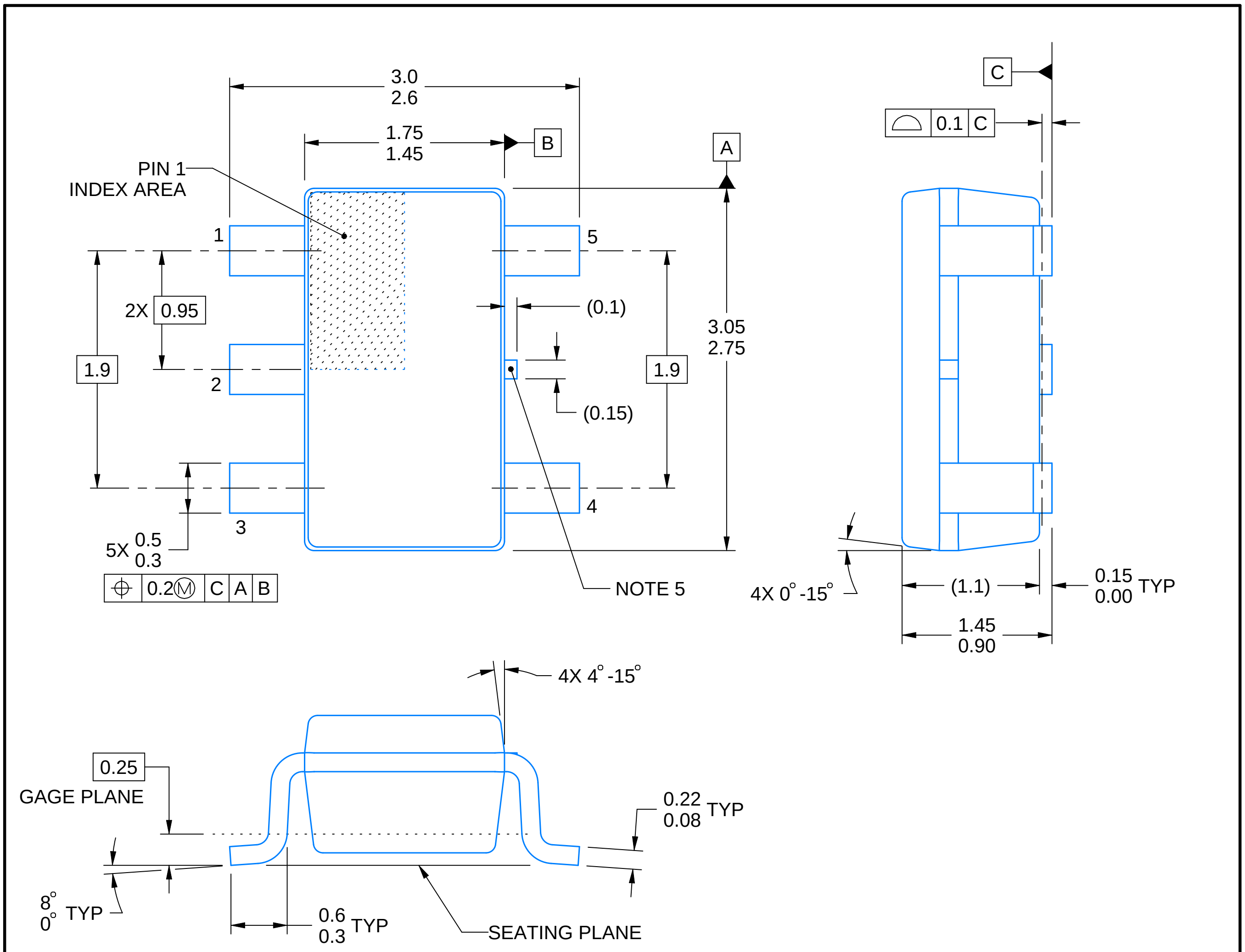
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78401BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78401QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78401QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS784075QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS784085BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78408BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78408QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78408QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS784105QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78410QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78411QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78412BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78412QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78412QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78412QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78415QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78415QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78417QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

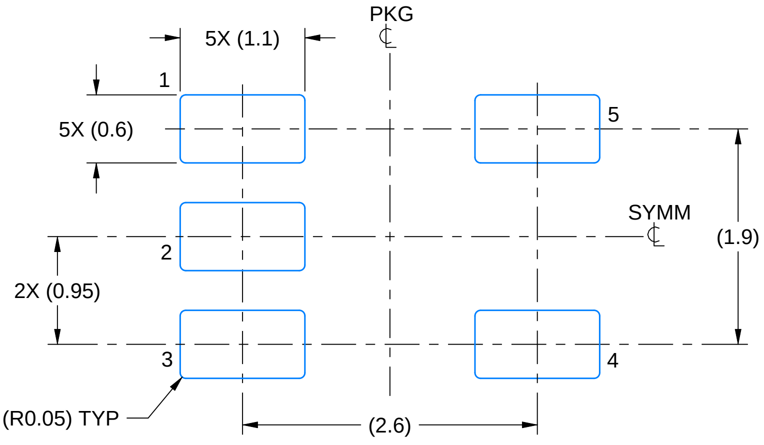
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78417QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78418BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78418QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78418QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78418QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78425BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78425QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78425QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78425QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78428QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78429QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78430QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78430QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78433BQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78433QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78433QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78433QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS78450QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS78450QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0



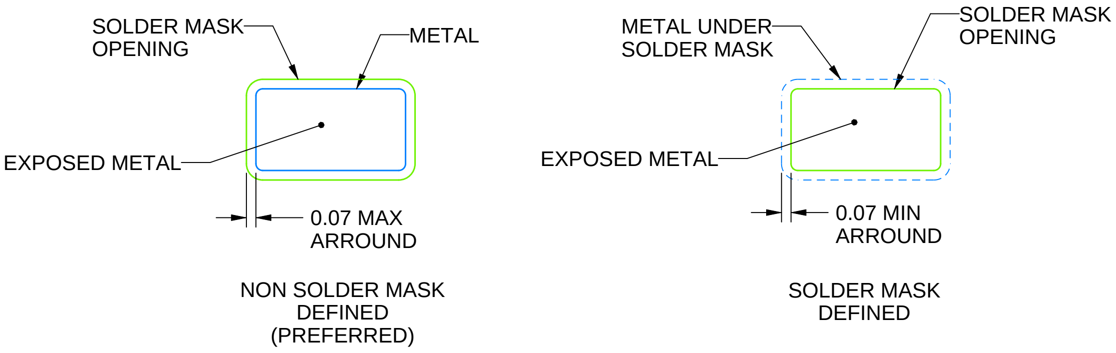
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

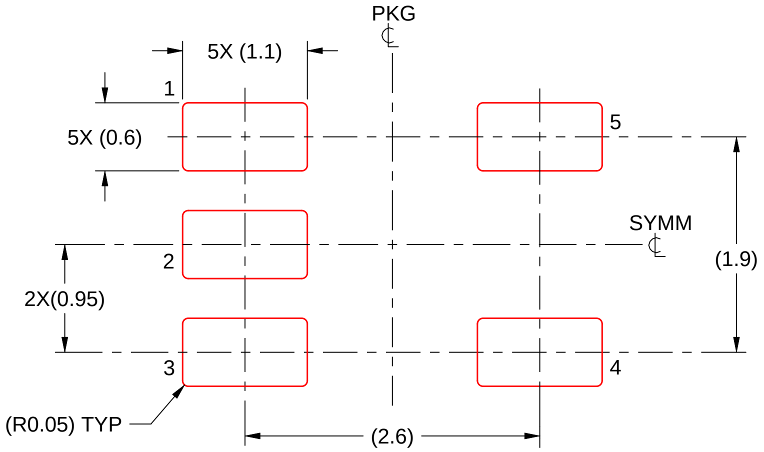


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

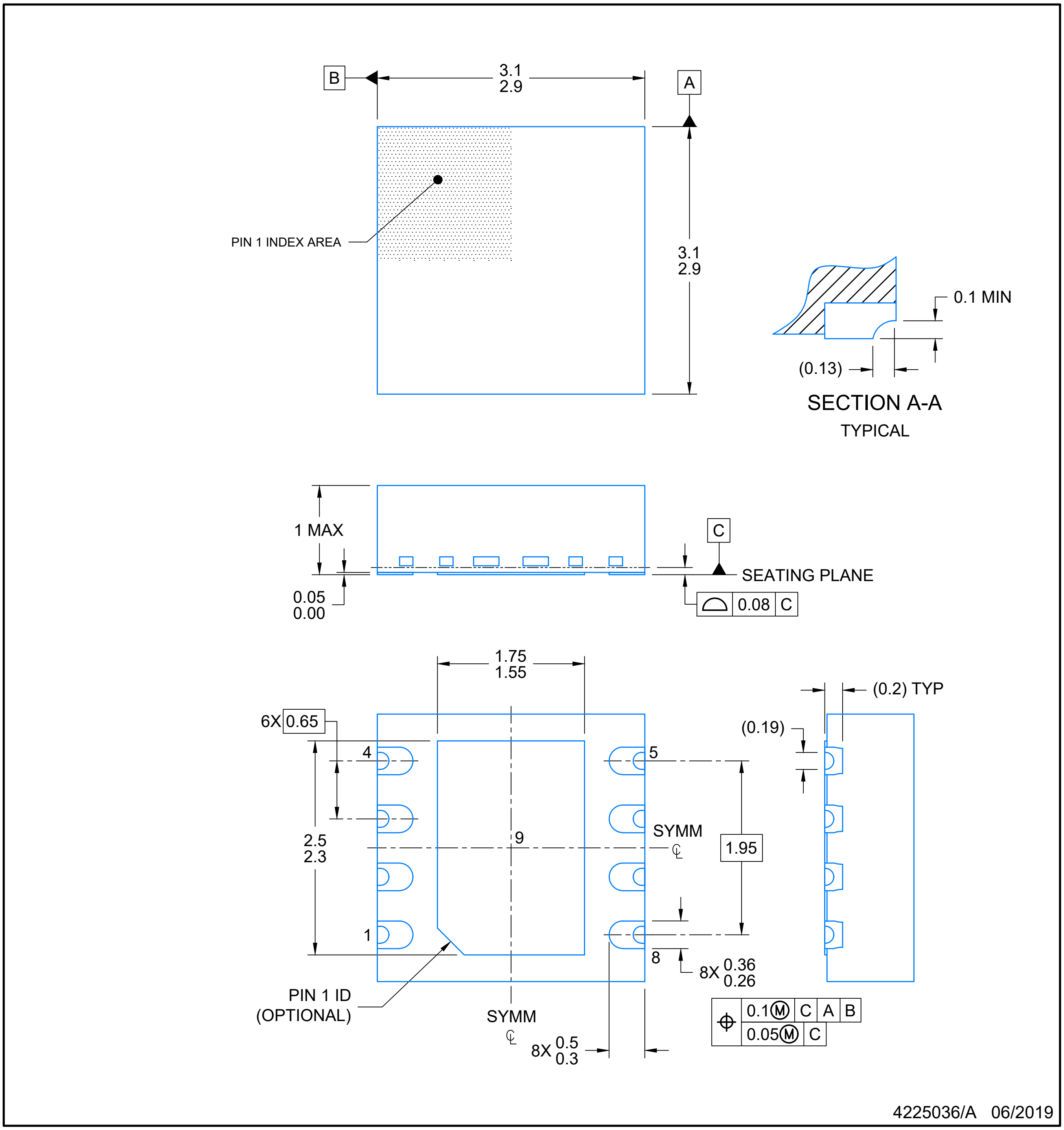
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRB0008J

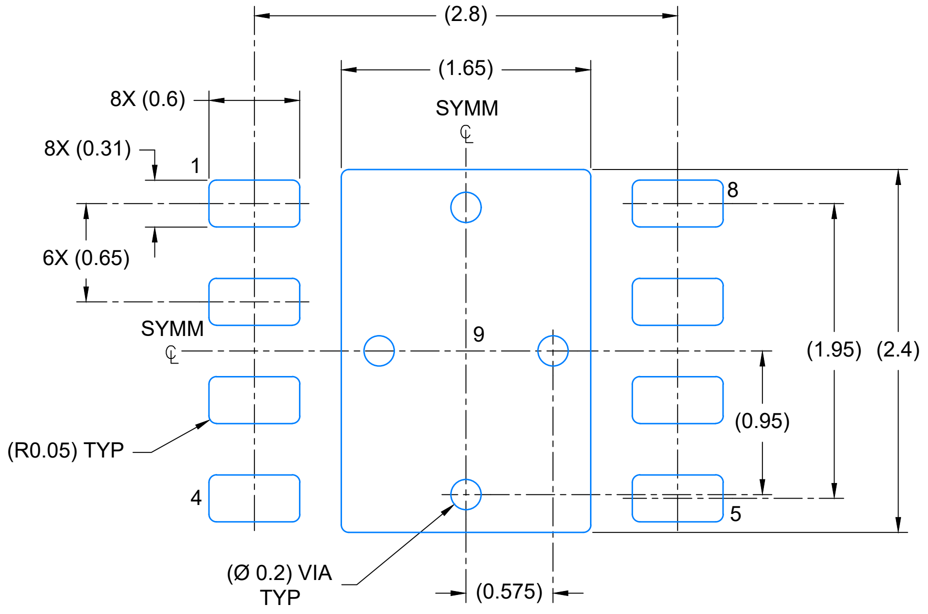
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

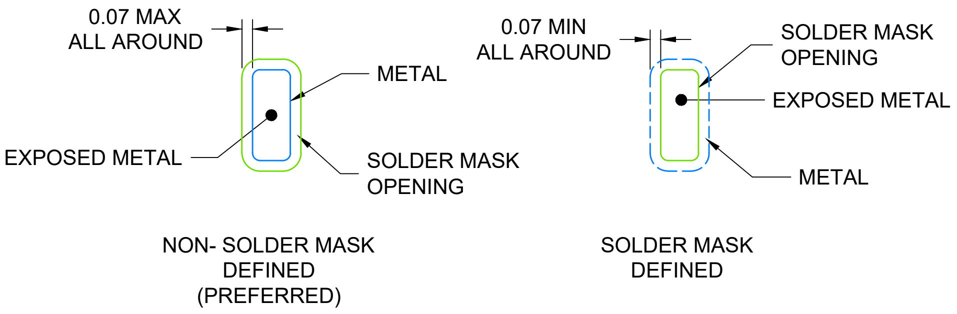


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

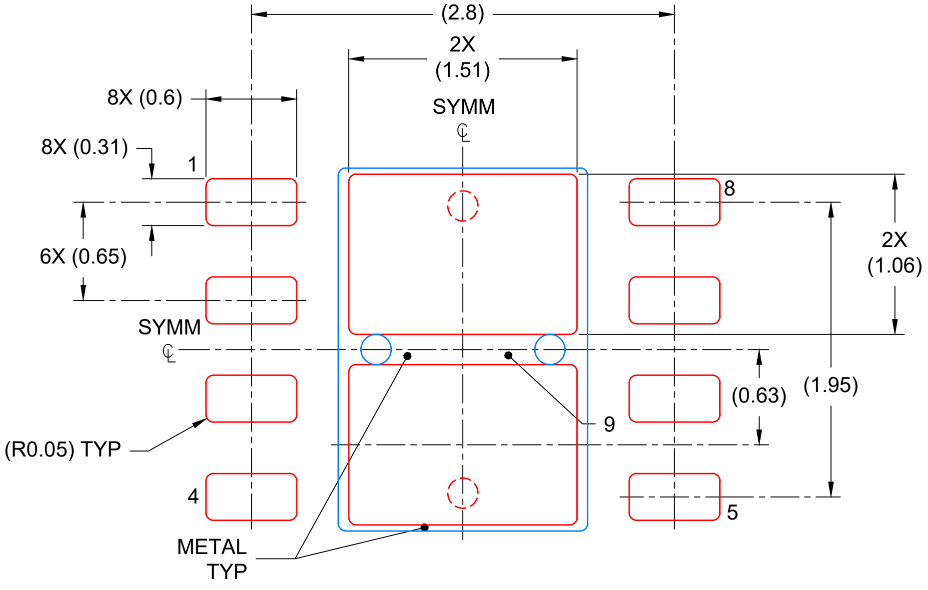
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項