TEXAS INSTRUMENTS
TPS7A02
JAJSHP3C – JULY 2019 – REVISED SEPTEMBER 2022

# TPS7A02 高速過渡応答、ナノパワー $I_Q$ = 25nA、200mA、低ドロップアウト電圧レギュレータ

## 1 特長

- きわめて低い $I_Q$: 25 ドロップアウト時でも nA (標準値)
- シャットダウン時 $I_Q$:3nA (標準値)
- 非常に優れた過渡応答 (1mA～50mA)
  - セトリング時間:10µs 未満
  - アンダーシュート:100mV
- パッケージ
  - 1.0mm × 1.0mm の X2SON
  - SOT23-5
  - 0.64mm × 0.64mm の DSBGA
- 入力電圧範囲:1.5V～6.0V
- 出力電圧範囲 0.8V～5.0V (固定)
- 出力精度:温度範囲全体で 1.5%
- スマート・イネーブルのプルダウン
- 非常に低いドロップアウト
  - 270mV 以下 (200mA、$V_{OUT}$ = 3.3V の場合)
- 1µF 以上のコンデンサで安定

## 2 アプリケーション

- ウェアラブル電子機器
- サーモスタット、煙感知器、熱感知器
- ガス、暖房、水道メーター
- 血糖値測定器およびパルス・オキシメータ (血中酸素飽和度計)
- 住宅用サーキット・ブレーカーおよび故障表示器
- ビル・セキュリティおよびビデオ監視デバイス
- EPOS (POS システム) カード・リーダー

## 3 概要

TPS7A02 は、非常に優れた過渡性能で 200mA を供給できる超小型超低静止電流の低ドロップアウト・レギュレータ (LDO) です。

$I_Q$ が 25nA と非常に小さい TPS7A02 は、超低静止電流が重要な条件であるアプリケーション向けに設計されています。このデバイスはドロップアウト・モードでも小さな $I_Q$ 消費を維持するため、バッテリ動作時間をさらに延長できます。シャットダウンまたはディセーブル・モードでは、わずか 3nA の $I_Q$ しか消費しないため、バッテリの保存寿命を延ばすのに役立ちます。
TPS7A02 は、最新のマイクロコントローラ (MCU) の低いコア電圧に対応するため、0.8V～5.0V (50mV 刻み) の出力範囲の製品を提供しています。

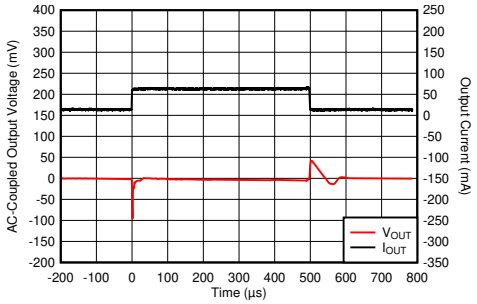
TPS7A02 は、スマート・イネーブル回路を備え、内部で制御されるプルダウン抵抗により、EN ピンをフローティング状態のままにしても LDO をディセーブル状態に維持します。これにより、EN ピンのプルダウンに使用する外付け部品を最小限に抑えることができます。この回路は、本デバイスがイネーブル状態のときに外付けプルダウン回路を流れる電流を最小化するのにも役立ちます。

TPS7A02 は、$T_J$ = -40℃～+125℃の範囲で動作が完全に規定されています。

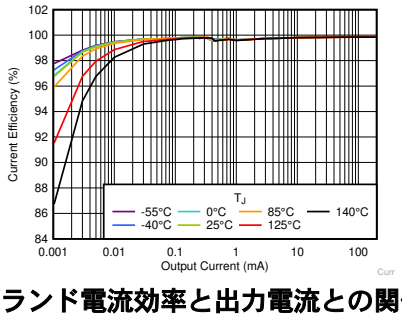
**パッケージ情報**(1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| TPS7A02 | DQN (X2SON、4) | 1.00mm × 1.00mm |
| | YCH (DSBGA、4) | 0.64mm×0.64mm |
| | DBV (SOT-23、5) | 2.90mm × 1.60mm |

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。




**負荷過渡応答 ($V_{IN}$ = $V_{OUT}$ + 1V、$C_{OUT}$ = 1µF、$I_{OUT}$ = 1µs で 1mA から 50mA に変化)**




**グランド電流効率と出力電流との関係**

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision B (March 2020) to Revision C (September 2022) | Page |
|---|---|
| • YCH (DGBGA) パッケージをプレビューから量産データに変更 | 1 |

| Changes from Revision A (December 2019) to Revision B (March 2020) | Page |
|---|---|
| • DBV (SOT23-5) パッケージをプレビューから量産データに変更 | 1 |


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## 5 Pin Configuration and Functions

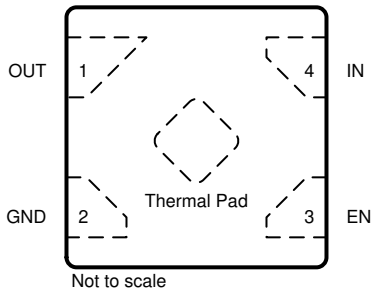



**図 5-1. DQN Package, 1-mm × 1-mm, 4-Pin X2SON (Top View)**

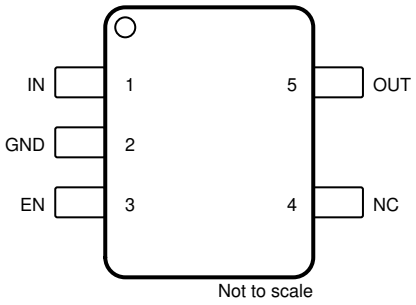



**図 5-2. DBV Package, 5-Pin SOT-23 (Top View)**

**表 5-1. Pin Functions: DQN, DBV**

| PIN | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | DQN | DBV | | |
| EN | 3 | 3 | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up. |
| GND | 2 | 2 | — | Ground pin. This pin must be connected to ground on the board. |
| IN | 4 | 1 | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible. |
| NC | — | 4 | — | No connect pin. This pin is not internally connected. Connect to ground or leave floating. |
| OUT | 1 | 5 | Output | Regulated output pin. A 0.5-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table. |
| Thermal pad | | — | — | Connect the thermal pad to a large-area ground plane. The thermal pad is internally connect to ground. |

(1) NC = No internal connection.

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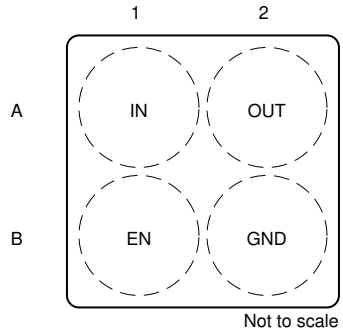



**図 5-3. YCH Package, 4-Pin DSBGA, 0.35-mm Pitch (Top View)**

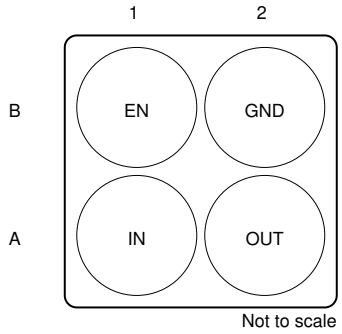



**図 5-4. YCH Package, 4-Pin DSBGA, 0.35-mm Pitch (Bottom View)**

**表 5-2. Pin Functions: YCH**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| YCH | NAME | | |
| A1 | IN | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to input of the device as possible. |
| A2 | OUT | Output | Regulated output pin. A 0.5-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table. |
| B1 | EN | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up. |
| B2 | GND | — | Ground pin. This pin must be connected to ground and the thermal pad. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 6.5 | V |
| | $V_{EN}$ | –0.3 | 6.5 | |
| | $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3 or 5.5(2) | |
| Current | Maximum output | Internally limited | | A |
| Temperature | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum is $V_{IN}$ + 0.3 V or 5.5 V, whichever is smaller.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 1.5 | | 6.0 | V |
| $V_{EN}$ | Enable voltage | 0 | | 6.0 | V |
| $V_{OUT}$ | Output voltage | 0.8 | | 5.0 | V |
| $I_{OUT}$ | Output current | 0 | | 200 | mA |
| $C_{IN}$ | Input capacitor | | 1 | | µF |
| $C_{OUT}$ | Output capacitor(1) (2) | 1 | 1 | 22 | µF |
| $F_{EN}$ | EN toggle frequency | | | 10 | kHz |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) 22 µF is the maximum derated capacitance that can be used for stability.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS7A02 | | | UNIT |
|---|---|---|---|---|---|
| | | DQN (X2SON) | DBV (SOT-23-5) | YCH (DSBGA) | |
| | | 4 PINS | 5 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 179.1 | 181.9 | 201.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 137.6 | 53.0 | 2.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 116.3 | 88.1 | 67.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.1 | 27.1 | 1.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 116.3 | 52.7 | 67.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | 112.3 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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## 6.5 Electrical Characteristics

Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Nominal accuracy | $T_J$ = 25°C, $V_{OUT}$ ≥ 1.5 V, 1 µA[3] ≤ $I_{OUT}$ ≤ 1 mA | | –1 | | 1 | % |
| | | $T_J$ = 25°C; $V_{OUT}$ < 1.5 V | | –15 | | 15 | mV |
| | Accuracy over temperature | $V_{OUT}$ ≥ 1.5 V | $T_J$ = –40°C to +125°C | –1.5 | | 1.5 | % |
| | | $V_{OUT}$ < 1.5 V | | –20 | | 20 | mV |
| $\Delta V_{OUT}(\Delta V_{IN})$ | Line regulation | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.0 V[1] | $T_J$ = –40°C to +125°C | | | 5 | mV |
| $\Delta V_{OUT}(\Delta I_{OUT})$ | Load regulation[2] | 1 mA ≤ $I_{OUT}$ ≤ 200 mA, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V[1] | $T_J$ = –40°C to +85°C | | 20 | 38 | mV |
| | | | $T_J$ = –40°C to +125°C | | | 50 | |
| $I_{GND}$ | Ground current | $I_{OUT}$ = 0 mA | $T_J$ = 25°C | | 25 | 46 | nA |
| | | | $T_J$ = –40°C to +85°C | | | 60 | |
| $I_{GND}/I_{OUT}$ | Ground current vs load current | 5 µA ≤ $I_{OUT}$ < 1 mA | $T_J$ = 25°C | | 1 | | % |
| | | 1 mA ≤ $I_{OUT}$ < 100 mA | | | 0.25 | | |
| | | $I_{OUT}$ ≥ 100 mA | | | 0.15 | | |
| $I_{GND(DO)}$ | Ground current in dropout[3] | $I_{OUT}$ = 0 mA, $V_{IN}$ = 95% x $V_{OUT\ (NOM)}$ | $T_J$ = 25°C | | 25 | | nA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ = 0 V, 1.5 V ≤ $V_{IN}$ ≤ 5.0 V, $T_J$ = 25°C | | | 3 | 10 | nA |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 90% × $V_{OUT(nom)}$ | $V_{OUT}$ < 2.5V, $V_{IN}$ = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 1.0 V | 240 | 450 | 750 | mA |
| | | | $V_{OUT}$ ≥ 2.5V, $V_{IN}$ = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V | 240 | 450 | 750 | mA |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0 V | | | 65 | | mA |
| $V_{DO}$ | Dropout voltage[4] | $T_J$ = –40°C to +85°C | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | | 1050 | mV |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | | 790 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 650 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 490 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 400 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | | 310 | |
| | | | 3.3 V ≤ $V_{OUT}$ ≤ 5.0 V | | | 270 | |
| | | $T_J$ = –40°C to +125°C | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | | 1100 | |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | | 850 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 700 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 560 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 450 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | | 360 | |
| | | | 3.3 V ≤ $V_{OUT}$ ≤ 5.0 V | | | 310 | |
| PSRR | Power-supply rejection ratio | f = 1 kHz, $I_{OUT}$ = 30 mA | | | 55 | | dB |
| $V_N$ | Output voltage noise | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 0.8 V, $I_{OUT}$ = 30 mA | | | 130 | | $\mu V_{RMS}$ |
| $V_{UVLO}$ | UVLO threshold | $V_{IN}$ rising | | 1.23 | 1.3 | 1.47 | V |
| | | $V_{IN}$ falling | | 1.0 | 1.12 | 1.41 | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | $V_{IN}$ hysteresis | | | 180 | | mV |


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## 6.5 Electrical Characteristics (continued)

Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{EN(HI)}$ | EN pin logic high voltage | | 1.1 | | | V |
| $V_{EN(LOW)}$ | EN pin logic low voltage | | | | 0.3 | V |
| $I_{EN}$ | EN pin leakage current | $V_{EN}$ = $V_{IN}$ = 6.0 V | | 10 | | nA |
| $R_{EN(PULLDOWN)}$ | Smart enable pulldown resistor | $V_{EN}$ = 0.3 V | | 500 | | KΩ |
| $R_{PULLDOWN}$ | Pulldown resistor | $V_{IN}$ = 3.3 V, device disabled | | 60 | | Ω |
| $T_{SD(shutdown)}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | 170 | | °C |
| $T_{SD(reset)}$ | Thermal shutdown reset temperature | Reset, temperature decreasing | | 145 | | |

(1) $V_{IN}$ = 2.0 V for $V_{OUT}$ ≤ 1.5 V.
(2) Load Regulation is normalized to the output voltage at $I_{OUT}$ = 1 mA.
(3) Specified by design
(4) Dropout is measured by ramping $V_{IN}$ down until $V_{OUT}$ = $V_{OUT\ (nom)}$ x 95%, with $I_{OUT}$ = 200 mA.

## 6.6 Switching Characteristics

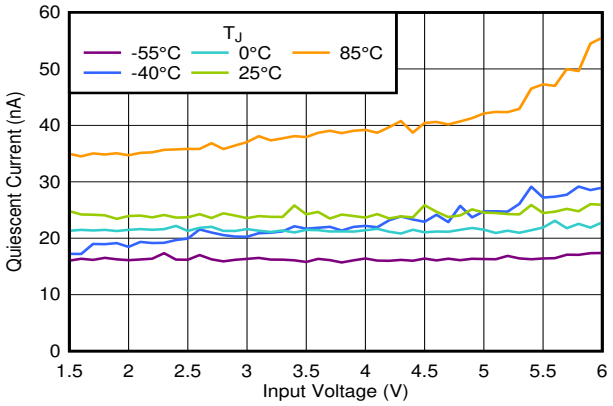
Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STR}$ | Start-up time | From EN assertion to $V_{OUT}$ = 90% × $V_{OUT(nom)}$ | 0.8V ≤ $V_{OUT}$ ≤ 1.5 V | | 500 | 800 | µs |
| | | | 1.5V < $V_{OUT}$ ≤ 3.0 V | | 750 | 1200 | |
| | | | 3.0V < $V_{OUT}$ ≤ 5.0 V | | 1200 | 1600 | |

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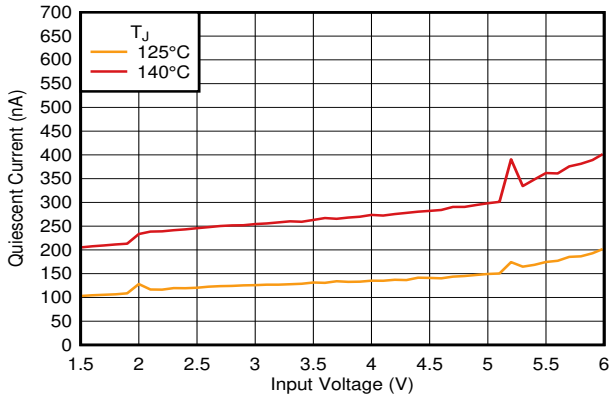
## 6.7 Typical Characteristics

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



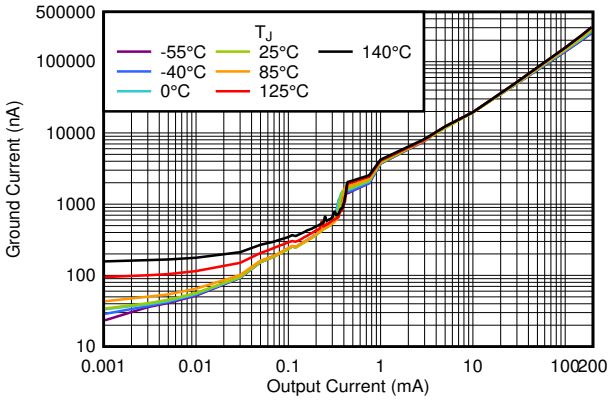

$I_{OUT}$ = 0 mA, $V_{EN}$ = $V_{IN}$

**図 6-1. $I_Q$ vs $V_{IN}$ and Temperature**



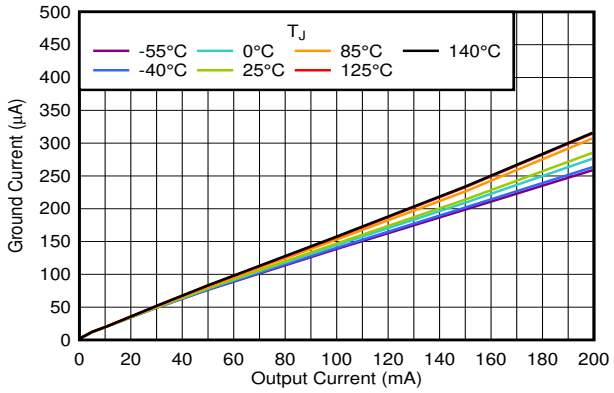

$I_{OUT}$ = 0 mA, $V_{EN}$ = $V_{IN}$

**図 6-2. $I_Q$ vs $V_{IN}$ and Temperature**



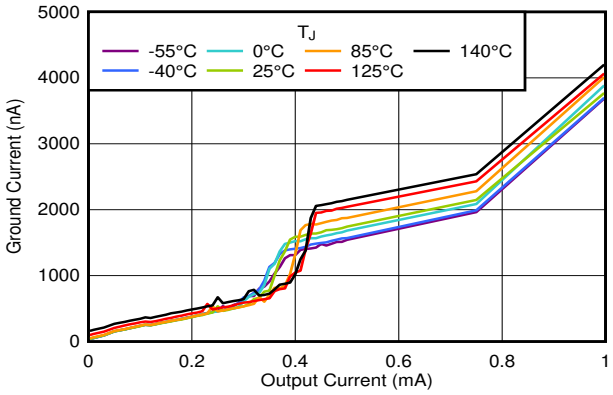

$V_{OUT}$ = 1.8 V, $V_{IN}$ = $V_{EN}$ = 2.3 V

**図 6-3. $I_Q$ vs $I_{OUT}$ and Temperature up to 200 mA**



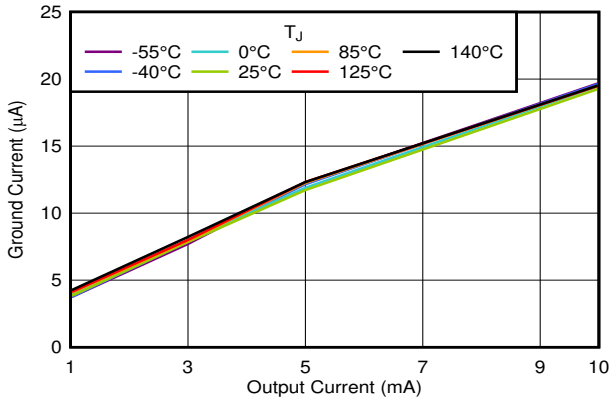

$V_{OUT}$ = 1.8 V, $V_{IN}$ = $V_{EN}$ = 2.3 V

**図 6-4. $I_Q$ vs $I_{OUT}$ and Temperature Up to 200 mA**




$V_{OUT}$ = 1.8 V, $V_{IN}$ = $V_{EN}$ = 2.3 V

**図 6-5. $I_Q$ vs $I_{OUT}$ and Temperature Up to 1 mA**



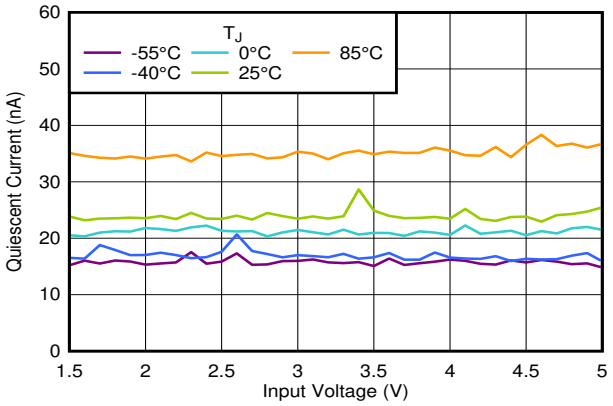

$V_{OUT}$ = 1.8 V, $V_{IN}$ = $V_{EN}$ = 2.3 V

**図 6-6. $I_Q$ vs $I_{OUT}$ and Temperature for 1 mA to 10 mA**


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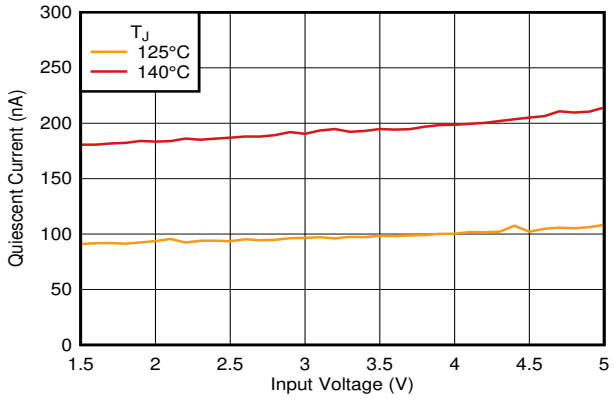
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



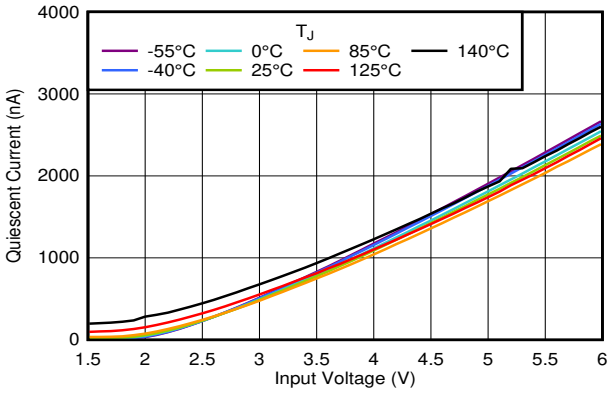

$V_{OUT}$ = 5.0 V, $V_{EN}$ = $V_{IN}$

**図 6-7. $I_Q$ in Dropout vs $V_{IN}$ and Temperature**



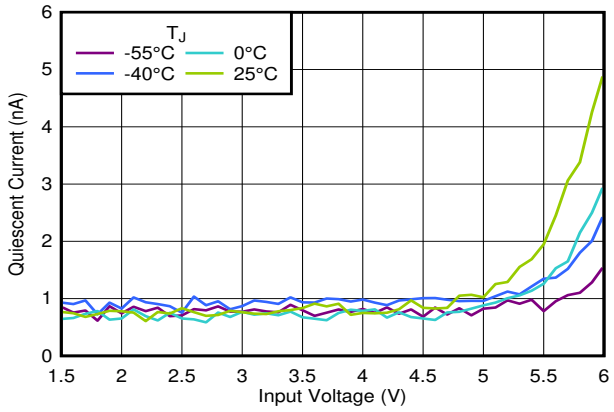

$V_{OUT}$ = 5.0 V, $V_{EN}$ = $V_{IN}$

**図 6-8. $I_Q$ in Dropout vs $V_{IN}$ and Temperature**



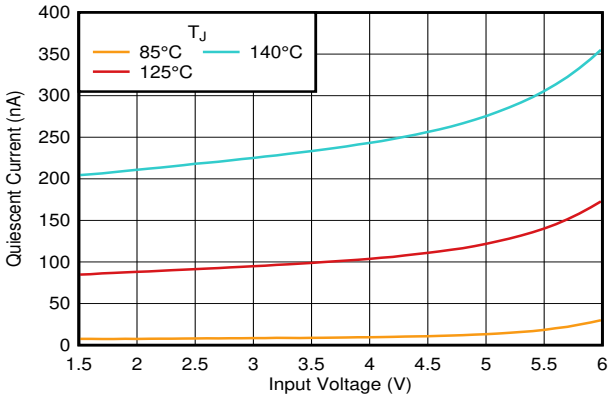

$I_{OUT}$ = 0 mA, $V_{EN}$ = 1.1 V

**図 6-9. $I_Q$ vs $V_{IN}$ and Temperature**



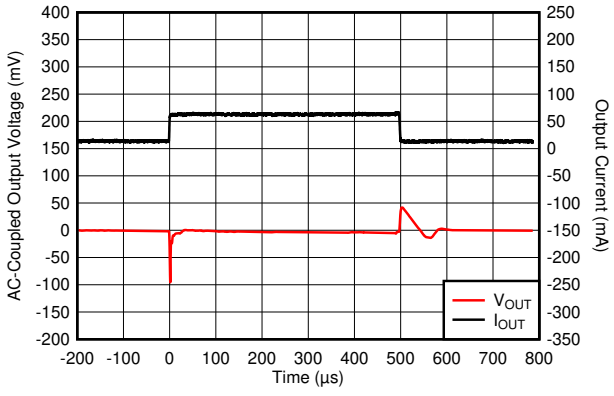

$V_{EN}$ = 0 V

**図 6-10. $I_{SHDN}$ vs $V_{IN}$ and Temperature**




$V_{EN}$ = 0 V

**図 6-11. $I_{SHDN}$ vs $V_{IN}$ and Temperature**



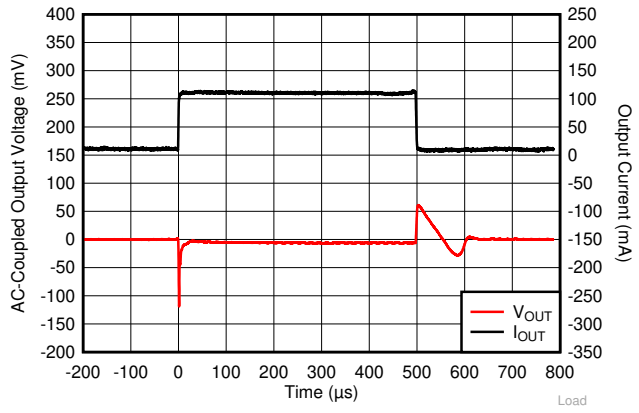

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-12. $I_{OUT}$ Transient From 1 mA to 50 mA**

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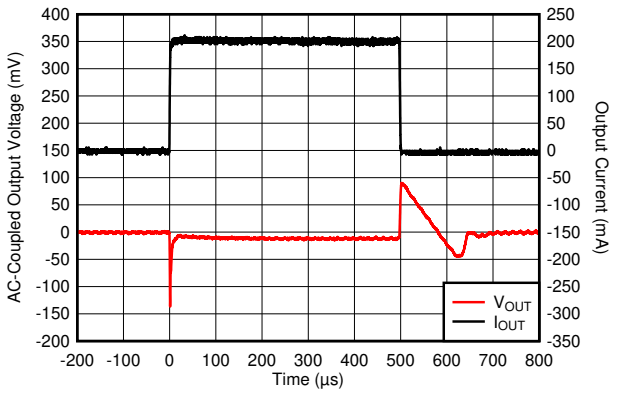
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



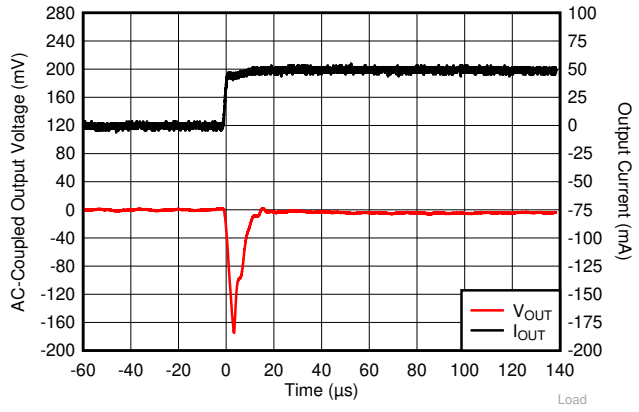

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-13. $I_{OUT}$ Transient From 1 mA to 100 mA**



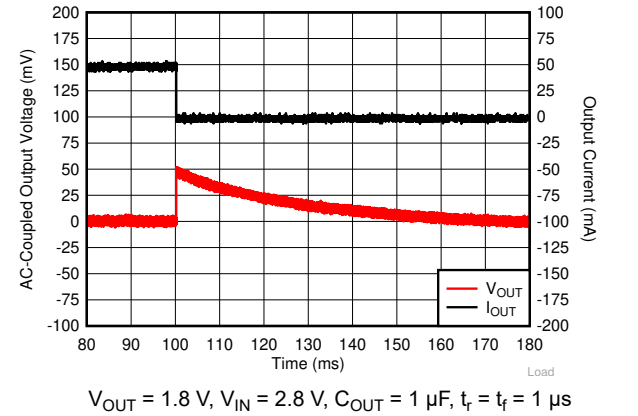

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-14. $I_{OUT}$ Transient From 1 mA to 200 mA**



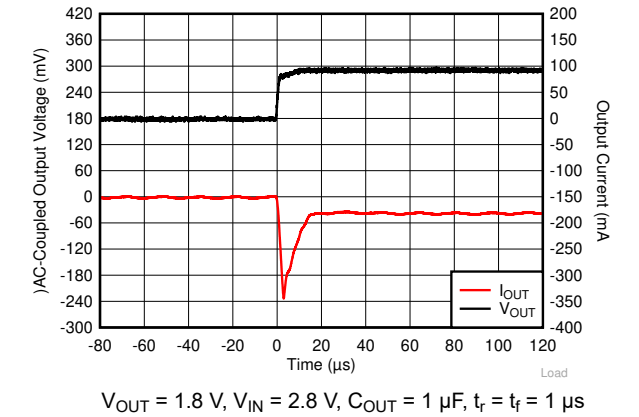

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-15. $I_{OUT}$ Transient From 0 mA to 50 mA**



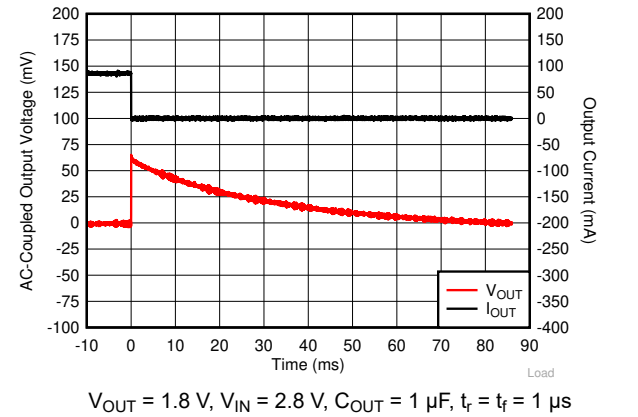

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-16. $I_{OUT}$ Transient From 50 mA to 0 mA**




$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-17. $I_{OUT}$ Transient From 0 mA to 100 mA**



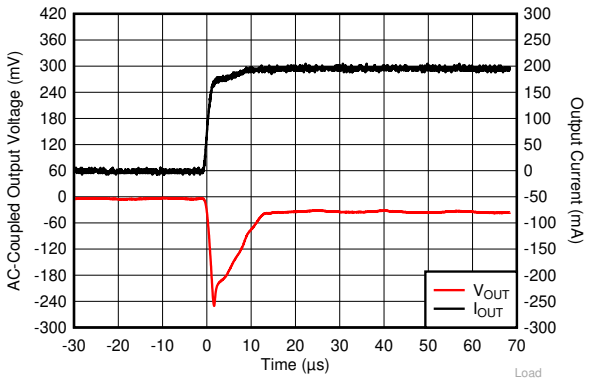

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-18. $I_{OUT}$ Transient From 100 mA to 0 mA**


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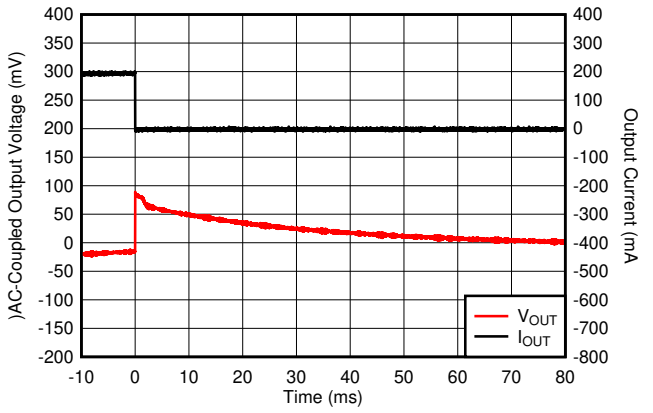
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



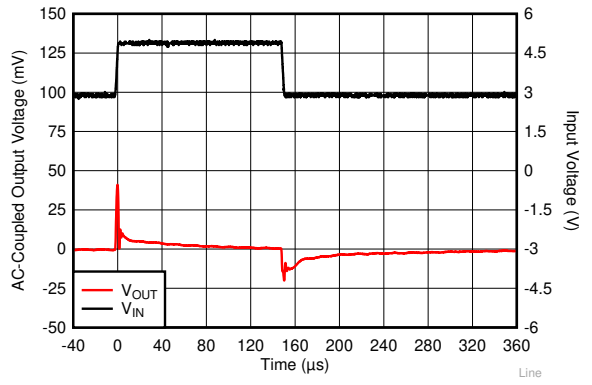

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-19. $I_{OUT}$ Transient From 0 mA to 200 mA**



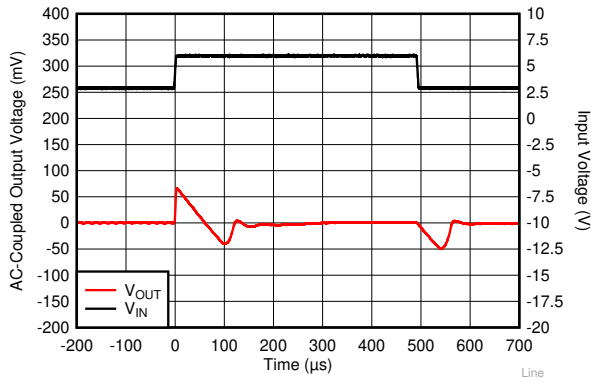

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF, $t_r$ = $t_f$ = 1 µs

**図 6-20. $I_{OUT}$ Transient From 200 mA to 0 mA**



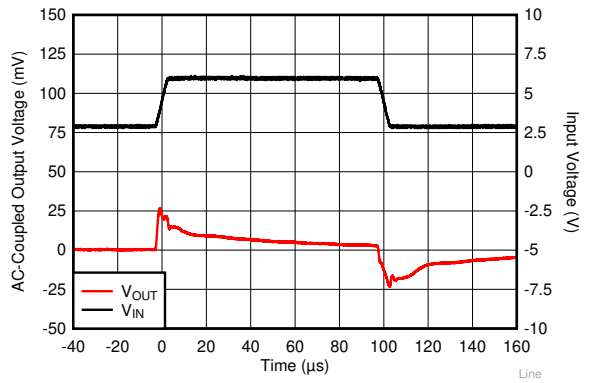

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF, slew rate = 1 V/µs

**図 6-21. $V_{IN}$ Transient From 2.8 V to 4.8 V**



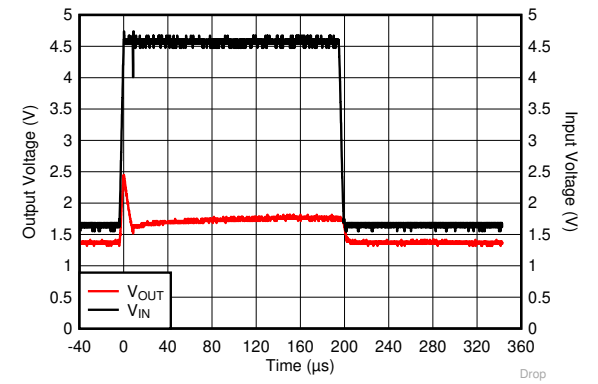

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1 µF, slew rate = 1 V/µs

**図 6-22. $V_{IN}$ Transient From 2.8 V to 6.0 V**




$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF, slew rate = 1 V/µs

**図 6-23. $V_{IN}$ Transient From 2.8 V to 6.0 V**



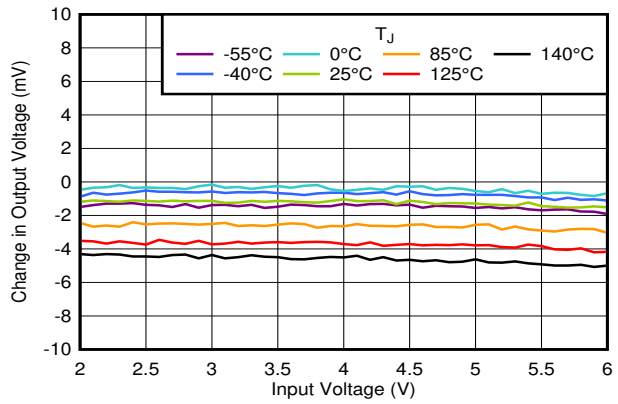

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 100 mA, $C_{OUT}$ = 1 µF, slew rate = 1 V/µs

**図 6-24. $V_{IN}$ Transient From 1.5 V to 4.5 V**

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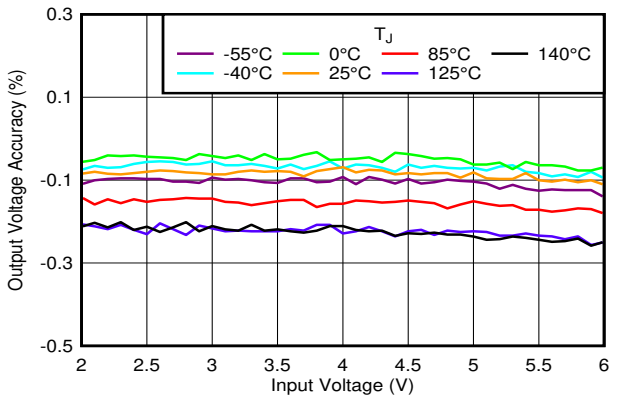
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



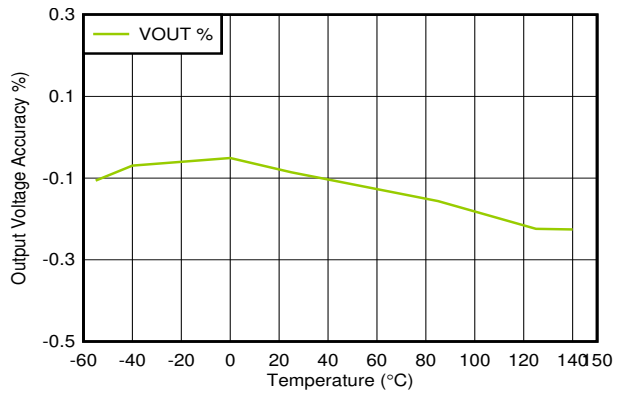

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 1 mA

**図 6-25. Line Regulation vs $V_{IN}$ and Temperature**



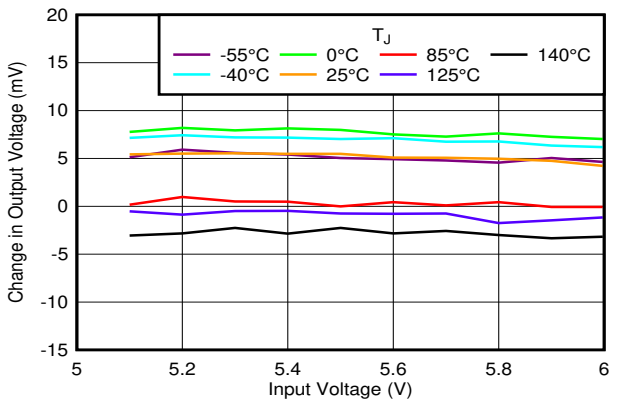

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 1 mA

**図 6-26. Output Accuracy vs $V_{IN}$ and Temperature**



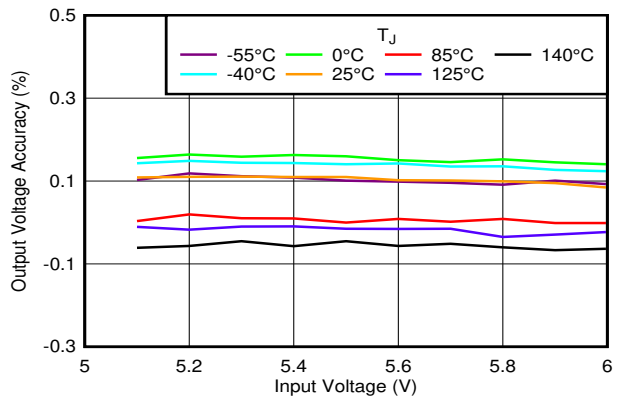

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 1 mA

**図 6-27. Output Accuracy vs Temperature**



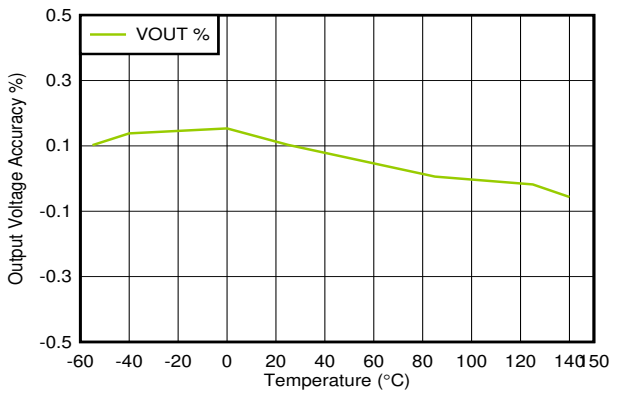

$V_{OUT}$ = 5.0 V, $I_{OUT}$ = 1 mA

**図 6-28. Line Regulation vs $V_{IN}$ and Temperature**




$V_{OUT}$ = 5.0 V, $I_{OUT}$ = 1 mA

**図 6-29. Output Accuracy vs $V_{IN}$ and Temperature**



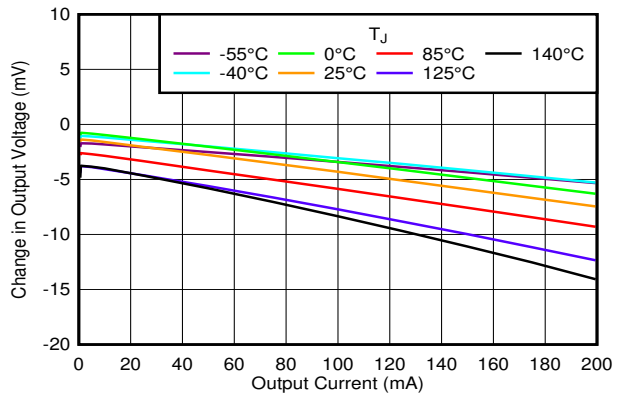

$V_{OUT}$ = 5.0 V, $I_{OUT}$ = 1 mA

**図 6-30. Output Accuracy vs Temperature**


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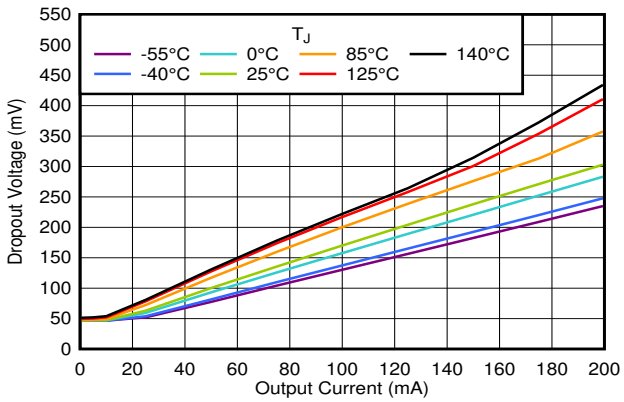
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



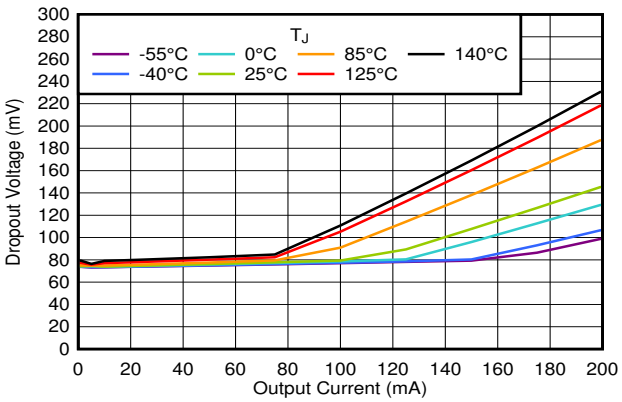

$V_{OUT}$ = 1.8 V

**図 6-31. Load Regulation vs $V_{IN}$ and Temperature**



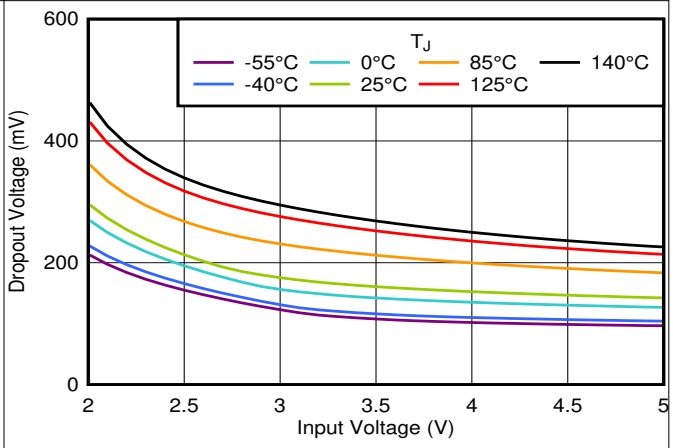

$V_{OUT}$ = 1.8 V

**図 6-32. Dropout vs $I_{OUT}$ and Temperature**



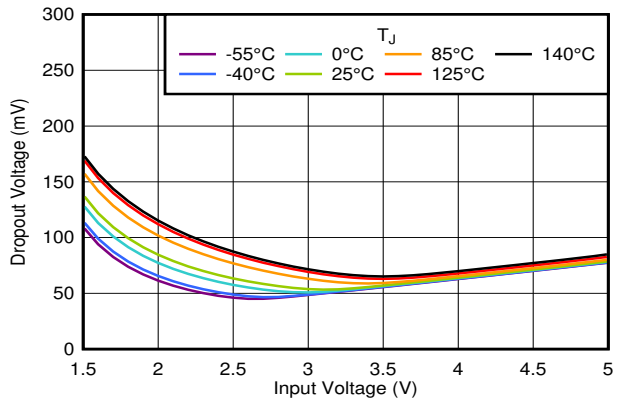

$V_{OUT}$ = 5.0 V

**図 6-33. Dropout vs $I_{OUT}$ and Temperature**



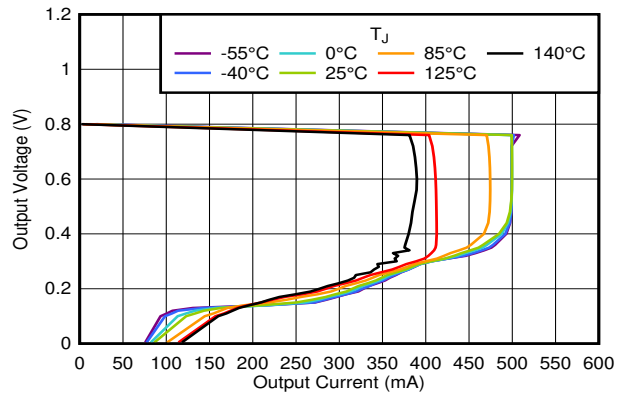

$I_{OUT}$ = 200 mA

**図 6-34. Dropout vs $V_{IN}$ and Temperature**




$I_{OUT}$ = 50 mA

**図 6-35. Dropout vs $V_{IN}$ and Temperature**



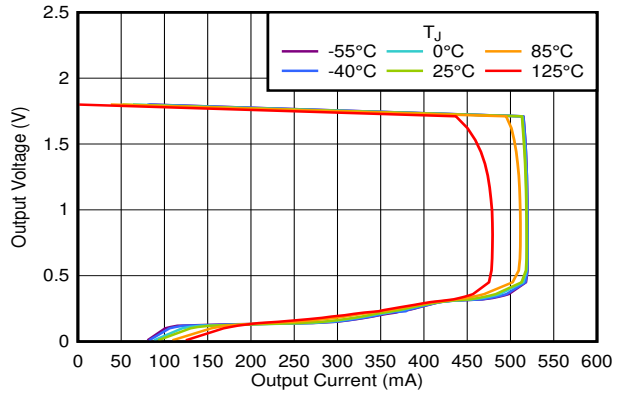

$V_{OUT}$ = 0.8 V

**図 6-36. Foldback Current Limit vs $I_{OUT}$ and Temperature**

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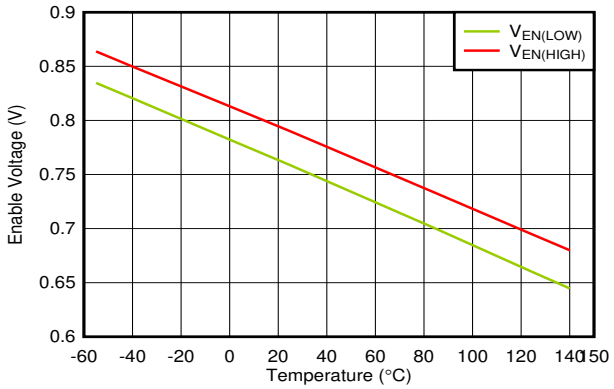
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



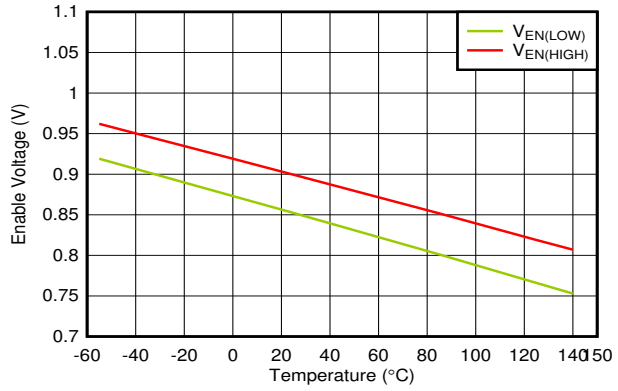

$V_{OUT}$ = 1.8 V

**図 6-37. Foldback Current Limit vs $I_{OUT}$ and Temperature**



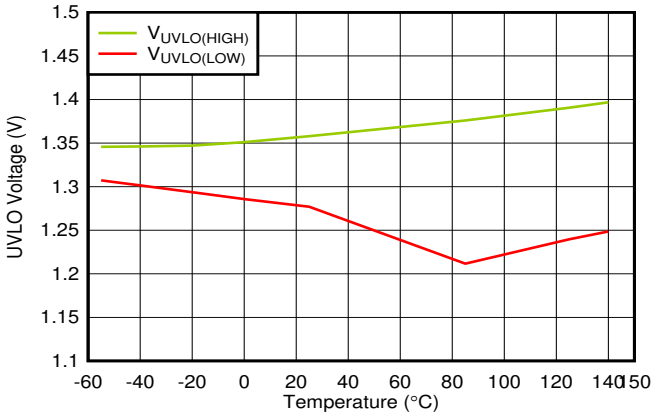

$V_{OUT}$ = 0.8 V

**図 6-38. EN High and Low Threshold vs Temperature**




$V_{OUT}$ = 5.0 V

**図 6-39. EN High and Low Threshold vs Temperature**




$V_{OUT}$ = 5.0 V, $I_{OUT}$ = 1 mA

**図 6-40. UVLO Rising and Falling Threshold vs Temperature**

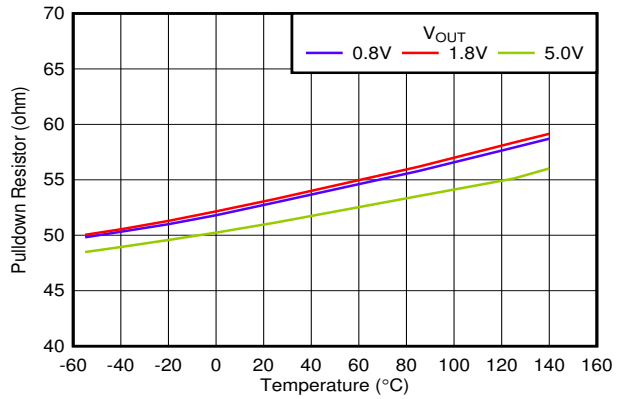



**図 6-41. Pulldown Resistor vs Temperature and $V_{OUT}$**

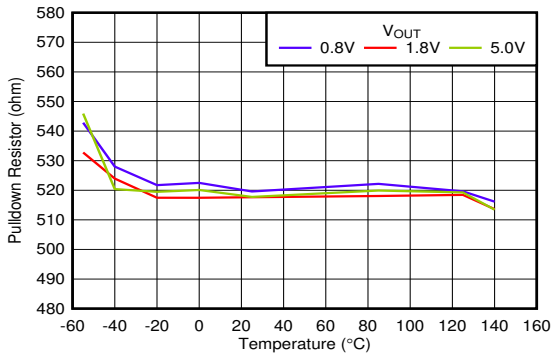
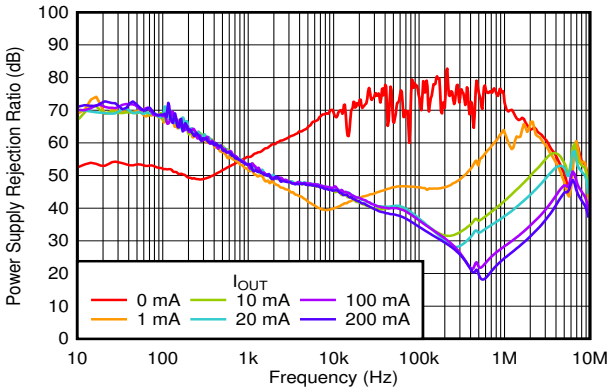



**図 6-42. Smart Enable Pulldown Resistor vs Temperature and $V_{OUT}$**


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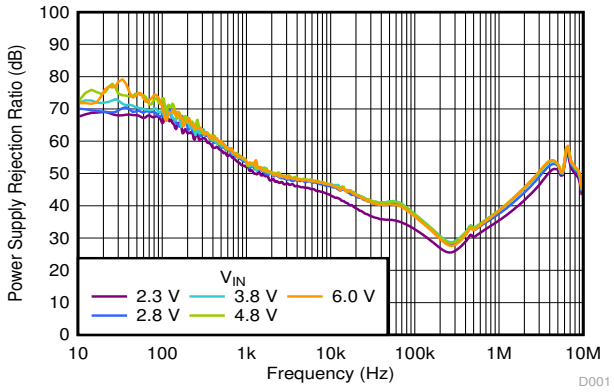
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



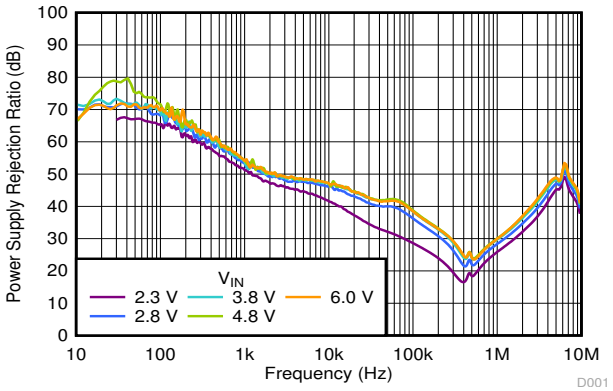

$V_{IN}$ = 2.8 V, $V_{OUT}$ = 1.8 V, $C_{OUT}$ = 1 µF

**図 6-43. PSRR vs Frequency and $I_{OUT}$**



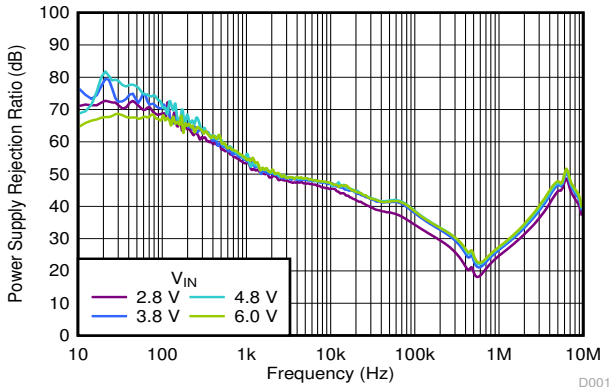

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 20 mA, $C_{OUT}$ = 1 µF

**図 6-44. PSRR vs Frequency and $V_{IN}$**



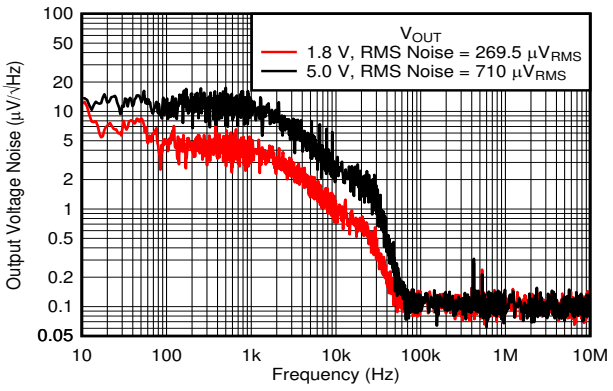

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 100 mA, $C_{OUT}$ = 1 µF

**図 6-45. PSRR vs Frequency and $V_{IN}$**



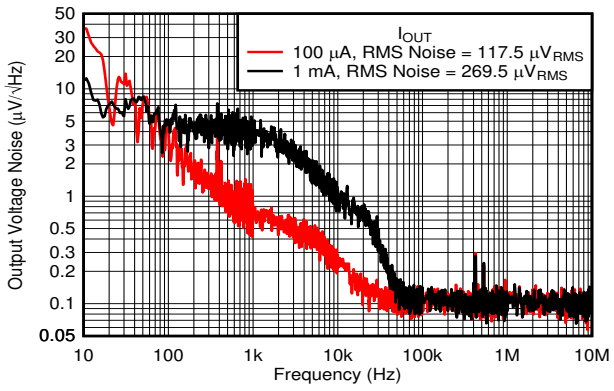

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF

**図 6-46. PSRR vs Frequency and $V_{IN}$**




$V_{IN}$ = $V_{OUT}$+ 1.0 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1 µF

**図 6-47. Output Noise vs Frequency and $V_{OUT}$**



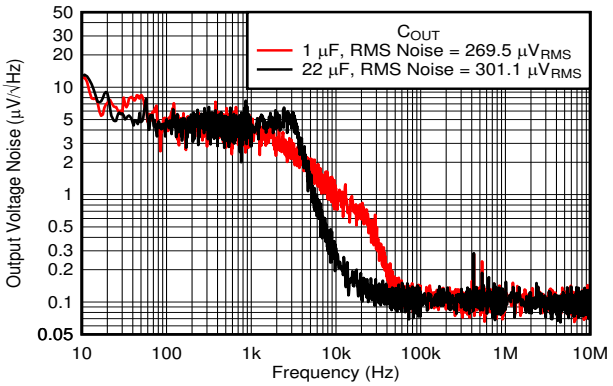

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $C_{OUT}$ = 1 µF

**図 6-48. Output Noise vs Frequency and $I_{OUT}$**

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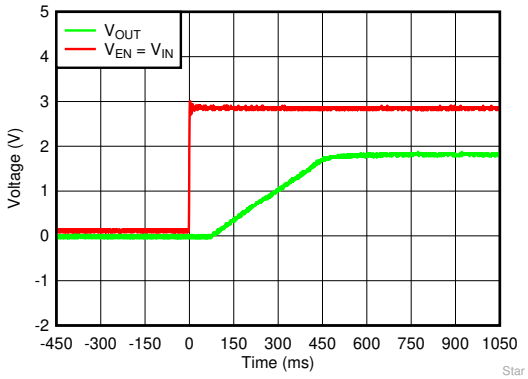
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



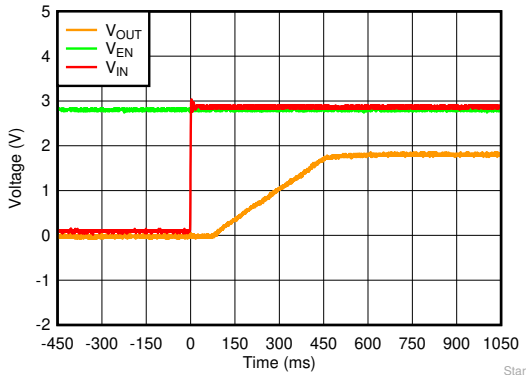

$V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $I_{OUT}$ = 1 mA

**図 6-49. Output Noise vs Frequency and $C_{OUT}$**



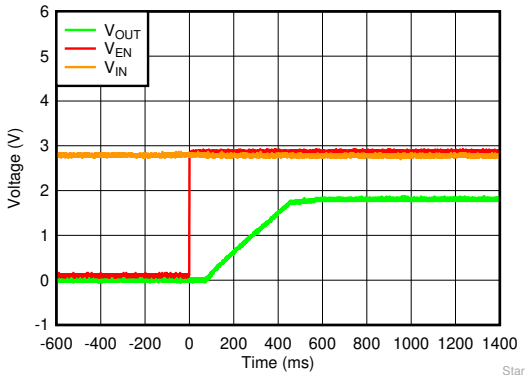

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF

**図 6-50. Startup With $V_{EN}$ = $V_{IN}$**



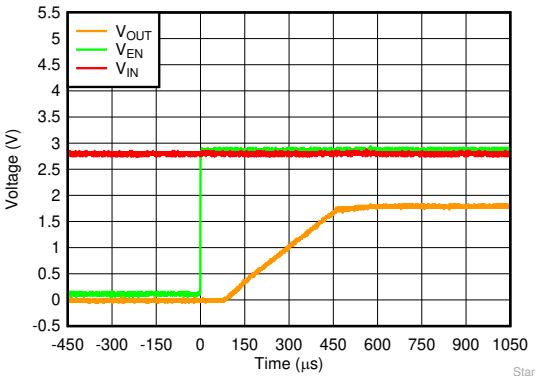

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF

**図 6-51. Startup With $V_{EN}$ Before $V_{IN}$**



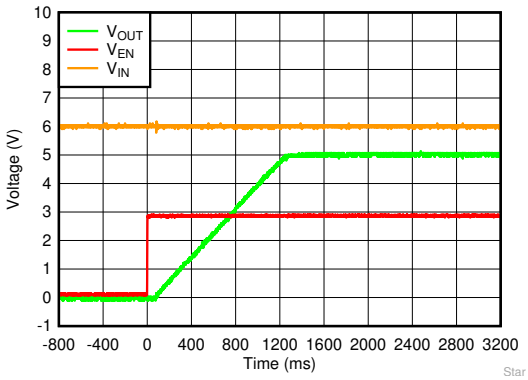

$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF

**図 6-52. Startup With $V_{EN}$ After $V_{IN}$**




$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 0 mA, $C_{OUT}$ = 1 µF

**図 6-53. Startup With $V_{EN}$ After $V_{IN}$**



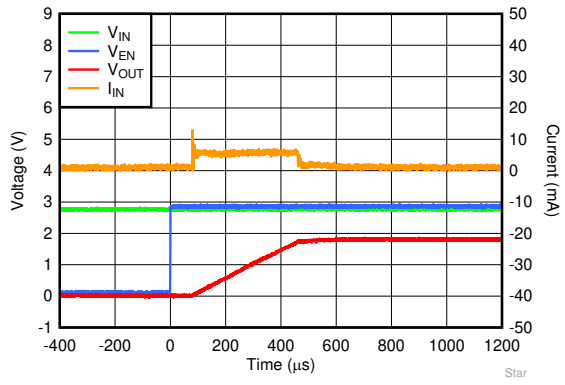

$V_{OUT}$ = 5.0 V, $I_{OUT}$ = 200 mA, $C_{OUT}$ = 1 µF

**図 6-54. Startup With $V_{EN}$ After $V_{IN}$**


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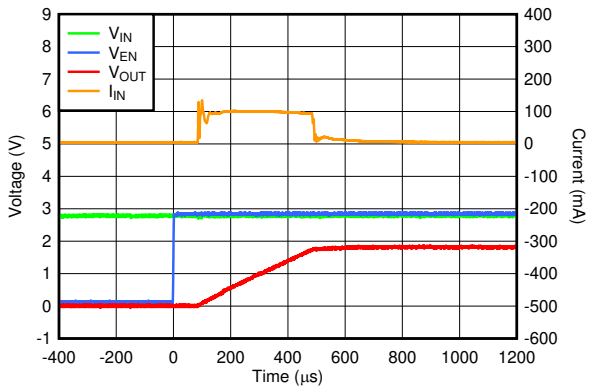
## 6.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)




$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 0 mA

**図 6-55. Startup Inrush Current With $C_{OUT}$= 1 µF**




$V_{OUT}$ = 1.8 V, $I_{OUT}$ = 0 mA

**図 6-56. Startup Inrush Current With $C_{OUT}$= 22 µF**

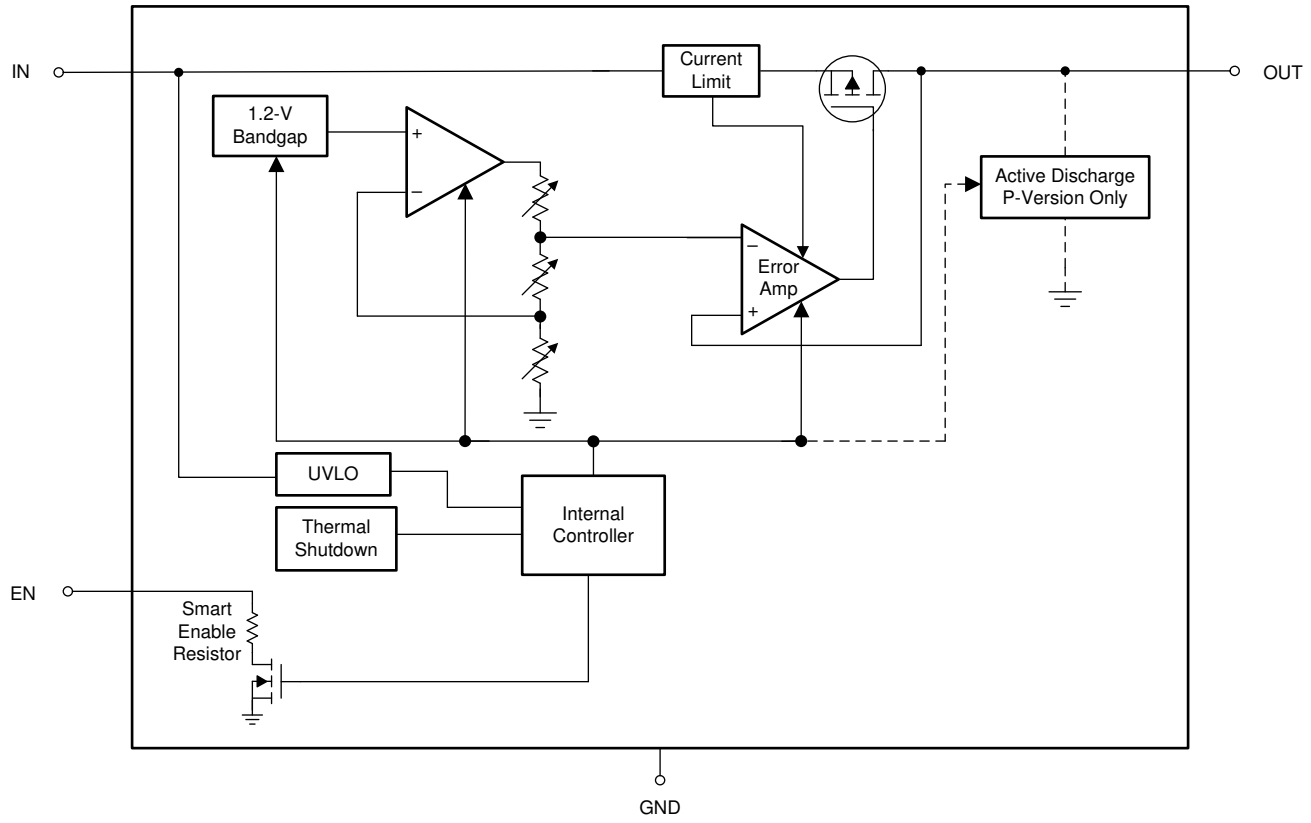
# 7 Detailed Description

## 7.1 Overview

The TPS7A02 is a ultra-low $I_Q$ linear voltage regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications.

This low-dropout linear regulator (LDO) offers active discharge, foldback current limit, shutdown, and thermal protection capability.

## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 Excellent Transient Response

The TPS7A02 includes several innovative circuits to ensure excellent transient response. Dynamic biasing increases the $I_Q$ for a short duration during transients to extend the closed-loop bandwidth and improve the output response time to transients.

Adaptive biasing increases the $I_Q$ as the DC load current increases, extending the bandwidth of the loop. The response time across the output voltage range is constant because a buffered reference topology is used, which keeps the control loop in unity gain at any output voltage.

These features give the device a wide loop bandwidth during transients that ensures excellent transient response while maintaining low $I_Q$ in steady-state conditions.

### 7.3.2 Active Discharge (P-Version Only)

The device has an internal pulldown MOSFET that connects a $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin or by the undervoltage lockout (UVLO).

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

### 7.3.3 Low $I_Q$ in Dropout

In most LDOs the $I_Q$ significantly increases when the device is placed into dropout, which is especially true for low $I_Q$ LDOs. The TPS7A02 helps to reduce the battery discharge by detecting when the device is operating in dropout conditions and maintaining a low $I_Q$.

### 7.3.4 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

### 7.3.5 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

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### 7.3.6 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.5 V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

図 7-1 shows a diagram of the foldback current limit.

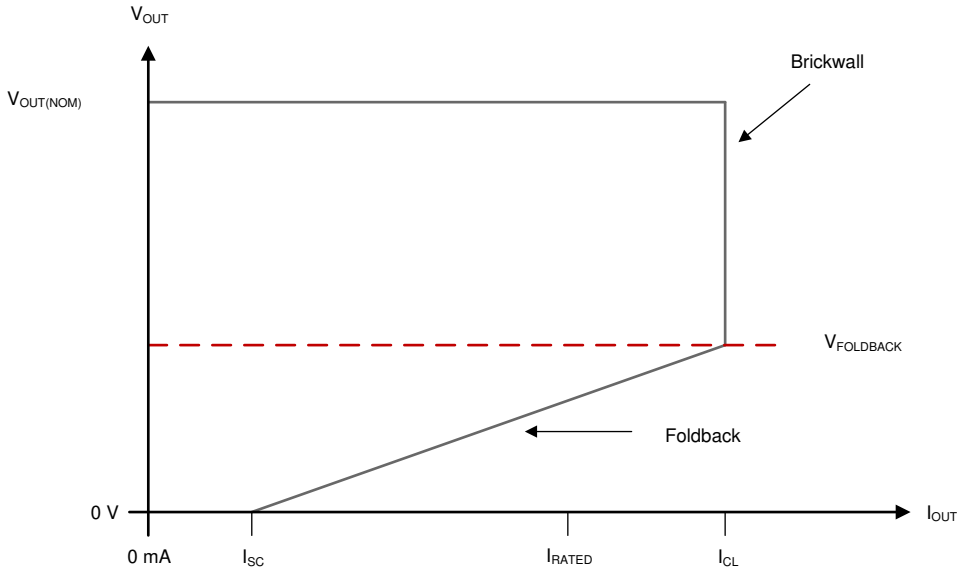



**図 7-1. Foldback Current Limit**

### 7.3.7 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 7.3.8 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).


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The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**表 7-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.


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# 8 Application and Implementation

注

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## 8.1 Application Information

### 8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### 8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

### 8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 図 8-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

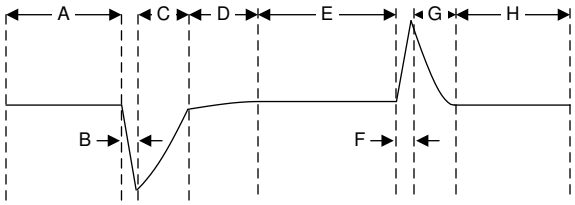



**図 8-1. Load Transient Waveform**

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

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During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

### 8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before the input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. 図 8-2 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

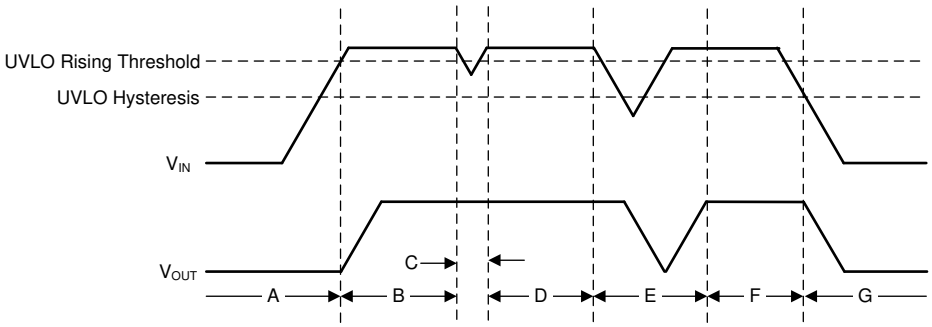



**図 8-2. Typical UVLO Operation**

### 8.1.5 Power Dissipation ($P_D$)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 2 to approximate $P_D$:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A02 allows for maximum efficiency across a wide range of output voltages.


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The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. According to 式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$). 式 4 rearranges 式 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

#### 8.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are used in accordance with 式 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- $P_D$ is the power dissipated as explained in 式 2
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

#### 8.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 図 8-3 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 式 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

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図 8-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

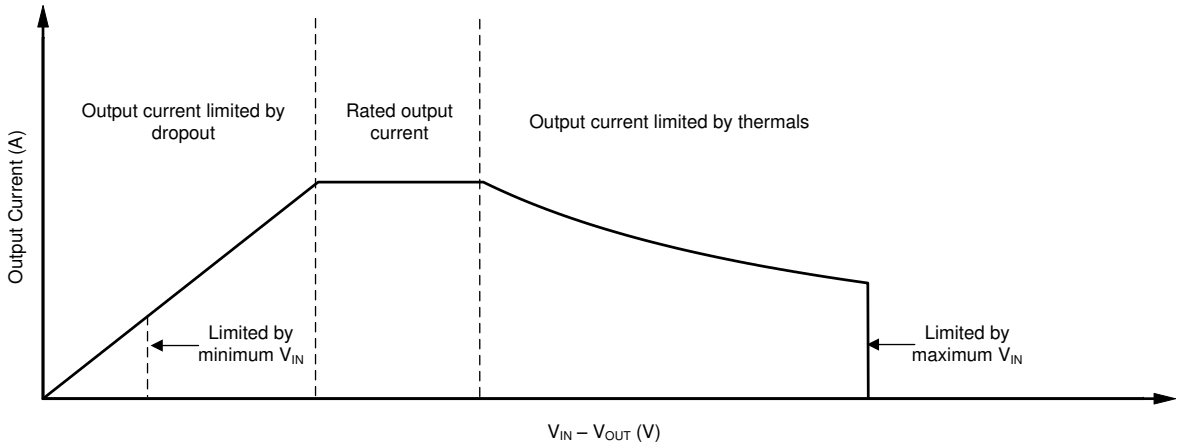



**図 8-3. Region Description of Continuous Operation Regime**

## 8.2 Typical Application

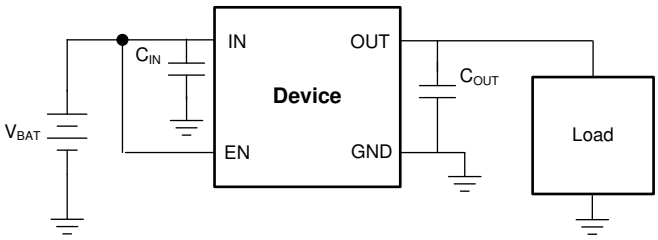



**図 8-4. Operation From a Battery Input Supply**

### 8.2.1 Design Requirements

**表 8-1. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 1.8 V to 3.0 V (two 1.5-V batteries) |
| Output voltage | 1.0 V, ±1% |
| Input current | 200 mA, maximum |
| Output load | 10-mA DC |
| Maximum ambient temperature | 70°C |

### 8.2.2 Detailed Design Procedure

For this design example, the 1.0-V, fixed-version TPS7A0210 is selected. A dual AA Alkaline battery was used, thus a 1.0-µF input capacitor is recommended to minimize transient currents drawn from the battery. A 1.0-µF output capacitor is also recommended for excellent load transient response. The dropout voltage ($V_{DO}$) is kept within the TPS7A02 dropout voltage specification for the 1.0-V output voltage option to keep the device in regulation under all load and temperature conditions for this design. Use the recommend 1-µF input and output capacitor because the input source has a high equivalent series resistor (ESR) of 600 mΩ (typ). The very small ground current consumed by the regulator maintains a high current efficiency as compared to the load current consumed by the system, as shown in 図 8-5 which allows for long battery life. 式 6 can be used to calculate the current efficiency ($I_\eta$) of this system.

$$I_\eta(\%) = I_{OUT} / (I_{OUT} + I_Q) \times 100 \quad (6)$$


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### 8.2.3 Application Curve

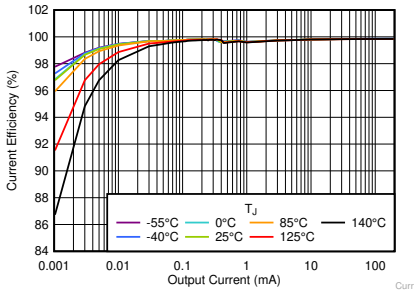



**図 8-5. Current Efficiency vs $I_{OUT}$ and Temperature**

## 8.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.5 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V. TI highly recommends using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

### 8.4.2 Layout Examples

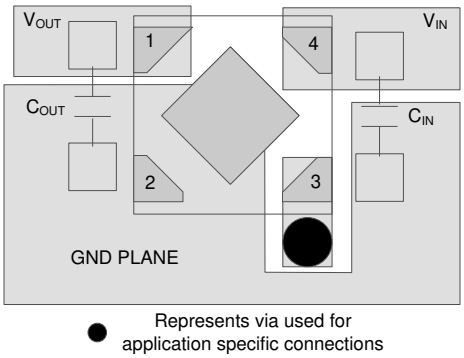



**図 8-6. Layout Example for the DQN Package**

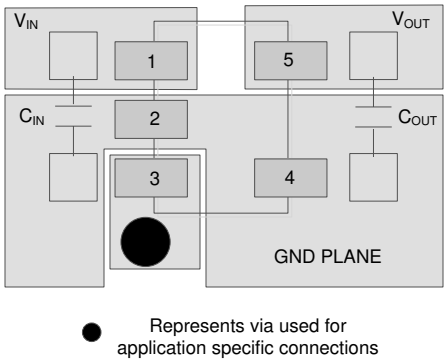



**図 8-7. Layout Example for the DBV Package**

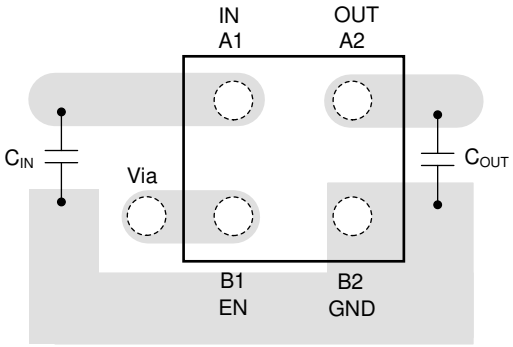



**図 8-8. Layout Example for the YCH Package**


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# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Device Nomenclature

**表 9-1. Device Nomenclature(1) (2)**

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS7A02 **xx(x)Pyyyz** | **XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V).<br>**P** indicates an active output discharge feature. All members of the TPS7A02 family actively discharge the output when the device is disabled.<br>**YYY** is the package designator.<br>**Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A0210PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GH |
| TPS7A0210PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GH |
| TPS7A0212PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21GF |
| TPS7A0212PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21GF |
| TPS7A0212PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | A |
| TPS7A0212PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | A |
| TPS7A0215DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OS |
| TPS7A0215DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OS |
| TPS7A0215PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21KF |
| TPS7A0215PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21KF |
| TPS7A0215PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F3 |
| TPS7A0215PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F3 |
| TPS7A02175PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | S |
| TPS7A02175PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | S |
| TPS7A02185DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OR |
| TPS7A02185DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OR |
| TPS7A02185PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HO |
| TPS7A02185PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HO |
| TPS7A0218DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 2CDT |
| TPS7A0218DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 2CDT |
| TPS7A0218PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21LF |
| TPS7A0218PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21LF |
| TPS7A0218PDBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21LF |
| TPS7A0218PDBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21LF |
| TPS7A0218PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F4 |
| TPS7A0218PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F4 |
| TPS7A0218PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | B |
| TPS7A0218PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | B |
| TPS7A0220PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 22MT |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A0220PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 22MT |
| TPS7A0220PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F5 |
| TPS7A0220PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F5 |
| TPS7A0222DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IN |
| TPS7A0222DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IN |
| TPS7A0222PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21HF |
| TPS7A0222PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21HF |
| TPS7A0222PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GI |
| TPS7A0222PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GI |
| TPS7A0223PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21IF |
| TPS7A0223PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21IF |
| TPS7A0223PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F6 |
| TPS7A0223PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F6 |
| TPS7A0225PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21DF |
| TPS7A0225PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21DF |
| TPS7A0225PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F7 |
| TPS7A0225PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F7 |
| TPS7A0225PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | C |
| TPS7A0225PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | C |
| TPS7A0228DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 29PT |
| TPS7A0228DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 29PT |
| TPS7A0228DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IE |
| TPS7A0228DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IE |
| TPS7A0228PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21EF |
| TPS7A0228PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21EF |
| TPS7A0228PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F8 |
| TPS7A0228PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F8 |
| TPS7A0228PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | D |
| TPS7A0228PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | D |
| TPS7A0230PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21MF |
| TPS7A0230PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21MF |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A0230PDBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21MF |
| TPS7A0230PDBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21MF |
| TPS7A0230PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | F9 |
| TPS7A0230PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | F9 |
| TPS7A0230PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | F |
| TPS7A0230PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | F |
| TPS7A0231PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GJ |
| TPS7A0231PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GJ |
| TPS7A0233DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 29QT |
| TPS7A0233DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 29QT |
| TPS7A0233DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IF |
| TPS7A0233DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IF |
| TPS7A0233PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21FF |
| TPS7A0233PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21FF |
| TPS7A0233PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FA |
| TPS7A0233PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | FA |
| TPS7A0233PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | G |
| TPS7A0233PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | G |
| TPS7A0236PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (21FF, 21JF) |
| TPS7A0236PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (21FF, 21JF) |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

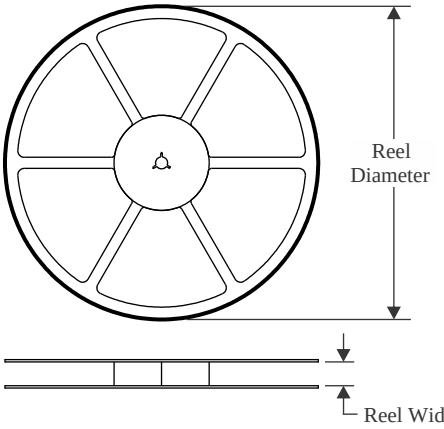
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

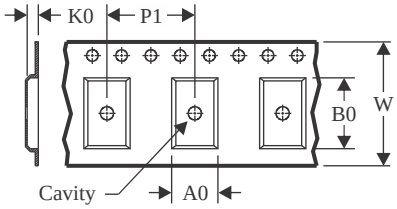
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

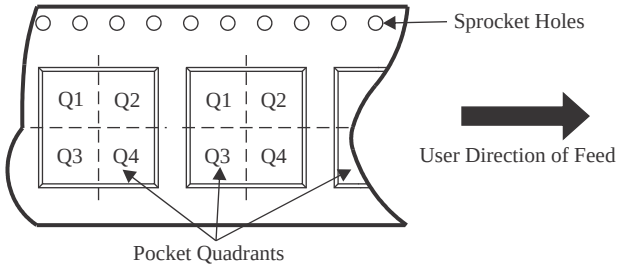



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

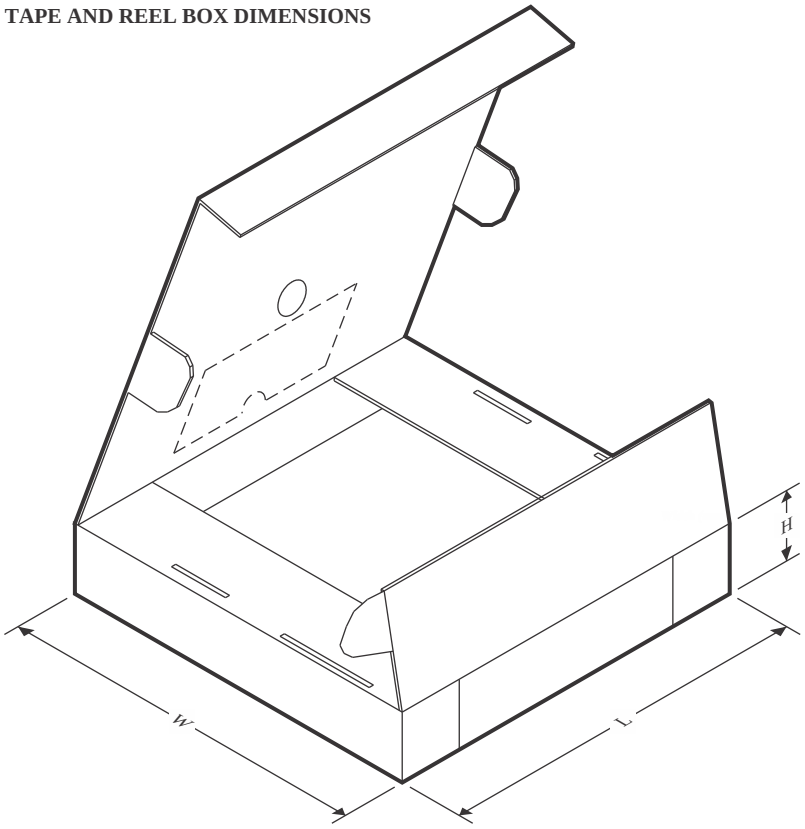



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A0210PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0212PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0212PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0212PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0215DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0215PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0215PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A02175PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A02185DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A02185PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A02185PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A02185PDQNR | X2SON | DQN | 4 | 3000 | 178.0 | 8.4 | 1.13 | 1.13 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS7A0218DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0218PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0218PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0218PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A0218PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0218PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0220PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0220PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0220PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0222DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0222PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0222PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0223PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0223PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0225PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0225PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0225PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0225PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0225PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0228DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0228DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0228DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0228PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0228PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0228PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0230PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0230PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0230PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0230PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0231PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0233DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0233DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0233PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0233PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0233PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0233PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0233PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0236PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A0210PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0212PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0212PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0212PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0215DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0215PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0215PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A02175PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A02185DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A02185PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A02185PDQNR | X2SON | DQN | 4 | 3000 | 184.0 | 184.0 | 19.0 |
| TPS7A02185PDQNR | X2SON | DQN | 4 | 3000 | 205.0 | 200.0 | 33.0 |
| TPS7A0218DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0218PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0218PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0218PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0218PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0218PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A0220PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0220PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0220PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0222DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0222PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0222PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0223PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0223PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0225PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0225PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0225PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0225PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0225PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0228DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0228DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0228DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0228PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0228PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0228PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0230PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0230PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0230PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0230PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0231PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0233DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0233DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0233PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0233PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0233PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0233PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0233PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0236PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

## DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

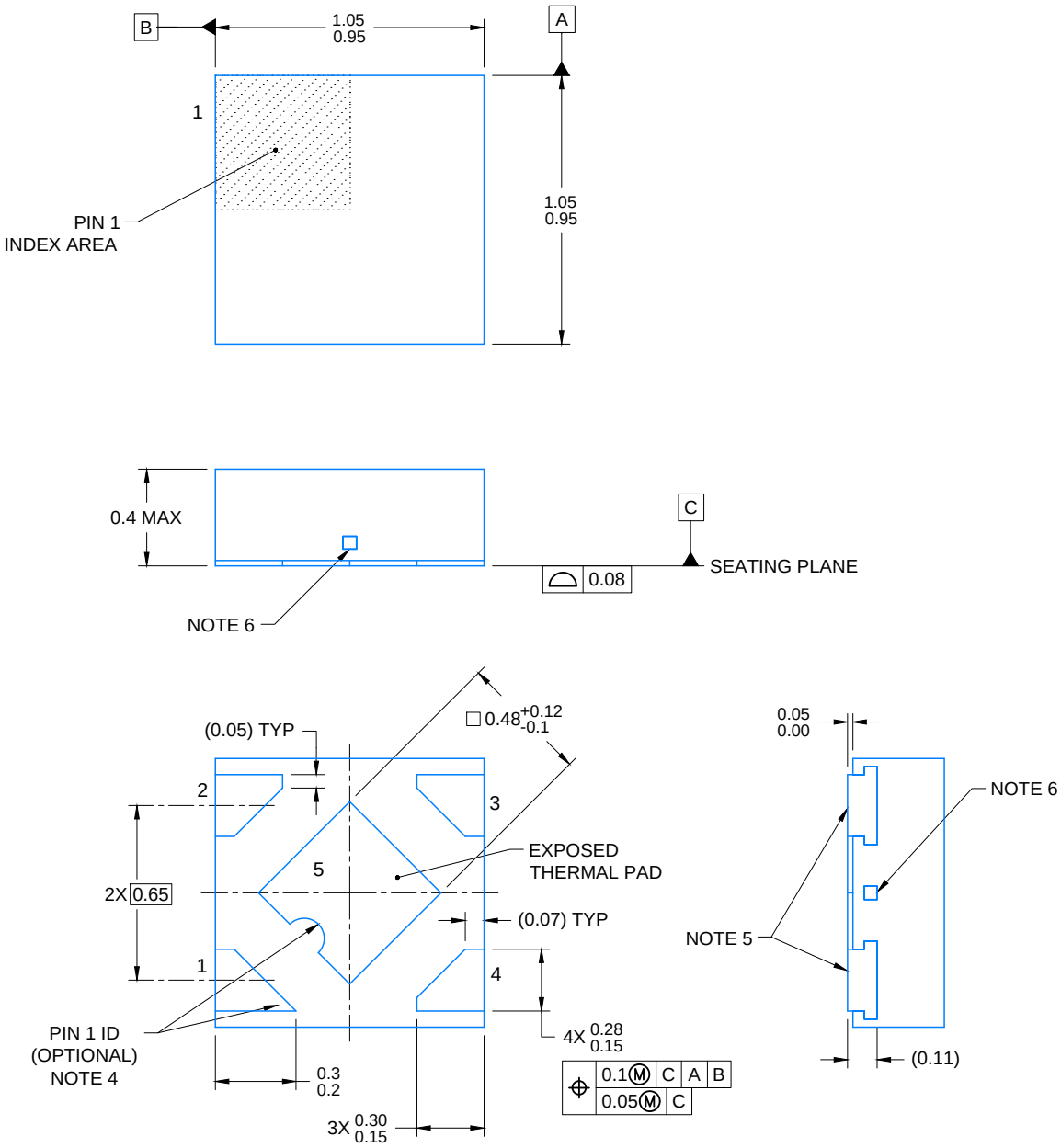
4210367/F

# PACKAGE OUTLINE

## DQN0004A

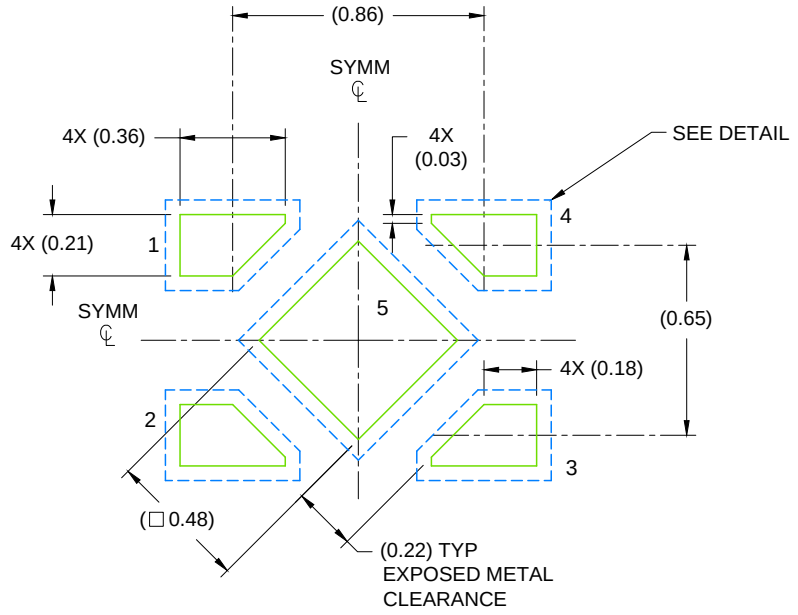
## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



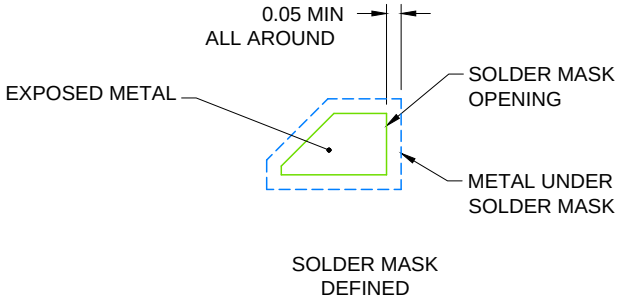

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.




LAND PATTERN EXAMPLE

SCALE: 40X

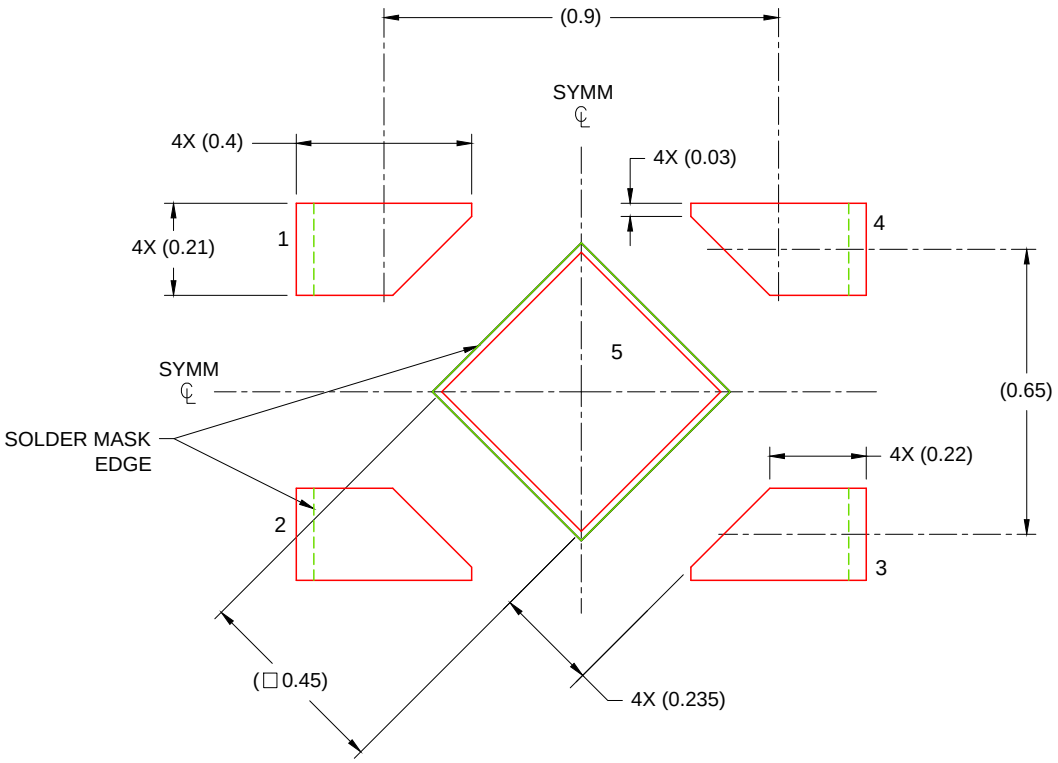



SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

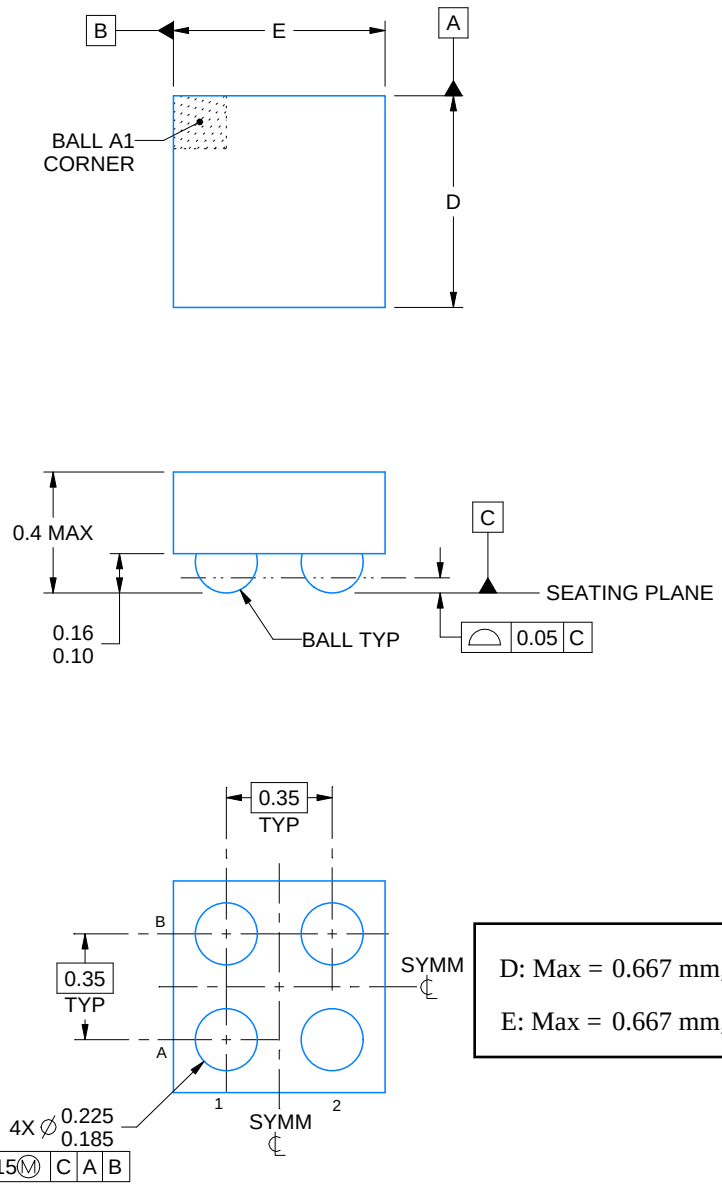
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# YCH0004

# PACKAGE OUTLINE

## DSBGA - 0.4 mm max height

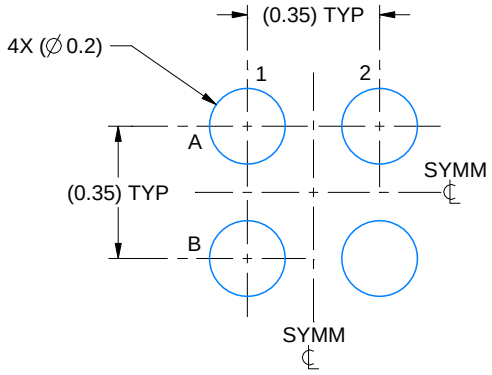
DIE SIZE BALL GRID ARRAY



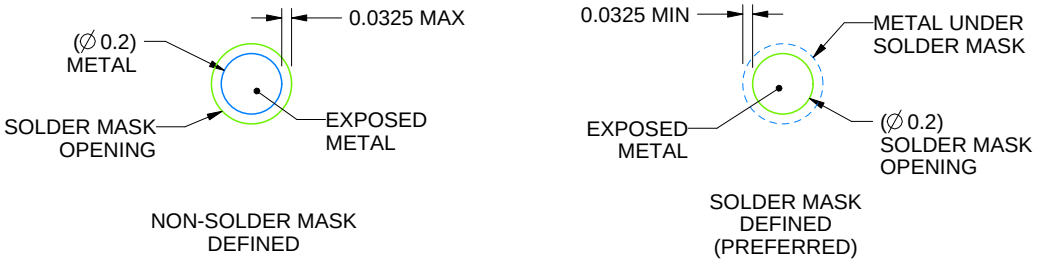

4224061/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

4224061/A 12/2017

NOTES: (continued)

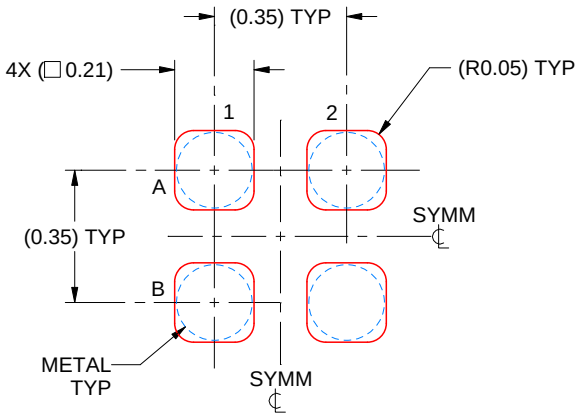
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YCH0004

## DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4224061/A 12/2017

NOTES: (continued)

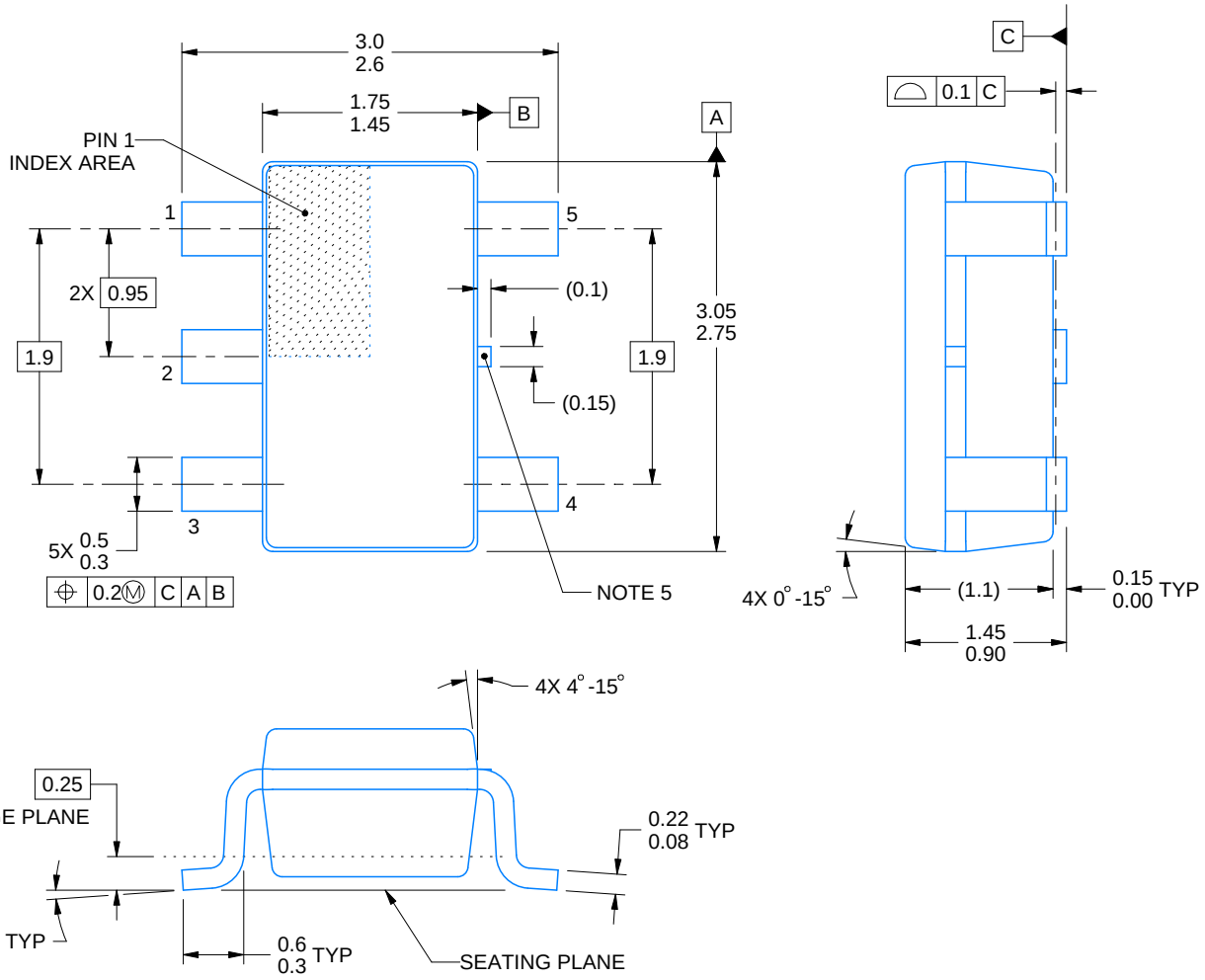
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

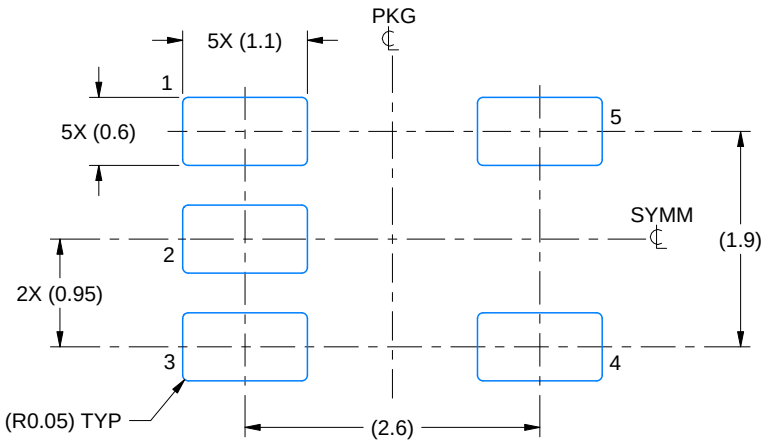
SMALL OUTLINE TRANSISTOR



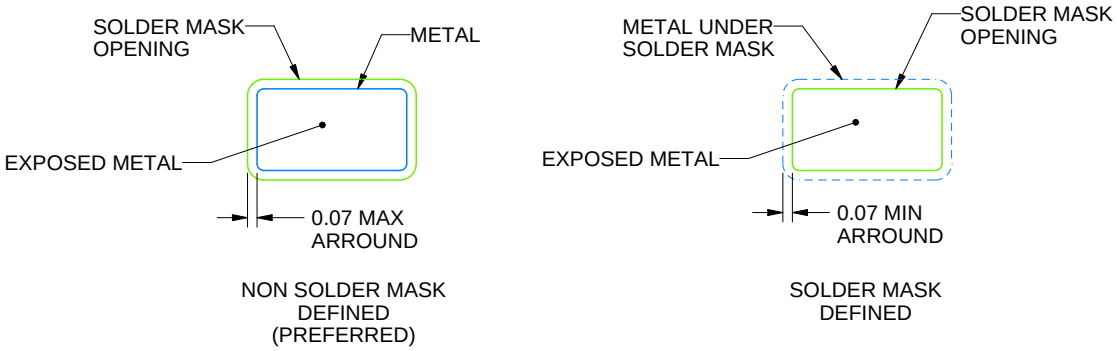

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

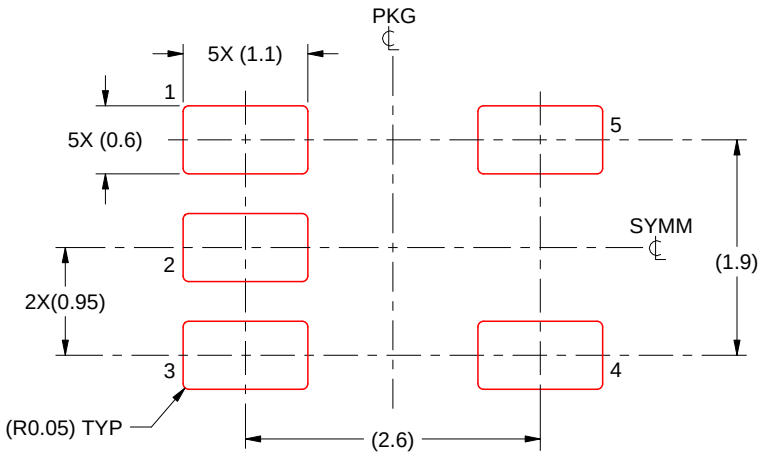



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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