TPS7A21 500mA、低ノイズ、低 I_Q、高 PSRR LDO

1 特長

- 超低 I_Q:6.5μA
- 入力電圧範囲:2.0V～6.0V
- 出力電圧範囲:0.8V～5.5V (50mV 刻み)
- 高 PSRR:1kHz 時に 91dB
- 低い出力電圧ノイズ:7.7μV_{RMS}
- 低いドロップアウト:
  – 500mA 出力時に 175mV (最大値) (2.5V の V_{OUT} の場合)
- スマート EN プルダウン
- 出力電圧許容誤差:
  – ±1.5% (ライン、負荷、温度)
- 幅広いセラミック・コンデンサをサポート:
  – 1μF～200μF
- 動作時接合部温度:–40℃～+125℃
- パッケージ:
  – 0.602mm × 0.602mm パワー DSBGA

2 アプリケーション

- 携帯電話およびタブレット
- ウェアラブル
- IP カメラ
- 携帯医療機器
- スマート・メータとフィールド・トランスミッタ
- RF、PLL、VCO、およびクロック電源
- モーター・ドライブ

3 概要

TPS7A21 は、500mA の出力電流を供給できる超小型の低ドロップアウト (LDO) リニア・レギュレータです。このデバイスは、低ノイズ、高 PSRR、および非常に優れた負荷およびライン過渡応答を特長とし、RF やその他の外部からの影響を受けやすいアナログ回路の要件に対応できます。革新的な設計手法により、外部ノイズ・バイパス・コンデンサを追加しなくても低ノイズ性能を実現します。低静止電流の TPS7A21 は、バッテリ駆動のシステムに最適な選択肢です。2.0V～6.0V の入力電圧範囲と、0.8V～5.5V の出力電圧範囲は、さまざまなシステム要件に対応しています。内部の高精度リファレンス電圧回路により、非常に優れた精度が得られます。負荷、ライン、温度の変化に対する最大出力電圧許容誤差は 1.5% です。

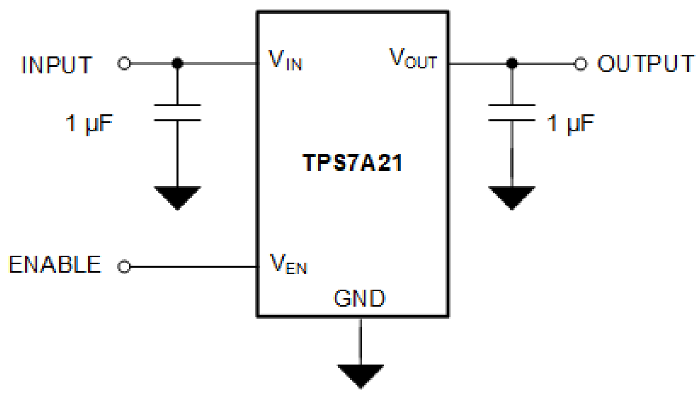
内部のソフトスタート回路により突入電流を制御できるため、スタート・アップ時の入力電圧降下を最小限に抑えることができます。LDO は小さなセラミック・コンデンサでも安定して動作するため、ソリューション全体を小型化できます。

内部制御のプルダウン抵抗を持つスマート・イネーブル入力回路により、EN ピンが接続されていない場合でも LDO をディセーブル状態に維持するため、EN 入力をプルダウンするのに必要な外付け部品を不要にできます。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS7A21	YWD (DSBGA、4)	0.602mm × 0.602mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2021) to Revision A (September 2022) **Page**

- 「特長」セクションの「出力電圧許容範囲」の箇条書き項目にライン、負荷、温度を追加 1
- 「特長」セクションの「幅広いセラミック・コンデンサをサポート」の箇条書き項目を変更 1
- 「アプリケーション」セクションを変更 1
- Changed description of OUT pin in *Pin Functions: DSBGA* table 3
- Changed typical short-circuit current limit from 300 mA to 325 mA 5
- Changed typical value of smart enable pulldown resistor from 450 kΩ to 440 kΩ 5
- Changed *Output Voltage Accuracy vs* I_{OUT} and I_Q *vs* V_{IN} figures in *Typical Characteristics* section 7
- Deleted second I_{GND} *vs* I_{OUT} figure from *Typical Characteristics* section 7
- Added discussion regarding sources with limited current drive capability to *Smart Enable (EN)* section 15
- Added discussion that input voltage must be high enough to enable the active discharge to *Active Discharge* section 15
- Added last sentence to *Dropout Operation* section 17
- Changed *Input voltage* and *Output current* parameters in *Design Parameters* table 21
- Changed *Detailed Design Procedure* section 22
- Added *Device Nomenclature* section 25

5 Pin Configuration and Functions

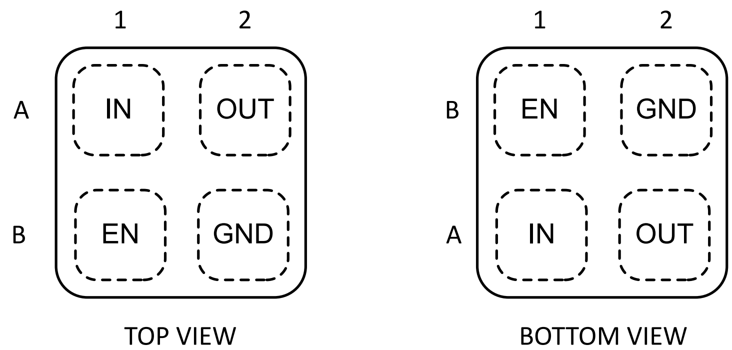


図 5-1. YWD Package, 4-Pin DSBGA

表 5-1. Pin Functions: DSBGA

PIN		I/O	DESCRIPTION
DSBGA	NAME		
A1	IN	I	Input voltage supply. For best transient response and to minimize input impedance, use the recommended value or larger capacitor from IN to GND, as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
A2	OUT	O	Regulated output voltage. Connect a low-equivalent series resistance (ESR) capacitor to this pin. For best transient response, use the nominal recommended value or larger capacitor from OUT to GND. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on OUT when the regulator is in shutdown mode (V_{EN}< $V_{EN(LOW)}$).
B1	EN	I	Enable input. A low voltage (V_{EN} < $V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 150-Ω pulldown resistor. A high voltage (V_{EN} > $V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 450-kΩ pulldown resistor to hold the regulator off by default. When V_{EN} > $V_{EN(HI)}$, the 450-kΩ pulldown resistor is disconnected to reduce input current.
B2	GND	—	Common ground.

6 Specifications

6.1 Absolute Maximum Ratings

ratings apply over operating free-air temperature range (unless otherwise noted)[(1) (3)]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6.5	V
V_{OUT}	Output voltage	–0.3	See[(2)]	V
V_{EN}	Enable input voltage	–0.3	6.5	V
	Maximum output current[(4)]	Internally limited		A
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Absolute maximum V_{OUT} is the lesser of V_{IN} + 0.3 V, or 6.5 V.
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry helps protect the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

conditions apply over the operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.0		6.0	V
V_{EN}	Enable input voltage	0		6.0	V
V_{OUT}	Nominal output voltage range	0.8		5.5	V
I_{OUT}	Output current	0		500	mA
C_{IN}	Input capacitor[(2)]		1		µF
C_{OUT}	Output capacitor[(3)]	1		200	µF
ESR	Output capacitor effective series resistance			100	mΩ
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to the GND pin.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.
(3) Effective output capacitance of 0.4 µF minimum and 200 µF maximum over all temperature and voltage conditions is required for stability with ESR values as high as 100 mΩ. If the ESR is reduced to 20 mΩ or lower, stable operation can be achieved with effective output capacitance as low as 0.3 µF.

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS7A21 YWD (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	197.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	52.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and ICPackage Thermal Metrics and An empirical analysis of the impact of board layout on LDO thermal performance application notes.

6.5 Electrical Characteristics

specified over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 2 V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 500 mA, V_{OUT} ≥ 1.85 V		–1.5		1.5	%
		V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 500 mA, V_{OUT} < 1.85 V		–30		30	mV
ΔV_{OUT}	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA			0.03		%/V
ΔV_{OUT}	Load regulation	I_{OUT} = 1 mA to 500 mA			0.001		%/mA
I_{GND}	Quiescent current	V_{EN} = V_{IN}, V_{IN} = 6.0 V, I_{OUT} = 0 mA	T_J = 25°C		6.5	9	µA
			T_J = –40°C to 85°C			11	
			T_J = –40°C to 125°C			15	
		V_{EN} = V_{IN}, V_{IN} = 6.0 V, I_{OUT} = 500 mA			2900	3500	
I_{SHTDWN}	Shutdown current	V_{EN} = 0 V (disabled), V_{IN} = 6.0 V, T_J = 25°C			0.15	1	µA
		V_{EN} = 0 V (disabled), V_{IN} = 6.0 V, T_J = –40°C to 125°C				4	
$I_{Q(DO)}$	Quiescent current in dropout	V_{IN} ≤ $V_{OUT(NOM)}$, I_{OUT} = 0 mA			7	15	µA
V_{DO}	Dropout voltage	I_{OUT} = 500 mA, V_{OUT} = 95% × $V_{OUT(NOM)}$	0.8 V ≤ V_{OUT} < 1.0 V [(1)]			750	mV
			1.0 V ≤ V_{OUT} < 1.2 V [(1)]			530	
			1.2 V ≤ V_{OUT} < 1.5 V [(1)]			395	
			1.5 V ≤ V_{OUT} < 2.5 V			260	
			2.5 V ≤ V_{OUT} ≤ 5.5 V			175	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		740	1060	1500	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V			325		mA
PSRR	Power-supply rejection ratio	I_{OUT} = 20 mA, V_{IN} = V_{OUT} + 1.0 V	f = 100 Hz		90		dB
			f = 1 kHz		91		
			f = 10 kHz		71		
			f = 100 kHz		61		
			f = 1 MHz		50		
		I_{OUT} = 500 mA, V_{IN} = V_{OUT} + 1.0 V	f = 100 Hz		65		dB
			f = 1 kHz		85		
			f = 10 kHz		79		
			f = 100 kHz		44		
			f = 1 MHz		50		

6.5 Electrical Characteristics (continued)

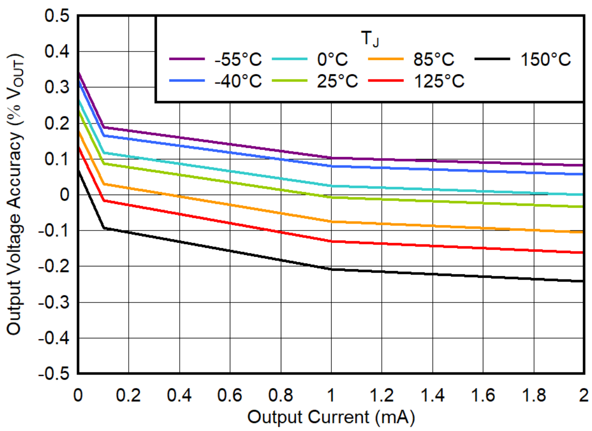
specified over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 2 V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	I_{OUT} = 500 mA		7.7		μV_{RMS}
			I_{OUT} = 1 mA		10		
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{IN} = 2 V, V_{EN} < V_{IL} (output disabled)			150		Ω
T_{SD}	Thermal shutdown rising	T_J rising			165		°C
	Thermal shutdown falling	T_J falling			140		
$V_{EN(LOW)}$	Low input threshold	V_{IN} = 2.0 V to 6.0 V, V_{EN} falling until the output is disabled				0.3	V
$V_{EN(HI)}$	High input threshold	V_{IN} = 2.0 V to 6.0 V, V_{EN} rising until the output is enabled		0.9			V
V_{UVLO}	UVLO threshold	V_{IN} rising		1.11	1.32	1.63	V
		V_{IN} falling		1.05	1.27	1.57	
$V_{UVLO(HYST)}$	UVLO hysteresis				50		mV
I_{EN}	EN pin leakage current	V_{EN} = 6.0 V and V_{IN} = 6.0 V			100	250	nA
$R_{EN(PULL-DOWN)}$	Smart enable pulldown resistor				440		kΩ
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$		120	200	280	µs

(1) Dropout voltages for V_{OUT} values below or very near the UVLO threshold cannot be measured directly. Values shown are verified by simulation.

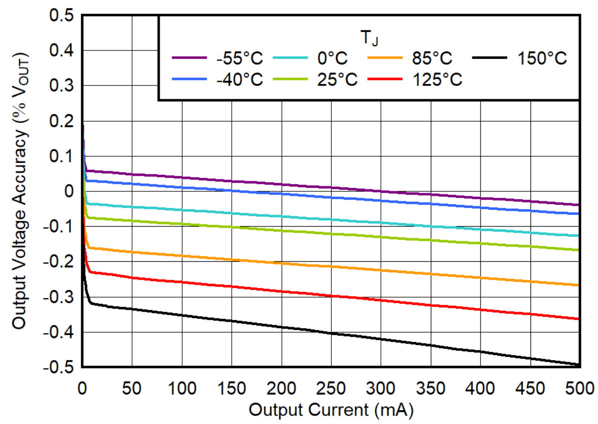
6.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



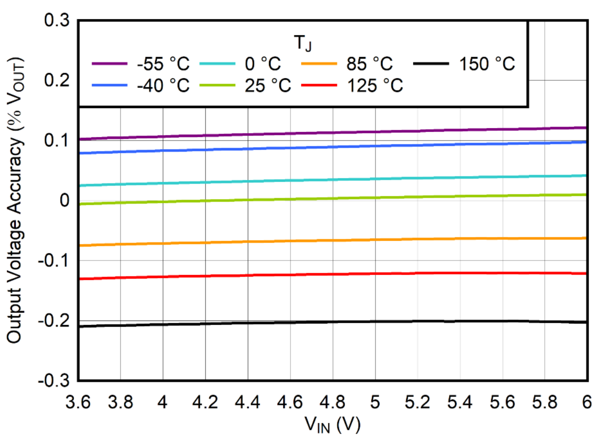
V_{EN} = 1 V

図 6-1. Output Voltage Accuracy vs I_{OUT}



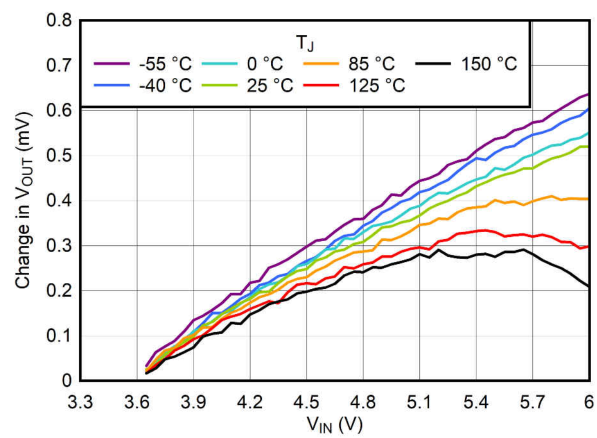
V_{EN} = 1 V

図 6-2. Output Voltage Accuracy vs I_{OUT}



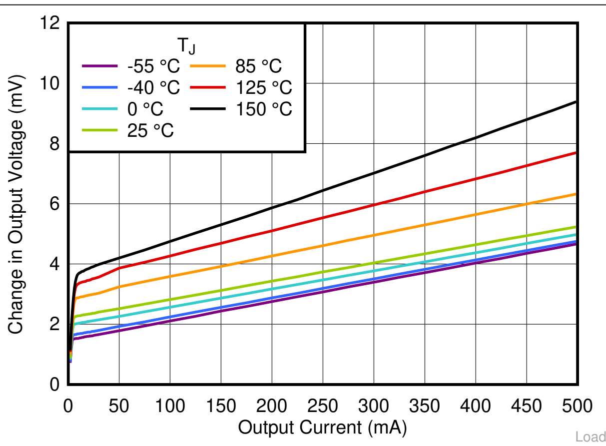
V_{EN} = 1 V

図 6-3. Output Voltage Accuracy vs V_{IN}



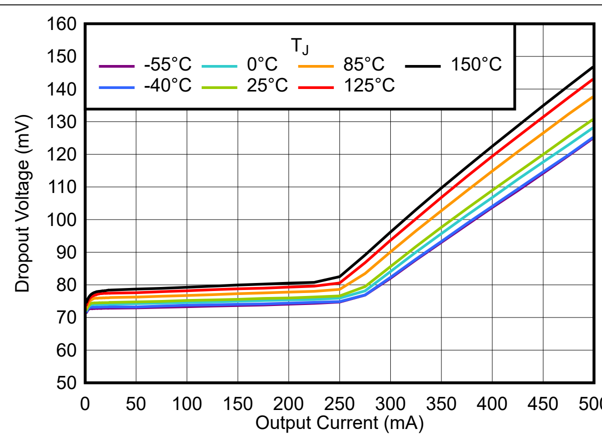
V_{EN} = 1 V

図 6-4. Line Regulation vs V_{IN}



V_{EN} = 1 V

図 6-5. Load Regulation vs I_{OUT}

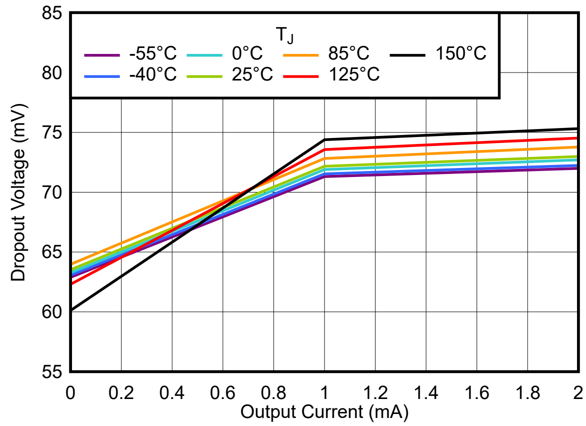


V_{EN} = 1 V

図 6-6. Dropout Voltage vs I_{OUT}

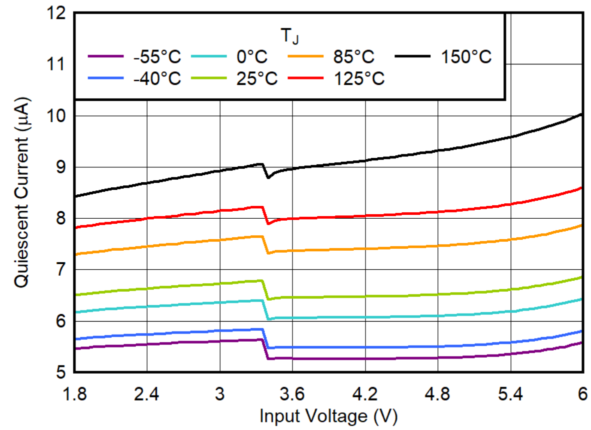
6.6 Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



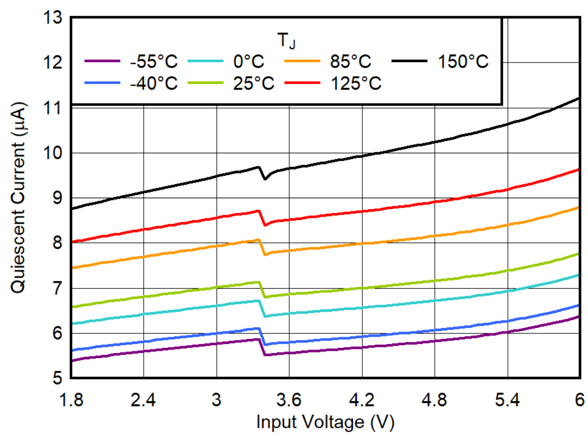
V_{EN} = 1 V

図 6-7. Dropout Voltage vs I_{OUT}



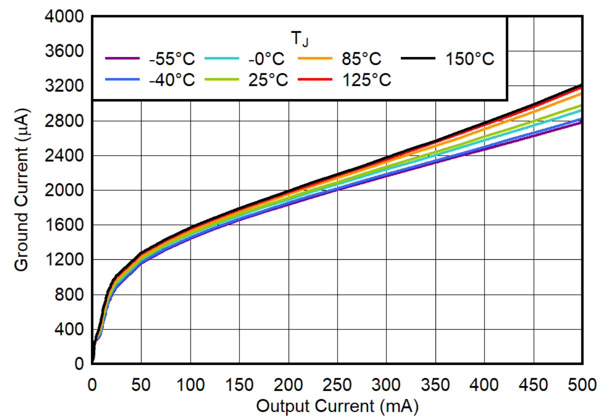
V_{EN} = V_{IN}

図 6-8. I_Q vs V_{IN}



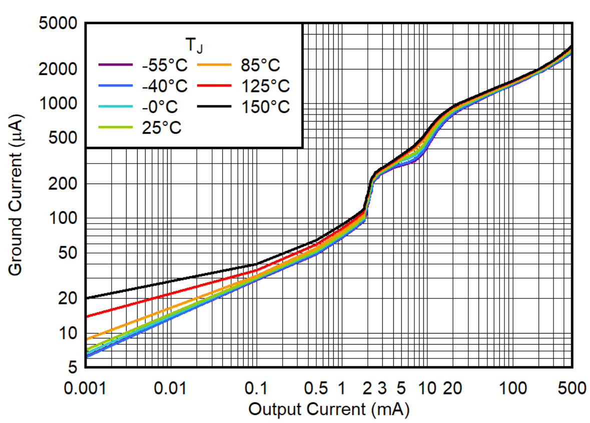
V_{EN} = 1 V

図 6-9. I_Q vs V_{IN}



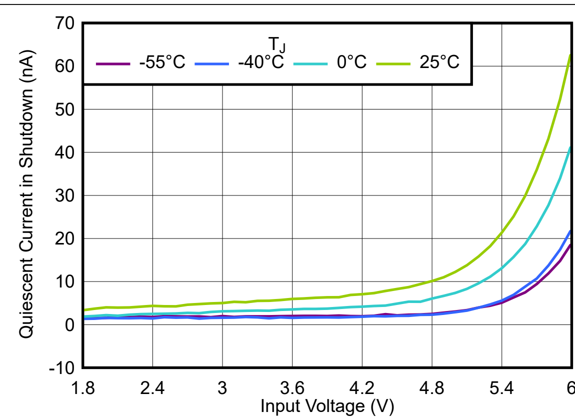
V_{EN} = 1 V

図 6-10. I_{GND} vs I_{OUT}



V_{EN} = 1 V

図 6-11. I_{GND} vs I_{OUT}

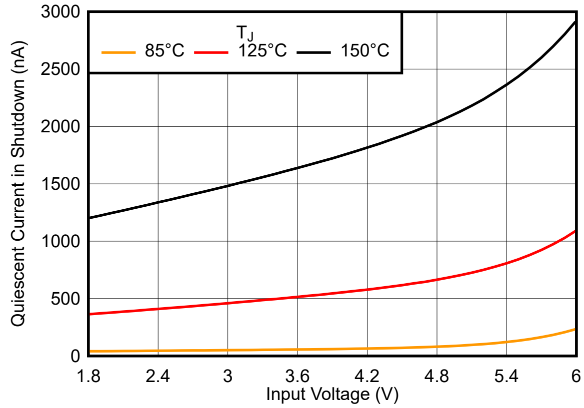


V_{EN} = 0 V, I_{OUT} = 0 mA

図 6-12. Shutdown Current vs V_{IN}

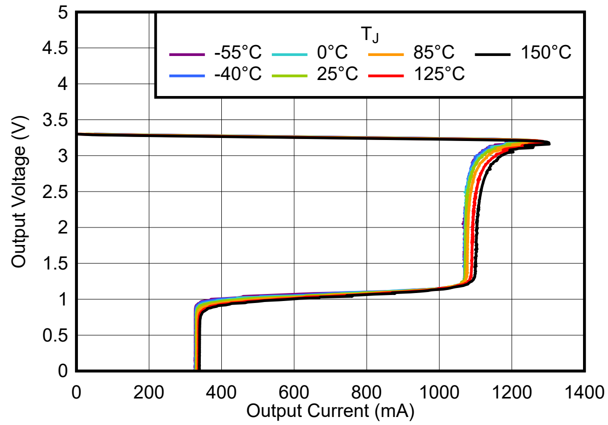
6.6 Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



V_{EN} = 0 V, I_{OUT} = 0 mA

図 6-13. Shutdown Current vs V_{IN}



V_{EN} = 1 V

図 6-14. Foldback Current Limit

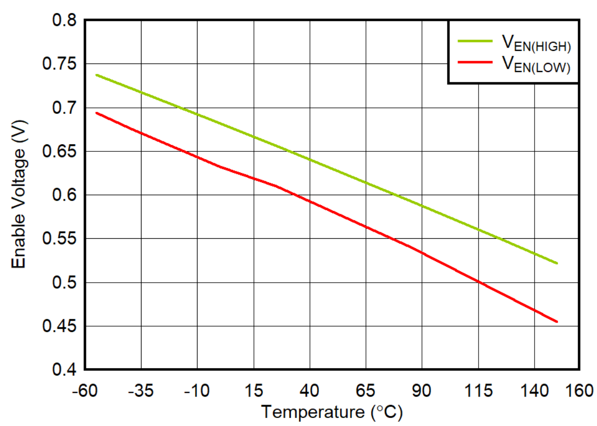
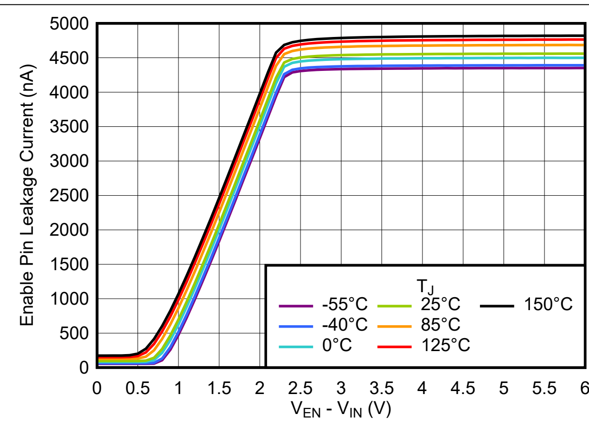
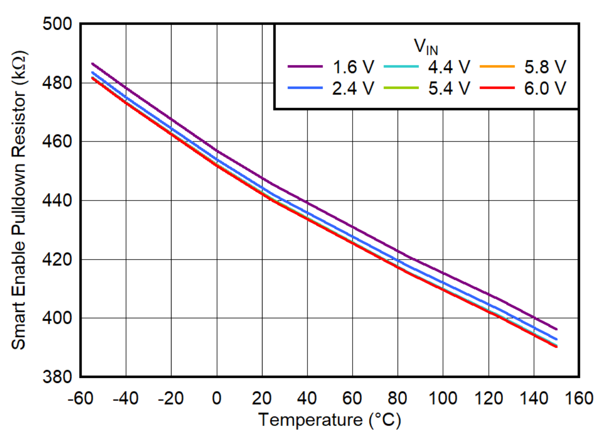


図 6-15. Enable Logic Threshold vs Temperature



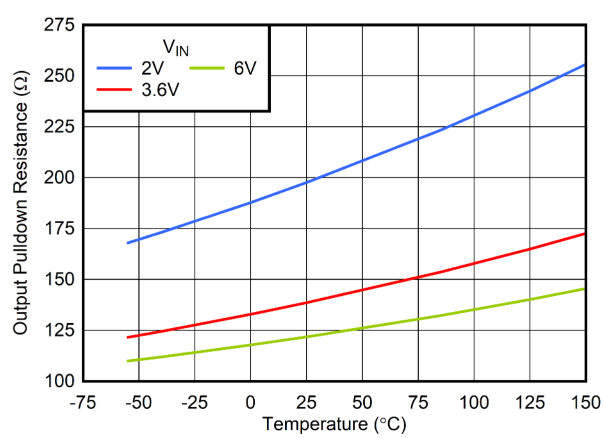
V_{EN} = 6 V, I_{OUT} = 0 mA

図 6-16. Enable Pin Leakage Current vs V_{EN} – V_{IN}



V_{EN} = 0.3 V

図 6-17. Smart Enable Pulldown Resistor vs Temperature and V_{IN}

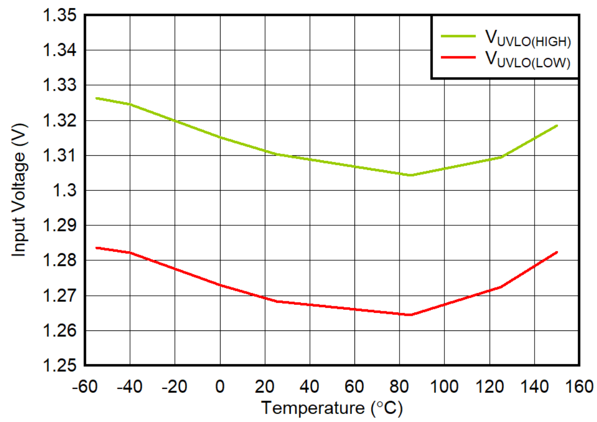


V_{EN} = 0.3 V

図 6-18. Output Pulldown Resistance vs Temperature and V_{IN}

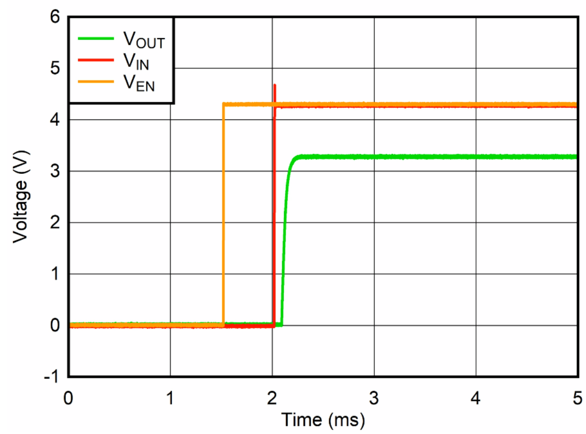
6.6 Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



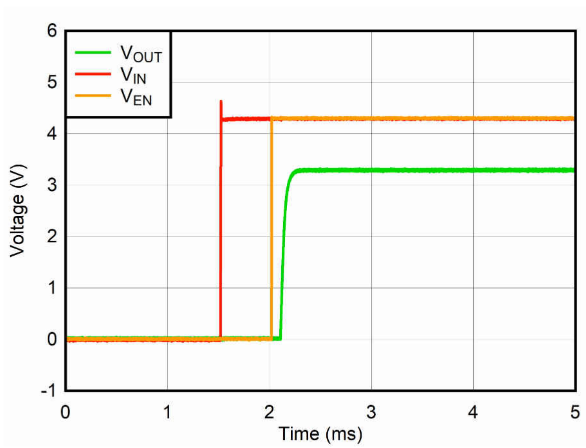
V_{EN} = 1 V

図 6-19. V_{IN} UVLO Threshold vs Temperature



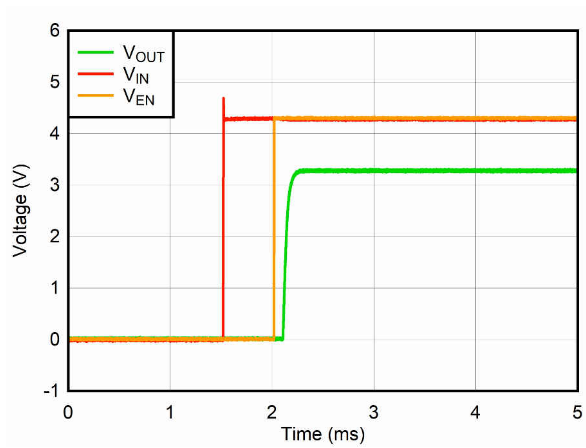
V_{IN} = 0 V to 4.3 V, slew rate = 1 V/µs, I_{OUT} = 500 mA

図 6-20. Start-Up With V_{EN} Before V_{IN}



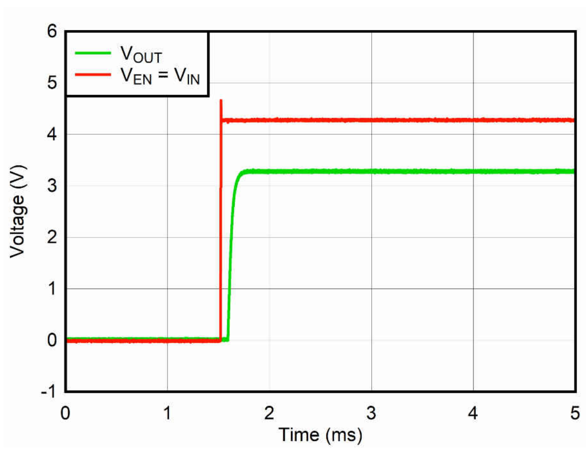
V_{IN} = 0 V to 4.3 V, slew rate = 1 V/µs, I_{OUT} = 0 mA

図 6-21. Start-Up With V_{EN} After V_{IN}



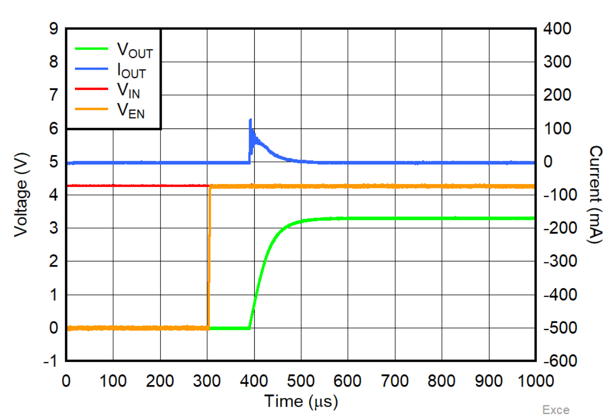
V_{IN} = 0 V to 4.3 V, slew rate = 1 V/µs, I_{OUT} = 500 mA

図 6-22. Start-Up With V_{EN} After V_{IN}



V_{IN} = 0 V to 4.3 V, slew rate = 1 V/µs, I_{OUT} = 500 mA

図 6-23. Start-Up With V_{EN} = V_{IN}

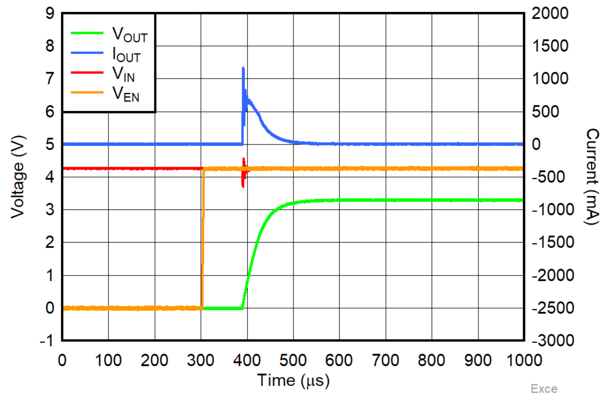


V_{IN} = 4.3 V, V_{EN} = 0 V to 4.3 V, slew rate = 1 V/µs, I_{OUT} = 0 mA, C_{OUT} = 1 µF

図 6-24. Start-Up Inrush Current

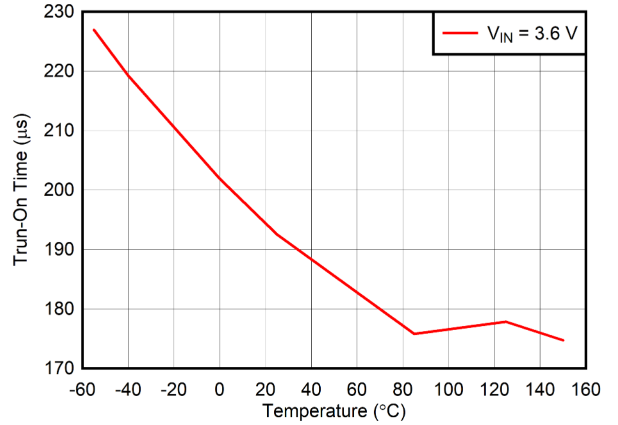
6.6 Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



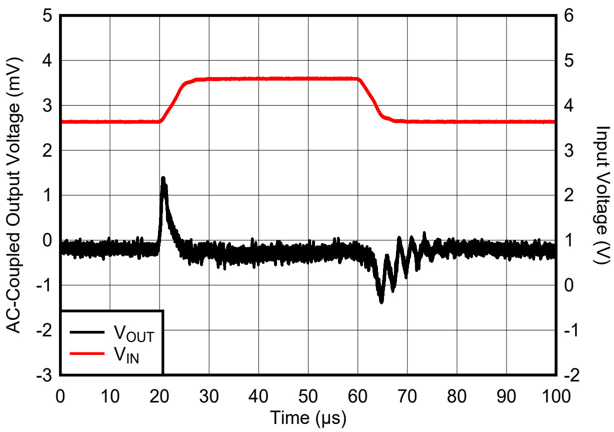
V_{IN} = 4.3 V, V_{EN} = 0 V to 4.3 V, slew rate = 1 V/µs,
I_{OUT} = 0 mA, C_{OUT} = 10 µF

図 6-25. Start-Up Inrush Current



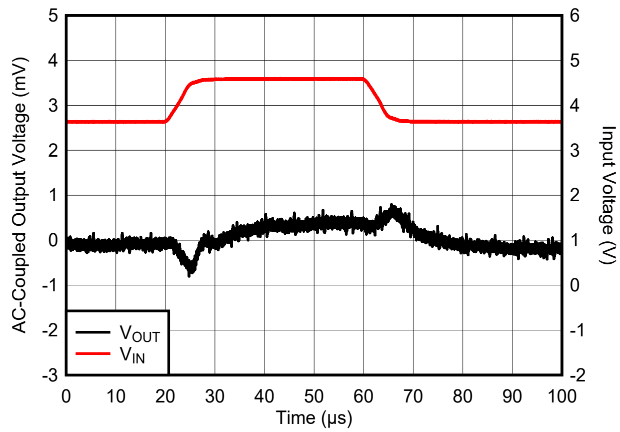
V_{EN} = $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, I_{OUT} = 0 mA

図 6-26. Start-Up Turn-On Time vs Temperature



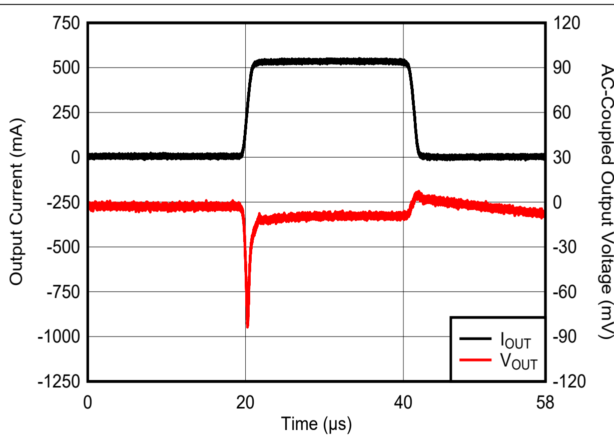
V_{EN} = V_{IN}, t_r = t_f = 5 µs, I_{OUT} = 500 mA

図 6-27. Line Transient From 3.6 V to 4.6 V



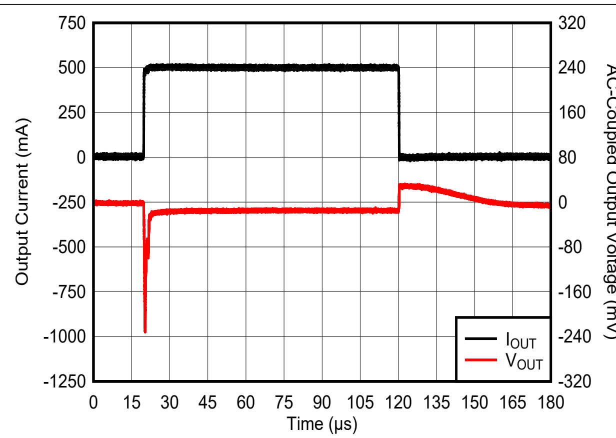
V_{EN} = V_{IN}, t_r = t_f = 5 µs, I_{OUT} = 1 mA

図 6-28. Line Transient From 3.6 V to 4.6 V



V_{EN} = V_{IN}, t_r = t_f = 1 µs

図 6-29. Load Transient From 1 mA to 500 mA

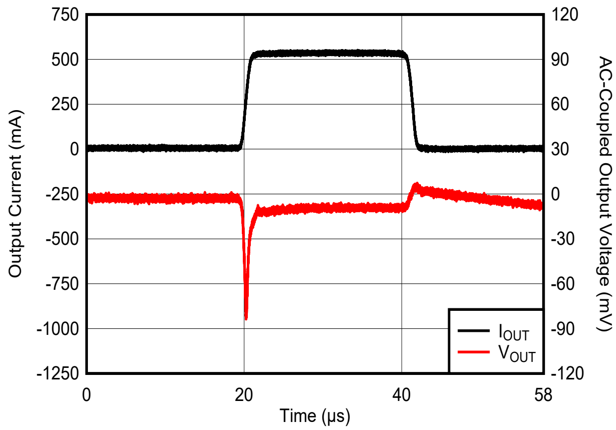


V_{EN} = V_{IN}, t_r = t_f = 200 ns

図 6-30. Load Transient From 1 mA to 500 mA

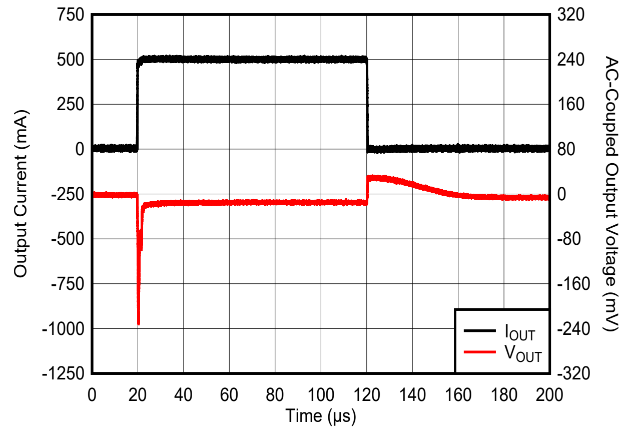
6.6 Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



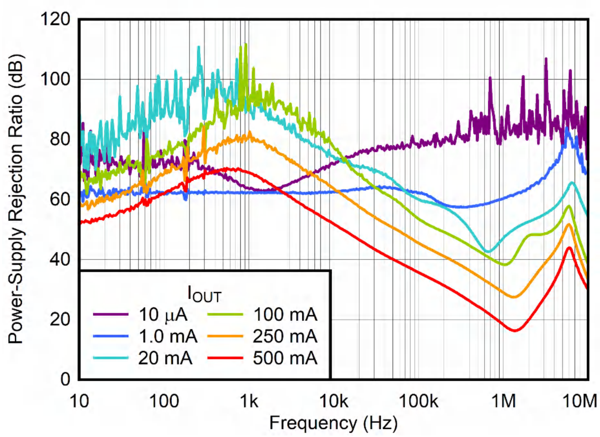
V_{EN} = V_{IN}, t_r = t_f = 1 µs

図 6-31. Load Transient From 0 mA to 500 mA



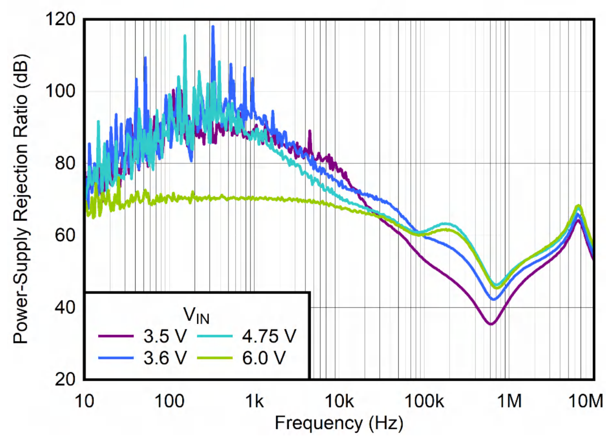
V_{EN} = V_{IN}, t_r = t_f = 200 ns

図 6-32. Load Transient From 0 mA to 500 mA



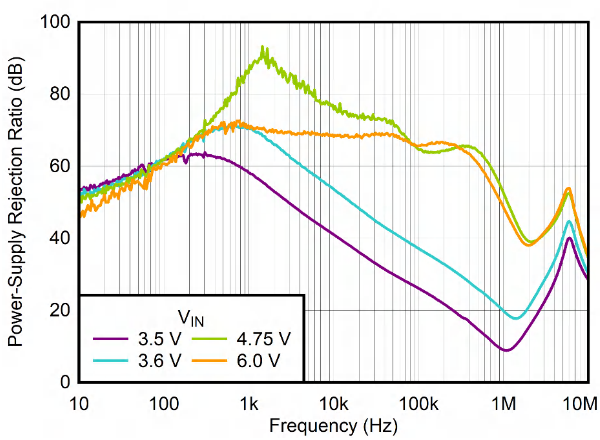
V_{EN} = V_{IN}

図 6-33. PSRR vs Frequency and I_{OUT}



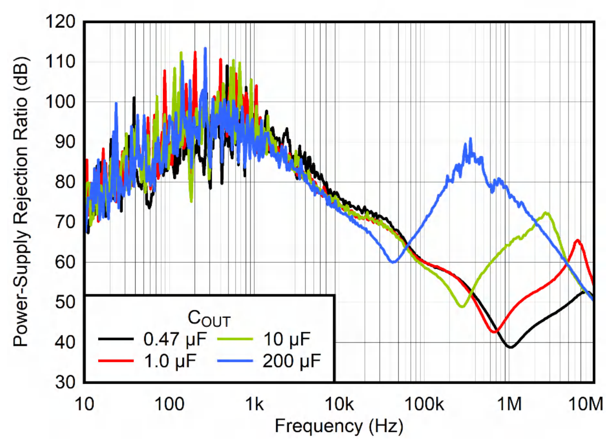
V_{EN} = V_{IN}, I_{OUT} = 20 mA

図 6-34. PSRR vs Frequency and V_{IN}



V_{EN} = V_{IN}, I_{OUT} = 500 mA

図 6-35. PSRR vs Frequency and V_{IN}

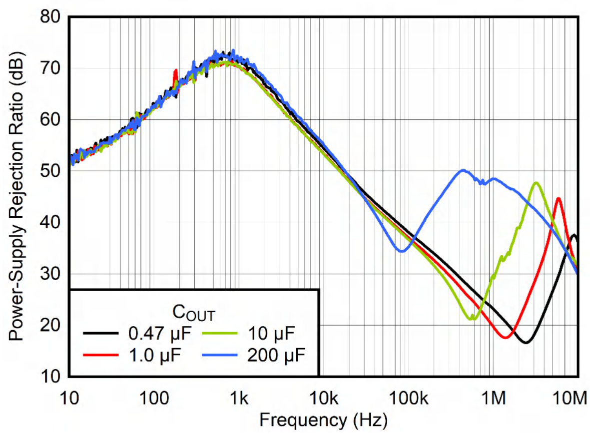


V_{EN} = V_{IN}, I_{OUT} = 20 mA

図 6-36. PSRR vs Frequency and C_{OUT}

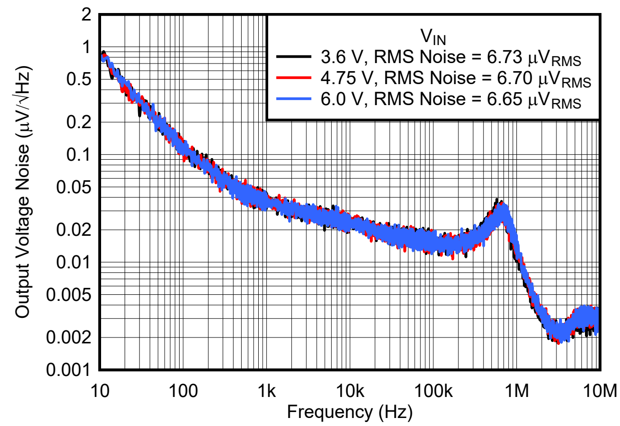
6.6 Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



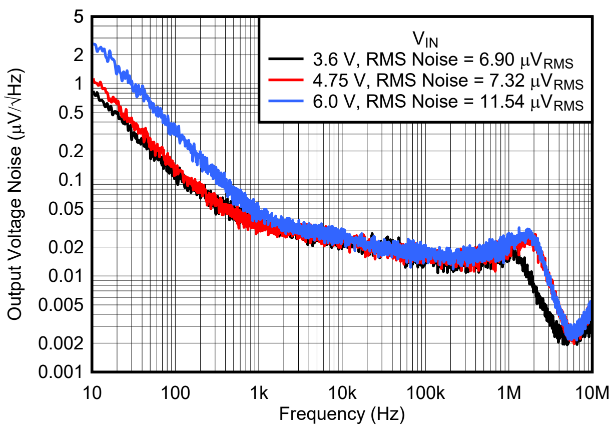
V_{EN} = V_{IN}, I_{OUT} = 500 mA

図 6-37. PSRR vs Frequency and C_{OUT}



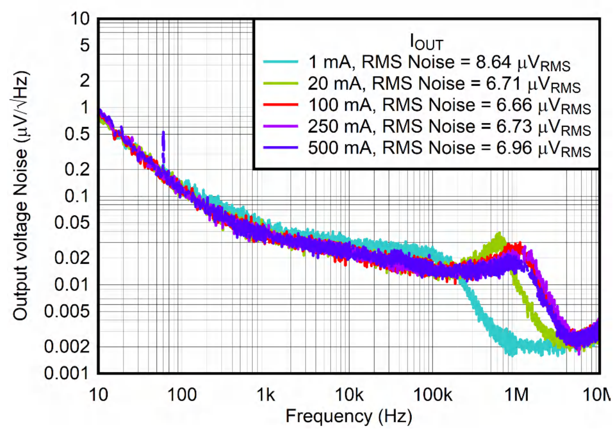
V_{EN} = V_{IN}, I_{OUT} = 20 mA

図 6-38. Noise vs Frequency and V_{IN}



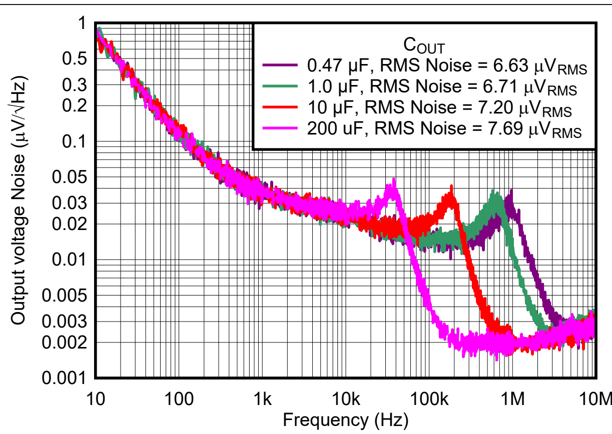
V_{EN} = V_{IN}, I_{OUT} = 500 mA

図 6-39. Noise vs Frequency and V_{IN}



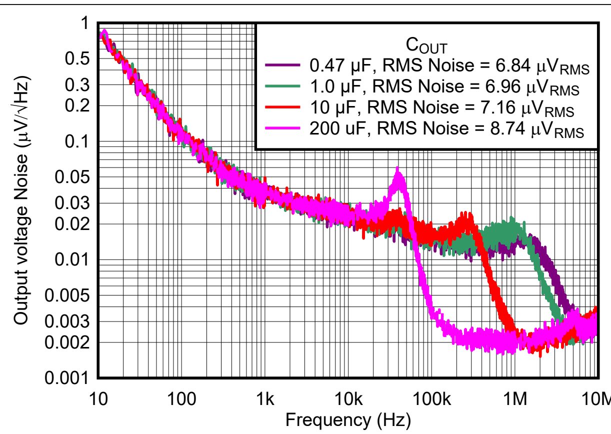
V_{EN} = V_{IN}

図 6-40. Noise vs Frequency and I_{OUT}



V_{EN} = V_{IN}, I_{OUT} = 20 mA

図 6-41. Noise vs Frequency and C_{OUT}



V_{EN} = V_{IN}, I_{OUT} = 500 mA

図 6-42. Noise vs Frequency and C_{OUT}

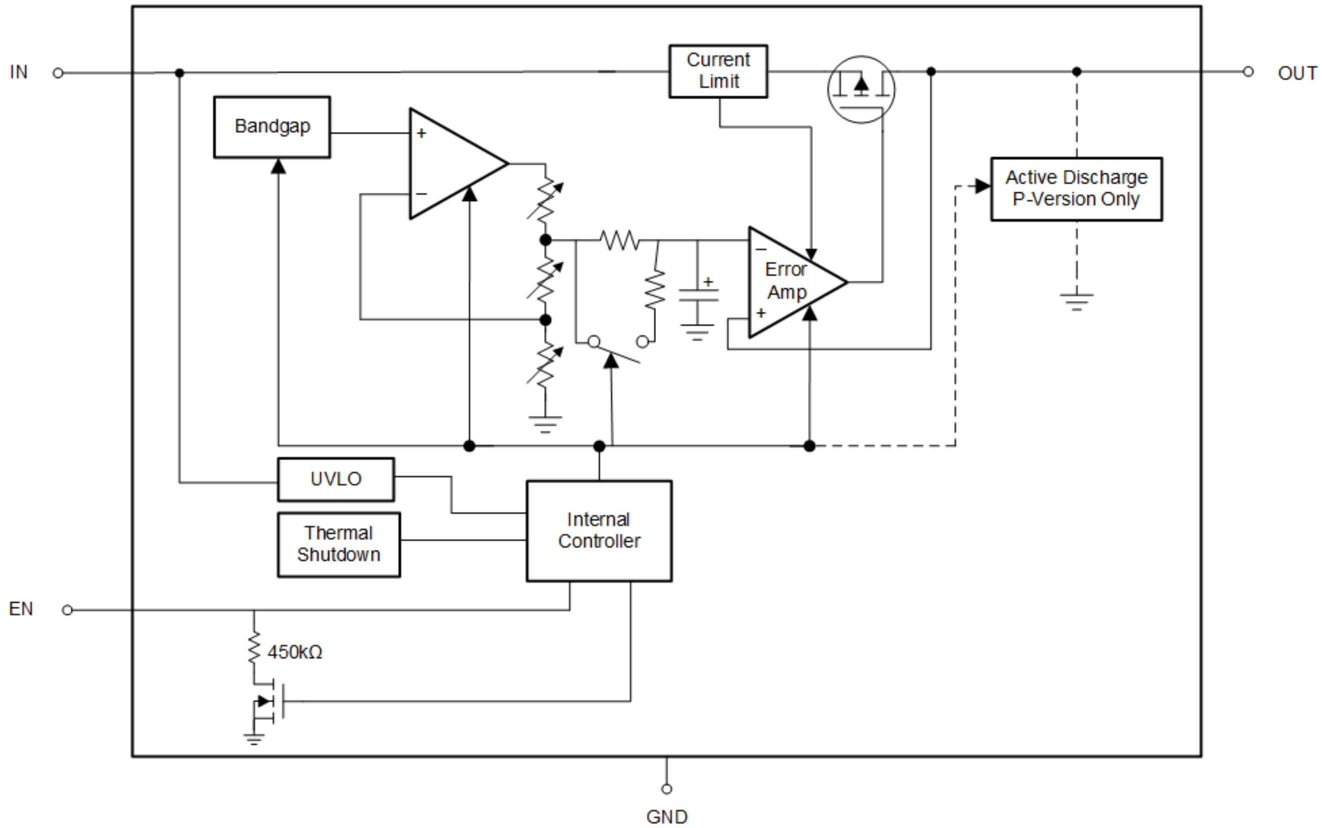
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A21 provides low noise, high PSRR, and low quiescent current, as well as excellent line and load transient response. The TPS7A21 achieves excellent noise performance without the need for a separate noise filter capacitor.

The TPS7A21 is designed to operate properly with a single 1-μF input capacitor and a single 1-μF ceramic output capacitor. The effective output capacitance must be at least 0.4 μF across all operating voltage and temperature conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Enable (EN)

The enable pin (EN) is active high. The output is enabled when the voltage applied to EN is greater than $V_{EN(HI)}$ and disabled when the applied voltage is less than $V_{EN(LOW)}$. If external control of the output voltage is not needed, connect EN to IN. This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, the output is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the output. In addition to reducing quiescent current, the smart pulldown helps ensure that the logic level is correct even when EN is driven from a source that has limited current drive capability. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

7.3.2 Low Output Noise

Any internal noise at the TPS7A21 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cutoff frequency of approximately 0.1 Hz. During start-up, the filter resistor is bypassed to reduce output rise time. The filter begins normal operation after the output voltage reaches the nominal value.

7.3.3 Active Discharge

The regulator has an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a pulldown resistor between the output and ground pins when the device is disabled to actively discharge the output voltage. The voltage on IN must be high enough to turn on the pulldown MOSFET; when V_{IN} is too low to provide sufficient V_{GS} on the pulldown MOSFET, the pulldown circuit is not active. The active discharge circuit is activated by the enable pin, or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for only a short period of time.

7.3.4 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), when the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to support output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. 式 1 calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.5 Foldback Current Limit

The TPS7A21 has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$).

In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the output voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the *short-circuit current limit* (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the output is shorted and the output voltage is less than $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 7-1 shows a diagram of the foldback current limit.

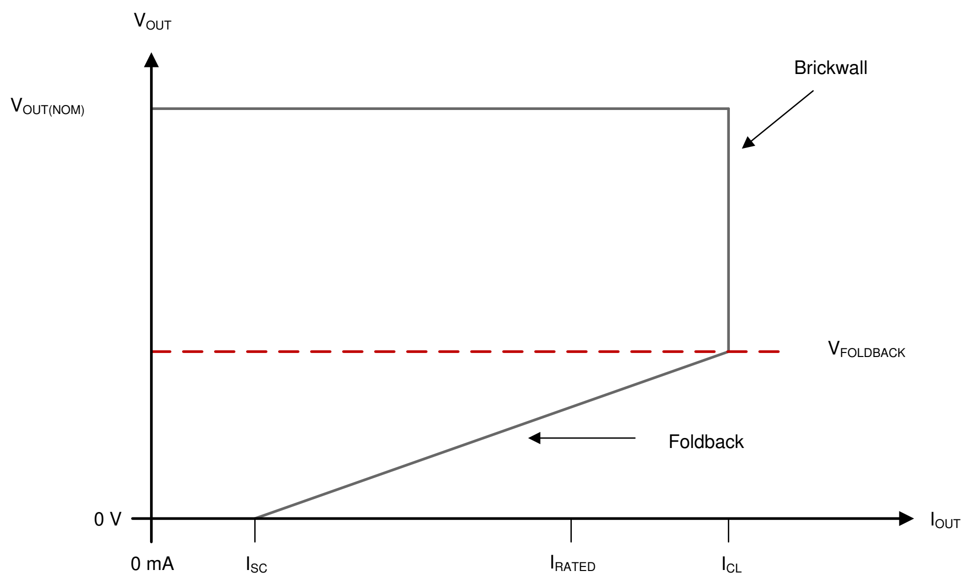


図 7-1. Foldback Current Limit

7.3.6 Undervoltage Lockout

An independent undervoltage lockout (UVLO) circuit monitors the input voltage, allowing a controlled and consistent turn on and turn off of the output voltage. If the input voltage drops during load transients (when the device output is enabled), the UVLO has built-in hysteresis to prevent unwanted turn off.

7.3.7 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature T_J rises to the shutdown temperature threshold T_{SD}. The thermal shutdown circuit hysteresis requires the temperature to fall to a lower temperature before turning on again. The thermal time constant of the semiconductor die is fairly short; thus, the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced.

Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the regulator to exceed operational specifications.

Although the thermal shutdown circuitry is designed to protect against temporary thermal overload conditions, this circuitry is not intended to replace proper thermal design. Continuously running the regulator into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} \geq V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} \geq V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} \leq V_{EN(LOW)}$	Not applicable	$T_J \geq T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

For output currents less than about 200 mA, the slope of the dropout voltage curve is lower than for higher currents. This slope helps maintain better performance when the LDO is in dropout.

7.4.4 Disabled

The output of the device can be shut down by forcing the voltage of the enable pin to less than $V_{EN(LOW)}$. When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for many types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Consult the manufacturer data sheet to verify performance. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although the LDO is stable without an input capacitor, good design practice is to connect a capacitor from IN to GND, with a value at least equal to the nominal value specified in the *Recommended Operating Conditions* table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5 Ω. When the source resistance and inductance are sufficiently high, the overall system can be susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between IN and GND. A capacitor with a value greater than the minimum may be necessary if there are large fast-rise-time load or line transients or if the LDO is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps ensure stability and improve dynamic performance. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table.

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 図 8-1 are broken down as follows. Regions A, E, and H are where the output voltage is in a steady state.

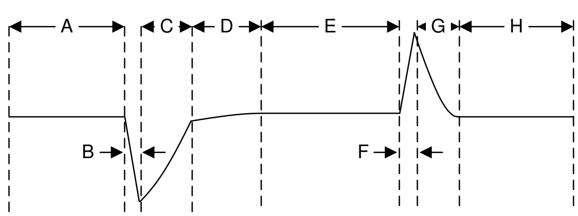


図 8-1. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit verifies that the device stays disabled before the input supply reaches the minimum operational voltage range, and makes sure that the device shuts down when the input supply collapses. 図 8-2 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The device remains enabled even if the output falls out of regulation.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

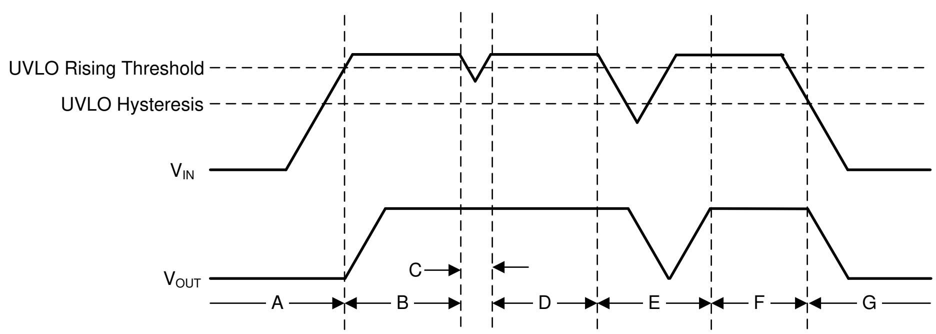


図 8-2. Typical UVLO Operation

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{2}$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A21 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum allowable junction temperature (T_J) determines the maximum power dissipation for the device. According to 式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

式 4 rearranges 式 3 for output current.

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} \times (V_{IN} – V_{OUT})] \tag{4}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \tag{5}$$

where:

- P_D is the power dissipated as explained in the *Power Dissipation (P_D)* section
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.7 Recommended Area For Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 図 8-3 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is depicted in the third region of 図 8-3. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO. Thus, when $V_{IN} – V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

図 8-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{θJA}$, as given in the *Thermal Information* table.

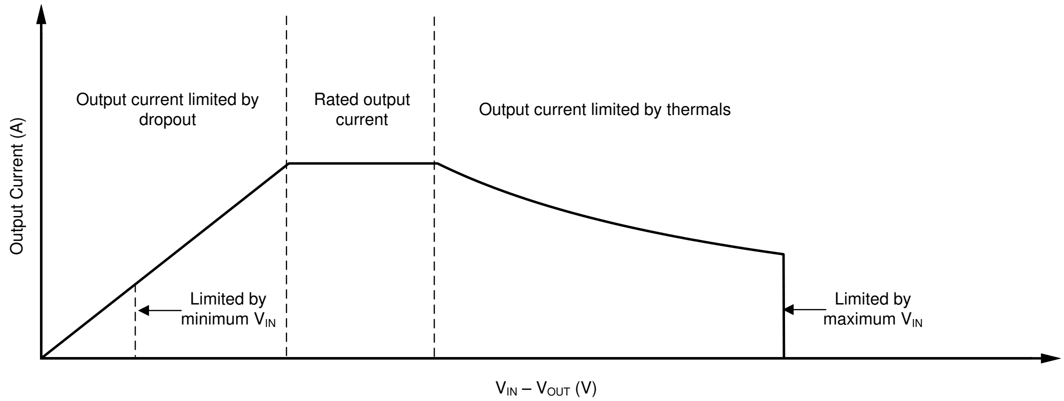


図 8-3. Region Description of Continuous Operation Regime

8.2 Typical Application

図 8-4 shows the typical application circuit for the TPS7A21. Input and output capacitances may need to be increased above the 1 µF minimum value for some applications.

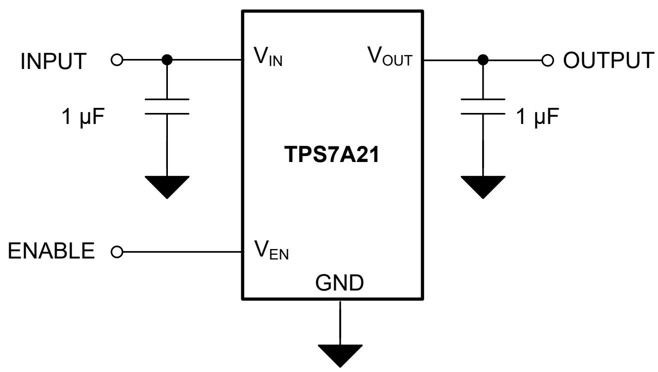


図 8-4. TPS7A21 Typical Application

8.2.1 Design Requirements

表 8-1 summarizes the design requirements for the typical application circuit.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.6 V
Output voltage	3.3 V
Output current	400 mA
Maximum ambient temperature	85°C

8.2.2 Detailed Design Procedure

For this design example, the 3.3-V output version (TPS7A2133) is selected. A nominal 3.6-V input supply is assumed. Use a minimum 1.0-µF input capacitor to minimize the effect of resistance and inductance between the 3.6-V source and the LDO input. A minimum 1.0-µF output capacitor is also used for stability and good load transient response. The dropout voltage (V_{DO}) is less than 150 mV maximum at a 3.3-V output voltage and 500-mA output current, so there are no dropout issues with a minimum input voltage of 3.5 V and a maximum output current of 400 mA.

With an ambient temperature of 85°C, an input voltage of 3.6 V and an output current of 400 mA, the die temperature is 0.3 V × 0.4 A × 197.1°C/W + 85°C = 108.7°C.

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source (the junctions of the device) to the ultimate heat sink of the ambient environment. Thus, power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

式 6 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \tag{6}$$

式 7 represents the actual power being dissipated in the device:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{7}$$

These two equations establish the relationship between the maximum power dissipation allowed resulting from thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Use these two equations to determine the optimum operating conditions for the device in the application.

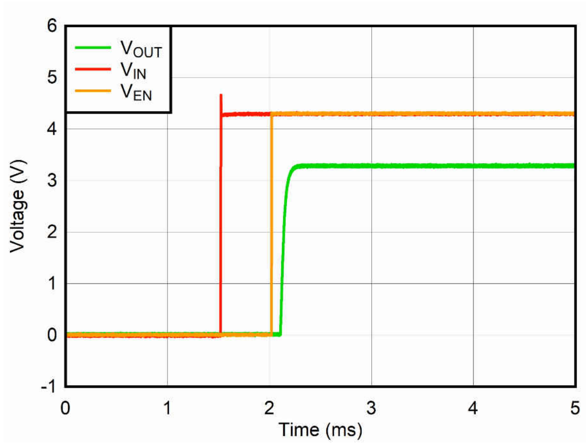
In applications where lower power dissipation (P_D) or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. As given by 式 8, $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the device or package in the application ($R_{\theta JA}$):

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \tag{8}$$

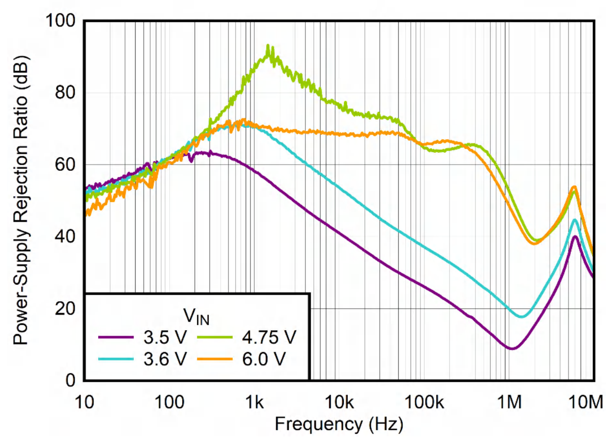
Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This reduction can be accomplished by reducing V_{IN} in the V_{IN}–V_{OUT} term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.3 Application Curves



V_{IN} = 0 V to 4.3 V, slew rate = 1 V/µs, I_{OUT} = 1 mA

図 8-5. Start-Up With V_{EN} After V_{IN}



V_{EN} = V_{IN}, I_{OUT} = 500 mA

図 8-6. PSRR vs Frequency and V_{IN}

8.3 Power Supply Recommendations

This LDO is designed to operate from an input supply voltage range of 2.0 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the TPS7A21 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 0.3 V. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

8.4 Layout

8.4.1 Layout Guidelines

The dynamic performance of the TPS7A21 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the TPS7A21.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the TPS7A21, and as close to the package as practical. The ground connections for C_{IN} and C_{OUT} must be back to the TPS7A21 ground pin using as wide and short a copper trace as practical.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. These connections add parasitic inductances and resistance that results in inferior performance, especially during transient conditions.

8.4.1.1 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in the *AN-1112 DSBGA Wafer Level Chip Scale Package* application note. For best results during assembly, alignment ordinals on the PCB can be used to facilitate placement of the DSBGA device.

8.4.1.2 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

8.4.2 Layout Example

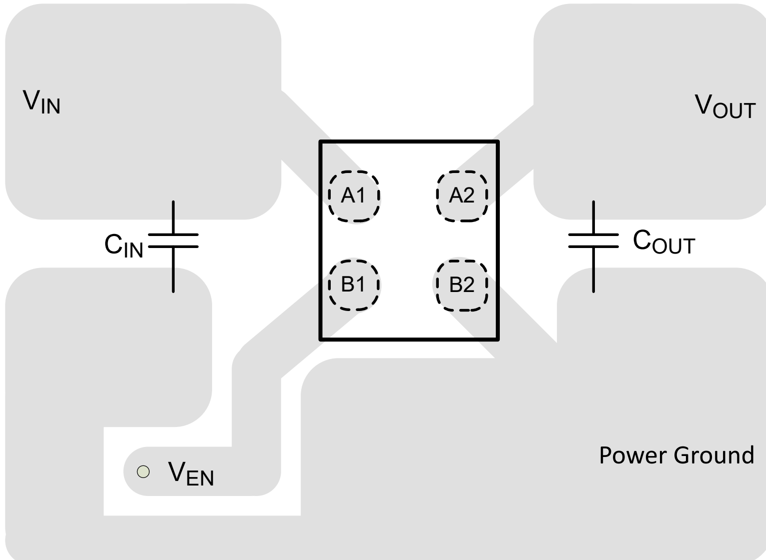


図 8-7. Typical DSBGA Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

表 9-1. Device Nomenclature[1][2]

PRODUCT	V_{OUT}
TPS7A21**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TPS7A21 family actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. J is for 12000-piece reel.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.8 V to 5.5 V in 50-mV increments are available. Contact the factory for details and availability.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *TPS7A21EVM-059 Evaluation Module* user guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

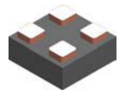
9.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

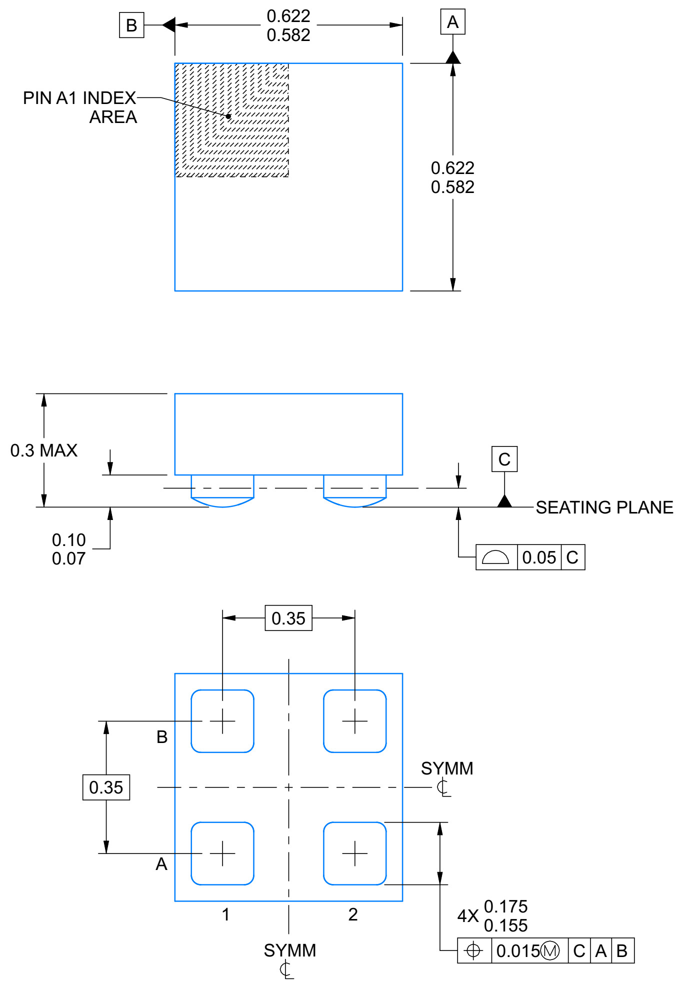


YWD0004A-C01

PACKAGE OUTLINE

PowerWCSP - 0.3 mm max height

POWER CHIP SCALE PACKAGE



4228730/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

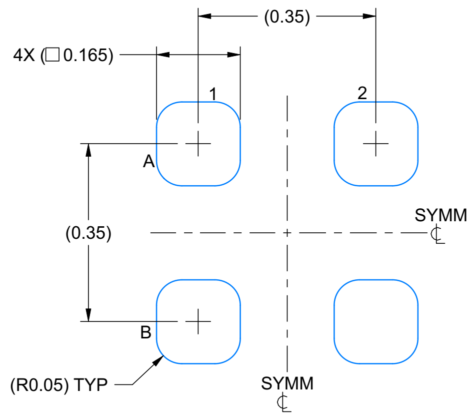
www.ti.com

EXAMPLE BOARD LAYOUT

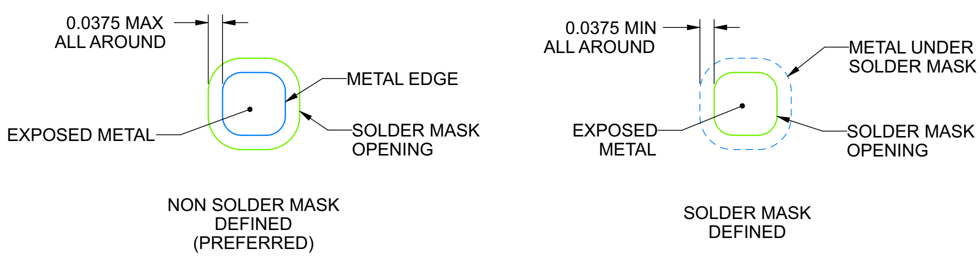
YWD0004A-C01

PowerWCSP - 0.3 mm max height

POWER CHIP SCALE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 80X



SOLDER MASK DETAILS
NOT TO SCALE

4228730/A 05/2022

NOTES: (continued)

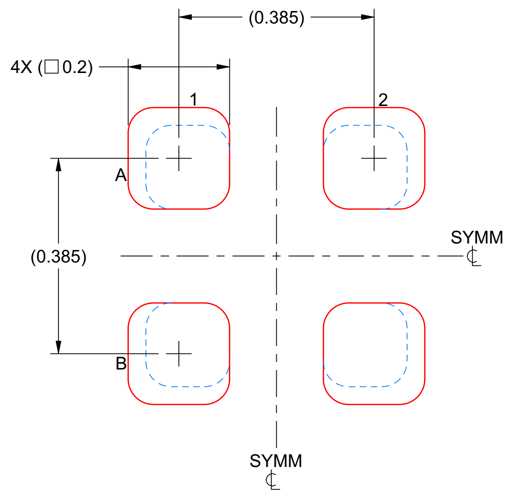
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

YWD0004A-C01

PowerWCSP - 0.3 mm max height

POWER CHIP SCALE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 80X

4228730/A 05/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A2128PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y
TPS7A2128PYWDJ.A	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y
TPS7A2130PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	R
TPS7A2130PYWDJ.A	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	R
TPS7A2132PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y
TPS7A2133BPYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A2133BPYWDJ.A	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A2133PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A2133PYWDJ.A	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A21345PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1
TPS7A21345PYWDJ.A	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1
TPS7A2135PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Z
TPS7A2137PYWDJ	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	7
TPS7A2137PYWDJ.A	Active	Production	DSBGA (YWD) | 4	12000 | JUMBO T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	7

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS7A21 :

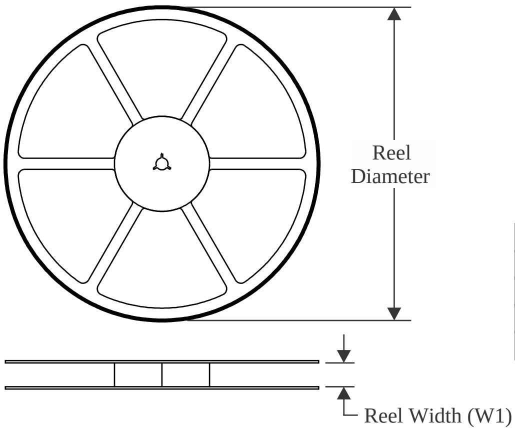
- Automotive : TPS7A21-Q1

NOTE: Qualified Version Definitions:

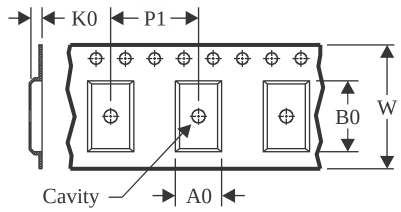
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

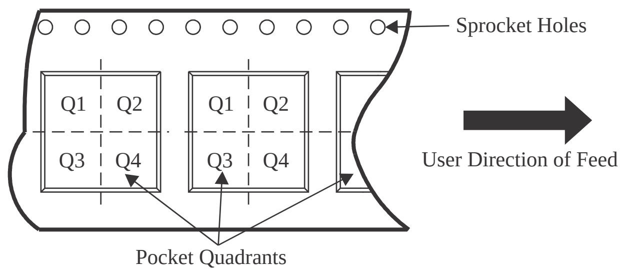


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

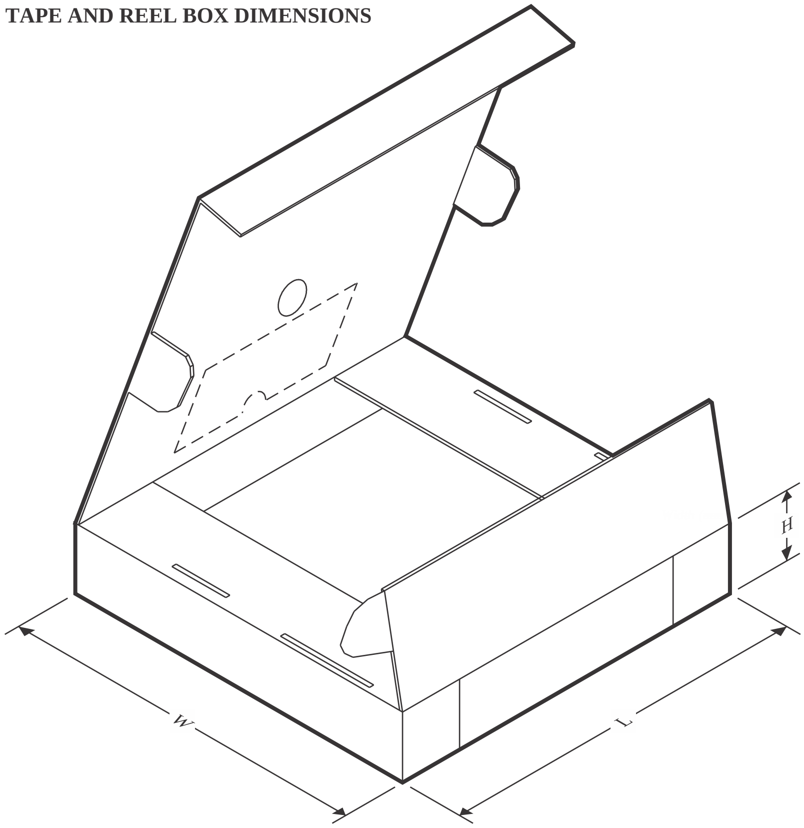
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

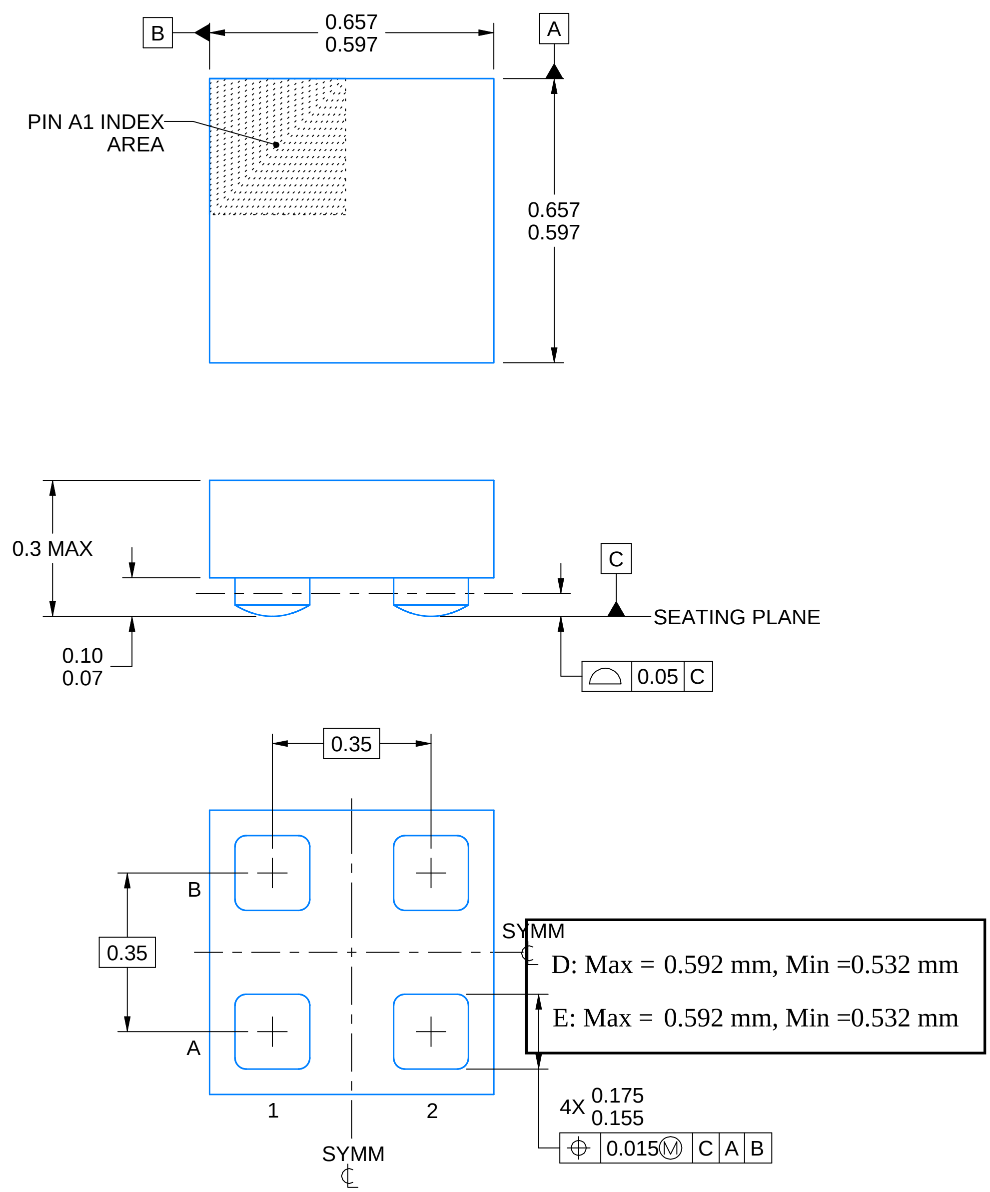
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2128PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2130PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2130PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2132PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2132PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2133BPYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2133PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2133PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A21345PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2135PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2137PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1
TPS7A2137PYWDJ	DSBGA	YWD	4	12000	180.0	8.4	0.69	0.69	0.37	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

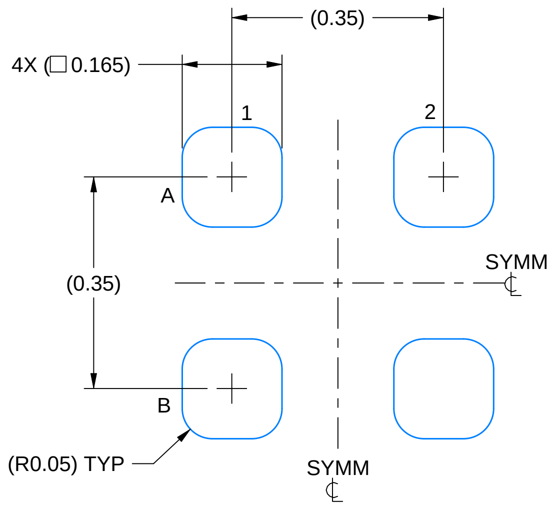
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2128PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2130PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2130PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2132PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2132PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2133BPYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2133PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2133PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A21345PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2135PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2137PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0
TPS7A2137PYWDJ	DSBGA	YWD	4	12000	182.0	182.0	20.0



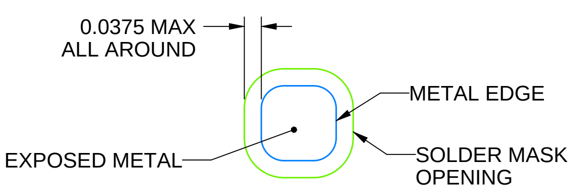
4225173/A 07/2019

NOTES:

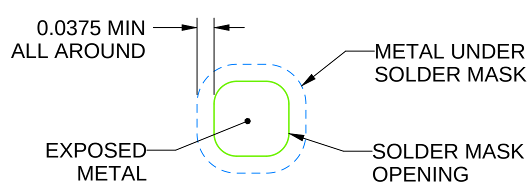
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 80X



NON SOLDER MASK
DEFINED
(PREFERRED)



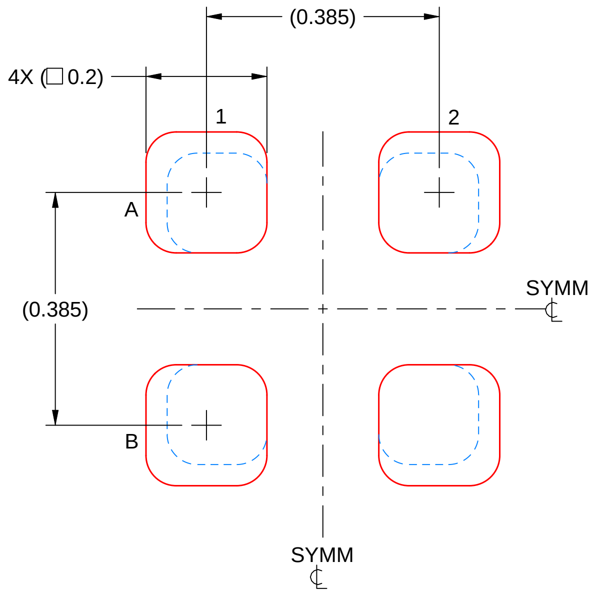
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4225173/A 07/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 80X

4225173/A 07/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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