TPS7A7100 1A、高速過渡、低ドロップアウト電圧レギュレータ

1 特長

- 低いドロップアウト電圧：1A 時に 140mV
- V_{IN} 範囲：1.5V～6.5V
- 構成可能な固定 V_{OUT} の範囲：0.9V～3.5V
- 調整可能な V_{OUT} の範囲：0.9V～5V
- 非常に優れた負荷 / 入力電圧過渡応答
- セラミック出力コンデンサの使用により安定性を確保
- 精度 1.5% の過入力電圧、過負荷、過熱
- プログラマブル・ソフト・スタート
- パワー・グッド (PG) 出力
- パッケージ：
  - 3mm × 3mm、16 ピン VQFN
  - 5mm × 5mm、20 ピン VQFN

2 アプリケーション

- ワイヤレス・インフラ
- RF コンポーネント
- セット・トップ・ボックス
- PC とプリンタ
- オーディオと映像

3 概要

TPS7A7100 低ドロップアウト (LDO) 電圧レギュレータは、1.5V～6.5V の入力電圧に対して、非常に低いドロップアウト性能 (1A 時に 140mV) を必要とするアプリケーション向けに設計されています。 TPS7A7100 は、0.9V～3.5V の範囲でユーザーが構成可能な出力電圧を設定する革新的な機能を備えており、外付け抵抗やそれに関連するエラーを解消します。

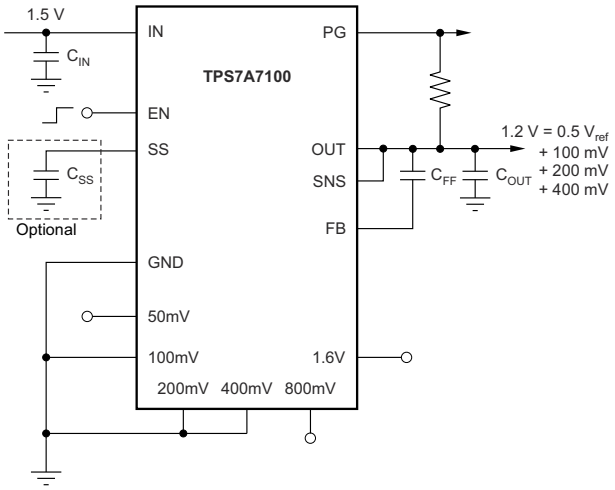
TPS7A7100 は、非常に高速な負荷過渡応答、セラミック出力コンデンサによる安定性、および入力電圧、負荷、温度に対する 2% 未満の精度を提供します。ソフトスタート・ピンにより、アプリケーションにおける負荷への突入電流を低減できます。さらに、オープン・ドレインのパワー・グッド信号により、電源レールのシーケンシングが可能です。

TPS7A7100 は、3mm × 3mm、16 ピンの VQFN、および 5mm × 5mm、20 ピンの VQFN パッケージで供給されます。

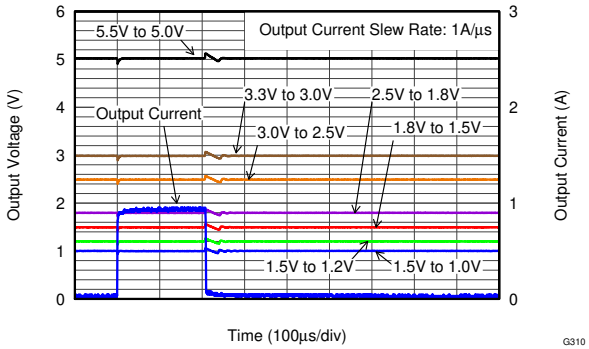
パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
TPS7A7100	RGT (VQFN、16)	3mm × 3mm
	RGW (VQFN、20)	5mm × 5mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路



7 つの異なる出力の負荷過渡応答：$1.5V_{IN}$ から $1V_{OUT}$、$1.5V_{IN}$ から $1.2V_{OUT}$、$1.8V_{IN}$ から $1.5V_{OUT}$、$2.5V_{IN}$ から $1.8V_{OUT}$、$3V_{IN}$ から $2.5V_{OUT}$、$3.3V_{IN}$ から $3V_{OUT}$、$5.5V_{IN}$ から $5V_{OUT}$

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configurations

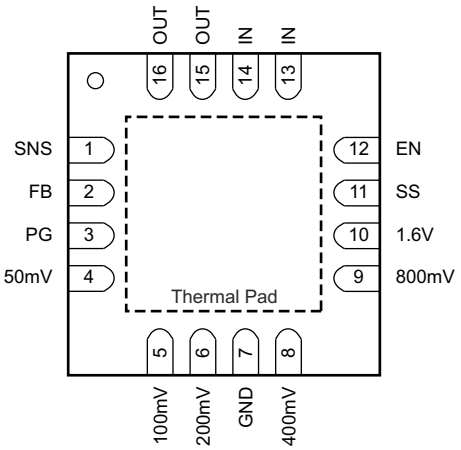


図 4-1. RGT Package, 16-Pin VQFN (Top View)

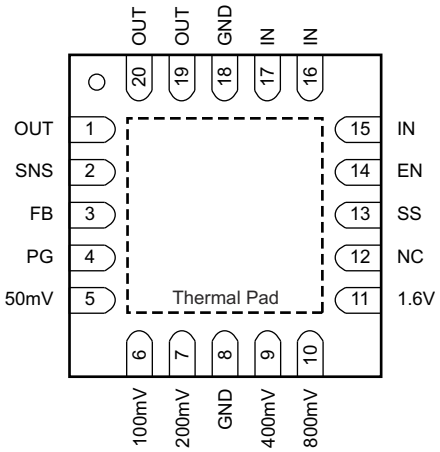


図 4-2. RGW Package, 20-Pin VQFN With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	RGW	RGT		
50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	5, 6, 7, 9, 10, 11	4, 5, 6, 8, 9, 10	I	Output voltage setting pins. These pins must be connected to ground or left floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the *User-Configurable Output Voltage* section for more details.
EN	14	12	I	Enable pin. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. See the *Enable* section for more details.
FB	3	2	I	Output voltage feedback pin. Connected to the error amplifier. See the *User-Configurable Output Voltage* and *Traditional Adjustable Configuration* sections for more details. Connect a 220-pF ceramic capacitor from the FB pin to OUT.
GND	8, 18	7	—	Ground pin.
IN	15, 16, 17	13, 14	I	Unregulated supply voltage pin. Connect an input capacitor to this pin. See the *Input Capacitor Requirements* section for more details.
NC	12	—	—	Not internally connected. The NC pin is not connected to any electrical node. This pin and the thermal pad must be connected to a large-area ground plane. See the *Power Dissipation* section for more details.
OUT	1, 19, 20	15, 16	O	Regulated output pin. A 4.7-µF or larger capacitance is required for stability. See the *Output Capacitor Requirements* section for more details.
PG	4	3	O	Active-high power good pin. An open-drain output that indicates when the output voltage reaches 90% of the target. See the *Power-Good* section for more details.
SNS	2	1	I	Output voltage sense input pin. See the *User-Configurable Output Voltage* and *Traditional Adjustable Configuration* sections for more details.
SS	13	11	—	Soft-start pin. Leaving this pin open provides a soft start of the default setting. Connecting an external capacitor between this pin and ground enables the soft-start function by forming an RC-delay circuit in combination with the integrated resistance on the silicon. See the *Soft-Start* section for more details.
Thermal Pad			—	The thermal pad must be connected to a large-area ground plane. If available, connect an electrically-floating, dedicated thermal plane to the thermal pad as well.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, PG, EN	–0.3	7	V
	SS, FB, SNS, OUT	–0.3	V_{IN} + 0.3(2)	V
	50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	–0.3	V_{OUT} + 0.3(2)	V
Current	OUT	Internally limited		A
	PG (sink current into IC)		5	mA
Temperature	Operating virtual junction, T_J	–55	160	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or +7 V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	1.425		6.5	V
V_{OUT}	Output voltage	0.9		5	V
V_{EN}	Enable voltage	0		6.5	V
V_{PG}	Pullup voltage	0		6.5	V
	Any-out voltage: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	0		V_{OUT}	
I_{OUT}	Output current	0		1	A
C_{OUT}	Output capacitance	4.7		200(1)	µF
C_{FF}	Feedforward capacitance	0		100	nF
T_J	Junction temperature	–40		125	°C

(1) For output capacitors larger than 47 µF a feedforward capacitor of at least 220 pF must be used.

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5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS7A7100(3)		UNIT
		RGW (VQFN)	RGT (VQFN)	
		20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(4)	35.7	44.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(5)	33.6	54.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(6)	15.2	17.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter(7)	0.4	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(8)	15.4	17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(9)	3.8	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) For thermal estimates of this device based on printed-circuit-board (PCB) copper area, see the TI PCB thermal calculator.
(3) Thermal data for the RGW package is derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
   a. i. RGW: The exposed pad is connected to the PCB ground layer through a 4 × 4 thermal via array.
      ii. RGT: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
   b. i. RGW: Both the top and bottom copper layers have a dedicated pattern for 4% copper coverage.
      ii .RGT: Both the top and bottom copper layers have a dedicated pattern for 5% copper coverage.
   c. These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inch × 3-inch copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $R_{\theta JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $R_{\theta JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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5.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), 1.425 V ≤ V_{IN} ≤ 6.5 V, V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V or V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.5 V(1) (2), OUT connected to 50 Ω to GND(4),V_{EN} = 1.1 V, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{FF} = 0 pF (RGW package), C_{FF} = 220 pF (RGT package)(8), and PG pin pulled up to V_{IN} with 100 kΩ, 27 kΩ ≤ R2 ≤ 33 kΩ for adjustable configuration(3) (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		1.425		6.5	V
$V_{(SS)}$	SS pin voltage			0.5		V
V_{OUT}	Output voltage	Adjustable with external feedback resistors	0.9		5	V
		Fixed with voltage setting pins	0.9		3.5	
	Output voltage accuracy(5) (6)	RGT package only, adjustable, –40°C ≤ T_A ≤ 85°C, 25 mA ≤ I_{OUT} ≤ 1 A	–1.5%		1.5%	
		RGT package only, fixed, –40°C ≤ T_A ≤ 85°C, 25 mA ≤ I_{OUT} ≤ 1 A	–2%		2%	
		Adjustable, 25 mA ≤ I_{OUT} ≤ 1 A	–2%		2%	
		Fixed, 25 mA ≤ I_{OUT} ≤ 1 A	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 25 mA		0.01		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	25 mA ≤ I_{OUT} ≤ 1 A		0.1		%/A
$V_{(DO)}$	Dropout voltage (7)	V_{OUT} ≤ 3.3 V, I_{OUT} = 1 A, $V_{(FB)}$ = GND			140	mV
		3.3 V < V_{OUT}, I_{OUT} = 1 A, $V_{(FB)}$ = GND			350	
$I_{(LIM)}$	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = 3.3 V, $V_{OUT(TARGET)}$ = 0.9 V	1.1	1.6		A
$I_{(GND)}$	GND pin current	Full load, I_{OUT} = 1 A		1.8		mA
		Minimum load, V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.9 V, I_{OUT} = 25 mA			4	
		Shutdown, PG = (open), V_{IN} = 6.5 V, $V_{OUT(TARGET)}$ = 0.9 V, $V_{(EN)}$ < 0.5 V		0.1	5	µA
$I_{(EN)}$	EN pin current	V_{IN} = 6.5 V, $V_{(EN)}$ = 0 V and 6.5 V			±0.1	µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)		0		0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1		6.5	V
$V_{IT(PG)}$	PG pin threshold	For the direction PG ↓ with decreasing V_{OUT}	0.85V_{OUT}	0.9V_{OUT}	0.96V_{OUT}	V
$V_{hys(PG)}$	PG pin hysteresis	For PG ↑		0.02V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, $V_{(PG)}$ = 6.5 V			1	µA
$I_{(SS)}$	SS pin charging current	$V_{(SS)}$ = GND, V_{IN} = 3.3 V	3.5	5.1	7.2	µA
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 A		39.57		μV_{RMS}
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

(1) When V_{OUT} ≤ 3.5 V, V_{IN} ≥ (V_{OUT} + 0.3 V) or 1.425 V, whichever is greater; when V_{OUT} > 3.5 V, V_{IN} ≥ (V_{OUT} + 0.5 V).
(2) $V_{OUT(TARGET)}$ is the calculated target V_{OUT} value from the output voltage setting pins: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V in fixed configuration, or the expected V_{OUT} value set by external feedback resistors in adjustable configuration.
(3) R2 is the bottom-side of the feedback resistor between the FB pin and GND. See the *Traditional Adjustable Configuration* section for details.
(4) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(5) When the TPS7A7100 is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(6) The TPS7A7100 is not tested at V_{OUT} = 0.9 V, 2.7 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 1 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package.
(7) $V_{(DO)}$ is not defined for output voltage settings less than 1.2 V.
(8) C_{FF} is the capacitor between FB pin and OUT.

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5.6 Typical Characteristics

at T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with a 100-kΩ pullup resistor (unless otherwise noted)

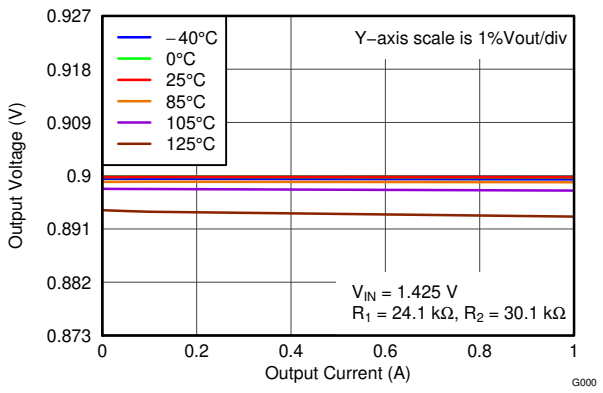


図 5-1. Load Regulation (0.9 V, Adjustable)

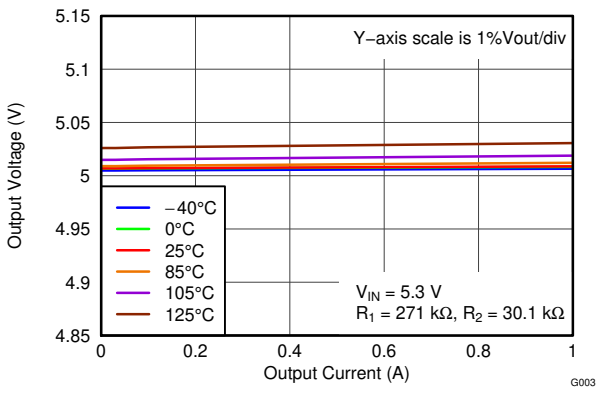


図 5-2. Load Regulation (5 V, Adjustable)

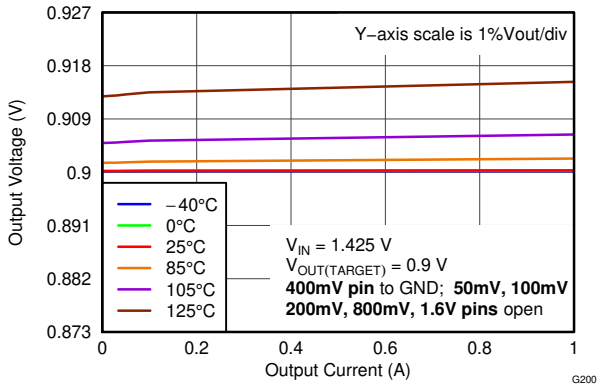


図 5-3. Load Regulation (0.9 V, Fixed By Setting Pins)

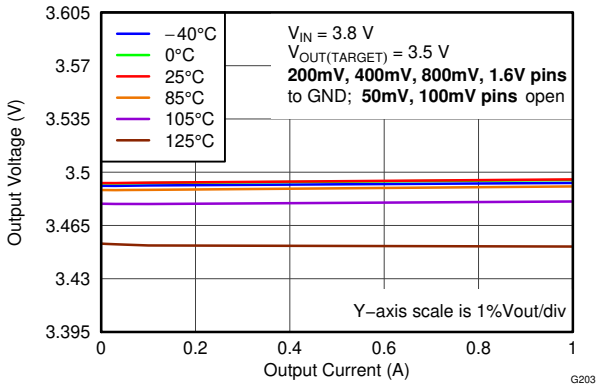


図 5-4. Load Regulation (3.5 V, Fixed By Setting Pins)

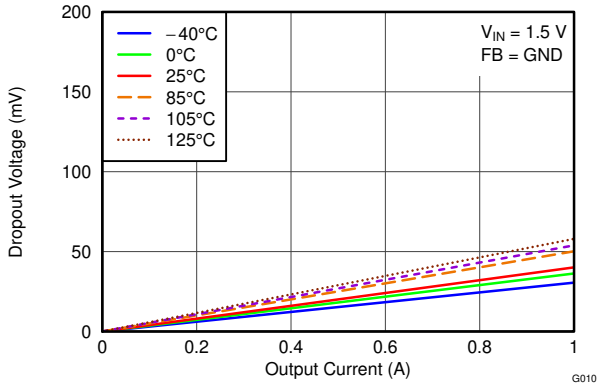


図 5-5. Dropout Voltage vs Output Current

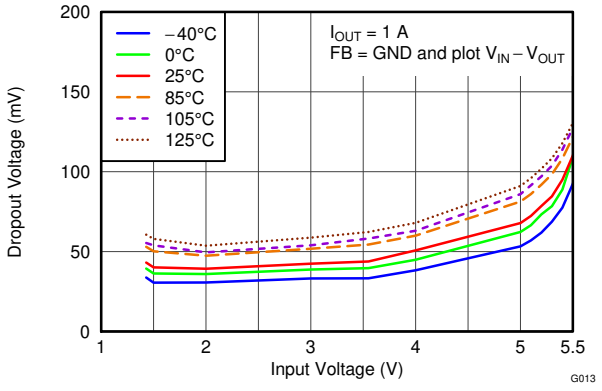


図 5-6. Dropout Voltage vs Temperature

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with a 100-kΩ pullup resistor (unless otherwise noted)

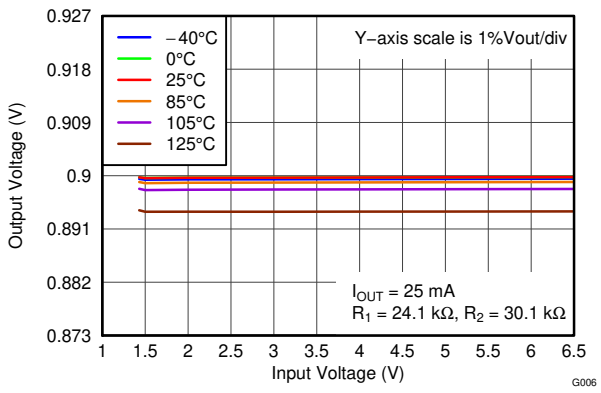


図 5-7. Line Regulation (0.9 V, Adjustable)

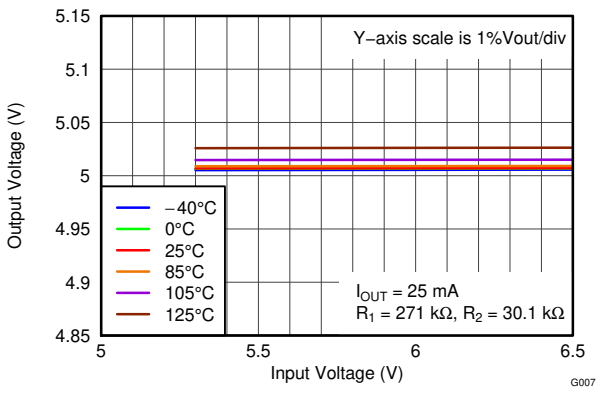


図 5-8. Line Regulation (5 V, Adjustable)

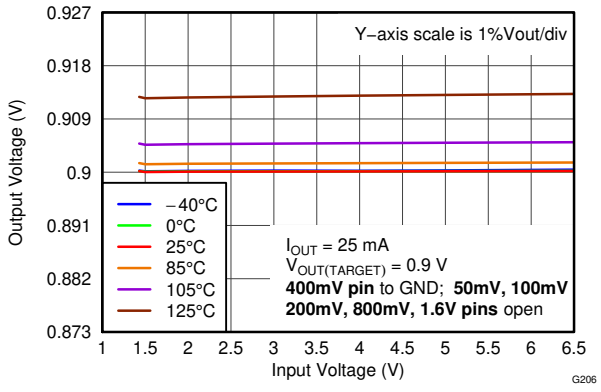


図 5-9. Line Regulation (0.9 V, Fixed By Setting Pins)

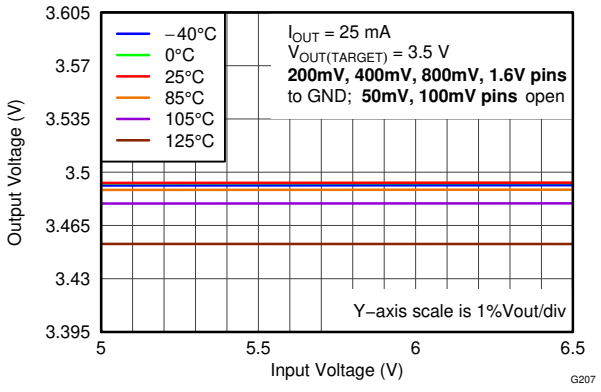


図 5-10. Line Regulation (3.5 V, Fixed By Setting Pins)

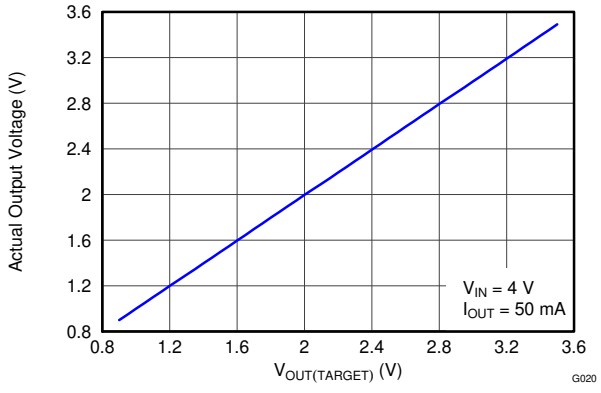


図 5-11. Measured Output Voltage vs Pin Setting

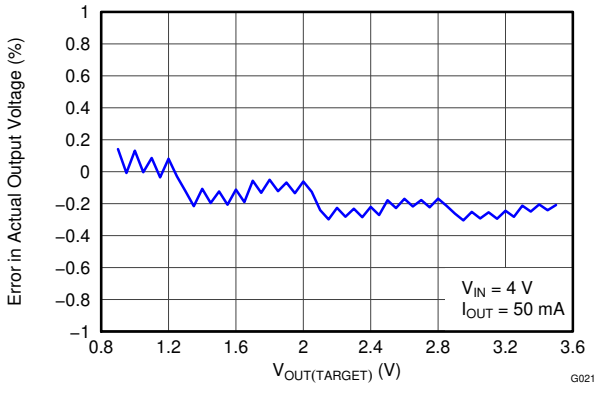


図 5-12. Accuracy vs Pin Setting

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with a 100-kΩ pullup resistor (unless otherwise noted)

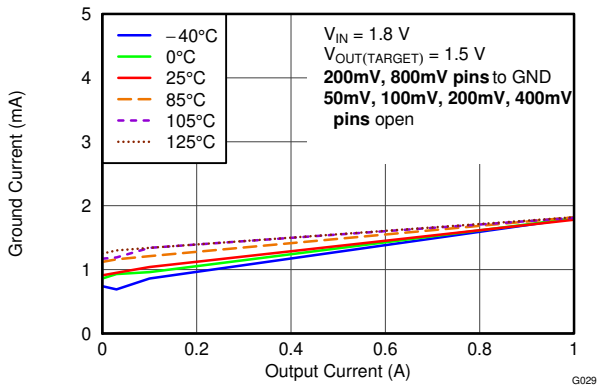


図 5-13. GND Pin Current vs Output Current

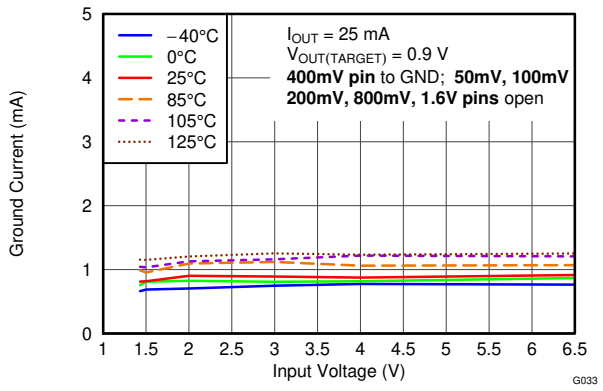


図 5-14. GND Pin Current vs Input Voltage

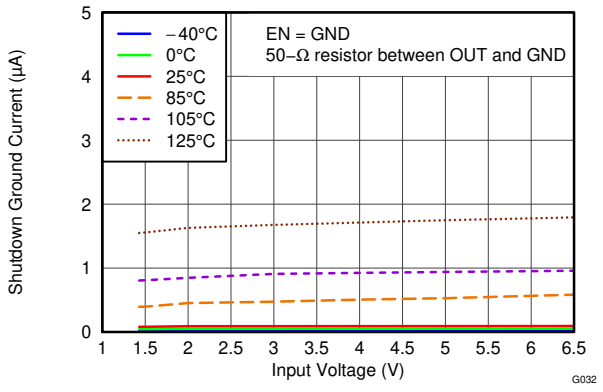


図 5-15. GND Pin Current In Shutdown vs Temperature

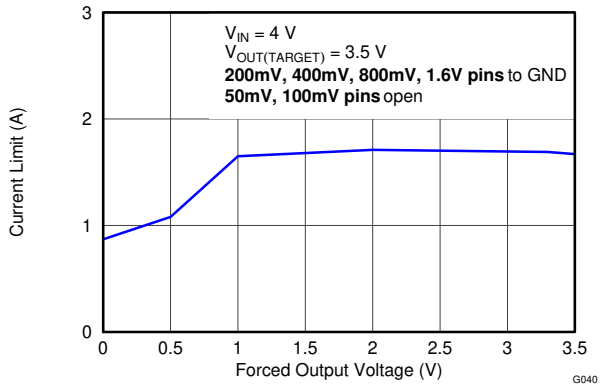


図 5-16. Current Limit vs Output Voltage (Foldback)

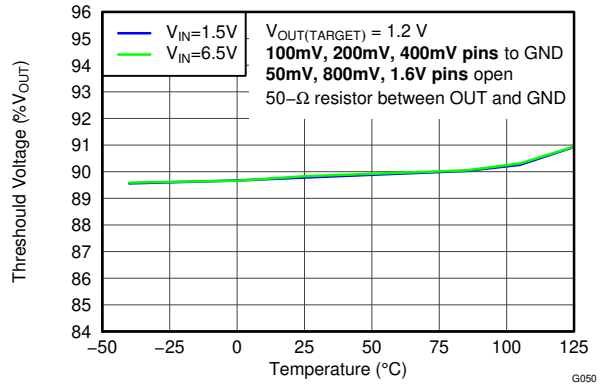


図 5-17. Power-Good Threshold Voltage vs Temperature

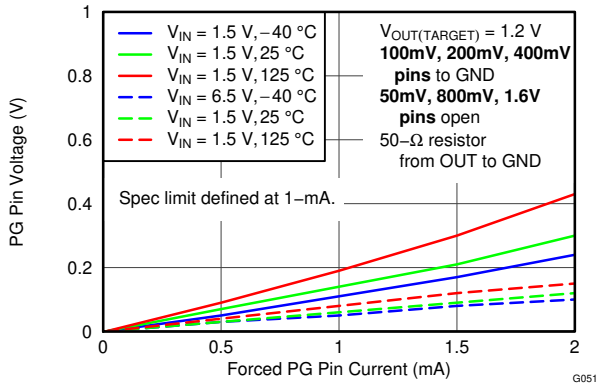


図 5-18. Power-Good Pin Drive Capability

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(TARGET)}$ + 0.3 V, I_{OUT} = 25 mA, $V_{(EN)}$ = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{(SS)}$ = 10 nF, and the PG pin pulled up to V_{IN} with a 100-kΩ pullup resistor (unless otherwise noted)

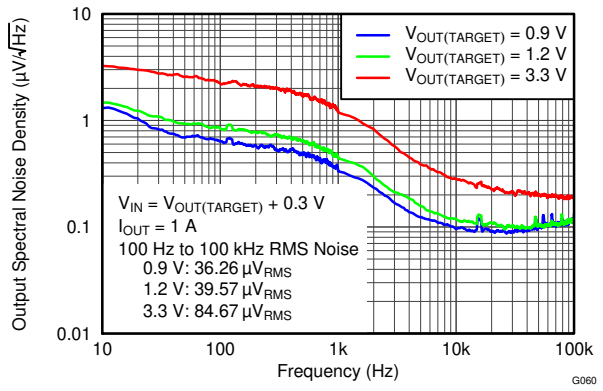


図 5-19. Noise Spectral Density By Output Voltage

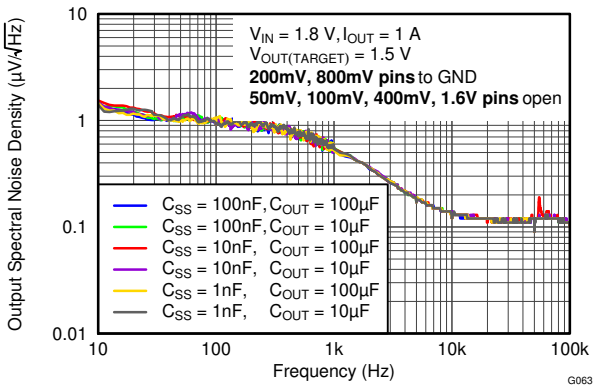


図 5-20. Noise Spectral Density By External Capacitors

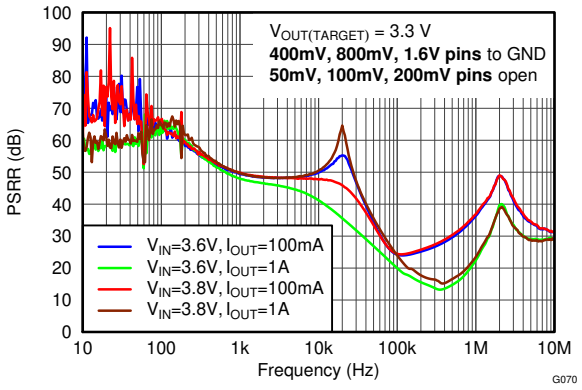


図 5-21. Power-Supply Ripple Rejection vs Frequency

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6 Detailed Description

6.1 Overview

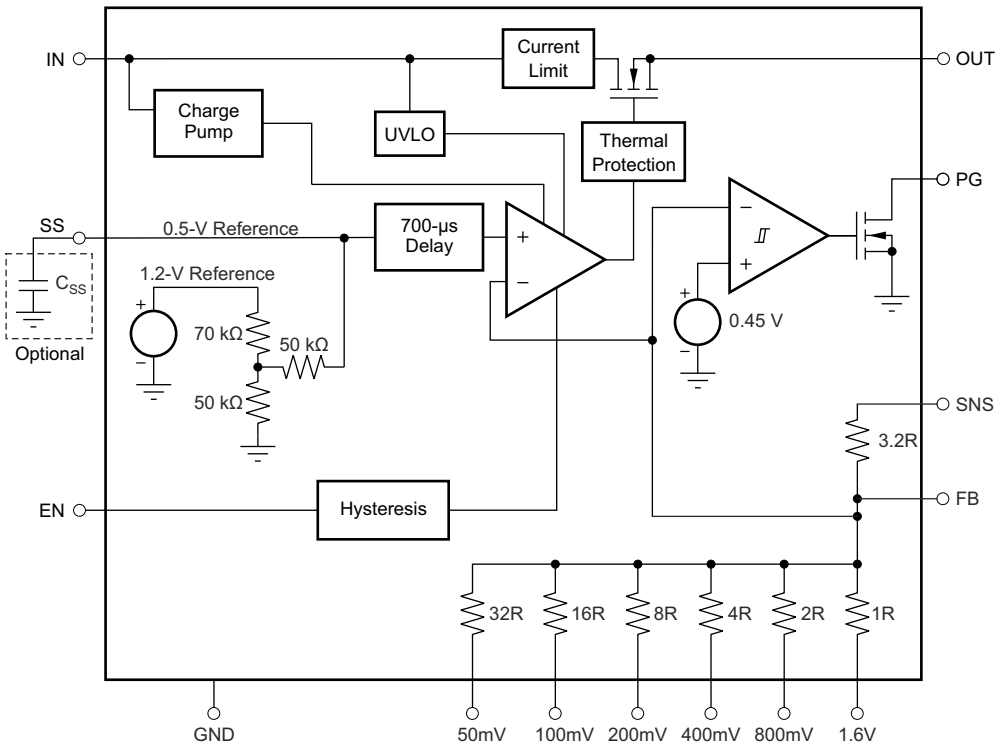
The TPS7A7100 is a low-dropout (LDO) regulator that uses innovative circuitry to offer very low dropout voltage along with the flexibility of a programmable output voltage.

The dropout voltage for this LDO regulator is 0.14 V at 1 A. This voltage is makes the TPS7A7100 into a point-of-load (POL) regulator because 0.14 V at 1 A is lower than any voltage gap among the most common voltage rails: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3 V, and 3.3 V. This device offers a fully user-configurable output voltage setting method. The TPS7A7100 output voltage can be programmed to any target value from 0.9 V to 3.5 V in 50-mV steps.

Another big advantage of using the TPS7A7100 is the wide range of available operating input voltages: from 1.5 V to 6.5 V. The TPS7A7100 also has very good line and load transient response. All these features allow the TPS7A7100 to meet most voltage-regulator needs for under 6-V applications, using only one device so less time is spent on inventory control.

Texas Instruments also offers different output current ratings with other family devices: the TPS7A7200 (2 A) and TPS7A7300 (3 A).

6.2 Functional Block Diagram



NOTE: 32R = 1.024 MΩ (that is, 1R = 32 kΩ).

6.3 Feature Description

6.3.1 User-Configurable Output Voltage

Unlike traditional LDO devices, the TPS7A7100 comes with only one orderable part number. There is no adjustable or fixed output voltage option. The output voltage of the TPS7A7100 is selectable in accordance with the names given to the output voltage setting pins: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V. For each pin connected to the ground, the output voltage setting increases by the value associated with that pin name, starting from the value of the reference voltage of 0.5 V. Floating the pins has no effect on the output voltage. 図 6-1 through 図 6-6 show examples of how to program the output voltages.

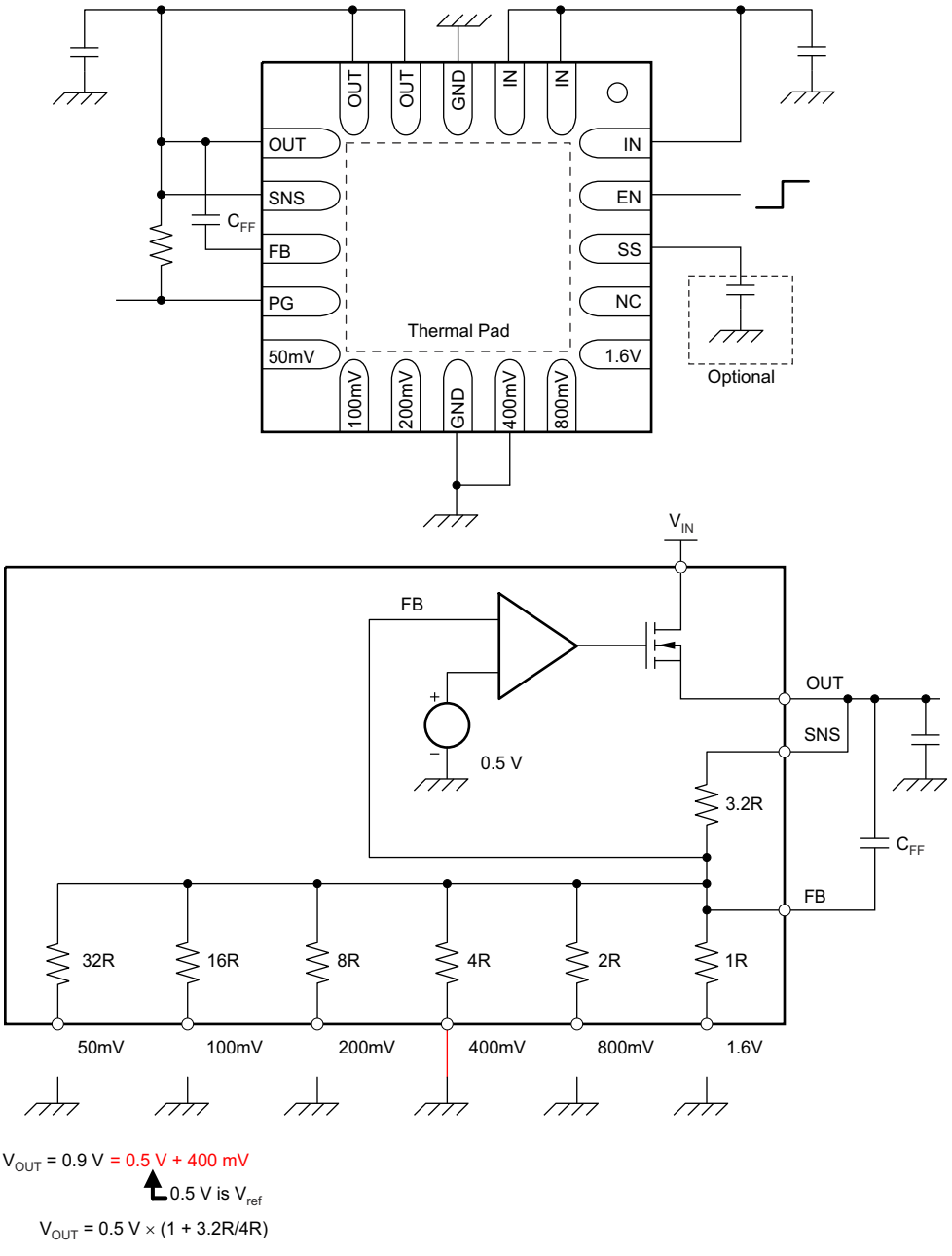
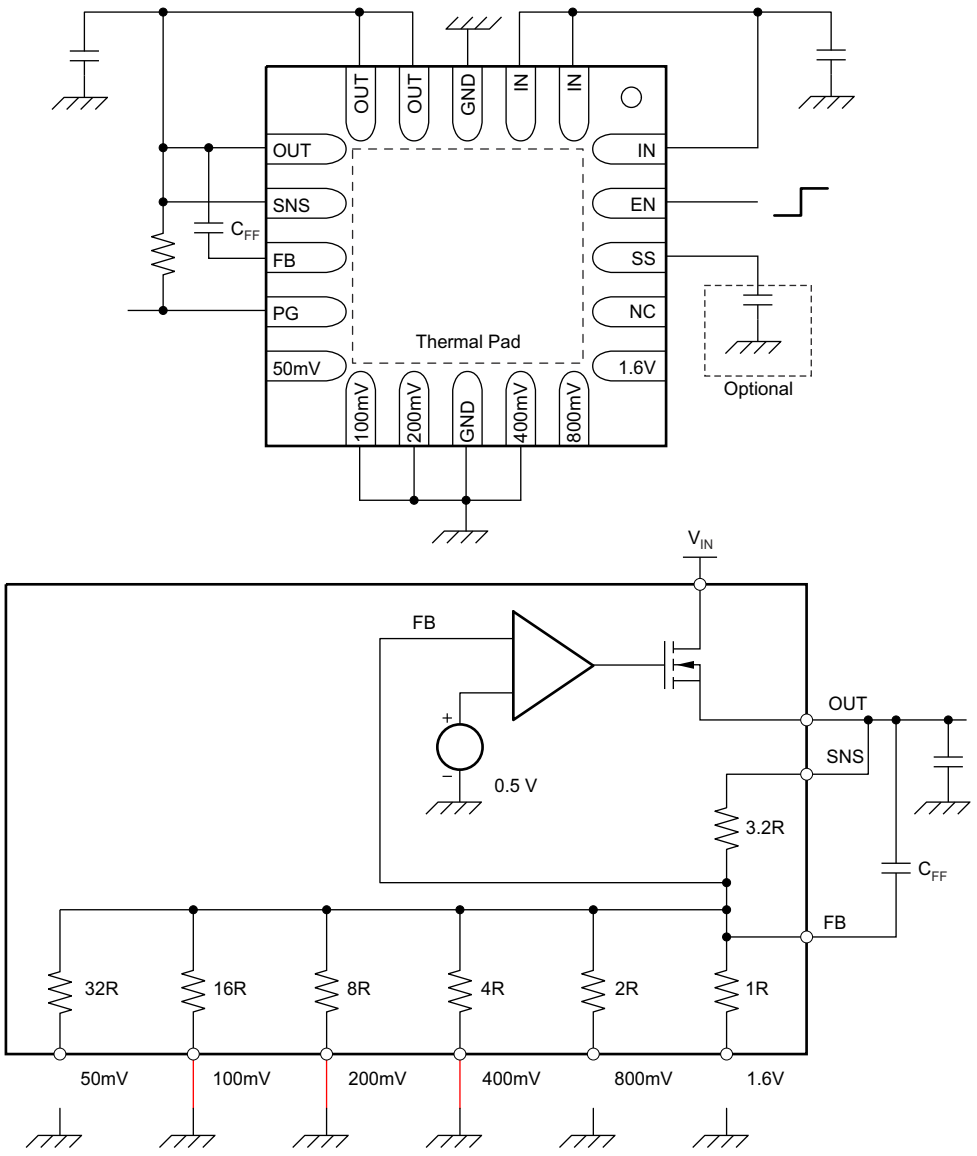


図 6-1. 0.9-V Configuration

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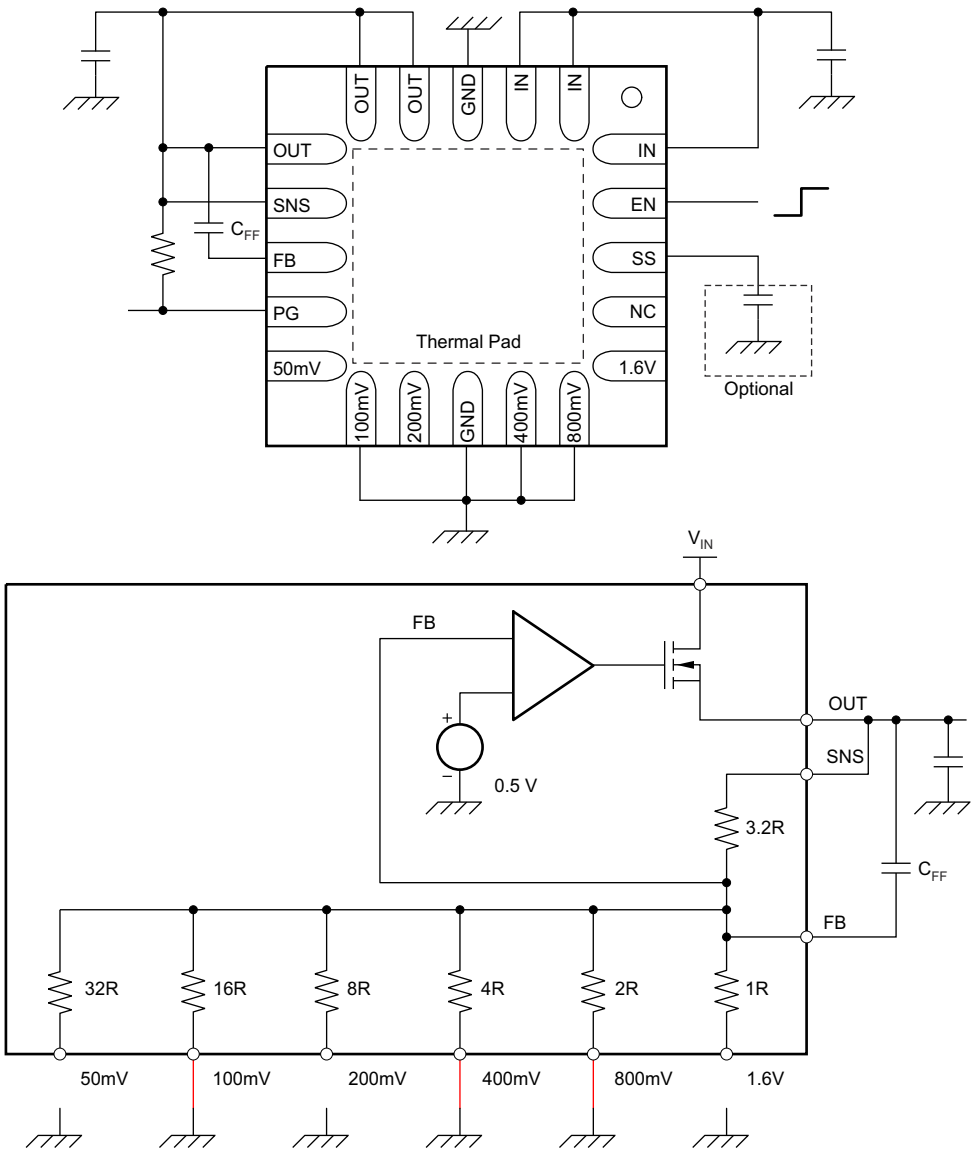


V_{OUT} = 1.2 V = 0.5 V + 100 mV + 200 mV + 400 mV

0.5 V is V_{ref}

V_{OUT} = 0.5 V × (1 + 3.2R/2.29R) 2.29R is parallel resistance of 16R, 8R, and 4R.

図 6-2. 1.2-V Configuration



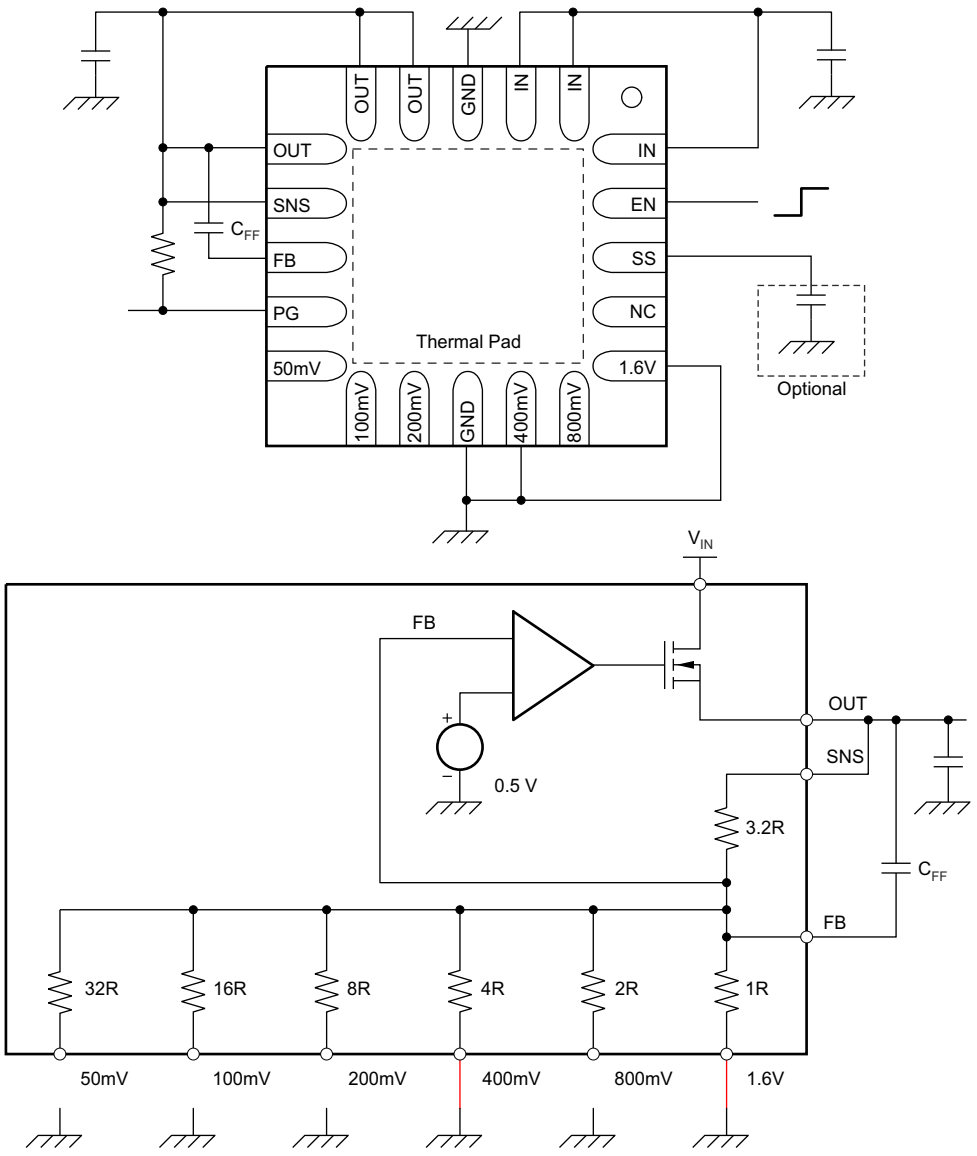
V_{OUT} = 1.8 V = 0.5 V + 100 mV + 400 mV + 800 mV

0.5 V is V_{ref}

V_{OUT} = 0.5 V × (1 + 3.2R/1.23R) 1.23R is parallel resistance of 16R, 4R, and 2R.

図 6-3. 1.8-V Configuration

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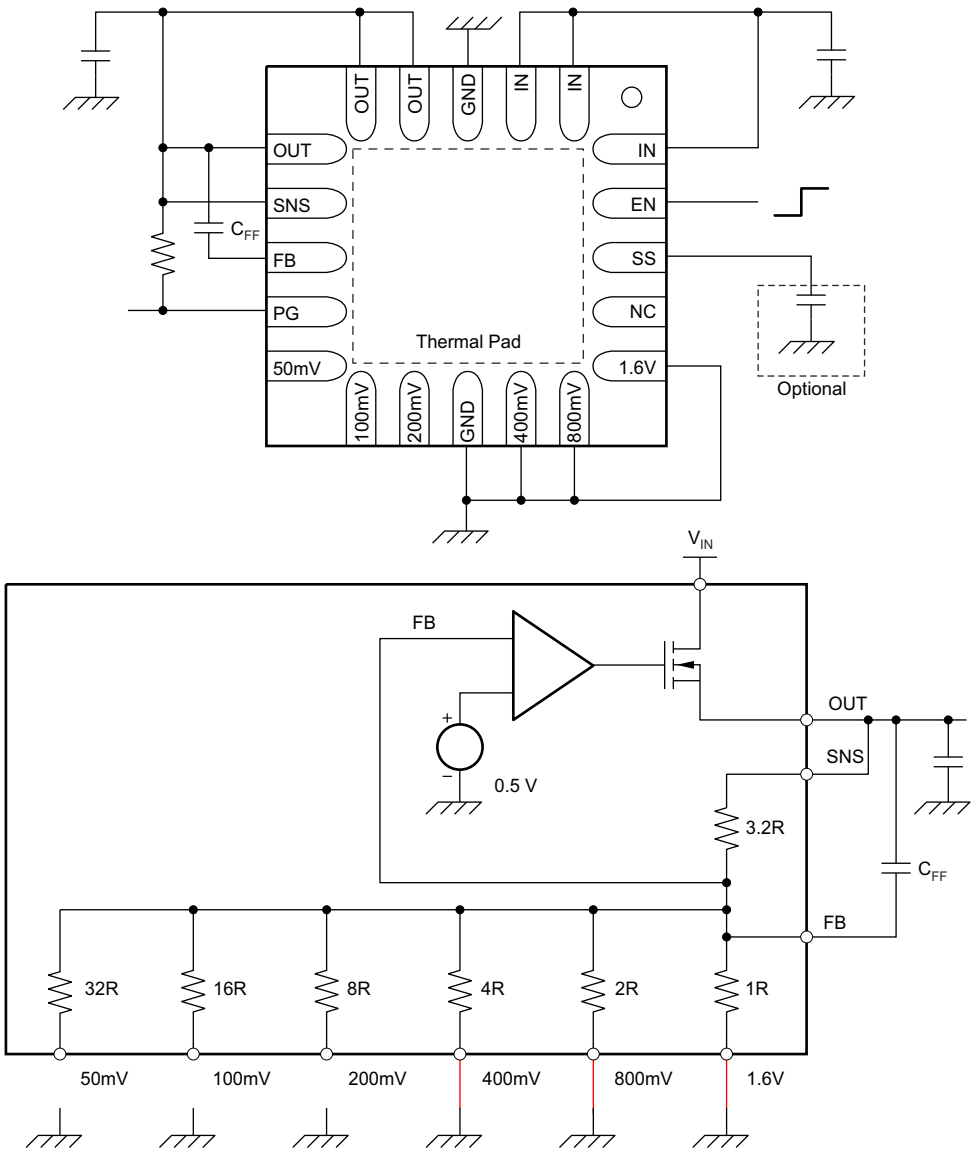


V_{OUT} = 2.5 V = 0.5 V + 400 mV + 1.6 V

0.5 V is V_{ref}

V_{OUT} = 0.5 V × (1 + 3.2R/0.8R) 0.8R is parallel resistance of 4R and 1R.

図 6-4. 2.5-V Configuration



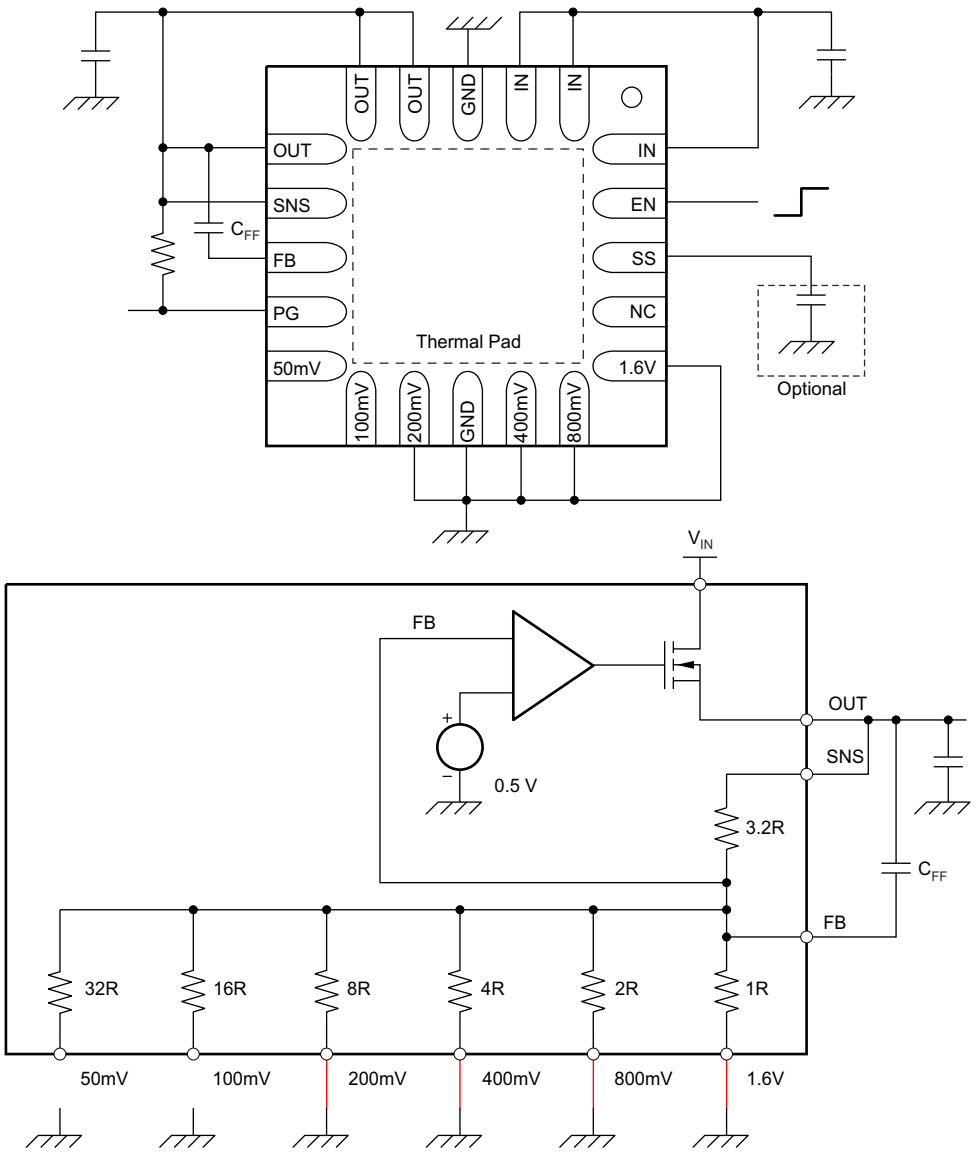
V_{OUT} = 3.3 V = 0.5 V + 400 mV + 800 mV + 1.6 V

0.5 V is V_{ref}

V_{OUT} = 0.5 V × (1 + 3.2R/0.571R) 0.571R is parallel resistance of 4R, 2R, and 1R.

図 6-5. 3.3-V Configuration

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V_{OUT} = 3.5 V = 0.5 V + 200 mV + 400 mV + 800 mV + 1.6 V

0.5 V is V_{ref}

$V_{OUT} = 0.5\ V \times (1 + 3.2R/0.533R)$ 0.533R is parallel resistance of 8R, 4R, 2R, and 1R.

図 6-6. 3.5-V Configuration

See 表 6-1 for a full list of target output voltages and corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.9 V to 3.5 V in 50-mV steps.

図 5-11 and 図 5-12 illustrate this output voltage programming performance.

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注

Any output voltage setting that is not listed in 表 6-1 is not covered in the *Electrical Characteristics* . For output voltages greater than 3.5 V, use a traditional adjustable configuration (see the *Traditional Adjustable Configuration* section).

表 6-1. User Configurable Output Voltage Setting

$V_{OUT(TARGET)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
0.9	open	open	open	GND	open	open
0.95	GND	open	open	GND	open	open
1	open	GND	open	GND	open	open
1.05	GND	GND	open	GND	open	open
1.1	open	open	GND	GND	open	open
1.15	GND	open	GND	GND	open	open
1.2	open	GND	GND	GND	open	open
1.25	GND	GND	GND	GND	open	open
1.3	open	open	open	open	GND	open
1.35	GND	open	open	open	GND	open
1.4	open	GND	open	open	GND	open
1.45	GND	GND	open	open	GND	open
1.5	open	open	GND	open	GND	open
1.55	GND	open	GND	open	GND	open
1.6	open	GND	GND	open	GND	open
1.65	GND	GND	GND	open	GND	open
1.7	open	open	open	GND	GND	open
1.75	GND	open	open	GND	GND	open
1.8	open	GND	open	GND	GND	open
1.85	GND	GND	open	GND	GND	open
1.9	open	open	GND	GND	GND	open
1.95	GND	open	GND	GND	GND	open
2	open	GND	GND	GND	GND	open
2.05	GND	GND	GND	GND	GND	open
2.1	open	open	open	open	open	GND
2.15	GND	open	open	open	open	GND
2.2	open	GND	open	open	open	GND
2.25	GND	GND	open	open	open	GND
2.3	open	open	GND	open	open	GND
2.35	GND	open	GND	open	open	GND
2.4	open	GND	GND	open	open	GND
2.45	GND	GND	GND	open	open	GND
2.5	open	open	open	GND	open	GND
2.55	GND	open	open	GND	open	GND
2.6	open	GND	open	GND	open	GND
2.65	GND	GND	open	GND	open	GND
2.7	open	open	GND	GND	open	GND
2.75	GND	open	GND	GND	open	GND
2.8	open	GND	GND	GND	open	GND
2.85	GND	GND	GND	GND	open	GND
2.9	open	open	open	open	GND	GND

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表 6-1. User Configurable Output Voltage Setting (続き)

$V_{OUT(TARGET)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
2.95	GND	open	open	open	GND	GND
3	open	GND	open	open	GND	GND
3.05	GND	GND	open	open	GND	GND
3.1	open	open	GND	open	GND	GND
3.15	GND	open	GND	open	GND	GND
3.2	open	GND	GND	open	GND	GND
3.25	GND	GND	GND	open	GND	GND
3.3	open	open	open	GND	GND	GND
3.35	GND	open	open	GND	GND	GND
3.4	open	GND	open	GND	GND	GND
3.45	GND	GND	open	GND	GND	GND
3.5	open	open	GND	GND	GND	GND

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6.3.2 Traditional Adjustable Configuration

For any output voltage target that is not supported in the *User-Configurable Output Voltage* section, a traditional adjustable configuration with external-feedback resistors can be used with the TPS7A7100. 図 6-7 shows how to configure the TPS7A7100 as an adjustable regulator with an equation and 表 6-2 lists recommended pairs of feedback resistor values.

注

The bottom side of feedback resistor R2 in 図 6-7 must be in the range of 27 kΩ to 33 kΩ to maintain the specified regulation accuracy.

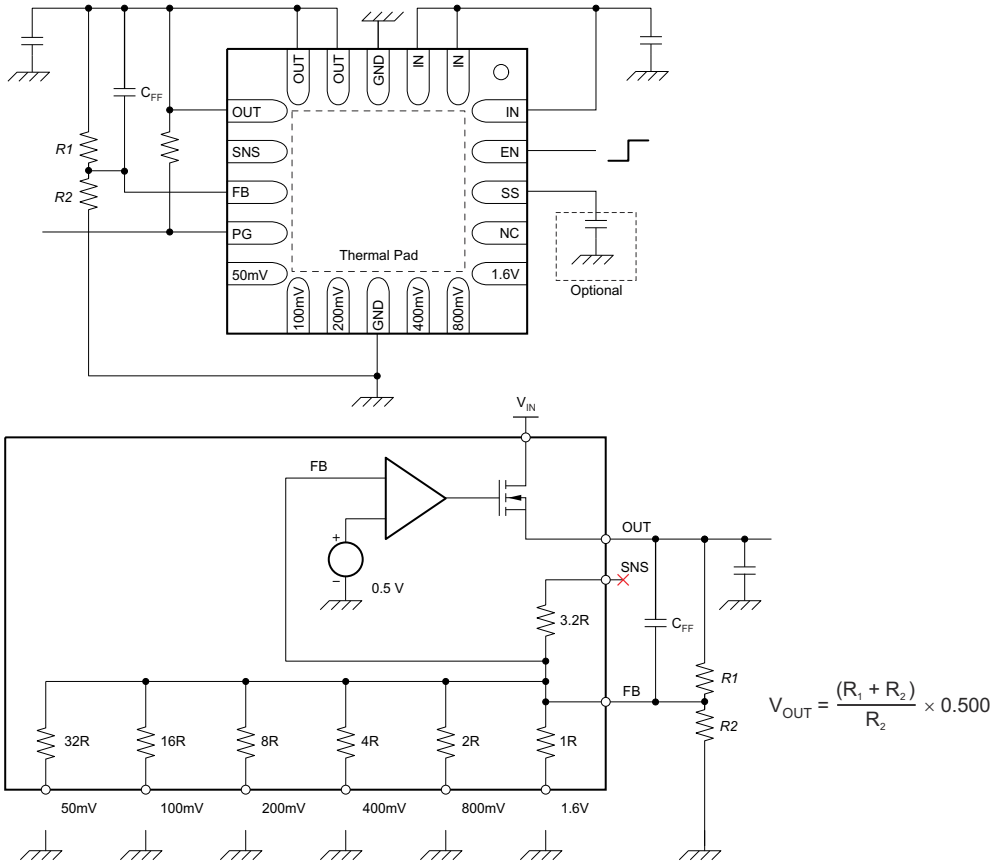


図 6-7. Traditional Adjustable Configuration With External Resistors

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表 6-2. Recommended Feedback-Resistor Values

$V_{OUT(TARGET)}$ (V)	E96 SERIES		R40 SERIES	
	R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	R2 (kΩ)
1	30.1	30.1	30	30
1.2	39.2	28	43.7	31.5
1.5	61.9	30.9	60	30
1.8	80.6	30.9	80	30.7
1.9	86.6	30.9	87.5	31.5
2.5	115	28.7	112	28
3	147	29.4	150	30
3.3	165	29.4	175	31.5
5	280	30.9	243	27.2

6.3.3 Undervoltage Lockout (UVLO)

The TPS7A7100 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature that typically ignores undershoot of the input voltage upon the event of device start-up. Still, a poor input line impedance can cause a severe input voltage drop when the device powers on. As explained in the *Input Capacitor Requirements* section, the input line impedance must be well-designed.

6.3.4 Soft-Start

The TPS7A7100 has an SS pin that provides a soft-start (slow start) function.

By leaving the SS pin open, the TPS7A7100 performs a soft-start by default.

As shown in the *Functional Block Diagram*, by connecting a capacitor between the SS pin and ground, the C_{SS} capacitor forms an RC pair together with the integrated 50-kΩ resistor. The RC pair operates as an RC-delay circuit for the soft-start with the internal 700-µs delay circuit.

The relationship between C_{SS} and the soft-start time is illustrated in the *Application Curves*.

6.3.5 Current Limit

The TPS7A7100 internal current limit circuitry protects the regulator during fault conditions. During a current limit event, the output sources a fixed amount of current that is mostly independent of the output voltage. The current limit function is provided as a fail-safe mechanism and is not intended to be used regularly. Do **not** design any applications to use this current-limit function as a part of expected normal operation. Extended periods of current-limit operation degrade device reliability.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, can result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps mitigate the load transient requirement of the upstream supply during these events.

6.3.6 Enable

The EN pin switches the enable and disable (shutdown) states of the TPS7A7100. A logic high input at the EN pin enables the device; a logic low input disables the device. When disabled, the device current consumption is reduced.

6.3.7 Power-Good

The TPS7A7100 has a power-good function that works with the PG output pin. When the output voltage undershoots the threshold voltage $V_{IT(PG)}$ during normal operation, the PG open-drain output turns from a high-impedance state to a low-impedance state. When the output voltage exceeds the $V_{IT(PG)}$ threshold by an amount

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greater than the PG hysteresis, $V_{hys(PG)}$, the PG open-drain output turns from a low-impedance state to high-impedance state. By connecting a pullup resistor (usually between the OUT and PG pins), any downstream device can receive an active-high enable logic signal.

When setting the output voltage to less than 1.8 V and using a pullup resistor between OUT and PG pins, depending on the downstream device specifications, the downstream device can possibly be unable to accept the PG output as a valid high-level logic voltage. In such cases, place a pullup resistor between the IN and PG pins, not between the OUT and PG pins.

図 5-18 illustrates the open-drain output drive capability. The on-resistance of the open-drain transistor is calculated using 図 5-18, and is approximately 200 Ω. Any pullup resistor greater than 10 kΩ works fine for this purpose.

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6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(MIN)}$
- The input voltage is greater than the nominal output voltage added to the dropout voltage
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

表 6-3 lists the conditions that lead to the different modes of operation.

表 6-3. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(NOM)} + V_{DO}$ and $V_{IN} > V_{IN(MIN)}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{(LIM)}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{IL(EN)}$	—	$T_J > 160°C$

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7 Application and Implementation

注

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7.1 Application Information

The TPS7A7100 is a very-low dropout LDO with very fast load transient response. The TPS7A7100 provides a number of features (such as a power-good signal for output monitoring and a soft-start pin to reduce inrush currents during start-up), and the device is designed for applications that require up to 1 A of output current.

7.2 Typical Application

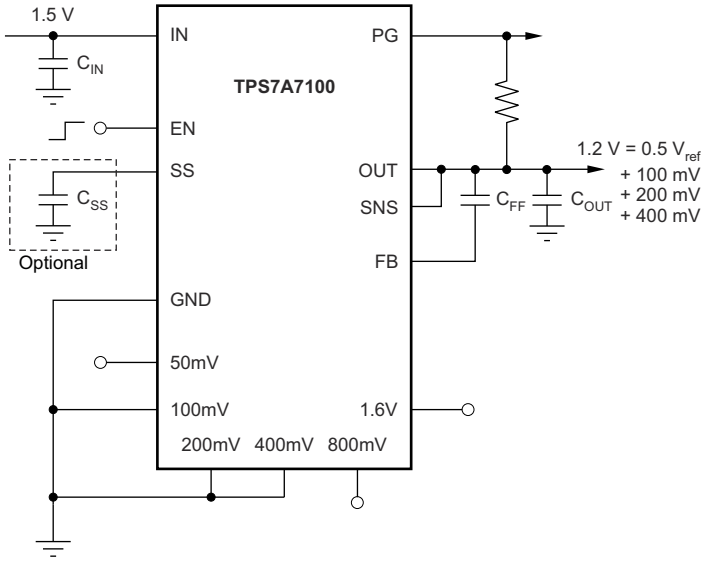


図 7-1. 1.2-V Output Using ANY-OUT Pins

7.2.1 Design Requirements

表 7-1 lists the design parameters for this example.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.425 V to 6.5 V
Output voltage	1.2 V
Output current rating	1 A
Output capacitor range	4.7 µF to 200 µF
feedforward capacitor range	220 pF to 100 nF
Soft-start capacitor range	0 µF to 1 µF

7.2.2 Detailed Design Procedure

7.2.2.1 ANY-OUT Programmable Output Voltage

For ANY-OUT operation, the TPS7A7100 does not use any external resistors to set the output voltage, but uses device pins labeled 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V to set the regulated output voltage. Each pin is either connected to ground (active) or is left open (floating). The ANY-OUT programming is set as the

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sum of the internal reference voltage ($V_{(SS)}$ = 0.5 V) plus the sum of the respective voltages assigned to each active pin. By leaving all ANY-OUT pins open, or floating, the output is set to the minimum possible output voltage equal to $V_{(SS)}$. By grounding all of the ANY-OUT pins, the output is set to 3.65 V.

When using the ANY-OUT pins, the SNS pin must always be connected between the OUT and FB pins. However, the feedforward capacitor must be connected to the FB pin, not the SNS pin.

7.2.2.2 Traditional Adjustable Output Voltage

For applications that need the regulated output voltage to be greater than 3.65 V (or those that require more resolution than the 50 mV that the ANY-OUT pins provide), the TPS7A7100 can also be use the traditional adjustable method of setting the regulated output.

When using the traditional method of setting the output, the FB pin must be connected to the node connecting the top and bottom resistors of the resistor divider. The SNS pin must be left floating.

7.2.2.3 Input Capacitor Requirements

As a result of the very fast transient response and low-dropout operation support, the line impedance must be reduced at the input pin of the TPS7A7100. The line impedance depends heavily on various factors, such as wire (PCB trace) resistance, wire inductance, and output impedance of the upstream voltage supply (power supply to the TPS7A7100). Therefore, a specific value for the input capacitance cannot be recommended until the previously listed factors are finalized.

In addition, simple usage of large input capacitance can form an unwanted LC resonance in combination with input wire inductance. For example, a 5-nH inductor and a 10-µF input capacitor form an LC filter that has a resonance at 712 kHz. This value of 712 kHz is well inside the bandwidth of the TPS7A7100 control loop.

The best guideline is to use a capacitor of up to 1 µF with well-designed wire connections (PCB layout) to the upstream supply. If optimizing the input line is difficult, use a large tantalum capacitor in combination with a good-quality, low-ESR, 1-µF ceramic capacitor.

7.2.2.4 Output Capacitor Requirements

The TPS7A7100 is designed to be stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF without a feedforward capacitor. For output capacitors from 47 µF to 200 µF a feedforward capacitor of at least 220 pF must be used. The TPS7A7100 is evaluated using an X5R-type, 10-µF ceramic capacitor. Use X5R- and X7R-type capacitors because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

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7.2.3 Application Curves

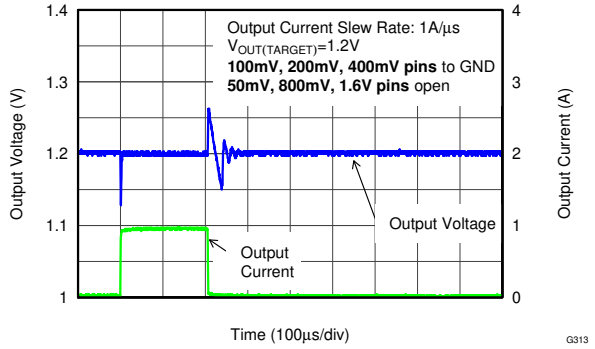


図 7-2. Load Transient Response (V_{OUT} = 1.2 V)

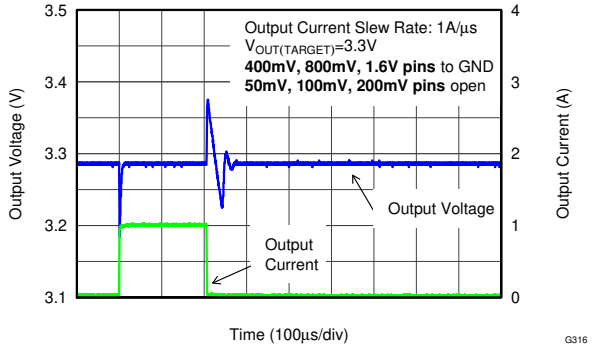


図 7-3. Load Transient Response (V_{OUT} = 3.3 V)

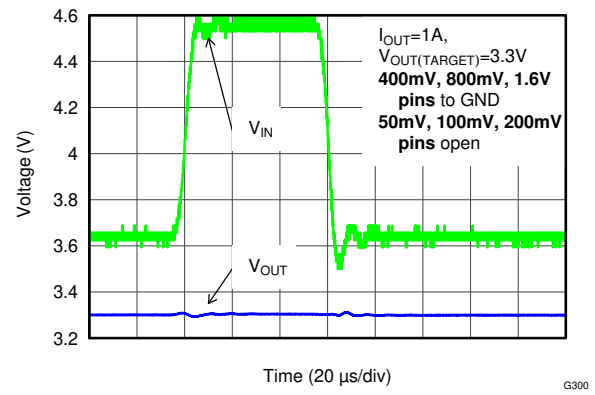


図 7-4. Line Transient Response

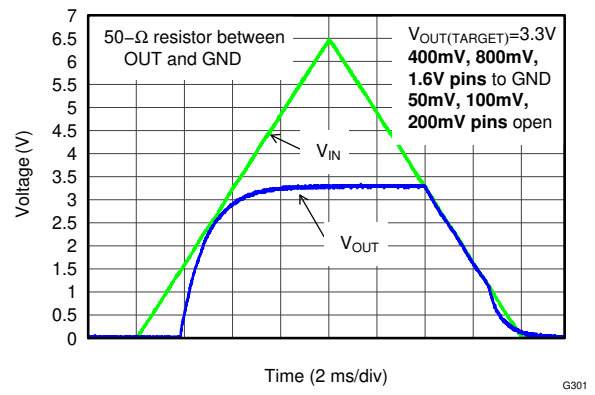


図 7-5. Power Up and Power Down (IN = EN)

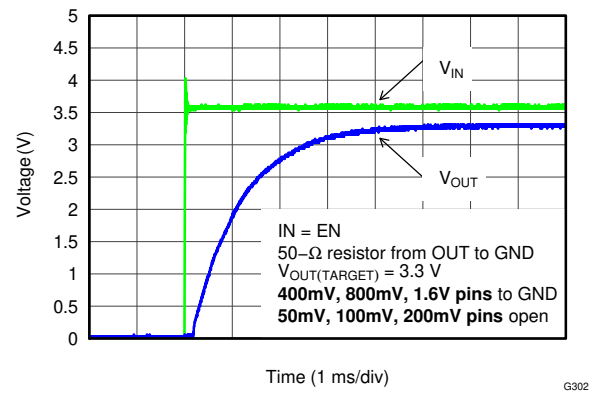


図 7-6. Turnon Response (IN = EN)

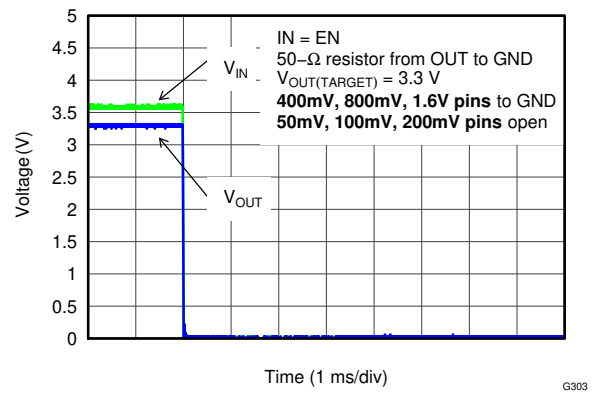


図 7-7. Turnoff Response (IN = EN)

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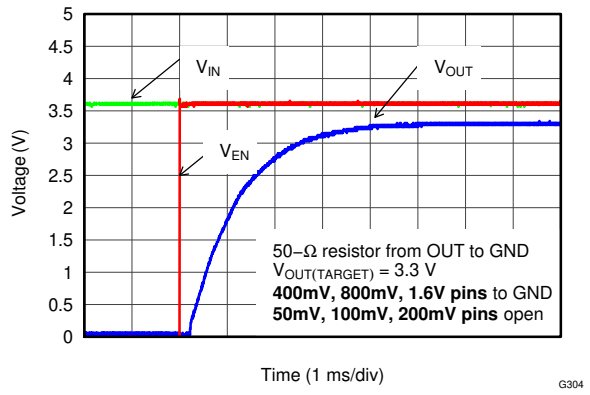


図 7-8. EN Pulse On Response (Over Stable V_{IN})

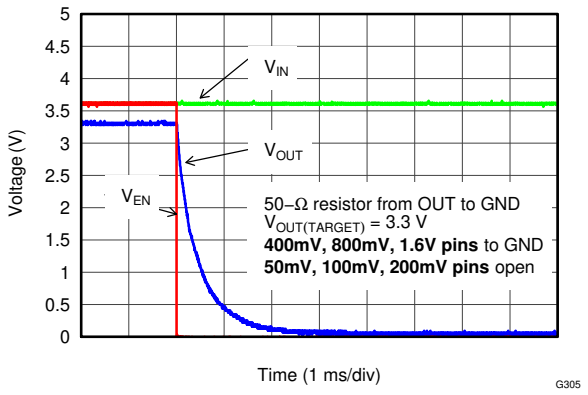


図 7-9. EN Pulse Off Response (Over Stable V_{IN})

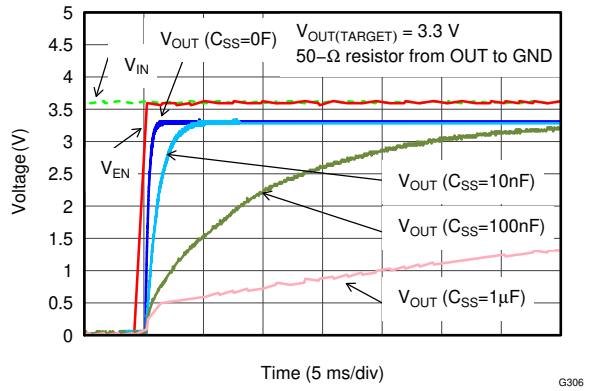


図 7-10. Soft-Start Delay vs C_{SS} (Enlarged View)

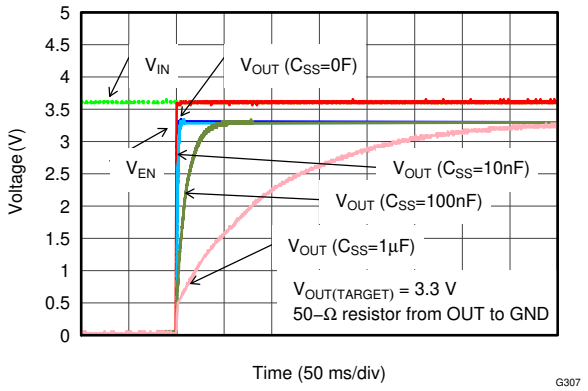


図 7-11. Soft-Start Delay vs C_{SS} (Reduced View)

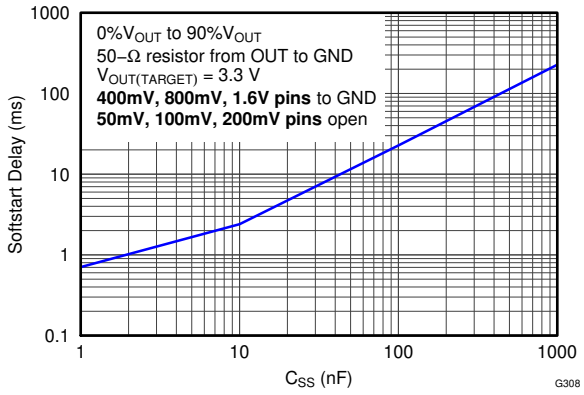


図 7-12. Soft-Start Delay vs C_{SS}

7.3 Power Supply Recommendations

This device is designed for operation from an input voltage supply ranging from 1.425 V to 6.5 V. This input supply must be well regulated. The TPS7A7100 fast-transient, low-dropout linear regulator achieves stability with a minimum output capacitance of 4.7 µF; however, use 10-µF ceramic capacitors for both the input and output to maximize AC performance.

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7.4 Layout

7.4.1 Layout Guidelines

- To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device.
- In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.
- Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability.
- Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.
- Do **not** place any of the capacitors on the opposite side of the PCB from where the regulator is installed.
- The use of vias and long traces is strongly discouraged because these components can impact system performance negatively and even cause instability.
- If possible, and to provide the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A7100 evaluation board, see the *TPS7A7x00EVM-718 Evaluation Module* user guide.

7.4.1.1 Thermal Considerations

The thermal protection feature disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal-protection circuit can cycle on and off. This thermal limit protects the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest-expected ambient temperature and worst-case load.

The internal-protection circuitry of the TPS7A7100 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A7100 into thermal shutdown degrades device reliability.

7.4.1.2 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and providing reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using 式 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW or RGT) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or be left floating; however, the pad must be attached to an appropriate amount of copper PCB area to make sure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using 式 2:

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$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \quad (2)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 図 7-13.

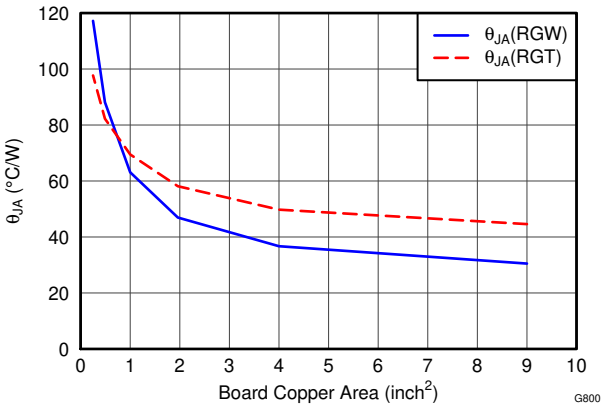


図 7-13. $R_{\theta JA}$ vs Board Size

図 7-13 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and must not be used to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, Ψ_{JT} and Ψ_{JB} must be used as explained in the *Estimating Junction Temperature* section.

7.4.1.3 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as listed in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 式 3). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \quad (3)$$

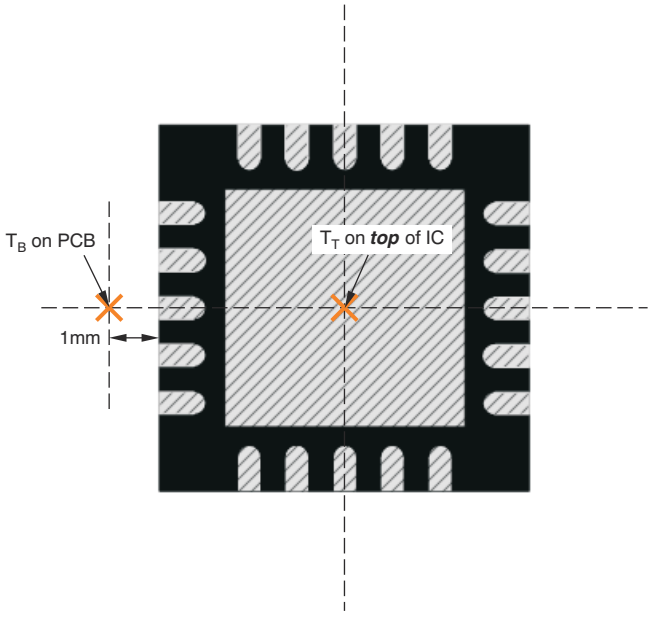
where:

- P_D is the power dissipation shown by 式 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB temperature measured 1 mm away from the device package *on the PCB surface* (see 図 7-14)

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note.



(a) Example RGW (QFN) Package Measurement

図 7-14. Measuring Points For T_T and T_B

From 図 7-15, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) are shown to have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with 式 3 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

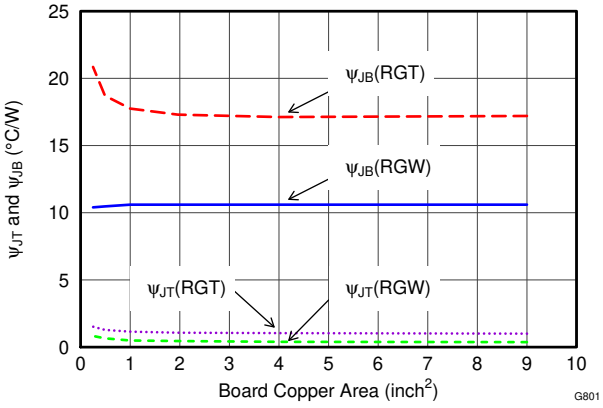
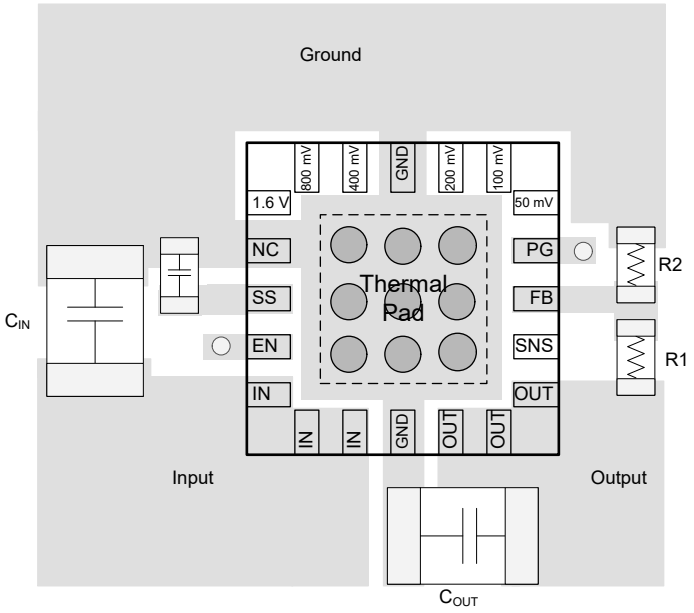


図 7-15. Ψ_{JT} And Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note.

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7.4.2 Layout Example



Notes: C_{in} and C_{out} are 0805 packages
C_{SS}, R_1, and R_2 are 0402 packages
R_1 and R_2 only needed for adjustable operation
○Denotes a via to a connection made on another layer

図 7-16. TPS7A7100 Recommended Layout

8 Device And Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *TPS7A7x00EVM-718 Evaluation Module* user guide
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from October 4, 2023 to October 30, 2023 (from Revision F (September 2015) to Revision G (October 2023)) — **Page**

- 「アプリケーション」セクションにリンクを追加 1
- Changed SS and EN position in *Layout Example* to match device pinout 31

Changes from Revision E (September 2013) to Revision F (September 2015) — **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1

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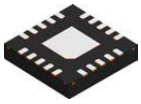
- Changed name of section from *Enable and Shutdown the Device* to *Enable* 21

10 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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10.1 Mechanical Data

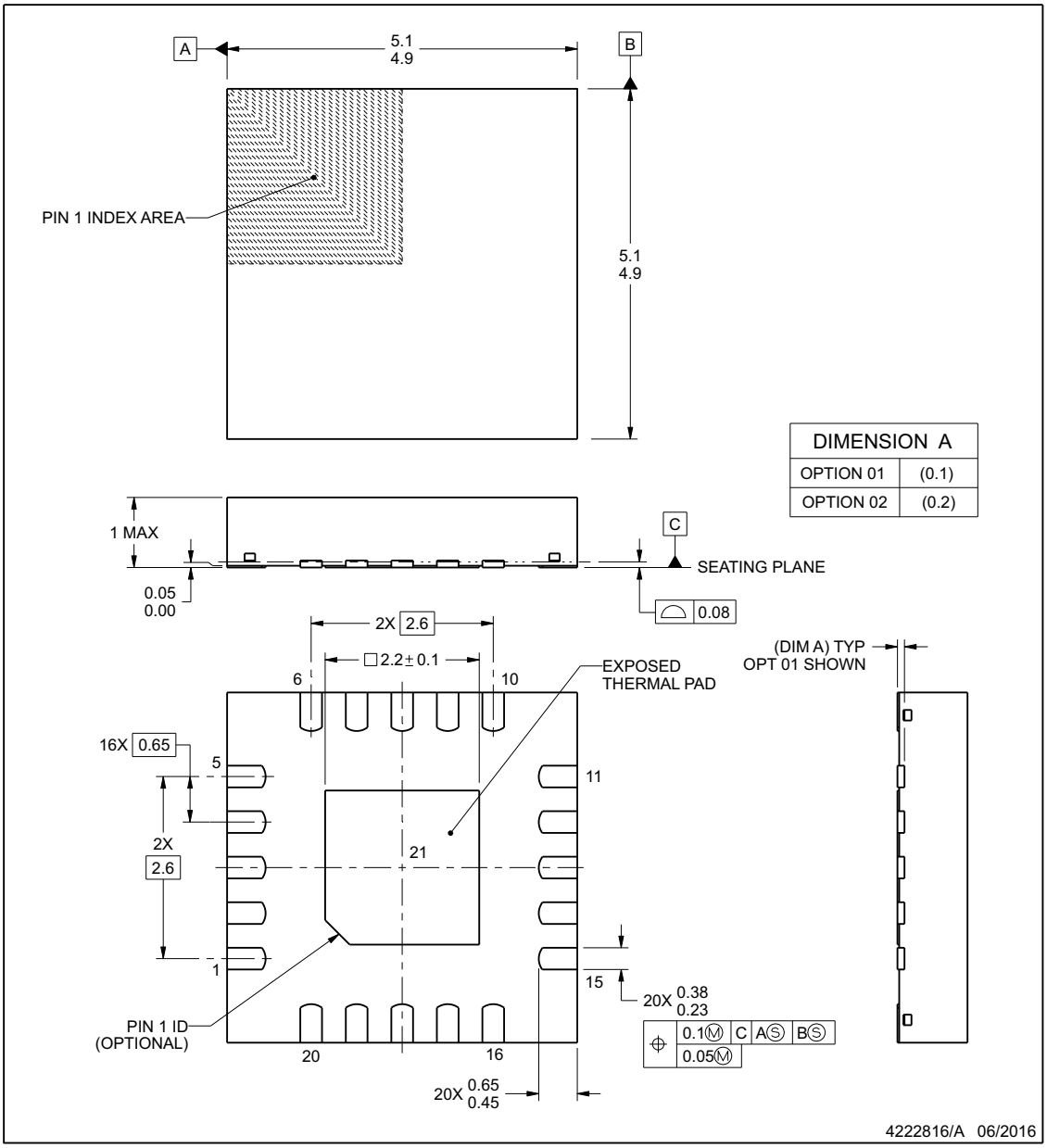


RGW0020B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

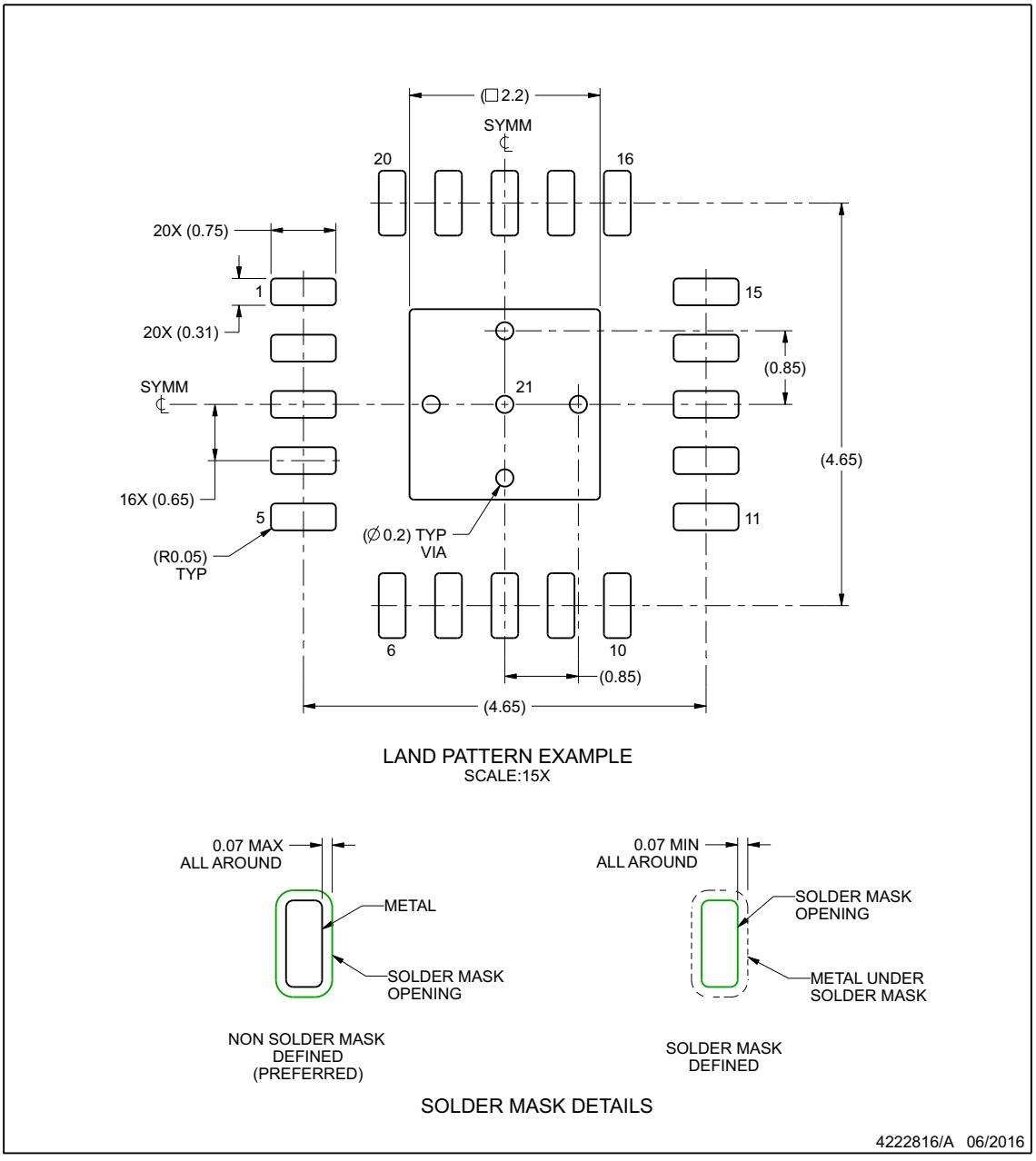
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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EXAMPLE BOARD LAYOUT

RGW0020B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

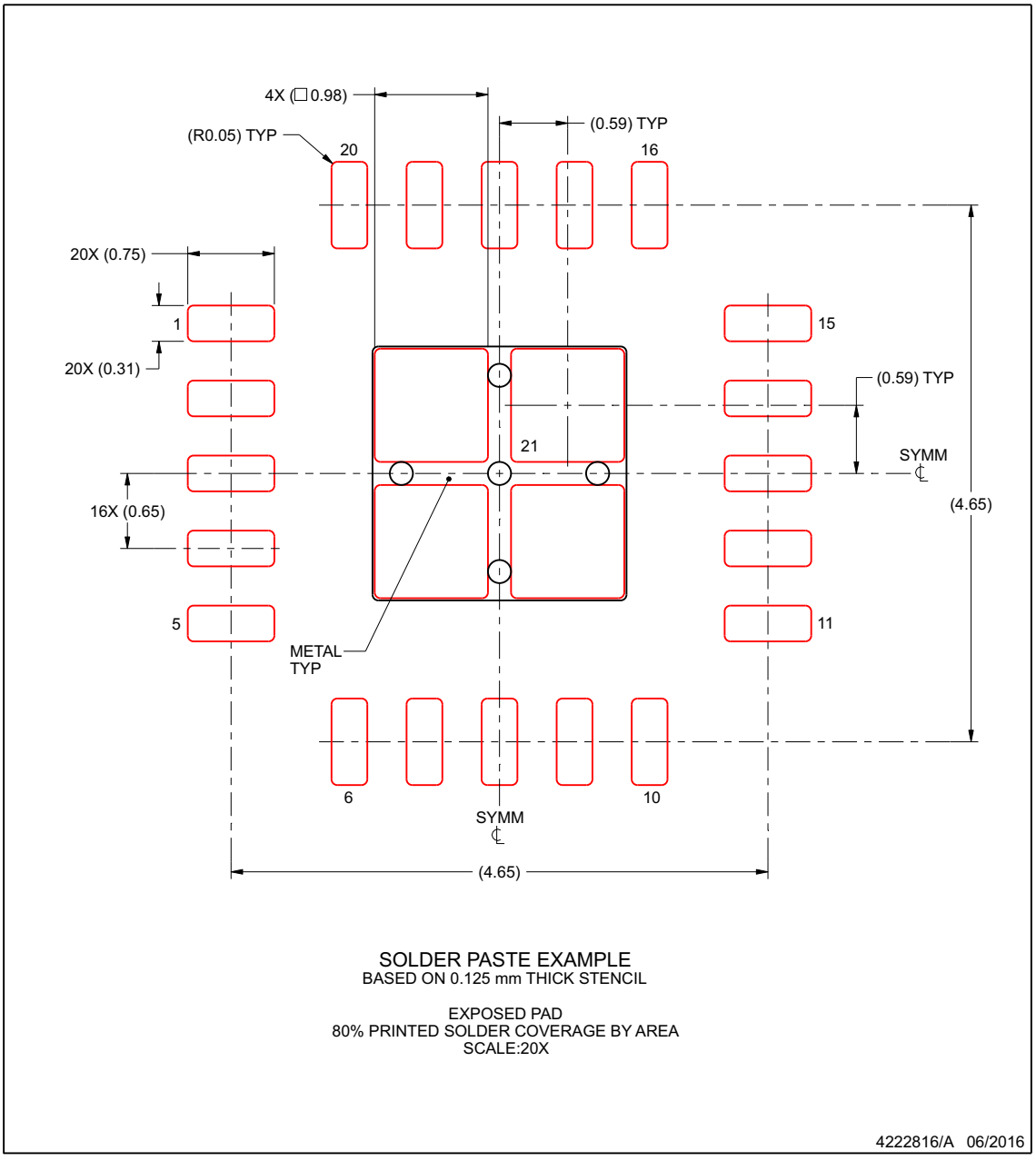
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RGW0020B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222816/A 06/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A7100RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	PYLQ
TPS7A7100RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	PYLQ
TPS7A7100RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYLQ
TPS7A7100RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYLQ
TPS7A7100RGTTG4	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYLQ
TPS7A7100RGTTG4.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYLQ
TPS7A7100RGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBS
TPS7A7100RGWR.B	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBS
TPS7A7100RGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBS
TPS7A7100RGWT.B	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBS
TPS7A7100RGWTG4	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBS
TPS7A7100RGWTG4.B	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

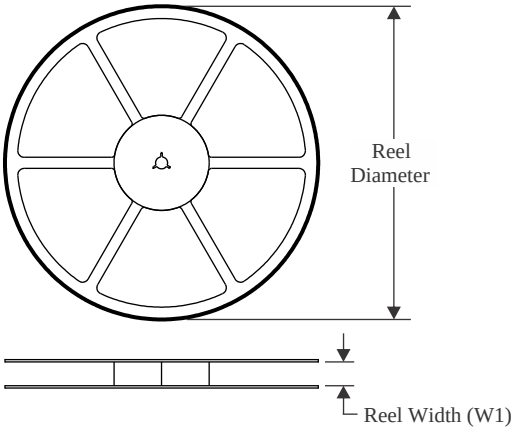
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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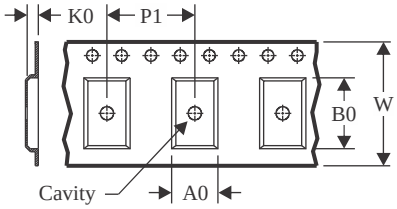
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

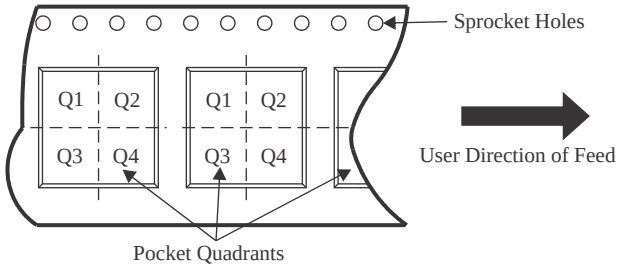


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

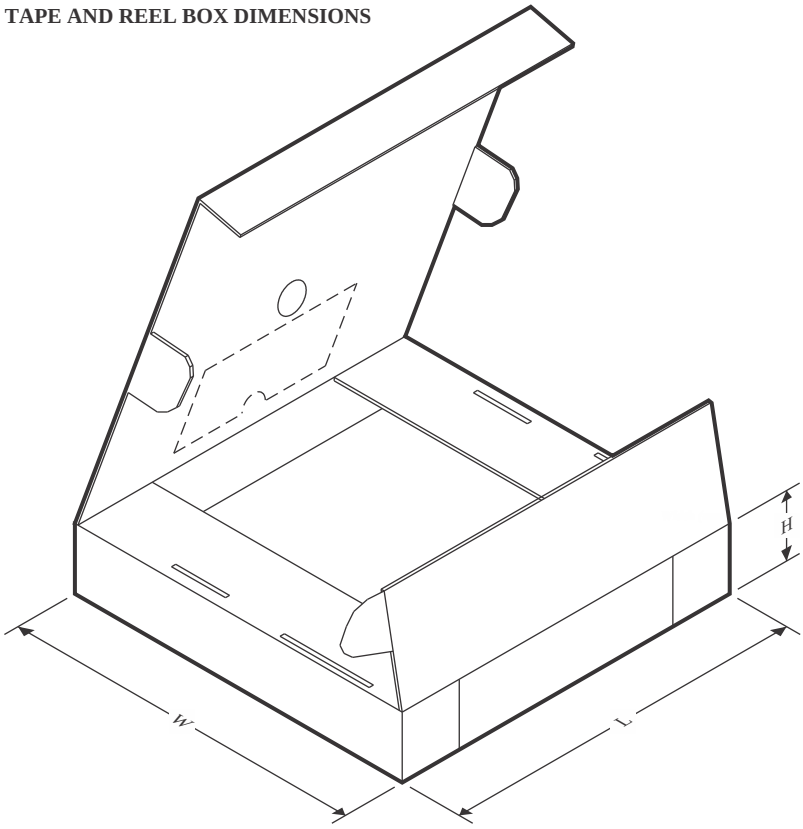
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7100RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7100RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7100RGTTG4	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A7100RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A7100RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A7100RGWTG4	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7100RGTR	VQFN	RGT	16	3000	335.0	335.0	25.0
TPS7A7100RGTT	VQFN	RGT	16	250	182.0	182.0	20.0
TPS7A7100RGTTG4	VQFN	RGT	16	250	182.0	182.0	20.0
TPS7A7100RGWR	VQFN	RGW	20	3000	346.0	346.0	33.0
TPS7A7100RGWT	VQFN	RGW	20	250	210.0	185.0	35.0
TPS7A7100RGWTG4	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

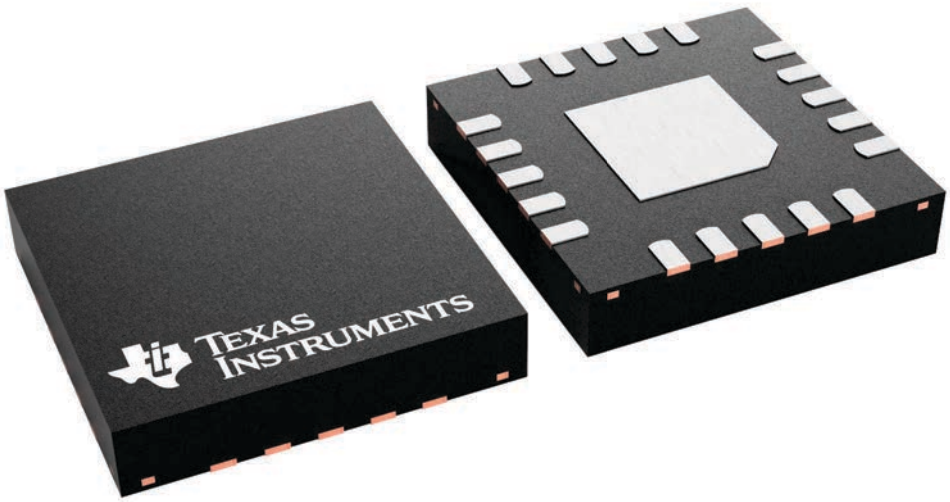
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

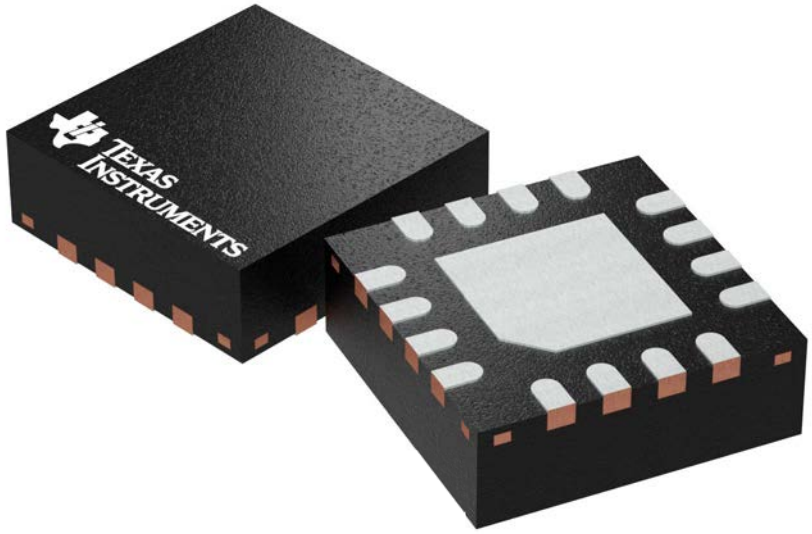
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227157/A

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



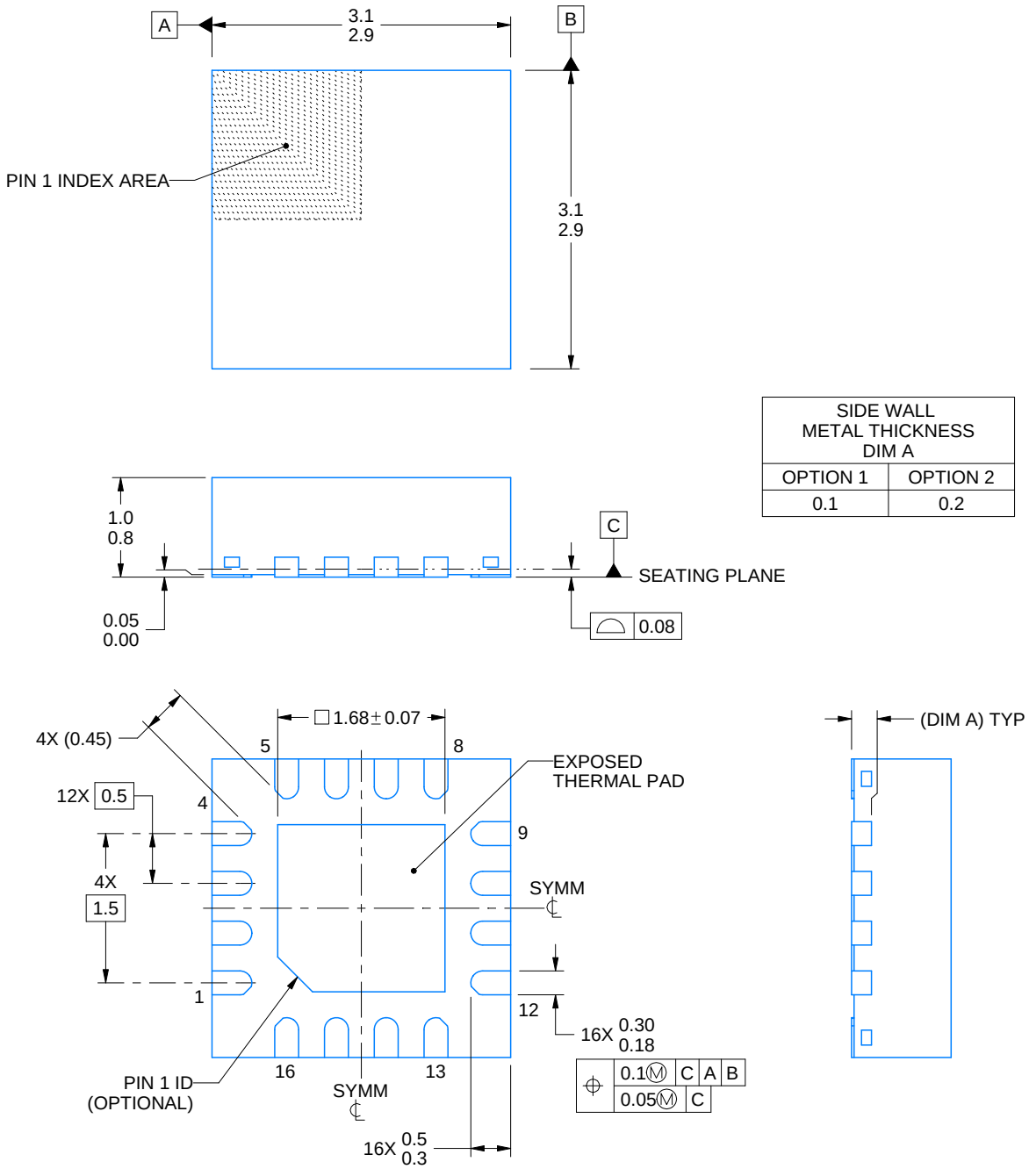
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

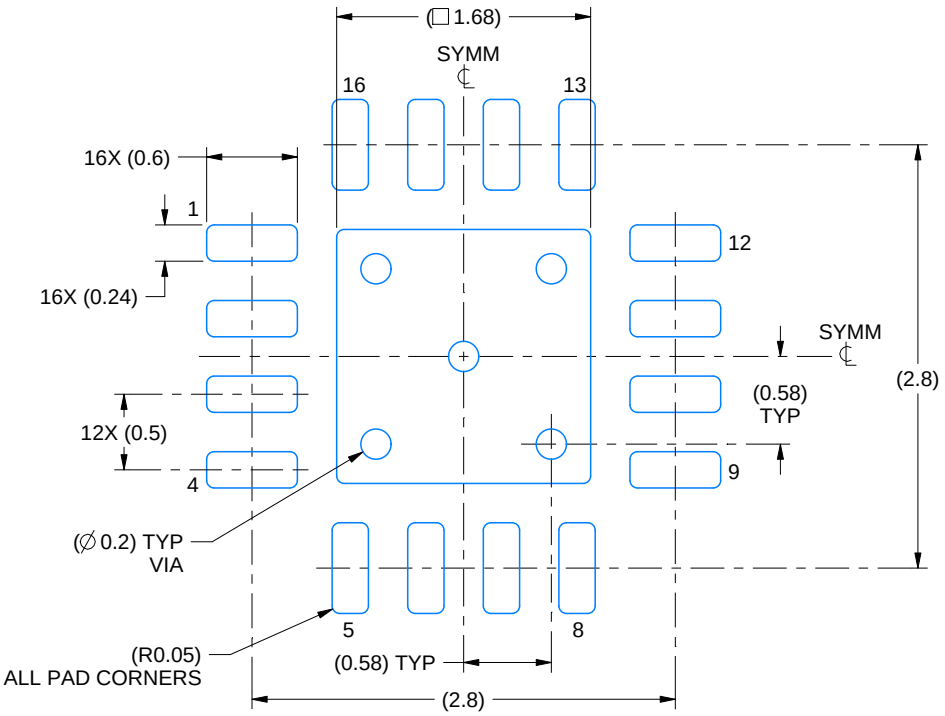
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

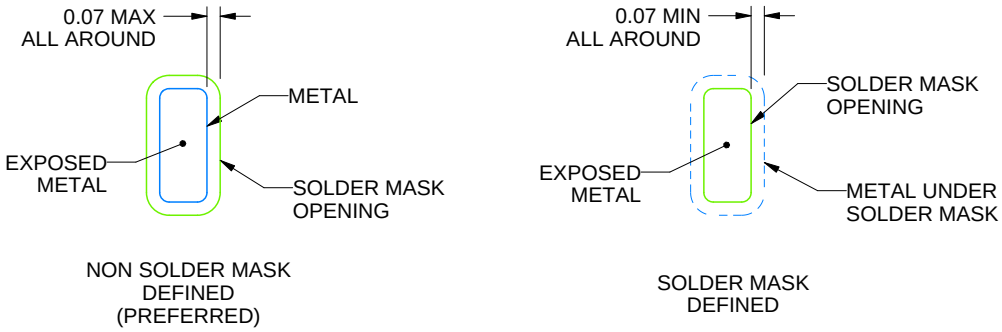


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

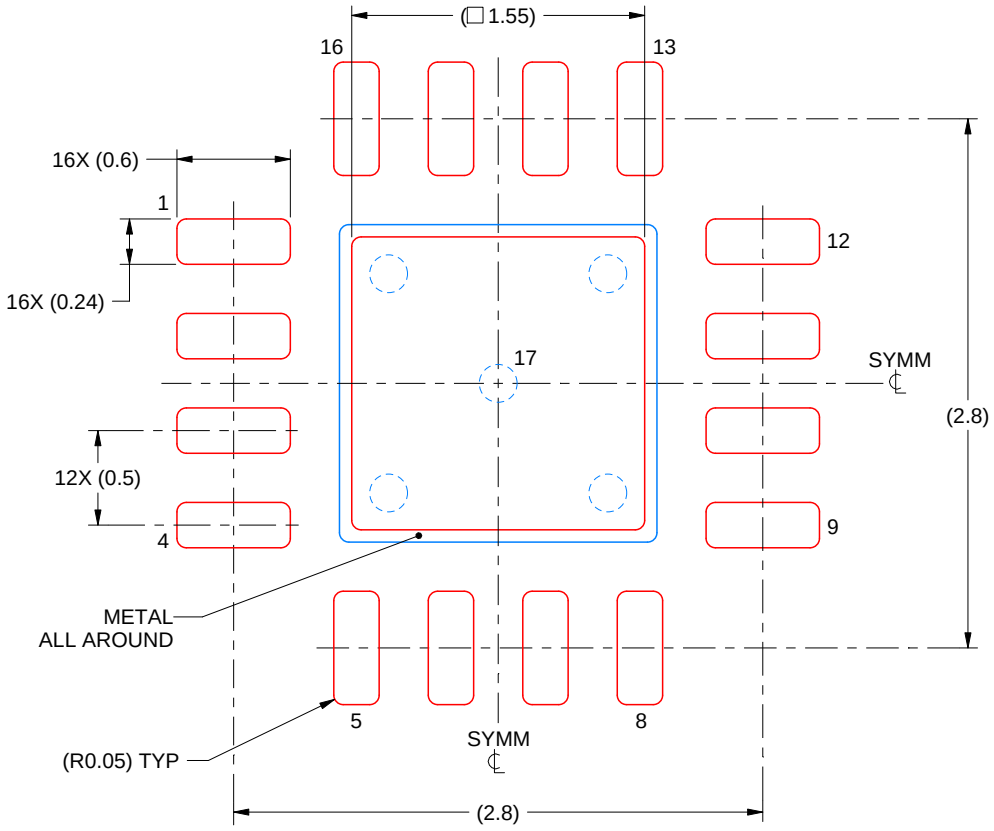


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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