TPS7A96 2A、超低ノイズ、超高 PSRR、RF 電圧レギュレータ

1 特長

- 超低出力ノイズ:
  - 0.5μV_{RMS} (代表値、10Hz～100kHz)
- 高い電源リップル除去 (PSRR):
  - 100Hz 時に 94dB
  - 1kHz 時 104dB
  - 10kHz 時 76dB
  - 100kHz 時 58dB
  - 1MHz 時 48dB
- 入力、負荷、温度に関する精度:1%
- 低いドロップアウト:2A 時に 160mV
- 広い入力電圧範囲:1.9V～5.7V
- 広い出力電圧範囲:0.4V～5.5V
- 並列接続による低ノイズ化と大電流化が可能
- 高速過渡応答
- 高精度のイネーブルと UVLO
- プログラム可能な電流制限
- プログラム可能な PG スレッショルド
- 可変スタートアップ突入電流の制御
- オープン・ドレインのパワー・グッド (PG) 出力
- パッケージ:3.00mm × 3.00mm の 10 ピン WSON:
  - JEDEC $R_{\theta JA}$:46.1℃/W
  - EVM $R_{\theta JA}$:25.6℃/W

2 アプリケーション

- マクロ・リモート無線ユニット (RRU)
- 屋外バックホール・ユニット
- mMIMO アクティブ・アンテナ・システム (AAS)
- 超音波スキャナ
- 実験室およびフィールド向け計測機器
- センサ、画像処理、レーダー

3 概要

TPS7A96 は、わずか 200mV のドロップアウトで 2A を供給できる超低ノイズ (0.5μV_{RMS})、低ドロップアウト (LDO) の電圧レギュレータです。この小さいドロップアウトは、エラー・アンプの広い帯域幅とあいまって、小さい動作ヘッドルーム (500mV) と大出力電流 (1.75A) でも非常に大きい PSRR (1kHz で 104dB、1MHz で 48dB) を可能にします。

デバイスの出力電圧は、外付け抵抗によって 0.4V～5.5V の範囲で調整可能です。入力電圧範囲が広く、最低 1.9V、最高 5.7V での動作がサポートされています。このデバイスには、プログラム可能な電流制限、プログラム可能な PG スレッショルド、および高精度イネーブルが搭載されているため、アプリケーションをより的確に制御できます。

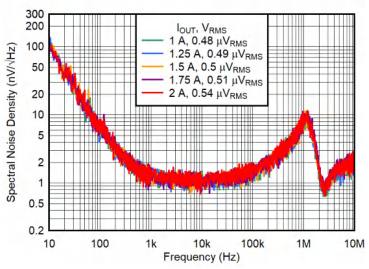
高精度の基準電圧と広帯域幅のトポロジを備えたこのデバイスは、並列接続することで簡単に低ノイズと大電流を実現できます。

このデバイスは、1% の出力電圧精度 (入力、負荷、温度に関して) およびソフトスタート機能により突入電流が低減されるため、敏感なアナログ低電圧デバイスへの電力供給向けの設計になっています。

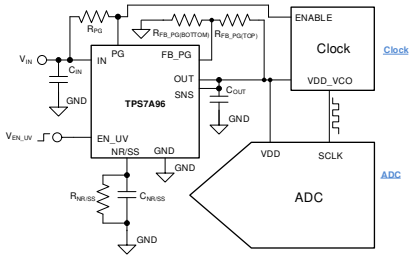
パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TPS7A96	DSC (WSON、10)	3mm × 3mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



出力電圧の影響を受けない超低出力ノイズ (10Hz～100kHz)



代表的なアプリケーション回路

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2023) to Revision A (July 2023)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

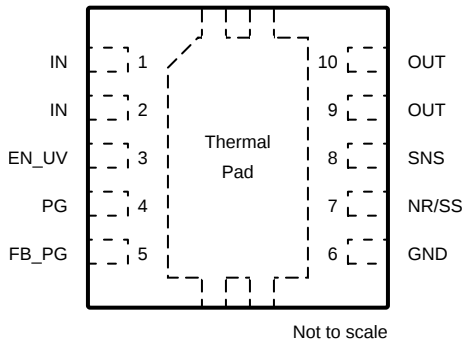


図 5-1. DSC Package, 10-Pin WSON (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	WSON		
EN_UV	3	I	Precision enable and undervoltage lockout pin. See the *Precision Enable and UVLOs* section for details.
FB_PG	5	I	Power-good feedback pin. This pin has a dual function. This pin programs the PG pin output threshold and scales the factory-programmed current limit value specified in the *Electrical Characteristics* table to either 100%, 80%, or 60%. See the *Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)* section for details.
GND	6	G	Ground pin. See the *Layout Guidelines* section for details.
IN	1, 2	P	Input voltage supply pin. A 4.7-µF or larger ceramic capacitor is recommended. See the *Recommended Capacitor Types* section and the *Recommended Operating Conditions* table for additional information.
NR/SS	7	I	Output voltage set and noise-reduction pin. See the *Programmable Soft-Start and Noise-Reduction (NR/SS Pin)* section for details.
OUT	9, 10	O	Regulated output pin. A 4.7-µF or larger ceramic capacitor is recommended. See the *Load Transient Response* section for additional information.
PG	4	O	Open-drain, power-good indicator pin for the LDO output voltage. See the *Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)* section for additional information.
SNS	8	I	Output sense pin. This pin is the input to the noninverting terminal of the error amplifier. See the *Layout Guidelines* section for details.
Thermal pad		G	The thermal pad is electrically connected to the GND pin. See the *Layout Guidelines* section for details.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND(unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, PG, EN_UV	–0.3	6.0	V
	FB_PG	–0.3	1.5	
	OUT	–0.3	V_{IN} + 0.3	
	NR/SS, SNS	–0.3	6.0	
Current	OUT	Internally limited		A
	PG (sink current into the device)		5	mA
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.9		5.7	V
V_{OUT}	Output voltage range	0.4		V_{IN} - V_{DO}	V
I_{OUT}	Output current	0		2	A
C_{IN}	Input capacitor	4.7	10	1000	µF
C_{OUT}	Output capacitor	4.7	10	1000	µF
C_{OUT_ESR}	Output capacitor ESR	1		20	mΩ
Z_{OUT_ESL}	Total output loop impedance			2	nH
$C_{NR/SS}$	Noise-reduction capacitor	1	4.7	100	µF
R_{PG}	Power-good pull-up resistance	10		100	kΩ
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A96 DSC (WSON) 10 Pins(2)		UNIT
		JEDEC	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.1	25.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.2	-	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.1	-	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.
(2) The JEDEC colum refers to JEDEC standard (2s2p) and EVM column refers to the EVM thermal model using JEDEC measurement methodology, see TPS7A96EVM-106 thermal analysis.

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6.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.5 V, $V_{OUT(NOM)}$ = 3.3 V, I_{OUT} = 1 mA, V_{EN} = 1.8 V, C_{IN} = C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (4) (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range		1.9		5.7	V
V_{UVLO}	Input supply UVLO	V_{IN} rising, no load		1.6	1.7	V
$V_{HYS(UVLO)}$	Input supply UVLO hysteresis	No load	40	53		mV
$I_{NR/SS}$	NR/SS pin current	V_{IN} = 1.9 V, I_{OUT} = 1 mA, V_{OUT} = 1.2 V		150		µA
		1.9 V ≤ V_{IN} ≤ 5.5 V, 0.4 V ≤ V_{OUT} < 1.2 V, 1 mA ≤ I_{OUT} ≤ 2A	–1.5		1.5	%
		1.9 V ≤ V_{IN} ≤ 5.5 V, 1.2 V ≤ V_{OUT} ≤ 5.1 V, 1 mA ≤ I_{OUT} ≤ 2A	–1		1	
I_{FAST_SS}	NR/SS fast start-up charging current	$V_{NR/SS}$ = GND, V_{IN} ≥ 2.5 V, V_{FB_PG} < 0.2 V, I_{OUT} = 0 mA		2.1		mA
		$V_{NR/SS}$ = GND, V_{IN} = 1.9 V, V_{FB_PG} < 0.2 V, I_{OUT} = 0 mA		1.5		
V_{OUT}	Output voltage range		0		5.5	V
V_{OS}	Output offset voltage ($V_{NR/SS}$ – V_{OUT})	1.9 V ≤ V_{IN} ≤ 5.7 V, 1.2 V ≤ V_{OUT} ≤ 5.1 V, 1 mA ≤ I_{OUT} ≤ 2 A	–2	±0.1	2	mV
		1.9 V ≤ V_{IN} ≤ 5.7 V, 0.4 V ≤ V_{OUT} < 1.2 V, 1 mA ≤ I_{OUT} ≤ 2 A	–5	±0.2	5	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation: $\Delta I_{NR/SS}$	0.4 V ≤ V_{OUT} < 1.2 V, I_{OUT} = 1 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.7 V		–0.9		nA/V
		V_{OUT} = 1.2 V and V_{OUT} = 3.3 V, I_{OUT} = 1mA, V_{IN} = (V_{OUT} + 0.5V) to 5.7 V		2		
	Line regulation: ΔV_{OS}	0.4 V ≤ V_{OUT} < 1.2 V, I_{OUT} = 1 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.7 V		–4.5		µV/V
		V_{OUT} = 1.2 V & V_{OUT} = 3.3 V, I_{OUT} = 1 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.7 V		2.1		
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation: $\Delta I_{NR/SS}$ (1)	V_{IN} = 1.9 V, V_{OUT} = 1.2 V, 1 mA ≤ I_{OUT} ≤ 2 A		2.3		nA
		V_{IN} = 3.8 V, V_{OUT} = 3.3 V, 1 mA ≤ I_{OUT} ≤ 2 A		–3.6		
		V_{IN} = 5.6 V, V_{OUT} = 5.1 V, 1 mA ≤ I_{OUT} ≤ 2 A		–21		
	Load regulation: ΔV_{OS} (1)	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, 1.2V ≤ V_{OUT} ≤ 5.1 V, 1 mA ≤ I_{OUT} ≤ 2 A		0.03		mV
$\Delta I_{NR/SS(\Delta VNR/SS)}$	Change in $I_{NR/SS}$ vs $V_{NR/SS}$	0.4 V ≤ $V_{NR/SS}$ ≤ 1.5 V, V_{IN} = 5.7 V, I_{OUT} = 1 mA		6.3		nA
		1.5 V ≤ $V_{NR/SS}$ ≤ 5 V, V_{IN} = 5.7 V, I_{OUT} = 1 mA		–3.3		
$\Delta V_{OS(\Delta VNR/SS)}$	Change in V_{OS} vs $V_{NR/SS}$	0.4 V ≤ $V_{NR/SS}$ ≤ 1.5 V, V_{IN} = 5.7 V, I_{OUT} = 1 mA		0.033		mV
		1.5 V ≤ $V_{NR/SS}$ ≤ 5 V, V_{IN} = 5.7 V, I_{OUT} = 1 mA		0.013		
V_{DO}	Dropout voltage(2)	1.9 V ≤ V_{IN} < 2.0 V, I_{OUT} = 1 mA, V_{OUT} = 99% x $V_{OUT(NOM)}$		160		mV
		1.9 V ≤ V_{IN} < 2.4 V, I_{OUT} = 2 A, V_{OUT} = 99% x $V_{OUT(NOM)}$		215	350	
		V_{IN} ≥ 2.0 V, I_{OUT} = 1 mA, V_{OUT} = 99% x $V_{OUT(NOM)}$		140		
		V_{IN} ≥ 2.4 V, I_{OUT} = 2 A, V_{OUT} = 99% x $V_{OUT(NOM)}$		160	250	
I_{LIM}	Output current limit	V_{OUT} forced at 90% of $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 200 mV or V_{IN} = 1.9 V whichever is greater, $V_{OUT(NOM)}$ ≥ 1.2 V, $R_{PGFB\text{-}to\text{-}GND}$ ≤ 12.5 kΩ (±1%)	2.4	2.6	2.8	A
		V_{OUT} forced at 90% of $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 200 mV or V_{IN} = 1.9 V whichever is greater, $V_{OUT(NOM)}$ ≥ 1.2 V, $R_{PGFB\text{-}to\text{-}GND}$ = 50 kΩ (±1%)	1.92	2.07	2.24	
		V_{OUT} forced at 90% of $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 200 mV or V_{IN} = 1.9 V whichever is greater, $V_{OUT(NOM)}$ ≥ 1.2 V, $R_{PGFB\text{-}to\text{-}GND}$ = 100 kΩ (±1%)	1.44	1.55	1.68	
ΔI_{SC}	Short-circuit current-limit variation (3)	V_{IN} = $V_{OUT(NOM)}$ + 200 mV or V_{IN} = 1.9 V whichever is greater, V_{OUT} = 0 V		4.56		%
I_{GND}	GND pin current	V_{IN} = 5.7 V, V_{OUT} = 5.1 V, I_{OUT} = 0.1 mA	8	15	22	mA
		V_{IN} = 1.9 V, I_{OUT} = 2 A, V_{OUT} = 1.2 V	40	49	59	

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6.5 Electrical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), $V_{IN(NOM)} = V_{OUT(NOM)}$ + 0.5 V, $V_{OUT(NOM)}$ = 3.3 V, I_{OUT} = 1 mA, V_{EN} = 1.8 V, $C_{IN} = C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ (4) (unless otherwise noted); typical values are at T_J = 25°C

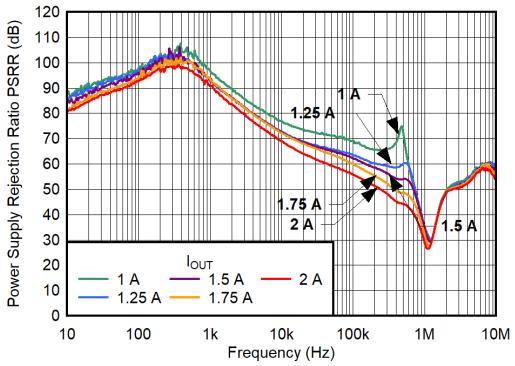
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown GND pin current	PG = (open), V_{IN} = 5.7 V, V_{EN_UV} = 0.4 V		0.1	30	µA
I_{EN_UV}	EN_UV pin current	V_{IN} = 5.7 V, 0 V ≤ V_{EN_UV} ≤ 5.5 V	–1		1	µA
$V_{IH(EN_UV)}$	EN_UV trip point rising (turn-on)	V_{IN} = 1.9 V, no load	1.20	1.22	1.25	V
$V_{HYS(EN_UV)}$	EN_UV trip point hysteresis	V_{IN} = 1.9 V, no load		150		mV
t_{PGDH}	PG delay time rising	Time from V_{OUT} crossing PG threshold% to PG reaching 20% of its value		1.1		ms
t_{PGDL}	PG delay time falling	Time from 90% of V_{OUT} to 80% of PG		3		µs
V_{FB_PG}	FB_PG pin trip point (rising)	1.9 V ≤ V_{IN} ≤ 5.7 V	0.19	0.2	0.21	V
$V_{HYS(FB_PG)}$	FB_PG pin hysteresis	1.9 V ≤ V_{IN} ≤ 5.7 V		6		mV
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} = 1.9 V, V_{OUT} < $V_{FB_PG(threshold)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{PG(LKG)}$	PG pin leakage current	V_{IN} = 5.7 V, V_{OUT} > $V_{FB_PG(threshold)}$, V_{PG} = 5.5 V			1	µA
I_{FB_PG}	FB_PG pin leakage current	V_{IN} = 5.7 V, V_{FB_PG} = 0.2 V	–100		100	nA
PSRR	Power-supply ripple rejection	f = 1 MHz, V_{IN} = 3.8 V, $V_{OUT(NOM)}$ = 3.3 V, I_{OUT} = 1.5 A, $C_{NR/SS}$ = 4.7 µF		30		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, 1.9 V ≤ V_{IN} ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 2.0 A, $C_{NR/SS}$ = 4.7 µF		0.5		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{IN} = 2 V, $V_{OUT(NOM)}$ = 0.8 V, I_{OUT} = 2.0 A, $C_{NR/SS}$ = 4.7 µF		0.835		
	Noise spectral density	f = 100 Hz, 1.9 V ≤V_{IN} ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 1.0 A, $C_{NR/SS}$ = 4.7 µF		6.6		$nV/\sqrt{Hz}$
		f = 1 kHz, 1.9 V ≤V_{IN} ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 1.0 A, $C_{NR/SS}$ = 4.7 µF		1.3		
		f = 10 kHz, 1.9 V ≤ V_{IN} ≤ 5.7 V, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 1.0 A, $C_{NR/SS}$ = 4.7 µF		1.1		
$R_{PULLDOWN_NRSS}$	NRSS active discharge resistance	V_{IN} = 1.9 V, V_{EN_UV} = GND		15		Ω
$R_{PULLDOWN}$	Output active discharge resistance	V_{IN} = 1.9 V, V_{EN_UV} = GND		195		Ω
TSD(shutdown)	Thermal shutdown temperature	Shutdown, temperature increasing		175		°C
TSD(reset)	Thermal shutdown reset temperature	Reset, temperature decreasing		160		

(1) The device is not tested under conditions where $V_{IN} > V_{OUT(NOM)}$ + 2.5 V and I_{OUT} > 1.5 A because the junction temperature is higher than +125°C. Also, this accuracy specification does not apply on any application condition that exceeds the maximum junction temperature.
(2) Measured when output voltage drops 1% below targeted value.
(3) Brick-wall current limit: $I_{CL_\%} = (I_{SC} - I_{CL_@0.9xVOUT}) / I_{CL_@0.9xVOUT}$ x 100.
(4) Additional information on setting the PG pullup resistor can be found in the application section.

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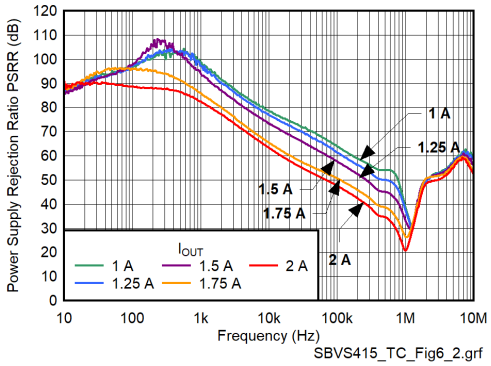
6.6 Typical Characteristics

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



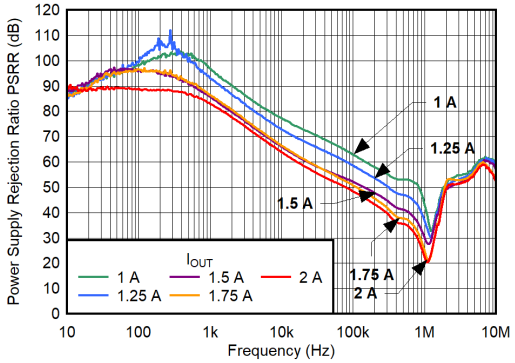
V_{IN} = 1.9 V, C_{IN} = 1.0 µF

図 6-1. PSRR vs Frequency and I_{OUT} for V_{OUT} = 1.2 V



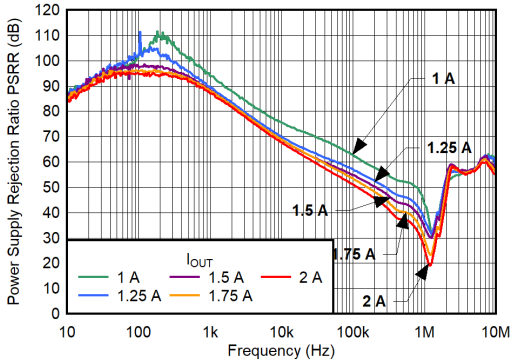
V_{IN} = 2.3 V, C_{IN} = 1.0 µF

図 6-2. PSRR vs Frequency and I_{OUT} for V_{OUT} = 1.8 V



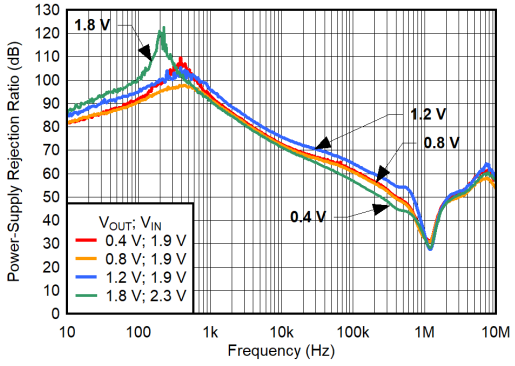
V_{IN} = 3.8 V, C_{IN} = 1.0 µF

図 6-3. PSRR vs Frequency and I_{OUT} for V_{OUT} = 3.3 V



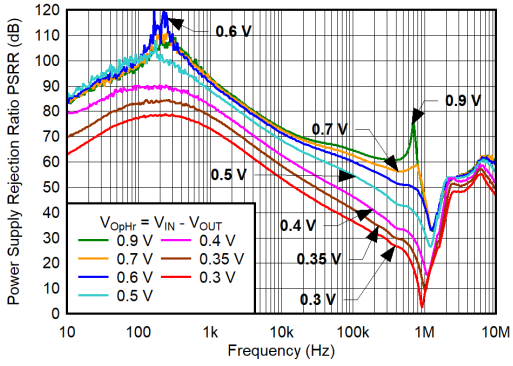
V_{IN} = 5.5 V, C_{IN} = 1.0 µF

図 6-4. PSRR vs Frequency and I_{OUT} for V_{OUT} = 5.0 V



V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1.5 A, C_{IN} = 1.0 µF

図 6-5. PSRR vs Frequency and Input Pairs



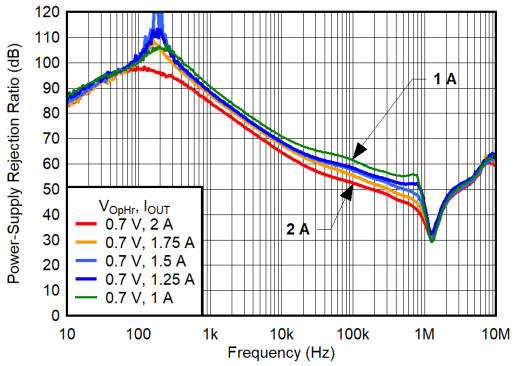
V_{IN} = V_{OUT} + V_{OpHr}, V_{OUT} = 3.3 V, I_{OUT} = 1.5 A, C_{IN} = 1.0 µF

図 6-6. PSRR vs Frequency for Operating Headroom (V_{OpHr})

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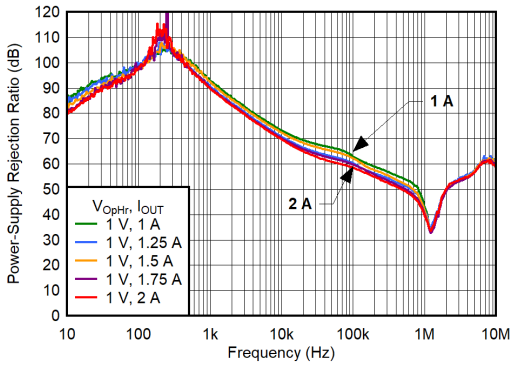
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



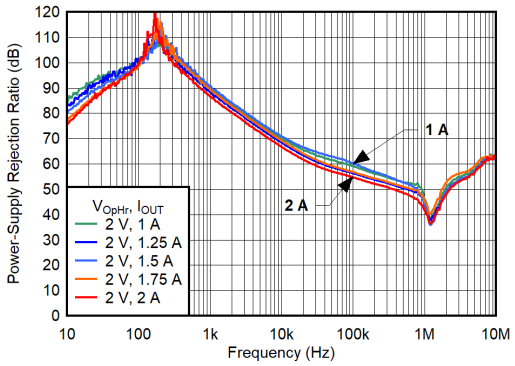
V_{OUT} = 3.3 V, C_{IN} = 1.0 µF

図 6-7. PSRR vs Frequency for Operating Headroom (V_{OpHr}) and I_{OUT}



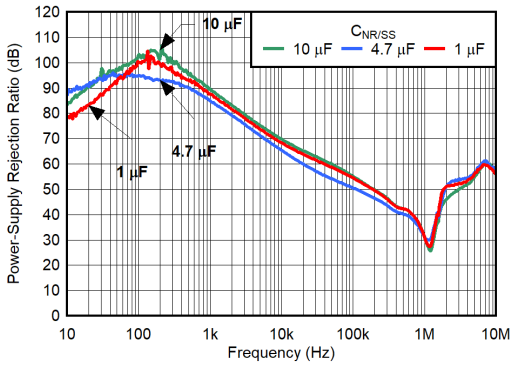
V_{OUT} = 3.3 V, C_{IN} = 1.0 µF

図 6-8. PSRR vs Frequency for Operating Headroom (V_{OpHr}) and I_{OUT}



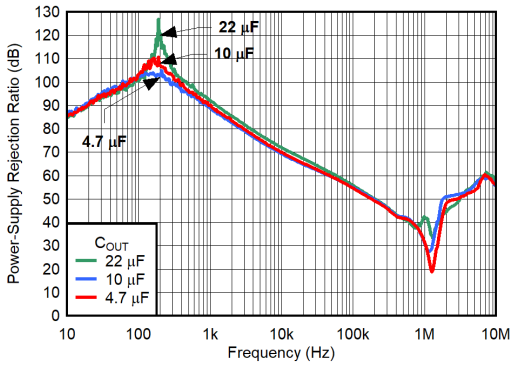
V_{OUT} = 3.3 V, C_{IN} = 1.0 µF

図 6-9. PSRR vs Frequency for Operating Headroom (V_{OpHr}) and I_{OUT}



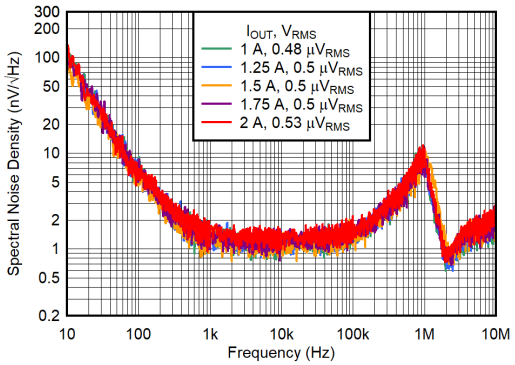
V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1.5 A, C_{IN} = 1.0 µF

図 6-10. PSRR vs Frequency and $C_{NR/SS}$



V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1.5 , C_{IN} = 1.0 µF

図 6-11. PSRR vs Frequency and C_{OUT}



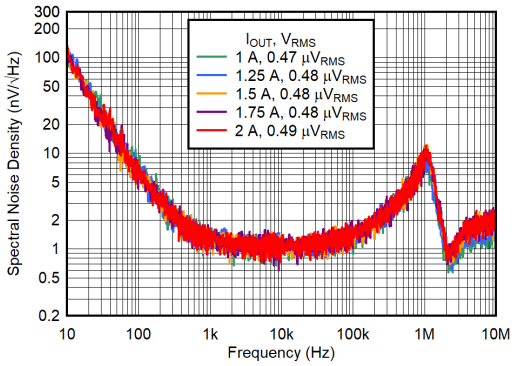
$C_{NR/SS}$ = 4.7 µF (10 Hz–100 kHz)

図 6-12. Output Voltage Noise Density vs Frequency for I_{OUT} and V_{OUT} = 1.2 V

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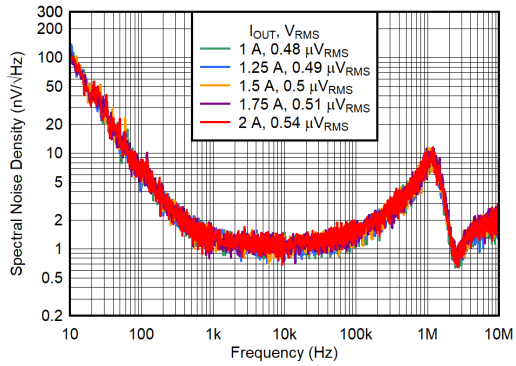
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



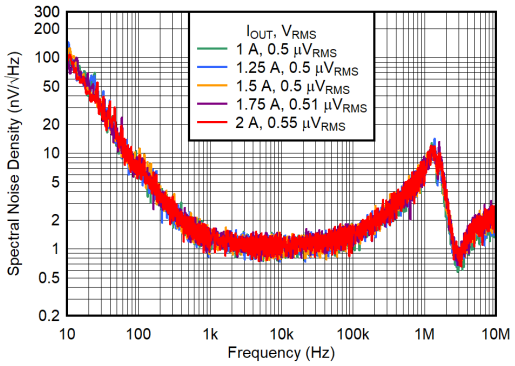
$C_{NR/SS}$ = 4.7 µF (10 Hz–100 kHz)

図 6-13. Output Voltage Noise Density vs Frequency for I_{OUT} and V_{OUT} = 1.8 V



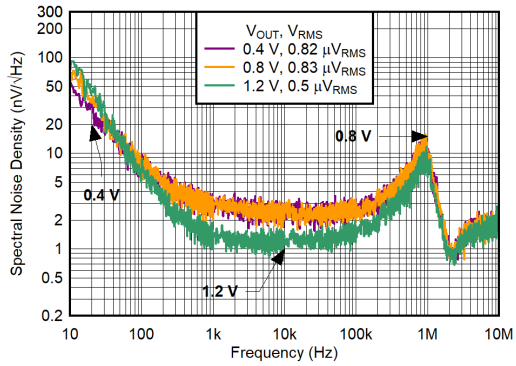
$C_{NR/SS}$ = 4.7 µF (10 Hz–100 kHz)

図 6-14. Output Voltage Noise Density vs Frequency for I_{OUT} and V_{OUT} = 3.3 V



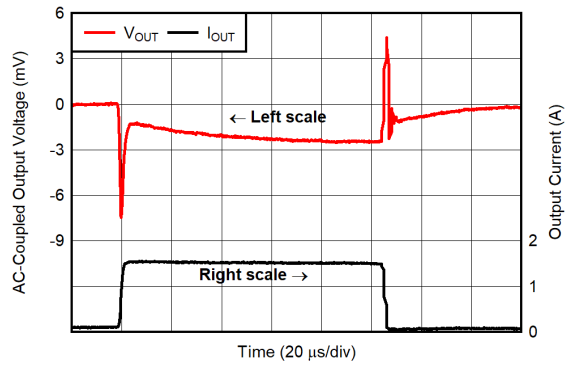
$C_{NR/SS}$ = 4.7 µF (10 Hz–100 kHz)

図 6-15. Output Voltage Noise Density vs Frequency for I_{OUT} and V_{OUT} = 5.0 V



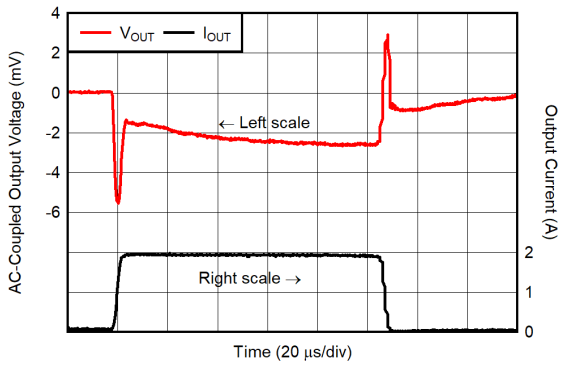
I_{OUT} = 1.5 A (10 Hz–100 kHz)

図 6-16. Output Voltage Noise Density vs Frequency and Input Pairs



V_{IN} = 1.9 V, SR = 1 A/µs

図 6-17. Load Transient Response for V_{OUT} = 1.2 V, I_{OUT} = 100 mA to 1.5 A



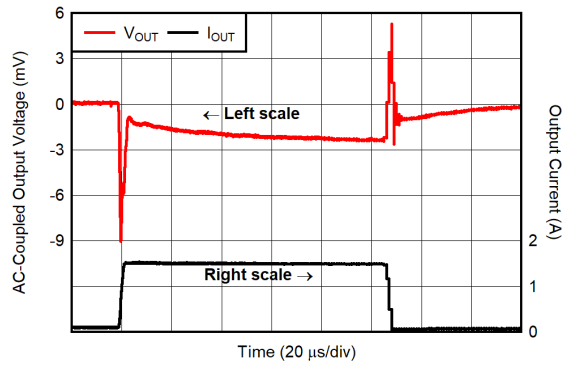
V_{IN} = 1.9 V, SR = 1 A/µs

図 6-18. Load Transient Response for V_{OUT} = 1.2 V, I_{OUT} = 100 mA to 2 A

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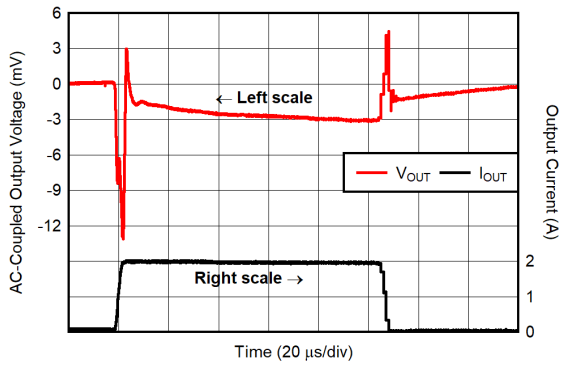
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



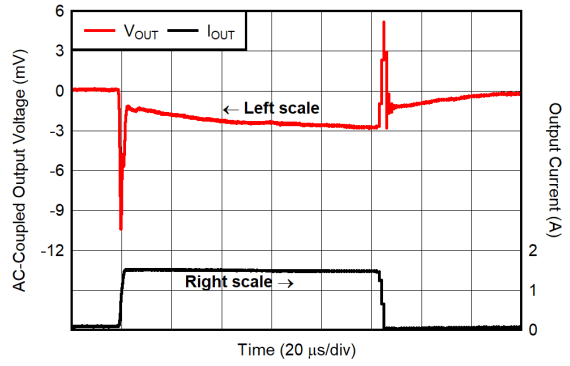
V_{IN} = 3.8 V, SR = 1 A/µs

図 6-19. Load Transient Response for V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 1.5 A



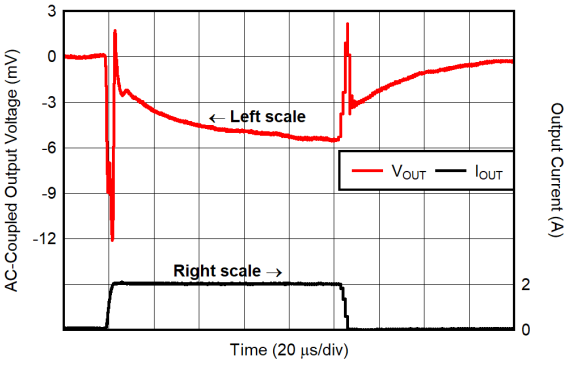
V_{IN} = 3.8 V, SR = 1 A/µs

図 6-20. Load Transient Response for V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 2 A



V_{IN} = 5.7 V, SR = 1 A/µs

図 6-21. Load Transient Response for V_{OUT} = 5.2 V, I_{OUT} = 100 mA to 1.5 A



V_{IN} = 5.7 V, SR = 1 A/µs

図 6-22. Load Transient Response for V_{OUT} = 5.2 V, I_{OUT} = 100 mA to 2 A

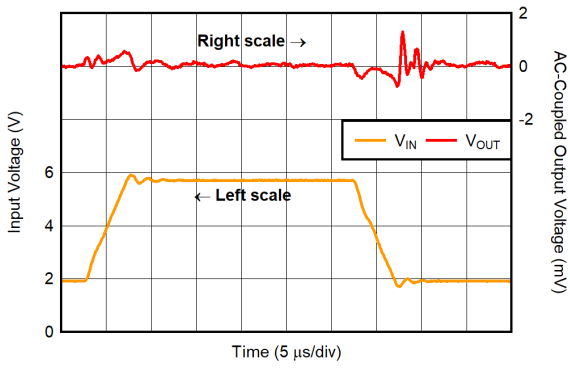


図 6-23. Line Transient Response for V_{OUT} = 1.2 V, I_{OUT} = 1.5 A

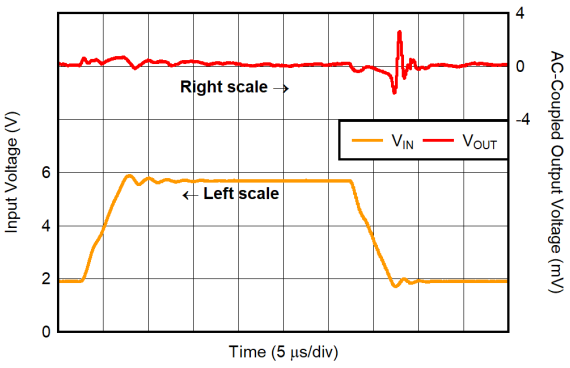
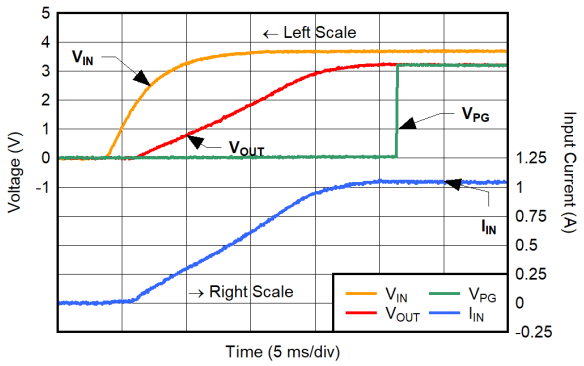


図 6-24. Line Transient Response for V_{OUT} = 1.2 V, I_{OUT} = 2 A

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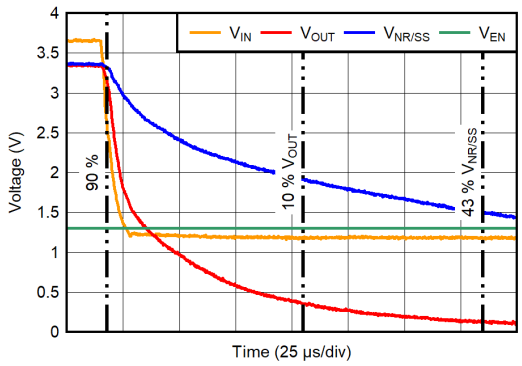
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



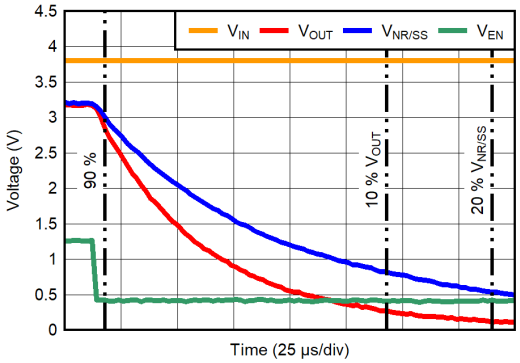
V_{OUT} = 3.3 V

図 6-25. Start-Up Waveform for I_{OUT} = 1 A



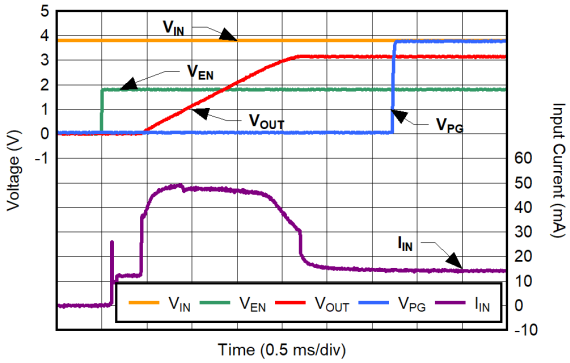
V_{OUT} = 3.3 V

図 6-26. Shutdown Waveform for $UVLO_{(IN)}$



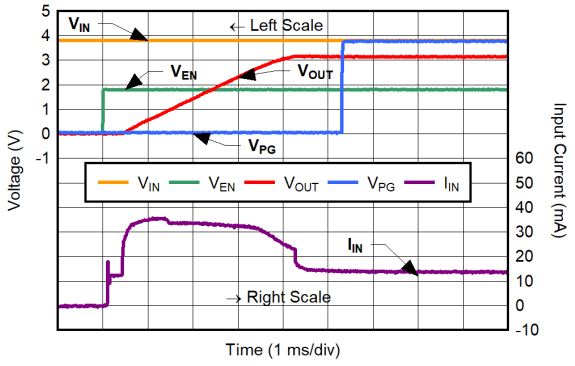
V_{OUT} = 3.3 V

図 6-27. Shutdown Waveform With EN



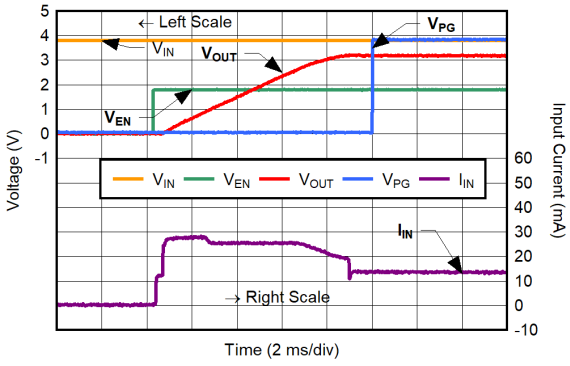
I_{OUT} = 0 mA, V_{IN} = 3.8 V, V_{OUT} = 3.3 V

図 6-28. Inrush Current for $C_{NR/SS}$ = 1.0 µF



I_{OUT} = 0 mA, V_{IN} = 3.8 V, V_{OUT} = 3.3 V

図 6-29. Inrush Current for $C_{NR/SS}$ = 2.2 µF



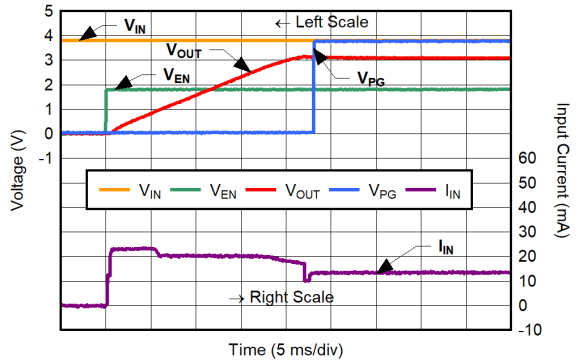
I_{OUT} = 0 mA, V_{IN} = 3.8 V, V_{OUT} = 3.3 V

図 6-30. Inrush Current for $C_{NR/SS}$ = 4.7 µF

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6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



I_{OUT} = 0 mA, V_{IN} = 3.8 V, V_{OUT} = 3.3 V

図 6-31. Inrush Current for $C_{NR/SS}$ = 10 µF

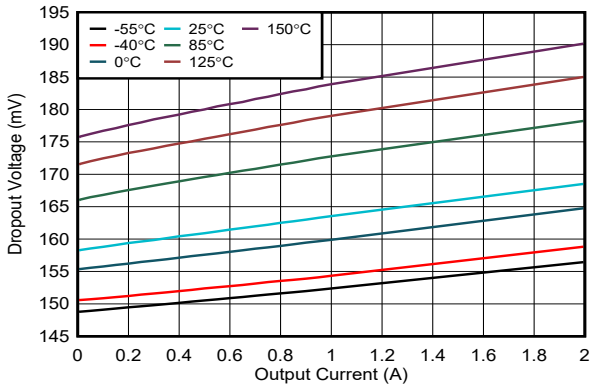


図 6-32. Dropout Voltage vs I_{OUT} for V_{OUT} = 1.8 V

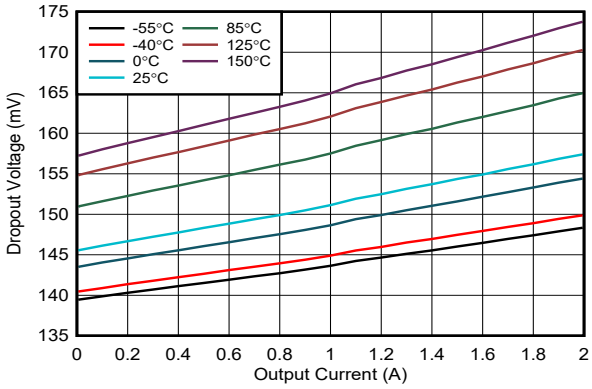
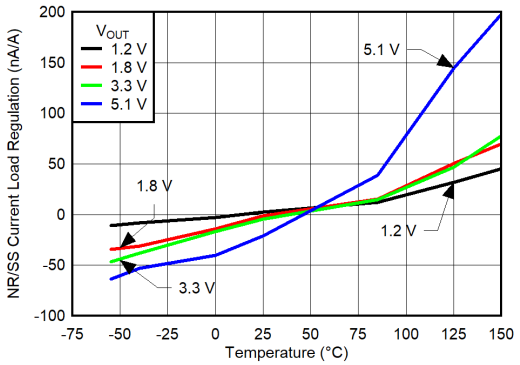


図 6-33. Dropout Voltage vs I_{OUT} for V_{OUT} = 3.3 V



C_{IN} = C_{OUT} = 10 µF, $C_{NR/SS}$ = 4.7 µF

図 6-34. $I_{NR/SS}$ Load Regulation

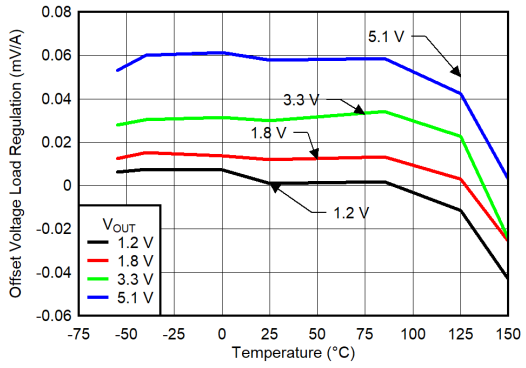


図 6-35. V_{OS} Load Regulation

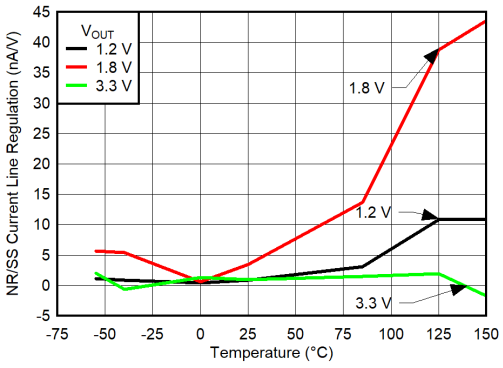


図 6-36. $I_{NR/SS}$ Line Regulation

6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C

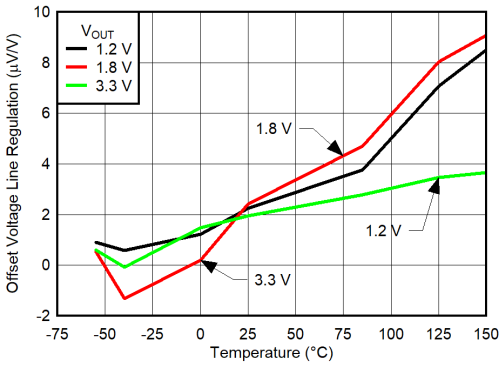
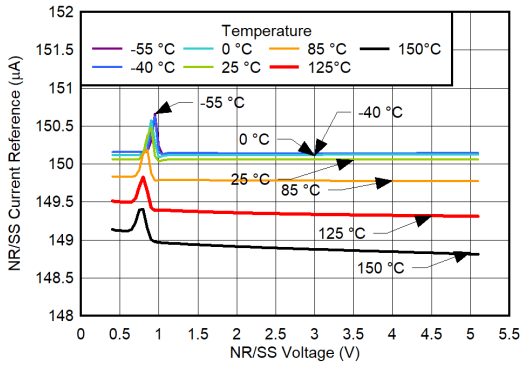
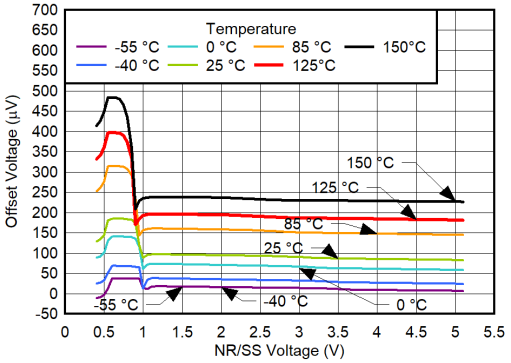


図 6-37. V_{OS} Line Regulation



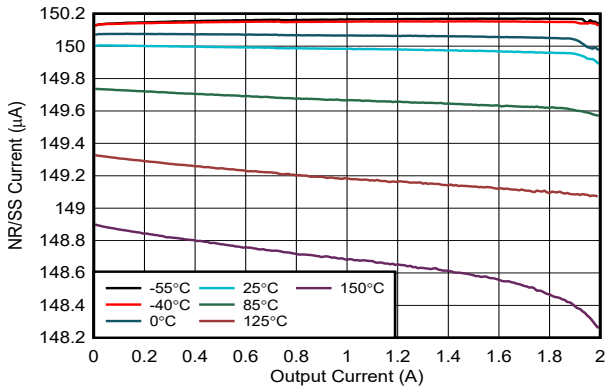
I_{OUT} = 0 mA

図 6-38. $I_{NR/SS}$ vs $V_{NR/SS}$ and Temperature



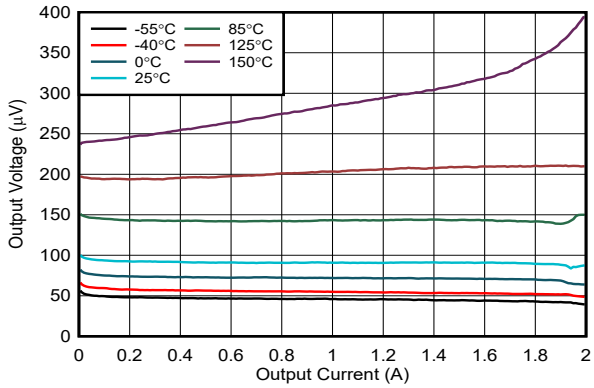
I_{OUT} = 0 mA

図 6-39. V_{OS} vs $V_{NR/SS}$ and Temperature for I_{OUT}



V_{OUT} = 3.3 V

図 6-40. $I_{NR/SS}$ vs I_{OUT} and Temperature for V_{IN} = 3.8 V



V_{OUT} = 3.3 V

図 6-41. V_{OS} vs I_{OUT} and Temperature for V_{IN} = 3.8 V

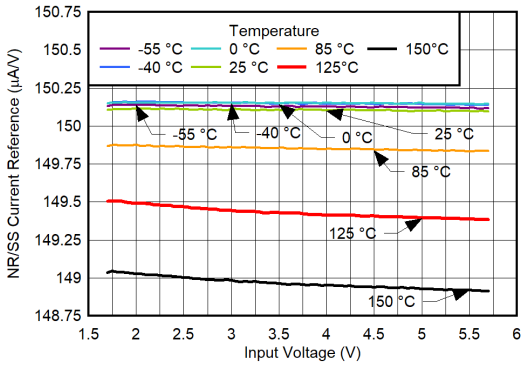


図 6-42. $I_{NR/SS}$ vs V_{IN} and Temperature for V_{OUT} = 1.2 V

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6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C

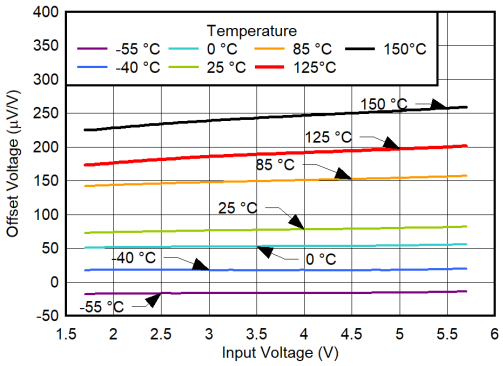


図 6-43. V_{OS} vs V_{IN} and Temperature for V_{OUT} = 1.2 V

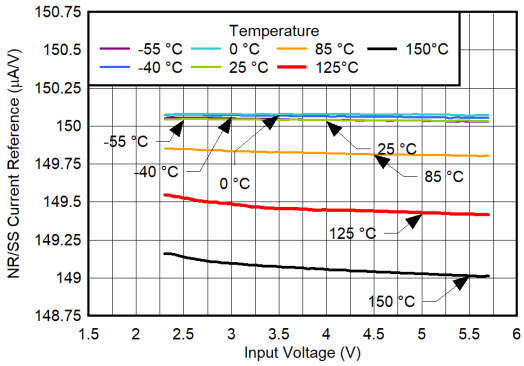


図 6-44. $I_{NR/SS}$ vs V_{IN} and Temperature for V_{OUT} = 1.8 V

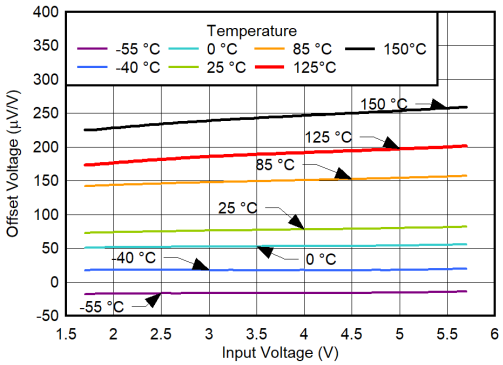


図 6-45. V_{OS} vs V_{IN} and Temperature for V_{OUT} = 1.8 V

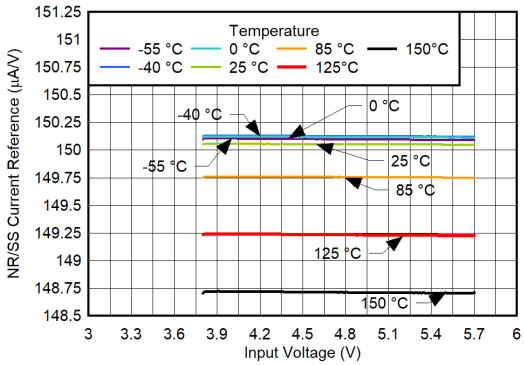


図 6-46. $I_{NR/SS}$ vs V_{IN} and Temperature for V_{OUT} = 3.3 V

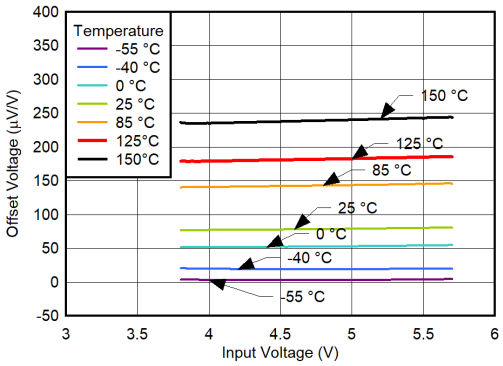


図 6-47. V_{OS} vs V_{IN} and Temperature for V_{OUT} = 3.3 V

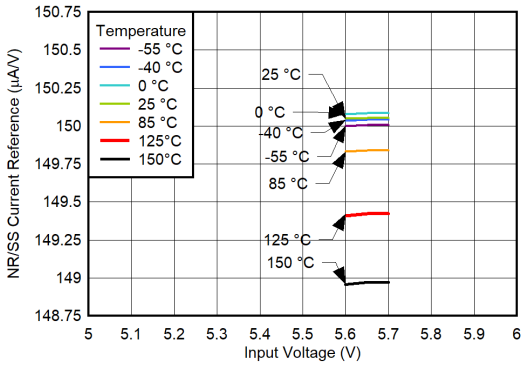


図 6-48. $I_{NR/SS}$ vs V_{IN} and Temperature for V_{OUT} = 5.1 V

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6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C

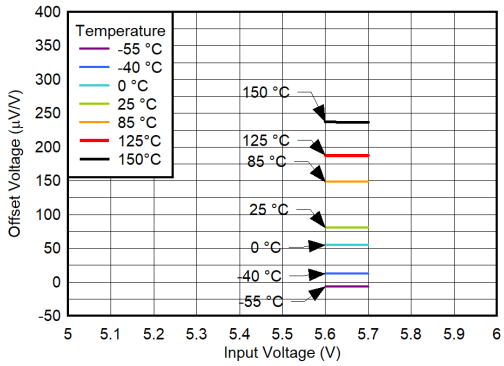


図 6-49. V_{OS} vs V_{IN} and Temperature for V_{OUT} = 5.1 V

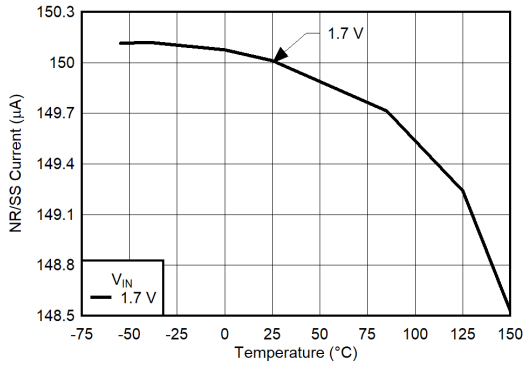


図 6-50. $I_{NR/SS}$ vs Temperature for V_{IN_Min}, V_{OpHr} = 0.2 V

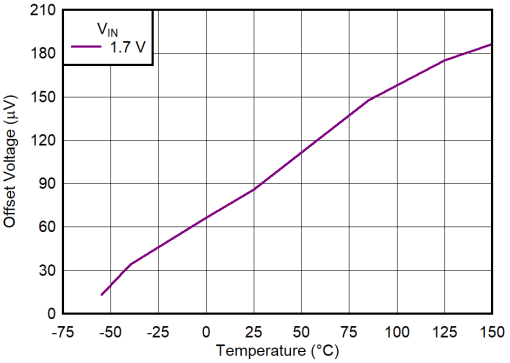


図 6-51. V_{OS} vs Temperature for V_{IN_Min}, V_{OpHr} = 0.2 V

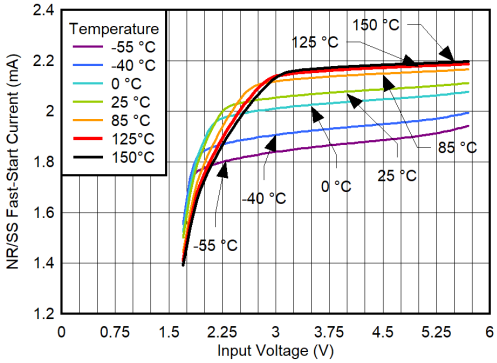


図 6-52. $I_{NR/SS}$ Fast-Start vs V_{IN} and Temperature

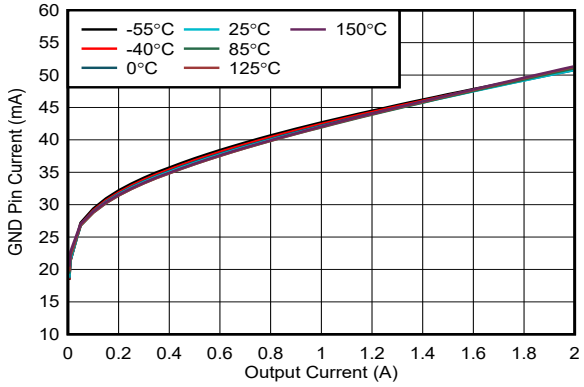


図 6-53. GND Pin Current vs I_{OUT} and Temperature for V_{OUT} = 3.3 V

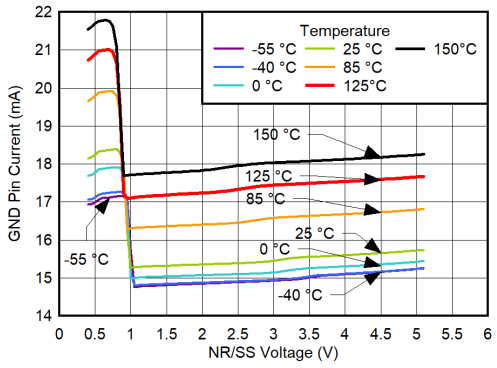
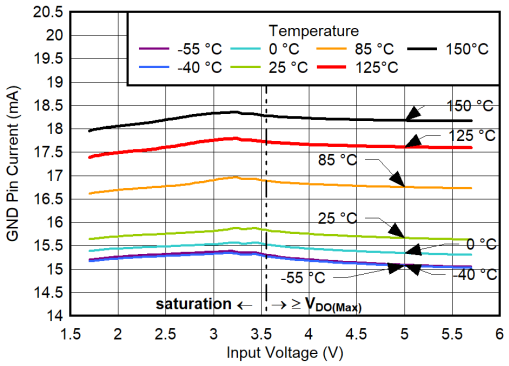


図 6-54. GND Pin Current vs $V_{NR/SS}$ and Temperature

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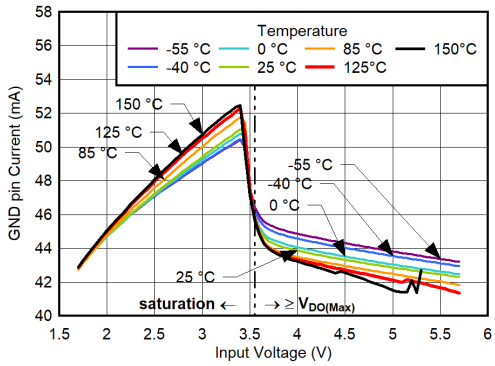
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



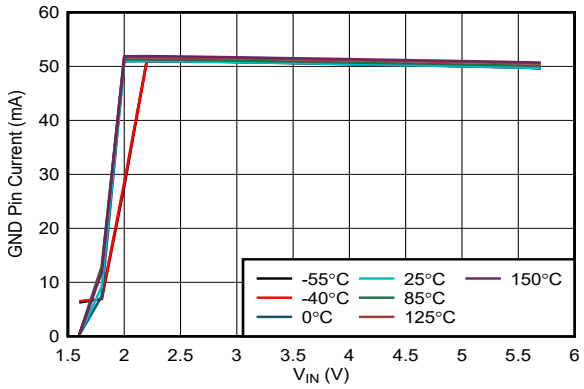
V_{OpHr} = 500 mV

図 6-55. GND Pin Current vs V_{IN} and Temperature for I_{OUT} = 1 mA



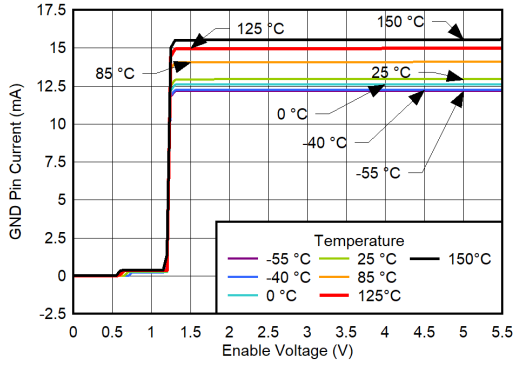
V_{OUT} = V_{IN} – 0.5 V

図 6-56. GND Pin Current vs V_{IN} and Temperature for I_{OUT} = 1 A



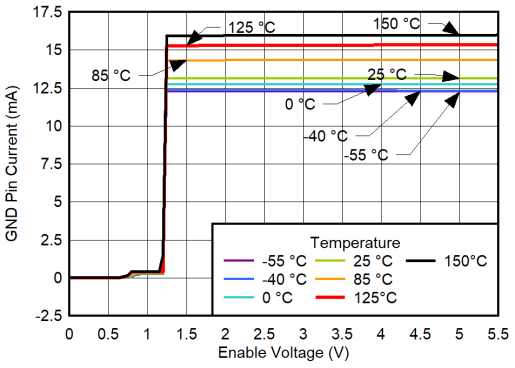
V_{OUT} = V_{IN} – 0.5 V

図 6-57. GND Pin Current vs V_{IN} and Temperature for I_{OUT} = 2 A



I_{OUT} = 0 mA, V_{OUT} = 3.3 V

図 6-58. GND Pin Current vs V_{EN} and Temperature for V_{IN} = 1.7 V (Dropout Operation)



I_{OUT} = 0 mA, V_{OUT} = 3.3 V

図 6-59. GND Pin Current vs V_{EN} and Temperature for V_{IN} = 5.7 V

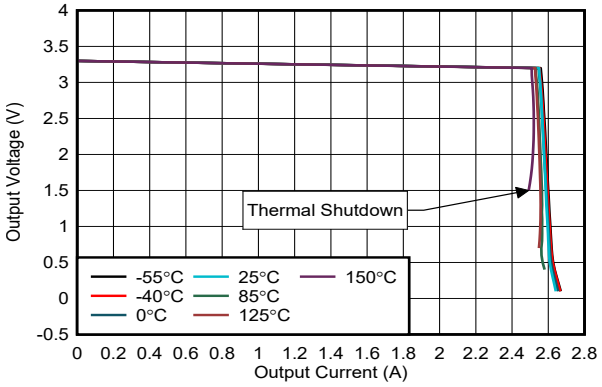


図 6-60. 100% Current Limit vs Temperature for V_{OUT} = 3.3 V

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6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C

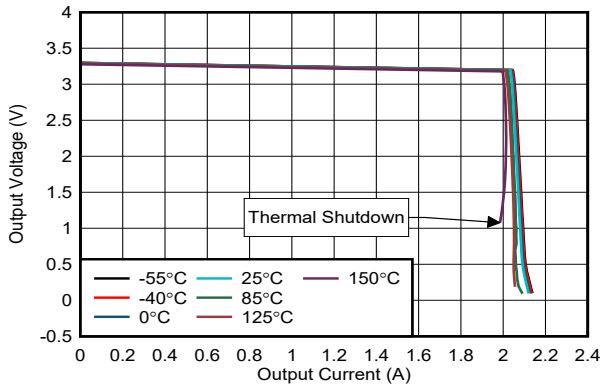


図 6-61. 80% Current Limit vs Temperature for V_{OUT} = 3.3 V

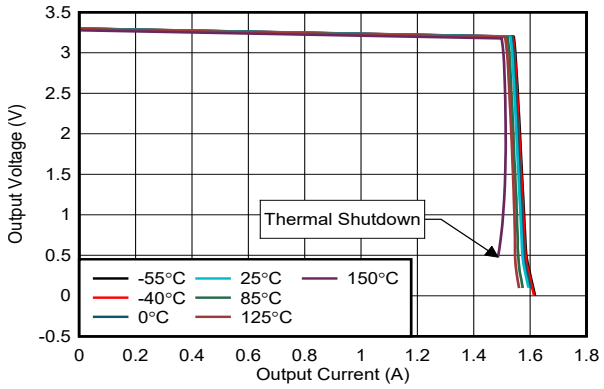
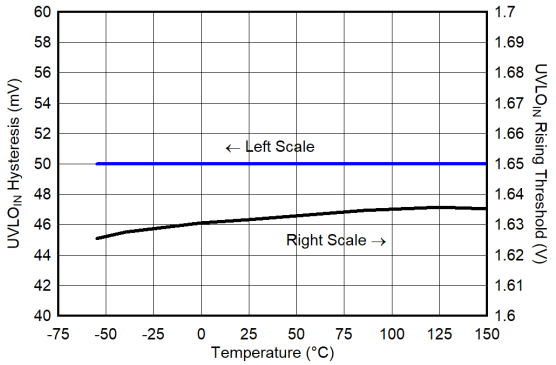
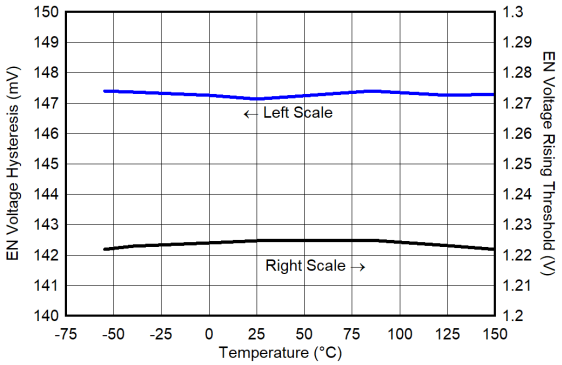


図 6-62. 60% Current Limit vs Temperature for V_{OUT} = 3.3 V



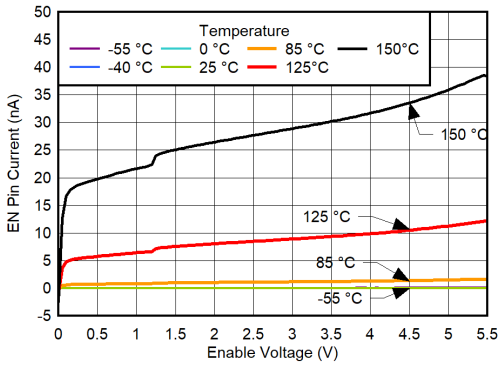
I_{OUT} = 0 mA

図 6-63. $UVLO_{IN}$ vs Temperature



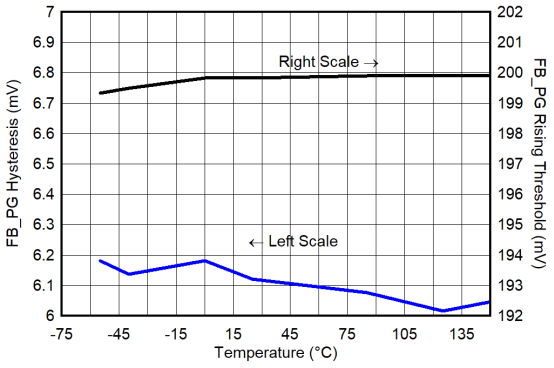
I_{OUT} = 0 mA

図 6-64. V_{EN} Hysteresis and Threshold vs Temperature



I_{OUT} = 0 mA

図 6-65. EN Pin Current vs V_{EN} and Temperature for V_{IN} = 5.7 V



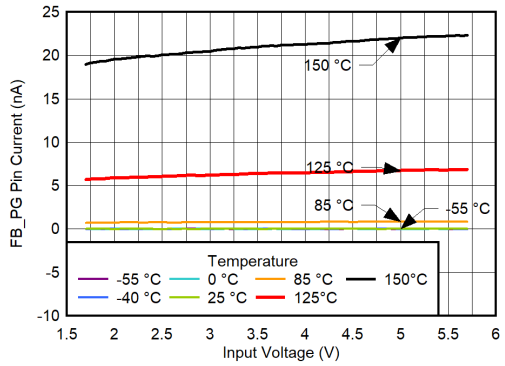
I_{OUT} = 0 mA

図 6-66. V_{FB_PG} Hysteresis and Threshold vs Temperature

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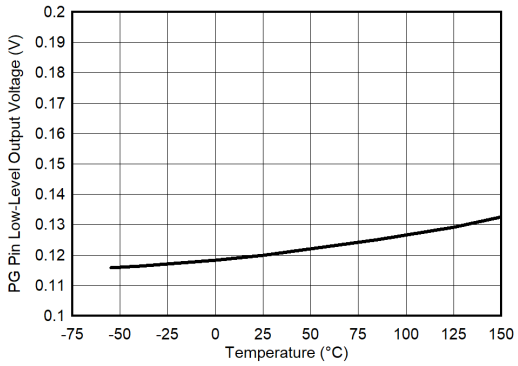
6.6 Typical Characteristics (continued)

at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 10 µF, and I_{OUT} = 1 mA (unless otherwise noted); typical values are at T_J = 25°C



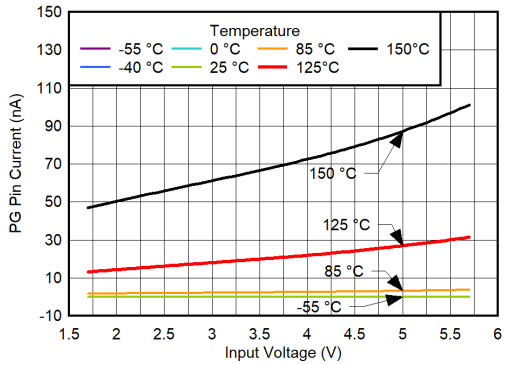
I_{OUT} = 0 mA

図 6-67. FB_PG Pin Current vs V_{IN} and Temperature



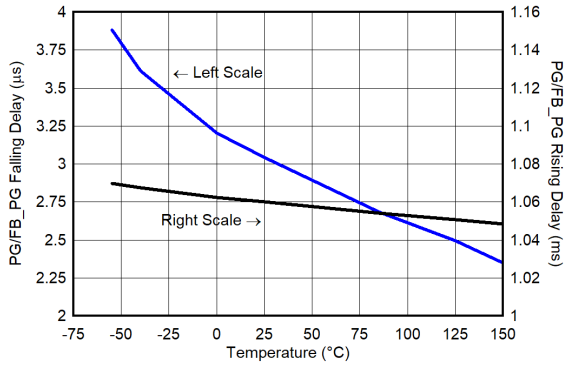
I_{PG} = –1 mA, V_{IN} = 1.7 V, I_{OUT} = –1 mA

図 6-68. V_{PG} Low-Level Output Voltage vs Temperature



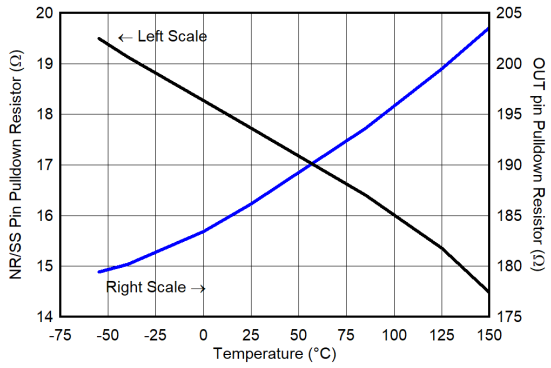
I_{OUT} = 0 mA

図 6-69. PG Pin Current vs V_{IN} and Temperature



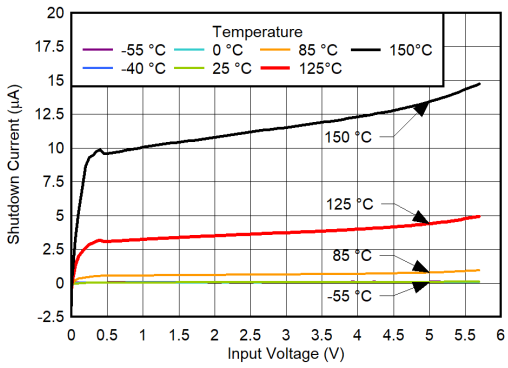
I_{OUT} = 0 mA

図 6-70. FB_PG Pin to PG Pin Rising and Falling Delay vs Temperature



I_{OUT} = 0 mA

図 6-71. NR/SS and OUT Pulldown Resistors vs Temperature



I_{OUT} = 0 mA

図 6-72. Shutdown Current vs V_{IN} and Temperature

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7 Detailed Description

7.1 Overview

The TPS7A96 is an ultra-low noise (0.5 μV_{RMS} over 10-Hz to 100-kHz bandwidth), ultra-high PSRR (> 50 dB to 2 MHz), high-accuracy (1%), low-dropout (LDO) linear voltage regulator with an input range of 1.9 V to 5.7 V and an output voltage range from 0 V to $V_{IN} – V_{DO}$ and is fully specified above 0.4 V_{OUT}. This LDO regulator uses innovative circuitry to achieve wide bandwidth and high loop gain, resulting in ultra-high PSRR even when operating under very low operational headroom ($V_{IN} – V_{OUT}$). At a high level, the device has two main blocks (the current reference and the unity-gain LDO buffer) and a few secondary features (such as the precision enable, current limit, and PG pin).

The current reference is controlled by the NR/SS pin. This pin sets the output voltage with a single resistor, sets the start-up time, and filters the noise generated by the reference and external set resistor.

The unity-gain LDO buffer is controlled by the OUT pin. The ultra-low noise does not increase with output voltage and provides wideband PSRR. As such, the SNS pin is only used for remote sensing of the load.

The EN_UV pin sets the precision enable feature. Select the optimal input voltage at which the LDO starts at. There are two independent UVLO voltages in this device: the internal IN rail UVLO and the EN_UV pin.

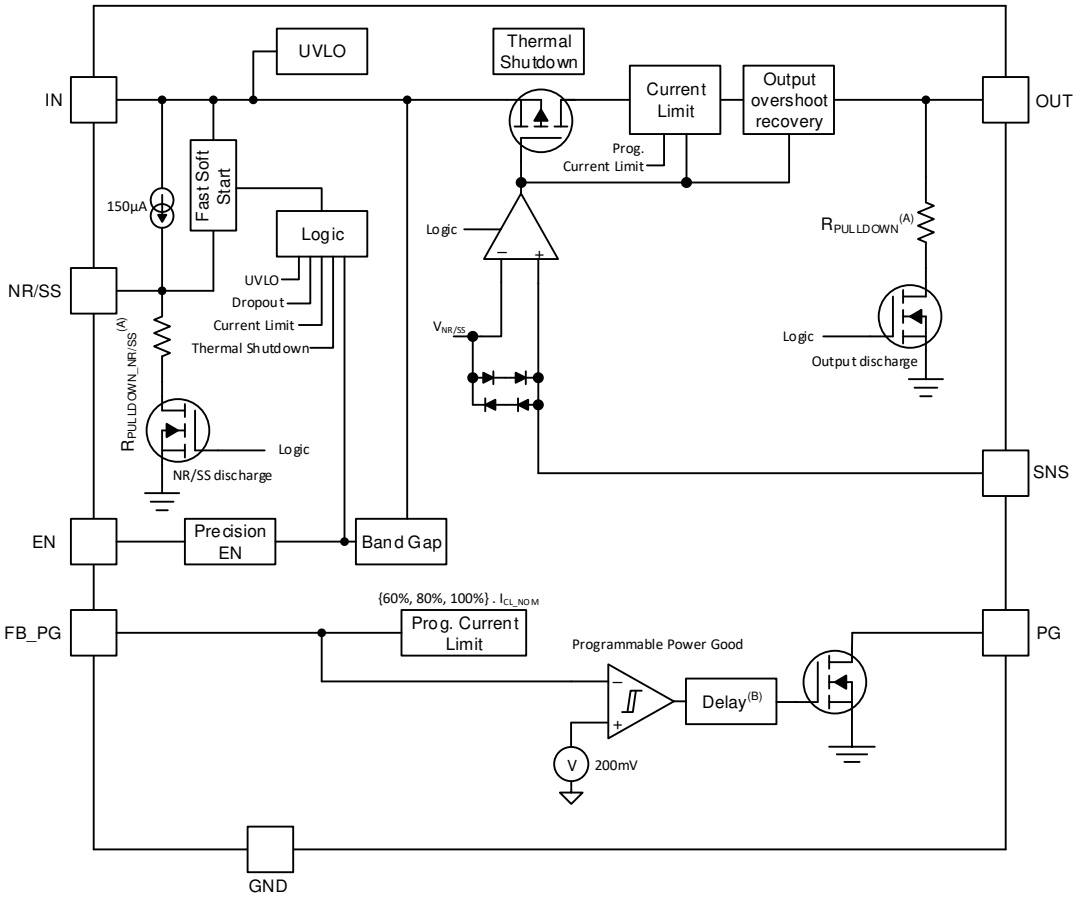
The FB_PG pin sets the current limit and power-good (PG) features. A voltage divider on this pin programs both the current limit and the PG trip point.

An ultra-low-noise current reference (150 µA, typical) is used in conjunction with an external resistor ($R_{NR/SS}$) to set the output voltage. This process allows the output voltage range to be set from 0.4 V to ($V_{IN} – V_{DO}$). To achieve this ultra-low noise, an external capacitor $C_{NR/SS}$ (typically 4.7 µF) is placed in parallel to the $R_{NR/SS}$ resistor used to set the output voltage. The unity-gain architecture provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

This regulator offers programmable current-limit, thermal protection, is fully specified from –40°C to +125°C above 0.4 V_{OUT}, and is offered in a thermally efficient 10-pin, 3-mm × 3-mm WSON package.

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7.2 Functional Block Diagram

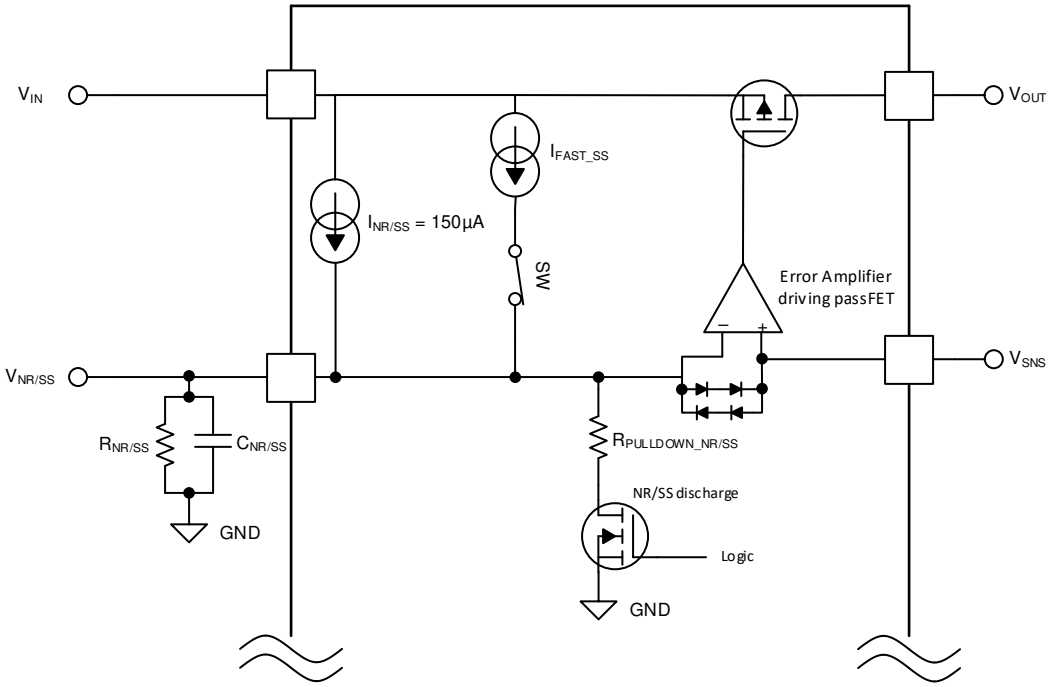


A. See the $R_{PULLDOWN}$ output active discharge resistance value in the *Electrical Characteristics* table.
B. See the delay value in the *Electrical Characteristics* table.

7.3 Feature Description

7.3.1 Output Voltage Setting and Regulation

図 7-1 shows a simplified regulation circuit, where the input signal ($V_{NR/SS}$) is generated by the internal current source ($I_{NR/SS}$) and the external resistor ($R_{NR/SS}$). Because the error amplifier is always operating in unity-gain configuration, the LDO output voltage is directly programmed by the NR/SS pin voltage ($V_{NR/SS}$). The $V_{NR/SS}$ reference voltage is generated by an internal low-noise current source driving the $R_{NR/SS}$ resistor and is designed to have very low bandwidth at the input to the error amplifier through the use of a low-pass filter ($C_{NR/SS}$ || $R_{NR/SS}$).



$V_{OUT} = I_{NR/SS} \times R_{NR/SS}$.

図 7-1. Simplified Regulation Circuit

This unity-gain configuration, along with the highly accurate $I_{NR/SS}$ reference current, enables the device to achieve excellent output voltage accuracy. However, the $R_{NR/SS}$ accuracy can become the limiting factor when operating at low output voltage. The low-dropout voltage (V_{DO}) provides reduced thermal dissipation and achieves robust performance. This combination of features makes this device an excellent voltage source for powering sensitive analog low-voltage devices.

7.3.2 Ultra-Low Noise and Ultra-High Power-Supply Rejection Ratio (PSRR)

The architecture features a highly accurate, high-precision, low-noise current reference followed by a state-of-the-art error amplifier (1.1 nV/$\sqrt{\text{Hz}}$ at 10-kHz noise for V_{OUT} ≥ 1.2 V) comparable to, if not better than, that of a precision amplifier. The unity-gain configuration provides ultra-low noise over the entire output voltage range. Additional noise reduction and higher output current can be achieved by placing multiple TPS7A96 LDOs in parallel.

7.3.3 Programmable Current Limit and Power-Good Threshold

The brick-wall current limit can be programmed to either 100%, 80%, or 60% of the nominal factory-programmed value by setting the input impedance for the FB_PG pin. Similarly, the power-good indication threshold can also be adjusted between 85% and 95% of the nominal output voltage by changing the FB_PG resistor divider ratio; see the *Adjusting the Factory-Programmed Current Limit* section for details.

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7.3.4 Programmable Soft-Start (NR/SS Pin)

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that uses the $C_{NR/SS}$ capacitor to minimize inrush current into the output capacitor and load during start up. This circuitry can also reduce the start-up time for some applications that require the output voltage to reach at least 90% of the set value. See the *Programmable Soft-Start and Noise-Reduction (NR/SS Pin)* section for more details.

7.3.5 Precision Enable and UVLOs

Two independent undervoltage lockout (UVLO) circuits are present. An internally set UVLO on the input supply (IN pin) disables the LDO when the input voltage reaches the minimum threshold. A precision EN function (EN_UV pin) can also be used as a user-programmable UVLO.

- The input supply voltage UVLO circuit prevents the regulator from turning on when the input voltage is not high enough; see the *Electrical Characteristics* table for more details.
- The precision enable circuit allows for a simple sequencing of multiple power supplies with a resistor divider from another supply. This enable circuit can be used to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN_UV pin; see the *Precision Enable (External UVLO)* section for more details.

7.3.6 Active Discharge

The device incorporates two internal pulldown metal-oxide semiconductor field effect transistors (MOSFETs). The first pulldown MOSFET connects a resistor ($R_{PULLDOWN}$) from OUT to ground when the device is disabled to actively discharge the output capacitor. The second pulldown MOSFET connects a resistor ($R_{PULLDOWN_NR/SS}$) from NR/SS to ground when the device is disabled and discharges the NR/SS capacitor. Both pulldown MOSFETs are activated by any one or more of the following:

- Driving the EN_UV pin below the $V_{EN(LOW)}$ threshold
- The IN pin voltage falling below the undervoltage lockout V_{UVLO} threshold
- Having the output voltage greater than the input voltage

7.3.7 Thermal Shutdown Protection (T_{SD})

A thermal shutdown protection circuit disables the LDO when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical). The thermal time constant of the semiconductor die is fairly short, thus the device can cycle off and on when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors.

Under some conditions, the thermal shutdown protection can disable the device before start-up completes. For reliable operation, limit the junction temperature to the maximum listed in the *Electrical Characteristics* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN_UV}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN_UV} > V_{IH(EN_UV)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN_UV} > V_{IH(EN_UV)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$ or $V_{IN} < V_{OUT}$ + 90 mV or $V_{IN} < V_{NR/SS}$ + 20 mV	$V_{EN_UV} < V_{IL(EN_UV)}$	Not applicable	$T_J > T_{SD}$
Current-limit operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN_UV} > V_{IH(EN_UV)}$	$I_{OUT} \geq I_{CL(min)}$	$T_J < T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < TSD_{(shutdown)}$)
- The voltage on the EN_UV pin has previously exceeded the $V_{IH(EN_UV)}$ threshold voltage and has not yet decreased to less than the $V_{IL(EN_UV)}$ falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

注

While in dropout, if a heavy load transient event forces $V_{IN} < V_{OUT(NOM)}$ + 90 mV or $V_{IN} < V_{NR/SS}$ + 20 mV, the device restarts to prevent the output voltage from overshooting to protect the device and load.

When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

For additional information, see the *Output Voltage Restart (Overshoot Prevention Circuit)* section.

7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the EN_UV pin to less than the $V_{IL(EN_UV)}$ threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and both the NR/SS pin and OUT pin voltages are actively discharged to ground by internal discharge circuits to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

7.4.4 Current-Limit Operation

If the output current is greater than or equal to the minimum current limit, ($I_{CL(Min)}$), then the device operates in current-limit mode. The current limit is brick-wall scheme and is programmable with the PG_FB pin. For additional information, see the *Adjusting the Factory-Programmed Current Limit* section.

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8 Application and Implementation

注

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8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 Output Voltage Restart (Overshoot Prevention Circuit)

Wide bandwidth linear regulators suffer from an undesirable excessive overshooting of the output voltage during restart events that occur when the $C_{NR/SS}$ and C_{OUT} capacitors are not fully discharged. In this device, and as shown in 図 8-1, this undesirable behavior is mitigated by implementing low hysteresis circuitry consisting of two ORed comparators to detect when the input voltage is either 20 mV (typical) lower than the $V_{NR/SS}$ reference voltage or 300 mV (typical) lower than V_{OUT}.

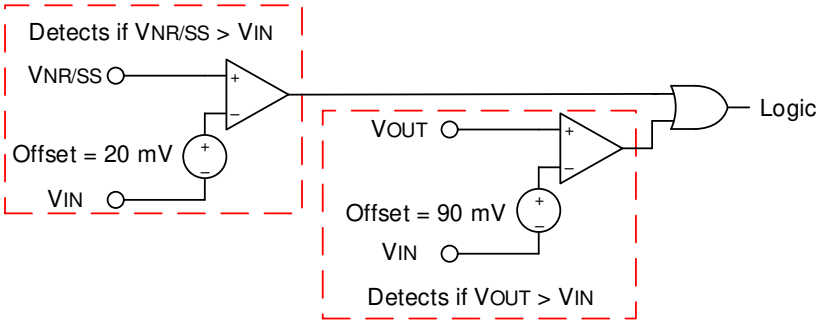


図 8-1. Overshoot Prevention Circuit

When the device is operating in dropout, transient events (such as an input voltage brownout, heavy load transient, or short-circuit event) can force the device in a reversed bias condition where the input voltage is either 20 mV (typical) lower than the $V_{NR/SS}$ reference voltage or 300 mV (typical) lower than V_{OUT}. The output overshoot prevention circuit can be triggered, as shown in 図 8-2, thus forcing the device to shutdown and restart, thereby preventing output voltage overshoot. If the device is still operating in dropout and the error condition that triggered this circuit is still present, an additional restart can occur until these conditions are removed or the device is no longer in dropout. The restart always occurs from a discharged state and always has the same characteristics as the initial LDO power-up, so the start-up time, V_{OUT} ramp rate, and V_{OUT} monotonicity are all predictable.

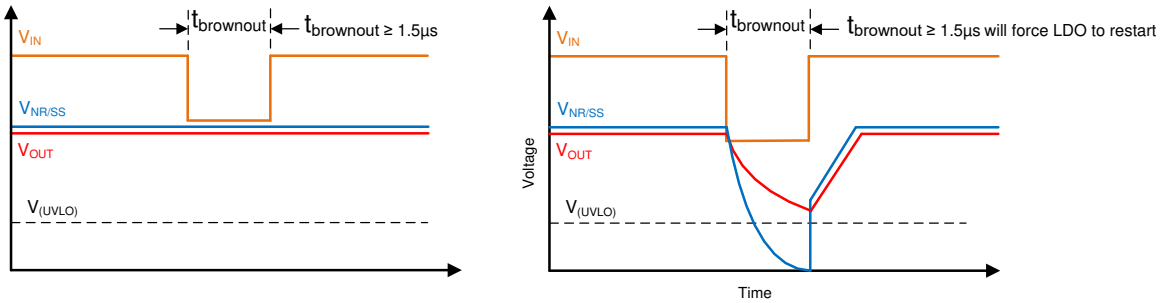


図 8-2. Device Behavior in Dropout

図 8-3 and 図 8-4 show examples of a soft brownout and a brownout event, respectively.

The brownout overshoot is present with higher V_{IN} slew rates. A 1-V/µs slew rate was used in 図 8-5.

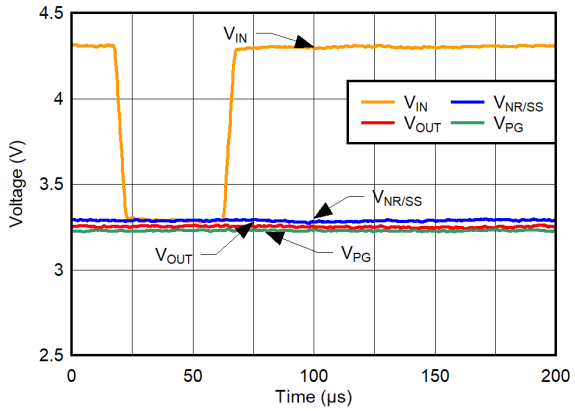


図 8-3. Example: Soft Brownout to $V_{NR/SS}$

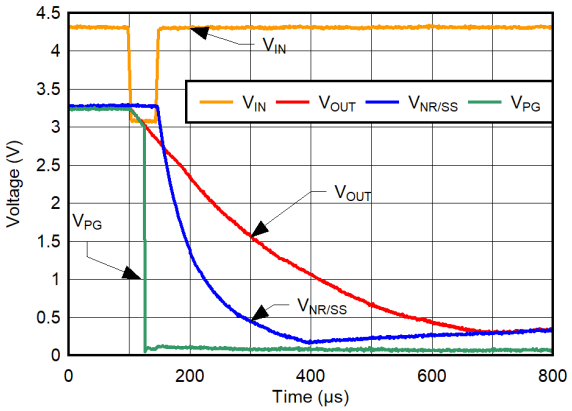


図 8-4. Example: Brownout

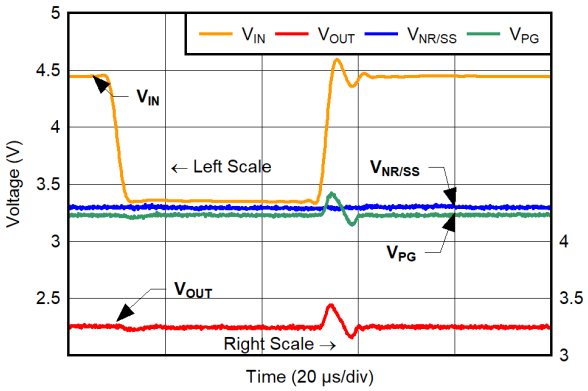


図 8-5. Example: Brownout With Overshoot Recovery

The overshoot prevention circuit is implemented to provide a predictable start-up and shutdown of the device without output overshoot if the EN_UV external UVLO is not used as described in this section. This circuit can be prevented from triggering by:

1. Using an input supply capable of handling heavy load transients or a larger value input capacitor
2. Increasing the operating headroom between V_{IN} and V_{OUT} (for example, when using a battery as an input supply to make sure that V_{IN} stays higher than V_{OUT} even when the battery is near the full discharge state)
3. Using an input supply with a ramp rate faster than the set output voltage time constant formed by $C_{NR/SS}$ || $R_{NR/SS}$
4. Discharging the input supply slower than the discharge time formed by C_{OUT} || (Load || $R_{PULLDOWN}$) or by the $C_{NR/SS}$ || ($R_{NR/SS}$ || $R_{PULLDOWN_NR/SS}$)

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8.1.2 Precision Enable (External UVLO)

The precision enable circuit is used to turn the device on and off. This circuit can be used to set an external undervoltage lockout (UVLO) voltage (図 8-6) to turn on and off the device using a resistor divider between IN, EN_UV, and GND.

If $V_{EN_UV} \geq V_{IH(EN_UV)}$, the regulator is enabled. If $V_{EN_UV} \leq V_{IL(EN_UV)}$, the regulator is disabled. The EN_UV pin does not incorporate an internal pulldown resistor to GND and must not be left floating. Use the precision enable circuit for this pin to set an external UVLO input supply voltage to turn on and off the device with a resistor divider between IN, EN_UV, and GND.

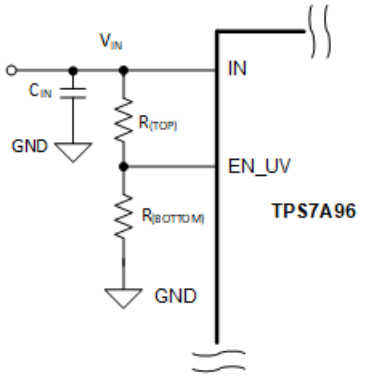


図 8-6. Precision EN Used as External UVLO

This external UVLO configuration prevents the LDO from turning on when the input supply voltage is insufficient and places the device in dropout operation.

Using the EN_UV pin as an externally set UVLO allows simple sequencing of cascaded power supplies. An additional benefit is that the EN_UV pin is never left floating. The EN_UV pin does not have an internal pulldown resistor. In addition to the resistor divider, a zener diode can be needed between the EN_UV pin and ground to comply with the absolute maximum ratings on this pin.

When V_{IN} exceeds the targeted V_{ON} voltage and the $R_{(BOTTOM)}$ resistor is set, 式 1 and 式 2 provide the $R_{(TOP)}$ resistor value and the V_{OFF} voltage at which the input voltage must drop below to disable the LDO.

$$R_{TOP} \leq R_{BOTTOM} \times \left(\frac{V_{ON}}{V_{IH(EN_UV)}} - 1 \right) \quad (1)$$

$$V_{(OFF)} < \left[\frac{R_{TOP}}{R_{BOTTOM}} + 1 \right] \times \left(V_{IH(EN_UV)} - V_{HYS(EN_UV)} \right) \quad (2)$$

where:

- V_{OFF} is the input voltage where the regulator shuts off
- V_{ON} is the voltage where the regulator turns on

Consider the EN_UV current pin when selecting the $R_{(TOP)}$ and $R_{(BOTTOM)}$ values.

8.1.3 Undervoltage Lockout (UVLO) Operation

The UVLO circuit, present on the IN pin, makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The $UVLO_{IN}$ circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 1.6 V causes the input supply UVLO to assert for a short time. However, the $UVLO_{IN}$ circuit can possibly not have enough stored energy to fully discharge the internal circuits inside of the device. When the $UVLO_{IN}$ circuit does not fully discharge, internal circuitry is not fully disabled.

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The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the solution proposed in the *Precision Enable (External UVLO)* section.

図 8-7 shows the $UVLO_{IN}$ circuit response to various input voltage events. This diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output can fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

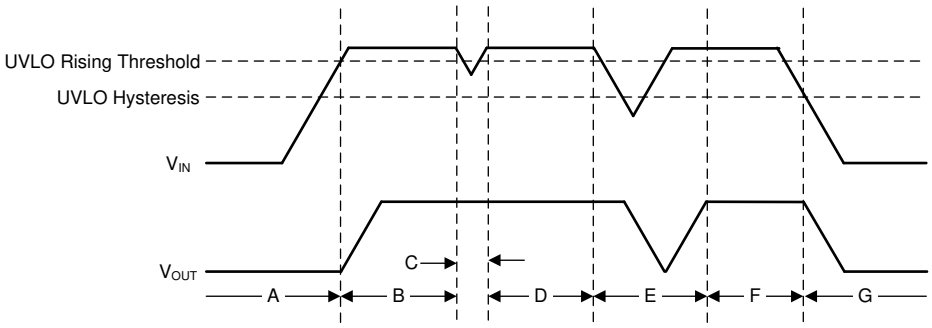


図 8-7. Typical UVLO Operation

8.1.4 Dropout Voltage (V_{DO})

Dropout voltage refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$) that is required for regulation. When the input voltage (V_{IN}) drops to or below the maximum dropout voltage ($V_{DO(Max)}$) for the given load current, see the *Electrical Characteristics* table, the device functions as a resistive switch and does not regulate the output voltage. When the device is operating in dropout, the output voltage tracks the input voltage. For high current, the dropout voltage (V_{DO}) is proportional to the output current because the device is operating as a resistive switch. For low current, internal nodes are saturating and the dropout plateaus to the minimum value. As mentioned in the *Output Voltage Restart (Overshoot Prevention Circuit)* section, transient events such as an input voltage brownout, heavy load transient, or short-circuit event can trigger the overshoot prevention circuit. Operating the device at or near dropout significantly degrades both transient performance and PSRR, and can also trigger the overshoot prevention circuit. Maintaining sufficient operating headroom ($V_{OpHr} = V_{IN} – V_{OUT}$) significantly improves the device transient performance and PSRR, and prevents triggering the overshoot prevention circuit.

注

For this device, the pass transistor does not limit the dropout voltage factor. Because the reference voltage is generated by a current source and the NR/SS resistor, and because the operating headroom is reducing (even at low load), the internal current source ($I_{NR/SS}$) saturates faster than the pass transistor. This behavior is described in the dropout voltage plot (図 6-33). Notice that the dropout does not go to 0 V.

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8.1.5 Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)

For proper device operation, the resistor divider network input to the FB_PG pin must be connected. The FB_PG pin must not be left floating because this pin represents an analog input to the device internal logic and the input impedance is sampled during device start up.

The PG pin is an output indicating whether the LDO is ready to provide power. This pin is implemented using an open-drain architecture. The FB_PG pin programs the PG pin and serves a dual purpose of programming the PG threshold assert voltage and adjusting the current limit, I_{CL}.

The PG pin must use the minimum value or larger pullup resistor from PG to IN, as shown in 図 8-8, or the external rail as listed in the *Electrical Characteristics* table. If PG functionality is not used, leave this pin floating or connected to GND.

The FB_PG pin uses the parallel impedance formed by the resistor divider $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ to program the current limit value during LDO initialization. If this impedance is less than 12.5 kΩ, then the nominal factory-programmed, current-limit value is selected. If the input impedance is less than 50 kΩ, but greater than 12.5 kΩ, then 80% of the nominal factory-programmed current limit is selected. If the input impedance is less than 100 kΩ, but greater than 50 kΩ, then 60% of the nominal factory-programmed current limit is selected. Connect the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors as indicated in this section for proper operation of the LDO. Do not float this pin.

When initialization is complete, the voltage divider provides the necessary feedback to the PG pin by setting the PG assert threshold voltage.

To properly select the values of the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors, see the *Adjusting the Factory-Programmed Current Limit* section for detailed explanation and calculation.

注

The $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistor divider ratio sets the power-good assert threshold voltage between 85% to 95% of the V_{FB_PG} voltage for 60% and 80% of the nominal factory-programmed current limit.

If the current limit is set for 100% of the nominal factory-programmed current limit, the PG threshold range is not limited. A PG threshold greater than 80% is common for systems where start-up inrush current must be minimized. Lower PG thresholds can be needed in systems with fast start-up time constraints.

Setting the PG threshold based off the V_{FB_PG} voltage sets the PG to assert when the output voltage reaches the corresponding percentage level of V_{FB_PG} because V_{FB_PG} is a scaled version of the output voltage.

図 8-8 shows the internal circuitry for both the FB_PG and PG pins.

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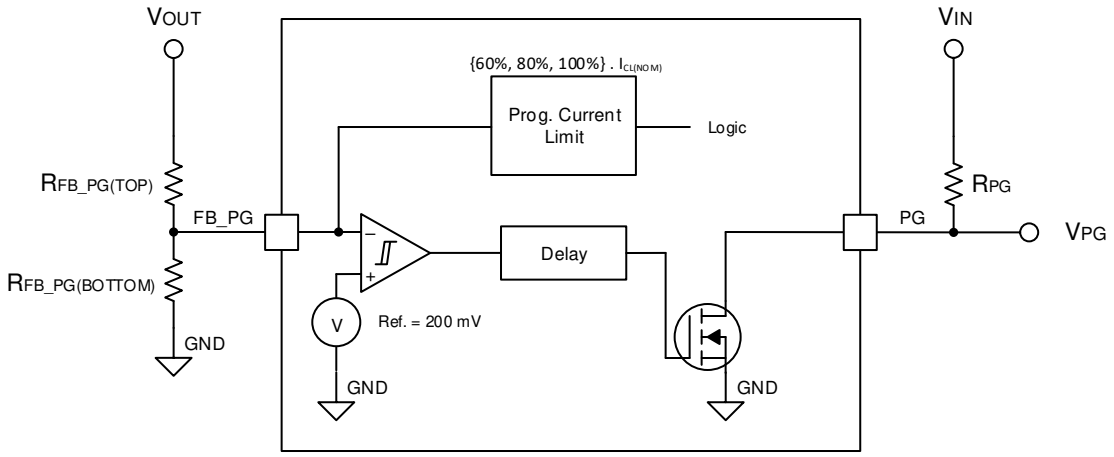


図 8-8. Programmable Power-Good Threshold Simplified Schematic

The PG pin pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal can possibly not read a valid digital logic level.

The state of the PG signal is only valid when the FB_PG pin resistor divider network is set properly and the device is in normal operating mode.

8.1.6 Adjusting the Factory-Programmed Current Limit

The current limit is a brick-wall scheme and the factory-programmed current limit value can be programmed to a set of discrete values (100%, 80%, or 60% of the default value), as specified in the *Electrical Characteristics* table. This adjustment can be done by changing the input impedance of the FB_PG pin represented by the parallel resistance of $R_{FB_PG(TOP)}$ || $R_{FB_PG(BOTTOM)}$. The FB_PG pin has dual functionality of adjusting the I_{CL} value and setting the power-good (PG) assert threshold.

Prior to start-up, the input impedance of the FB_PG pin is sampled and the I_{CL} value is adjusted based on the input impedance.

Current limit programmability is dependent on the output voltage. For voltages below 0.4 V, the current limit cannot be programmed. For voltages between 0.4 V and 1.2 V, the current limit cannot be adjusted and is always set to 100%. 表 8-1 describes this behavior.

表 8-1. Programmable Current Limit vs Output Voltage

NOMINAL OUTPUT VOLTAGE (V)	$R_{FB_PG(BOTTOM)}$ (kΩ)	$R_{FB_PG(TOP)}$ (kΩ)	I_{CL} SETTING (%)
$V_{OUT(nom)}$ ≥ 1.2 V	$R_{FB_PG(BOTTOM)}$ = 0.2 V / 16 µA	$R_{FB_PG(TOP)} = R_{FB_PG(BOTTOM)} \times (V_{OUT(nom)} / 0.2\ V \times K - 1)$ with K = PG threshold (%V_{OUT})	100
	$R_{FB_PG(BOTTOM)}$ = 0.2 V / 4 µA		80
	$R_{FB_PG(BOTTOM)}$ = 0.2 V / 2 µA		60
0.4 V ≤ $V_{OUT(nom)}$ < 1.2 V	$R_{FB_PG(BOTTOM)}$ = 0.2 V / 6 µA		100

表 8-2 provides values for various output voltages using 1% resistors.

表 8-2. Programmable Current Limit Voltage-Divider Current Settings

NOMINAL OUTPUT VOLTAGE (V)	$R_{FB_PG(BOTTOM)}$ (kΩ)	$R_{FB_PG(TOP)}$ (kΩ)	I_{CL} SETTING (%)	PG THRESHOLD (%)
$V_{OUT(nom)}$ = 1.2 V	12.4	51.1	100	85
	49.9	205	80	85
	100	412	60	85

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表 8-2. Programmable Current Limit Voltage-Divider Current Settings (continued)

NOMINAL OUTPUT VOLTAGE (V)	$R_{FB_PG(BOTTOM)}$ (kΩ)	$R_{FB_PG(TOP)}$ (kΩ)	I_{CL} SETTING (%)	PG THRESHOLD (%)
$V_{OUT(nom)}$ = 3.3 V	12.4	187	100	95
	49.9	732	80	95
	100	1470	60	95
$V_{OUT(nom)}$ = 5.1 V	12.4	287	100	95
	49.9	1150	80	95
	100	2320	60	95

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図 8-9 shows the different I_{CL} settings for a nominal 3.3-V output voltage.

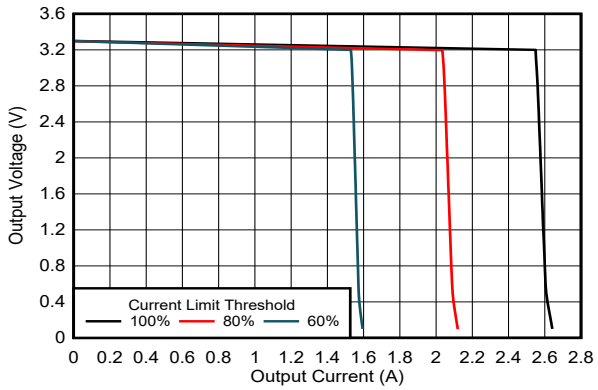


図 8-9. Programmable Current Limit Behavior (Typical) for a 3.3-$V_{OUT(nom)}$

8.1.7 Programmable Soft-Start and Noise-Reduction (NR/SS Pin)

The NR/SS pin is the input to the inverting terminal of the error amplifier, see the *Functional Block Diagram*. A resistor connected from this pin to GND sets the output voltage by the pin internal reference current $I_{NR/SS}$, as given in the following equation:

$$V_{OUT} = I_{NR/SS} \times R_{NR/SS} \quad (3)$$

Connecting a capacitor from this pin to GND significantly reduces the output noise, limits the input inrush-current, and soft-starts the output voltage. Use the minimum value or larger capacitor from NR/SS to ground as listed in the *Electrical Characteristics* table and place the NR/SS capacitor as close to the NR/SS and GND pins of the device as possible.

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor ($C_{NR/SS}$). In addition to the soft-start feature, the $C_{NR/SS}$ capacitor also lowers the output voltage noise of the LDO. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a monotonic start-up, the device output voltage tracks the $V_{NR/SS}$ reference voltage until this reference reaches the set value (the set output voltage). The $V_{NR/SS}$ reference voltage is set by the $R_{NR/SS}$ resistor and, during start-up, using a fast charging current (I_{FAST_SS}) in addition to the $I_{NR/SS}$ current, as illustrated in 図 8-10, to charge the $C_{NR/SS}$ capacitor.

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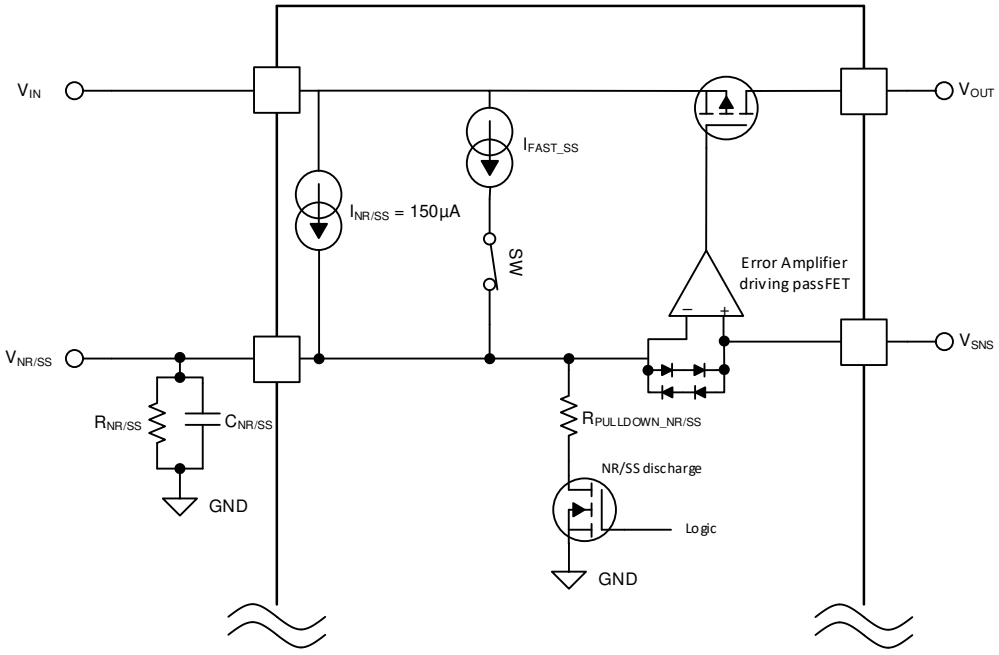


図 8-10. Simplified Soft-Start Circuit

The 2.1-mA (typical) I_{FAST_SS} current and 150-µA (typical) $I_{NR/SS}$ current quickly charge $C_{NR/SS}$ until the voltage reaches approximately 93% of the set output voltage, then the I_{FAST_SS} current disengages and only the $I_{NR/SS}$ current continues to charge $C_{NR/SS}$ to the set output voltage level. If there is any error during start-up or the output overshoot prevention circuit is triggered, the NR/SS discharge FET turns on, thus discharging the $C_{NR/SS}$ capacitor to protect both the LDO and the load.

The soft-start ramp time depends on the fast start-up (I_{FAST_SS}) charging current, the reference current ($I_{NR/SS}$), $C_{NR/SS}$ capacitor value, and the set (targeted) output voltage ($V_{OUT(target)}$). 式 4 calculates the soft-start ramp time.

$$\text{Soft-Start Time } (t_{SS}) = \frac{V_{OUT(target)} \times C_{NR/SS}}{I_{NR/SS} + I_{FAST_SS}} \quad (4)$$

The $I_{NR/SS}$ current is provided in the *Electrical Characteristics* table and has a value of 150 µA (typical). The I_{FAST_SS} current has a value of 2 mA (typical) for V_{IN} > 2.5 V. 図 8-11 and 図 8-12 show the $I_{NR/SS}$ and I_{FAST_SS} current versus V_{IN} and temperature.

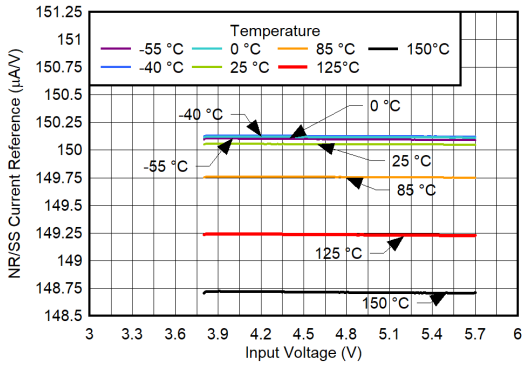


図 8-11. $I_{NR/SS}$ Reference vs Input Voltage and Temperature for V_{OUT} = 3.3 V

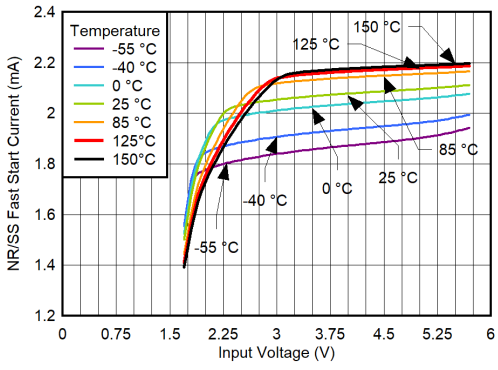


図 8-12. I_{FAST_SS} Reference vs Input Voltage and Temperature for V_{OUT} = 3.3 V

Because the error amplifier is always operating in unity-gain configuration, the output voltage noise can only be adjusted by increasing the $C_{NR/SS}$ capacitor. The $C_{NR/SS}$ capacitor and $R_{NR/SS}$ resistor form a low-pass filter (LPF) that filters out noise from the $V_{NR/SS}$ voltage reference, thereby reducing the device noise floor. The LPF is a single-pole filter and 式 5 calculates the LPF cutoff frequency. Increasing the $C_{NR/SS}$ capacitor can significantly lower output voltage noise; however, doing so greatly lengthens start-up time. For low-noise applications, use a 4.7-µF $C_{NR/SS}$ for optimal noise and start-up time trade off.

$$\text{Cutoff Frequency } (f_{cutoff}) = \frac{1}{2\pi \times R_{NR/SS} \times C_{NR/SS}} \quad (5)$$

The *Typical Characteristics* section illustrates the impact of the $C_{NR/SS}$ capacitor on the LDO output voltage noise.

図 8-13 shows the relationship, timing, and output voltage value during the start-up phase.

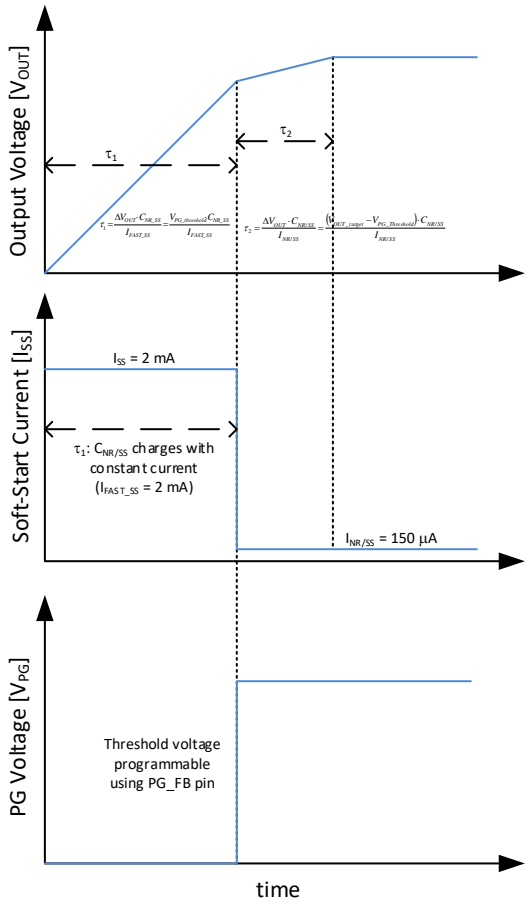


図 8-13. Relationship Between Threshold Voltage, Output Voltage, I_{FAST_SS}, and $I_{NR/SS}$ During Start-Up

8.1.8 Inrush Current

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed. Operating without an input capacitor is not recommended because this capacitor is required for stability. However, 式 6 can be used to estimate this current.

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$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (6)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

As illustrated in 図 8-10, the external capacitor at the NR/SS pin ($C_{NR/SS}$) sets the output start-up time by setting the rise time of the $V_{NR/SS}$ reference voltage.

Inrush current for a no-load condition is given in 図 6-28 to 図 6-31.

8.1.9 Optimizing Noise and PSRR

Noise can be generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output). Noise can easily be noticed in audio as a hissing or popping sound. Noise produced from an external circuit or the 50- to 60-hertz power-line noise (spikes), along with the harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry, such as resistors and transistors. The two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage ($V_{NR/SS}$). Extrinsic noise, including the switching mode power-supply ac ripple voltage, coupled onto the input supply of the LDO is attenuated by the LDO power-supply rejection ratio, or PSRR. PSRR is a measurement of the noise attenuation from the input to the output of the LDO.

Optimize the intrinsic noise and PSRR by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range up to the device bandwidth
- C_{OUT} for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, $V_{IN} – V_{OUT}$ (V_{DO}), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a lesser effect

These behaviors are described in the *Typical Characteristics* curves.

図 8-14 shows the measured PSRR for a 1.2-V device output voltage with a 0.7-V headroom for 1-A, 1.5-A, and 2-A load currents. 表 8-3 lists the typical output noise for these capacitors.

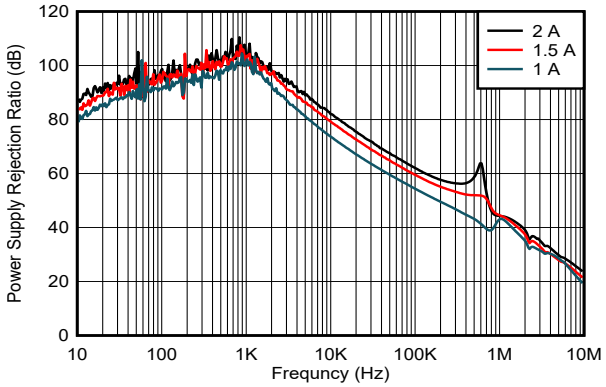


図 8-14. PSRR vs Frequency and I_{OUT} for V_{OUT} = 1.2 V, C_{OUT} = 10 µF

表 8-3. Typical Output Noise for 1.2-V_{OUT} vs $C_{NR/SS}$, C_{OUT}, and Typical Start-Up Time

V_n (μV_{RMS}), 10-Hz to 100-kHz BW	$C_{NR/SS}$ (μF)	C_{OUT} (μF)	START-UP TIME (ms)
0.98	1	10	3.73
0.62	2.2	10	6.21
0.489	4.7	10	13.97
0.42	10	10	28.21

PSRR can be viewed as being simply the ratio of the output capacitor impedance by the LDO output impedance. At low frequency, the output impedance is very low whereas the output impedance of the capacitor is high, resulting in high PSRR. As the frequency increases, the output capacitor impedance reduces and reaches a minima set by the ESR.

As given in 図 8-14, to achieve high PSRR at high frequencies, make sure that the output capacitor equivalent series resistance (ESR) and equivalent series inductance (ESL) are minimal. This figure shows how to use a single 10-μF output capacitor implementation. However, minimizing the ESR- and ESL-generated resonance point in the output capacitance allows for a smoother transition between the LDO active PSRR component to the passive PSRR of the capacitors, therefore using output capacitors in parallel helps above 200 kHz, improving the PSRR by 5 dB to 7 dB.

注

The TPS7A96 is optimized for the 1-A to 2-A output current range. For current below this range, consider the TPS7A94 device.

8.1.10 Adjustable Operation

As shown in 図 8-15, the output voltage of the device can be set using a single external resistor ($R_{NR/SS}$). 式 7 calculates the output voltage.

$$V_{OUT} = I_{NR/SS(NOM)} \times R_{NR/SS} \quad (7)$$

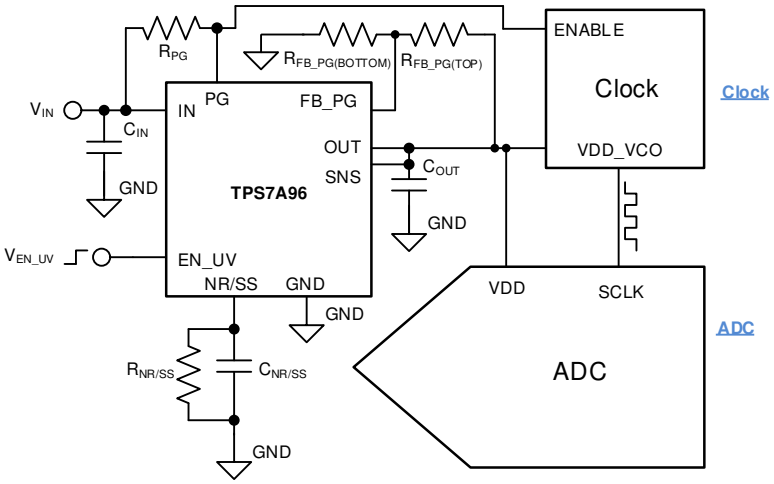


図 8-15. Typical Circuit

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表 8-4 lists the recommended $R_{NR/SS}$ resistor values to achieve several common rails using a standard 1%-tolerance resistor.

表 8-4. Recommended $R_{NR/SS}$ Values

TARGETED OUTPUT VOLTAGE (V)	$R_{NR/SS}$ (kΩ)	CALCULATED OUTPUT VOLTAGE (V)
0.4	2.67	0.4005
0.5	3.32	0.498
0.6	4.02	0.603
0.7	4.64	0.696
0.8	5.36	0.804
0.9	6.04	0.906
1.0	6.65	0.9975
1.2	8.06	1.209
1.5	10.0	1.5
2.5	16.5	2.475
3.0	20.0	3.0
3.3	22.1	3.315
3.6	24.3	3.645
4.7	31.6	4.74
5.0	33.2	4.98

注

To avoid engaging the current limit during start-up with a large C_{OUT} capacitor, make sure that:

- A minimum NR/SS capacitor of 1 µF is used
- When the output capacitor is greater than 100 µF, maintain a C_{OUT} to $C_{NR/SS}$ ratio < 100

Because the set resistor is also placed on the NR/SS pin, consider using a thin-film resistor and provide enough resistor temperature drift to provide the targeted accuracy.

8.1.11 Paralleling for Higher Output Current and Lower Noise

Achieving higher output current and lower noise is achievable by paralleling two or more LDOs. Implementation must be carefully planned out to optimize performance and minimize output current imbalance.

Because the TPS7A96 output voltage is set by a resistor driven by a current source, the NR/SS resistor and capacitor must be adjusted as per the following:

$$R_{NR/SS_Parallel} = \frac{V_{OUT_TARGET}}{n \times I_{NR/SS}} \quad (8)$$

$$C_{NR/SS_Parallel} = n \times C_{NR/SS_Single} \quad (9)$$

where:

- n is the number of LDOs in parallel
- $I_{NR/SS}$ is the NR/SS current as provided in the data sheet *Electrical Characteristics* table
- $C_{NR/SS}$_single is the NR/SS capacitor for a single LDO

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When connecting the input and NR/SS pin together, and with the LDO being a buffer, the current imbalance is only affected by the error offset voltage of the error amplifier. As such, the current imbalance can be expressed as:

$$\varepsilon_I = \frac{V_{OS} \times 2 \times R_{BALLAST}}{R_{BALLAST}^2 - \Delta R_{BALLAST}^2} \quad (10)$$

where:

- ε_I is the current imbalance
- V_{OS} is the LDO error offset voltage
- $R_{BALLAST}$ is the ballast resistor
- $\Delta R_{BALLAST}$ is the deviation of the ballast resistor value from the nominal value

With the typical offset voltage of 200 µV, considering no error from the design of the PCB ballast resistor ($\Delta R_{BALLAST}$ = 0) and a 100-mA maximum current imbalance, the ballast resistor must be 4 mΩ or greater; see 図 8-16.

Using the configuration described, the LDO output noise is reduced by:

$$e_{O_parallel} = \frac{1}{\sqrt{n}} \times e_{O_single} \quad (11)$$

where:

- n is the numbers of LDOs in parallel
- e_{O_single} is the output noise density from a single LDO
- $e_{O_parallel}$ is the output noise density for the resulting parallel LDO

In 図 8-16, the noise is reduced by 1 / $\sqrt{2}$.

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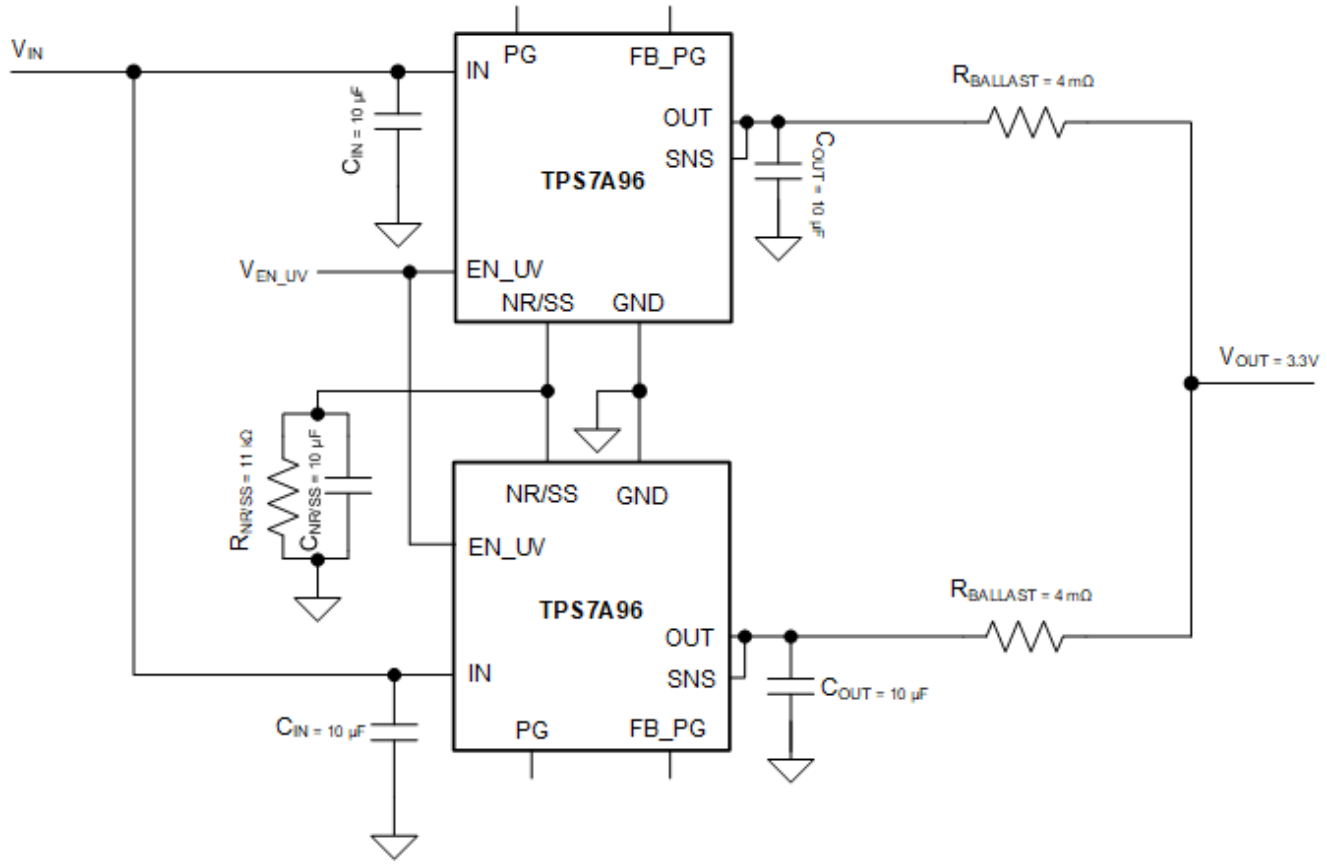


図 8-16. Paralleling Multiple TPS7A96 Devices

8.1.12 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-rated, or better dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (V_{IN} = 5.5 V to V_{OUT} = 5.0 V), the derating can be greater than 50%, which must be taken into consideration.

The device requires input, output, and noise-reduction capacitors for proper operation of the LDO. Use the nominal or larger than the nominal input and output capacitors, as specified in the *Recommended Operating Conditions* table. Place input and output capacitors as close as possible to the corresponding pin and make the capacitor GND connections as close as possible to the device GND pin to minimize PCB loop inductance, thus reducing transient voltage spikes during a load step.

Multiple parallel capacitors can be used to lower the impedance present on the line, which counteracts input trace inductance, improves transient response, and reduces input ripple and noise. Using an output capacitor larger than the typical value can also improve transient response.

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8.1.13 Load Transient Response

注

For best transient response, use the nominal value or larger capacitor from OUT to ground as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.

For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.

The load-step transient response is the LDO output voltage response to load current changes. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in 図 8-17 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

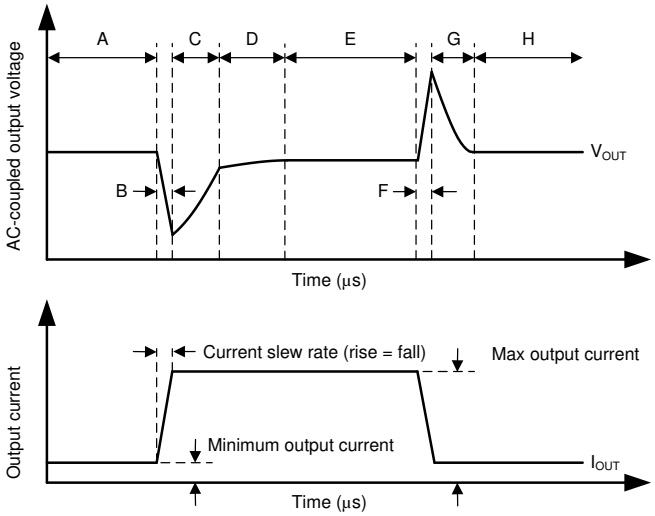


図 8-17. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

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8.1.14 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 式 12 calculates P_D:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (12)$$

注

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation by the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to 式 13. This equation is rearranged for output current in 式 14.

$$T_J = T_A = (R_{\theta JA} \times P_D) \quad (13)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (14)$$

This thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the DSC package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

8.1.15 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 15 and are given in the *Thermal Information* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (15)$$

where:

- P_D is the power dissipated as explained in the *Power Dissipation (P_D)* section
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.16 TPS7A96EVM-106 Thermal Analysis

The TPS7A96EVM-106 evaluation board was used to develop the thermal model. The DSC package is a 3-mm × 3-mm, 10-pin VQFN with 25-µm plating on each via. The EVM is a 2.85-inch × 3.35-inch (72.39 mm × 85.09 mm) PCB comprised of four layers. 表 8-5 lists the layer stackup for the EVM. 図 8-18 to 図 8-22 illustrate the various layer details for the EVM.

表 8-5. TPS7A96EVM-106 PCB Stackup

LAYER	NAME	MATERIAL	THICKNESS (mil)
1	Top overlay	—	—
2	Top solder	Solder resist	0.4
3	Top layer	Copper	2.8
4	Dielectric 1	FR-4 high Tg	10
5	Mid layer 1	Copper	2.8
6	Dielectric 2	FR-4 high Tg	30
7	Mid layer 2	Copper	2.8
8	Dielectric 3	FR-4 high Tg	10
9	Bottom layer	Copper	2.8
10	Bottom solder	Solder resist	0.4

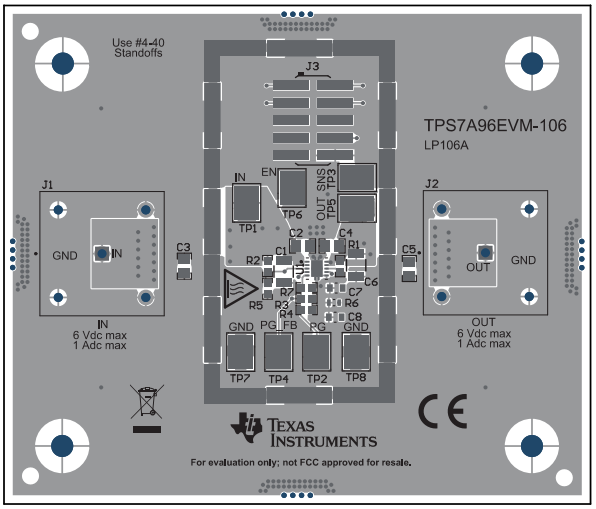


図 8-18. Top Composite View

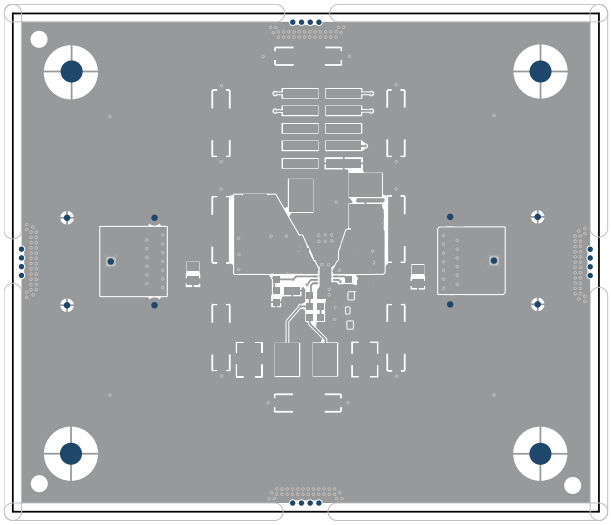


図 8-19. Top Layer Routing

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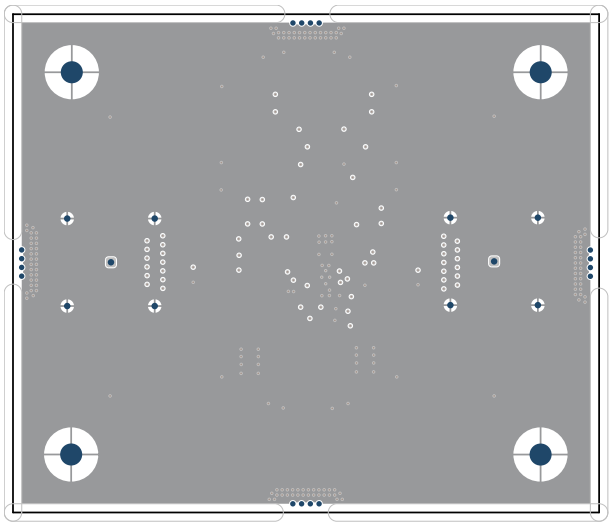


図 8-20. Mid Layer 1 Routing

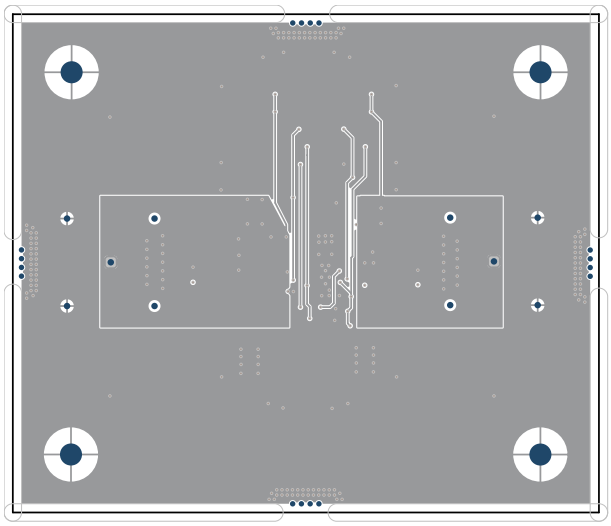


図 8-21. Mid Layer 2 Routing

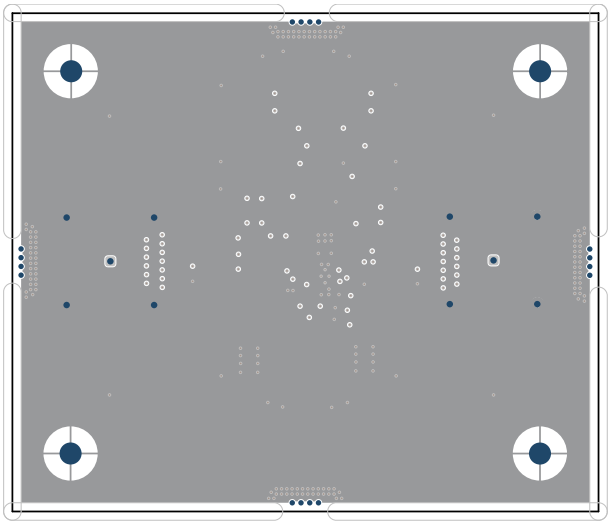


図 8-22. Bottom Layer Routing

図 8-23 to 図 8-25 show the thermal gradient on the PCB and device that results when a 1-W power dissipation is used through the pass transistor with a 25°C ambient temperature. 表 8-6 shows thermal simulation data for the TPS7A96EVM-106.

表 8-6. TPS7A96EVM-106 Thermal Simulation Data

DUT	$R_{\theta JA}$ (°C/W)	Ψ_{JB} (°C/W)	Ψ_{JT} (°C/W)
TPS7A96EVM-106	25.6	11.5	0.3

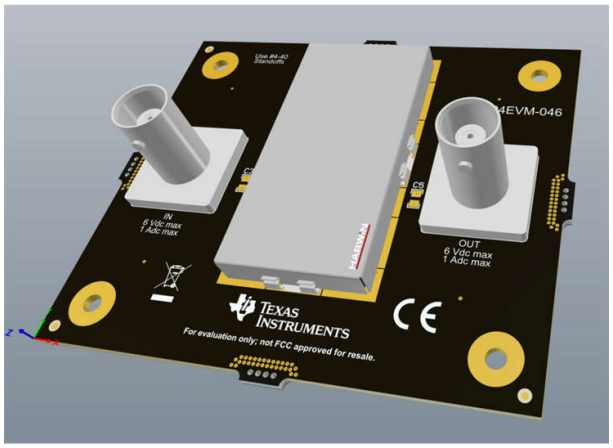
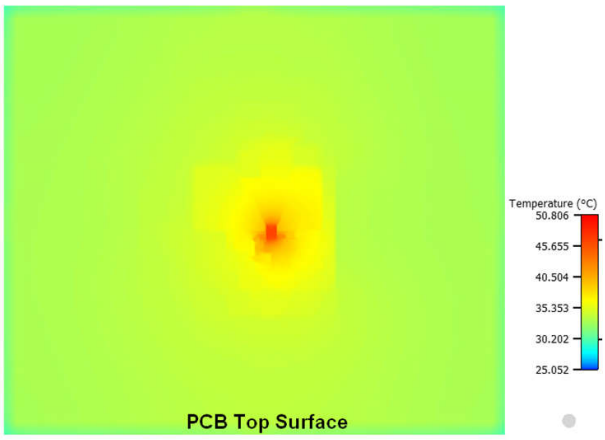


図 8-23. TPS7A96EVM-106 3D View



C

図 8-24. TPS7A96EVM-106 PCB Thermal Gradient

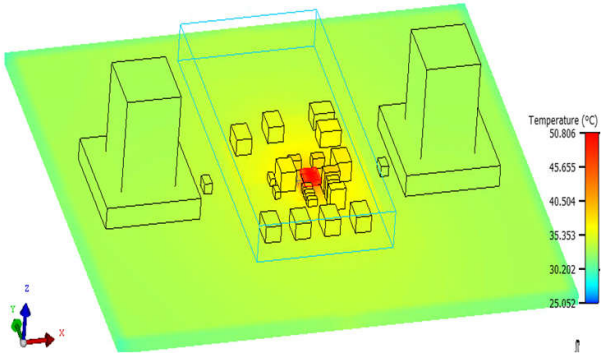


図 8-25. TPS7A96EVM-106 Device Thermal Gradient

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8.2 Typical Application

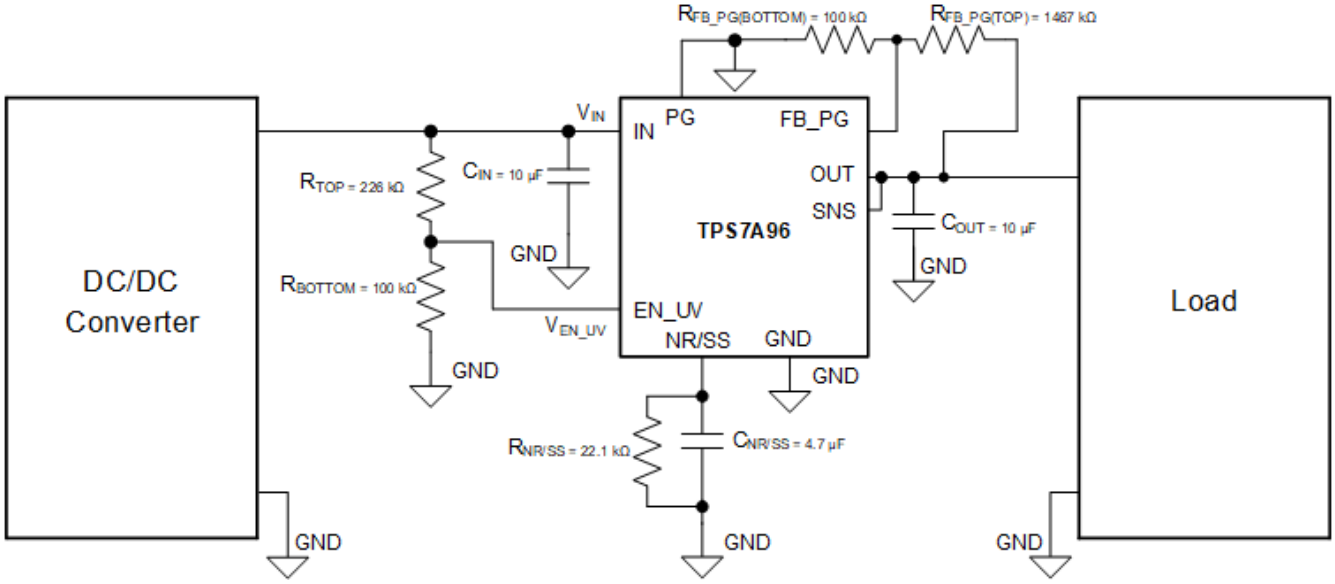


図 8-26. Typical Application Circuit

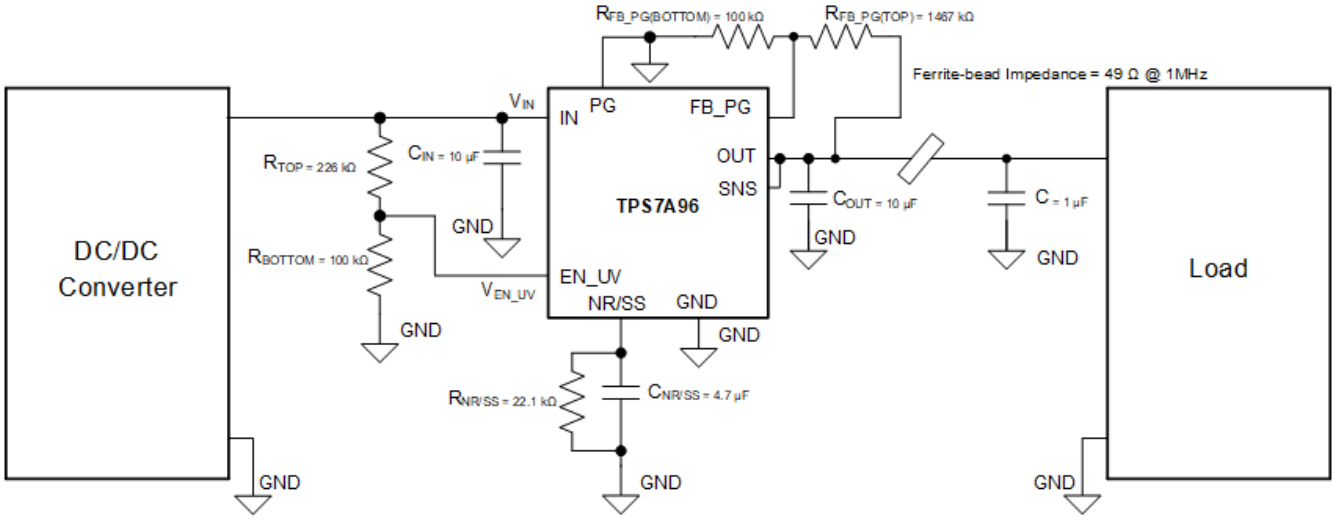


図 8-27. Typical Application Circuit With Added Pi-Filter

8.2.1 Design Requirements

表 8-7 lists the required application parameters for this design example.

表 8-7. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	V_{IN} ≥ 5 V, ±3%, provided by the dc/dc converter switching at 1 MHz
Output voltage	3.3 V, ±1%
Output current	1.5 A (maximum), 800 mA (minimum)
Current limit	2 A
PG threshold	95%
Targeted spectral noise	Targeted noise compliance mask Zone 1 (10 Hz to 100 Hz): Spectral noise ≤ 100 nV/√Hz Zone 2 (100 Hz to 1 kHz): Spectral noise ≤ 10 nV/√Hz Zone 3 (> 1 kHz): Spectral noise ≤ 3 nV/√Hz
PSRR at 1 MHz	> 50 dB at max load current
Start-up environment	Device to be enabled when V_{IN} ≥ 80% × V_{IN_Target} Device to be disabled when V_{IN} < 80% × V_{IN_Target} Start-up time < 25 ms

8.2.2 Detailed Design Procedure

In this design example, the device is powered by a dc/dc convertor switching at 1 MHz. The load requires a 3.3-V clean rail with the spectral noise mask versus frequency shown in 図 8-28 and a maximum load of 500 mA. The typical 10-µF input and output capacitors and 4.7-µF NR/SS capacitors are used to achieve a good balance between fast start-up time and excellent noise and PSRR performance.

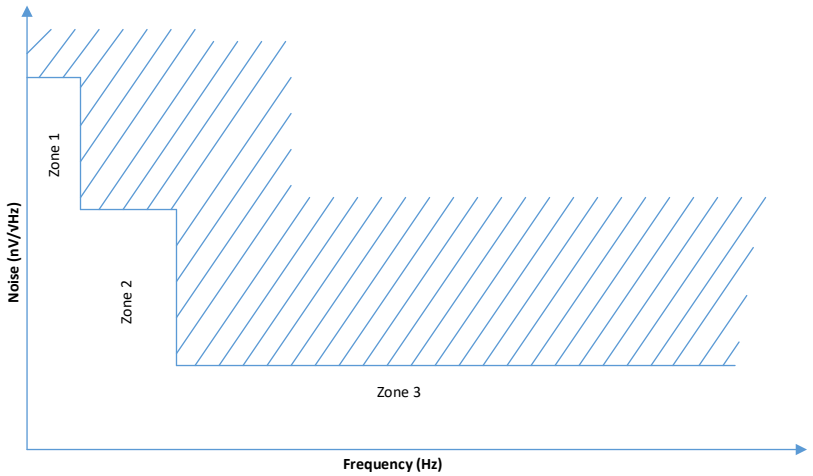


図 8-28. Noise Compliance Mask

The output voltage is set using a 22.1-kΩ, thin-film resistor value calculated as described in the *Adjustable Operation* section. To set the current limit to a value close to the 750 mA required by the application, and to set the PG threshold to 95%, use 表 8-2 to set the R_{FB_PG} top and bottom resistors values at 1.47 MΩ and 100 kΩ, respectively.

Setting R_B to 100 kΩ and using a 4-V V_{ON} and 式 1 provides the R_T value of 226 kΩ. V_{OFF} is calculated with 式 2 to be 3.5 V.

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図 8-29 shows that the device meets all design noise requirements except for the noise peaking at 900 kHz. However, this noise peaking can be easily attenuated to the required noise level by means of a pi-filter positioned after the LDO. 図 8-30 shows that this design is very close to the PSRR level at 1 MHz and can require more margin. Fortunately, both requirements are easily achieved by inserting a pi-filter consisting of a ferrite bead and a small capacitor beyond the LDO and before the load; see 図 8-27.

The ferrite bead was selected to have a very small dc resistance of less than 50 mΩ, 1 A of current rating, and a relatively small footprint. The added pi-filter components have almost no impact on the LDO accuracy performance and no significant increase in the design total cost.

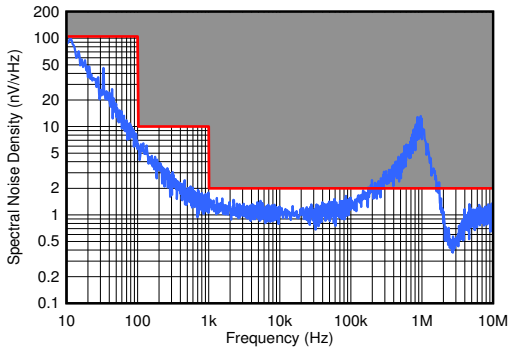


図 8-29. Output Noise vs Frequency

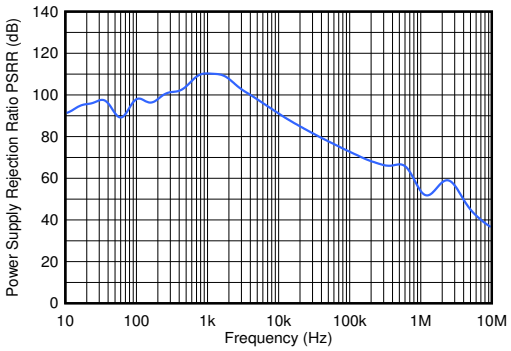


図 8-30. PSRR vs Frequency

8.2.3 Application Curves

図 8-31 and 図 8-32 show the design noise and PSRR performance after inserting the pi-filter.

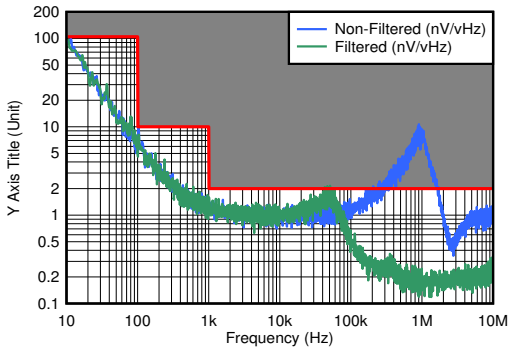


図 8-31. Noise vs Frequency

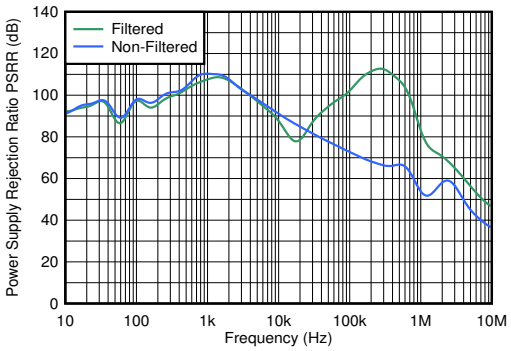


図 8-32. PSRR vs Frequency

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging from 1.7 V to 5.7 V. Make sure that the input voltage range provides adequate operational headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, use additional input capacitors with low ESR and increase the operating headroom to achieve the desired output noise, PSRR, and load transient performance.

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8.4 Layout

8.4.1 Layout Guidelines

For good thermal performance, connect the thermal pad to a large-area GND plane.

Kelvin connects the SNS pin through a low-impedance connection to the output capacitor and load for optimal transient performance. Do not float this pin.

Connect the GND pin to the device thermal pad and connect both this pin and the thermal pad to the ground on the board through a low-impedance connection.

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias or long traces to the input and output capacitors. The grounding and layout scheme described in 図 8-33 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the printed circuit board (PCB) or placed on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

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8.4.2 Layout Example

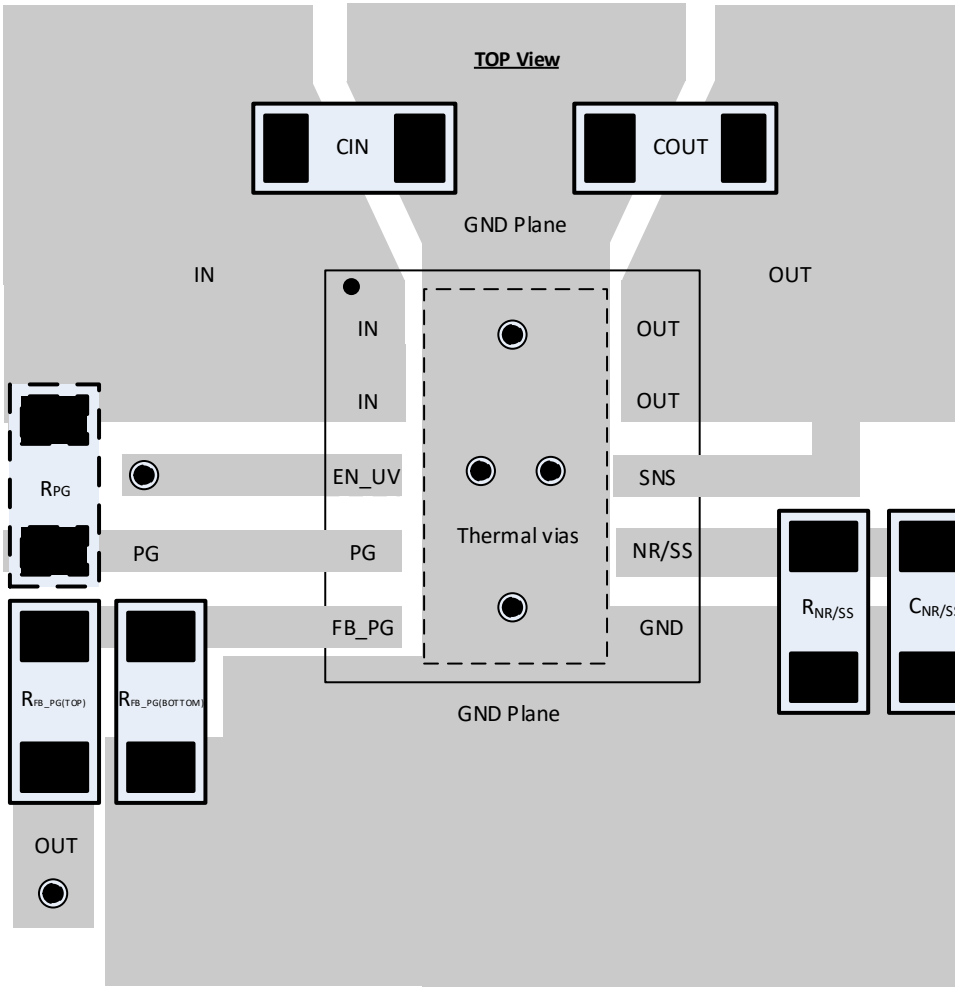


図 8-33. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A96. The summary information for this fixture is shown in 表 9-1.

表 9-1. Design Kits and Evaluation Modules

NAME	LITERATURE NUMBER
TPS7A96EVM-106 evaluation module	SBVU081

The EVM can be requested at the Texas Instruments web site through the TPS7A96 product folder.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A96 is available through the TPS7A96 product folder under simulation models.

9.1.2 Device Nomenclature

表 9-2. Ordering Information(1)

PRODUCT	DESCRIPTION
TPS7A9601**yyyz**	**yyy** is the package designator. **z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS3702 High-Accuracy, Overvoltage and Undervoltage Monitor* data sheet
- Texas Instruments, *TPS7A96EVM-106 Evaluation Module* user guide
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, Parallel LDO Architecture Design Using Ballast Resistors
- Texas Instruments, TPS7A57 evaluation module for 5-A low-noise high-accuracy low-dropout (LDO) voltage regulator
- Texas Instruments, Parallel low-dropout (LDO) calculator

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A9601DSCR	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A9601
TPS7A9601DSCR.A	Active	Production	WSON (DSC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7A9601

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

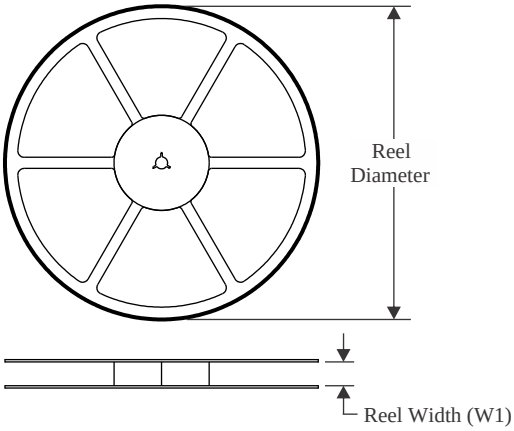
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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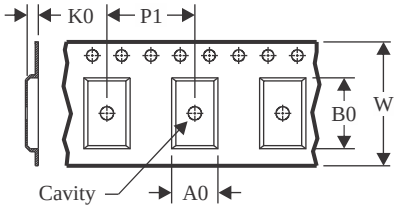
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

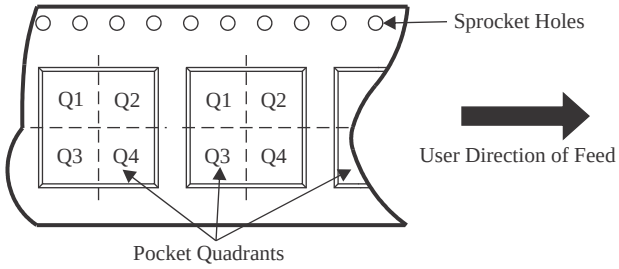


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

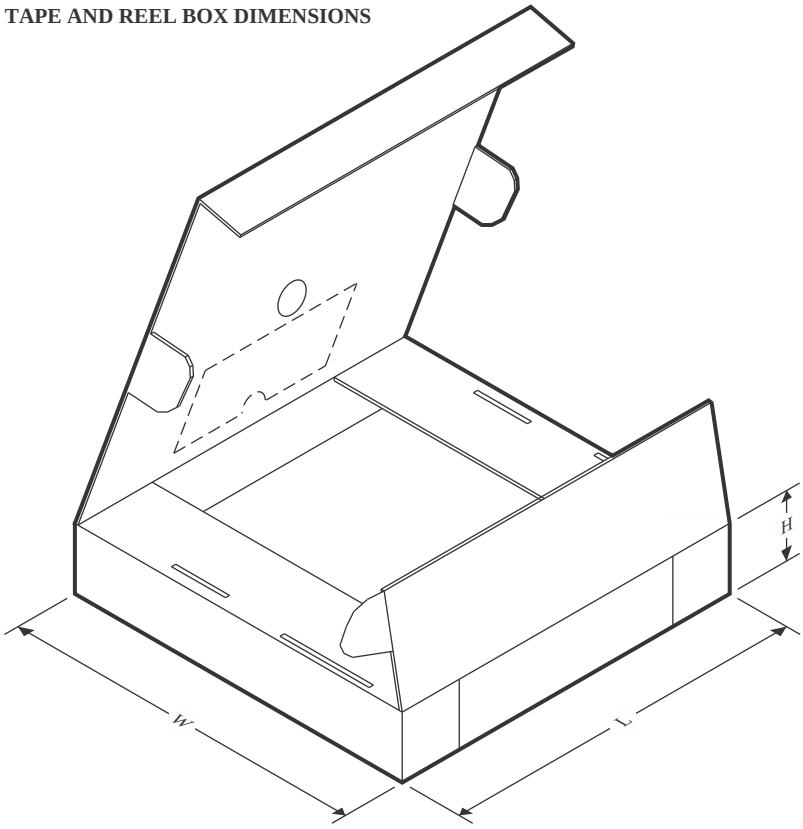
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A9601DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



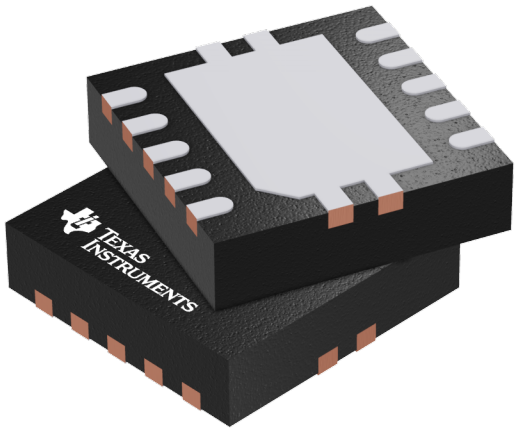
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A9601DSCR	WSON	DSC	10	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

DSC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



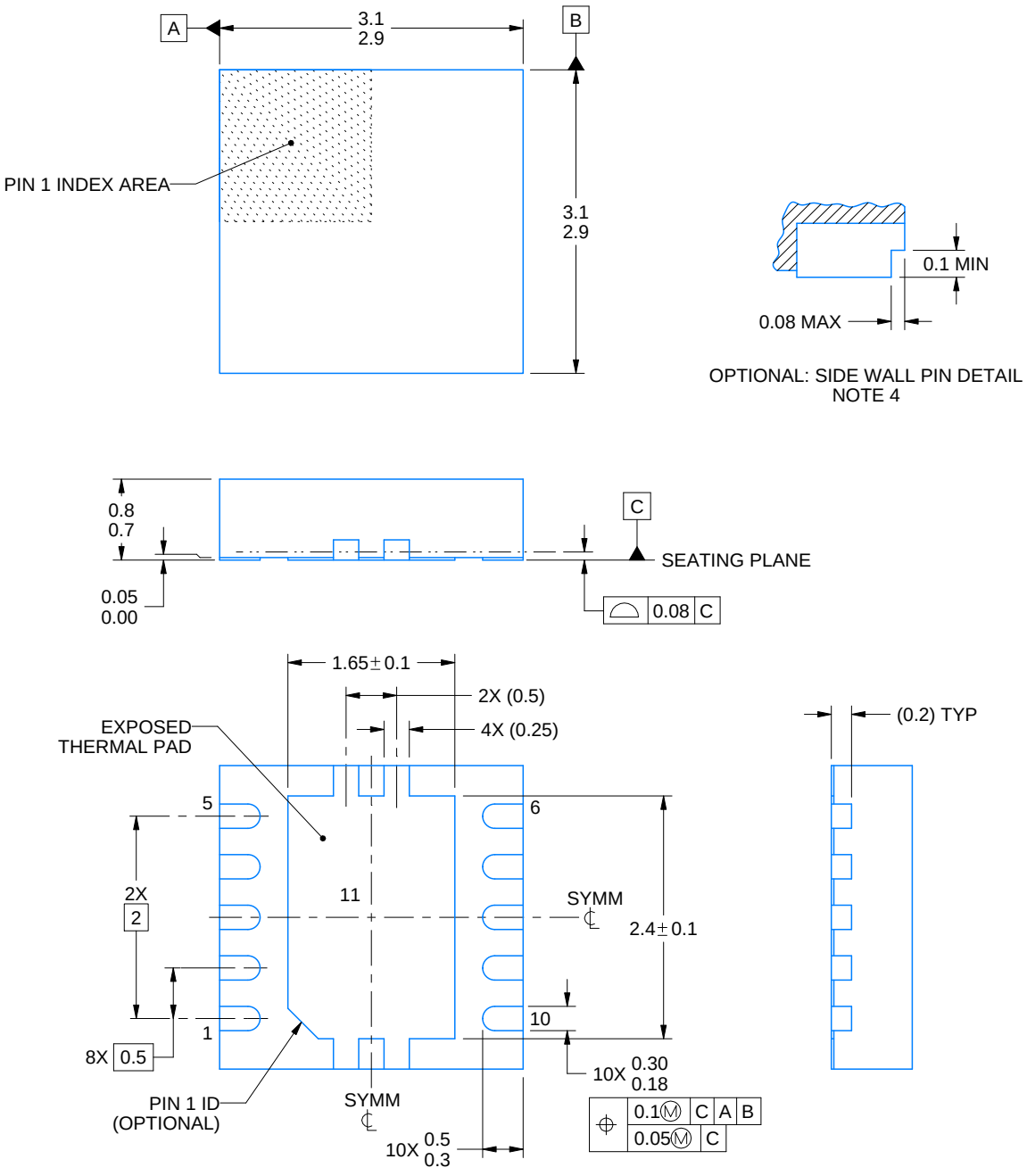
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSC0010J

PACKAGE OUTLINE

WSON - 0.8 mm max height

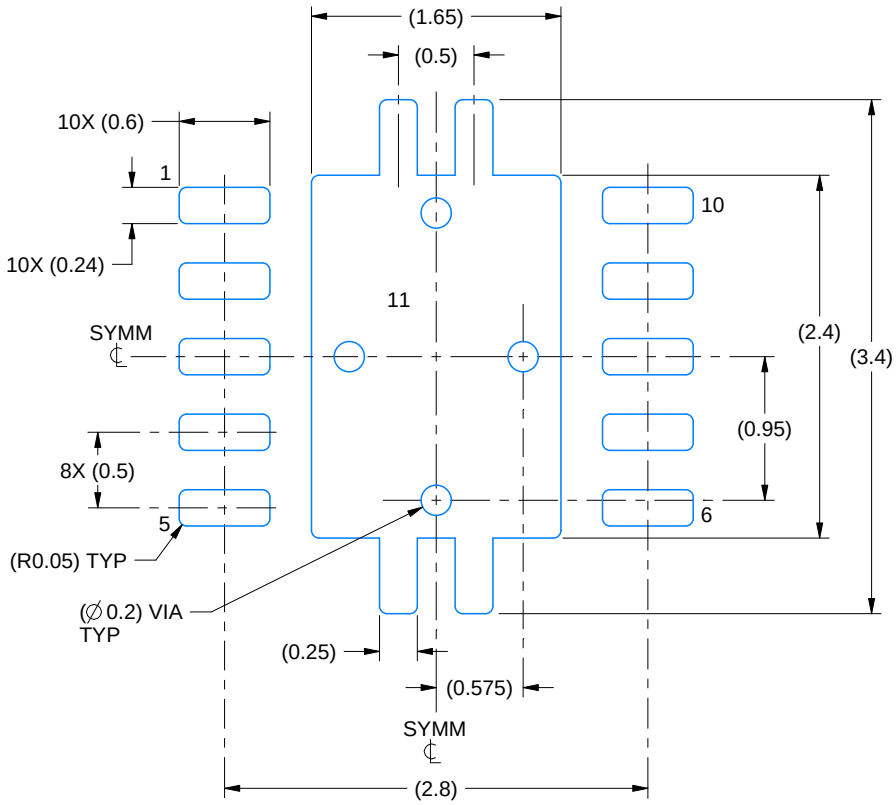
PLASTIC SMALL OUTLINE - NO LEAD



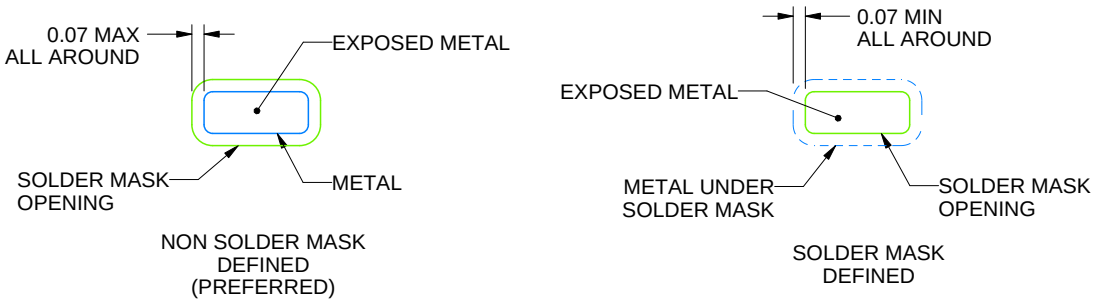
4221826/E 03/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

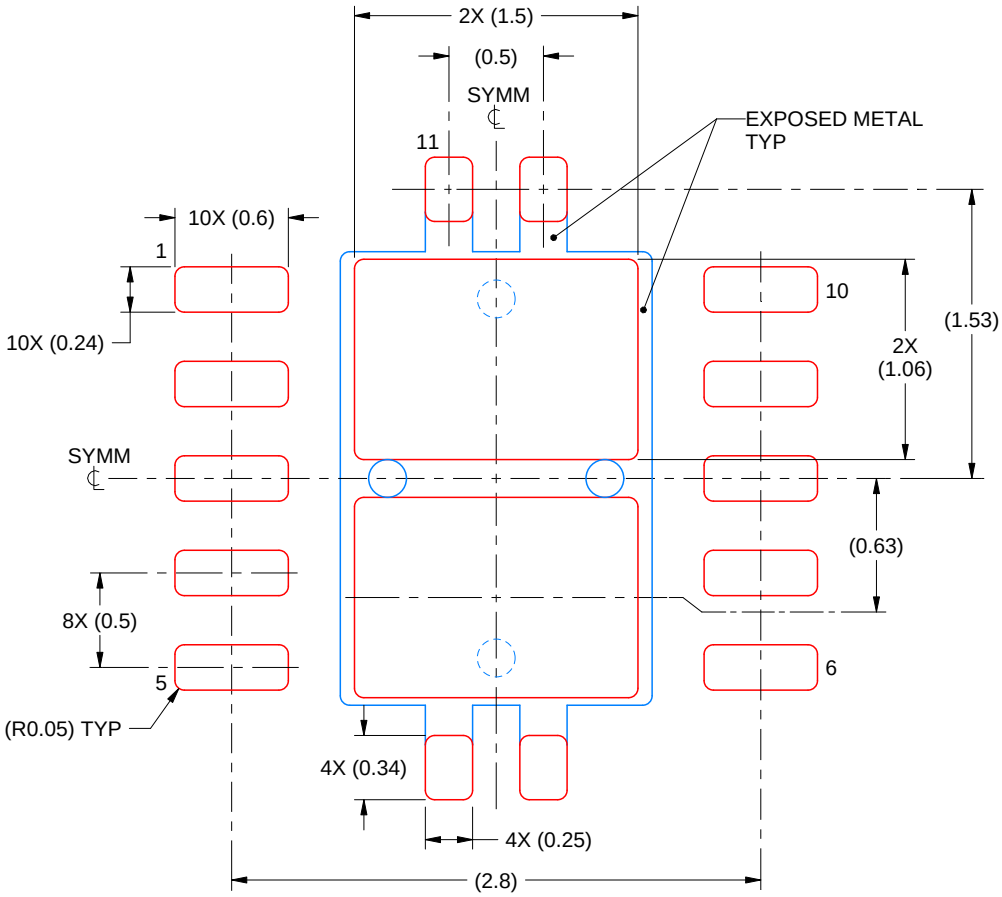


SOLDER MASK DETAILS

4221826/E 03/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221826/E 03/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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