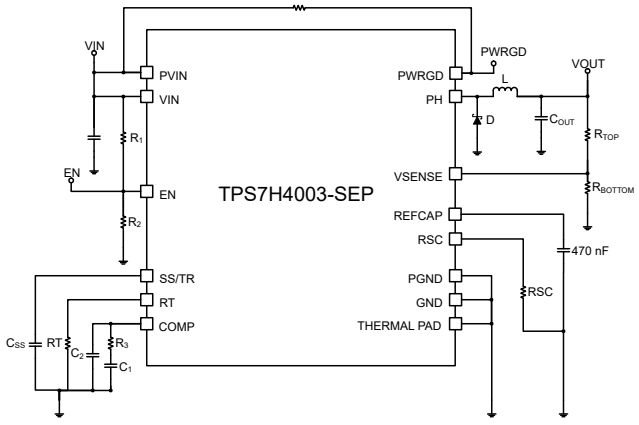
TEXAS INSTRUMENTS
TPS7H4003-SEP
JAJSNN5 – JANUARY 2022

TPS7H4003-SEP 放射線耐性、3V～7V 入力、18A、同期整流降圧コンバータ、宇宙用強化プラスチック

1 特長

- 耐放射線性能:
  - SEL、SEB、SEGR 耐性:
    LET = 43MeV-cm^2/mg (最大値)
  - SET および SEFI 特性:
    LET = 43MeV-cm^2/mg (最大値)
  - すべてのウェハー・ロットについて
    最大 50krad(Si) の吸収線量 (TID) を保証
- ピーク効率:94% (V_O = 1V、100kHz 時)
- 17mΩ および 9mΩ の MOSFET を内蔵
- 電源レール:3V～7V (VIN)
- 柔軟なスイッチング周波数オプション:
  - 100kHz～1MHz の可変内部発振器
  - 外部同期機能:100 kHz～1 MHz
  - SYNC ピンは、最大
    4 個のデバイスを並列に配置し、90° の位相差で
    500kHz のクロックとして構成可能
- 温度、放射線、ラインおよび負荷レギュレーションの全範囲で 0.6V±1.7% の基準電圧
- プリバイアスされた出力への単調スタートアップ
- 調整可能なスロープ補償とソフトスタート
- 調整可能な入力イネーブルとパワーグッド出力による電源シーケンス
- 44 ピン PowerPAD™ HTSSOP パッケージ
- 宇宙用強化プラスチック:
  - 管理されたベースライン
  - Au ボンド・ワイヤと NiPdAu リード仕上げ
  - モールド・コンパウンドの改良による低いガス放出
  - 単一の製造、アセンブリ、テスト施設
  - 長い製品ライフ・サイクル
  - 長期にわたる製品変更通知
  - 製品のトレーサビリティ



機能ダイアグラム

2 アプリケーション

- 人工衛星のポイント・オブ・ロード電源
- 通信ペイロード
- 光学画像処理ペイロード

3 概要

TPS7H4003-SEP は、耐放射線性、7V 、18A 同期整流降圧コンバータで、放熱特性の優れた 34 ピン・セラミック・フラットパック・パッケージに封止され、低抵抗のハイサイド MOSFET とローサイド MOSFET を内蔵しています。電流モード制御による高い効率と部品数の削減が可能です。

出力電圧のスタートアップ・ランプは、SS/TR ピンで制御されます。これにより、スタンドアロン電源としても、トラッキング状況でも動作できます。イネーブルおよびパワー・グッド・ピンを適切に構成することにより、電源シーケンシングが可能です。TPS7H4003-SEP は、プライマリ・セカンダリ・モードに設定することができ、SYNC2 ピンを使って、外部クロックなしで 4 個のデバイスの並列構成が可能です。

ハイサイド FET にサイクル単位の電流制限を適用することにより、過負荷状態からデバイスを保護します。また、ローサイドのソース電流制限により電流暴走を防止します。さらに、ローサイドのシンク電流制限によりローサイド MOSFET をオフにすることで、過度な逆方向電流を防止します。ダイの温度が温度限界値を超えると、サーマル・シャットダウンによりデバイスがディセーブルになります。

デバイス情報

部品番号(1)	グレード	パッケージ
TPS7H4003MDDWSEP	50-krad(Si) RLAT	HTSSOP (44) 6.10mm × 14.00mm 質量 = 243.8mg(2)
TPS7H4003MDDWTSEP		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) 質量の精度は ±10% です。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2022	*	Initial Release

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5 Pin Configuration and Functions

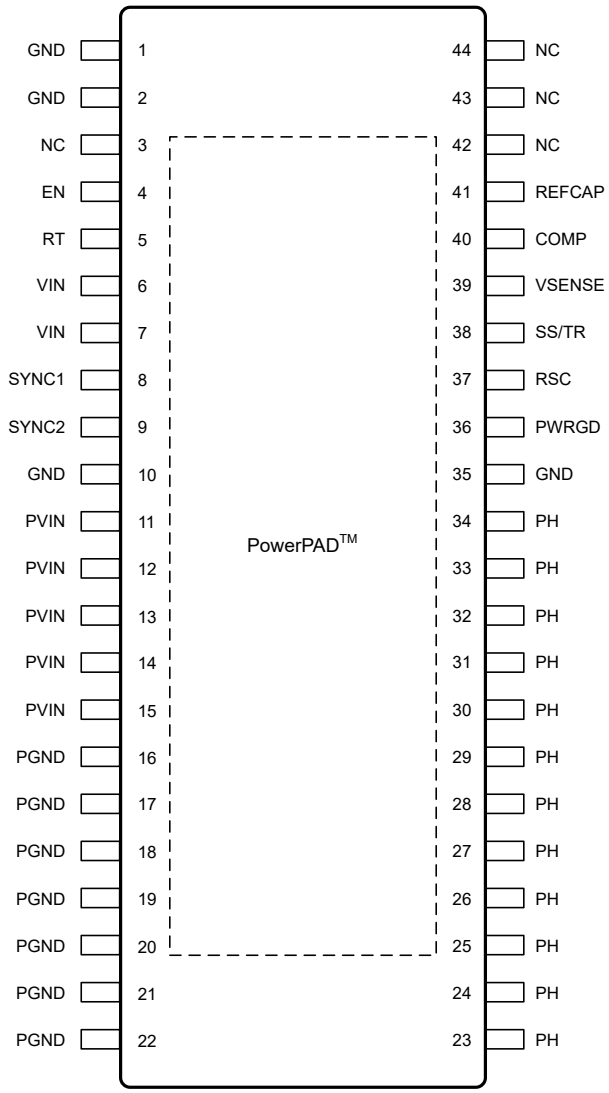


図 5-1. DDW Package 44-Pin HTSSOP (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 2, 10, 35	GND	—	Return for control circuitry.
3, 42–44	NC	I	No connect.
4	EN	I	EN pin is internally pulled up allowing for the pin to be floated to enable the device.
5	RT	I/O	A resistor connected between RT and GND sets the switching frequency of the converter. The switching frequency range is 100 kHz to 1 MHz. When an external clock is used, RT must be selected such that the set switching frequency coincides with the frequency of the applied clock. Leaving this pin floating sets the internal switching frequency to 500 kHz and SYNC1 and SYNC2 become output clocks at 500 kHz, with SYNC1 aligned with the converter switching and SYNC2 90° out of phase.
6, 7	VIN	I	Input power for the control circuitry of the switching regulator.

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
8	SYNC1	I/O	SYNC1 is an input when an external clock is provided. The frequency of the external clock should match the switching frequency that is set by the resistor between RT and GND. With an external clock applied, the converter switching action is 180° out of phase with the external clock. When RT is floating, SYNC1 serves as an output of a 500-kHz clock signal that is in phase with the converter switching action. SYNC1 can be used in combination with SYNC2 in order to connect up to four devices in parallel.
9	SYNC2	I/O	SYNC2 is used for connecting multiple devices in parallel. For the primary device, with RT floating, SYNC2 outputs 500-kHz signal that is 90° out of phase with the SYNC1 output clock. For the secondary devices, in which RT is populated, SYNC2 is used to configure the phase of the input clock signal on SYNC1. When SYNC2 is connected to VIN, the internal clock of the secondary device is in phase with clock provided at SYNC1. When SYNC2 is connected to GND, the input clock signal at SYNC1 is internally inverted.
11–15	PVIN	I	Input power for the output stage of the switching regulator.
16–22	PGND	—	Return for low-side power MOSFET.
23–34	PH	O	Switch phase node.
36	PWRGD	O	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during soft-start.
37	RSC	I/O	A resistor to GND sets the desired slope compensation.
38	SS/TR	I/O	Soft-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
39	VSENSE	I	Inverting input of the gm error amplifier.
40	COMP	I/O	Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.
41	REFCAP	O	Required 470-nF external capacitor for internal reference.
	PowerPAD™	—	Used for heat sinking by soldering to GND copper on printed circuit board.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7.5	V
	PVIN	–0.3	7.5	
	EN	–0.3	7.5	
	RSC	–0.3	3.3	
	VSENSE	–0.3	3.3	
	COMP	–0.3	3.3	
	PWRGD	–0.3	7.5	
	SS/TR	–0.3	3.3	
	RT	–0.3	3.3	
	SYNC1	–0.3	7.5	
	SYNC2	–0.3	7.5	
Output voltage	REFCAP	–0.3	3.3	V
	PH	–1	7.5	
	PH 10-ns transient	–3	7.5	
Vdiff	(GND to exposed thermal pad)	–0.2	0.2	V
Source current	PH		Current limit	A
	RT		±100	µA
Sink current	PH		Current limit	A
	PVIN		Current limit	A
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
I_{OUT}	Maximum switching current			18	A
T_J	Junction operating temperature	–55		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS7H4003-SEP HTSSOP 44 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953)

6.5 Electrical Characteristics

T_J = –55°C to 125°C, V_{IN} = P_{VIN} = 3 V to 7 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)						
PVIN operating input voltage			3.0		7.0	V
PVIN internal UVLO threshold	PVIN rising		2.425	2.50	2.575	V
PVIN internal UVLO hysteresis	Load = 0 A		425	450	475	mV
VIN operating input voltage			3.0		7.0	V
VIN internal UVLO threshold	VIN rising		2.71	2.75	2.80	V
VIN internal UVLO hysteresis			134	150	178	mV
VIN shutdown supply current	V_{EN} = 0 V			2.32	2.85	mA
VIN operating – non switching supply current	V_{SENSE} = V_{BG}			4	6	mA
ENABLE AND UVLO (EN PIN)						
Enable threshold	Rising		1.110	1.14	1.172	V
	Falling		1.080	1.11	1.148	
Input current	V_{EN} = 1.1 V		4.8	6.1	7.6	µA
Hysteresis current	V_{EN} = 1.3 V		2.4	3.0	3.9	µA
VOLTAGE REFERENCE						
Internal voltage reference initial tolerance	0 A ≤ Iout ≤ 18 A, 25°C		0.598	0.605	0.613	V
Internal voltage reference	0 A ≤ Iout ≤ 18 A	–55°C	0.594	0.602	0.609	V
		–40°C	0.596	0.602	0.608	
		85°C	0.600	0.606	0.613	
		125°C	0.599	0.607	0.614	
REFCAP voltage	REFCAP = 470 nF		1.189	1.209	1.228	V
MOSFET						
High-side switch resistance[1]	PVIN = VIN = 3 V, lead length = 3 mm	–55°C		16	18	mΩ
		25°C		19	21	
		125°C		23	27	
	PVIN = VIN = 5 V, lead length = 3 mm	–55°C		14	16	
		25°C		17	19	
		125°C		20	23	
	PVIN = VIN = 7 V, lead length = 3 mm[3]	–55°C		13	15	
		25°C		15	18	
		125°C		19	22	

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6.5 Electrical Characteristics (continued)

T_J = –55°C to 125°C, V_{IN} = P_{VIN} = 3 V to 7 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Low-side switch resistance[1]	PVIN = VIN = 3 V, lead length = 3 mm	–55°C		7	11	mΩ
		25°C		9	12	
		125°C		13	17	
	PVIN = VIN = 5 V, lead length = 3 mm	–55°C		6	10	
		25°C		9	11	
		125°C		12	15	
	PVIN = VIN = 7 V, lead length = 3 mm[3]	–55°C		5	9	
		25°C		8	10	
		125°C		11	14	
ERROR AMPLIFIER						
Error amplifier input offset voltage	V_{SENSE} = 0.6 V		–2		2.55	mV
VSENSE pin input current	V_{SENSE} = 0.6 V		–15		15	nA
Error amplifier transconductance (g_m)	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V		1150	1800	2400	µS
Error amplifier DC gain[2]	V_{SENSE} = 0.6 V			10000		V/V
Error amplifier source	$V_{(COMP)}$ = 1 V, 100-mV input overdrive		100	140	190	µA
Error amplifier sink			100	140	190	µA
Error amplifier output resistance				7		MΩ
COMP to Iswitch gm[3]	COMP = 0.5 V	–55°C	28	38	49	S
		25°C	29	40	50	
		125°C	30	41	52	
OVERCURRENT PROTECTION						
High-side switch current limit threshold[3]	V_{IN} = 7 V			27	34	A
Low-side switch sourcing overcurrent threshold[3]	V_{IN} = 7 V			25	32	A
Low-side switch sinking overcurrent threshold[3]	V_{IN} = 7 V		3.5	6		A
SLOPE COMPENSATION						
Slope compensation[4]	f_{SW} = 100 kHz, RSC = 1.1 MΩ			–1.2		A/µs
	f_{SW} = 500 kHz, RSC = 196 kΩ			–6.0		
	f_{SW} = 1000 kHz, RSC = 80.6 kΩ			–16.0		
THERMAL SHUTDOWN						
Thermal shutdown				190		°C
Thermal shutdown hysteresis				18		°C
INTERNAL SWITCHING FREQUENCY						
Internally set frequency	RT = Open	VIN = 3 V	444	473	515	kHz
		VIN = 5 V	449	502	560	
Externally set frequency	RT = 1.07 MΩ (1%)	VIN = 3 V	80	98	125	kHz
		VIN = 5 V	80	100	125	
	RT = 165 kΩ (1%)	VIN = 3 V	455	495	535	
		VIN = 5 V	475	523	615	
	RT = 73.2 kΩ (1%)	VIN = 3 V	689	850	1011	
		VIN = 5 V	760	986	1212	

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6.5 Electrical Characteristics (continued)

T_J = –55°C to 125°C, V_{IN} = P_{VIN} = 3 V to 7 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL SYNCHRONIZATION					
SYNC1/SYNC2 out low-to-high rise time (10%/90%)	Cload = 25 pF		70	180	ns
SYNC1/SYNC2 out high-to-low fall time (90%/10%)	Cload = 25 pF		10	21	ns
SYNC2 to SYNC1 rising edge phase shift		77	85	94	°
SYNC1 falling edge delay(3)		165	180	185	°
SYNC1/SYNC2 out high level threshold	I_{OH} = 50 µA	VIN – 0.3			V
SYNC1/SYNC2 out low level threshold	I_{OL} = 50 µA			600	mV
SYNC1/SYNC2 in low level threshold	PVIN = VIN = 3 V			800	mV
	PVIN = VIN = 5 V			800	
	PVIN = VIN = 7 V(3)			800	
SYNC1/SYNC2 in high level threshold	PVIN = VIN = 3 V	2.25			V
	PVIN = VIN = 5 V	3.5			
	PVIN = VIN = 7 V(3)	4.9			
SYNC1 in frequency range	PVIN = VIN = 5 V	100		1000	kHz
SYNC1 in duty cycle range	Duty cycle of external clock	40		60	%
PH (PH PIN)					
Minimum on time	Measured at 10% to 90% of VIN, I_{PH} = 2 A, VIN = 3 V		190	235	ns
	Measured at 10% to 90% of VIN, I_{PH} = 2 A, VIN = 5 V		190	225	
SOFT START AND TRACKING (SS/TR PIN)					
SS charge current		1.5	2.5	3	µA
SS/TR to VSENSE matching(3)	$V_{(SS/TR)}$ = 0.3 V		30	90	mV
POWER GOOD (PWRGD PIN)					
VSENSE threshold	V_{SENSE} falling (fault)	90	91		%VREF
	V_{SENSE} rising (good)		94	97	
	V_{SENSE} rising (fault)		109	111	
	V_{SENSE} falling (good)	103	106		
Output high leakage	V_{SENSE} = VREF, V(PWRGD) = 5 V		30	181	nA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.1	V

(1) Measured at pins.
(2) Ensured by design only. Not tested in production.
(3) Bench verified. Not tested in production.
(4) Example values are shown in the table. Actual values are application specific and should be calculated as detailed in the *Slope Compensation* section.

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6.6 Typical Characteristics

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.

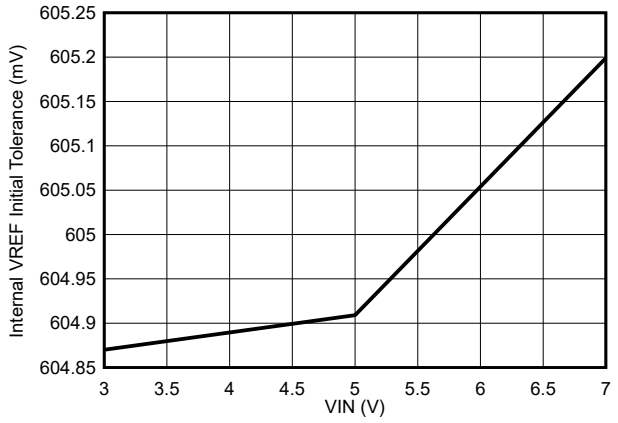


図 6-1. Internal VREF Initial Tolerance

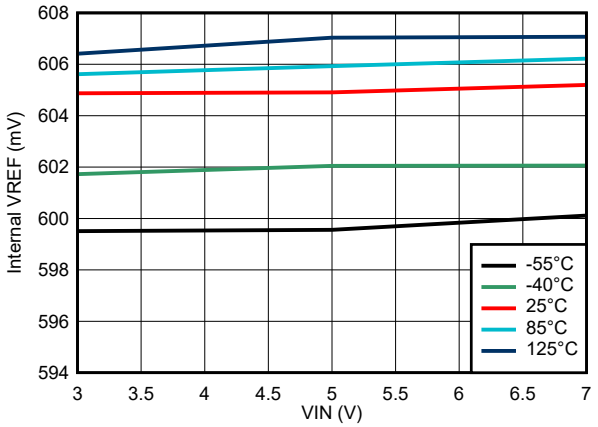


図 6-2. Internal VREF Variation

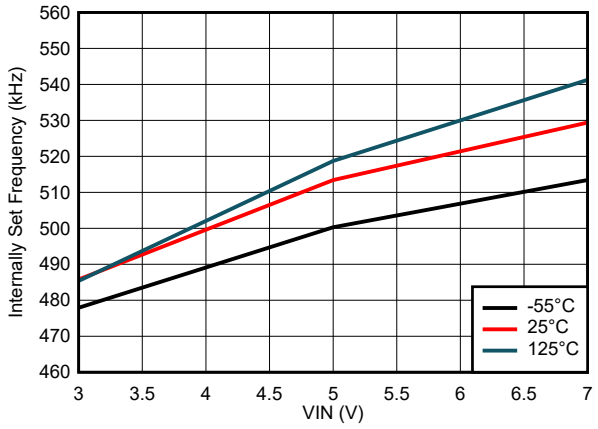


図 6-3. Internal Frequency Variation

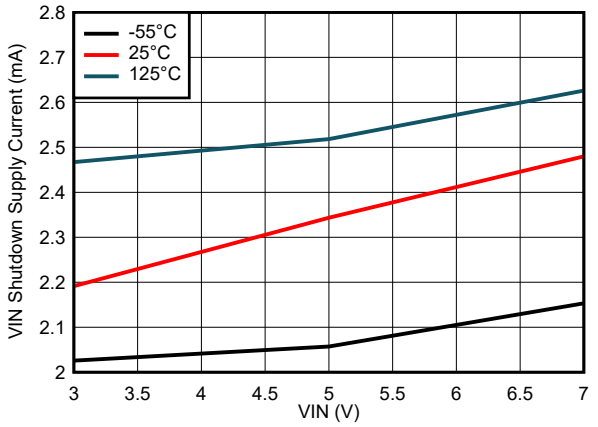


図 6-4. VIN Shutdown Supply Current Variation

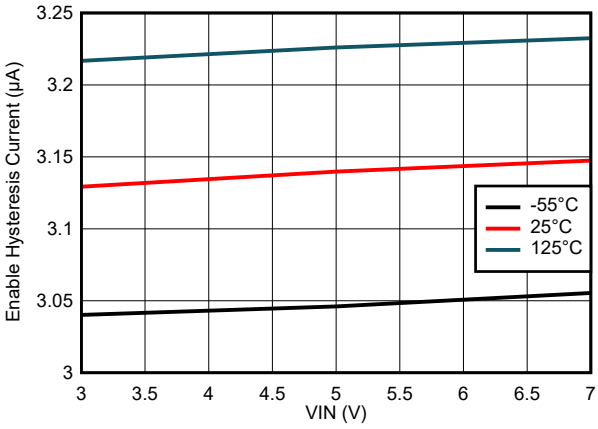


図 6-5. Enable Hysteresis Current Variation

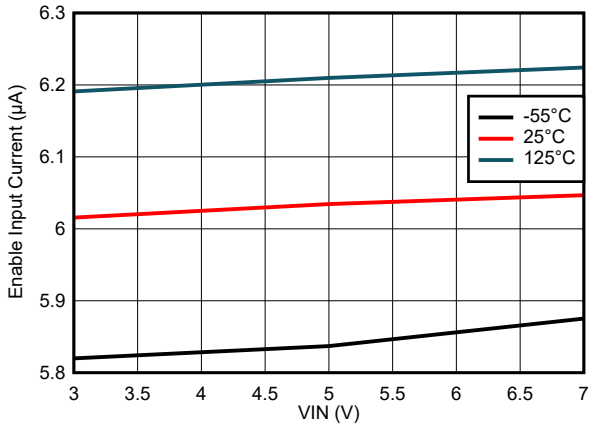


図 6-6. Enable Input Current Variation

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6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.

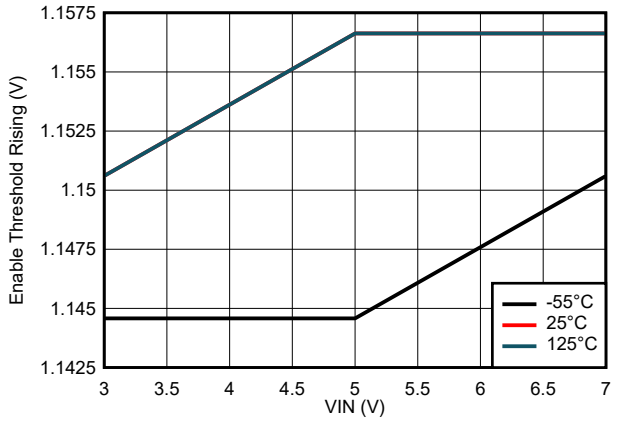


図 6-7. Enable Threshold Rising Variation

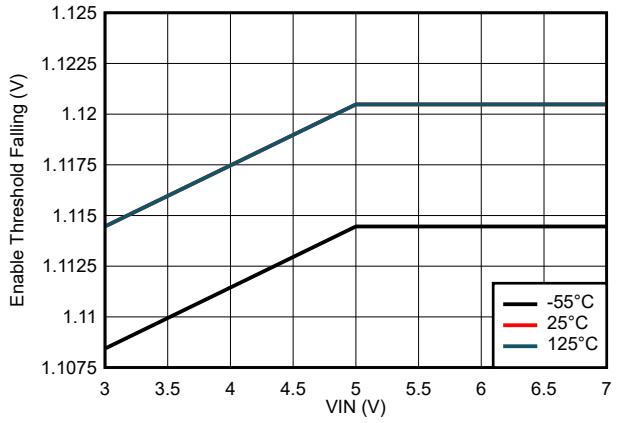


図 6-8. Enable Threshold Falling Variation

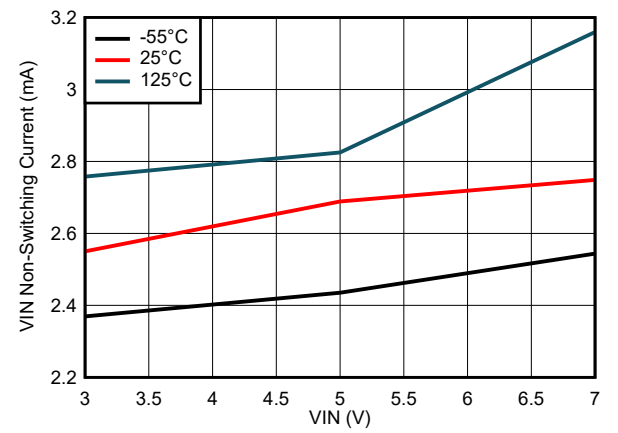


図 6-9. VIN Non-Switching Current Variation

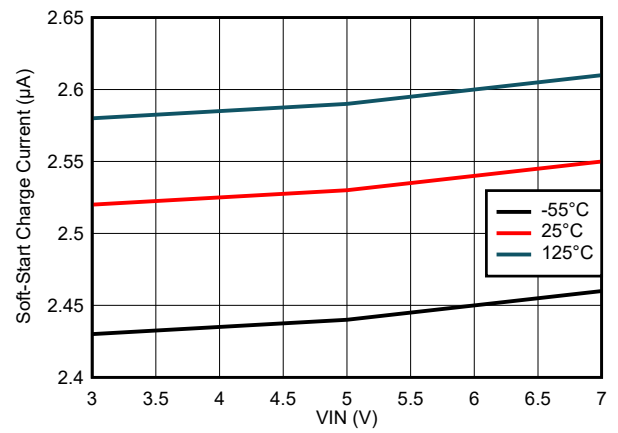


図 6-10. SS Charge Current Variation

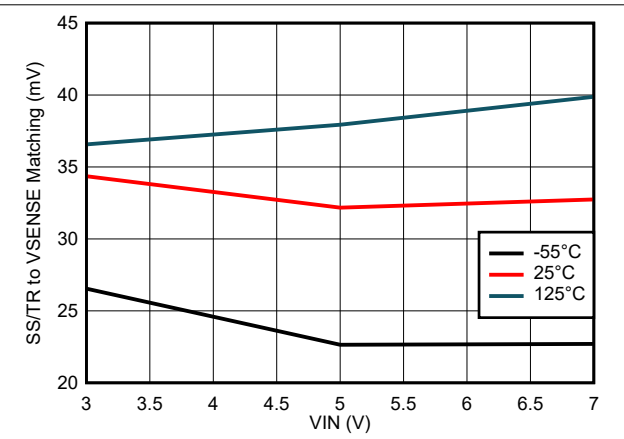


図 6-11. SS/TR to VSENSE Matching Variation

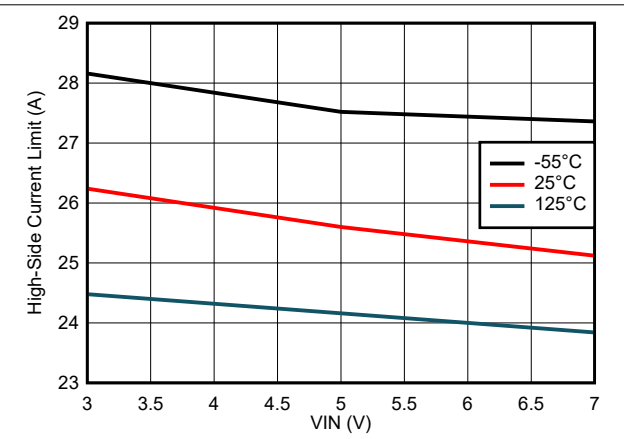


図 6-12. High-Side Current Limit Variation

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6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.

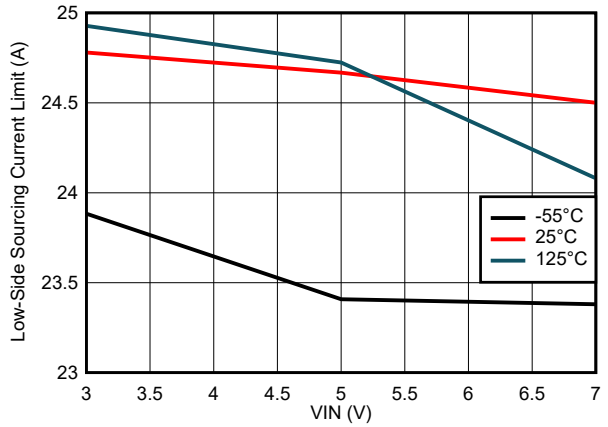


図 6-13. Low-Side Sourcing Current Limit Variation

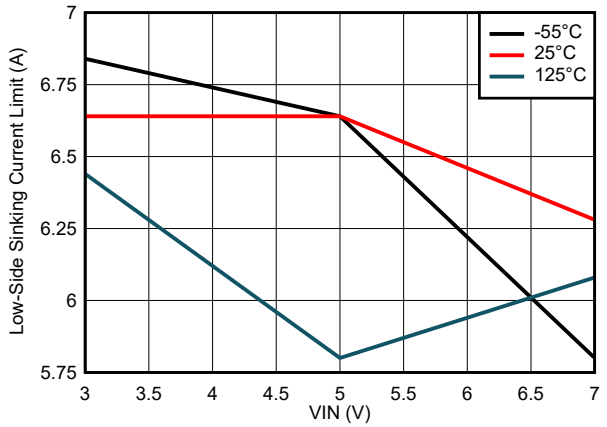


図 6-14. Low-Side Sinking Current Limit Variation

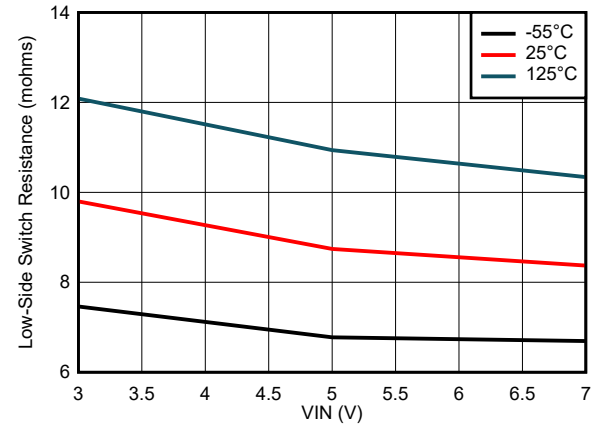


図 6-15. Low-Side Switch Resistance Variation

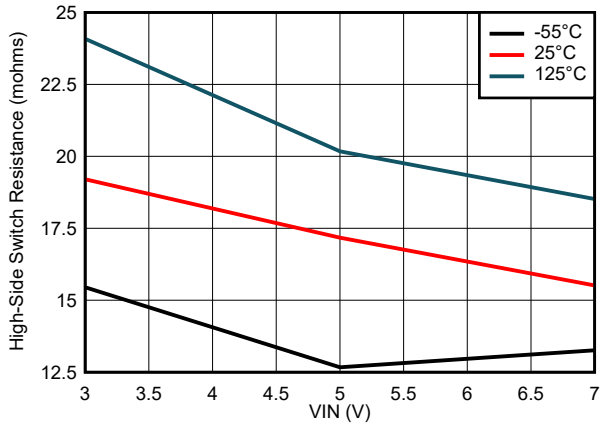
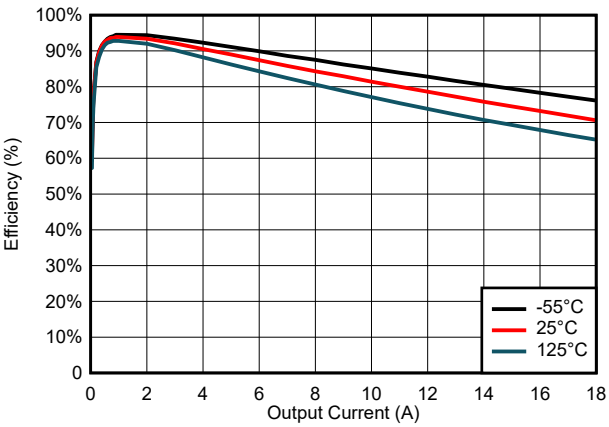
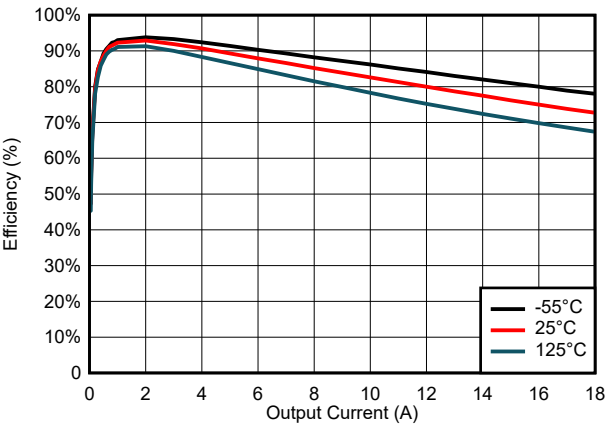


図 6-16. High-Side Switch Resistance Variation



VOUT = 1 V, f_{sw} = 100 kHz

図 6-17. Efficiency for VIN = 3.3 V



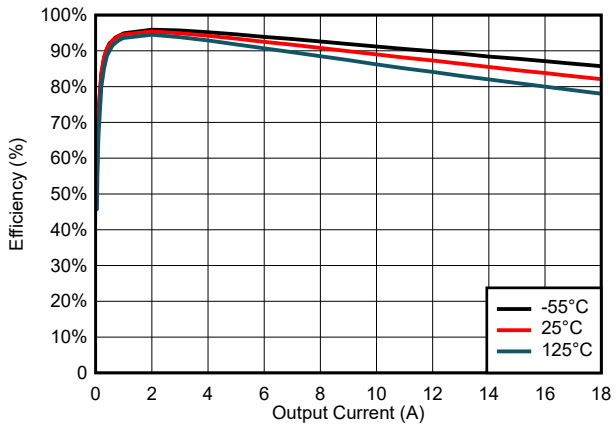
VOUT = 1 V, f_{sw} = 100 kHz

図 6-18. Efficiency for VIN = 5 V

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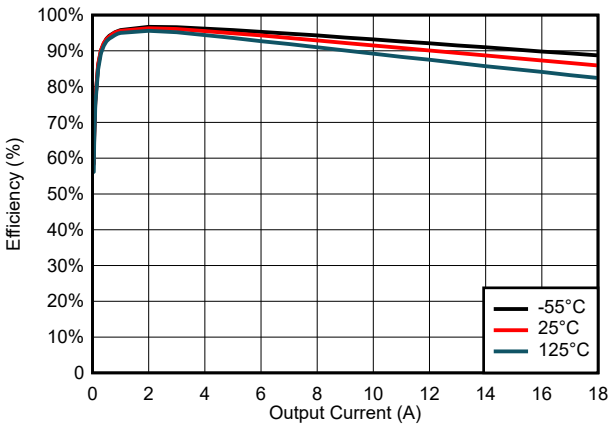
6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.



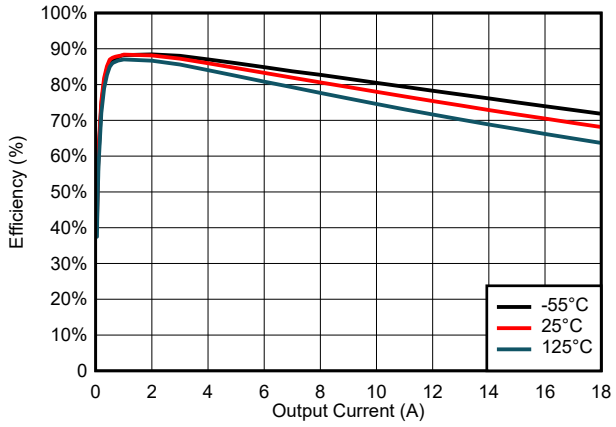
VOUT = 1.8 V, f_{sw} = 100 kHz

図 6-19. Efficiency for VIN = 5 V



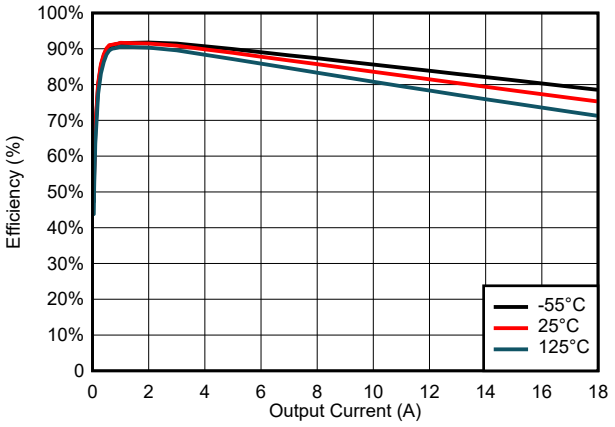
VOUT = 2.5 V, f_{sw} = 100 kHz

図 6-20. Efficiency for VIN = 5 V



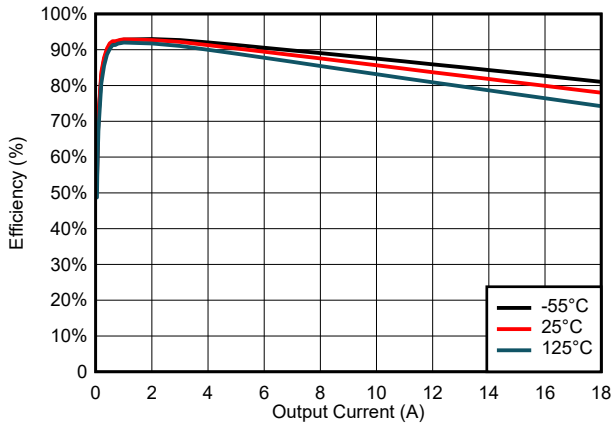
VOUT = 1 V, f_{sw} = 500 kHz

図 6-21. Efficiency for VIN = 3 V



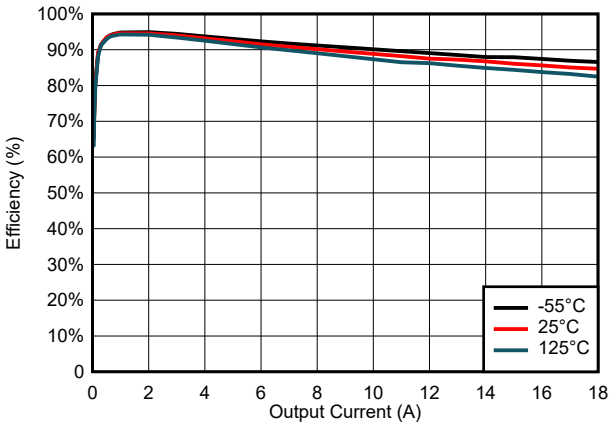
VOUT = 1.5 V, f_{sw} = 500 kHz

図 6-22. Efficiency for VIN = 3 V



VOUT = 1.8 V, f_{sw} = 500 kHz

図 6-23. Efficiency for VIN = 3 V



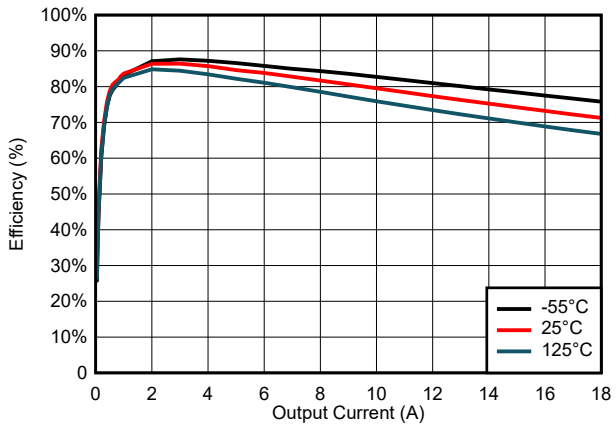
VOUT = 2.5 V, f_{sw} = 500 kHz

図 6-24. Efficiency for VIN = 3 V

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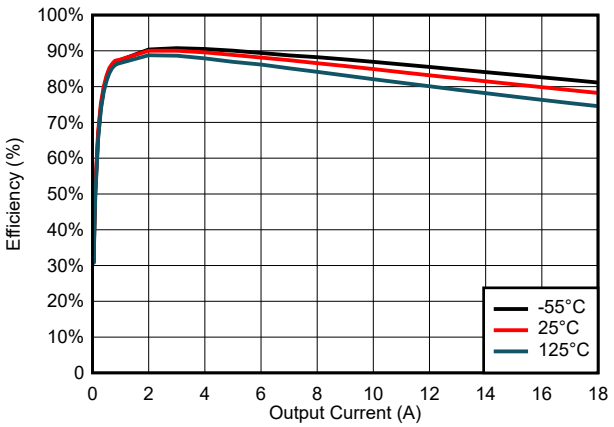
6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.



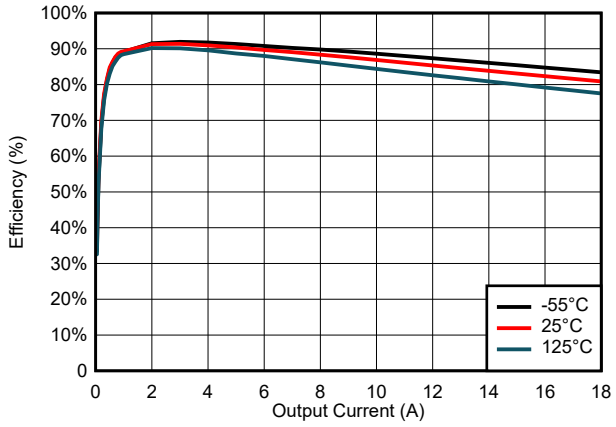
VOUT = 1 V, f_{sw} = 500 kHz

図 6-25. Efficiency for VIN = 5 V



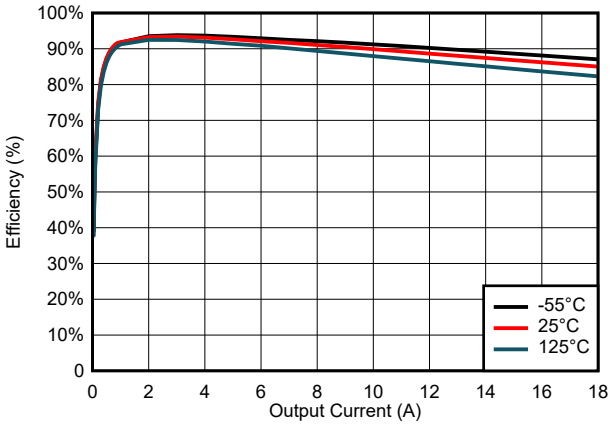
VOUT = 1.5 V, f_{sw} = 500 kHz

図 6-26. Efficiency for VIN = 5 V



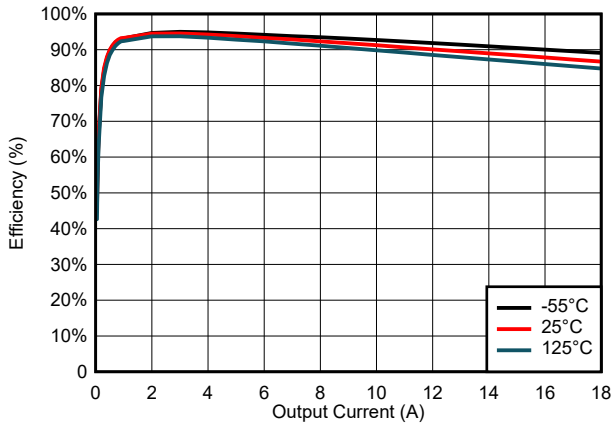
VOUT = 1.8 V, f_{sw} = 500 kHz

図 6-27. Efficiency for VIN = 5 V



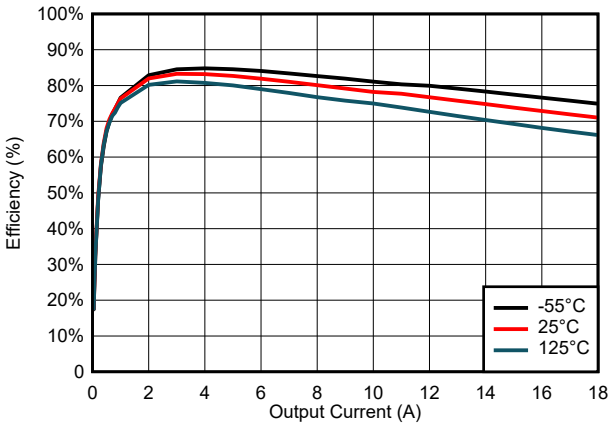
VOUT = 2.5 V, f_{sw} = 500 kHz

図 6-28. Efficiency for VIN = 5 V



VOUT = 3.3 V, f_{sw} = 500 kHz

図 6-29. Efficiency for VIN = 5 V



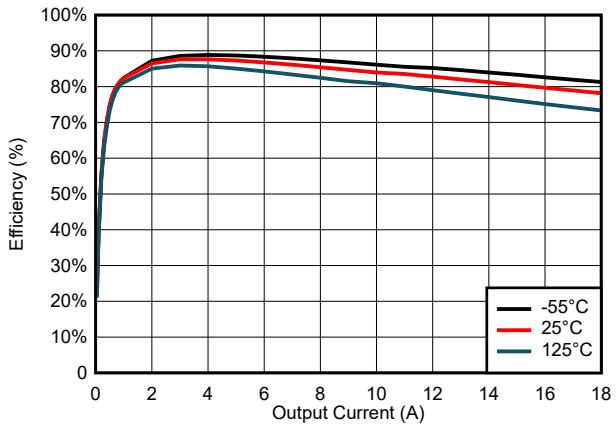
VOUT = 1 V, f_{sw} = 500 kHz

図 6-30. Efficiency for VIN = 7 V

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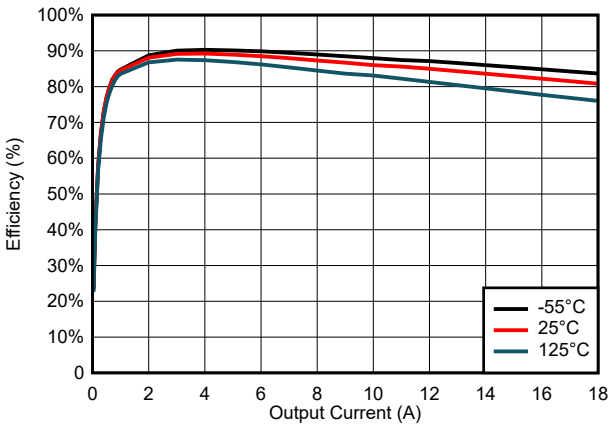
6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.



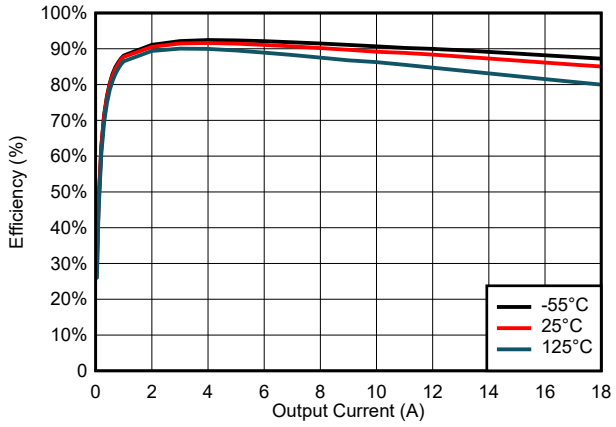
VOUT = 1.5 V, f_{sw} = 500 kHz

図 6-31. Efficiency for VIN = 7 V



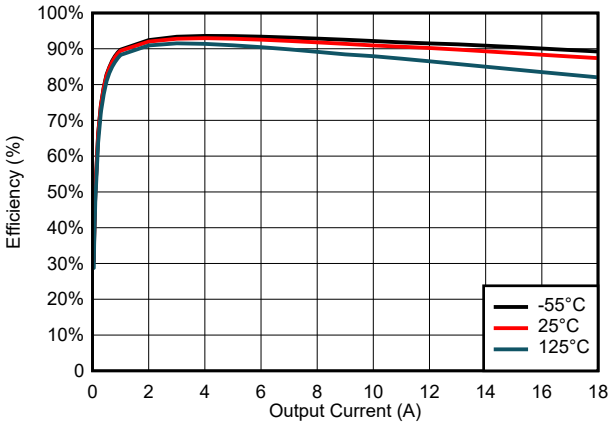
VOUT = 1.8 V, f_{sw} = 500 kHz

図 6-32. Efficiency for VIN = 7 V



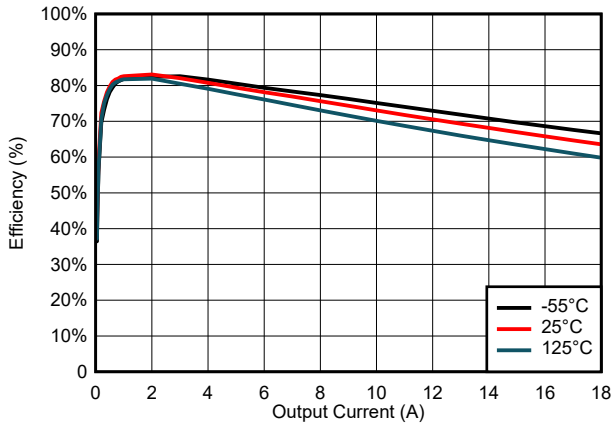
VOUT = 2.5 V, f_{sw} = 500 kHz

図 6-33. Efficiency for VIN = 7 V



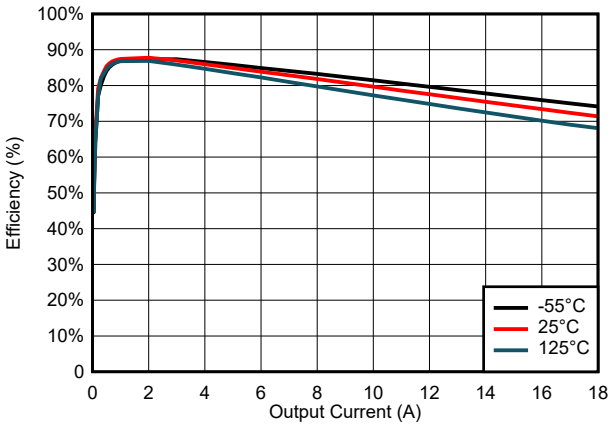
VOUT = 3.3 V, f_{sw} = 500 kHz

図 6-34. Efficiency for VIN = 7 V



VOUT = 1 V, f_{sw} = 1 MHz

図 6-35. Efficiency for VIN = 3 V



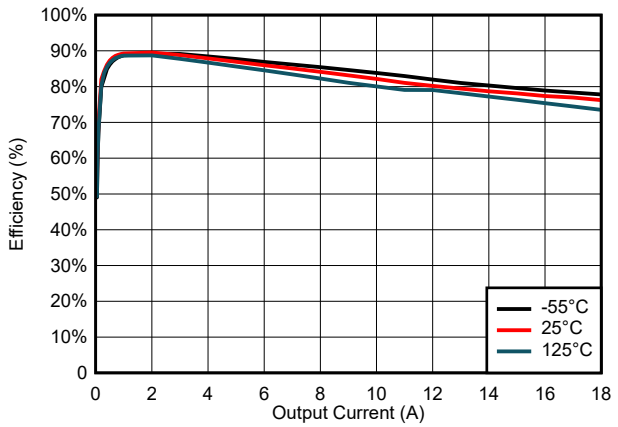
VOUT = 1.5 V, f_{sw} = 1 MHz

図 6-36. Efficiency for VIN = 3 V

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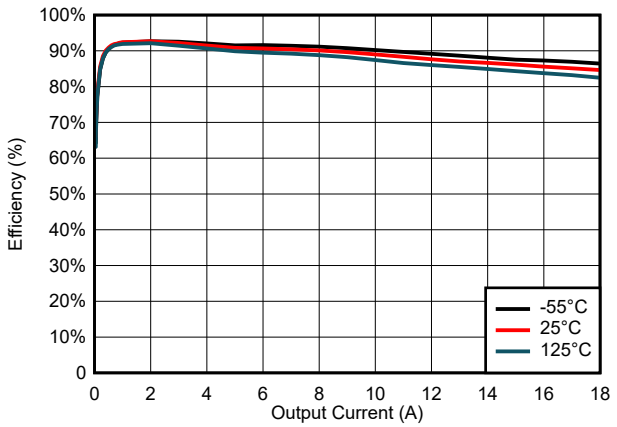
6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.



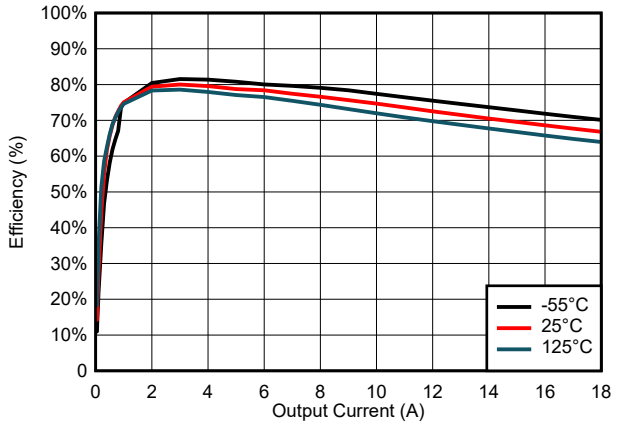
VOUT = 1.8 V, f_{sw} = 1 MHz

図 6-37. Efficiency for VIN = 3 V



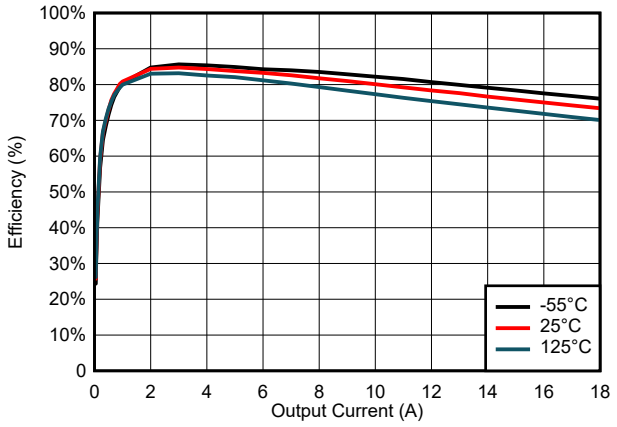
VOUT = 2.5 V, f_{sw} = 1 MHz

図 6-38. Efficiency for VIN = 3 V



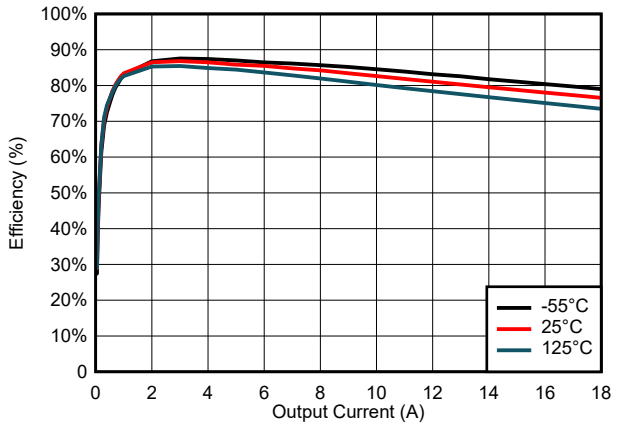
VOUT = 1 V, f_{sw} = 1 MHz

図 6-39. Efficiency for VIN = 5 V



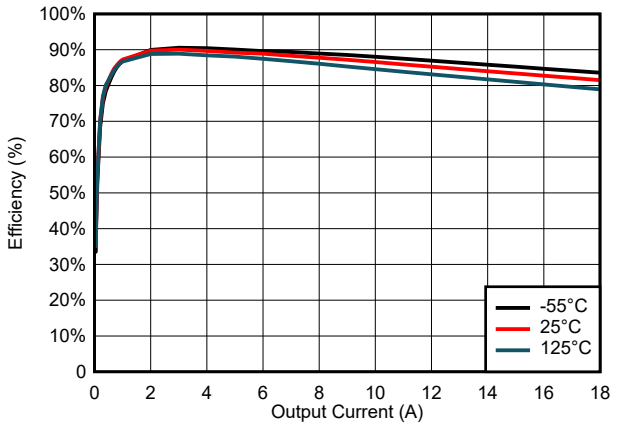
VOUT = 1.5 V, f_{sw} = 1 MHz

図 6-40. Efficiency for VIN = 5 V



VOUT = 1.8 V, f_{sw} = 1 MHz

図 6-41. Efficiency for VIN = 5 V



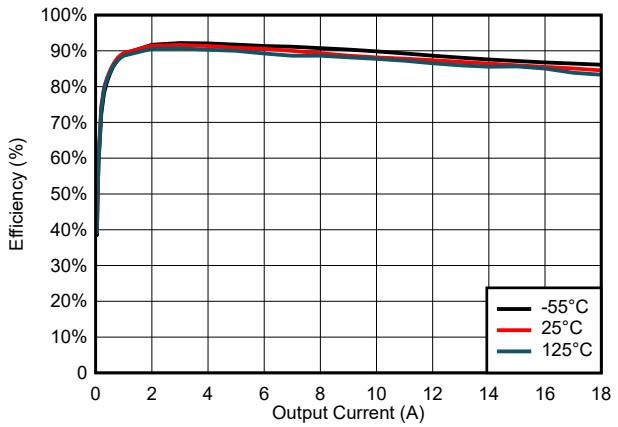
VOUT = 2.5 V, f_{sw} = 1 MHz

図 6-42. Efficiency for VIN = 5 V

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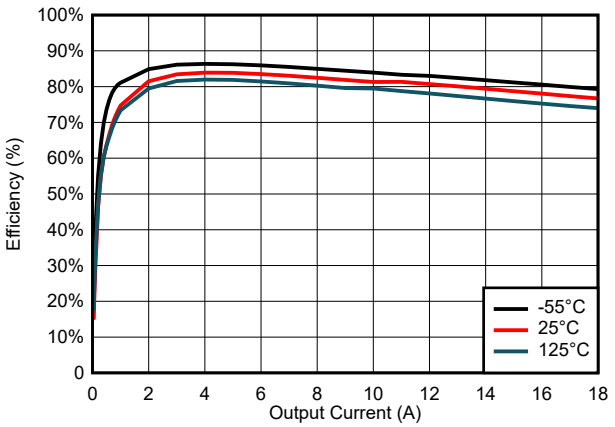
6.6 Typical Characteristics (continued)

Output inductor of L = 10 µH (part number XAL1510-103MED) was used for all 100-kHz efficiency measurements. For 500-kHz and 1-MHz efficiency measurements, output inductor of L = 1 µH (XAL1580-102MED) was used.



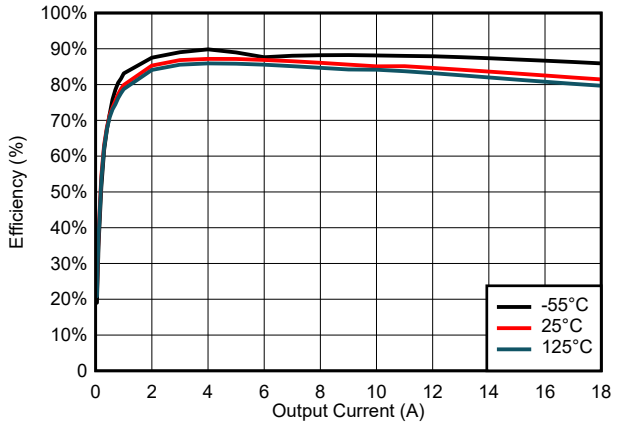
VOUT = 3.3 V, f_{sw} = 1 MHz

図 6-43. Efficiency for VIN = 5 V



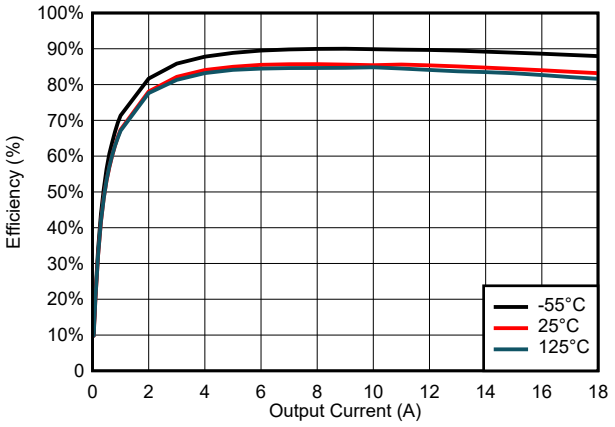
VOUT = 1.8 V, f_{sw} = 1 MHz

図 6-44. Efficiency for VIN = 7 V



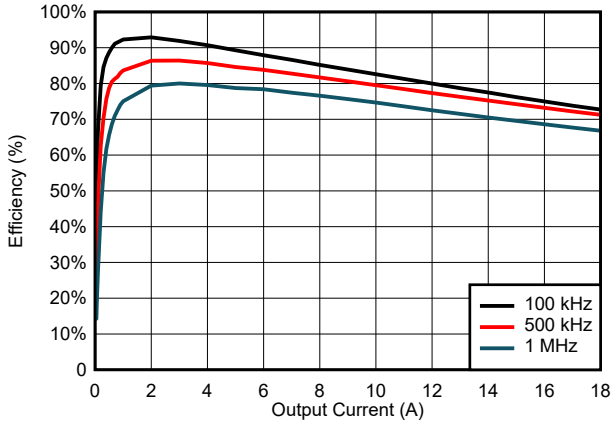
VOUT = 2.5 V, f_{sw} = 1 MHz

図 6-45. Efficiency for VIN = 7 V



VOUT = 3.3 V, f_{sw} = 1 MHz

図 6-46. Efficiency for VIN = 7 V



VOUT = 1 V, f_{sw} = 100 kHz, 500 kHz, 1 MHz

図 6-47. Efficiency for VIN = 5 V

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7 Detailed Description

7.1 Overview

The device is a 7-V, 18-A synchronous step-down (buck) converter with two integrated MOSFETs; a PMOS for the high side and a NMOS for the low side. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control, which also simplifies external frequency compensation. The wide switching frequency, 100 kHz to 1 MHz, allows for efficiency and size optimization when selecting the output filter components. The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 18 A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device is designed for safe monotonic startup into prebiased loads. The default start up is when VIN is typically 2.75 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. The total operating current for the device is approximately 4 mA when not switching and under no load. When the device is disabled, the supply current is typically 2.3 mA.

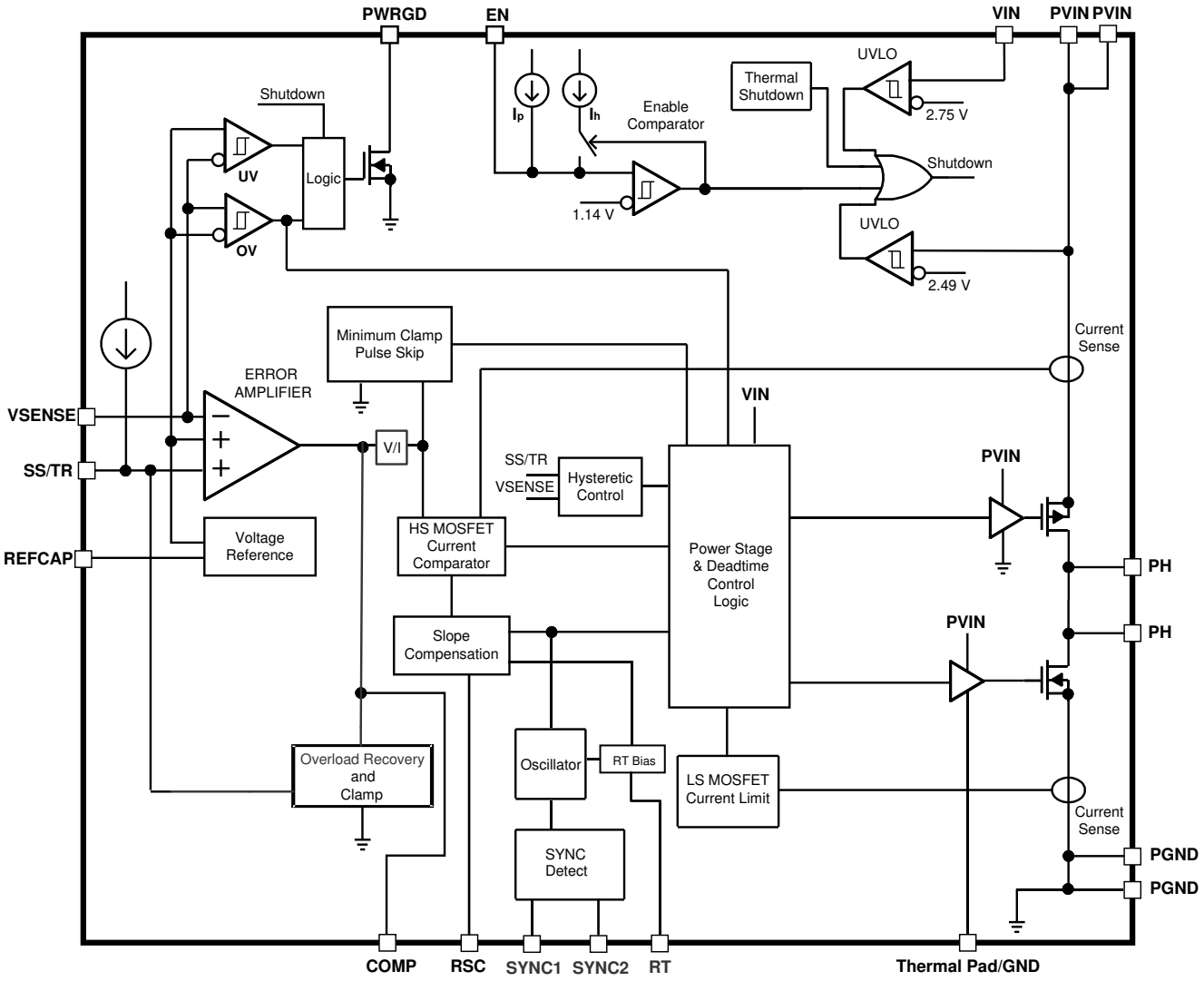
The device has a power-good comparator (PWRGD) with hysteresis, which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open-drain MOSFET, which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage VREF and asserts high when the VSENSE pin voltage is 94% to 106% of the VREF.

The SS/TR (soft-start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power-up. A small-value capacitor or resistor divider should be coupled to the pin for soft-start or critical power-supply sequencing requirements. If VSENSE is greater than the voltage at SS during startup, the device will enter into a pulse-skipping mode.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power-good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the VREF. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections, which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the soft-start circuit automatically when the junction temperature drops 18°C (typical) below the thermal shutdown trip point.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system. Both pins have an input voltage range from 3 V to 7 V. A voltage divider connected to the EN pin can adjust the input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power-up behavior.

7.3.2 Voltage Reference

The device generates an internal 1.21-V bandgap reference that is utilized throughout the various control logic blocks. This is the voltage present on the REFCAP and SS/TR pins during steady state operation. This voltage is divided down to 0.605 V to produce the reference for the error amplifier. The error amplifier reference is measured at the COMP pin to account for offsets in the error amplifier and maintains regulation within ±1.7% across line, load, temperature, and TID as shown in the *Electrical Characteristics*. A 470-nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.

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7.3.3 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. TI recommends to use 1% tolerance or better resistors. Start with a 10 kΩ for R_{TOP} and use 式 1 to calculate R_{BOTTOM}. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R_{BOTTOM} = \frac{V_{REF}}{VOUT - V_{REF}} \times R_{TOP} \quad (1)$$

where

- V_{REF} = 0.605 V

7.3.4 Safe Start-Up Into Prebiased Outputs

The device prevents the low-side MOSFET from discharging a prebiased output lower than the configured output voltage through the VSENSE pin.

7.3.5 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.605-V voltage reference. The transconductance of the error amplifier is 1800 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground. The error amplifier DC gain is typically 10,000 V/V.

7.3.6 Enable and Adjust UVLO

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device enables operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low I_q state. The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150-mV typical.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN in split-rail applications, then the EN pin can be configured as shown in 図 7-1, 図 7-2, and 図 7-3. A ceramic capacitor in parallel with the bottom resistor R_2 is recommended to reduce noise on the EN pin as used in the TPS7H4003-SEP evaluation module (EVM). See the *TPS7H4003EVM-CVAL Evaluation Module (EVM) User's Guide* for more information.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. Calculate the UVLO thresholds with 式 2 and 式 3.

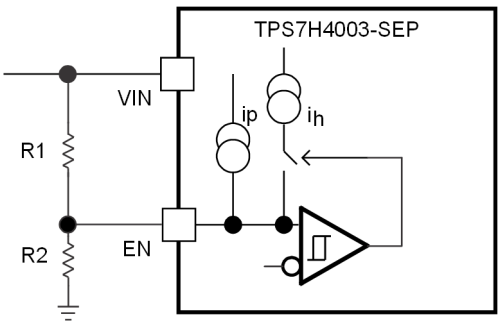


図 7-1. Adjustable VIN UVLO

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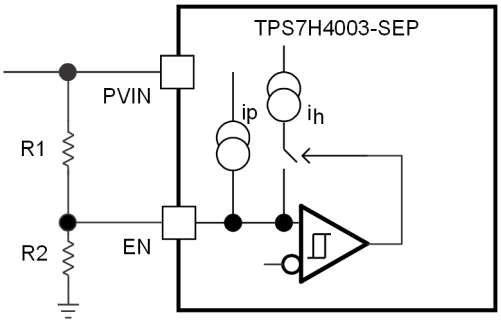


図 7-2. Adjustable PVIN UVLO

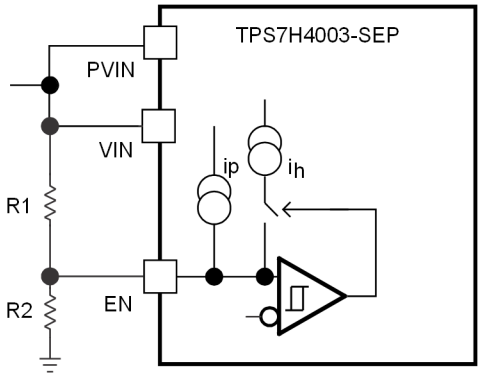


図 7-3. Adjustable VIN and PVIN UVLO

$$R_1 = \frac{V_{START} \times \frac{V_{ENFALLING}}{V_{ENRISING}} - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_p + I_h)} \quad (3)$$

where

- I_h = 3 µA
- I_p = 6.1 µA
- $V_{ENRISING}$ = 1.14 V
- $V_{ENFALLING}$ = 1.11 V

7.3.7 Adjustable Switching Frequency and Synchronization (SYNC)

The switching frequency of the device supports three modes of operations. The modes of operation are set by the conditions on the RT, SYNC1, and SYNC2 pins. At a high level, these modes can be described as internal oscillator, external synchronization, and primary-secondary operation modes.

7.3.7.1 Internal Oscillator Mode

In internal oscillator mode, a resistor is connected between the RT pin and GND to configure the switching frequency, f_{SW}, of the device. The switching frequency is adjustable from 100 kHz to 1 MHz depending on the RT resistor value, which can be calculated using 式 4. 図 7-4 shows the relationship curve between the RT resistor value and the configurable switching frequency range. It is recommended that the SYNC2 pin be connected to GND for this mode of operation.

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$$RT = 223260 \times f_{SW}^{-1.159} \quad (4)$$

where

- RT in kΩ
- f_{SW} in kHz

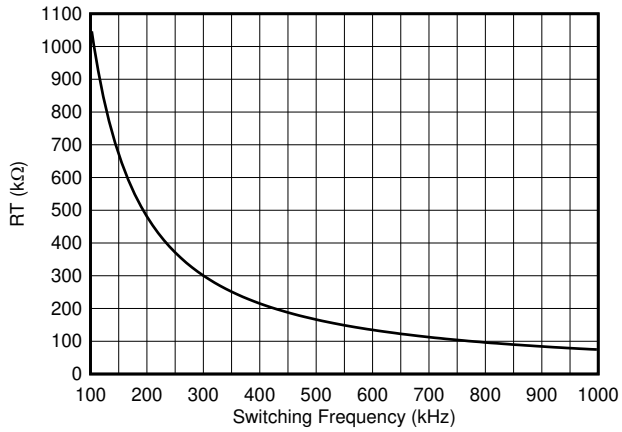


図 7-4. RT vs Switching Frequency

7.3.7.2 External Synchronization Mode

In external synchronization mode, a resistor is connected between the RT pin and GND corresponding to the external clock frequency as indicated in 式 4 and 図 7-4. During this mode of operation, the SYNC1 pin connects to the input clock and the SYNC2 pin must be connected to either GND or VIN depending on whether it is desired to invert the clock SYNC1 receives. When SYNC2 is connected to GND, the clock provided on SYNC1 is inverted. When SYNC2 is connected to VIN, the input clock signal on SYNC1 does not get inverted. As a result, external synchronization mode can be used to connect 2, 3, or 4 devices in parallel using an external clock (at any frequency between 100 kHz and 1 MHz) as long as the clocks used for each device are in the proper out of phase configuration. If no external clock signal is detected for 20 µs, then the TPS7H4003-SEP transitions to its internal clock and a switching frequency that is determined by the value of the RT resistor. If no external clock is available, then the primary-secondary operation mode can also be used to connect devices in parallel.

7.3.7.3 Primary-Secondary Operation Mode

In primary-secondary mode, the RT pin of the primary device must be left floating. This sets the internal switching frequency of the device, f_{SW} to a typical 500 kHz and the SYNC1 pin becomes an output clock at the same frequency and phase as f_{SW}. In addition, the SYNC2 pin becomes an output clock at the same frequency but at 90° out of phase with respect to SYNC1. These SYNC1 and SYNC2 output clock signals, in combination with the state of the SYNC2 pins of the secondary devices, can be used to connect 2, 3, or 4 devices in parallel configuration. 図 7-5 shows the SYNC1 and SYNC2 clock signals when the RT pin is floating in the primary device and how the signals can be used to generate the 90° out of phase clocks needed to connect 4 devices in parallel configuration (1 primary and 3 secondaries). The SYNC1b and SYNC2b indicate the clock signals being inverted either internally or due to the state of the SYNC2 pin in the secondary devices. When SYNC2 is connected to GND, the inverse functionality of the input clock signal in SYNC1 remains the same. When SYNC2 is connected to VIN, the input clock signal in SYNC1 does not get inverted. The RT pin of the secondary devices must have a resistor to GND corresponding to 500 kHz as indicated in 式 4 and 図 7-4.

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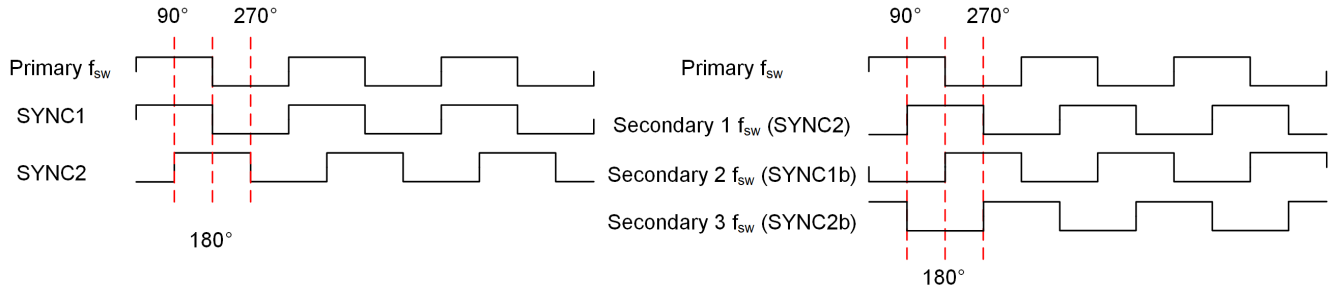


図 7-5. SYNC1 and SYNC2 Clock Signals in Primary-Secondary Mode

図 7-6 shows the SYNC1 and SYNC2 output signals from the primary device as well as signals and connections needed to operate 4 devices in parallel configuration. The f_{SW} clock signal by each device represents the switching frequency signal for the respective device.

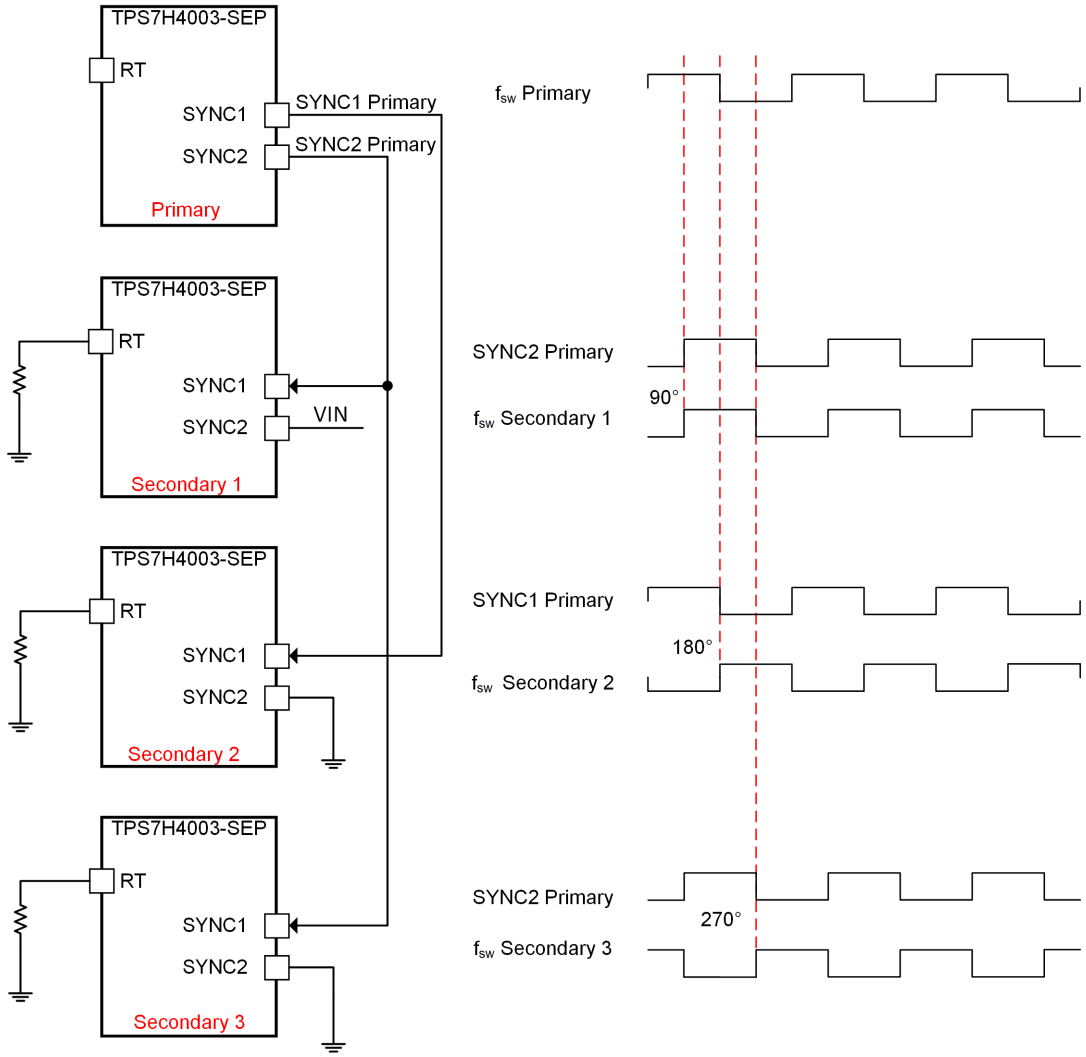


図 7-6. Parallel Operation With SYNC1 and SYNC2 Pins

The 3 modes previously described are summarized in 表 7-1.

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表 7-1. Switching Frequency, SYNC, and RT Pin Usage Table

MODE	RT PIN	SYNC1 PIN	SYNC2 PIN	SWITCHING FREQUENCY
Internal oscillator	Resistor to GND based on 図 7-4	Floating	GND	Configurable using internal oscillator from 100 kHz to 1 MHz depending on RT resistor value
External synchronization		External input clock. Signal will be inverted internally	GND or VIN	Internally synchronized to external clock between 100 kHz to 1 MHz
Primary	Float	Outputs 500-kHz clock in phase with internal switching frequency	Outputs 500-kHz clock at 90° out of phase with internal switching frequency	500 kHz

7.3.8 Soft-Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A C_{SS} capacitor on the SS/TR pin to GND implements a soft-start time. 式 5 shows the equation for the nominal soft-start time, t_{SS}. This is the time it will take VOUT to go from 10% to 90% of the programmed voltage. The voltage reference (VREF) is 0.605 V and the soft-start charge current (I_{SS}) is 2.5 µA. When calculating the soft-start time t_{SS}, it is important to take into account the variation of the parameters C_{SS}, VREF and I_{SS} as these may cause t_{SS} to deviate from the nominal value in the actual implementation.

$$t_{SS}\,(ms) = \frac{0.8 \times C_{SS}\,(nF) \times V_{REF}\,(V)}{I_{SS}\,(\mu A)} \tag{5}$$

When any of the following four scenarios occur the SS/TR pin is discharged:

- the input UVLO is triggered,
- the EN pin is pulled below 1.05 V,
- the high-side switch current limit threshold is exceeded, or
- a thermal shutdown event occurs.

With the exception of the scenario where the high-side current limit threshold is exceeded, the device will then stop switching and enter into low current operation. At the subsequent power-up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

The device will enter into a pulse-skipping mode during start-up in the event that VSENSE is greater than the voltage at the SS/TR pin. During this period, the high-side switch will remain off and the low-side switch will remain on until VSENSE again falls below the voltage at SS/TR.

7.3.9 Power Good (PWRGD)

The PWRGD pin is an open-drain output. When the VSENSE pin is between 94% and 106% of the internal voltage reference, the PWRGD pin pulldown is deasserted and the pin floats. TI recommends to use a pullup resistor between 10 kΩ to 100 kΩ to a voltage source that is equal to or less than VIN. The PWRGD is in a defined state when the VIN input voltage is greater than 1 V but has reduced current sinking capability. The PWRGD achieves full current sinking capability when the VIN input voltage is above 3 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low if:

- the input UVLO or thermal shutdown are asserted,
- the EN pin is pulled low, or
- the SS/TR pin is below 1.1 V.

7.3.10 Sequencing

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins.

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The sequential method is shown in 図 7-7 using two TPS7H4003-SEP devices. The PWRGD pin of the first device is coupled to the EN pin of the second device, which enables the second power supply after the primary supply reaches regulation.

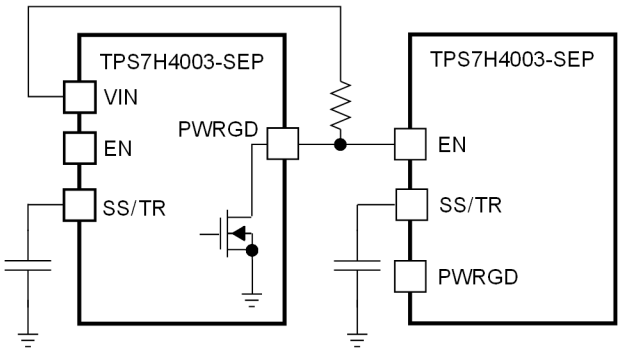


図 7-7. Sequential Start-Up Sequence

図 7-8 shows the method implementing ratiometric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pullup current source must be doubled in 式 5 as there is only one SS/TR capacitor. A similar situation applies if a resistor divider is used in the EN pin, that is, only one resistor divider is needed and the factor of 2 must be taken into account when calculating the resistor values. This ratiometric connection is the one used in primary mode as described in the *Adjustable Switching Frequency and Synchronization (SYNC)* section.

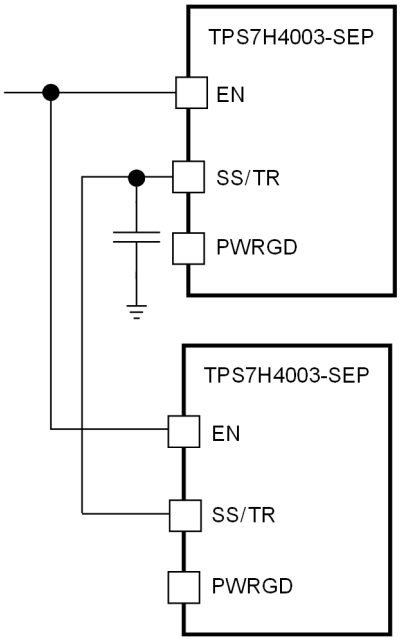


図 7-8. Ratiometric Start-Up Sequence

Ratiometric and simultaneous power-supply sequencing can be implemented by connecting the resistor network of R_1 and R_2 (shown in 図 7-9) to the output of the power supply that needs to be tracked or another voltage reference source. Using 式 6 and 式 7, the tracking resistors can be calculated to initiate the $VOUT_2$ slightly before, after, or at the same time as $VOUT_1$. 式 8 is the voltage difference between $VOUT_1$ and $VOUT_2$.

To design a ratiometric start-up in which the $VOUT_2$ voltage is slightly greater than the $VOUT_1$ voltage when $VOUT_2$ reaches regulation, use a negative number in 式 6 and 式 7 for ΔV. 式 8 results in a positive number for applications where the $VOUT_2$ is slightly lower than $VOUT_1$ when $VOUT_2$ regulation is achieved.

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The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{SS-OFFSET}$ = 30 mV) in the soft-start circuit and the offset created by the pullup current source (I_{SS} = 2.5 µA) and tracking resistors, the $V_{SS-OFFSET}$ and I_{SS} are included as variables in the equations.

To ensure proper operation of the device, the calculated R_1 value from 式 6 must be greater than the value calculated in 式 9.

$$R_1 = \frac{VOUT_2 + \Delta V}{V_{REF}} \times \frac{V_{SS-OFFSET}}{I_{SS}} \tag{6}$$

$$R_2 = \frac{V_{REF} \times R_1}{VOUT_2 + \Delta V - V_{REF}} \tag{7}$$

$$\Delta V = VOUT_1 - VOUT_2 \tag{8}$$

$$R_1 > 2800 \times VOUT_1 - 180 \times \Delta V \tag{9}$$

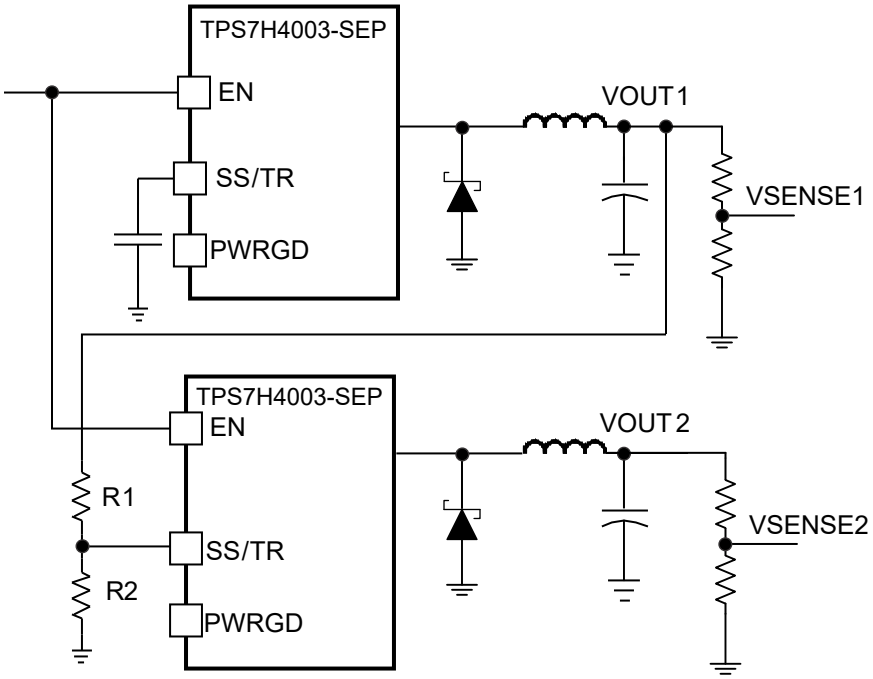


図 7-9. Ratiometric and Simultaneous Start-Up Sequence

7.3.11 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

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7.3.12 Overcurrent Protection

The device is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side and low-side MOSFET.

7.3.12.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control, which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off. In the event of an overcurrent detection, the following sequence of events occurs:

1. The SS/TR pin is discharged.
2. When the voltage at SS/TR falls below VSENSE, the device will stop switching.
3. As VOUT decreases, VSENSE does as well. At the point when VSENSE is equal to the voltage at SS/TR, the device will begin switching again.

7.3.12.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

When the low-side MOSFET turns off, the switch node voltage increases and forward biases the high-side MOSFET parallel diode (the high-side MOSFET is still off at this stage).

7.3.13 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 190°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 172°C (typical).

7.3.14 Turn-On Behavior

Minimum on-time specification determines the maximum operating frequency of the design. During soft-start, if the required duty cycle is less than the minimum controllable on-time, the device can enter into a pulse-skipping mode. Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is only evident when operating at high frequency with high bandwidth. When the minimum on-pulse is greater than the minimum controllable on-time, the turn-on behavior is normal.

7.3.15 Slope Compensation

The device adds a compensating ramp to the switch current signal for all duty cycles. The slope compensation adjusts the peak current during the charging of the inductor to avoid instability of the system. As a result, the ideal slope compensation is defined as the output voltage divided by the inductor size as shown in 式 10. The slope compensation, SC, can be configured with a resistor to GND connected to the RSC pin. The RSC resistor value, in kΩ, can be calculated using 式 11, where SC is in A/µs and f_{SW} is in kHz.

$$SC_{ideal} = \frac{di}{dt} = \frac{VOUT}{L} \tag{10}$$

$$RSC = \frac{24000}{f_{SW}} + \frac{1040}{SC} - 30 \tag{11}$$

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7.3.15.1 Slope Compensation Requirements

All the design parameters are relevant when configuring the slope compensation. The first requirement is that the inductor peak current I_{Lpeak} must be less than the compensated maximum high side FET current, I_{Lmax} as shown in 式 12.

$$I_{Lpeak} < I_{Lmax} \tag{12}$$

I_{Lpeak} can be calculated as shown in 式 13, where K_L relates I_{ripple} the inductor ripple current, to I_O the output current, as shown in 式 14.

$$I_{Lpeak} = I_O + \frac{I_{ripple}}{2} = I_O + \frac{K_L \times I_O}{2} \tag{13}$$

$$K_L = \frac{I_{ripple}}{I_O} \tag{14}$$

I_{Lmax} is defined as the difference between the high side current limit specified in the *Electrical Characteristics*, and the change in current due to the ramp, I_{SC} as shown in 式 15. I_{SC} can be calculated using 式 16, where t_{ON} is the on time for the high side FET. t_{ON} depends on the switching frequency and is related to the duty cycle as shown in 式 17.

$$I_{Lmax} = I_{HS_IL} - I_{SC} \tag{15}$$

$$I_{SC} = SC \times t_{ON} \tag{16}$$

$$t_{ON} = \frac{1}{f_{SW}} \times D = \frac{1}{f_{SW}} \times \frac{VOUT}{VIN} \tag{17}$$

The last requirement related to the slope compensation is related to the maximum value for K_L depending on the SC value selected so that the desired I_O can be supported. In other words, the maximum value for K_L such that I_{Lpeak} is less than I_{Lmax}. By substituting 式 16 and 式 17 into the combinations of 式 13 and 式 15, the equation for the maximum value for K_L can be derived as shown in 式 18.

$$K_{Lmax} < 2\left[\frac{I_{HS_IL} - \frac{SC}{f_{SW}}\left(\frac{VOUT}{VIN} - 0.25\right)}{I_O} - 1\right] \tag{18}$$

7.3.16 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits shown in 図 7-10. In Type 2A, one additional high-frequency pole is added to attenuate high-frequency noise.

The following design guidelines are provided for advanced users who prefer to compensate using the general method.

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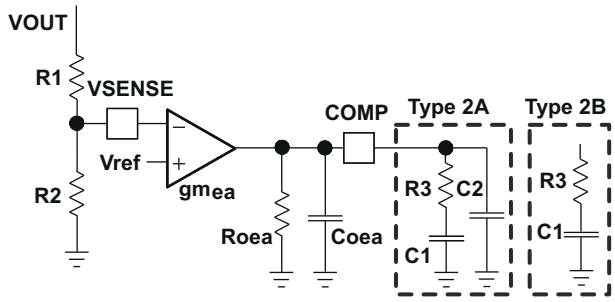


図 7-10. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency f_{co}. A good starting point is one-tenth of the switching frequency, f_{SW}.
2. R_3 can be determined by:

$$R_3 = \frac{2\pi \times f_{co} \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{ps}} \quad (19)$$

   where gm_{ea} is the transconductance of the error amplifier (1800 µS), gm_{ps} is the transconductance of the power stage (40 S) and VREF is the reference voltage (0.605 V).
3. Place a compensation zero at the dominant pole calculated in 式 20 using C_1 and R_3.
   C_1 can be determined by 式 21.

$$f_p = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (20)$$

$$C_1 = \frac{C_{OUT} \times R_L}{R_3} \quad (21)$$

4. C_2 is optional. It can be used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor C_{OUT}.

$$C_2 = \frac{C_{OUT} \times R_{ESR}}{R_3} \quad (22)$$

7.4 Device Functional Modes

7.4.1 Fixed-Frequency PWM Control

The device uses fixed frequency, peak current mode control. As a synchronous buck converter, the device normally operates in continuous current mode under all load conditions. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier, which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference, which compares to the high-side power switch current. When the power switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H4003-SEP device is a highly-integrated synchronous step-down DC-DC converter. The device is used to convert a higher DC-DC input voltage to a lower DC output voltage with a maximum output current of 18 A.

The TPS7H4003-SEP user's guide is available on the TI website, *TPS7H4003EVM-CVAL Evaluation Module (EVM) User's Guide*. The guide highlights standard EVM test results, schematic, and BOM for reference.

8.2 Typical Application

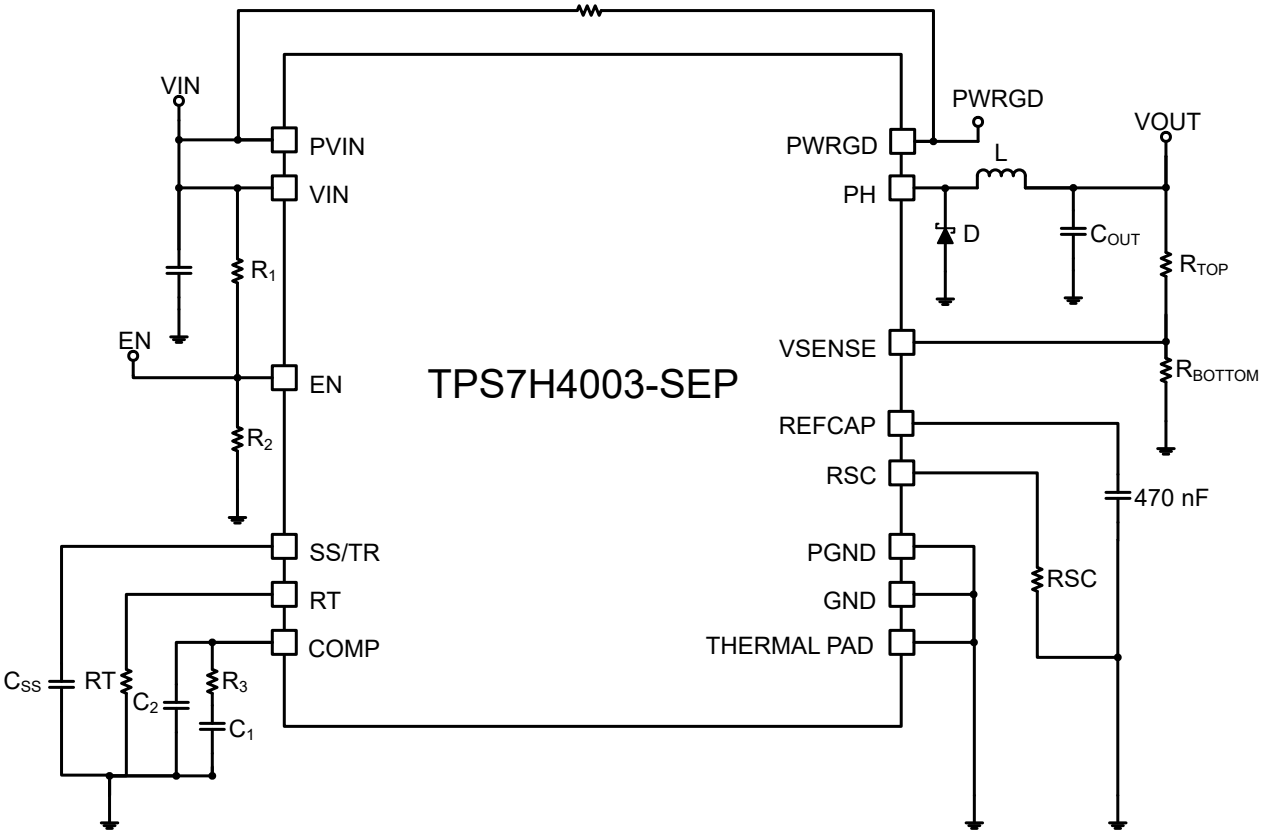


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This example highlights a design using the TPS7H4003-SEP based on its evaluation module. For more details, please refer to the EVM user's guide, *TPS7H4003EVM-CVAL Evaluation Module (EVM) User's Guide*. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	1 V
Maximum output current	18 A
Transient response 9-A load step	ΔVOUT = 5%
Input voltage	5 V
Output voltage ripple	20 mVp-p
Start input voltage (rising V_{IN})	4.5 V
Stop input voltage (falling V_{IN})	4.3 V
Switching frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance. In this design, a switching frequency of 500 kHz is selected. Since the regulator can internally generate a 500-kHz switching frequency, no RT resistor is necessary but can be used if desired.

8.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use 式 23. K_L is a coefficient that represents the amount of inductor ripple current relative to the maximum output current, I_O as shown in 式 14. The inductor ripple current is filtered by the output capacitor, therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer depending on specific system needs. Typical values for K_L range from 0.1 to 0.5. For low output currents, the value of K_L could be increased to reduce the value of the output inductor.

$$L = \frac{V_{INMAX} - VOUT}{I_O \times K_L} \times \frac{VOUT}{V_{INMAX} \times f_{SW}} \tag{23}$$

For this design example, use K_L = 0.1 and the inductor value is calculated to be 0.9 µH for nominal VIN = 5 V.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from 式 25 and 式 26.

$$I_{ripple} = \frac{V_{INMAX} - VOUT}{L} \times \frac{VOUT}{V_{INMAX} \times f_{SW}} \tag{24}$$

$$I_{Lrms} = \sqrt{{I_O}^2 + \frac{1}{12} \times \left(\frac{VOUT \times (V_{INMAX} - VOUT)}{V_{INMAX} \times L \times f_{SW}}\right)^2} \tag{25}$$

$$I_{Lpeak} = I_O + \frac{I_{ripple}}{2} \tag{26}$$

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For this design, the RMS inductor current is 18 A and the peak inductor current is 18.9 A. In order to satisfy all requirements, a 1-µH Coilcraft XAL1580 inductor was used.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.3 Output Capacitor Selection

There are several considerations in determining the value of the output capacitor. The selection of the output capacitor is driven by both the desired output voltage ripple and the allowable voltage deviation due to a large and abrupt change in load current. For space applications, the value of capacitance also has to account for the mitigation of single-event effects (SEE). The output capacitance needs to be selected based on the more stringent of these three criteria. It is also important to note that the value of the output capacitor directly influences the modulator pole of the converter frequency response, as shown in *Small Signal Model for Frequency Compensation*.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. 式 27 shows the minimum output capacitance, from the electrical point of view, necessary to accomplish this.

$$C_{OUT} > \frac{2 \times \Delta I_O}{f_{SW} \times \Delta VOUT} \tag{27}$$

Where ΔI_O is the change in output current, f_{SW} is the regulator switching frequency, and ΔVOUT is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in VOUT for a load step of 9 A. Also in this example, ΔI_O = 9 A and ΔVOUT = 0.05 × 1 = 0.05 V. Using these numbers gives a minimum capacitance of 720 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. However, for space applications and large capacitance values, tantalum capacitors are typically used, which have a certain ESR value to take into consideration.

式 28 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, $VOUT_{ripple}$ is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current. In this case, the maximum output voltage ripple is 20 mV and the inductor ripple current is 1.8 A. Under these conditions, 式 28 yields 22.5 µF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{I_{ripple}}{VOUT_{ripple}} \tag{28}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in, which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. 式 25 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 式 25 yields 519 mA.

式 29 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. 式 29 indicates the ESR should be less than 11.11 mΩ.

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$$R_{ESR} < \frac{VOUT_{ripple}}{I_{ripple}} \quad (29)$$

For this specific design, taking into consideration the stringent requirements for space applications, a total output capacitance of 2 mF with an equivalent ESR of approximately 2 mΩ has been selected. The output voltage deviation with this larger output capacitance was approximately 3.5% for a 9-A load step. This output voltage deviation can be further reduced by increasing the output capacitance.

8.2.2.4 Output Schottky Diode

図 8-1 shows a Schottky diode between the phase node pin (PH) and GND of the TPS7H4003-SEP. This external diode is in parallel with the internal low-side power FET of the device and typically has superior reverse recovery characteristics when compared to the body diode of the internal low-side FET. This improved reverse recovery provides two key benefits. The first benefit is an better overall efficiency for the converter due to lower losses associated with the diode reverse recovery. The second key advantage is that the parasitic-induced noise associated with the reverse recovery current pulse (as detailed in Figure 5 of *Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters*) is drastically reduced. In the absence of the Schottky diode, this noise can manifest itself on the power ground plane internal to the TPS7H4003-SEP. If significant enough, the noise can reduce the dynamic range of the error amplifier and result in higher output voltage ripple. For this reason, it is highly recommended to use the external Schottky diode in the converter design. At the least, a PCB footprint for the diode should be included in the PCB design phase in case it is needed to achieve the system requirements.

8.2.2.5 Input Capacitor Selection

The TPS7H4003-SEP requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins, and 4.7 µF on the VIN input voltage pin. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS7H4003-SEP. The input ripple current can be calculated using 式 30.

$$I_{CINrms} = I_O \times \sqrt{\frac{V_{OUT}}{V_{IN_MIN}} \times \frac{(V_{IN_MIN} - V_{OUT})}{V_{IN_MIN}}} \quad (30)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example, six 16-V, 22-µF ceramic capacitors and two 10-V, 330-µF polymer tantalum capacitors in parallel have been selected as the VIN and PVIN inputs are tied together so the TPS7H4003-SEP may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 31. Using the design example values, I_{OMAX} = 18 A, C_{IN} = 792 µF, f_{SW} = 500 kHz, yields an input voltage ripple of 11.4 mV and a RMS input ripple current of 7.2 A.

$$\Delta VIN = \frac{I_{OMAX} \times 0.25}{C_{IN} \times f_{SW}} \quad (31)$$

8.2.2.6 Soft-Start Capacitor Selection

The soft-start capacitor C_{SS}, determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge

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the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS7H4003-SEP reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft-start capacitor value can be calculated using 式 5. The example circuit has the soft-start time set to an arbitrary value of about 2 ms, which requires a 10-nF capacitor. In TPS7H4003-SEP, I_{SS} is 2.5-µA typical, and V_{REF} is 0.605 V.

8.2.2.7 Undervoltage Lockout (UVLO) Set Point

The UVLO can be adjusted using the external voltage divider network formed by R_1 and R_2. R_1 is connected between VIN and the EN pin of the TPS7H4003-SEP and R_2 is connected between EN and GND. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above selected voltage (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below (UVLO stop or disable) voltage. 式 2 and 式 3 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified in 表 8-1, the nearest standard resistor value for R_1 is 10 kΩ and for R_2 is 3.4 kΩ.

8.2.2.8 Output Voltage Feedback Resistor Selection

The resistor divider network R_{TOP} and R_{BOTTOM} is used to set the output voltage. For the example design, 10 kΩ was selected for R_{TOP}. Using 式 1, R_{BOTTOM} is calculated as 15.32 kΩ. The nearest standard 1% resistor is 15.4 kΩ.

8.2.2.8.1 Minimum Output Voltage

Due to the internal design of the TPS7H4003-SEP, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.605 V. Above 0.605 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by 式 32.

$$V_{OUTMIN} = V_{INMIN} \times t_{ON,MIN} \times f_{sw} \tag{32}$$

In this equation:

- V_{OUTMIN} is the minimum output voltage
- V_{INMIN} is the minimum input voltage for the application
- $t_{ON,MIN}$ is the minimum on-time for the device, for which the maximum specification is 235 ns
- f_{sw} is the switching frequency of the application.

8.2.2.9 Compensation Component Selection

There are several industry techniques used to compensate DC-DC regulators. For this design, type 2B compensation is used as shown in the *Small Signal Model for Frequency Compensation* section.

A good starting rule of thumb is to set the crossover frequency to one-tenth of the switching frequency. This will generally provide good transient response and ensure that the modulator poles do not degrade phase margin.

The compensation components can be calculated using 式 19 and 式 21. The values calculated for R_3 and C_1 are 8.66 kΩ and 12 nF, respectively. Note that frequency compensation is often tuned during testing in order to obtain the best possible performance.

An additional high frequency pole can be used if necessary by adding a capacitor in parallel with the series combination of R_3 and C_1. The pole frequency is given by 式 33.

$$f_p = \frac{1}{2\pi \times R_3 \times C_2} \tag{33}$$

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8.2.3 Parallel Operation

The TPS7H4003-SEP can be configured in primary-secondary mode to provide up to 72-A output current. 図 8-2 shows a parallel configuration that can be used to provide 36-A output.

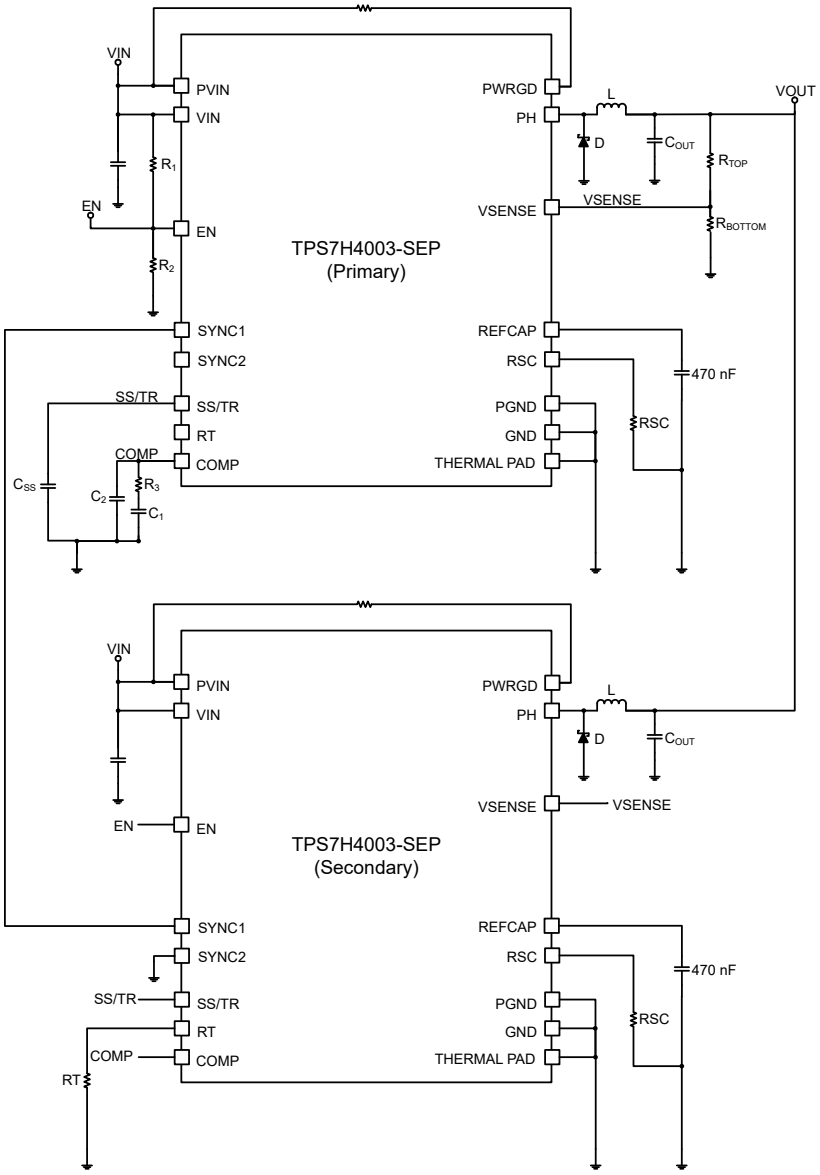


図 8-2. Parallel Configuration Showing Primary and Secondary

The design procedure to configure the primary-secondary operation using the internal oscillator is as follows:

- The RT pin of the primary device must be left floating. This achieves two purposes, to set the frequency to 500 kHz (typical) using the internal oscillator and to configure the SYNC1 and SYNC2 pins of the primary device as output pins with a 500-kHz clock, in-phase and 90° out of phase, respectively to the internal oscillator of the primary device. For more details, see *Adjustable Switching Frequency and Synchronization (SYNC)* section.
- The RT pin on secondary device should be connected to a resistor such that the frequency of the secondary device matches the primary's frequency, 500 kHz in this case. See 図 7-4 for reference.
- SYNC1 and/or SYNC2 pin of the primary device must be connected to the SYNC1 pin of the secondary device(s).

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- Only a single feedback network is connected to the VSENSE pin of the primary device. Therefore, all VSENSE pins must be connected.
- Only a single compensation network is needed connected to the COMP pin of the primary device. Therefore all COMP pins must be connected.
- Only a single soft-start capacitor is needed connected to the SS pin of the primary device. Therefore all SS pins must be connected.
- Only a single enable signal (or resistor divider) is needed connected to the EN pin of the primary device. Therefore all EN pins must be connected.
- Since the primary device controls the compensation, soft-start and enable networks, the factor of n must be taken into account when calculating the components associated with these pins, where n is the number of devices in parallel.

The primary-secondary mode can also be implemented using an external clock. In such case, a different frequency other than 500 kHz can be used. When using an external clock, the RT and SYNC pin configurations vary as follows:

- RT pins of both primary and secondary device must be connected to a resistor matching the frequency of the external clock being used. See 図 7-4 for reference.
- The external clock is connected to the SYNC1 pin of the primary device. A 10-kΩ resistor to GND should be connected to the SYNC1 pin as well.
- For two devices in parallel, an inverted clock (180° out of phase respect to the primary device) must be connected to the SYNC1 pin of the secondary device. A 10-kΩ resistor to GND should be connected to the SYNC1 pin as well. The SYNC2 pins of the primary and secondary devices should be connected to VIN.
- Another option for two devices in parallel is to use a single clock connected to the SYNC1 pins of both devices, with the SYNC2 pin of the primary device connected to VIN and the SYNC2 pin of the secondary device connected to GND.
- For four devices in parallel, the SYNC1 pin of each device can be supplied with a separate clock, each phase shifted 90° with respect to the other. In this configuration, all SYNC2 pins should be connected to VIN. There is also an option where two clocks can be used, where the second clock is phase shifted 90° with respect to the first. In this instance, the table below details how the SYNC1 and SYNC2 pins of each device should be configured.

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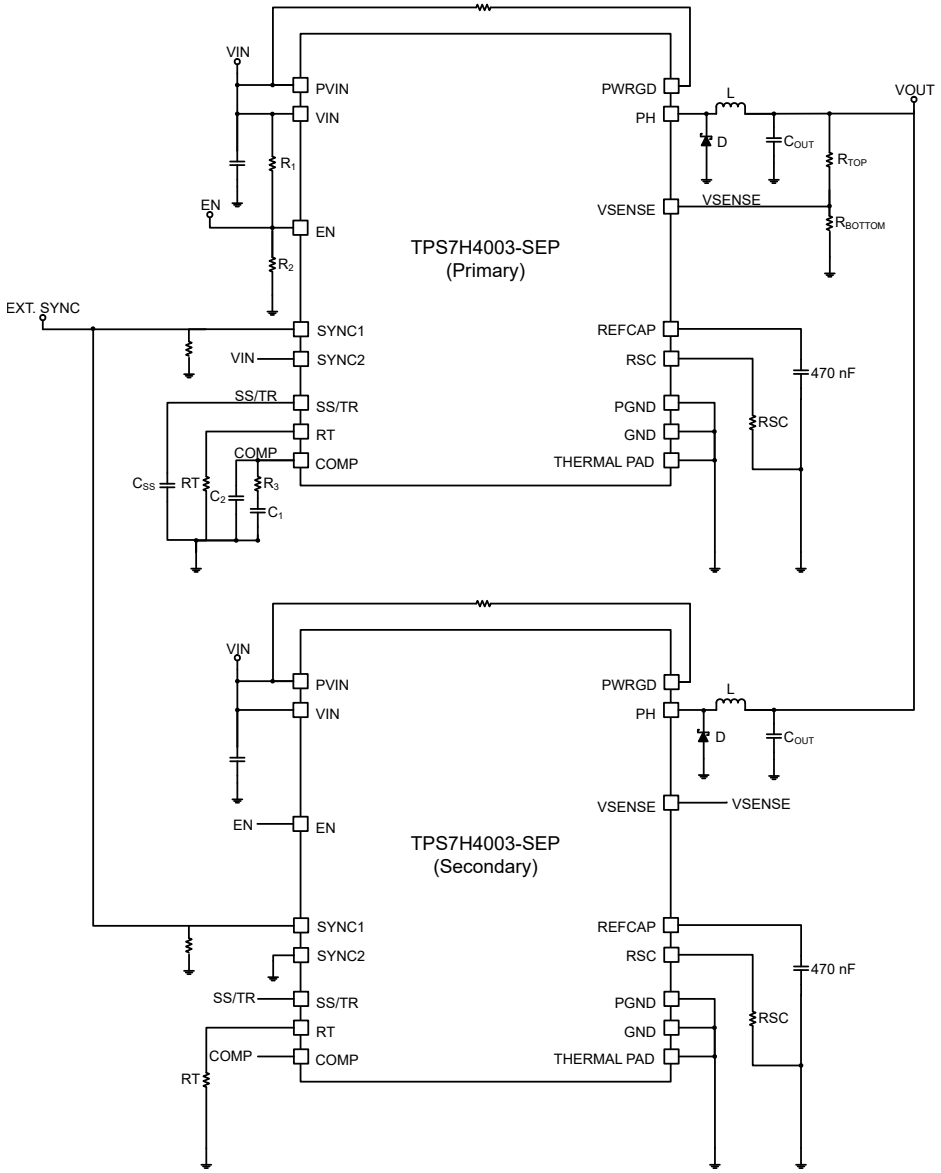


図 8-3. Parallel Configuration With External Sync

表 8-2. Pin Connections for Four Parallel Devices Using External Sync and Two Clocks

Device	SYNC1 Pin	SYNC2 Pin
1	Clock 1	VIN
2	Clock 2	VIN
3	Clock 1	GND
4	Clock 2	GND

The operation of multiple devices in parallel has an impact on some of the component calculations. For instance, since the enable pins are all connected together, the UVLO calculation as presented in the *Enable and Adjust UVLO* section will be modified according to the following equations, in which n is the number of paralleled devices:

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$$R_1 = \frac{V_{START} \times \frac{V_{ENFALLING}}{V_{ENRISING}} - V_{STOP}}{n \times I_p \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + (n \times I_h)} \quad (34)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + (n \times R_1)(I_p + I_h)} \quad (35)$$

Also, since all SS/TR pins will be connected for the paralleled devices, the soft-start calculation presented in the *Soft-Start (SS/TR)* section will be modified according to the following equation:

$$t_{SS}\,(ms) = \frac{0.8 \times C_{SS}\,(nF) \times V_{REF}\,(V)}{n \times I_{SS}\,(\mu A)} \quad (36)$$

The compensation design is detailed in the *Small Signal Model for Frequency Compensation* section. The equation for R_3 changes when the COMP pins of the devices in parallel are connected:

$$R_3 = \frac{2\pi \times f_{co} \times VOUT \times C_{OUT}}{n \times gm_{ea} \times V_{REF} \times n \times gm_{ps}} = \frac{2\pi \times f_{co} \times VOUT \times C_{OUT}}{n^2 \times gm_{ea} \times V_{REF} \times gm_{ps}} \quad (37)$$

Note that for parallel operation, the equations for the other compensation components, C1 and C2, will remain unchanged and still be calculated as shown in 式 21 and 式 22 due to the updated R3 calculation.

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8.2.4 Application Curve

The evaluation module for the TPS7H4003-SEP was used to capture a load step response of the device. The testing conditions were:

- VIN = PVIN = 5 V
- VOUT = 1 V
- Load step = 9 A to 18 A
- Switching frequency = 500 kHz

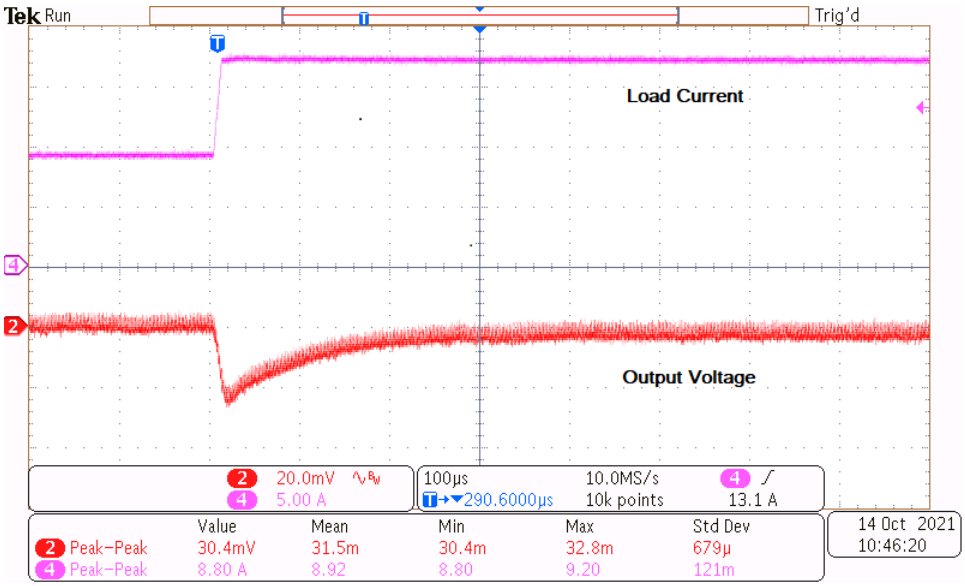


図 8-4. 9-A to 18-A Step Response for 500-kHz Switching Operation

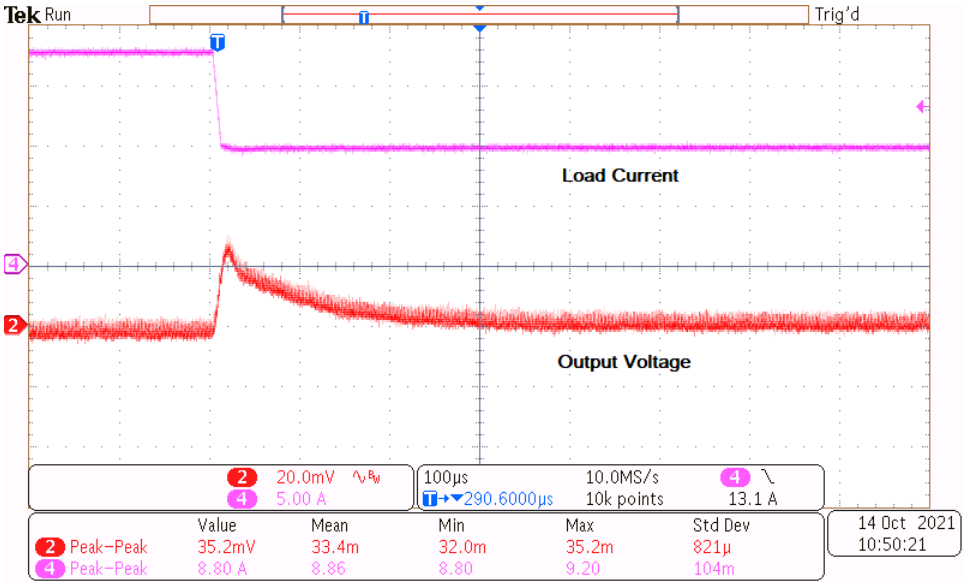


図 8-5. 18-A to 9-A Step Response for 500-kHz Switching Operation

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9 Power Supply Recommendations

The TPS7H4003-SEP is designed to operate from an input voltage supply range between 3 V and 7 V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7 µF (after de-rating) ceramic capacitor, type X5R or better from PVIN to GND, and from VIN to GND. Additional local ceramic bypass capacitance may be required in systems with small input ripple specifications, as well as additional bulk capacitance if the TPS7H4003-SEP device is located more than a few inches away from its input power supply. Bypass capacitors should be placed as close as possible to the input pins and have a low impedance path to GND.

Larger values of bypass capacitance will improve the response to radiation induced transients. The TPS7H4003-SEP Evaluation Module uses 6 × 22-µF capacitors in addition to 2 × 330-µF capacitors in parallel on the PVIN input. In systems with an auxiliary power rail available, the power stage input, PVIN, and the analog power input, VIN, may operate from separate input supplies.

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10 Layout

10.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See the *Layout Example* section for a PCB layout example.
- It is recommended to include a large topside area filled with ground. This top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS7H4003-SEP device to provide a thermal path from the exposed thermal pad land to ground. For operation at full rated load, the top side ground area together with the internal ground plane must provide adequate heat dissipating area.
- The GND pin should be tied directly to the thermal pad under the IC.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
- The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric. Make sure to connect this capacitor to the quieter analog ground trace rather than the power ground trace of the PVIN bypass capacitor.
- Since the PH connection is the switching node, the output inductor should be located close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- It is critical to keep the feedback trace away from inductor EMI and other noise sources. Run the feedback trace as far from the inductor, phase (PH) node, and noisy power traces as possible. Avoid routing this trace directly under the output inductor if possible. If not possible, ensure that the trace is routed on another layer with a ground layer separating the trace and inductor.
- Keep the resistive divider used to generate VSENSE voltage as close to the device pin as possible in order to reduce noise pickup.
- The RT and COMP pins are sensitive to noise as well, so components around these pins should be located as close as possible to the IC and routed with minimal lengths of trace.
- Make all of the power (high current) traces as short, direct, and thick as possible.
- It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

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10.2 Layout Example

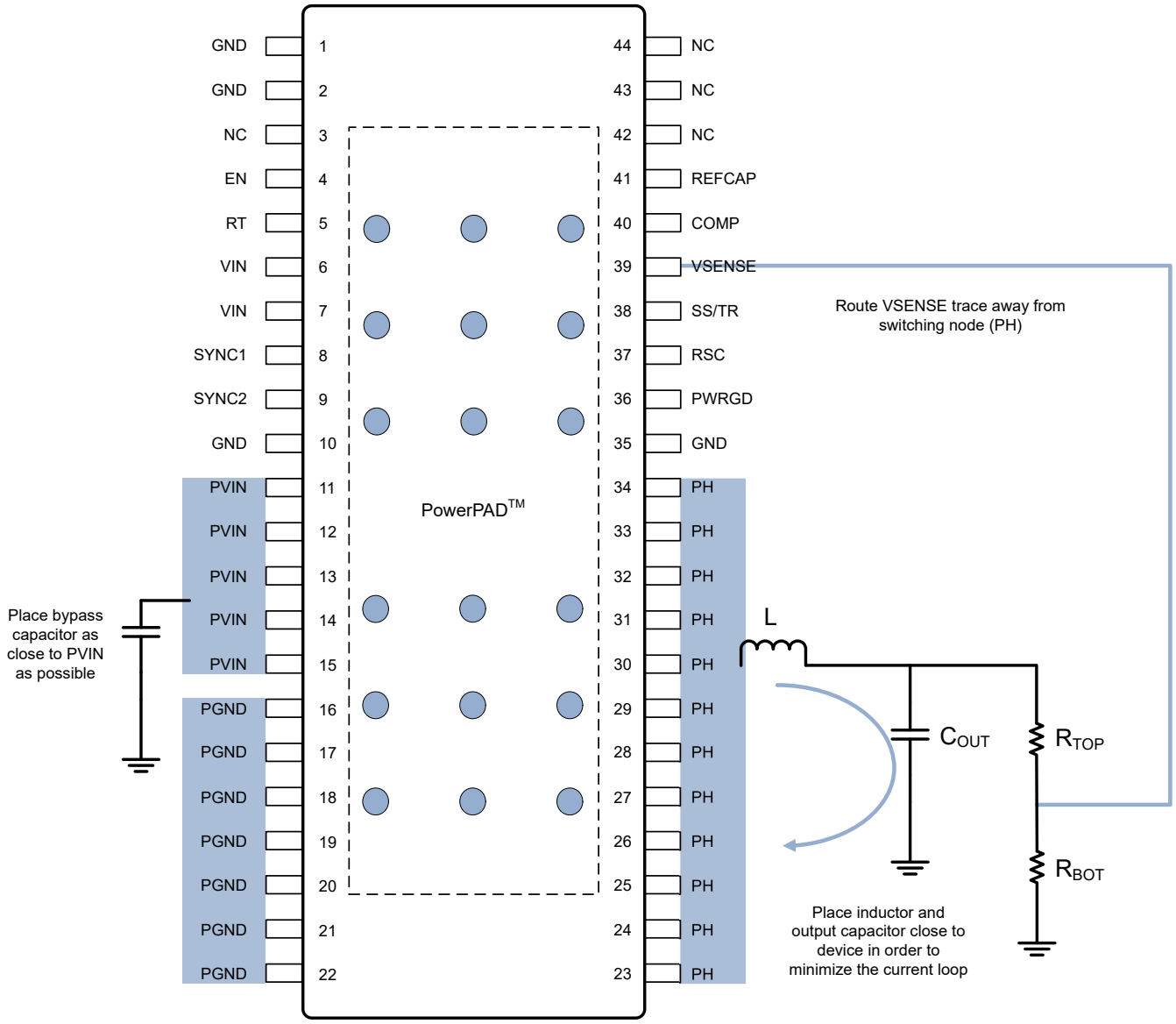


図 10-1. PCB Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H4003EVM Evaluation Module (EVM)* user's guide
- Texas Instruments, *TPS7H4003-SEP Single-Events Effect (SEE)* radiation report
- Texas Instruments, *TPS7H4003-SEP Total-Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H4003-SEP Neutron-Displacement Damage (NDD) Characterization* radiation report
- Texas Instruments, *TPS7H4003-SEP Production Flow and Reliability* reliability report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7H4003MDDWSEP	Active	Production	HTSSOP (DDW) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H4003
TPS7H4003MDDWTSEP	Active	Production	HTSSOP (DDW) | 44	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H4003
V62/21609-01XE	Active	Production	HTSSOP (DDW) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7H4003MDDWSEP	7H4003
V62/21609-01XE-T	Active	Production	HTSSOP (DDW) | 44	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7H4003MDDWTSEP	7H4003

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

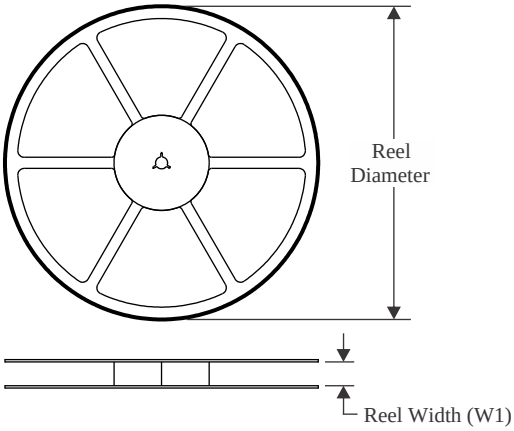
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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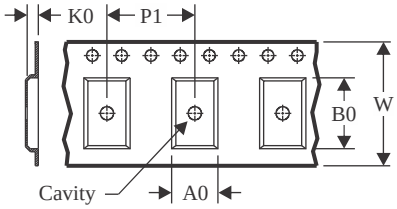
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

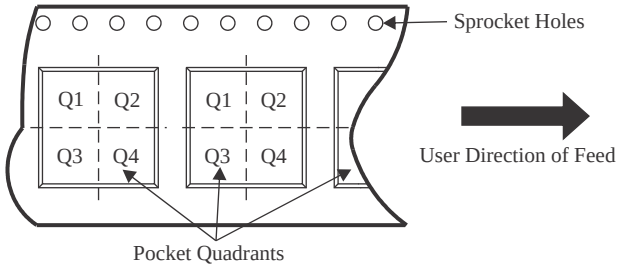


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

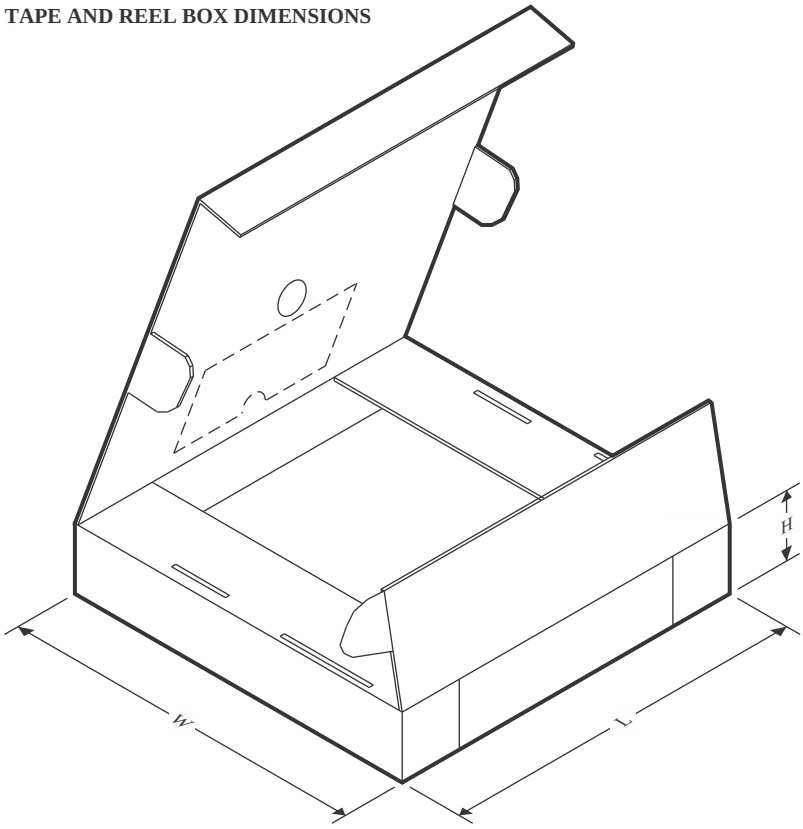
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H4003MDDWTSEP	HTSSOP	DDW	44	250	180.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

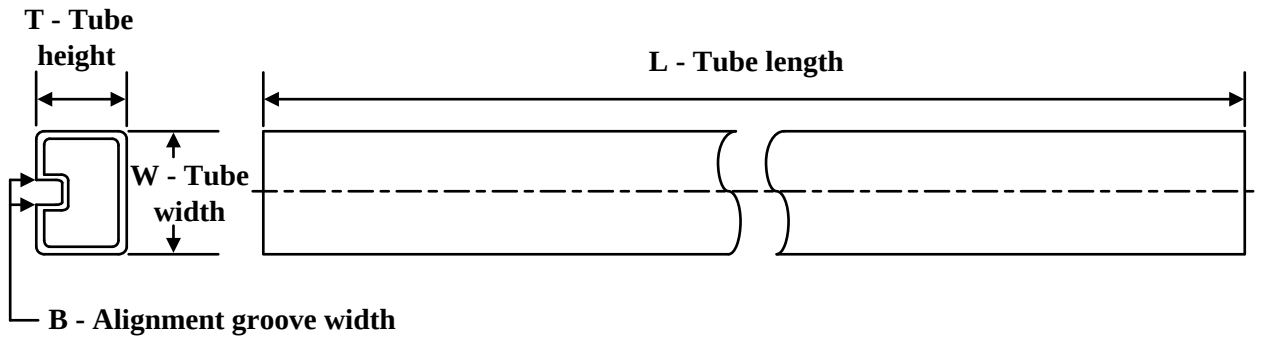
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H4003MDDWTSEP	HTSSOP	DDW	44	250	213.0	191.0	55.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7H4003MDDWSEP	DDW	HTSSOP	44	35	530	11.89	3600	4.9
V62/21609-01XE	DDW	HTSSOP	44	35	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

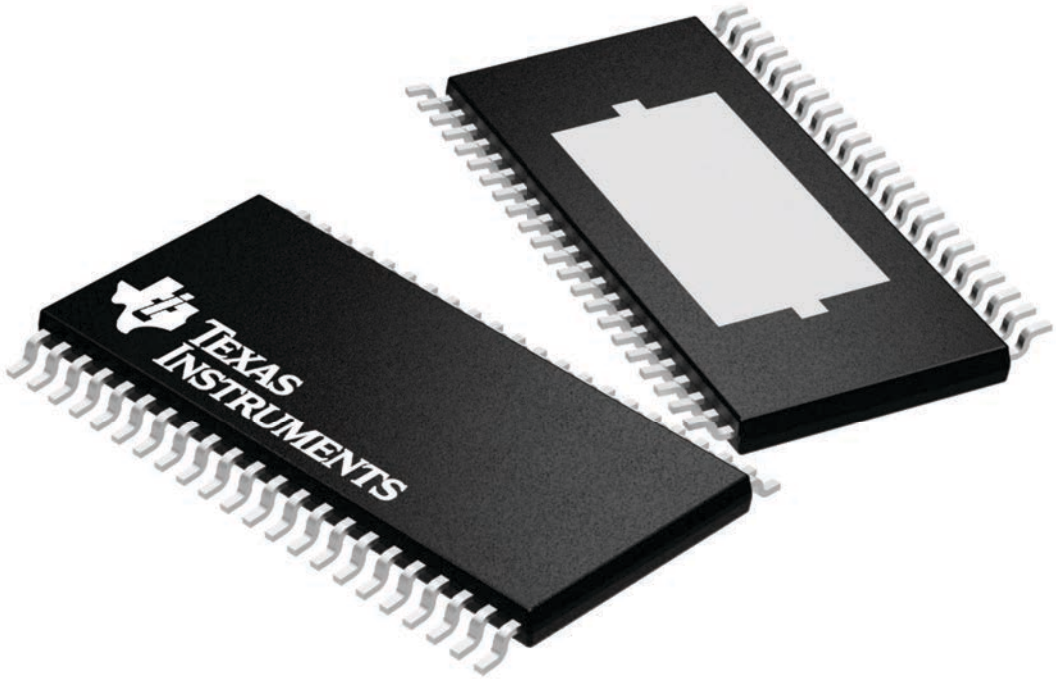
DDW 44

PowerPAD TSSOP - 1.2 mm max height

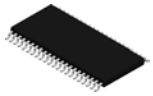
6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224876/A

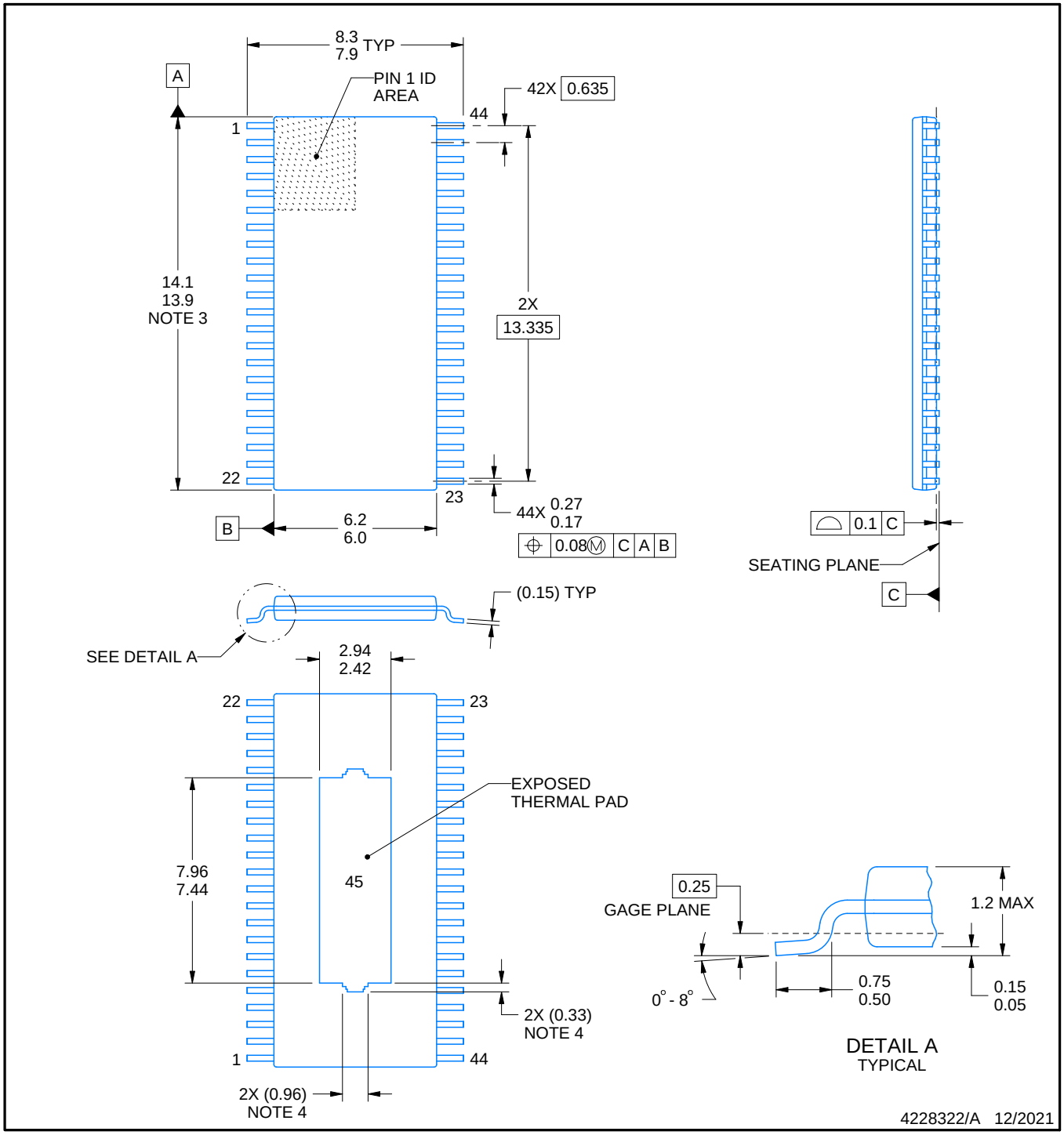


PACKAGE OUTLINE

DDW0044F

PowerPAD™ TSSOP - 1.2 mm max height

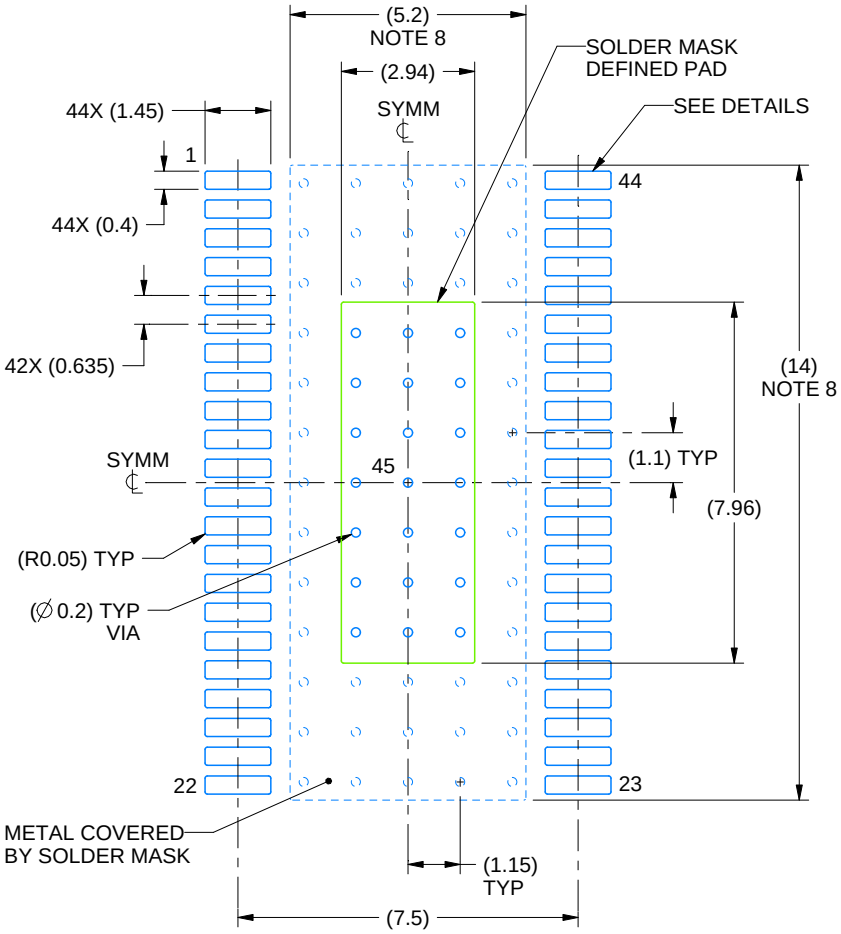
PLASTIC SMALL OUTLINE



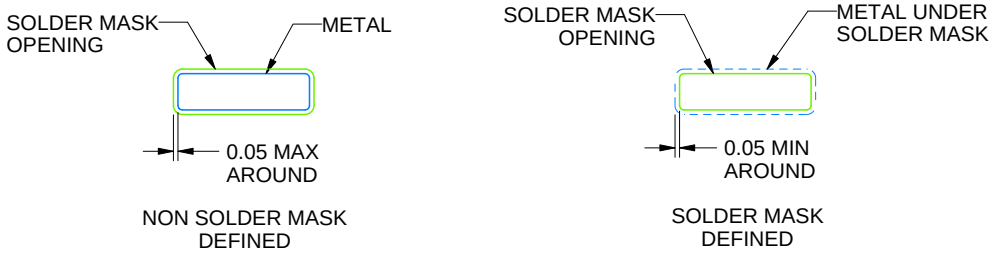
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

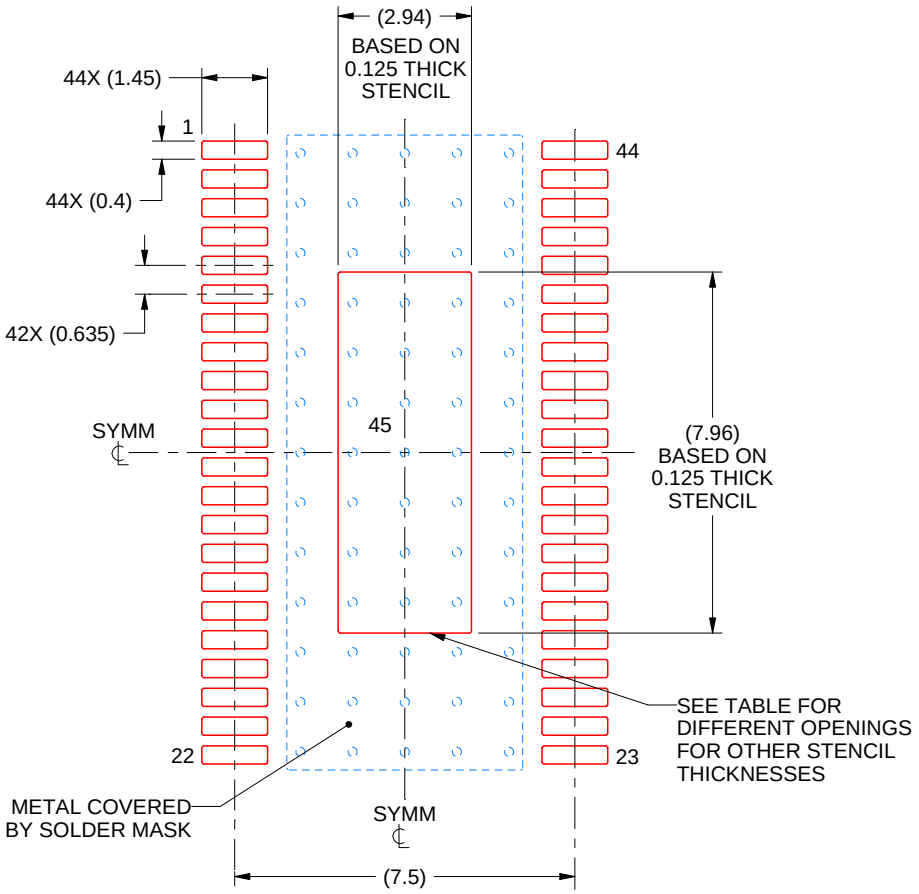


SOLDER MASK DETAILS
NOT TO SCALE

4228322/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.29 X 8.90
0.125	2.94 X 7.96 (SHOWN)
0.15	2.68 X 7.27
0.175	2.48 X 6.73

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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