TPS82130
JAJSGH9F – FEBRUARY 2016 – REVISED JANUARY 2023

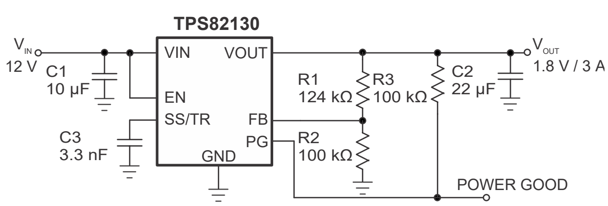
TPS82130 インダクタ統合型 17V 入力、3A 降圧コンバータ MicroSiP™ パワー・モジュール

1 特長

- 3mm × 2.8mm × 1.5mm の MicroSiP パッケージ
- 入力電圧範囲:3V～17V
- 連続出力電流:3A
- DCS-Control トポロジ
- パワーセーブ・モードによる軽負荷時の効率向上
- 動作時の静止電流:20μA
- 可変出力電圧範囲:0.9V～6V
- 100% デューティ・サイクル動作による最小のドロップアウト電圧
- パワー・グッド出力
- ソフト・スタートアップをトラッキング付きでプログラム可能
- サーマル・シャットダウン保護機能
- -40℃～125℃の動作温度範囲
- 中国語のデータシートが利用可能です
- WEBENCH® Power Designer により、TPS82130 を使用するカスタム設計を作成

2 アプリケーション

- 産業用アプリケーション
- テレコムおよびネットワーク・アプリケーション
- ソリッドステート・ドライブ



1.8V 出力のアプリケーションの概略回路図

3 概要

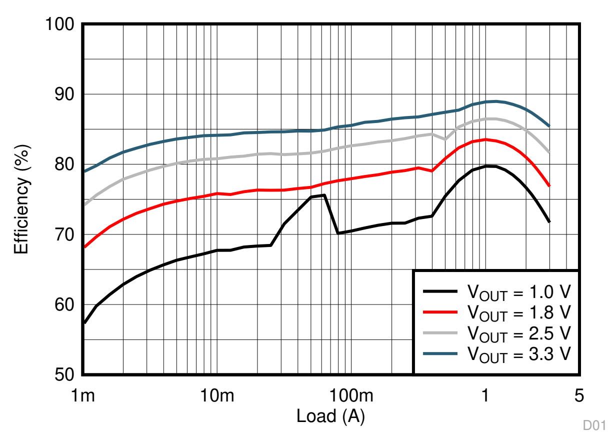
TPS82130 は、小さいソリューション・サイズと高い効率を実現できるように最適化された 17V 入力、3A 降圧コンバータ MicroSiP パワー・モジュールです。このモジュールには同期整流降圧コンバータとインダクタが組み込まれているため、設計の簡素化、外付け部品の低減、PCB 面積の削減が可能です。薄く小型のソリューションなので、標準の表面実装機による自動組み立てに適しています。

最大の効率を実現するため、このコンバータは公称スイッチング周波数
2MHz の PWM モードで動作し、負荷電流が小さいときには自動的にパワーセーブ・モードの動作に移行します。パワーセーブ・モードでは、20μA (標準値) の静止電流で動作します。このデバイスは DCS-Control トポロジを使用して、非常に優れた負荷過渡性能と、出力電圧の正確なレギュレーションを実現しています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS82130	SIL (µSiL、8)	3.00mm × 2.80mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



12V 入力電圧の効率

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2021) to Revision F (January 2023) **Page**

- 中国語に翻訳されたデータシートにハイパーリンクを追加.......... 1
- 商標の情報を更新.......... 1
- Added *Documentation Support* section.......... 18

Changes from Revision D (November 2018) to Revision E (October 2021) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新.......... 1

5 Pin Configuration and Functions

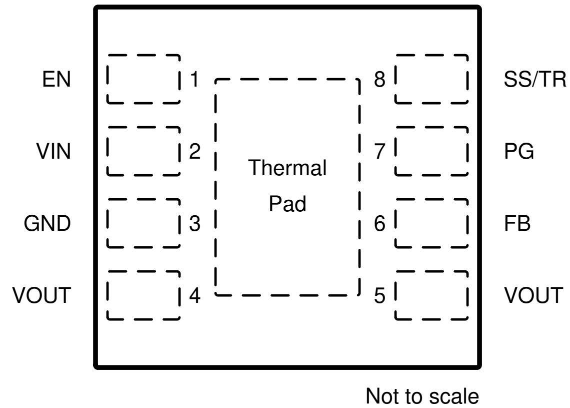


図 5-1. SIL 8-Pin µSiL Package (SIL0008C Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pulldown resistor of typically 400 kΩ when the device is disabled.
VIN	2	PWR	Input pin
GND	3		Ground pin
VOUT	4, 5	PWR	Output pin
FB	6	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
PG	7	O	Power-good open-drain output pin. A pullup resistor can be connected to any voltage less than 6 V. Leave this pin open if it is not used.
SS/TR	8	I	Soft start-up and voltage tracking pin. An external capacitor connected to this pin sets the internal reference voltage rising time.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage at pins(1) (2)	VIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN} + 0.3	
	PG, FB	–0.3	7	
	VOUT	0	7	
Sink current(1)	PG		10	mA
Module operating temperature(1)		–40	125	°C
Storage temperature(1)		–55	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V_{IN}	Input voltage	3	17	V
V_{PG}	Power good pull-up resistor voltage		6	V
V_{OUT}	Output voltage	0.9	6	V
I_{OUT}	Output current	0	3	A
T_J	Module operating temperature range for 100,000 hours lifetime(1)	–40	110	°C

(1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated. For applications where the module operates continuously at 125 °C temperature, the maximum lifetime is reduced to 50,000 hours.

6.4 Thermal Information

THERMAL METRIC(1)		TPS82130 (JEDEC 51-5)	TPS82130EVM-720	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.2	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.4	9.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.2	14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.3	21.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report. Theta-JA can be improved with a custom PCB design containing thermal vias where possible.

6.5 Electrical Characteristics

T_J = –40°C to 125°C and V_{IN} = 3.0 V to 17 V. Typical values are at T_J = 25°C and V_{IN} = 12 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN	No load, device not switching		20	35	µA
I_{SD}	Shutdown current into VIN	EN = Low		1.5	7.4	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	2.6	2.7	2.8	V
		V_{IN} rising	2.8	2.9	3.0	V
T_{JSD}	Thermal shutdown threshold	T_J rising		160		°C
		T_J falling		140		°C
LOGIC INTERFACE (EN)						
V_{IH}	High-level input voltage		0.9	0.65		V
V_{IL}	Low-level input voltage			0.45	0.3	V
$I_{lkg(EN)}$	Input leakage current into the EN pin	EN = High		0.01	1	µA
CONTROL (SS/TR, PG)						
$I_{SS/TR}$	SS/TR pin source current		2.1	2.5	2.8	µA
V_{PG}	Power-good threshold	V_{OUT} rising, referenced to V_{OUT} nominal	92%	95%	99%	
		V_{OUT} falling, referenced to V_{OUT} nominal	87%	90%	94%	
$V_{PG,OL}$	Power-good low-level voltage	I_{sink} = 2 mA		0.1	0.3	V
$I_{lkg(PG)}$	Input leakage current into the PG pin	V_{PG} = 1.8 V		1	400	nA
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode	785	800	815	mV
		PWM mode, T_J = 0°C to 85°C	788	800	812	mV
		PSM, C_{OUT} = 22 µF	785	800	823	mV
		PSM, C_{OUT} = 2 × 22 µF, T_J = 0°C to 85°C	788	800	815	mV
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.8 V		1	100	nA
	Line regulation	I_{OUT} = 1 A, V_{OUT} = 1.8 V		0.002		%/V
	Load regulation	I_{OUT} = 0.5 A to 3 A, V_{OUT} = 1.8 V		0.12		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500 mA, V_{IN} ≥ 6 V		90	170	mΩ
		I_{SW} = 500 mA, V_{IN} = 3 V		120		mΩ
	Low-side FET on-resistance	I_{SW} = 500 mA, V_{IN} ≥ 6 V		40	70	mΩ
		I_{SW} = 500 mA, V_{IN} = 3 V		50		mΩ
R_{DP}	Dropout resistance	100% mode, V_{IN} ≥ 6 V		125		mΩ
		100% mode, V_{IN} = 3 V		160		mΩ
I_{LIMF}	High-side FET switch current limit	V_{IN} = 6 V, T_A = 25°C	3.6	4.2	4.9	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.0		MHz

6.6 Typical Characteristics

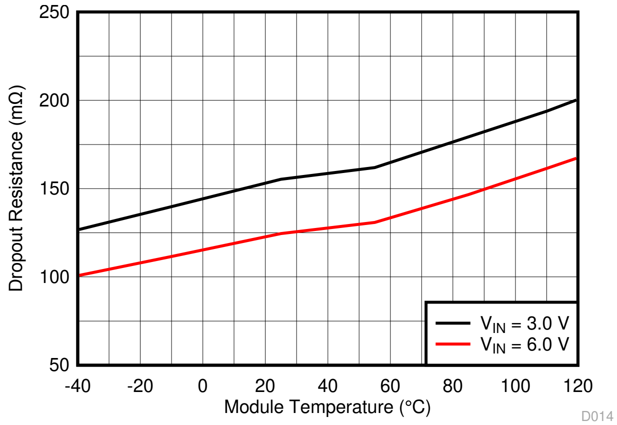


図 6-1. Dropout Resistance

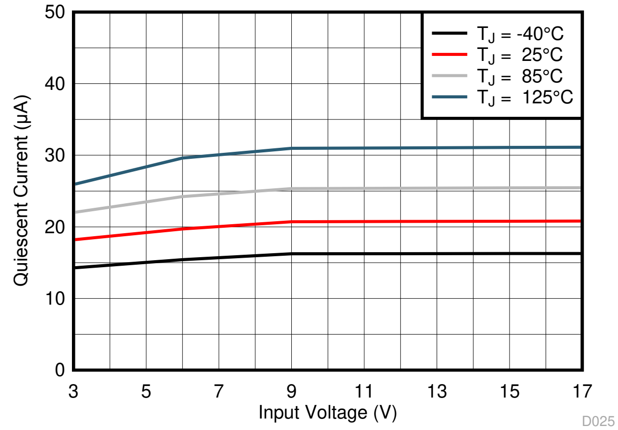


図 6-2. Quiescent Current

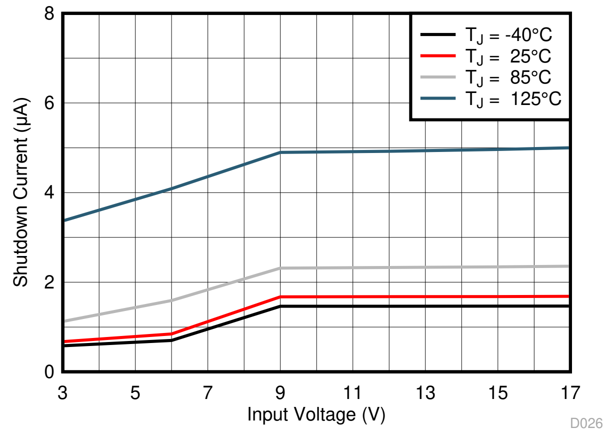


図 6-3. Shutdown Current

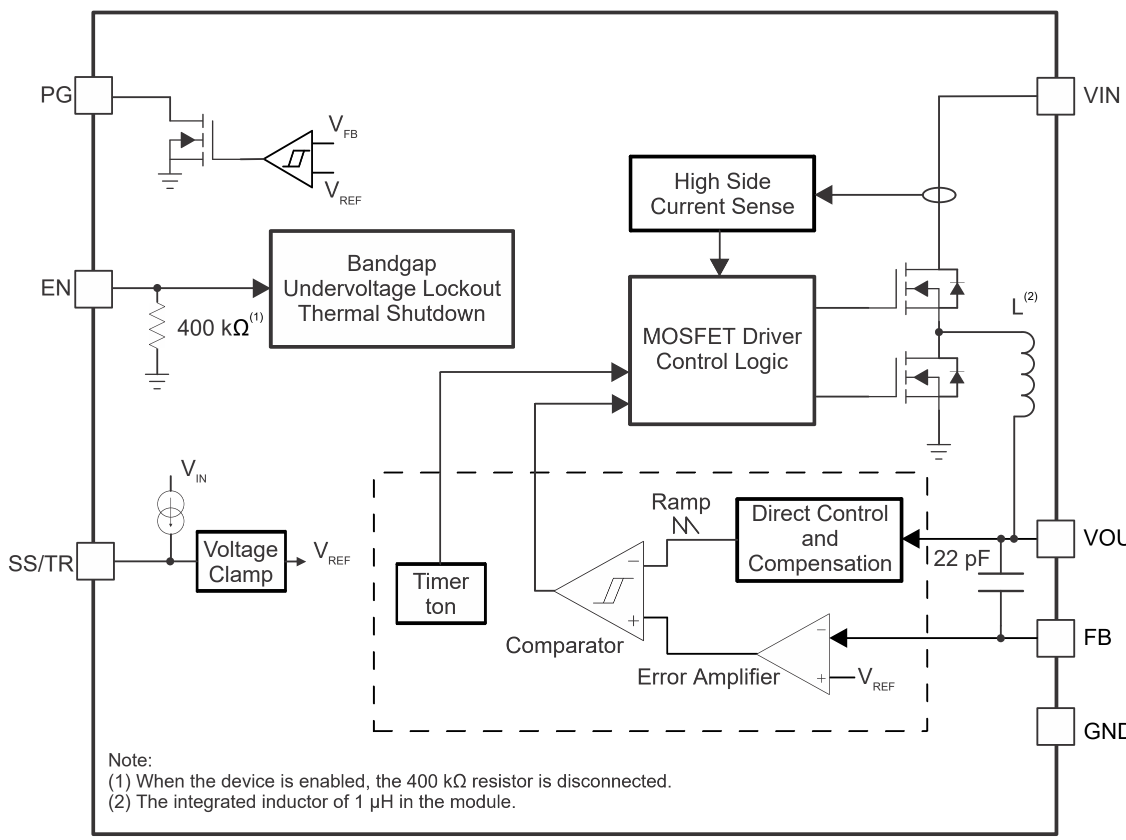
7 Detailed Description

7.1 Overview

The TPS82130 synchronous step-down converter MicroSiP power module is based on DCS-Control (Direct Control with Seamless transition into power save mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in PSM (power save mode) at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.0 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the quiescent current of the IC to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPS82130 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM and PSM Operation

The TPS82130 includes an on-time (t_{ON}) circuitry. t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 500ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

In PWM mode, the TPS82130 operates with pulse width modulation in continuous conduction mode (CCM) with a t_{ON} shown in 式 1 at medium and heavy load currents. A PWM switching frequency of typically 2.0 MHz is achieved by this t_{ON} circuitry. The device operates in PWM mode as long as the output current is higher than half of the ripple current of the inductor estimated by 式 2.

$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \tag{2}$$

To maintain high efficiency at light loads, the device enters power save mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half of the ripple current of the inductor. In PSM, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. PSM is also based on the t_{ON} circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \tag{3}$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in セクション 6.5 and given for a 22-µF output capacitor.

For very small output voltages, an absolute minimum on time of approximately 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also, the off time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases.

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS82130 cannot enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.3.2 Low Dropout Operation (100% Duty Cycle)

The TPS82130 offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \tag{4}$$

where

- R_{DP} = Resistance from V_{IN} to V_{OUT}, including high-side FET on-resistance and DC resistance of the inductor
- $V_{OUT(min)}$ = Minimum output voltage the load can accept

7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit after a propagation delay of typically 30 ns, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current.

7.3.4 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

7.3.5 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. After the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. Accordingly, shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 1.5 µA.

An internal 400-kΩ pulldown resistor is connected to the EN pin when the EN pin is Low. The pulldown resistor is disconnected when the EN pin is High.

7.4.2 Soft Start-Up (SS/TR)

The internal voltage clamp controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output voltage rise time. When the EN pin is pulled high, the device starts switching after a delay of typically 55 µs and the output voltage rises with a slope controlled by an external capacitor connected to the SS/TR pin. Using a very small capacitor or leaving the SS/TR pin floating provides the fastest start-up time.

The TPS82130 is able to start into a pre-biased output capacitor. During the pre-biased start-up, both the power MOSFETs are not allowed to turn on until the internal voltage clamp sets an output voltage above the pre-bias voltage.

When the device is in shutdown, undervoltage lockout, or thermal shutdown, the capacitor connected to the SS/TR pin is discharged by an internal resistor. Returning from those states causes a new start-up sequence.

7.4.3 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 図 7-1.

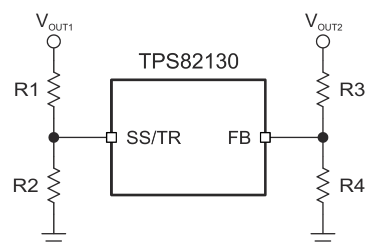


図 7-1. Output Voltage Tracking

When the SS/TR pin voltage is between 50 mV and 1.2 V, the VOUT2 tracks the VOUT1 as described in 式 5.

$$\frac{V_{OUT2}}{V_{OUT1}} \approx 0.64 \times \frac{R2}{R1+R2} \times \frac{R3+R4}{R4} \tag{5}$$

When the SS/TR pin voltage is above 1.2 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. To decrease the SS/TR pin voltage, the device does not sink current from the output, so the resulting decreases of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN + 0.3 V.

Details about tracking and sequencing circuits are found in the *Sequencing and Tracking With the TPS621-Family and TPS821-Family Application Report*.

7.4.4 Power-Good Output (PG)

The device has a power-good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 6 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used. 表 7-1 shows the PG pin logic.

表 7-1. Power Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN = Low)			√
UVLO	$0.7 V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7 V$	√	

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The output voltage of the TPS82130 is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Applications

8.2.1 1.8-V Output Application

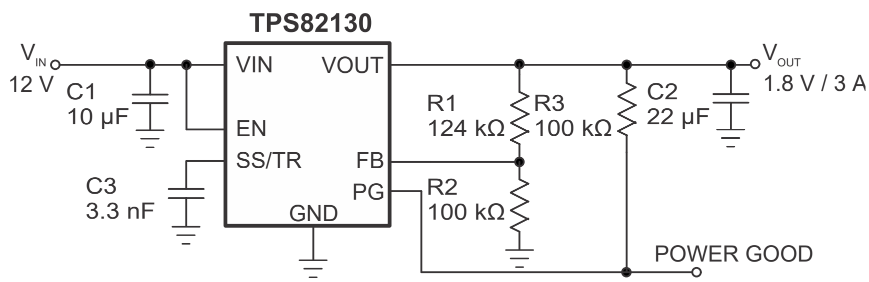


図 8-1. 1.8-V Output Application

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12 V
Output voltage	1.8 V
Output ripple voltage	< 20 mV
Output current rating	3 A

The components used for measurements are given in the following table.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, 25 V, X7R, ±20%, size 1206, C3216X7R1E106M160AE	TDK
C2	22 µF, 10 V, ±20%, X7S, size 0805, C2012X7S1A226M125AC	TDK
C3	3300 pF, 50 V, ±5%, C0G/NP0, size 0603, GRM1885C1H332JA01D	Murata
R1, R2, R3	Standard	

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 式 6:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \tag{6}$$

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. 図 8-1 shows the external resistor divider value for a 1.8-V output. Choose appropriate resistor values for other outputs.

In case the FB pin gets opened, the device clamps the output voltage at the VOUT pin internally to approximately 7 V.

8.2.1.2.3 Input and Output Capacitor Selection

For the best output and input voltage filtering, low-ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. A 10-µF or larger input capacitor is required. The output capacitor value can range from 22 µF up to more than 400 µF. Higher values are possible as well and can be evaluated through the transient response. TI recommends larger soft start times for higher output capacitances.

High capacitance ceramic capacitors have a DC bias effect, which have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.1.2.4 Soft Start-Up Capacitor Selection

A capacitance connected between the SS/TR pin and the GND allows programming the start-up slope of the output voltage. A constant current of 2.5 µA charges the external capacitor. The capacitance required for a given soft start-up time for the output voltage is given by:

$$C_{SS/TR} = t_{SS/TR} \times \frac{I_{SS/TR}}{1.25V} \tag{7}$$

8.2.1.3 Application Performance Curves

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 1.8 V, unless otherwise noted.

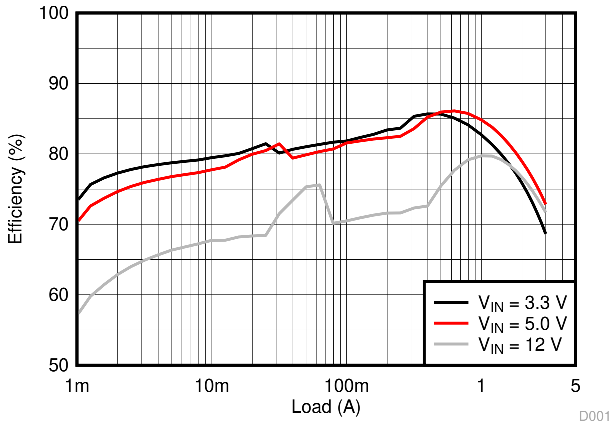


図 8-2. Efficiency, V_{OUT} = 1 V

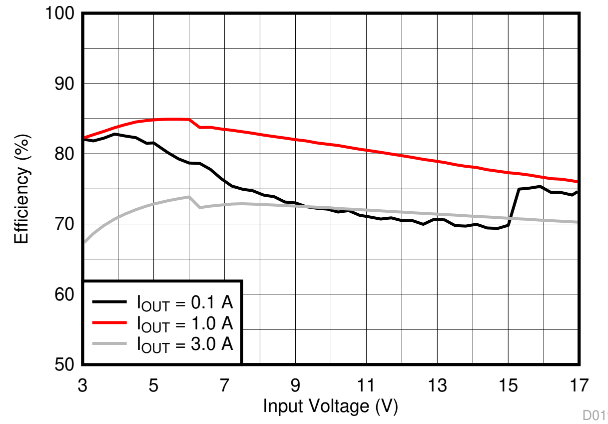


図 8-3. Efficiency, V_{OUT} = 1.0 V

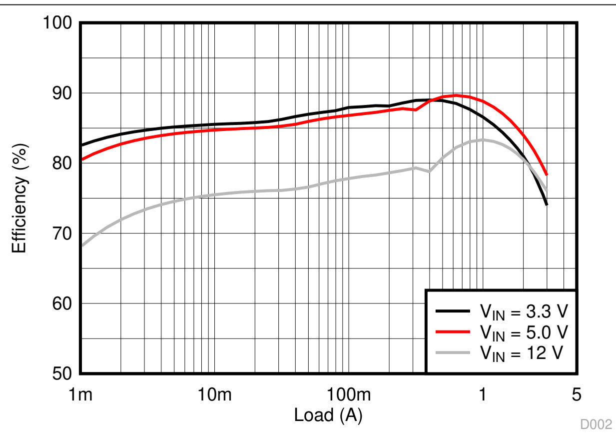


図 8-4. Efficiency, V_{OUT} = 1.8 V

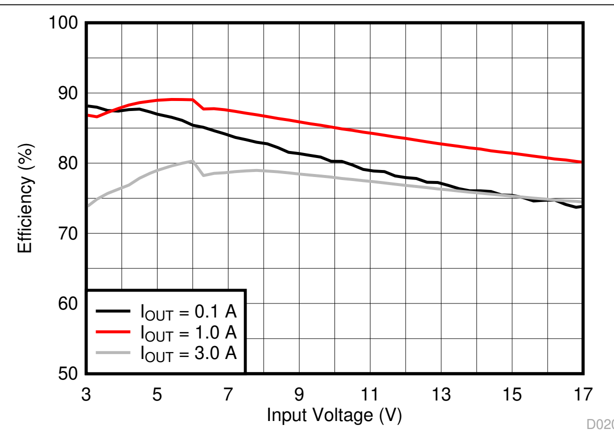


図 8-5. Efficiency, V_{OUT} = 1.8 V

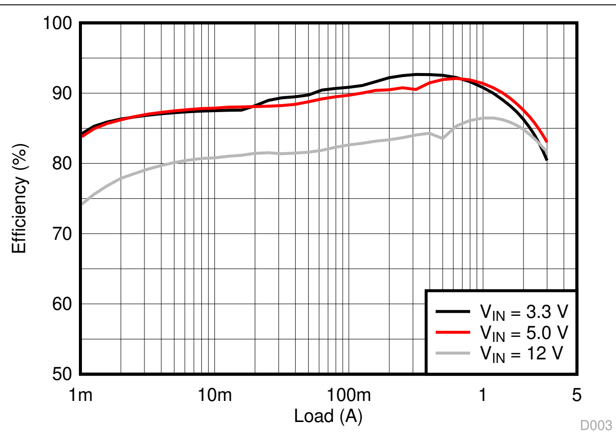


図 8-6. Efficiency, V_{OUT} = 2.5 V

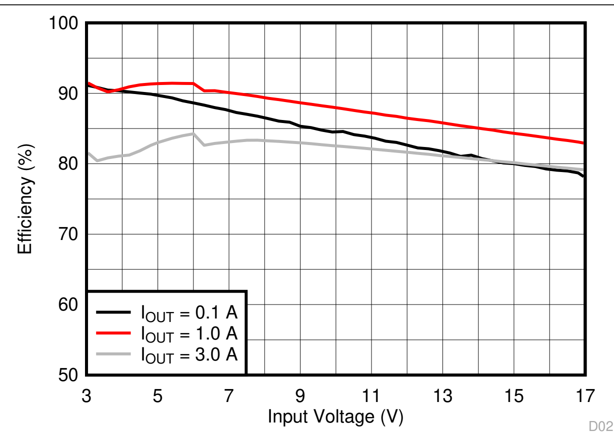


図 8-7. Efficiency, V_{OUT} = 2.5 V

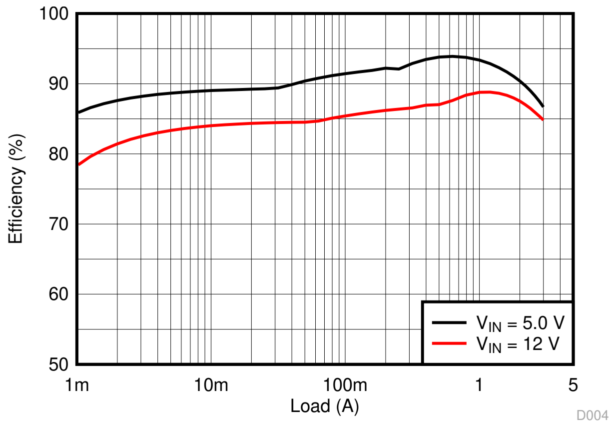


図 8-8. Efficiency, V_{OUT} = 3.3 V

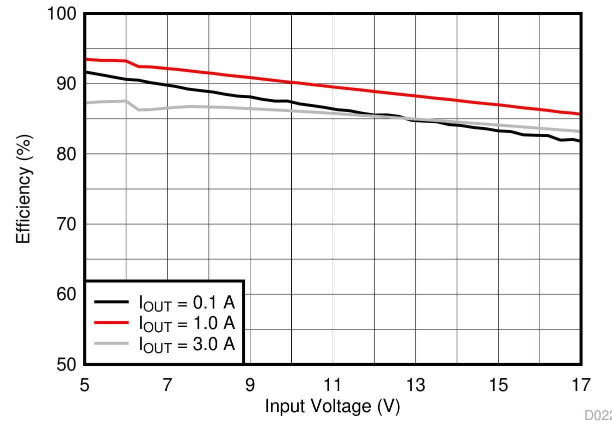


図 8-9. Efficiency, V_{OUT} = 3.3 V

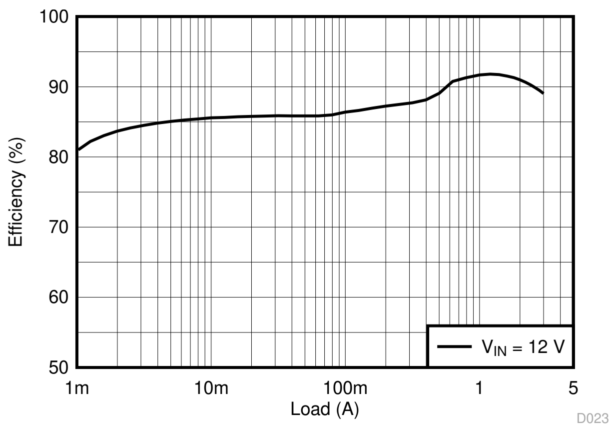


図 8-10. Efficiency, V_{OUT} = 5.0 V

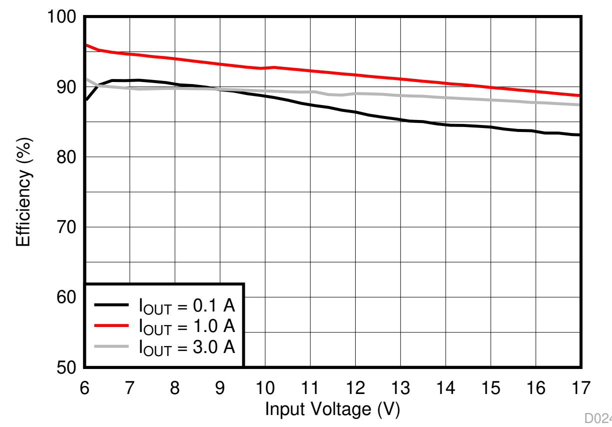
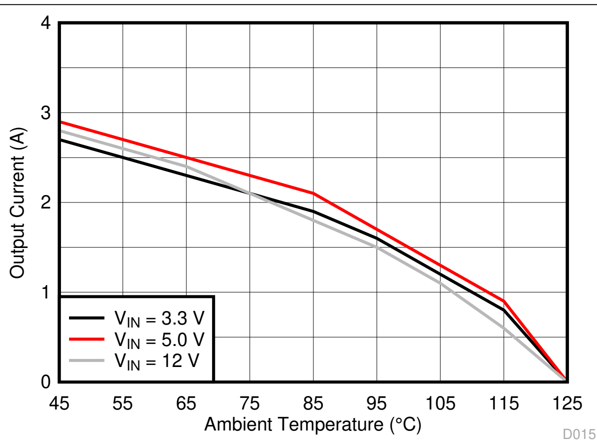
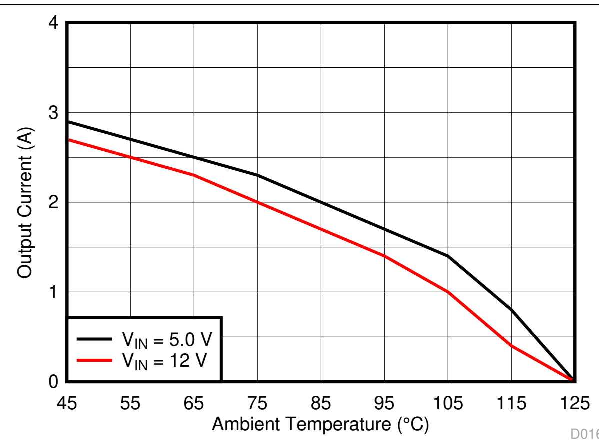


図 8-11. Efficiency, V_{OUT} = 5 V



V_{OUT} = 1.8 V θ_{JA} = 46.1°C/W

図 8-12. Thermal Derating, V_{OUT} = 1.8 V



V_{OUT} = 3.3 V θ_{JA} = 46.1°C/W

図 8-13. Thermal Derating, V_{OUT} = 3.3 V

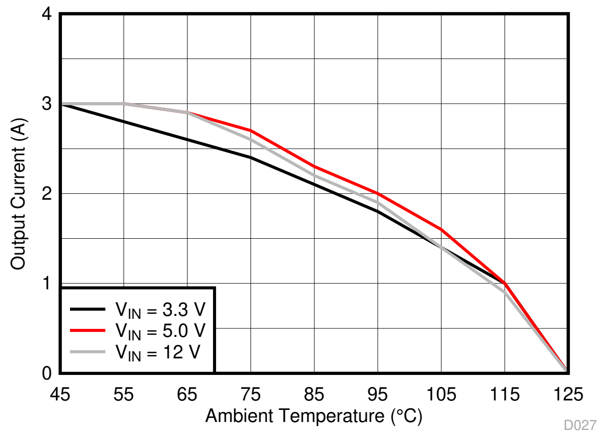
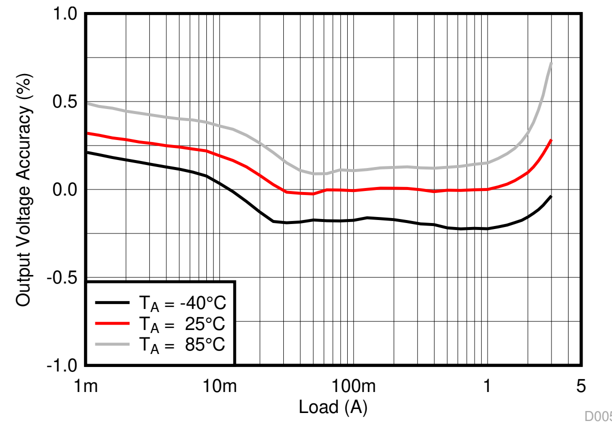
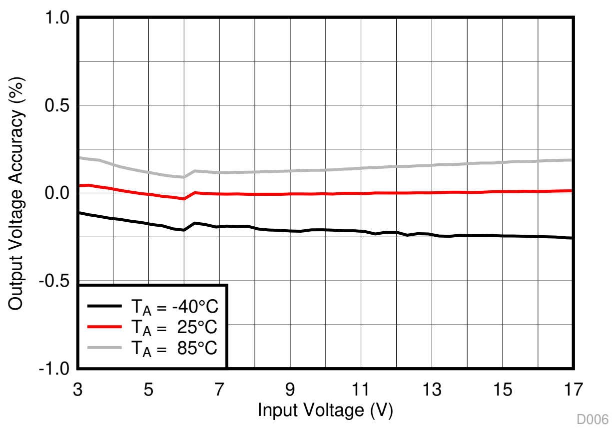


図 8-14. Thermal Derating, V_{OUT} = 1.0 V



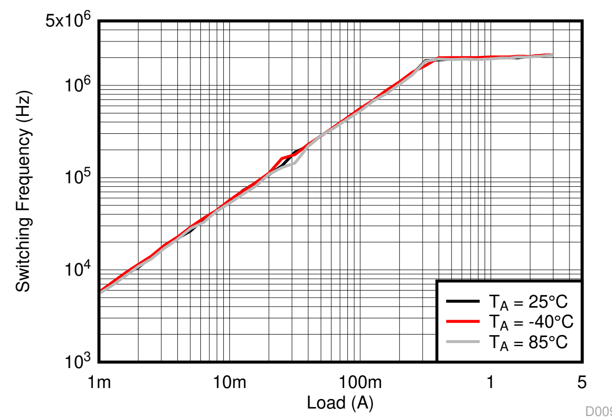
V_{IN} = 12 V

図 8-15. Load Regulation



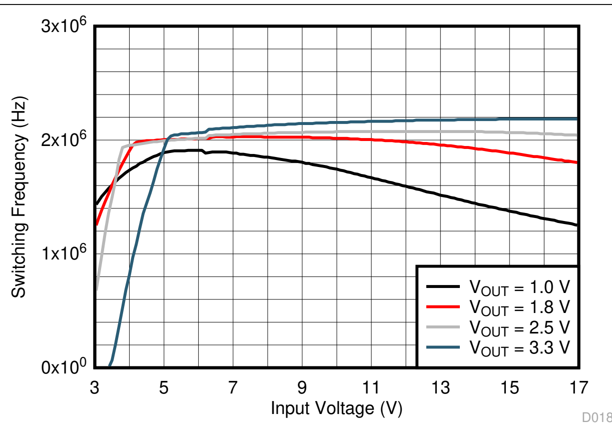
I_{OUT} = 1 A

図 8-16. Line Regulation



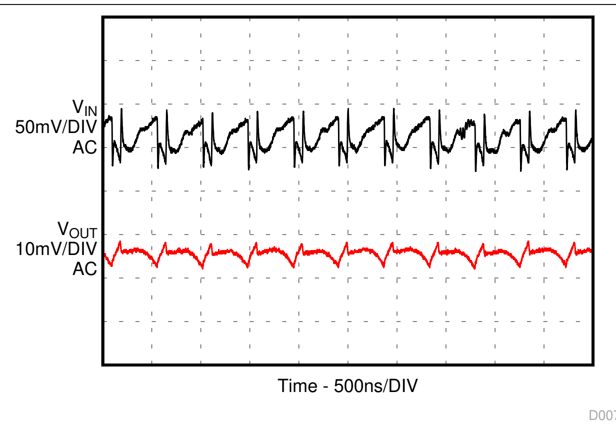
V_{OUT} = 1.8 V　V_{IN} = 12 V

図 8-17. Switching Frequency



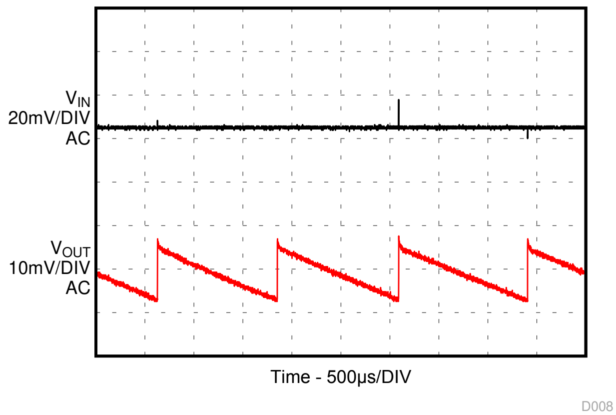
I_{OUT} = 1 A

図 8-18. Switching Frequency



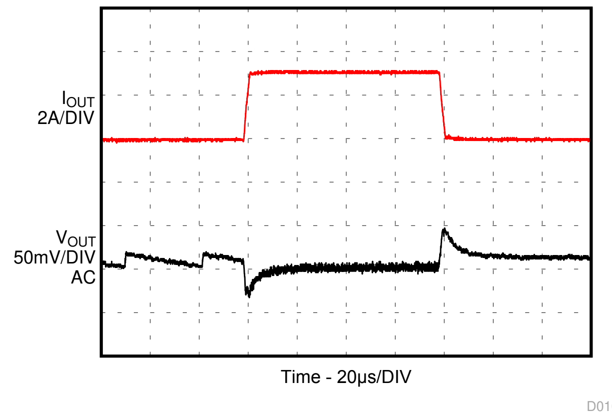
I_{OUT} = 3 A

図 8-19. Input and Output Ripple in PWM Mode



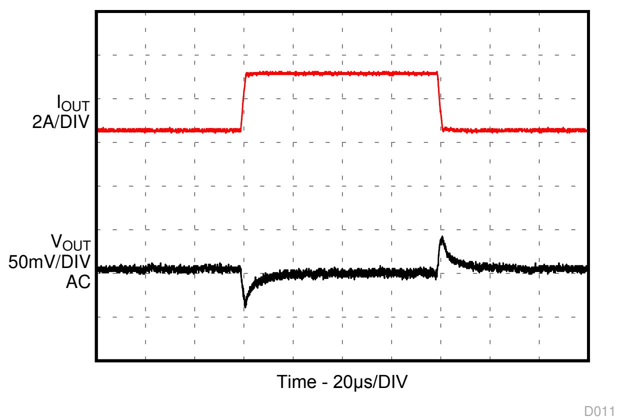
No Load

図 8-20. Input and Output Ripple in PSM Mode



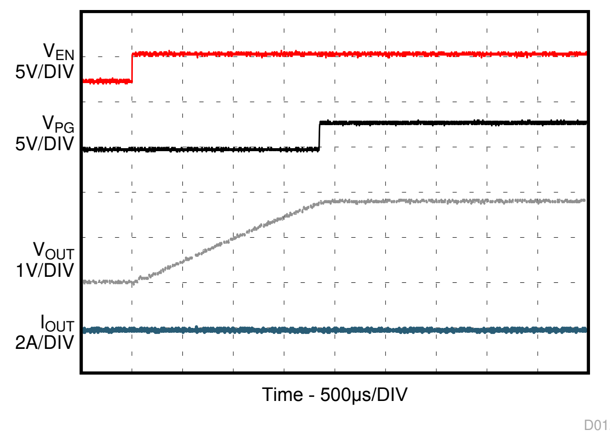
I_{OUT} = 0 A to 3 A, 1 A/µs

図 8-21. Load Transient



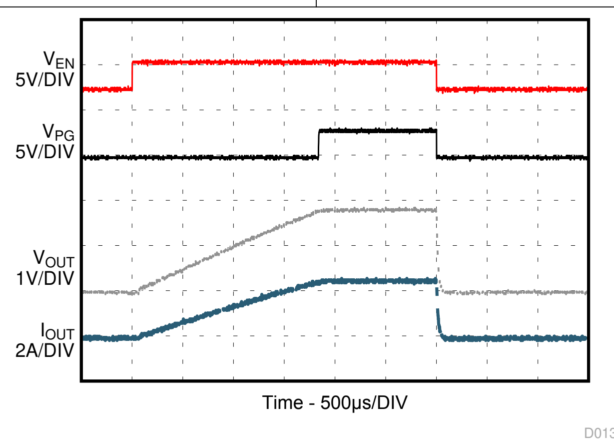
I_{OUT} = 0.5 A to 3 A, 1 A/µs

図 8-22. Load Transient



No Load

図 8-23. Startup without Load



R_{OUT} = 0.68Ω

図 8-24. Startup / Shutdown with Resistance Load

8.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3 V and 17 V. The average input current of the TPS82130 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \tag{8}$$

Ensure that the power supply has a sufficient current rating for the applications.

8.4 Layout

8.4.1 Layout Guidelines

- TI recommends placing all components as close as possible to the IC. The input capacitor placement specifically must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad must be connected to bottom or internal layer ground planes using vias.
- Refer to 図 8-25 for an example of component placement, routing, and thermal design.

8.4.2 Layout Example

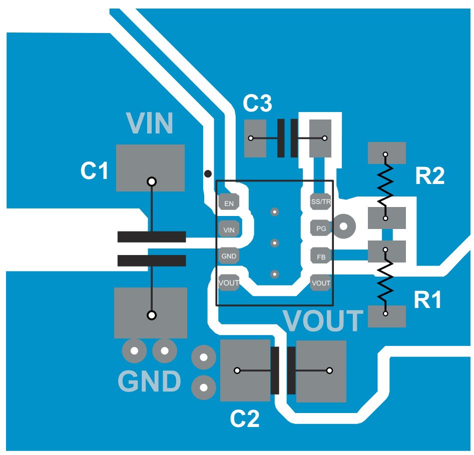


図 8-25. TPS82130 PCB Layout

8.4.3 Thermal Consideration

The output current of the TPS82130 must be derated when the device operates in a high ambient temperature or delivers high output power. The amount of current derating is dependent upon the input voltage, output power, PCB layout design, and environmental thermal condition. Care must especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS82130 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the TPS82130 to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82130, apply the typical efficiency stated in this data sheet to the desired application condition to find the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report* and *Semiconductor and IC Package Thermal Metrics application report*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 サード・パーティ製品に関する免責事項

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9.1.1.2 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report*
- Texas Instruments, *Sequencing and Tracking With the TPS621-Family and TPS821-Family application report*

9.3 ドキュメントの更新通知を受け取る方法

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9.4 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9.7 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10 Mechanical, Packaging, and Orderable Information

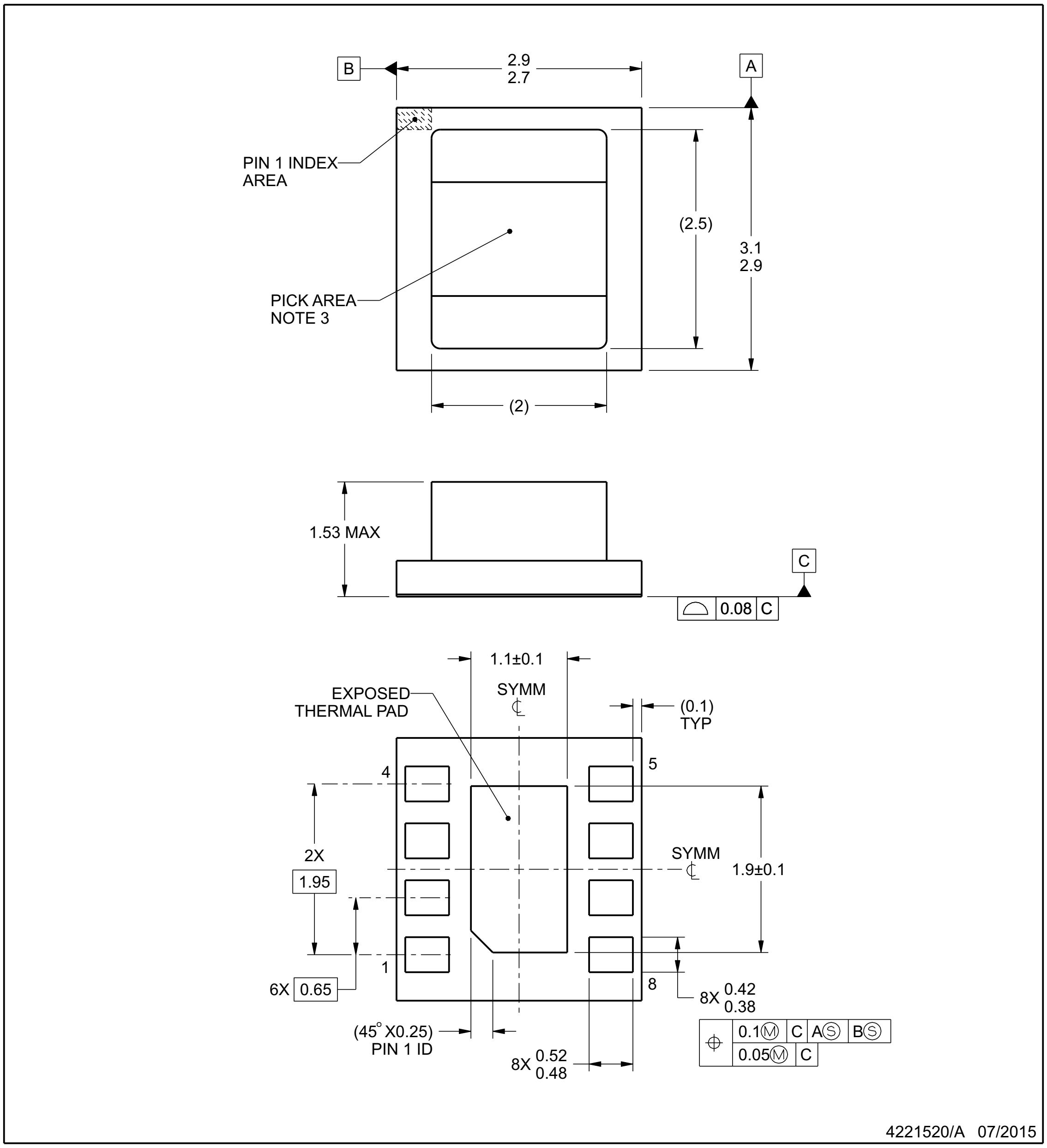
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

SIL0008D

MicroSiP™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

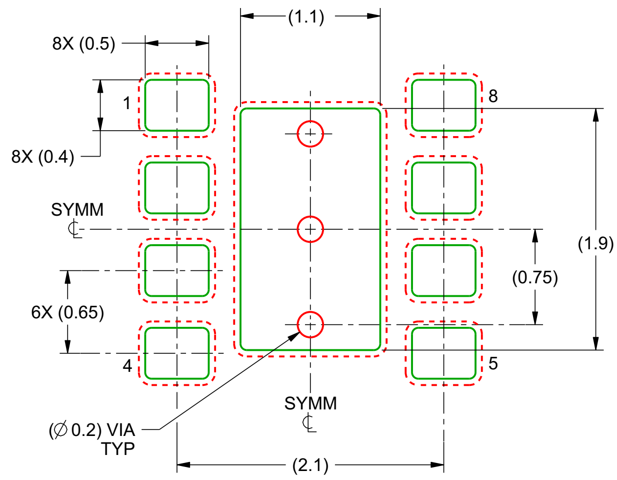
www.ti.com

EXAMPLE BOARD LAYOUT

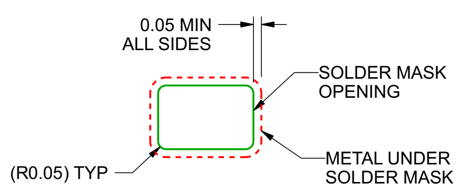
SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X



DETAIL
NOT TO SCALE

4221520/A 07/2015

NOTES: (continued)

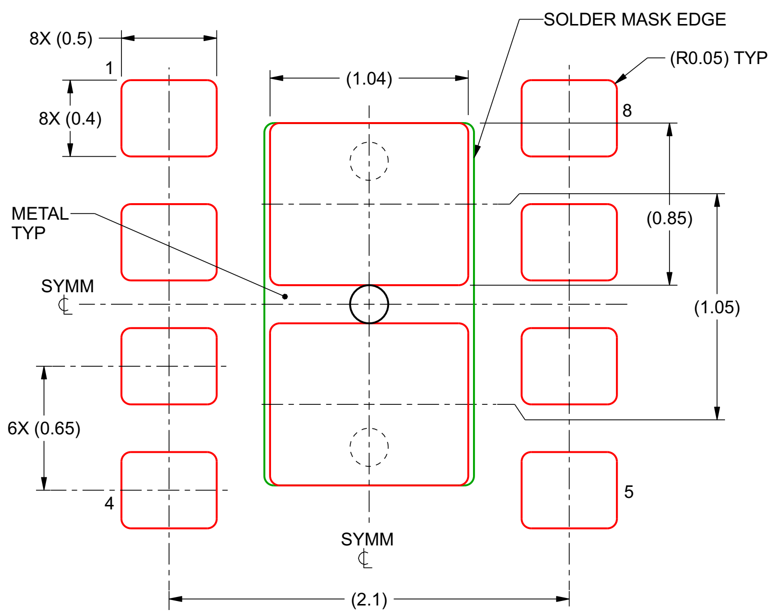
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS82130SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILR.A	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILR.B	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS82130SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILT.A	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILT.B	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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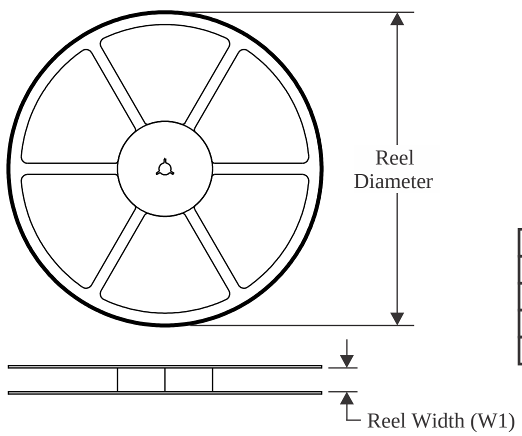
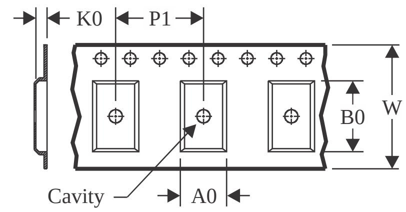
TAPE AND REEL INFORMATION

REEL DIMENSIONS

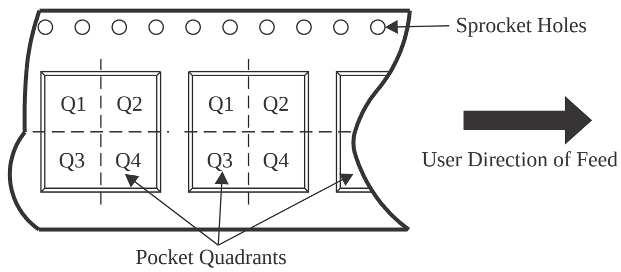


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

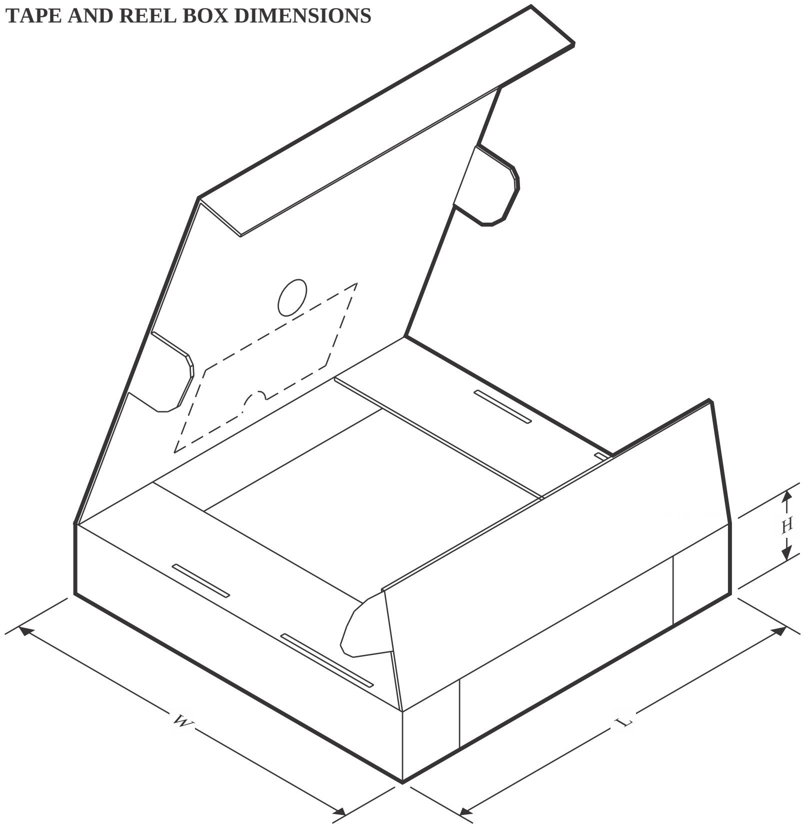
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82130SILR	uSiP	SIL	8	3000	330.0	12.4	3.05	3.25	1.68	8.0	12.0	Q1
TPS82130SILT	uSiP	SIL	8	250	178.0	13.2	3.05	3.25	1.68	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82130SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
TPS82130SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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