TPS82140 17V入力、2A降圧型コンバータ MicroSiP™モジュール、インダクタ搭載

1 特長

- 3.0mm×2.8mm×1.5mmの MicroSiP™パッケージ
- 入力電圧範囲: 3.0V～17V
- 2Aの連続出力電流をサポート
- DCS-Control™トポロジ
- パワーセービング・モードにより軽負荷時の効率を向上
- 動作時の静止電流20µA
- 出力電圧は0.9V～6Vまで可変
- 100%デューティ·サイクル動作により低いドロップアウト電圧を実現
- パワー・グッド出力
- ソフト・スタートアップをトラッキング付きでプログラム可能
- サーマル・シャットダウン保護機能
- TPS82130およびTPS82150とピン互換
- 動作温度範囲: -40℃～125℃
- WEBENCH® Power Designerにより、TPS82140を使用するカスタム設計を作成

2 アプリケーション

- 産業用アプリケーション
- テレコムおよびネットワーク・アプリケーション
- ソリッド・ステート・ドライブ
- 反転電源

3 概要

TPS82140は、17V入力の2A降圧型コンバータMicroSiP™電源モジュールで、小型で高効率のソリューション用に最適化されています。このモジュールには同期整流降圧型コンバータとインダクタが組み込まれているため、設計を簡素化し、外付けコンポーネントを減らして、PCB領域を削減できます。薄く小型のソリューションなので、標準の表面実装機による自動組み立てに適しています。

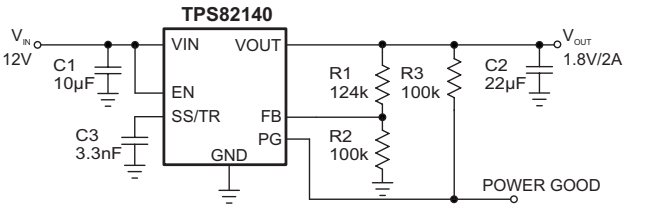
最大の効率を実現するため、このコンバータは公称スイッチング周波数2.0MHzのPWMモードで動作します。また、負荷電流が小さいときには自動的にパワーセービング・モードの動作に移行します。パワーセービング・モードでは、デバイスは標準20µAの静止電流で動作します。このデバイスは、DCS-Control™トポロジを使用して、非常に優れた負荷過渡性能と、出力電圧の正確なレギュレーションを実現しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS82140SIL	µSiL (8)	3.0mm×2.8mm×1.5mm

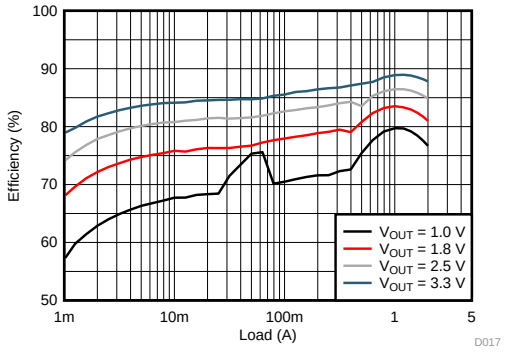
(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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効率と出力電流との関係、V_{IN} = 12V



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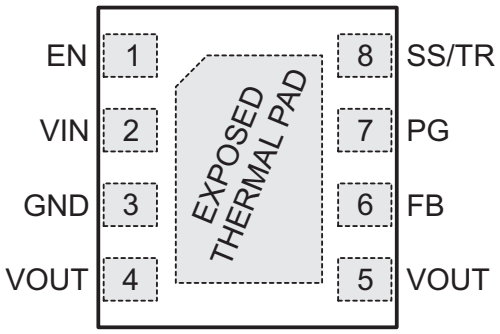
4 改訂履歴

日付	改訂内容	注
2017年6月	*	初版

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5 Pin Configuration and Functions

8-Pin µSiL Package
(SIL0008C Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400kΩ when the device is disabled.
VIN	2	PWR	Input pin.
GND	3		Ground pin.
VOUT	4,5	PWR	Output pin.
FB	6	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
PG	7	O	Power good open drain output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
SS/TR	8	I	Soft startup and voltage tracking pin. An external capacitor connected to this pin sets the internal reference voltage rising time.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at pins(2)	VIN	-0.3	20	V
	EN, SS/TR	-0.3	V_{IN} + 0.3	
	PG, FB	-0.3	7	
	VOUT	0	7	
Sink current	PG		10	mA
Module operating temperature		–40	125	°C
Storage temperature		–55	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	3	17	V
V_{PG}	Power good pull-up resistor voltage		6	V
V_{OUT}	Output voltage	0.9	6	V
I_{OUT}	Output current	0	2	A
T_J	Module operating temperature range for 100,000 hours lifetime(1)	-40	110	°C

(1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated. For applications where the module operates continuously at 125 °C temperature, the maximum lifetime is reduced to 50,000 hours.

6.4 Thermal Information

THERMAL METRIC(1)		TPS82140 8-Pin SIL		UNIT
		JEDEC 51-5	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.2	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.4	9.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.3	21.3	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953. Theta-JA can be improved with a custom PCB design containing thermal vias where possible.

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6.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 3.0V to 17V. Typical values are at T_J = 25°C and V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
I_Q	Quiescent current into VIN	No load, device not switching			20	35	µA
I_{SD}	Shutdown current into VIN	EN = Low			1.5	7.4	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling		2.6	2.7	2.8	V
		V_{IN} rising		2.8	2.9	3.0	V
T_{JSD}	Thermal shutdown threshold	T_J rising			160		°C
		T_J falling			140		°C
LOGIC INTERFACE (EN)							
V_{IH}	High-level input voltage			0.9	0.65		V
V_{IL}	Low-level input voltage				0.45	0.3	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High			0.01	1	µA
CONTROL (SS/TR, PG)							
$I_{SS/TR}$	SS/TR pin source current			2.1	2.5	2.8	µA
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal		92%	95%	99%	
		V_{OUT} falling, referenced to V_{OUT} nominal		87%	90%	94%	
$V_{PG,OL}$	Power good low-level voltage	I_{sink} = 2mA			0.1	0.3	V
$I_{lkg(PG)}$	Input leakage current into PG pin	V_{PG} = 1.8V			1	400	nA
OUTPUT							
V_{FB}	Feedback regulation voltage	PWM mode		785	800	815	mV
			T_J = 0°C to 85°C	788	800	812	
		PSM	C_{OUT} = 22µF	785	800	823	
			C_{OUT} = 2x22µF, T_J = 0°C to 85°C	788	800	815	
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.8V			1	100	nA
	Line regulation	I_{OUT} = 1A, V_{OUT} = 1.8V			0.002		%/V
	Load regulation	I_{OUT} = 0.5A to 2A, V_{OUT} = 1.8V			0.12		%/A
POWER SWITCH							
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500mA, V_{IN} ≥ 6V			90	170	mΩ
		I_{SW} = 500mA, V_{IN} = 3V			120		
	Low-side FET on-resistance	I_{SW} = 500mA, V_{IN} ≥ 6V			40	70	
		I_{SW} = 500mA, V_{IN} = 3V			50		
R_{DP}	Dropout resistance	100% mode, V_{IN} ≥ 6V			125		mΩ
		100% mode, V_{IN} = 3V			160		
I_{LIMF}	High-side FET switch current limit	V_{IN} = 6V, T_J = 25°C		3	3.5	4	A
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 1.8V			2.0		MHz

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6.6 Typical Characteristics

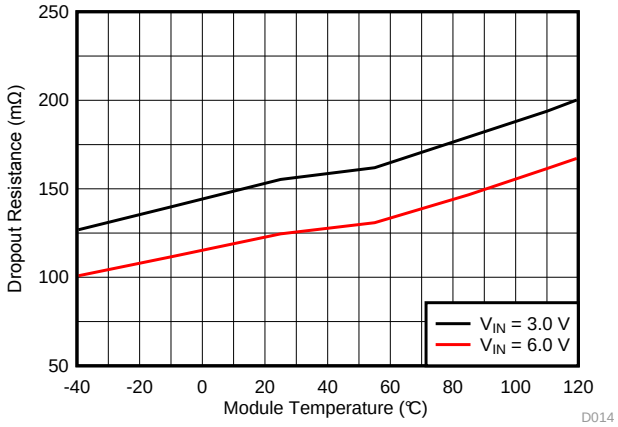


図 1. Dropout Resistance

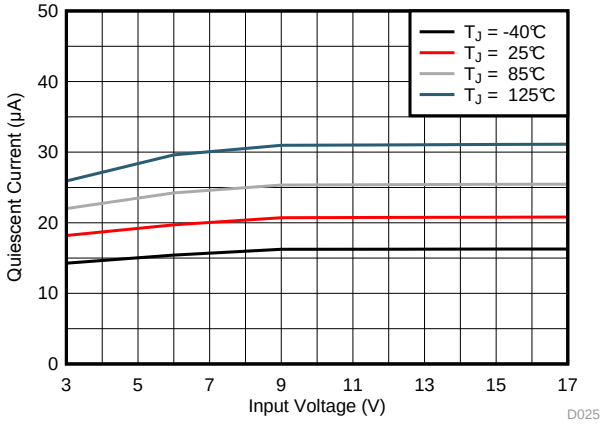


図 2. Quiescent Current

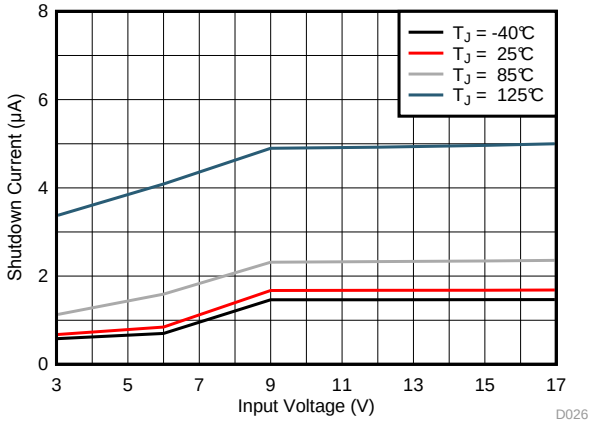


図 3. Shutdown Current

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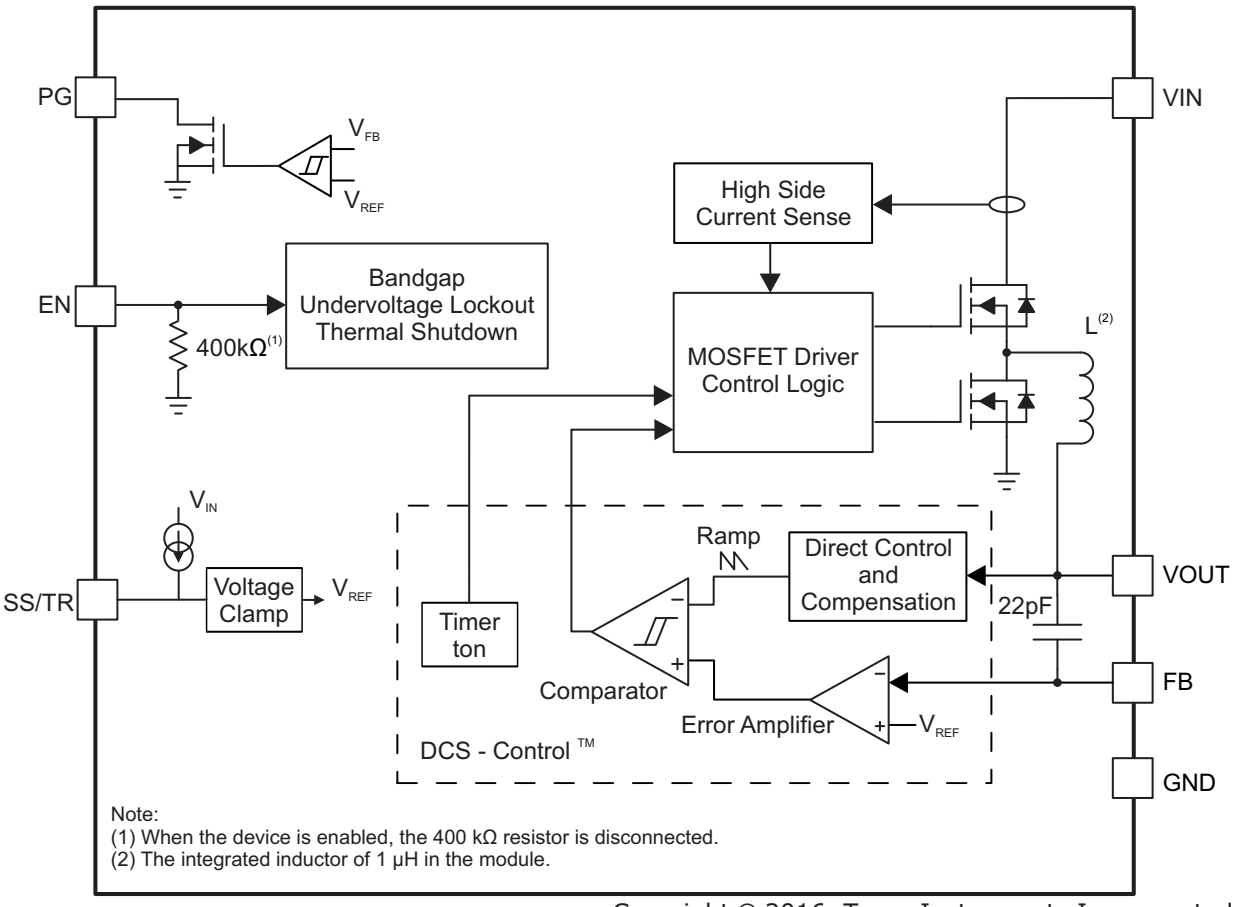
7 Detailed Description

7.1 Overview

The TPS82140 synchronous step-down converter MicroSiP™ power module is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power Save Mode) at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.0MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPS82140 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



Note:
(1) When the device is enabled, the 400 kΩ resistor is disconnected.
(2) The integrated inductor of 1 µH in the module.

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7.3 Feature Description

7.3.1 PWM and PSM Operation

The TPS82140 includes an on-time (t_{ON}) circuitry. This t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 500ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

In PWM mode, the TPS82140 operates with pulse width modulation in continuous conduction mode (CCM) with a t_{ON} shown in 式 1 at medium and heavy load currents. A PWM switching frequency of typically 2.0MHz is achieved by this t_{ON} circuitry. The device operates in PWM mode as long as the output current is higher than half the inductor's ripple current estimated by 式 2.

$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \quad (2)$$

To maintain high efficiency at light loads, the device enters Power Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the inductor's ripple current. In PSM, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. PSM is also based on the t_{ON} circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (3)$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases.

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS82140 can't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

7.3.2 Low Dropout Operation (100% Duty Cycle)

The TPS82140 offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (4)$$

Where

R_{DP} = Resistance from V_{IN} to V_{OUT}, including high-side FET on-resistance and DC resistance of the inductor
$V_{OUT(min)}$ = Minimum output voltage the load can accept.

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Feature Description (continued)

7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit after a propagation delay of typically 30ns, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current.

7.3.4 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 200mV.

7.3.5 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. Accordingly, the shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 1.5 μA.

An internal pull-down resistor of 400kΩ is connected to the EN pin when the EN pin is Low. The pull-down resistor is disconnected when the EN pin is High.

7.4.2 Soft Startup (SS/TR)

The internal voltage clamp controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. When the EN pin is pulled high, the device starts switching after a delay of typically 55μs and the output voltage rises with a slope controlled by an external capacitor connected to the SS/TR pin. Using a very small capacitor or leaving the SS/TR pin floating provides fastest startup time.

The TPS82140 is able to start into a pre-biased output capacitor. During the pre-biased startup, both the power MOSFETs are not allowed to turn on until the internal voltage clamp sets an output voltage above the pre-bias voltage.

When the device is in shutdown, undervoltage lockout or thermal shutdown, the capacitor connected to SS/TR pin is discharged by an internal resistor. Returning from those states causes a new startup sequence.

7.4.3 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 図 4.

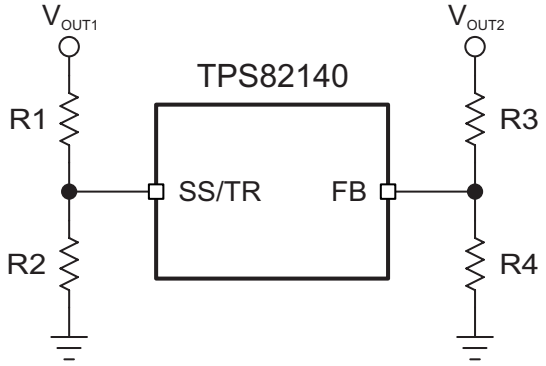


図 4. Output Voltage Tracking

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Device Functional Modes (continued)

When the SS/TR pin voltage is between 50 mV and 1.2 V, the VOUT2 tracks the VOUT1 as described in 式 5.

$$\frac{V_{OUT2}}{V_{OUT1}} \approx 0.64 \times \frac{R2}{R1+R2} \times \frac{R3+R4}{R4} \quad (5)$$

When the SS/TR pin voltage is above 1.2 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So the resulting decreases of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN+0.3V.

Details about tracking and sequencing circuits are found in SLVA470.

7.4.4 Power Good Output (PG)

The device has a power good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 2mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6V.

The PG pin goes low when the device is in shutdown or thermal shutdown. When the device is in UVLO, the PG pin is high impedance. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used. 表 1 shows the PG pin logic.

表 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The output voltage of the TPS82140 is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Applications

8.2.1 1.8-V Output Application

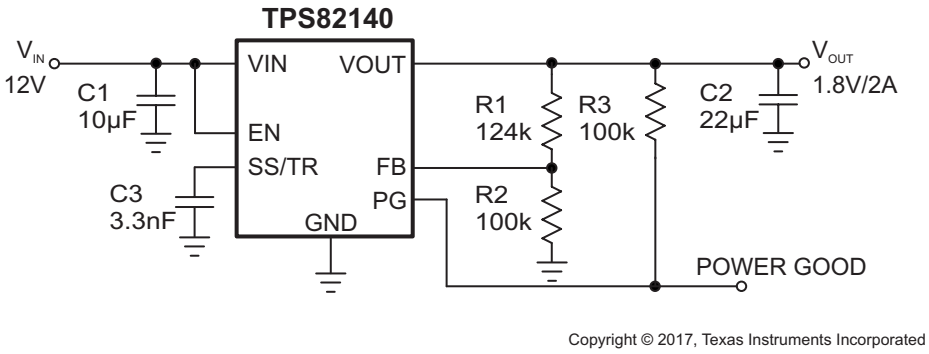


図 5. 1.8-V Output Application

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12V
Output voltage	1.8V
Output ripple voltage	< 20mV
Output current rating	2A

The components used for measurements are given in the following table.

表 3. List of Components

REFERENCE	DESCRIPTION(1)	MANUFACTURER
C1	10 µF, 25 V, X7R, ±20%, size 1206, C3216X7R1E106M160AE	TDK
C2	22 µF, 10 V, X7S, ±20%, size 0805, C2012X7S1A226M125AC	TDK
C3	3300 pF, 50 V, ±5%, C0G/NP0, size 0603, GRM1885C1H332JA01D	Murata
R1, R2, R3	Standard	

(1) SeeThird-party Products Disclaimer

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82140 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance
   – Run thermal simulations to understand the thermal performance of your board
   – Export your customized schematic and layout into popular CAD formats
   – Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (6)$$

R2 should not be higher than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. 図 5 shows the external resistor divider value for a 1.8-V output. Choose appropriate resistor values for other outputs.

In case the FB pin gets opened, the device clamps the output voltage at the VOUT pin internally to about 7V.

8.2.1.2.3 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-µF or larger input capacitor is required. The output capacitor value can range from 22µF up to more than 400µF. Higher values are possible as well and can be evaluated through the transient response. Larger soft start times are recommended for higher output capacitances.

High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.1.2.4 Soft Startup Capacitor Selection

A capacitance connected between the SS/TR pin and the GND allows programming the startup slope of the output voltage. A constant current of 2.5 µA charges the external capacitor. The capacitance required for a given soft startup time for the output voltage is given by:

$$C_{SS/TR} = t_{SS/TR} \times \frac{I_{SS/TR}}{1.25V} \quad (7)$$

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8.2.1.3 Application Performance Curves

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 1.8 V, unless otherwise noted.

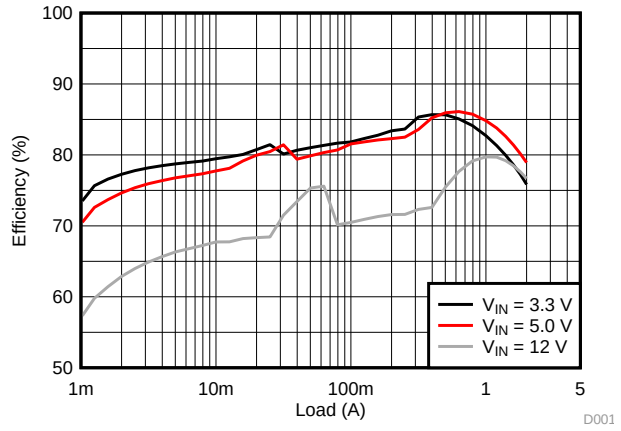


図 6. Efficiency, V_{OUT} = 1.0 V

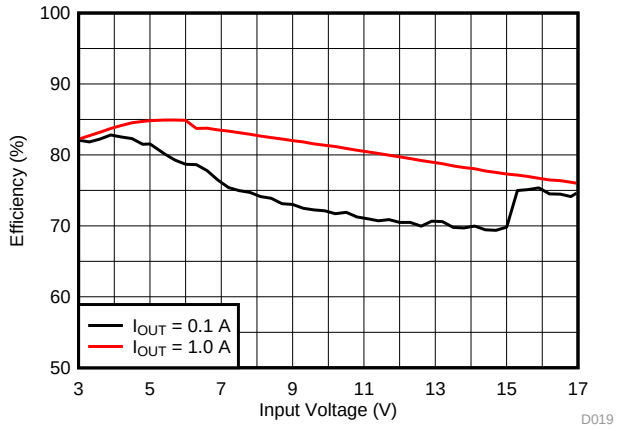


図 7. Efficiency, V_{OUT} = 1.0 V

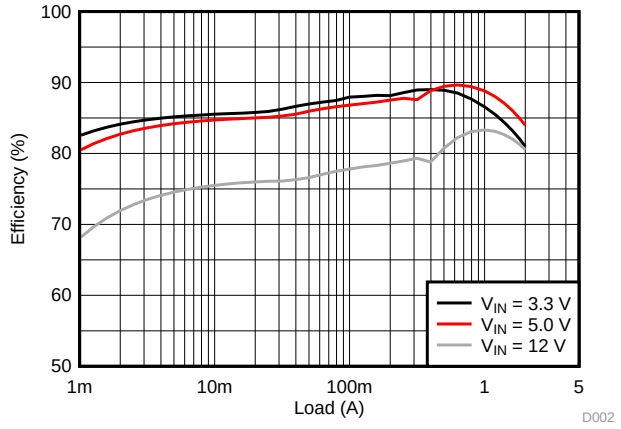


図 8. Efficiency, V_{OUT} = 1.8 V

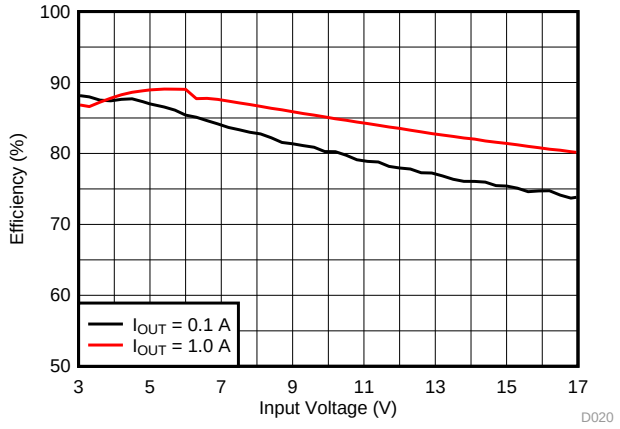


図 9. Efficiency, V_{OUT} = 1.8 V

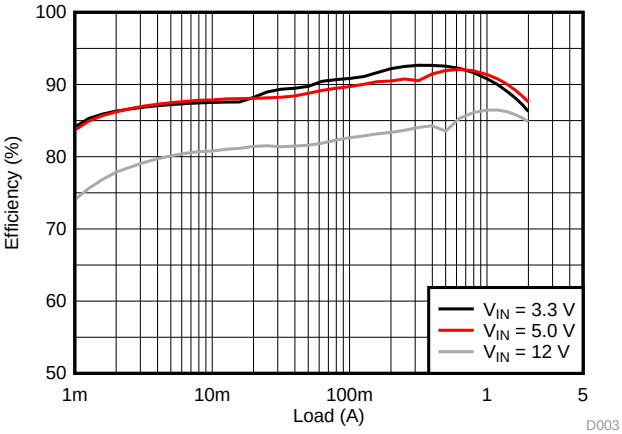


図 10. Efficiency, V_{OUT} = 2.5 V

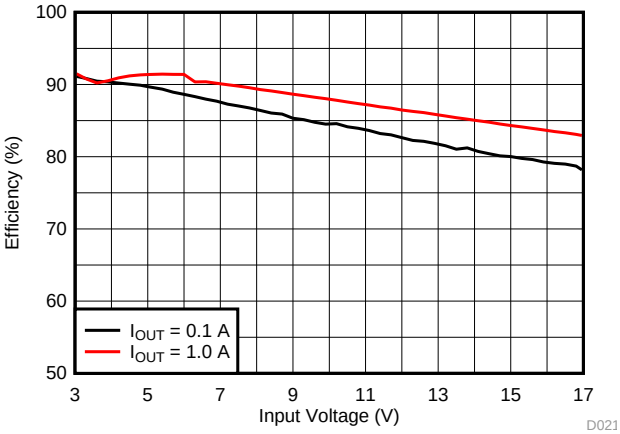


図 11. Efficiency, V_{OUT} = 2.5 V

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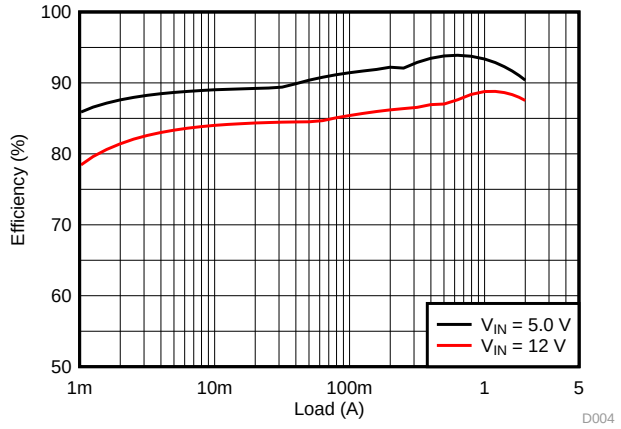


図 12. Efficiency, V_{OUT} = 3.3 V

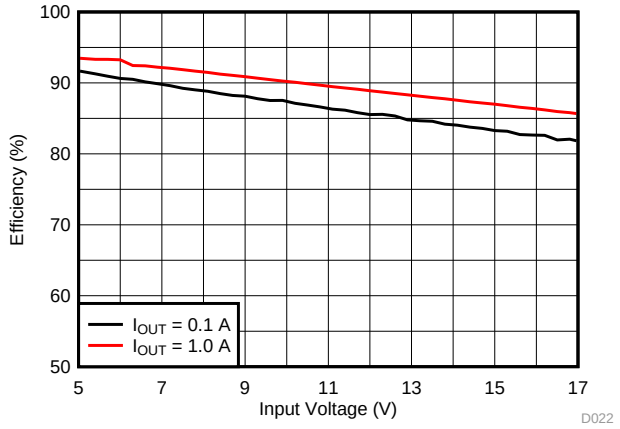


図 13. Efficiency, V_{OUT} = 3.3 V

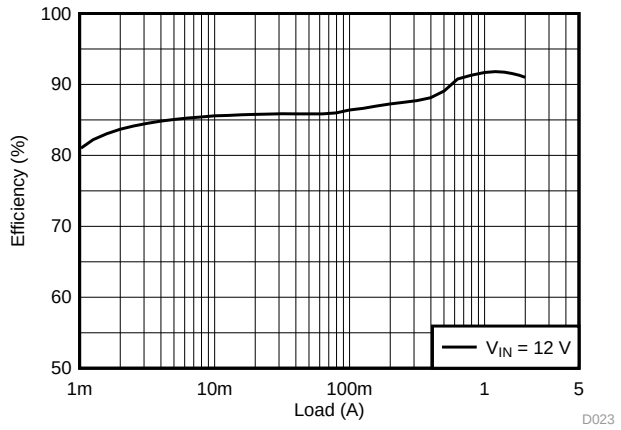


図 14. Efficiency, V_{OUT} = 5.0 V

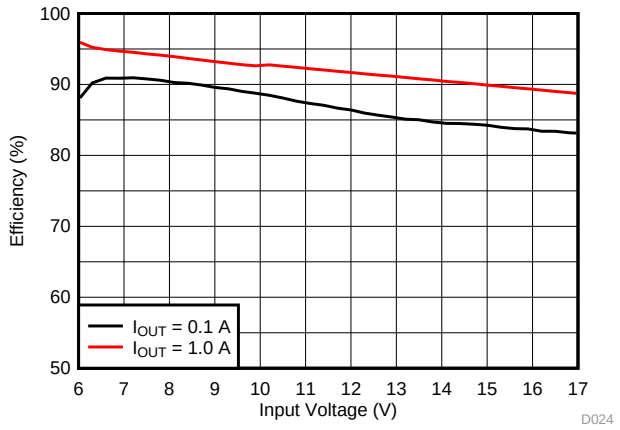
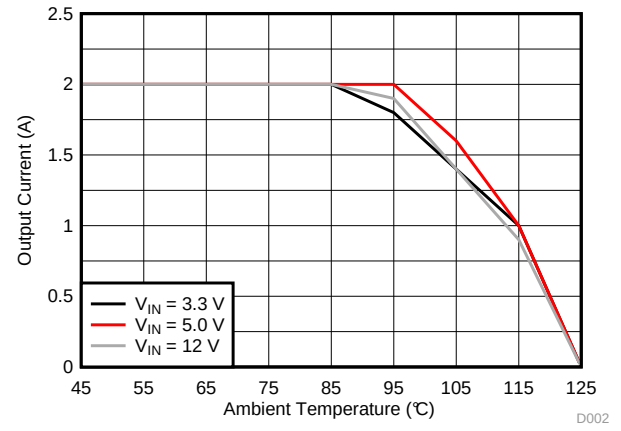
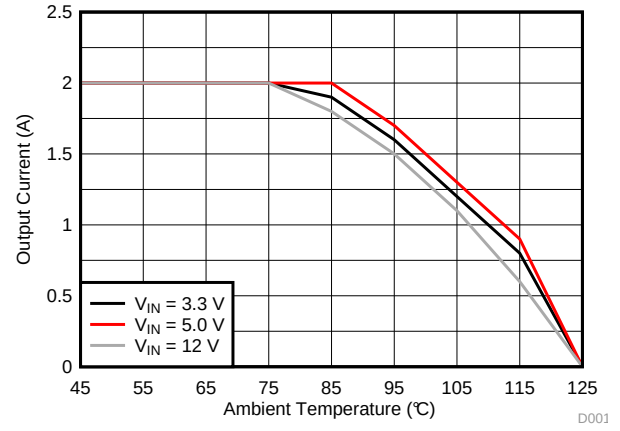


図 15. Efficiency, V_{OUT} = 5.0 V



θ_{JA} = 46.1 °C/W

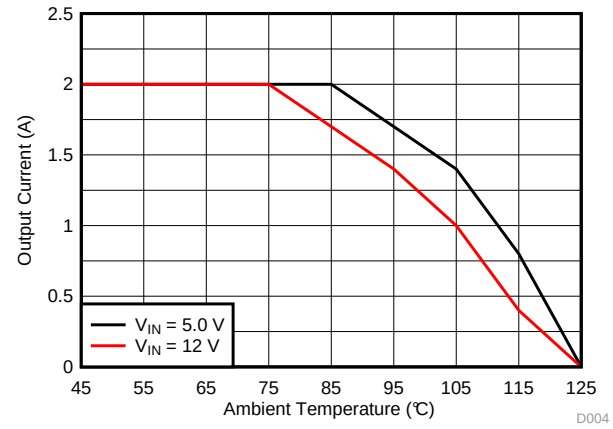
図 16. Thermal Derating, V_{OUT} = 1 V



θ_{JA} = 46.1 °C/W

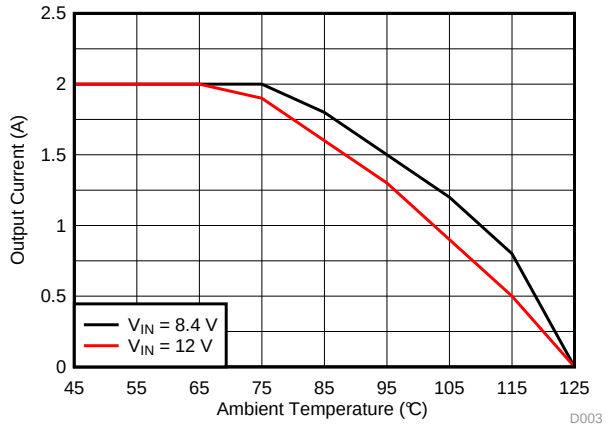
図 17. Thermal Derating, V_{OUT} = 1.8 V

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θ_{JA} = 46.1 °C/W

図 18. Thermal Derating, V_{OUT} = 3.3 V



θ_{JA} = 46.1 °C/W

図 19. Thermal Derating, V_{OUT} = 5 V

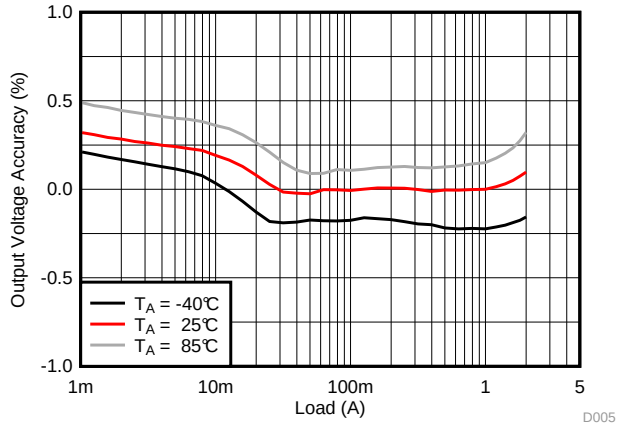
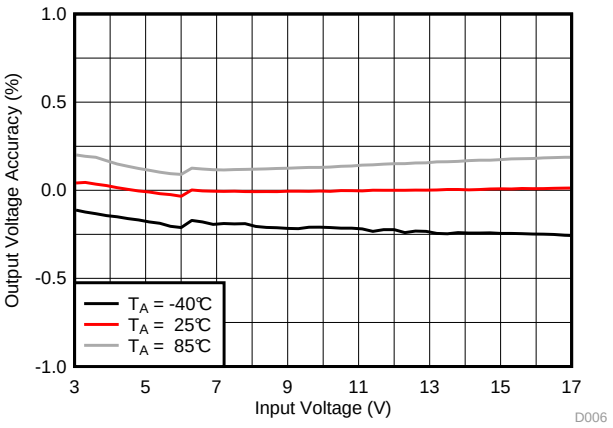
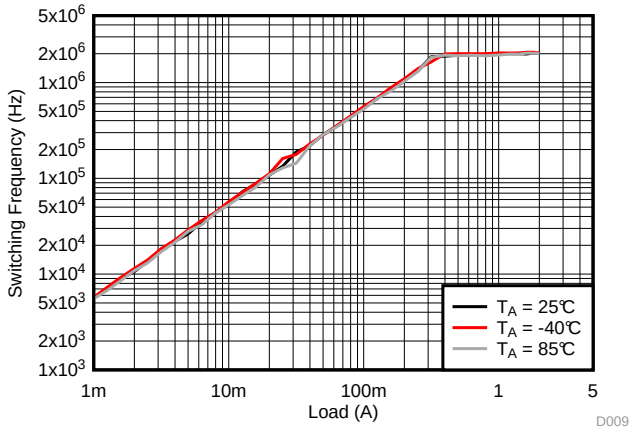


図 20. Load Regulation



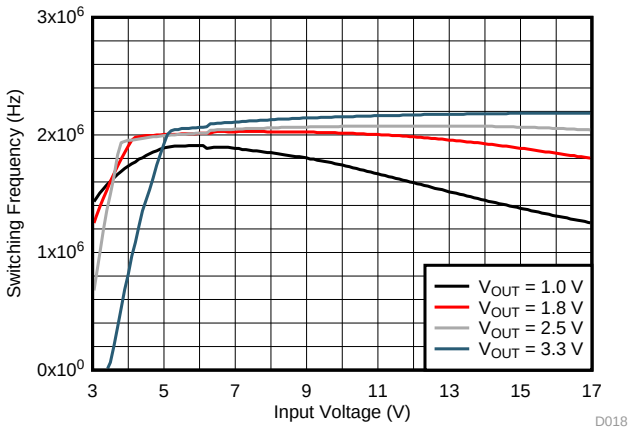
I_{OUT} = 1A

図 21. Line Regulation



V_{OUT} = 1.8V

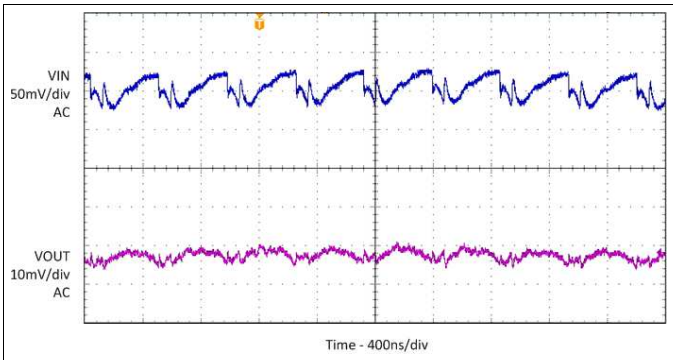
図 22. Switching Frequency



I_{OUT} = 1A

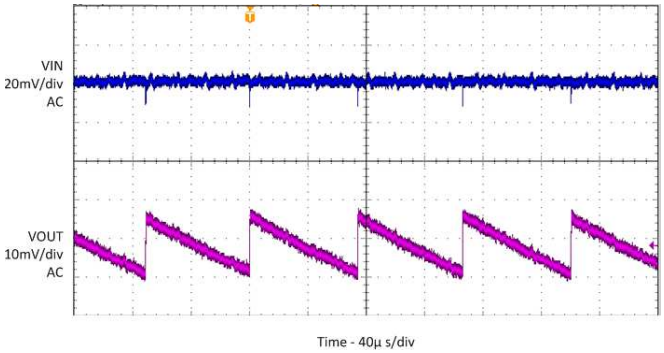
図 23. Switching Frequency

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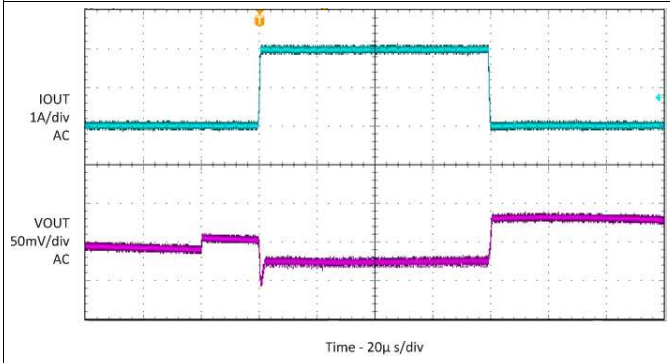
I_{OUT} = 2A

図 24. Input and Output Ripple in PWM Mode



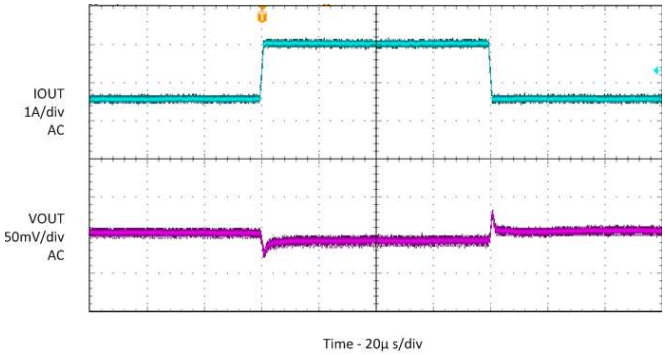
No Load

図 25. Input and Output Ripple in PSM Mode



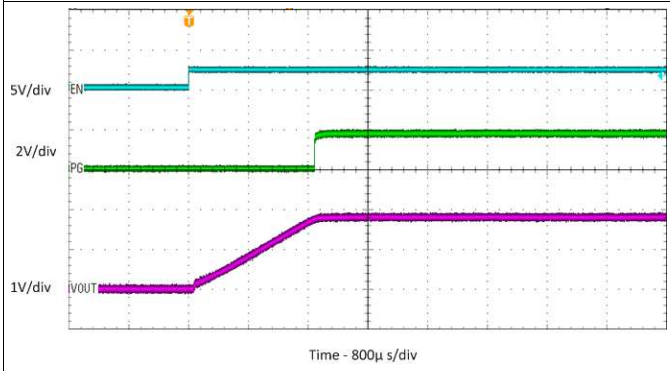
I_{OUT} = 0A to 2A,
1A/µs

図 26. Load Transient



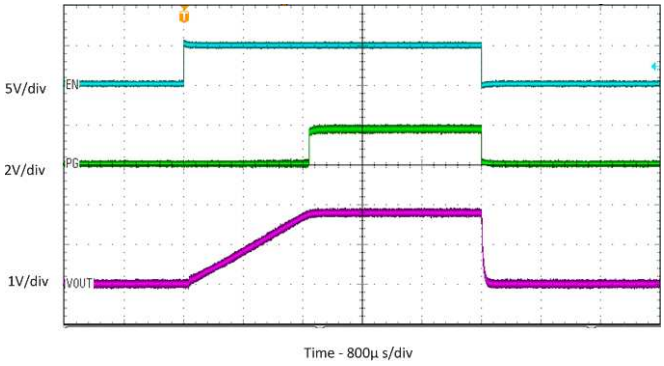
I_{OUT} = 0.5A to 2A,
1A/µs

図 27. Load Transient



No Load

図 28. Startup without Load



R_{OUT} = 1Ω

図 29. Startup / Shutdown with Resistance Load

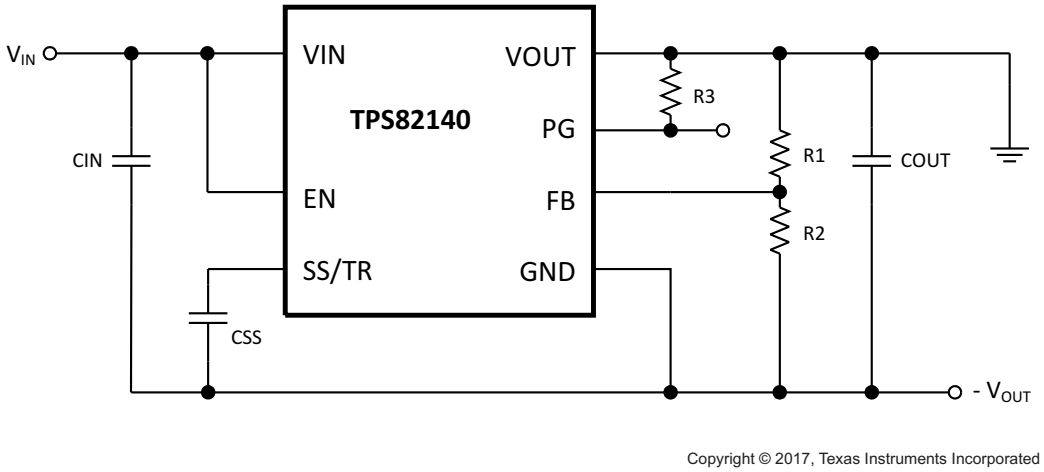
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8.3 System Examples

8.3.1 Inverting Power Supply

The TPS82140 can be used as inverting power supply by rearranging external circuitry as shown in 図 30. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17V (see 式 8).

$$V_{IN} + |V_{OUT}| \leq V_{INmax} \quad (8)$$



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図 30. Inverting Power Supply Schematic

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. Therefore the loop stability has to be adapted. More detailed information is given in TIDUCV2.

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3V and 17V. The average input current of the TPS82140 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (9)$$

Ensure that the power supply has a sufficient current rating for the applications.

10 Layout

10.1 Layout Guidelines

- TI recommends placing all components as close as possible to the IC. The input capacitor placement specifically, must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Refer to 図 31 for an example of component placement, routing and thermal design.

10.2 Layout Example

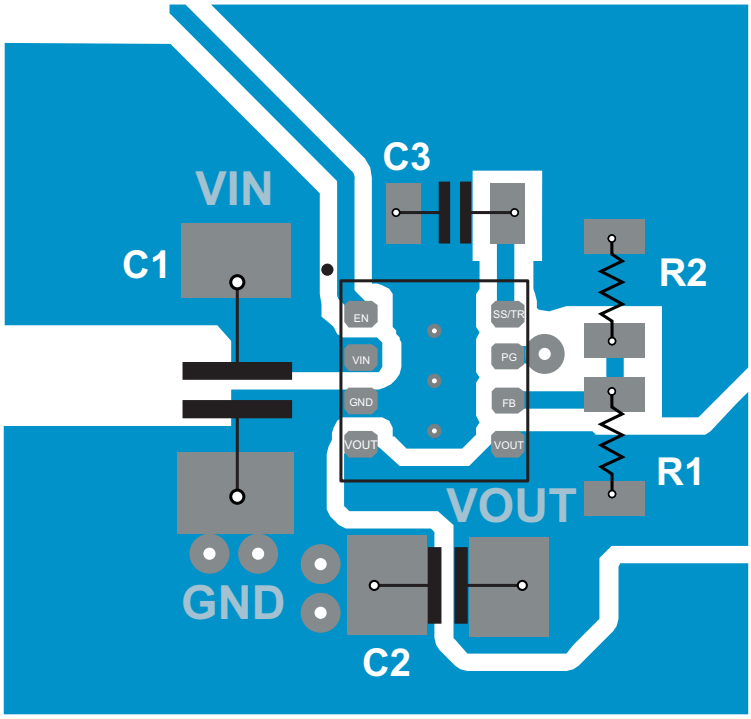


図 31. TPS82140 PCB Layout

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10.3 Thermal Consideration

The output current of the TPS82140 needs to be derated when the device operates in a high ambient temperature or delivers high output power. The amount of current derating is dependent upon the input voltage, output power, PCB layout design and environmental thermal condition. Care should especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS82140 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the TPS82140 to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82140, apply the typical efficiency stated in this datasheet to the desired application condition to find the module's power dissipation. Then calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: SZZA017 and SPRA953.

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.1.2 開発サポート

11.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPS82140デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

MicroSiP, DCS-Control, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

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11.6 Glossary

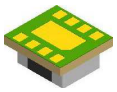
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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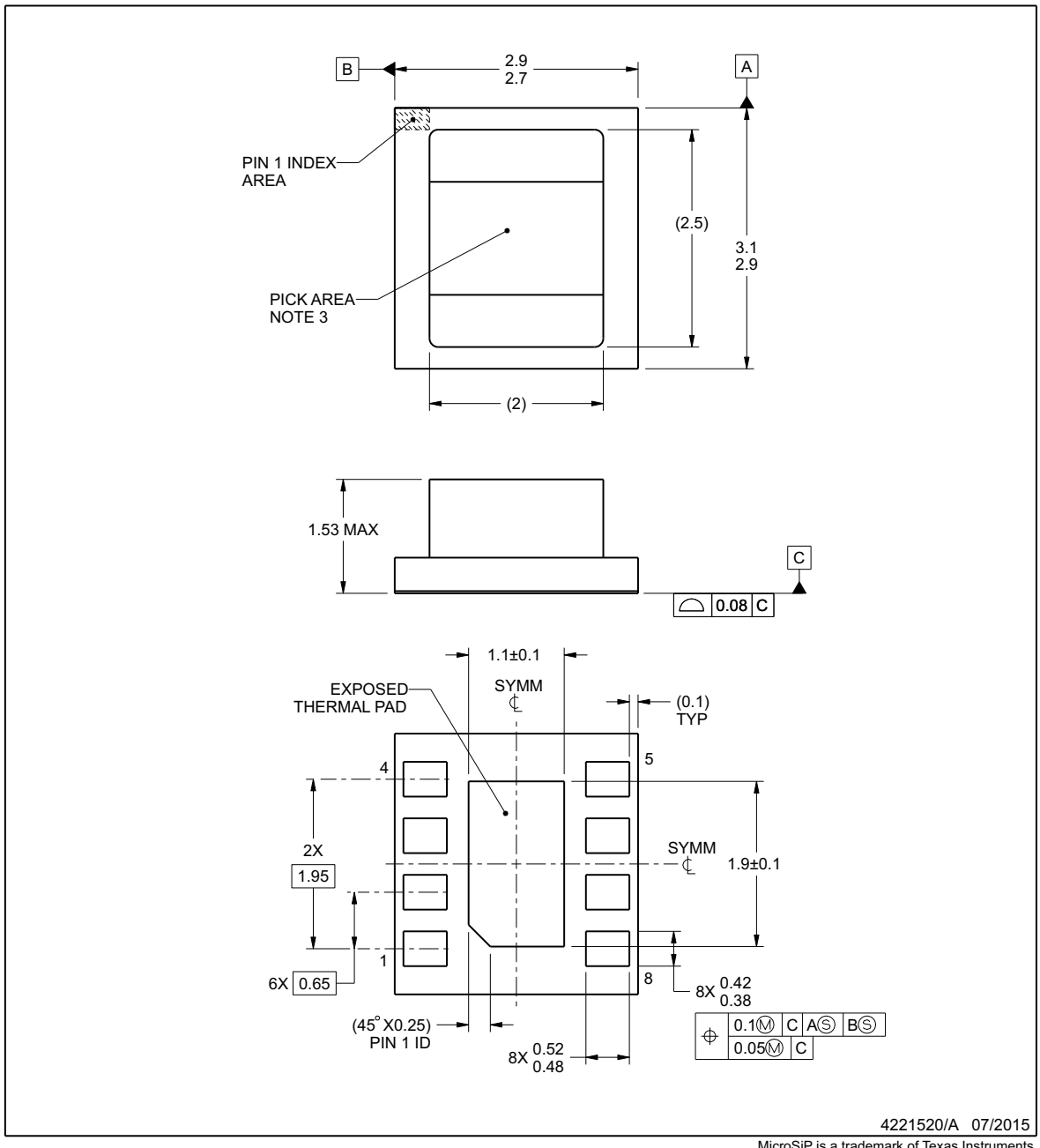


PACKAGE OUTLINE

SIL0008D

MicroSiP™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

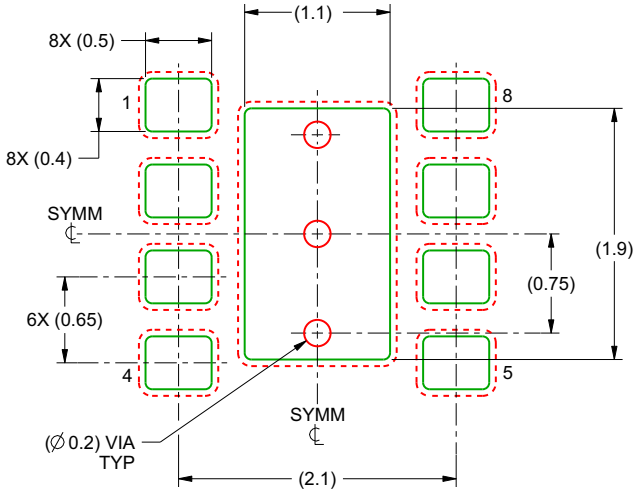
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EXAMPLE BOARD LAYOUT

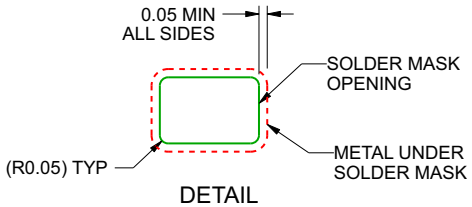
SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X



DETAIL
NOT TO SCALE

4221520/A 07/2015

NOTES: (continued)

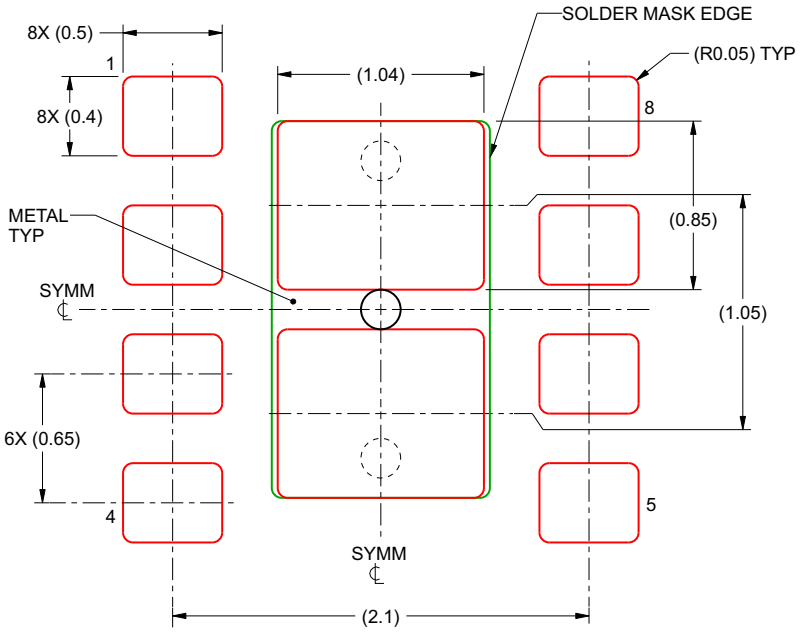
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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EXAMPLE STENCIL DESIGN

SIL0008D — **MicroSiP ™ - 1.53 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221520/A 07/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS82140SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	5R
TPS82140SILR.A	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	5R
TPS82140SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	5R
TPS82140SILT.A	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	5R

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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