TEXAS INSTRUMENTS
TPS84621
JAJSBO1E – DECEMBER 2011 – REVISED APRIL 2018

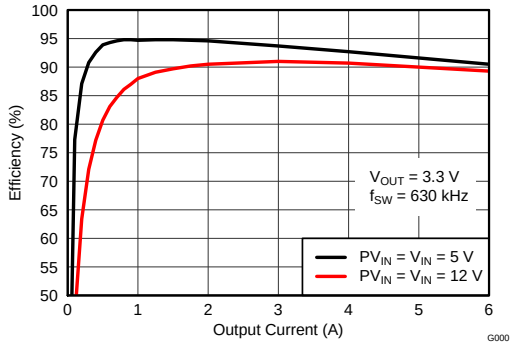
TPS84621 2.95V～14.5V入力、6A同期整流降圧型、統合電源ソリューション

1 特長

- 小さな占有面積で低プロファイルの設計を可能にする完全な統合電源ソリューション
- 最高96%の効率
- 0.6V～5.5Vの範囲で可変の広い出力電圧、リファレンス精度1%
- 並列動作によって大電流をサポート
- オプションの分割電源レールにより最低1.6Vの入力電圧を使用可能
- 可変スイッチング周波数(250kHz～780kHz)
- 外部クロックに同期
- 可変スロー・スタート
- 出力電圧のシーケンシングとトラッキング
- パワー・グッド出力
- 低電圧誤動作防止(UVLO)をプログラム可能
- 出力過電流保護(ヒカップ・モード)
- 過熱保護
- プリバイアスされた出力へのスタートアップ
- 動作温度範囲: -40℃～+85℃
- 強化された熱特性: 13℃/W
- EN55022 Class Bの放射規格に準拠
- 設計の手引きについては、http://www.ti.com/TPS84621を参照

2 アプリケーション

- ブロードバンドおよび通信インフラストラクチャ
- 自動試験機器/医療用機器
- Compact PCI、PCI Express、PXI Express
- DSPおよびFPGAのポイント・オブ・ロード・アプリケーション
- 高密度分散電源システム



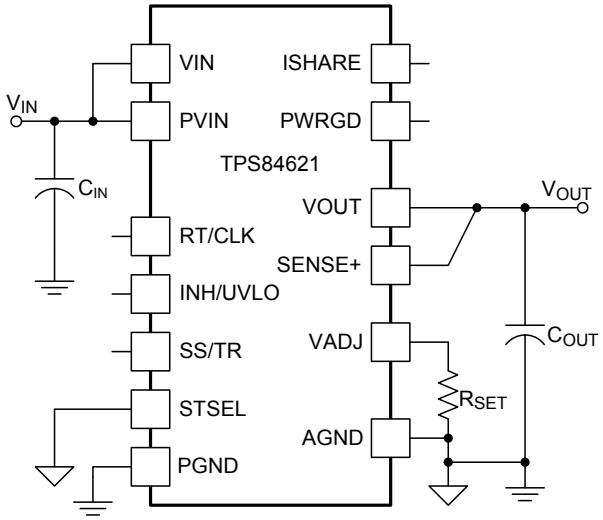
3 概要

TPS84621は使いやすい統合電源ソリューションで、6AのDC/DCコンバータとパワーMOSFET、インダクタ、受動部品が、低プロファイルのBQFNパッケージに組み合わされています。わずか3個の外付け部品だけで完全な電源ソリューションを構築でき、ループ補償や磁気部品の選択プロセスも不要になります。

9×15×2.8mmのBQFNパッケージはプリント基板にハンダ付けしやすく、小型のポイント・オブ・ロード設計で、90%を超える効率、優れた消費電力、接合部から周囲へ13℃/Wの熱インピーダンスを実現できます。このデバイスは、周囲温度85℃において無気流でも、6Aの定格出力電流を完全に供給できます。

TPS84621は、ディスクリートPOL設計と同等の柔軟性および機能セットを備え、高性能DSPおよびFPGAへの電力供給に最適です。先進のパッケージング技術により、標準のQFN実装/試験手法に対応した、堅牢で信頼性の高い電源ソリューションを実現できます。

アプリケーション概略図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table 1. ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

4 Specifications

4.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN, PVIN, INH/UVLO	–0.3	16	V
	PWRGD, RT/CLK	–0.3	6	V
	VADJ, SS/TR, STSEL, ISHARE	–0.3	3	V
Output Voltage	PH	–1	20	V
	PH 10-ns Transient	–3	20	V
V_{DIFF} (GND to exposed thermal pad)		–0.2	0.2	V
Source Current	RT/CLK	–100	100	µA
	PH		Current Limit	A
Sink Current	PH		Current Limit	A
	PVIN		Current Limit	A
	PWRGD	–0.1	5	mA
Operating Junction Temperature		–40	125(2)	°C
Storage Temperature		–65	150	°C
Peak Reflow Case Temperature(3)(4)			245	°C
Maximum Number of Reflows Allowed(3)(4)			3	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the Typical Characteristics section for thermal information.
(3) For soldering specifications, refer to the *Soldering Requirements for BQFN Packages* application note.
(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

Copyright © 2011–2018, Texas Instruments Incorporated

4.2 THERMAL INFORMATION

THERMAL METRIC(1)		TPS84621 RUQ47 47 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	13	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (4)	3.8	
θ_{JB}	Junction-to-board thermal resistance (5)	6	
ψ_{JT}	Junction-to-top characterization parameter(6)	2.5	
ψ_{JB}	Junction-to-board characterization parameter(7)	5	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm double-sided PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA}.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDECstandard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(7) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

4.3 PACKAGE SPECIFICATIONS

TPS84621		UNIT
Weight		1.26 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	33.9 MHrs

Copyright © 2011–2018, Texas Instruments Incorporated

4.4 ELECTRICAL CHARACTERISTICS

Over –40°C to 85°C free-air temperature, PVIN = VIN = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 6 A, C_{IN1} = 2 x 22 µF ceramic, C_{IN2} = 68 µF poly-tantalum, C_{OUT1} = 4 x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current	T_A = 85°C, natural convection		0		6	A
VIN	Input bias voltage range	Over I_{OUT} range		4.5		14.5	V
PVIN	Input switching voltage range	Over I_{OUT} range		1.6 (1)		14.5 (2)	V
UVLO	VIN Undervoltage lockout	VIN = increasing			4.0	4.5	V
		VIN = decreasing		3.5	3.85		
$V_{OUT(adj)}$	Output voltage adjust range	Over I_{OUT} range		0.6 (2)		5.5	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0A				±1.0% (3)	
	Temperature variation	-40°C ≤ T_A ≤ +85°C, I_{OUT} = 0A			±0.3%		
	Line regulation	Over PVIN range, T_A = 25°C, I_{OUT} = 0A			±0.1%		
	Load regulation	Over I_{OUT} range, T_A = 25°C			±0.1%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				±1.5% (3)	
η	Efficiency	PVIN = VIN = 12 V, I_O = 2 A	V_{OUT} = 5 V, f_{SW} = 780 kHz		92 %		
			V_{OUT} = 3.3 V, f_{SW} = 630 kHz		91 %		
			V_{OUT} = 2.5 V, f_{SW} = 530 kHz		89 %		
			V_{OUT} = 1.8 V, f_{SW} = 480 kHz		88 %		
			V_{OUT} = 1.2 V, f_{SW} = 480 kHz		85 %		
			V_{OUT} = 0.8 V, f_{SW} = 480 kHz		80 %		
		PVIN = VIN = 5 V, I_O = 2 A	V_{OUT} = 3.3V, f_{SW} = 630 kHz		95 %		
			V_{OUT} = 2.5V, f_{SW} = 530 kHz		93 %		
			V_{OUT} = 1.8V, f_{SW} = 480 kHz		91 %		
			V_{OUT} = 1.2V, f_{SW} = 480 kHz		89 %		
			V_{OUT} = 0.8V, f_{SW} = 480 kHz		85 %		
			V_{OUT} = 0.6V, f_{SW} = 250 kHz		83 %		
	Output voltage ripple	20 MHz bandwith			30		mV_{PP}
I_{LIM}	Overcurrent threshold				11		A
	Transient response	1.0 A/µs load step from 50 to 100% $I_{OUT(max)}$	Recovery time		80		µs
			V_{OUT} over/undershoot		60		mV
V_{INH-H}	Inhibit Control	Inhibit High Voltage		1.30		Open (4)	V
V_{INH-L}		Inhibit Low Voltage		–0.3		1.05	
	INH Input current	INH < 1.1 V			-1.15		µA
	INH Hysteresis current	INH > 1.26 V			-3.4		µA
$I_{I(stby)}$	Input standby current	INH pin to AGND			2	4	µA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		94%		
			Fault		109%		
		V_{OUT} falling	Fault		91%		
			Good		106%		
	PWRGD Low Voltage	I(PWRGD) = 2 mA				0.3	V
f_{SW}	Switching frequency	Over VIN and I_{OUT} ranges, RT/CLK pin OPEN		200	250	300	kHz
f_{CLK}	Synchronization frequency	CLK Control		250		780	kHz
V_{CLK-H}	CLK High-Level			2.0		5.5	V
V_{CLK-L}	CLK Low-Level					0.8	V
D_{CLK}	CLK Duty cycle			20%		80%	
	Thermal Shutdown	Thermal shutdown		160	175		°C
		Thermal shutdown hysteresis			10		°C

(1) The minimum PVIN voltage is 1.6V or (V_{OUT}+ 0.9V), whichever is greater. VIN must be greater than 4.5V.
(2) The maximum PVIN voltage is 14.5V or (15 x V_{OUT}), whichever is less.
(3) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(4) This control pin has an internal pullup. If this pin is left open circuit, the device operates when input power is applied. A small low-leakage MOSFET is recommended for control. See the application section for further guidance.

Copyright © 2011–2018, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Over –40°C to 85°C free-air temperature, PVIN = VIN = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 6 A, C_{IN1} = 2 x 22 µF ceramic, C_{IN2} = 68 µF poly-tantalum, C_{OUT1} = 4 x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	External input capacitance	Ceramic	44 (5)			µF
		Non-ceramic	68 (5)			
C_{OUT}	External output capacitance	Ceramic	47 (6)	200	1500	µF
		Non-ceramic		220 (6)	5000	
		Equivalent series resistance (ESR)			35	mΩ

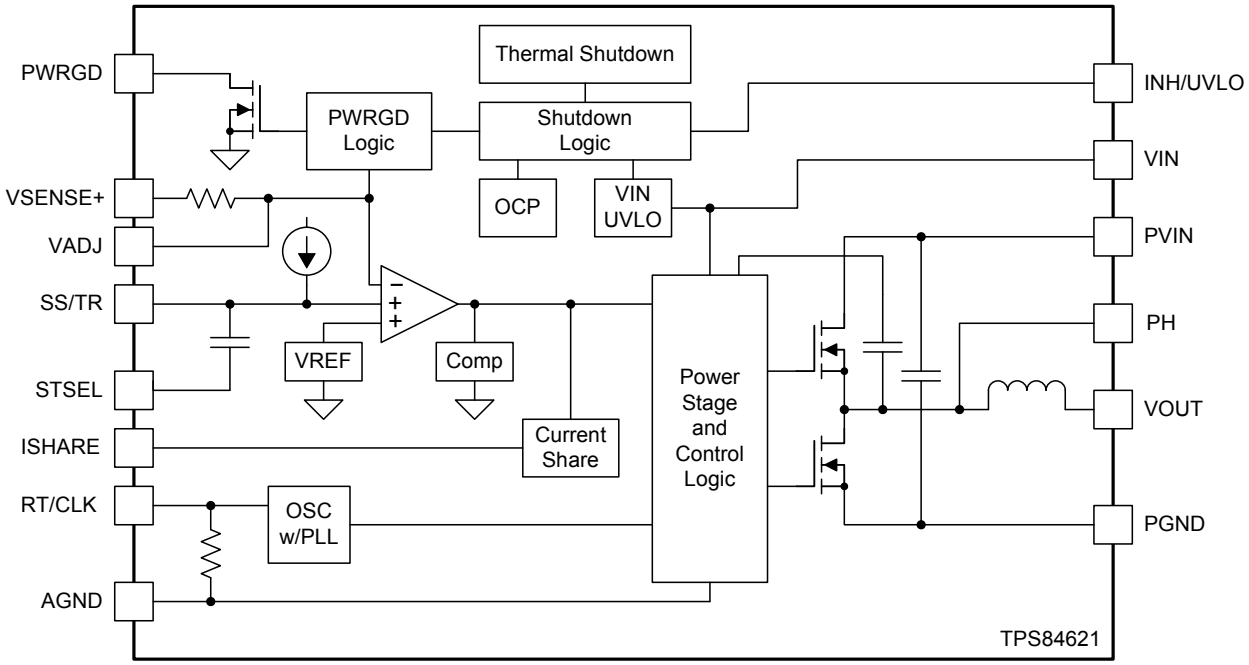
(5) A minimum of 100µF of polymer tantalum and/or ceramic external capacitance is required across the input (VIN and PVIN connected) for proper operation. Locate the capacitor close to the device. See Table 5 for more details. When operating with split VIN and PVIN rails, place 4.7µF of ceramic capacitance directly at the VIN pin.

(6) The amount of required output capacitance varies depending on the output voltage (see Table 4). The amount of required capacitance must include at least 1x 47µF ceramic capacitor. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 4 and Table 5 more details.

Copyright © 2011–2018, Texas Instruments Incorporated

5 DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



Copyright © 2011–2018, Texas Instruments Incorporated

PIN DESCRIPTIONS

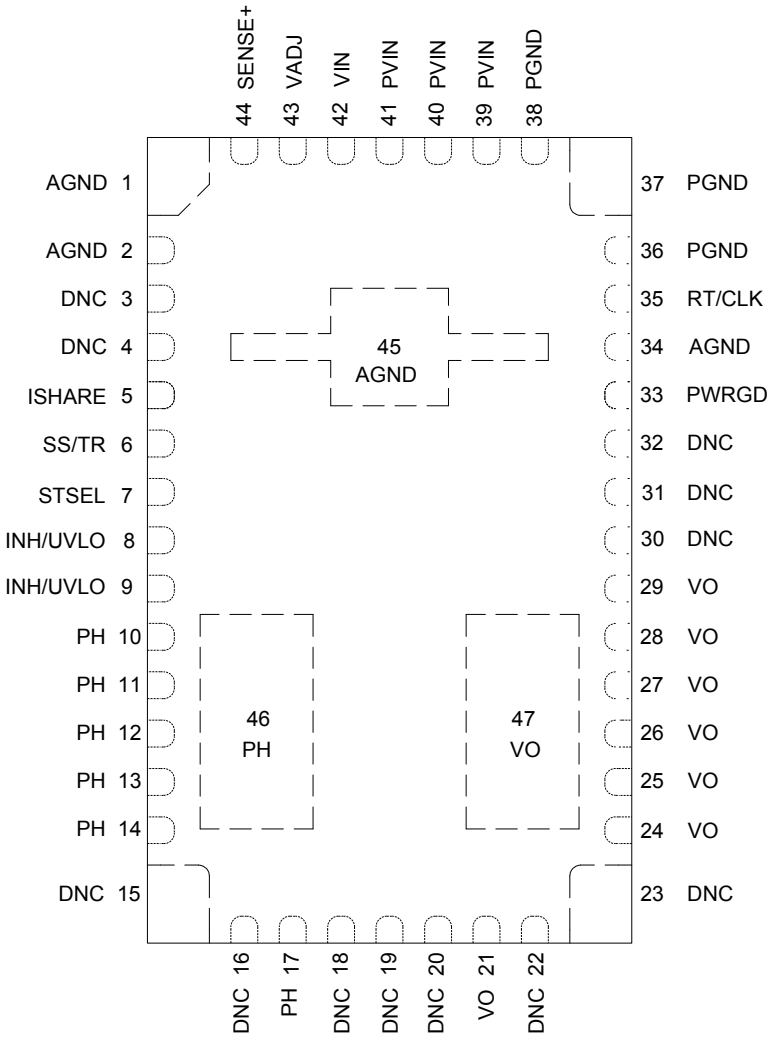
TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Zero VDC reference for the analog control circuitry. Connect AGND to PGND at a single point. Connect near the output capacitors. See Figure 43 for a recommended layout.
	2	
	34	
	45	
INH/UVLO	8	Inhibit and UVLO adjust pin. Use an open drain or open collector output logic to control the INH function. A resistor divider between this pin, AGND and VIN adjusts the UVLO voltage. Tie both pins together when using this control.
	9	
ISHARE	5	Current share pin. Connect this pin to other TPS84621 device's ISHARE pin when paralleling multple TPS84621 devices. When unused, treat this pin as a Do Not Connect (DNC) and leave it isolated from all other signals or ground.
DNC	3	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	4	
	15	
	16	
	18	
	19	
	20	
	22	
	23	
	30	
	31	
	32	
PGND	36	Common ground connection for the PVIN, VIN, and VOUT power connections. See Figure 43 for a recommended layout.
	37	
	38	
PH	10	Phase switch node. These pins should be connected to a small copper island under the device for thermal relief. Do not connect any external component to this pin or tie it to a pin of another function.
	11	
	12	
	13	
	14	
	17	
	46	
PWRGD	33	Power good fault pin. Asserts low if the output voltage is out of range. A pull-up resistor is required.
PVIN	39	Input switching voltage. This pin supplies voltage to the power switches of the converter. See Figure 43 for a recommended layout.
	40	
	41	
RT/CLK	35	This pin automatically selects between RT mode and CLK mode. A timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
SENSE+	44	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins.
SS/TR	6	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	7	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor with a SS interval of approximately 1.1 ms. Leave this pin open to enable the TR feature.
VADJ	43	Connecting a resistor between this pin and AGND sets the output voltage.
VIN	42	Input bias voltage pin. Supplies the control circuitry of the power converter. See Figure 43 for a recommended layout.

Copyright © 2011–2018, Texas Instruments Incorporated

PIN DESCRIPTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
VOUT	21	Output voltage. Connect output capacitors between these pins and PGND.
	24	
	25	
	26	
	27	
	28	
	29	
	47	

RUQ PACKAGE
47 PIN
TOP VIEW



Copyright © 2011–2018, Texas Instruments Incorporated

6 TYPICAL CHARACTERISTICS (PVIN = VIN = 12 V) (1) (2)

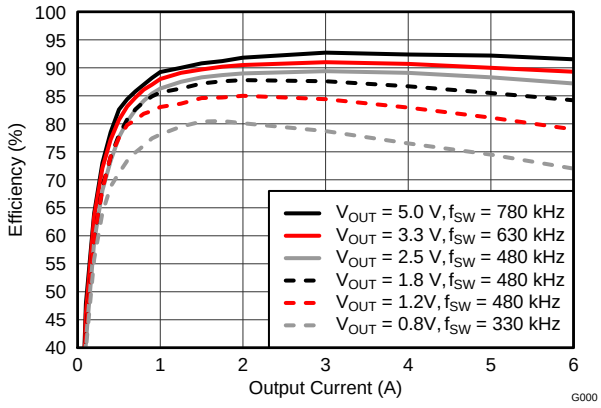


Figure 1. Efficiency vs. Output Current

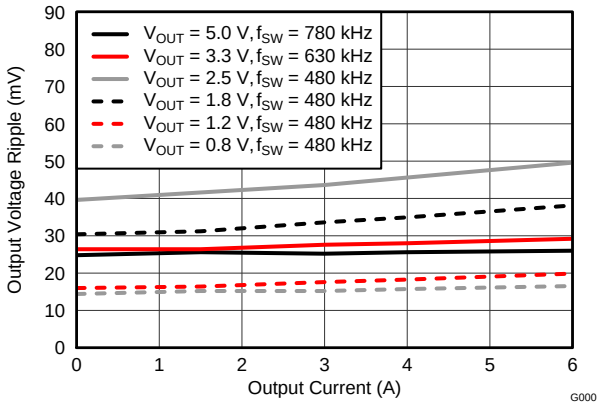


Figure 2. Voltage Ripple vs. Output Current

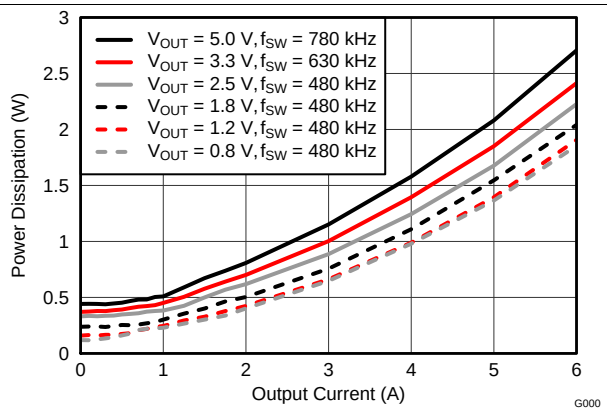


Figure 3. Power Dissipation vs. Output Current

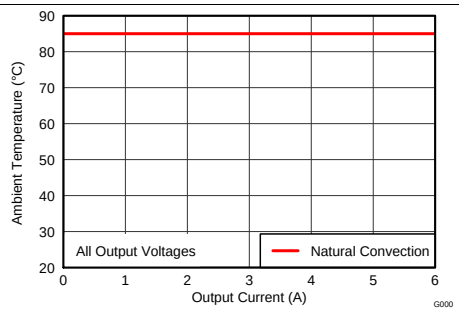


Figure 4. Safe Operating Area

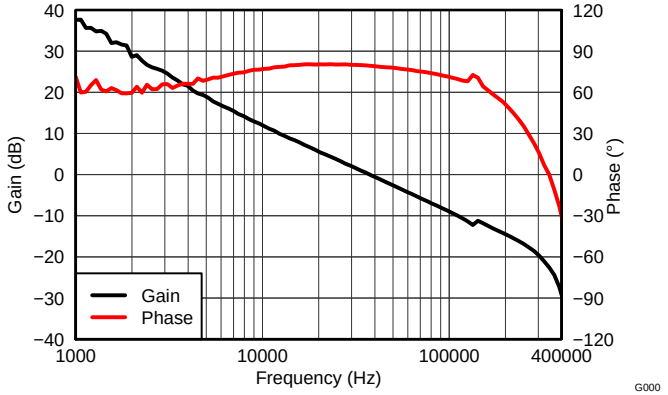


Figure 5. V_{OUT}= 1.8 V, I_{OUT}= 6 A, C_{OUT1}= 200 µF ceramic, f_{SW}= 480 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 4.

Copyright © 2011–2018, Texas Instruments Incorporated

7 TYPICAL CHARACTERISTICS (PVIN = VIN = 5 V) (1) (2)

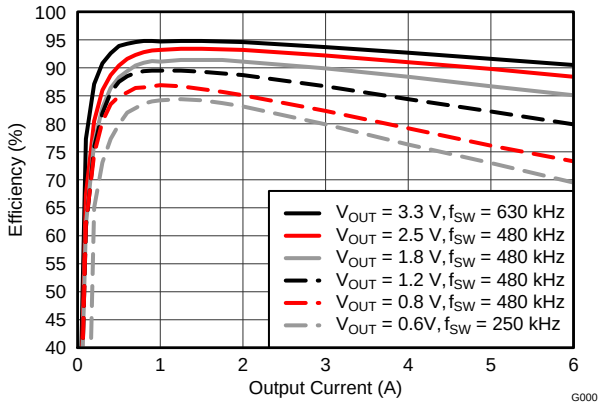


Figure 6. Efficiency vs. Output Current

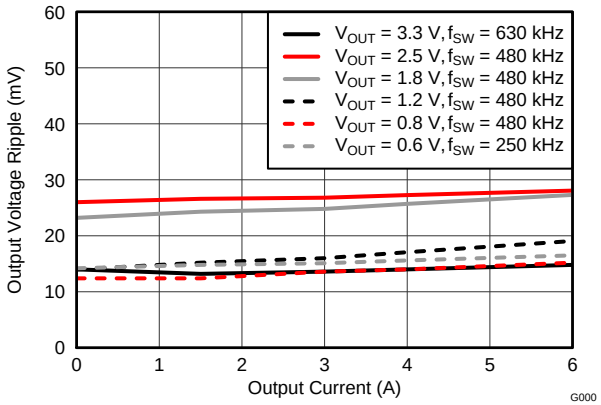


Figure 7. Voltage Ripple vs. Output Current

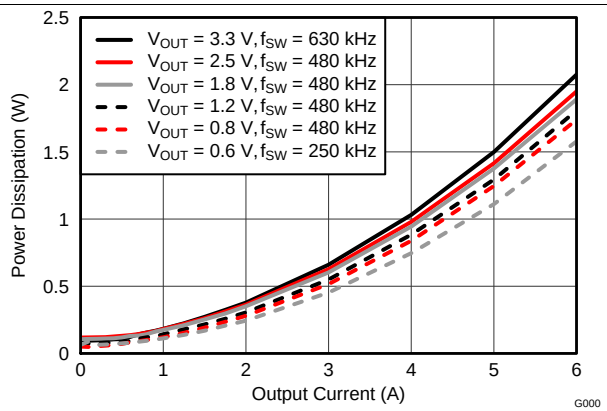


Figure 8. Power Dissipation vs. Output Current

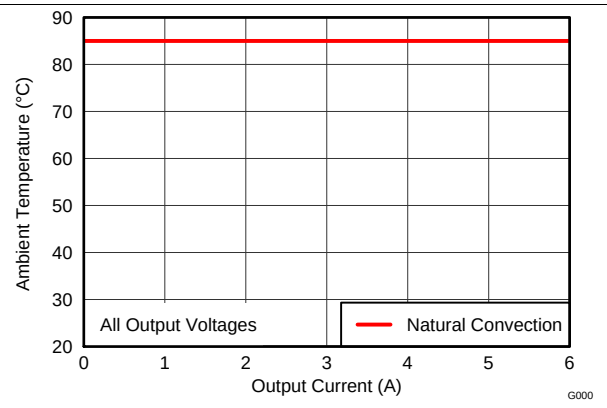


Figure 9. Safe Operating Area

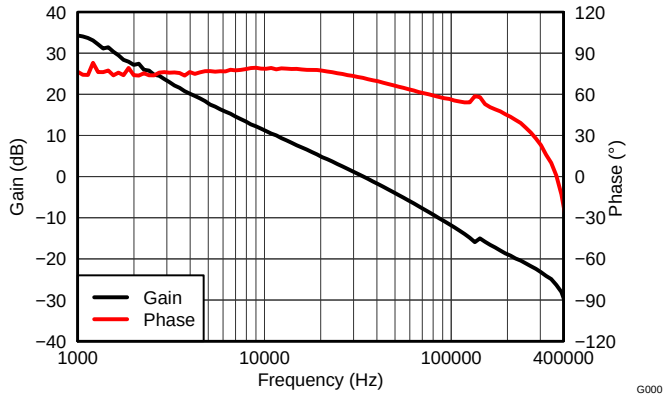


Figure 10. V_{OUT}= 1.8 V, I_{OUT}= 6 A, C_{OUT1}= 200 µF ceramic, f_{SW}=480 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 9.

Copyright © 2011–2018, Texas Instruments Incorporated

8 TYPICAL CHARACTERISTICS (PVIN = 12 V, VIN = 5 V) (1) (2)

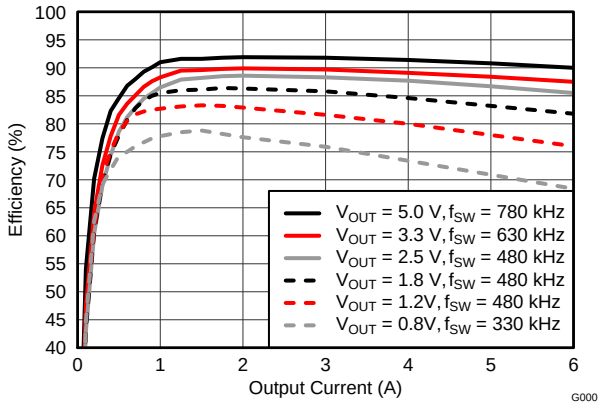


Figure 11. Efficiency vs. Output Current

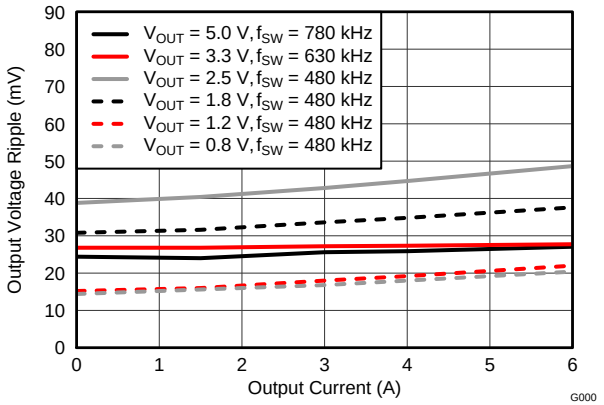


Figure 12. Voltage Ripple vs. Output Current

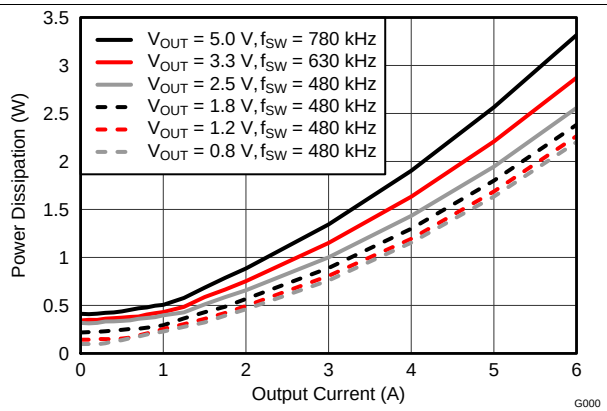


Figure 13. Power Dissipation vs. Output Current

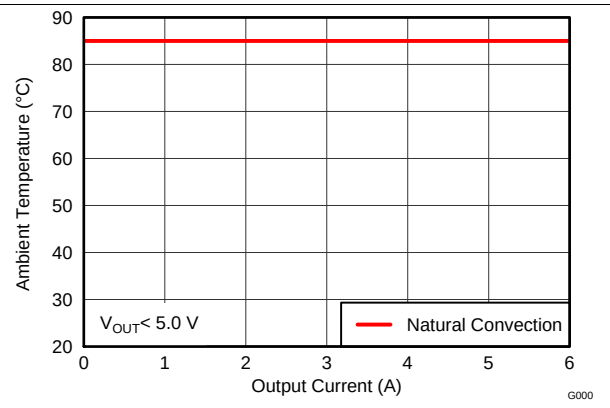


Figure 14. Safe Operating Area

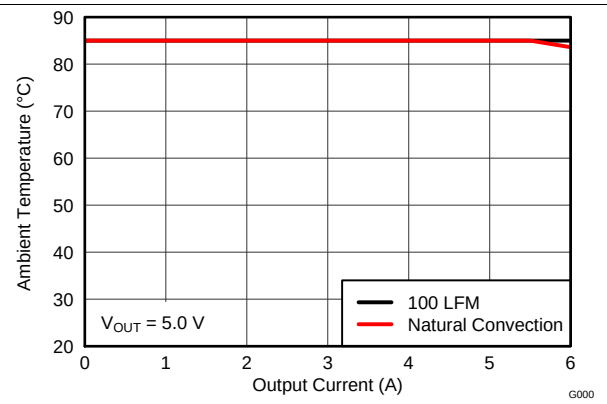


Figure 15. Safe Operating Area

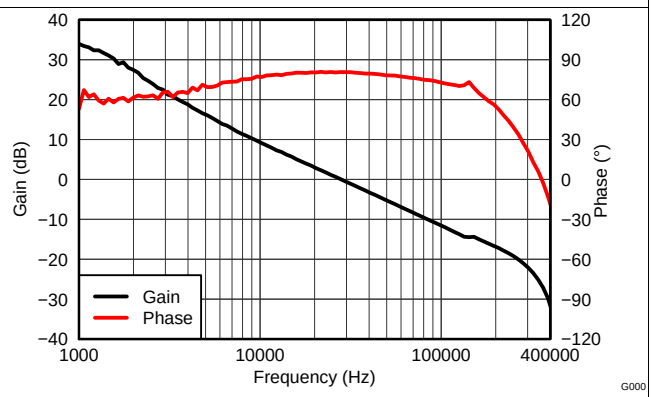


Figure 16. V_{OUT}= 2.5 V, I_{OUT}= 6 A, C_{OUT1}= 200 µF ceramic, f_{SW}= 480 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 11, Figure 12, and Figure 13.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 14 and Figure 15.

Copyright © 2011–2018, Texas Instruments Incorporated

9 APPLICATION INFORMATION

9.1 ADJUSTING THE OUTPUT VOLTAGE

The VADJ control sets the output voltage of the TPS84621. The output voltage adjustment range is from 0.6V to 5.5V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, the connection of SENSE+ to VOUT, and in some cases R_{RT} which sets the switching frequency. The R_{SET} resistor must be connected directly between the VADJ (pin 43) and AGND (pin 45). The SENSE+ pin (pin 44) must be connected to VOUT either at the load for improved regulation or at VOUT of the device. The R_{RT} resistor must be connected directly between the RT/CLK (pin 35) and AGND (pin 34). Table 2 gives the standard external R_{SET} resistor for a number of common bus voltages, along with the required R_{RT} resistor for that output voltage.

Table 2. Standard R_{SET} Resistor Values for Common Output Voltages

RESISTORS	OUTPUT VOLTAGE V_{OUT} (V)						
	0.9	1.0	1.2	1.8	2.5	3.3	5.0
R_{SET} (kΩ)	2.87	2.15	1.43	0.715	0.453	0.316	0.196
R_{RT} (kΩ)	261	261	200	200	165	121	86.6

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 3.

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \ (k\Omega) \quad (1)$$

Table 3. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)
0.6	open	open	250	3.1	0.348	140	580
0.7	8.66	590	330	3.2	0.332	140	580
0.8	4.32	590	330	3.3	0.316	121	630
0.9	2.87	261	430	3.4	0.309	121	630
1.0	2.15	261	430	3.5	0.294	121	630
1.1	1.74	261	430	3.6	0.287	121	630
1.2	1.43	200	480	3.7	0.280	121	630
1.3	1.24	200	480	3.8	0.267	107	680
1.4	1.07	200	480	3.9	0.261	107	680
1.5	0.953	200	480	4.0	0.255	107	680
1.6	0.866	200	480	4.1	0.243	107	680
1.7	0.787	200	480	4.2	0.237	95.3	730
1.8	0.715	200	480	4.3	0.232	95.3	730
1.9	0.665	200	480	4.4	0.226	95.3	730
2.0	0.619	200	480	4.5	0.221	95.3	730
2.1	0.576	200	480	4.6	0.215	95.3	730
2.2	0.536	200	480	4.7	0.210	95.3	730
2.3	0.511	200	480	4.8	0.205	86.6	780
2.4	0.475	200	480	4.9	0.200	86.6	780
2.5	0.453	200	480	5.0	0.196	86.6	780
2.6	0.432	165	530	5.1	0.191	86.6	780
2.7	0.412	165	530	5.2	0.187	86.6	780
2.8	0.392	165	530	5.3	0.182	86.6	780
2.9	0.374	165	530	5.4	0.178	86.6	780
3.0	0.357	140	580	5.5	0.174	86.6	780

Copyright © 2011–2018, Texas Instruments Incorporated

9.2 CAPACITOR RECOMMENDATIONS FOR THE TPS84621 POWER SUPPLY

9.2.1 Capacitor Technologies

9.2.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

9.2.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

9.2.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

9.2.2 Input Capacitor

The TPS84621 requires a minimum input capacitance of 100 µF of ceramic and/or polymer-tantalum capacitors. The ripple current rating of the capacitor must be at least 450 mArms. Table 5 includes a preferred list of capacitors by vendor.

9.2.3 Output Capacitor

The required output capacitance is determined by the output voltage of the TPS84621. See Table 4 for the amount of required capacitance. The required output capacitance must be comprised of all ceramic capacitors. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 5 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 6 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 5 includes a preferred list of capacitors by vendor.

Table 4. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.6	< 0.8	400 µF ceramic
0.8	< 1.2	300 µF ceramic
1.2	< 3.0	200 µF ceramic
3.0	< 4.0	100 µF ceramic
4.0	5.5	47 µF ceramic

Copyright © 2011–2018, Texas Instruments Incorporated

Table 5. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR (2) (mΩ)
Murata	X5R	GRM32ER61E226K	16	22	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	16TQC68M	16	68	50
Kemet	T520	T520V107M010ASE025	10	100	25
Sanyo	POSCAP	6TPE100MI	6.3	100	25
Sanyo	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Sanyo	POSCAP	2TPF330M6	2.0	330	6
Sanyo	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements.
(2) Maximum ESR @ 100kHz, 25°C.

9.3 Transient Response

Table 6. Output Voltage Transient Response

C_{IN1} = 47 µF CERAMIC, C_{IN2} = 220 µF POLYMER-TANTALUM						
V_{OUT} (V)	V_{IN} (V)	C_{OUT1} Ceramic	C_{OUT2} BULK	VOLTAGE DEVIATION (mV)		RECOVERY TIME (µs)
				2 A LOAD STEP, (1 A/µs)	3 A LOAD STEP, (1 A/µs)	
0.6	5	400 µF	330 µF	20	30	120
0.8	5	300 µF	220 µF	25	35	140
		300 µF	330 µF	20	30	140
	12	300 µF	220 µF	30	35	140
		300 µF	330 µF	25	30	140
1.2	5	200 µF	100 µF	40	50	150
		200 µF	220 µF	35	45	150
	12	200 µF	100 µF	35	45	150
		200 µF	220 µF	30	40	150
1.8	5	200 µF	-	65	85	160
		200 µF	100 µF	55	96	160
	12	200 µF	-	55	80	160
		200 µF	100 µF	50	75	160
3.3	5	100 µF	100 µF	90	140	180
	12	100 µF	100 µF	85	125	180

Copyright © 2011–2018, Texas Instruments Incorporated

9.4 Transient Waveforms

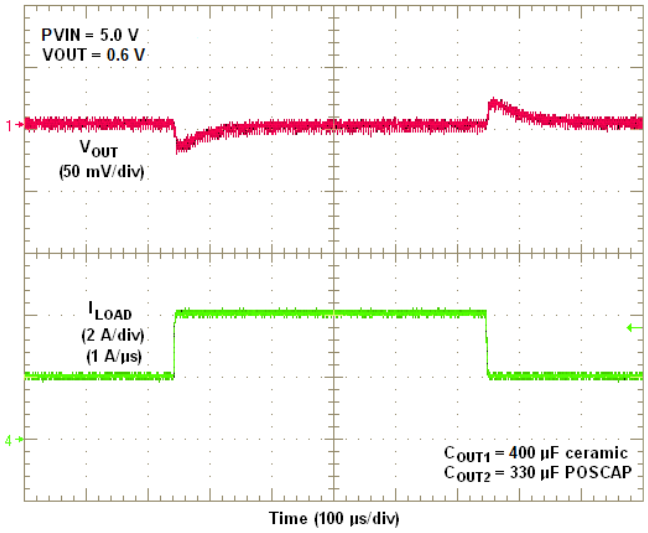


Figure 17. PVIN = 5V, VOUT = 0.6V, 2A Load Step

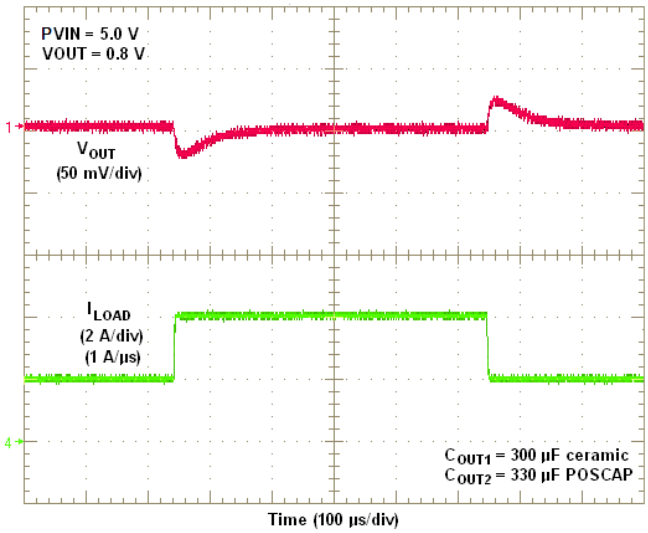


Figure 18. PVIN = 5V, VOUT = 0.8V, 2A Load Step

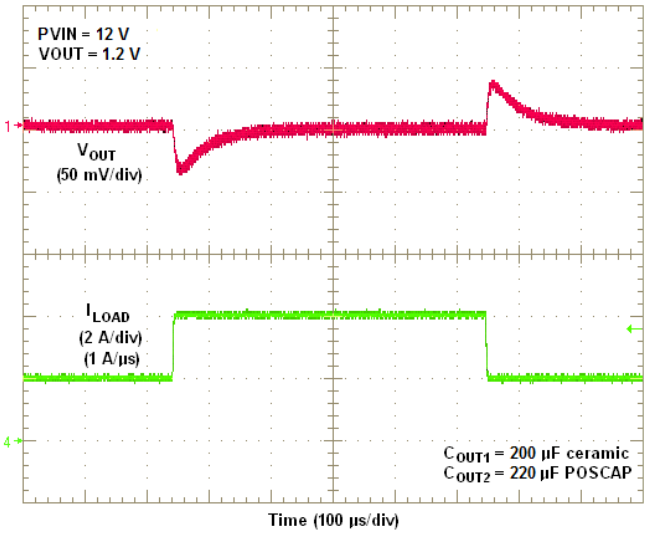


Figure 19. PVIN = 12V, VOUT = 1.2V, 2A Load Step

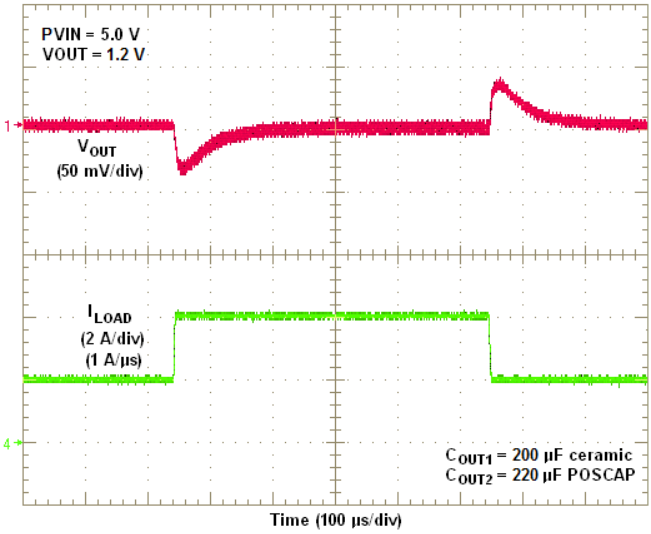


Figure 20. PVIN = 5V, VOUT = 1.2V, 2A Load Step

Copyright © 2011–2018, Texas Instruments Incorporated

Transient Waveforms (continued)

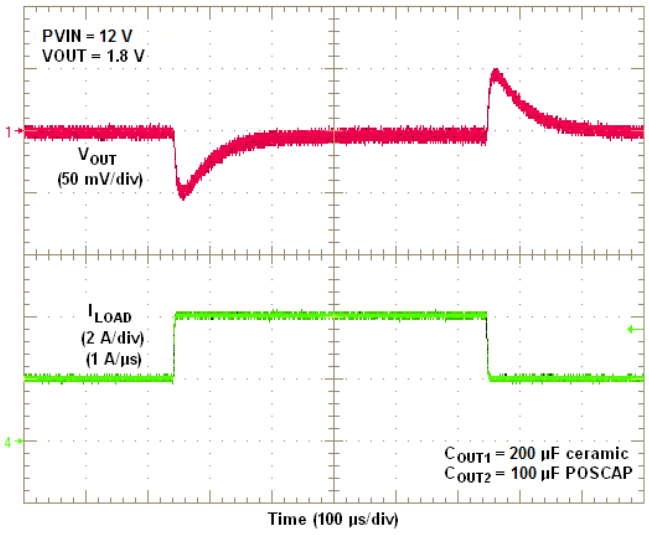


Figure 21. PVIN = 12V, VOUT = 1.8V, 2A Load Step

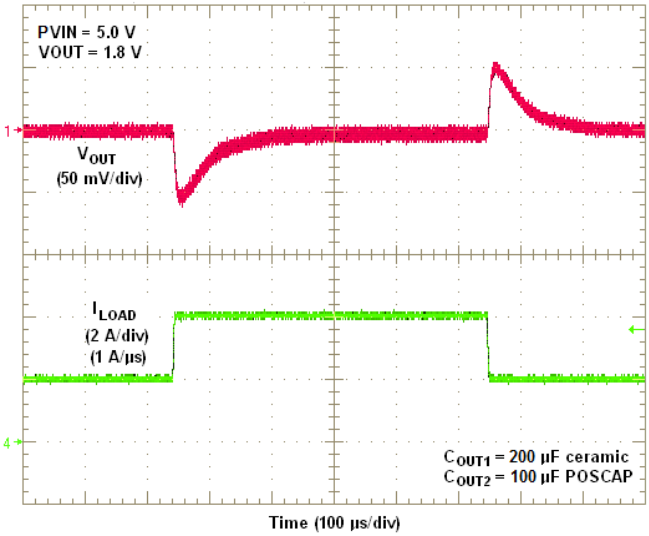


Figure 22. PVIN = 5V, VOUT = 1.8V, 2A Load Step

9.5 Application Schematics

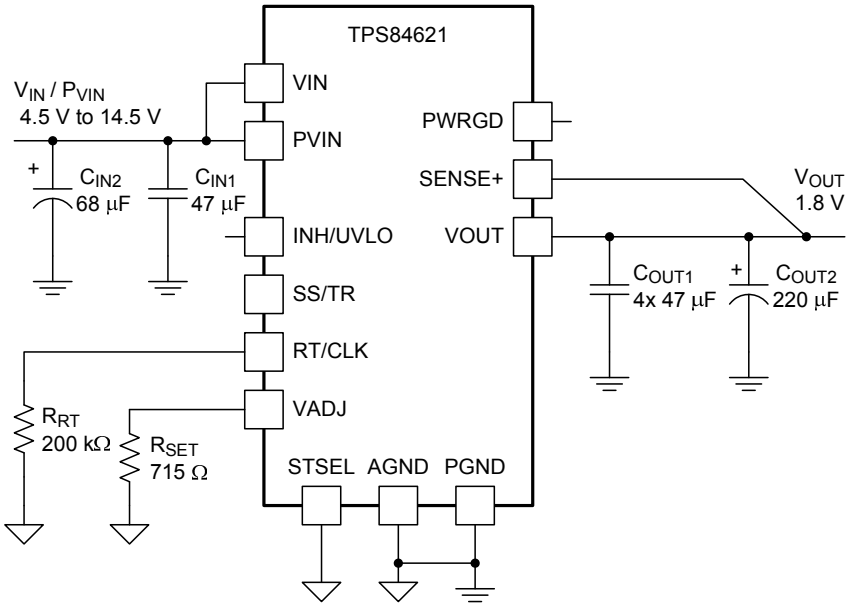


Figure 23. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 1.8 V

Copyright © 2011–2018, Texas Instruments Incorporated

Application Schematics (continued)

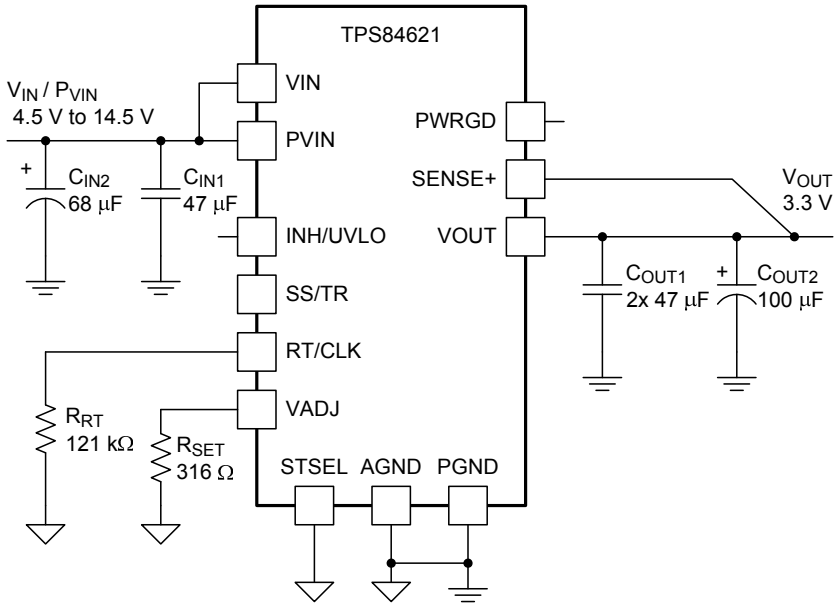


Figure 24. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 3.3 V

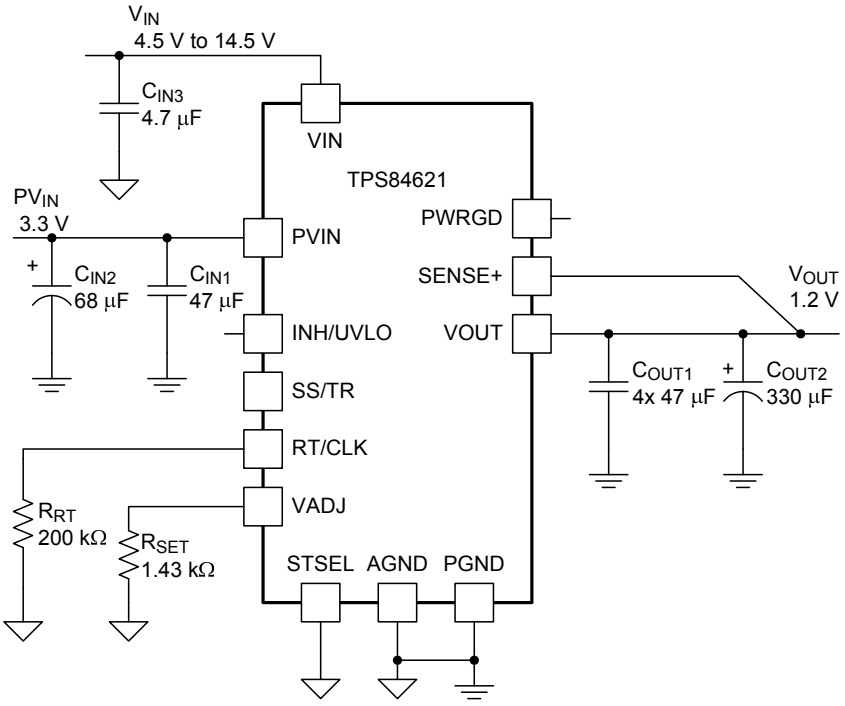


Figure 25. Typical Schematic
PVIN = 3.3 V, VIN = 4.5 V to 14.5 V, VOUT = 1.2 V

Copyright © 2011–2018, Texas Instruments Incorporated

9.6 VIN and PVIN Input Voltage

The TPS84621 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 14.5 V. If using the VIN pin separately from the PVIN pin, the VIN pin must be between 4.5 V and 14.5 V, and the PVIN pin can range from as low as 1.6 V to 14.5 V. A voltage divider connected to the INH/UVLO pin can adjust the either input voltage UVLO appropriately. See the Programmable Undervoltage Lockout (UVLO) section of this datasheet for more information.

9.7 3.3-V Input Operation

Applications operating from 3.3 V must provide at least 4.5 V for VIN. See application note, SLVA561 for help creating 5 V from 3.3 V using a small, simple charge pump device.

9.8 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 94% and 106% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.0 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 4.5V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 109% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, the INH pin is pulled low, or the SS/TR pin is below 1.4 V.

Copyright © 2011–2018, Texas Instruments Incorporated

9.9 Parallel Operation

Up to six TPS84621 devices can be paralleled for increased output current. Multiple connections must be made between the paralleled devices and the component selection is slightly different than for a stand-alone TPS84621 device. A typical TPS84621 parallel schematic is shown in Figure 26. Refer to application note, SLVA574 for information and design help when paralleling multiple TPS84621 devices.

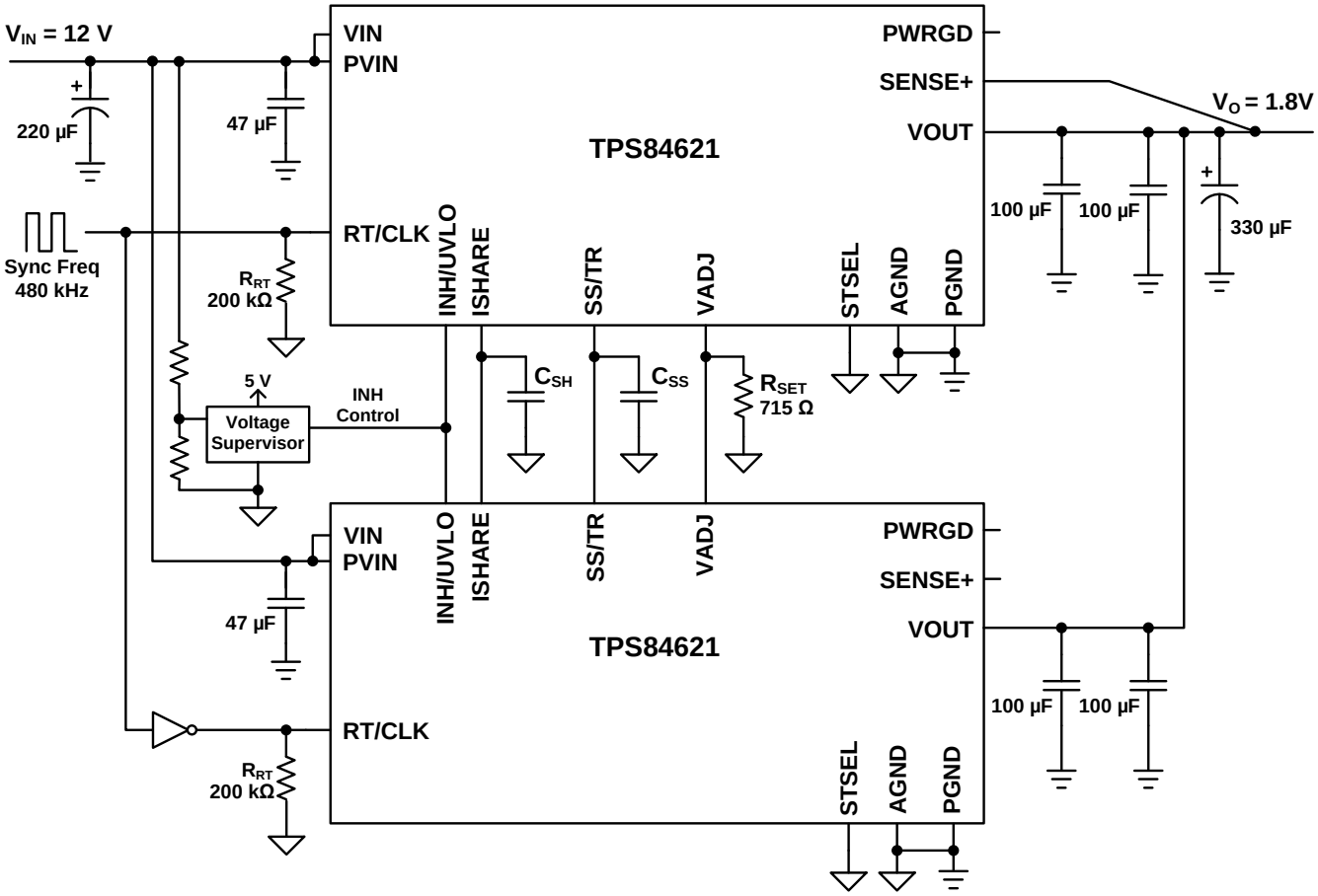


Figure 26. Typical TPS84621 Parallel Schematic

9.10 Power-Up Characteristics

When configured as shown in the front page schematic, the TPS84621 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 27 shows the start-up waveforms for a TPS84621, operating from a 5-V input (PVIN=VIN) and with the output voltage adjusted to 1.8 V. Figure 28 shows the start-up waveforms for a TPS84621 starting up into a pre-biased output voltage. The waveforms were measured with a 3-A constant current load.

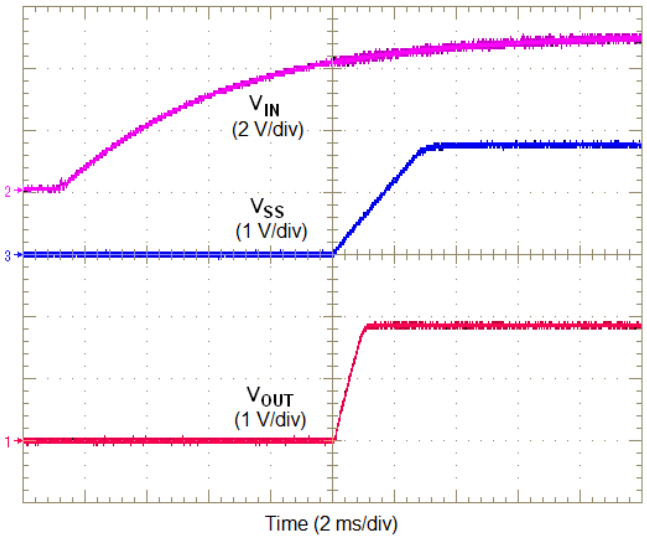


Figure 27. Start-Up Waveforms

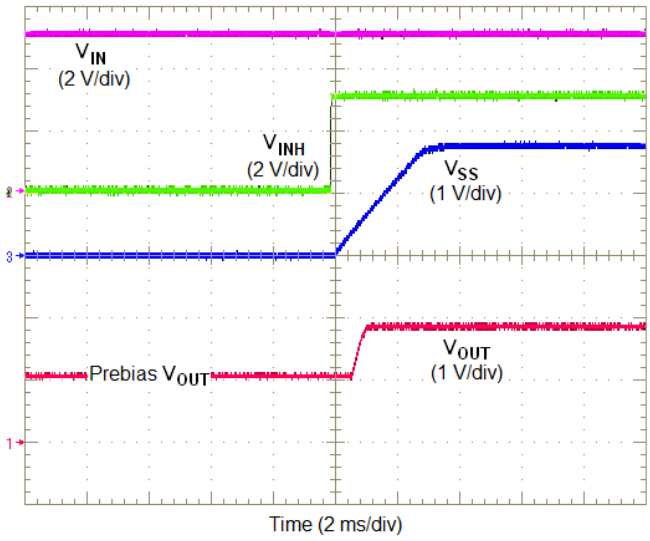


Figure 28. Start-up into Pre-bias

9.11 Pre-Biased Start-Up

The TPS84621 has been designed to prevent discharging a pre-biased output. During monotonic pre-biased startup, the TPS84621 does not allow current to sink until the SS/TR pin voltage is higher than 1.4 V.

9.12 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

9.13 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

Copyright © 2011–2018, Texas Instruments Incorporated

9.14 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 29 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 30. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 31. A regulated output voltage is produced within 3 ms. The waveforms were measured with a 3-A constant current load.

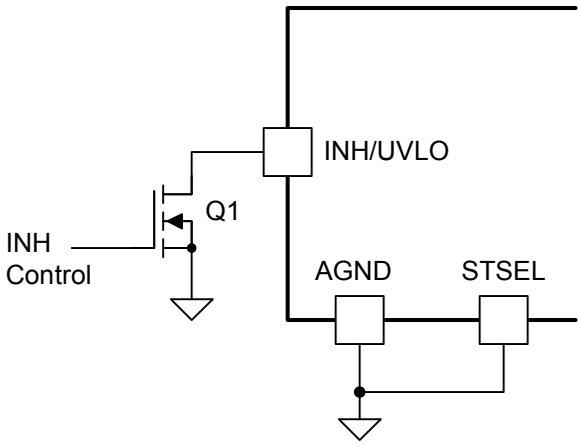


Figure 29. Typical Inhibit Control

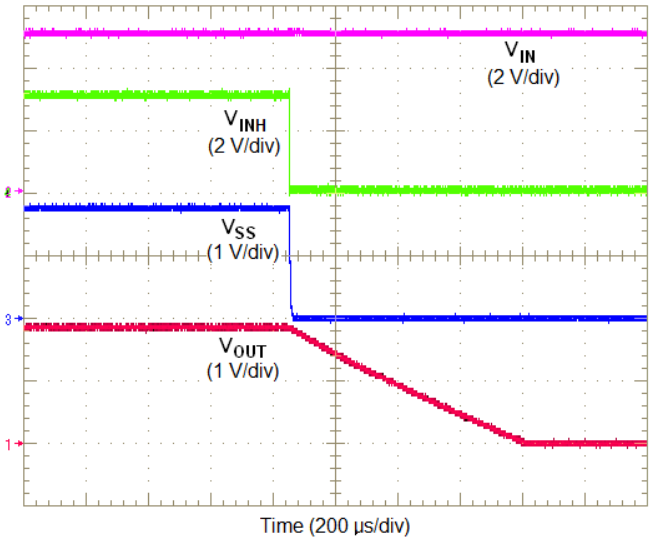


Figure 30. Inhibit Turn-Off

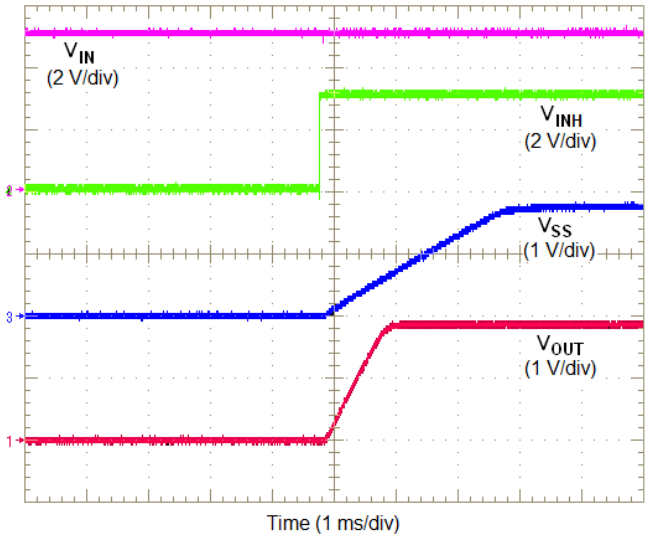


Figure 31. Inhibit Turn-On

Copyright © 2011–2018, Texas Instruments Incorporated

9.15 Slow Start (SS/TR)

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Table 7 shows an additional SS capacitor connected to the SS/TR pin and the STSEL pin connected to AGND. See Table 7 below for SS capacitor values and timing interval.

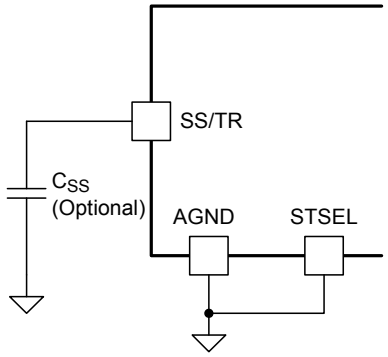


Figure 32. Slow-Start Capacitor (C_{SS}) and STSEL Connection

Table 7. Slow-Start Capacitor Values and Slow-Start Time

C_{SS} (pF)	open	2200	4700	10000	15000	22000	25000
SS Time (msec)	1.1	1.9	2.8	4.6	6.4	8.8	9.8

9.16 Overcurrent Protection

For protection against load faults, the TPS84621 incorporates output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in Figure 33. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 34.

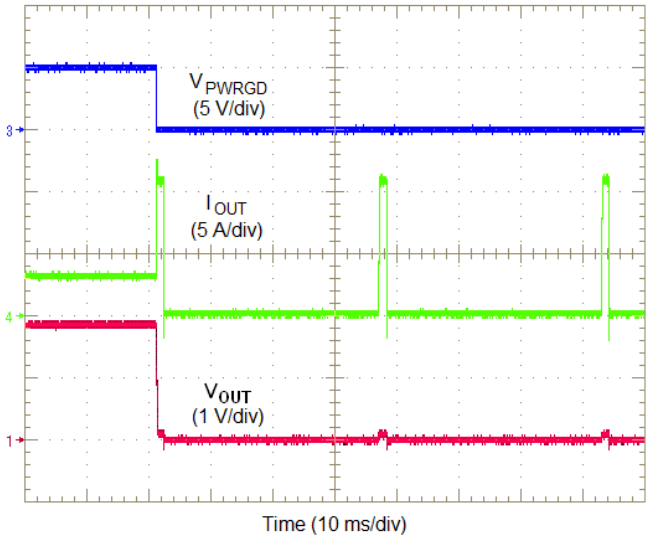


Figure 33. Overcurrent Limiting

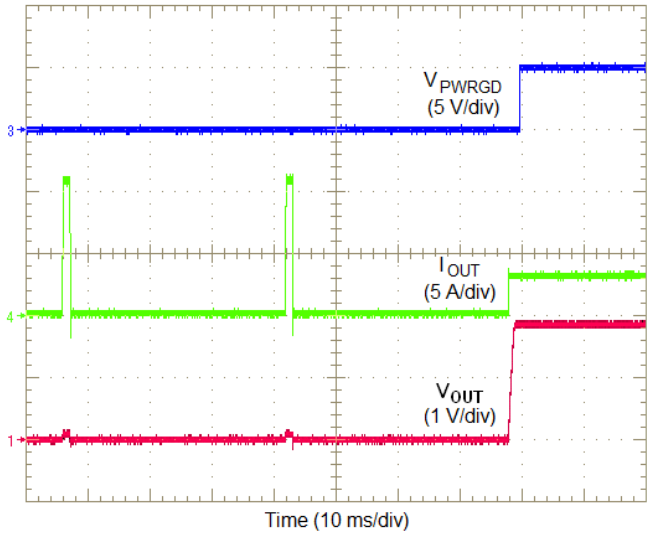


Figure 34. Removal of Overcurrent Condition

Copyright © 2011–2018, Texas Instruments Incorporated

9.17 Synchronization (CLK)

An internal phase locked loop (PLL) has been implemented to allow synchronization between 250 kHz and 780 kHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in .

Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to th CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor (R_{RT}).

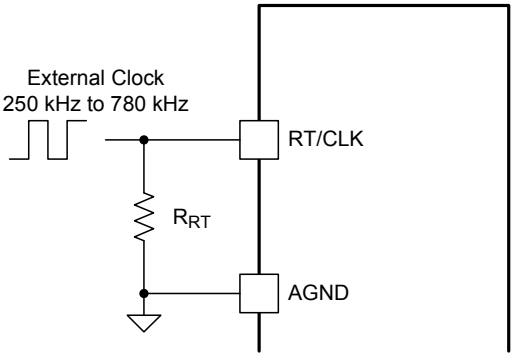


Figure 35. CLK/RT Configuration

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. Table 8 shows the allowable frequencies for a given range of output voltages. For the most efficient solution, always synchronize to the lowest allowable frequency. For example, an application requires synchronizing three TPS84621 devices with output voltages of 1.2 V, 1.8 V and 3.3 V, all powered from PVIN = 12 V. Table 8 shows that all three output voltages should be synchronized to 630 kHz.

Table 8. Synchronization Frequency vs Output Voltage

SYNCHRONIZATION FREQUENCY (kHz)	R_{RT} (kΩ)	PVIN = 12 V		PVIN = 5 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX
250	open	0.6	1.0	0.6	1.3
280	1100	0.6	1.2	0.6	1.6
330	590	0.6	1.5	0.6	4.5
380	357	0.7	1.7	0.6	4.5
430	261	0.8	2.1	0.6	4.5
480	200	0.9	2.5	0.6	4.5
530	165	1.0	2.9	0.6	4.5
580	140	1.1	3.2	0.6	4.5
630	121	1.2	3.7	0.6	4.5
680	107	1.3	4.1	0.6	4.5
730	95.3	1.4	4.7	0.6	4.5
780	86.6	1.5	5.5	0.6	4.5

Copyright © 2011–2018, Texas Instruments Incorporated

9.18 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, INH and PWRGD pins. The sequential method is illustrated in Figure 36 using two TPS84621 devices. The PWRGD pin of the first device is coupled to the INH pin of the second device which enables the second power supply once the primary supply reaches regulation. Figure 37 shows sequential turn-on waveforms of two TPS84621 devices.

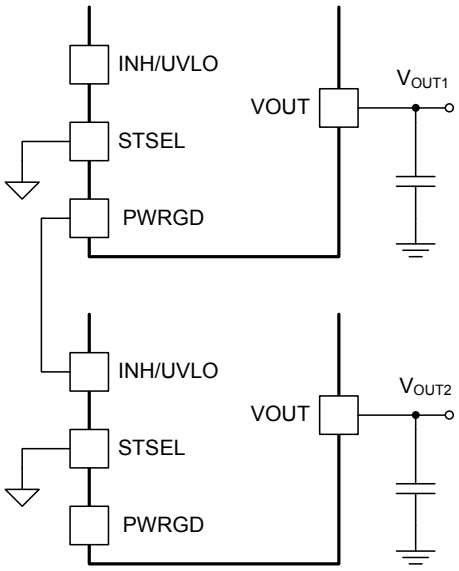


Figure 36. Sequencing Schematic

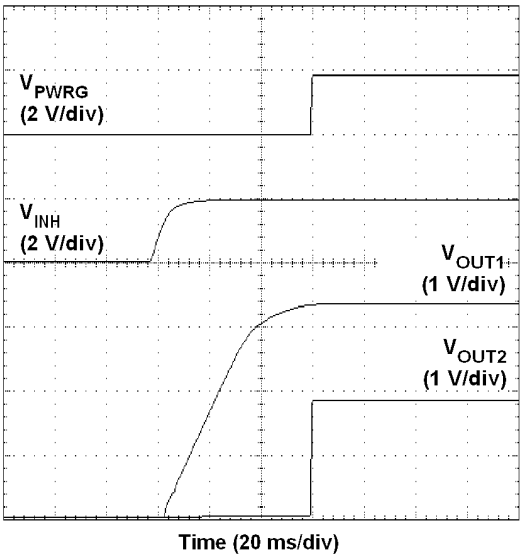


Figure 37. Sequencing Waveforms

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 38 to the output of the power supply that needs to be tracked or to another voltage reference source. Figure 39 shows simultaneous turn-on waveforms of two TPS84621 devices. Use Equation 2 and Equation 3 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 12.6)}{0.6} \ (k\Omega) \quad (2)$$

$$R2 = \frac{0.6 \times R1}{(V_{OUT2} - 0.6)} \ (k\Omega) \quad (3)$$

Copyright © 2011–2018, Texas Instruments Incorporated

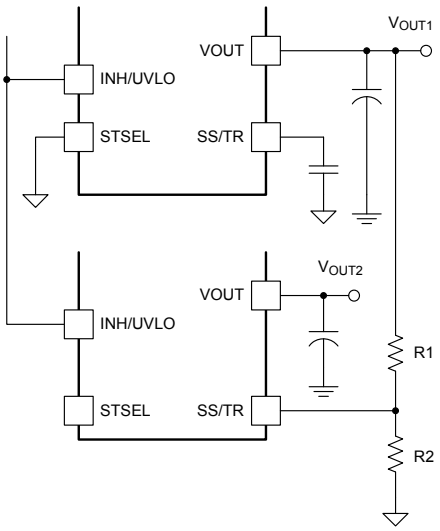


Figure 38. Simultaneous Tracking Schematic

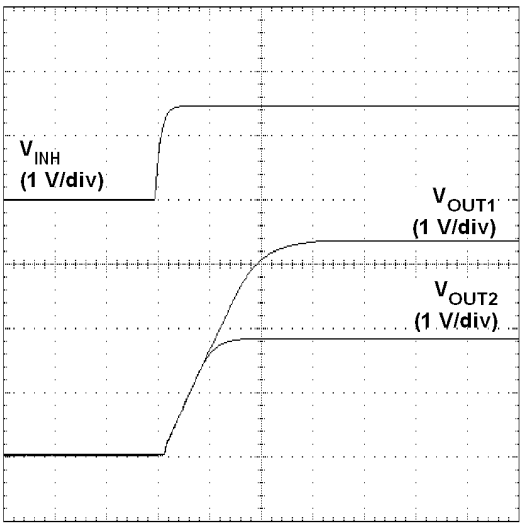


Figure 39. Simultaneous Tracking Waveforms

9.19 Programmable Undervoltage Lockout (UVLO)

The TPS84621 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.5 V(max) with a typical hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a higher UVLO threshold for a combined VIN and PVIN, then the UVLO pin can be configured as shown in Figure 40 or Figure 41. Table 9 lists standard values for R_{UVLO1} and R_{UVLO2} to adjust the VIN UVLO voltage up.

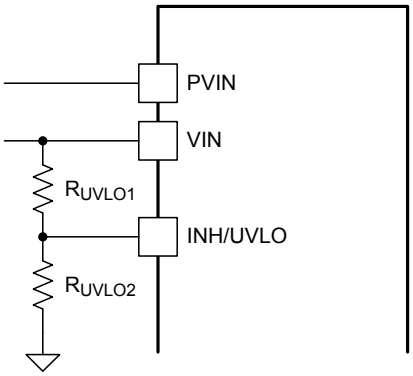


Figure 40. Adjustable VIN UVLO

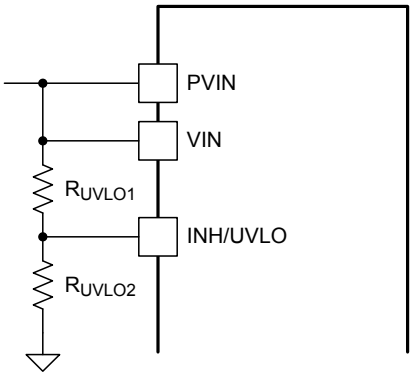


Figure 41. Adjustable VIN and PVIN Undervoltage Lockout

Table 9. Standard Resistor values for Adjusting VIN UVLO

VIN UVLO (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1
R_{UVLO2} (kΩ)	21.5	18.7	16.9	15.4	14.0	13.0	12.1	11.3	10.5	9.76	9.31
Hysteresis (mV)	400	415	430	450	465	480	500	515	530	550	565

For a split rail application, if a secondary UVLO on PVIN is required, VIN must be ≥ 4.5V. Figure 42 shows the PVIN UVLO configuration. Use Table 10 to select R_{UVLO1} and R_{UVLO2} for PVIN. If PVIN UVLO is set for less than 3.0 V, a 5.1-V zener diode should be added to clamp the voltage on the UVLO pin below 6 V.

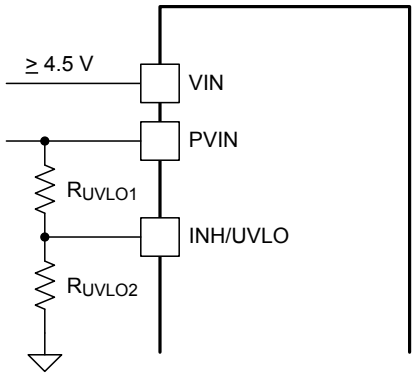


Figure 42. Adjustable PVIN Undervoltage Lockout, (VIN ≥4.5 V)

Table 10. Standard Resistor Values for Adjusting PVIN UVLO, (VIN ≥4.5 V)

PVIN UVLO (V)	2.0	2.5	3.0	3.5	4.0	4.5	
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1	68.1	For higher PVIN UVLO voltages see Table UV for resistor values
R_{UVLO2} (kΩ)	95.3	60.4	44.2	34.8	28.7	24.3	
Hysteresis (mV)	300	315	335	350	365	385	

Copyright © 2011–2018, Texas Instruments Incorporated

9.20 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 43, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the TPS84621.
- Isolate the PH copper area from the VOUT copper area using the AGND copper area.
- Connect the AGND and PGND copper area at one point; see AGND to PGND connection point in Figure 43.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

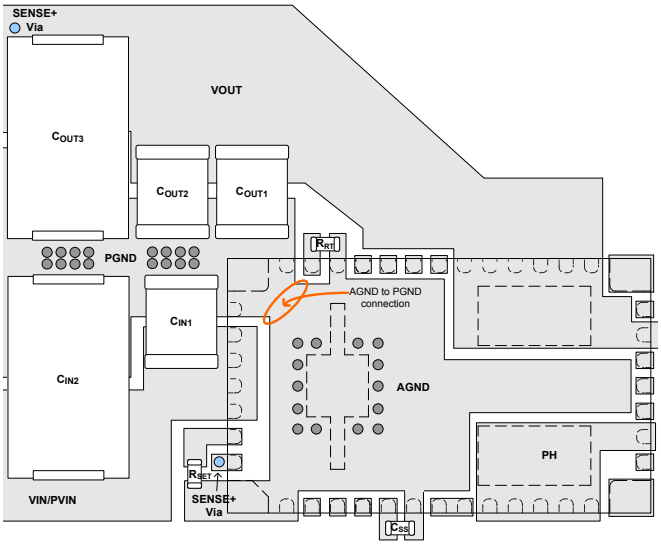


Figure 43. Typical Top-Layer Recommended Layout

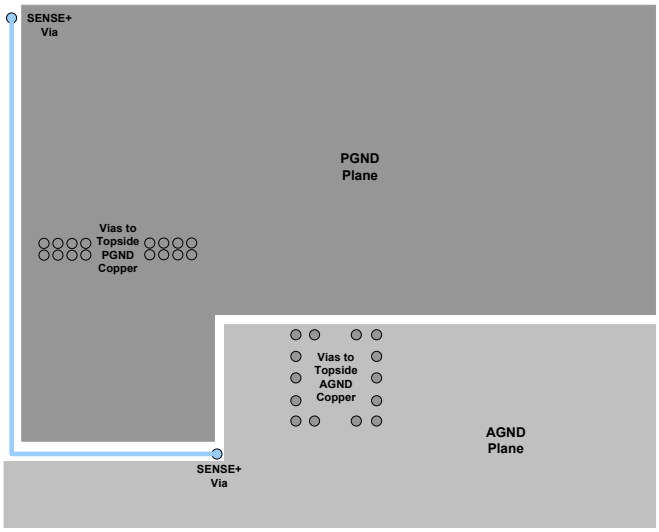


Figure 44. Typical GND-Layer Recommended Layout

9.21 EMI

The TPS84621 is compliant with EN55022 Class B radiated emissions. Figure 46 and Figure 45 show typical examples of radiated emissions plots for the TPS84621 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

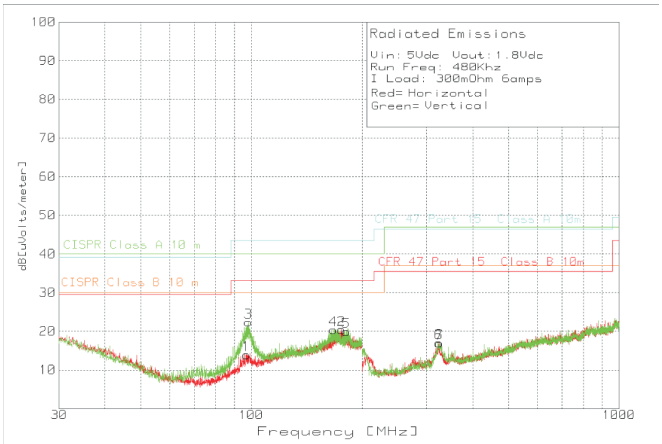


Figure 45. Radiated Emissions 5-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)

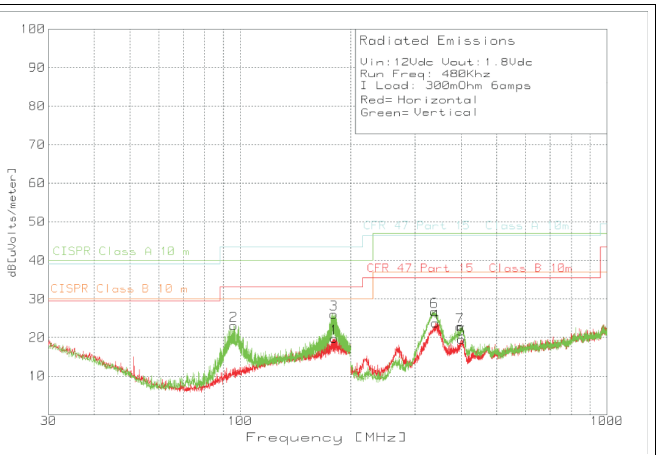


Figure 46. Radiated Emissions 12-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)

Copyright © 2011–2018, Texas Instruments Incorporated

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2017) to Revision E **Page**

- Increased the peak reflow temperature and maximum number of reflows to JEDEC specification for improved manufacturability 2

Changes from Revision C (February 2013) to Revision D **Page**

- Added peak reflow and maximum number of reflows information 2

Changes from Revision B (OCTOBER 2012) to Revision C **Page**

- 最小入力電圧を4.5Vから2.95Vへ 変更 1
- Added ISHARE parameter to Absolute Maximum Ratings table 2
- Added ISHARE to the Pin Description table 7
- Added Parallel Operation section. 19

Changes from Revision A (MAY 2012) to Revision B **Page**

- Added Thermal Information table 3

Changes from Original (DECEMBER 2011) to Revision A **Page**

- Changed – updated pin names in package drawing. 8

Copyright © 2011–2018, Texas Instruments Incorporated

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.3 商標

E2E is a trademark of Texas Instruments.

11.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2011–2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS84621RUQR	Active	Production	B1QFN (RUQ) | 47	500 | LARGE T&R	Exempt	NIPDAU	Level-3-245C-168 HR	-40 to 85	TPS84621
TPS84621RUQT	Active	Production	B1QFN (RUQ) | 47	250 | SMALL T&R	Exempt	NIPDAU	Level-3-245C-168 HR	-40 to 85	TPS84621
TPS84621RUQTG4	Active	Production	B1QFN (RUQ) | 47	250 | SMALL T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 85	TPS84621
TPS84621RUQTG4.B	Active	Production	B1QFN (RUQ) | 47	250 | SMALL T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 85	TPS84621

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

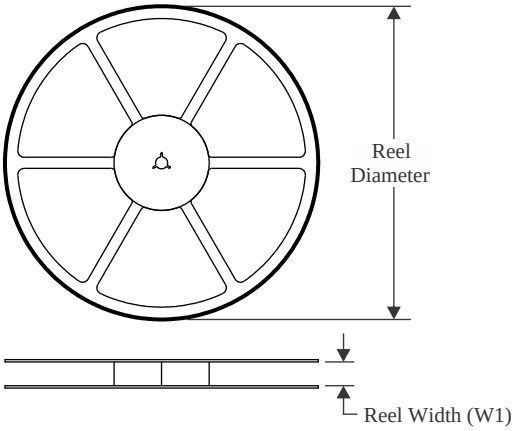
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

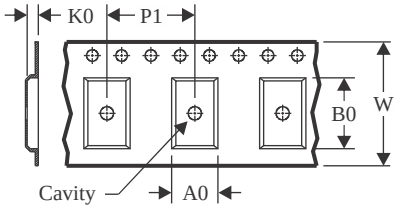
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

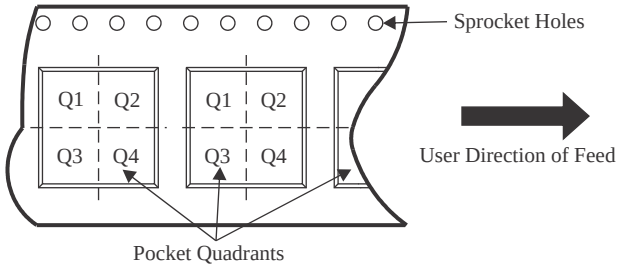


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

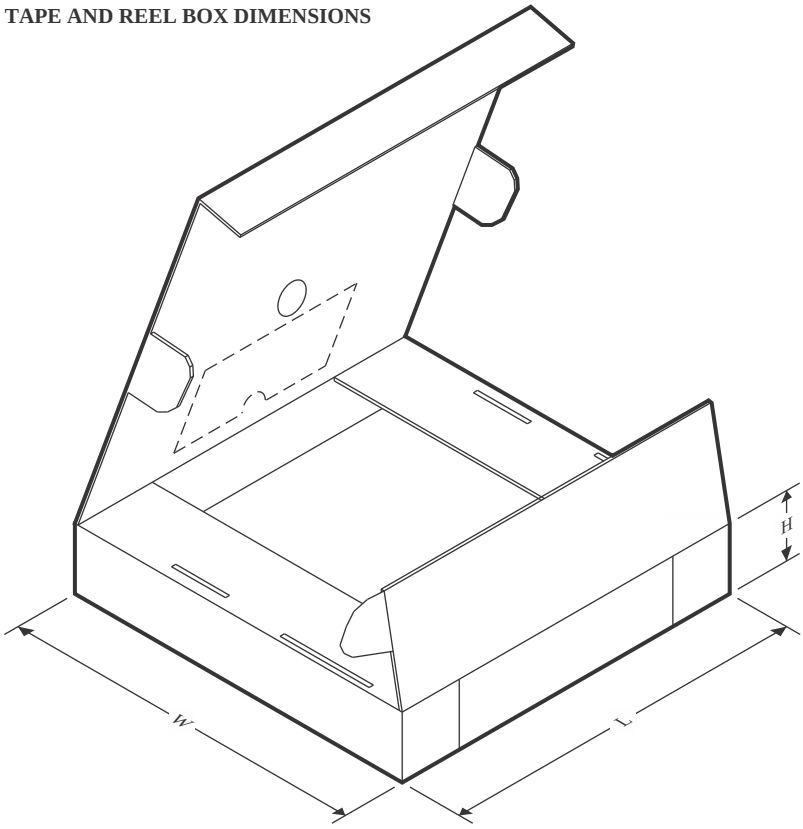
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84621RUQR	B1QFN	RUQ	47	500	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1
TPS84621RUQT	B1QFN	RUQ	47	250	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1
TPS84621RUQTG4	B1QFN	RUQ	47	250	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

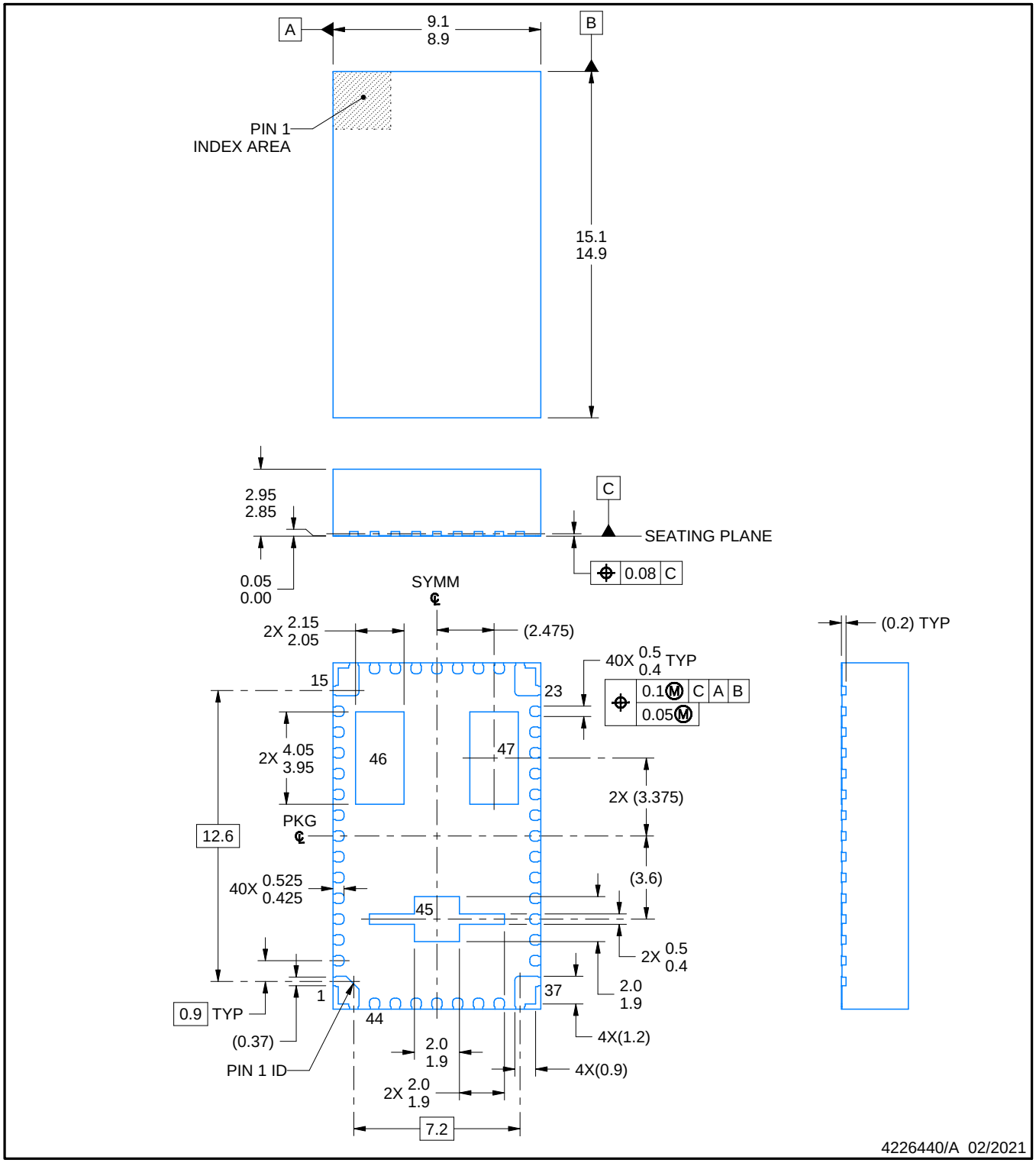
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84621RUQR	B1QFN	RUQ	47	500	383.0	353.0	58.0
TPS84621RUQT	B1QFN	RUQ	47	250	383.0	353.0	58.0
TPS84621RUQTG4	B1QFN	RUQ	47	250	383.0	353.0	58.0

PACKAGE OUTLINE

RUQ0047A

B1QFN - 2.95 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

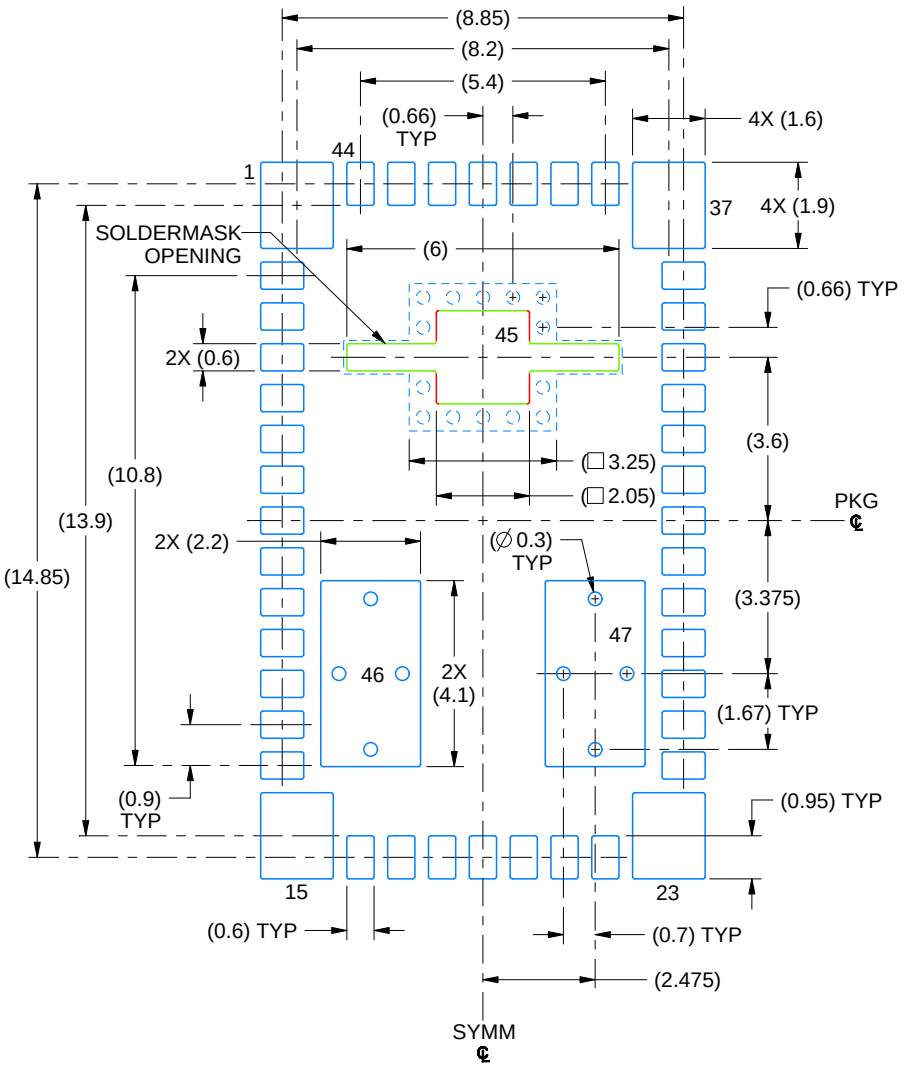
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

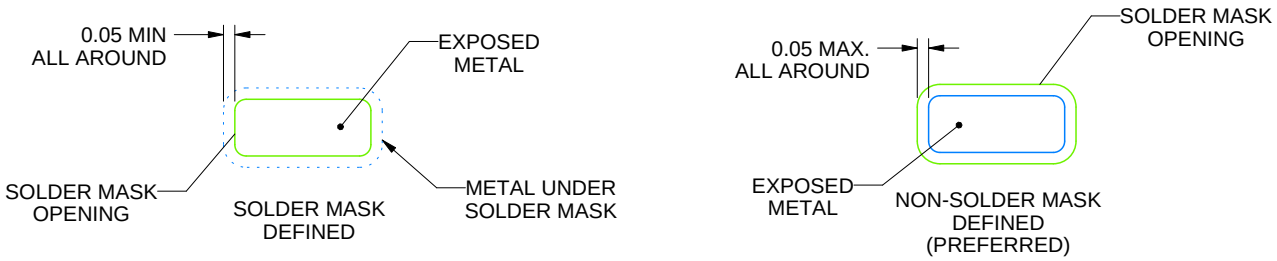
RUQ0047A

B1QFN - 2.95 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

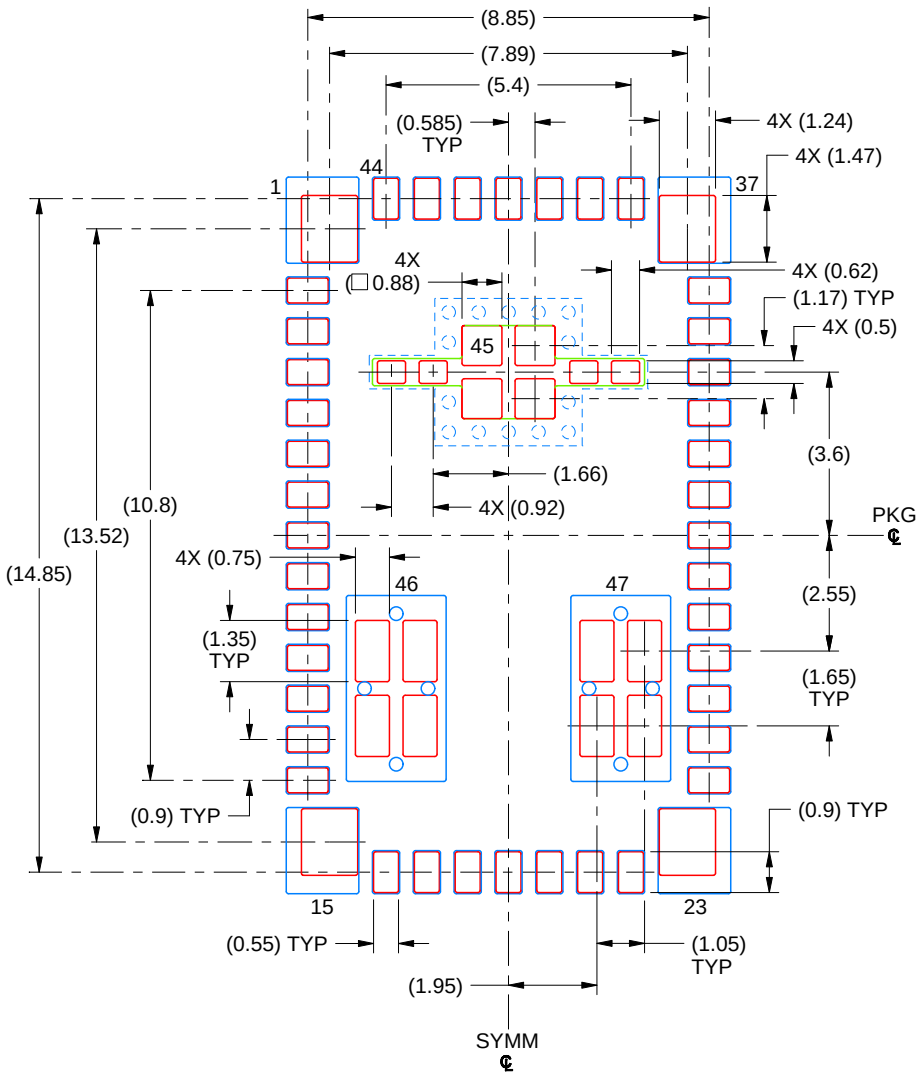


SOLDER MASK DETAIL

4226440/A 02/2021

NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm STENCIL THICKNESS

CORNER PINS 1, 15, 23 & 37:
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PAD 45:
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PAD 46 & 47:
45% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:6X

4226440/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月