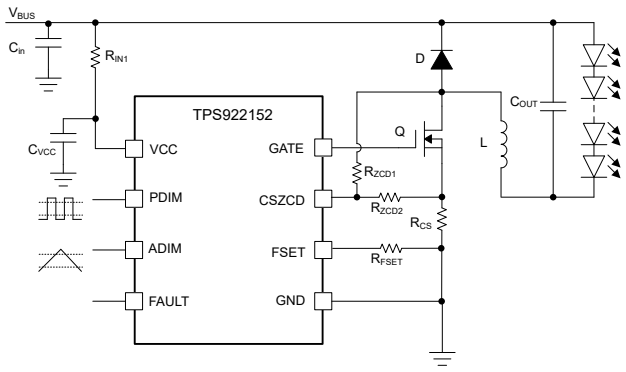
TPS922152 Average-Current Buck LED Driver with Wide Input Range, 0.1% Analog Dimming Ratio and Inductive Fast PWM Dimming

1 Features

- Wide application voltage up to 200V
- 4.5V to 15V input voltage range
- LED common Anode connection
- Adjustable switching frequency: 50kHz-1MHz
- Adaptive Off-Time mode
- Advanced dimming options:
  - Analog dimming (1000:1)
  - PWM dimming (50ns pulse width, 1000:1 at 20kHz)
  - Flexible dimming (20,000:1 at 20kHz PWM)
- Low Standby current
- Full protection features:
  - LED open and short protection
  - Cycle-by-cycle current limit
  - Sense resistor open and short protection
  - Fault output
- Package: SOIC-8

2 Applications

- Constant Illumination:
  - Residential lighting, Area & landscape lighting, Stage lighting
  - Laser TV and Display panel for TV
  - Exit & emergency lighting, LED power supply
- Instant Illumination:
  - Machine Vision
  - Fire safety system



Simplified Schematic

3 Description

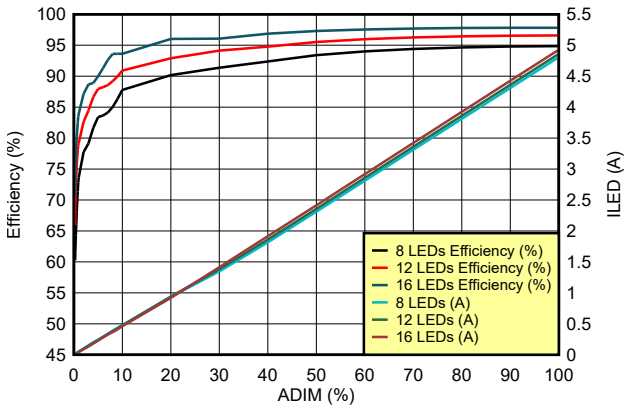
The TPS922152 is a non-synchronous, Average-Current control Buck LED driver with a wide bus voltage range of 4.5V to 200V. It utilizes Adaptive Off-Time (AOT) mode to drive external switching FETs, ensuring low LED current ripple and fast transient response even with a small output capacitor. The switching frequency is configurable from 50kHz to 1MHz, supporting single-layer PCB design and common anode configurations.

For dimming, the TPS922152 supports high-accuracy analog dimming via the ADIM pin, achieving a dimming ratio of up to 1000:1 using unique corrective sensing technology. For PWM dimming, the PDIM pin uses proprietary Inductive Fast Dimming (IFD) to provide high-frequency, high-ratio control with high precision. Additionally, the device integrates comprehensive protection features, including LED open/short and sense resistor open/short protection.

Device Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)
TPS922152	SOIC (8)	4.9mm × 3.9mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency and Dimming Linearity of V_{BUS}=60V, L=10µH, F_{SW}=400kHz

Table of Contents

4 Pin Configuration and Functions

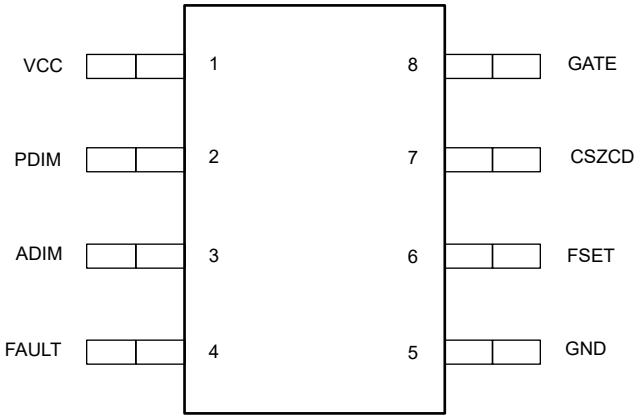


Figure 4-1. 8-Pin SOICTop View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	SOIC Package		
VCC	1	P	Analog controller bias input that provides power to the device. Includes an internal 15V(typical) startup bias that can connect to Vbus through a high-resistance path. Total VCC current is the sum of the quiescent VCC current and the average gate current.
PDIM	2	I	PWM dimming pin. Input a PWM signal for PWM dimming. Input a >1.2V pull-up voltage for pure analog dimming or shunt dimming. Pull down to ground to stop switching. Do not leave the pin floating.
ADIM	3	I	Analog dimming pin. Input a 0.2V~2.4V analog signal for analog dimming. Input a >2.4V and <2.8V pull up voltage for pure PWM dimming. Pull down to ground to disable the device for low-power standby mode. Do not leave the pin floating.
FAULT	4	O	Open-drain fault output with >2.4V pull up voltage. Can be configured via 1.2V~2.4V input to enable shunt dimming mode. Do not leave the pin floating, connect it to GND when not in use.
GND	5	G	Ground pin.
FSET	6	I	Switching frequency set pin for TPS922152. Connect a resistor to ground to configure the switching frequency.
CSZCD	7	I	Output current sense and zero-current detection pin. 200mV at full load current.
GATE	8	O	Gate drive pin for external switching FET.

(1) I = Input, O = Output, P = Supply, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VCC	–0.3	18	V
Voltage on pins	GATE	–0.3	VCC+0.3	V
Voltage on pins	FAULT	–0.3	20	V
Voltage on pins	PDIM, ADIM, FSET, CSZCD	–0.3	5.5	V
Operation junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VCC	4.5	15	V
Output voltage range	FAULT	0	20	V
Output voltage range	GATE	0	VCC+0.3	V
Input voltage range	PDIM, ADIM, CSZCD, FSET	0	5	V
Operation junction temperature	T_J	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS922152 SOIC 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.9	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics*application report, SPRA953.

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +125°C, V_{VCC} = 15 V, V_{BUS} = 60 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VCC_CLAMP}	VCC clamp voltage	I_{CC} = 10mA, ADIM = 0V		15	18	V
V_{VCC_UVLO}	VCC undervoltage lockout	Rising V_{VCC}	3.65	3.85	4.1	V
		Falling V_{VCC}	3.5	3.65	3.8	V
	Hysteresis			0.3		V
I_{OFF}	ADIM off quiescent current from VCC(1)	V_{GATE} = 0V, ADIM = 0V, T_J = 25°C		93		µA
FEEDBACK AND ERROR AMPLIFIER						
I_{LEAK_CS}	CSZCD pin leakage current	V_{CS} = 200 mV			1	µA
DIMMING						
V_{PWM_L}	Low-level input voltage		0.58	0.68	0.74	V
V_{PWM_H}	High-level input voltage		0.98	1.12	1.19	V
V_{ADIM}	DIM input voltage range		0.2		2.4	V
$V_{ADIM\_UVLO\_rising}$	Device enable voltage by ADIM			0.18	0.2	
$V_{ADIM\_UVLO\_falling}$	Device disable voltage by ADIM			0.16	0.18	V
$V_{ADIM\_high\_clamp}$	ADIM internal clamp voltage			2.8		V
$t_{PWM\_IN\_ON}$	PWM input minimum on time(1)				50	ns
CURRENT LIMIT						
G_{cs}	Current sense amplifier gain		10	10.9	11.8	
V_{CS_LIM}	CS cycle-by-cycle current limit	Measured from CS to GND	335	351	365	mV
V_{CS_OCP}	CS overcurrent protection	Measured from CS to GND	322	435	505	mV
V_{CS_OVP}	CS overvoltage protection	Measured from CS to GND	520	545	570	mV
GATE DRIVER						
V_{GATE-H}	GATE high saturation	V_{VCC} = 15V, I_{GATE} = 100mA source	14.2	14.7		V
V_{GATE-L}	GATE low saturation	V_{VCC}= 15V, I_{GATE} = 100mA sink		140	280	mV
t_{ON_MIN}	Minimum on time(1)			130		ns
t_{ON_MAX}	Maximum on time(1)			50		µs
t_{OFF_MIN}	Minimum off time(1)			150		ns
t_{OFF_MAX}	Maximum off time(1)			40		µs
FAULT						
V_{OL}	Output level low	I_{FAULT} = 1 mA			0.1	V
$I_{LEAKAGE}$	Output leakage current	V_{FAULT} = 20 V			1	µA
THERMAL PROTECTION						
T_{TSD}	Thermal shutdown temperature(1)			165		°C
T_{TSD}	Hysteresis			15		°C

(1) Not production tested. Specified by correlation by design.

5.6 Typical Characteristics

V_{VCC} = 15V, V_{BUS} = 60V, LED = 16, unless otherwise specified

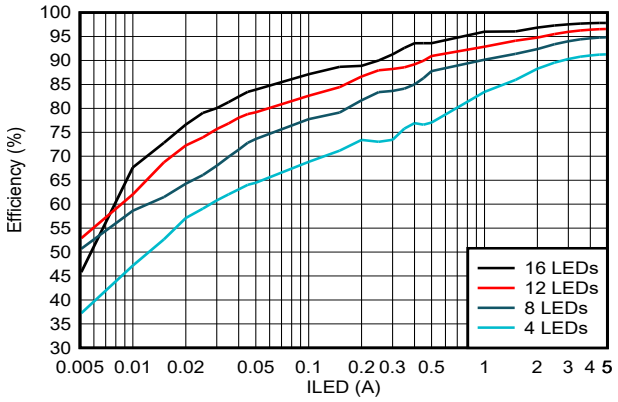


Figure 5-1. Efficiency at 5A Full Loading Output Current, 10µH Inductor, 60V Input Voltage

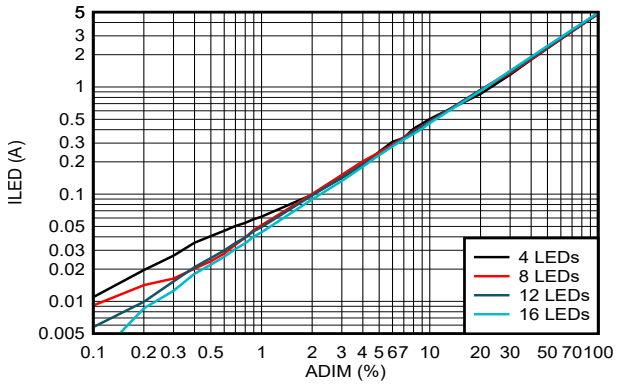


Figure 5-2. ADIM Ratio vs. Output Current

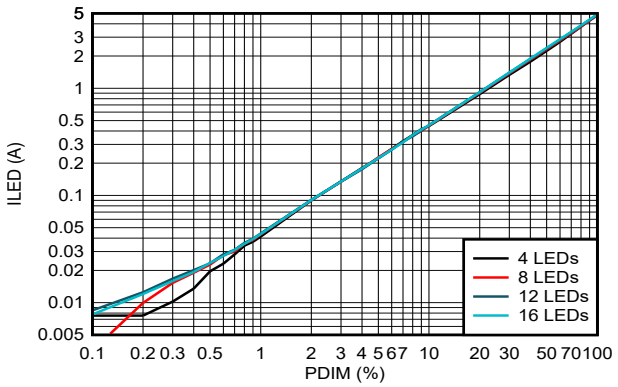


Figure 5-3. Output Current vs. 20kHz PDIM Duty Cycle

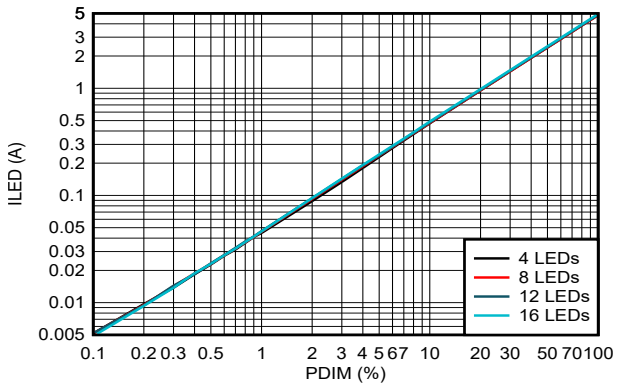


Figure 5-4. Output Current vs. 1kHz PDIM Duty Cycle

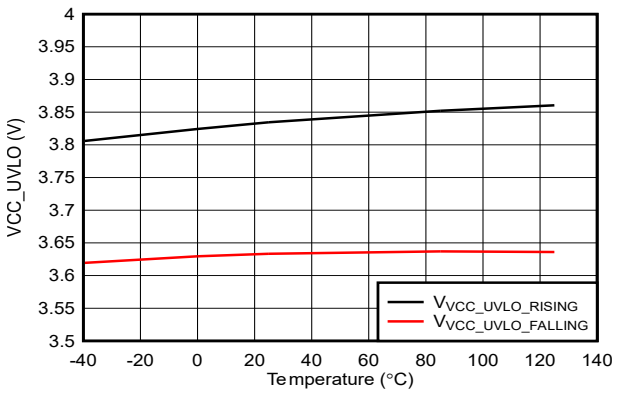


Figure 5-5. VCC UVLO rising vs. Junction Temperature

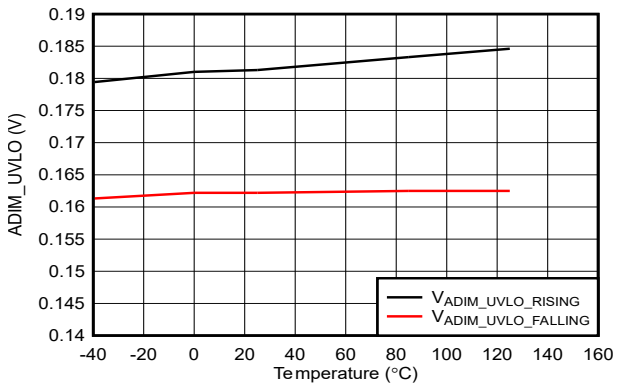


Figure 5-6. ADIM UVLO vs. Junction Temperature

6 Detailed Description

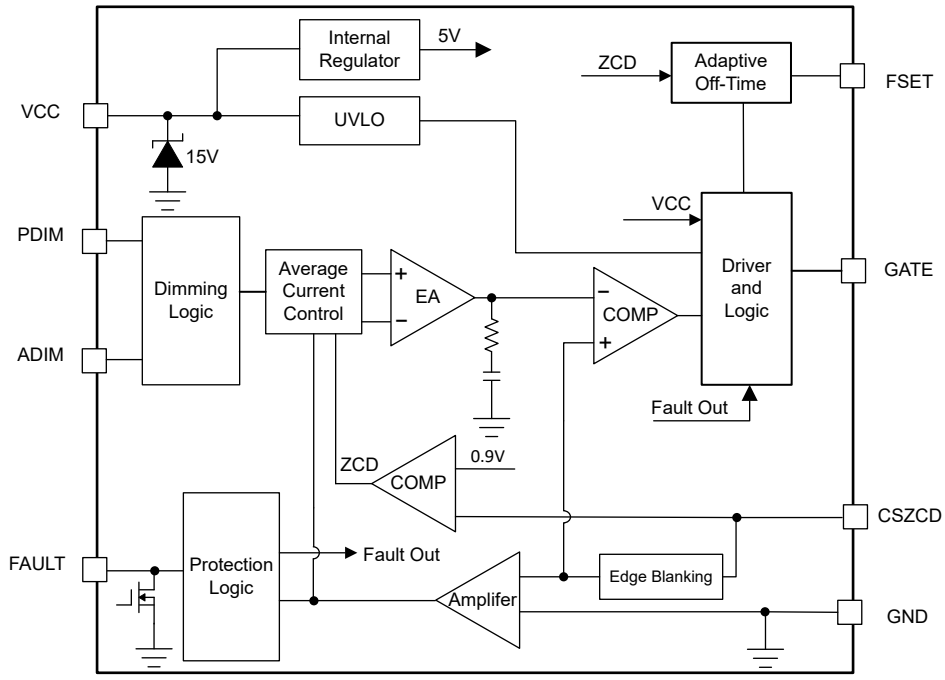
6.1 Overview

The TPS922152 as a non-synchronous Average-Current control Buck LED driver provides the features necessary to implement Adaptive Off-Time (AOT) control schemes with a minimum number of external components. The TPS922152 is capable of driving external switching FETs with wide input voltage range. The switching frequency is configurable through FSET pin, ranging from 50kHz-1MHz. With quasi constant frequency, it allows low LED current ripple and fast transient response with small output capacitors . Furthermore, the switching frequency is folded back at light load for higher efficiency and higher dimming ratio with common anode connection.

The TPS922152 support both analog dimming and PWM dimming. It provides wide analog dimming down to 0.1% with high-accuracy by configuring analog signals through the ADIM input pin. The TPS922152 is able to measure the current of LED load connected at input voltage node without the upper limit of the input voltage with high system reliability. High analog dimming ratio is achievable by the unique corrective sensing function. The device also provides high-frequency and high-ratio PWM dimming by configuring simple high and low signals through the PDIM input pin. The output current is regulated in PWM shape corresponding to on and off input signal at PDIM pin. Due to the unique inductive fast dimming (IFD), the device is capable of responding to an ultra-narrow pulse width input signal down to 50ns for a high PWM dimming ratio. The TPS922152 is internally compensated, which reduces design time and requires few external components. The device is also capable of supplying constant current continuously to support shunt dimming where the LED output is periodically shorted.

For safety and protection, the TPS922152 supports full systematic protections with hiccup mode including LED open and short, sense resistor open and short, switching FET open protection. The open-drain FAULT pin can send out the fault signal by connecting to a pull-up resistor. The input voltage is clamped at 15V(typical) to protect the gating voltage from exceeding the limit. The device can be supplied through an individual source or an RC circuit from the input bus voltage.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Adaptive Off-Time Mode

The TPS922152 adopts an adaptive off-time current-mode control with quasi-constant frequency to maintain accurate current regulation and fast transient response over a wide load range.

For accurate output current regulation, the voltage sensed across the sense resistor via the CSZCD pin and ground is amplified and averaged to generate a voltage proportional to the output current. This sensed voltage is then compared, through the error amplifier, to the filtered ADIM voltage, which serves as the reference. The error voltage generated by the error amplifier regulates the PWM duty cycle, thereby enabling the output current to track the ADIM voltage. During each switching cycle, when the switching FET is turned on, the current is sensed through the CSZCD pin. The error amplifier output, V_{COMP}, passes through an internal compensation network and is compared to the rising edge of the sensed current. When the sensed current reaches V_{COMP} at the PWM comparator input, the switching FET is turned off to set the peak current.

An off-time counter begins counting immediately after the switching FET is turned off. The counting off time corresponding to a switching frequency is determined by the external resistor connected to the FSET pin. Once the off-time counter reaches the target, the off-time counter is reset and remains inactive until the next switching cycle begins. This mechanism allows the device to maintain a nearly constant switching frequency in both steady-state CCM and DCM. By connecting an external resistor between FSET pin and ground, the switching frequency can be set in the range of 50kHz to 1MHz. The resistor value and the corresponding switching frequency can be calculated using Equation 1

$$F_{SW} = \frac{1}{R_{FSET} \times C_{FSET}} \quad (1)$$

where

- C_{FSET} = 100pF

Under light-load conditions, the device scales the peak current in proportion to the load. To maintain accurate regulation, the off-time is dynamically extended via Pulse Frequency Modulation (PFM). To maintain stability and prevent audible noise, the switching frequency is clamped at a minimum of 20kHz.

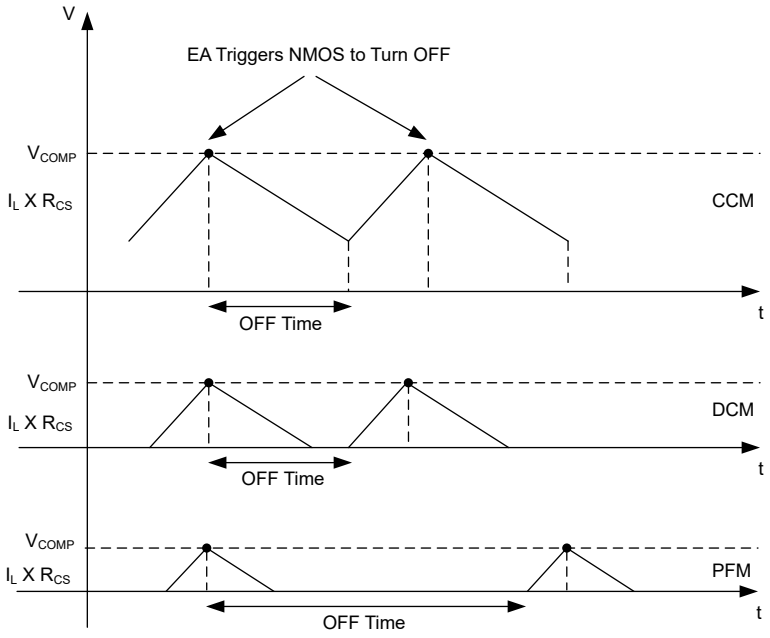


Figure 6-1. AOT mode average-current control

6.3.2 Setting LED Current

The LED current is set by the external sensing resistor R_{CS} between the switching FET source and ground. An internal circuit averages the current through R_{CS} during the main FET on-time to derive the effective LED current. The amplified and averaged voltage across the current-sense terminals, combined with the internal offset voltage, corresponds to the applied ADIM voltage. If the applied ADIM voltage exceeds 2.8V, the internal circuit clamps the error amplifier input to 2.8V. The full scale of LED current I_{LED_FS} can be caculated directly using Equation 2.

$$I_{LED\_FS} = \frac{V_{ADIM} - 0.2}{R_{cs} \times G_{cs}} \quad (2)$$

where

- V_{ADIM} is applied ADIM voltage
- G_{cs} is gain of current amplifier

The switching FET source is connected to the CSZCD pin via a switch-node voltage divider for current sense and zero current detection(ZCD). When the CSZCD pin voltage falls below the 0.9V threshold, the device identifies the entry into zero-current mode. To ensure reliable ZCD operation, the voltage divider ratio must satisfy

$$V_{BUS} \times \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} > 0.9V \quad (3)$$

$$V_{LED-} \times \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} < 0.9V \quad (4)$$

where V_{LED-} is the LED cathode voltage. R_{ZCD1} and R_{ZCD2} is recommended to be between 1kΩ and 1MΩ to reduce the noise as well as keep LED leakage current.

Considering the current sensing mismatch due to the voltage divider, the corrected sensing resistor can be calculated using Equation 5

$$R_{cs} = \frac{V_{ADIM} - 0.2}{I_{LED} \times G_{cs}} - \frac{R_{DS(ON)} \times R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} \quad (5)$$

6.3.3 VCC UVLO & Clamping

The TPS922152 features an internal undervoltage-lockout (UVLO) circuit connecting to the VCC pin. The device is disabled when the VCC voltage falls below the internal 3.8V(typical) UVLO threshold, with a 0.3V(typical) hysteresis voltage.

Additionally, an internal Zener clamping circuit is connect to VCC pin to limit the voltage on both VCC and GATE pins. The Zener begins to shunt current once the VCC voltage exceeds the 15V(typical) clamping threshold, with a maximum Zener current of approximately 20mA. The device can be powered by an external voltage source(≤15V), such as an LDO or auxiliary transformmer winding.

Alternatively, an $R_{IN1}C_{VCC}$ circuit can be used to power the device directly from the input bus voltage (VBUS). With the $R_{IN1}C_{VCC}$ circuit, the VCC pin is clamped to V_{VCC_CLAMP}, though a lower voltage can be achieved by adding an optional R_{IN2} voltage divider. An optional gate resistor, R_{GATE}, may also be used to limit gate current and reduce the switching slew rate.

TI recommends a specific power-up/down sequencing: ensure VBUS is stable before powering up VCC, and power off VCC before powering off VBUS

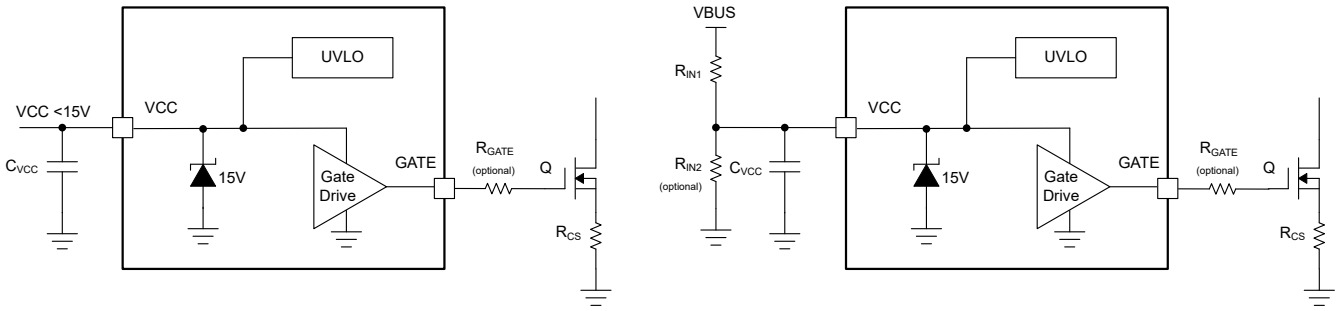


Figure 6-2. VCC Power Supply and Clamping

6.3.4 Dimming Mode

The TPS922152 provides flexible dimming capabilities, include analog dimming, PWM dimming, flexible dimming, and shunt dimming modes. By applying singals to both the ADIM and PWIM pins simultaneously, the device operates in flexible dimming mode. The dimming mode settings are outlined below:

Table 6-1. Dimming Mode Configuration

Dimming Mode	DIM Pin	Input Signal
PWM Dimming	PDIM	PWM Voltage
Analog Dimming	ADIM	Analog Voltage
Flexible Dimming	PDIM + ADIM	PWM Voltage + Analog Voltage
Shunt Dimming	FAULT	Voltage Divider

6.3.4.1 PWM Dimming

PWM dimming is enabled by applying a PWM signal to the PDIM pin. To support high dimming ratios, the TPS922152 accommodates ultra-narrow PWM pulses with widths as narrow as 50ns.

In PWM mode, a rising edge on the PDIM signal initiates switching, causing the inductor current to ramp up to the target level. The LED current is regulated at this level for the duration of the PWM high period. Upon a falling edge of the PDIM signal, the switching FET is turned off, allowing the inductor current to decay to zero. The FET remains in an off-state, and the LED current remains at zero during the PWM low period.

6.3.4.2 Analog Dimming

The TPS922152 supports analog dimming which regulates the LED current through the analog voltage signal at the ADIM pin.

The device operates in a low-power standby mode with minimal quiescent current when the ADIM voltage is below 0.18V (typical). Operation initiates once the ADIM voltage exceeds 0.18V (typical). As the ADIM voltage scales from 0.2V to 2.8V (typical), the LED current varies proportionally according to Equation 2. For ADIM voltages exceeding 2.8V (typical), the internal voltage is clamped at 2.8V (typical) via an RC filter (R=2MΩ, C=10pF); consequently, the LED current remains constant and does not increase further with rising ADIM voltage.

6.3.4.3 External Shunt Dimming

The TPS922152 supports external shunt-dimming by connecting a shunt MOSFET in parallel with the LED string. In this mode the shunt MOSFET periodically shorts the LEDs at the programmed dimming frequency, forcing the LED voltage to drop to near 0 V during each bypass interval. If the shunt MOSFET is disabled while the LEDs are shorted, the device interprets the condition as an LED-short fault. Therefore, when shunt-dimming is enabled, the FAULT pin is intentionally biased to a voltage between **1.2 V and 2.4 V** during a short-circuit event, preventing the short-circuit protection from triggering.

By connecting the FAULT pin to the LED cathode via a voltage divider, the FAULT pin voltage stays within the 1.2V and 2.4V range during the shunt FET conduction period and falls below 1.2V during the FET off-state. This configuration maintains the shunt dimming mode and prevents the activation of LED short-circuit protection, allowing the device to provide continuous output current regulation. Other protection features remain active, and any other fault condition pulls the FAULT pin low. The required voltage divider ratio for shunt dimming can be calculated using Equation 6

$$\frac{R_{SHNT1}}{R_{SHNT2}} > \frac{MAX\left(0.5 \times V_{BUS\_MAX}, V_{BUS\_MAX} - V_{LED\_MIN}\right)}{V_{SHNT}} - 1 \quad (6)$$

where

- V_{SHNT} = 1.2V

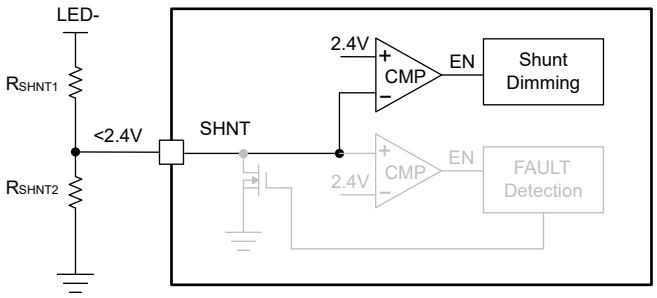


Figure 6-3. Shunt Dimming Mode Enable Setting

6.3.5 Fault Protection

The TPS922152 provides comprehensive fault protection and reports status by asserting the open-drain FAULT pin under various fault conditions, including: LED open/short, LED short to PGND, sense resistor open/short, and switching FET open. Upon detecting a fault, the device immediately suspends switching operations and enters a "hiccup" mode, attempting to restart every 1.6 seconds. The device will fully recover once the fault condition is cleared. However, if V_{CS} exceeds the Overvoltage Protection (V_{CS_OVP}) threshold, the device is disabled immediately without entering hiccup mode; it will only resume operation following a UVLO and restart sequence, provided the fault has been removed.

Table 6-2. Protections

TYPE	CRITERION	BEHAVIOR
LED open load	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.
LED+ and LED- short circuit during switching operation (shunt dimming mode is disabled)	$V_{CS} > V_{CS\_OVP}$	The device stops switching. It recovers after UVLO and restart with fault removed.
LED- short to PGND	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.
Sense-resistor open circuit	$V_{CS} > V_{CS\_OVP}$	The device stops switching. It recovers after UVLO and restart with fault removed.
Sense-resistor short circuit	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.
Switching FET open circuit	$t_{ON} > t_{ON\_MAX}$	The device stops switching. It hiccups every 1.6s and recovers when fault is removed.

The FAULT pin features an open-drain output, During normal operation, the pin is pulled up to VCC higher than 2.4V via a pull-up resistor, R_{FAULT}. Upon detection of a fault, the internal MOSFET activates, pulling the FAULT pin to ground. When FAULT is not used, please connect it to GND and do not let it floating.

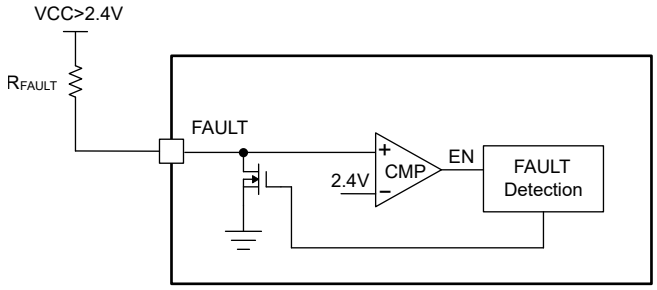


Figure 6-4. FAULT Open Drain

7 Application and Implementation

7.1 Application Information

The TPS922152 is an Average-Current control Buck controller designed to drive one or more LEDs from an input ranging from 4.5V to 200V.

7.2 Typical Application

7.2.1 TPS922152 60V Input Bus, 5A Output, 16-piece WLED With Analog and PWM Dimming

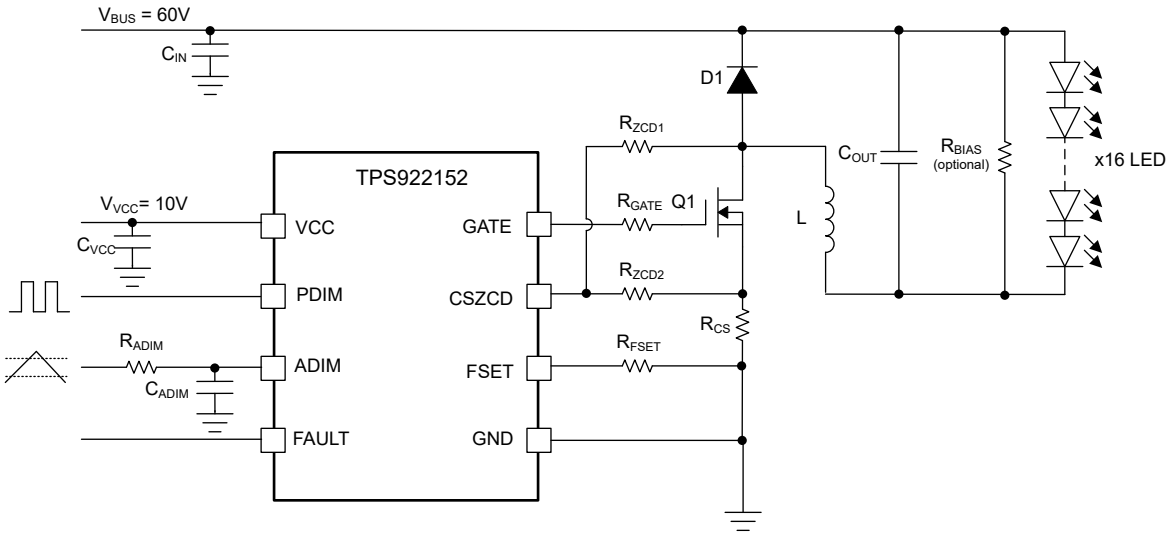


Figure 7-1. 60V Input Bus, 5A Output, 16-piece WLED, Buck AOT Mode Reference Design

7.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input bus voltage range	60V ±10%
LED forward voltage	3.0V
Switching Frequency	400kHz
Output voltage	48V (3.0V × 16)
Maximum LED current	5A
Inductor current ripple	60% of maximum inductor current
LED current ripple	100mA or less
Dimming type	Analog dimming: 0.2V to 2.4V analog input at the ADIM pin; PWM dimming: 0% to 100% PWM input at the PDIM pin

Component Specs

- L = 10µH
- C_{VCC} = 1µF
- C_{IN} = 22µF
- C_{OUT} = 3.3µF
- R_{FSET} = 25kΩ
- R_{ZCD1} = 105kΩ
- R_{ZCD2} = 2kΩ
- R_{CS} = 40mΩ
- R_{GATE} = 15Ω

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Inductor Selection

For this design, the input bus voltage is a 60V rail with 10% variation. The output is 16 white LEDs in series and the inductor current ripple by requirement is less than 60% of maximum inductor current. To ensure compliance, the low-side FET current limit must not be exceeded during full-load operation. Specifically, peak current of inductor must be lower than the current limit. Additionally, the ripple current should be optimized to maintain reasonable inductor core and copper losses. After determining the target ripple current, use Equation 7 to calculate the recommended value of the switching inductor L_{SW}.

$$L_{SW} = \frac{V_{LED} \times (V_{BUS\_MAX} - V_{LED})}{K_{IND} \times I_{LED\_MAX} \times F_{SW} \times V_{BUS\_MAX}} \quad (7)$$

where

- K_{IND} is a coefficient that represents the ratio of inductor ripple current to the maximum inductor current.
- I_{LED_MAX} is the maximum LED current.
- F_{SW} is the switching frequency.
- V_{BUS_MAX} is the maximum input bus voltage.
- V_{LED} is the sum of the voltage across LED load.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 8.

$$I_{L\_RIP} = \frac{V_{LED} \times (V_{BUS\_MAX} - V_{LED})}{L_{SW} \times F_{SW} \times V_{BUS\_MAX}} \quad (8)$$

To ensure reliable operation, the inductor's rated RMS current I_{L_RMS} and saturation current I_{L_SAT} must meet or exceed the maximum current levels defined by the system requirements. This prevents inductor overheating and magnetic saturation. During power-up, transient events, or fault conditions, the inductor current may surge beyond normal operating levels and approach the converter's current limit. To account for these surges, it is recommended to select an inductor with a saturation current I_{L_SAT} equal to or greater than the converter's current limit. The equations for peak inductor current I_{L_PEAK} and RMS current I_{L_RMS} are provided in Equation 9 and Equation 10, respectively.

$$I_{L\_PEAK} = I_{L\_MAX} + \frac{I_{L\_RIP}}{2} \quad (9)$$

$$I_{L\_RMS} = \sqrt{{I_{L\_MAX}}^2 + \frac{{I_{L\_RIP}}^2}{12}} \quad (10)$$

In this design, V_{BUS_MAX} = 66V, V_{LED} = 48V, I_{LED} = 5A, F_{SW} = 400kHz, select K_{IND} = 0.6, the calculated switching inductance is 10.9µH. Select the closest standard 10µH ferrite inductor with an I_{L_RMS} of 9.4A and an I_{L_SAT} of 12.7A. A 10µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 3.2A, 6.6A, and 5A, respectively.

7.2.1.2.2 MOSFET Selection

The TPS922152 requires an external MOSFET (Q1) to serve as the main power switch for the regulator. The selection of the MOSFET involves balancing conduction losses, switching losses, and gate-drive losses. The conduction loss is given by Equation 11

$$P_{DC} = D \times \left(I_{LED\_MAX}^2 + \frac{I_{L\_RIP}^2}{12} \right) \times R_{DS(ON)} \times 1.3 \quad (11)$$

where

- D is the duty cycle.

- I_{LED_MAX} is the maximum LED current
- I_{L_RIP} is the inductor ripple current

The factor 1.3 accounts for the temperature-dependent increase in $R_{DS(ON)}$. Alternatively, for a more precise calculation, the factor of 1.3 can be ignored and the on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs Temperature curves in the MOSFET datasheet.

The switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_{LED} \times (t_R + t_F) \times f_{SW} \quad (12)$$

where

- t_R is the rise time of the MOSFET
- t_F is the fall time of the MOSFET

The rise and fall times are typically mentioned in the MOSFET datasheet or can be empirically observed on the scope.

Gate charging loss results from the drive current charging the MSOFET gate capacitance from VCC. To minimize both switching and gate-drive losses, a MOSFET with low Q_g can be selected. The gate drive loss can be approximated as:

$$P_{GC} = VCC \times Q_g \times f_{sw} \quad (13)$$

where

- Q_g is gate charge.

For this example with the maximum input voltage of 66V, the V_{DS} breakdown rating of the selected MOSFET must be greater than 66V, plus any ringing across drain to source due to parasitics. To minimize switching time and gate drive losses, the selected MOSFET must also have low gate charge (Q_g). A good choice of MOSFET for this design example is the CSD19534Q5A which has a total gate charge of 17 nC and 12.6mohm Rdson

An input capacitor is required to reduce the surge current drawn from the gate driver. In this design, a 1µF, 25V X7R ceramic capacitor and a 0.1µF, 50V X7R ceramic capacitor are chosen.

7.2.1.2.3 Diode Selection

A Schottky diode is required for all TPS922152 applications. Schottky diodes are preferred due to excellent reverse recovery characteristics and low forward voltage drop, which are critical for high-input-voltage and low-output-voltage applications. The diode switching loss is minimized in a Schottky diode by the fast reverse recovery. The conduction loss can be approximated by Equation 14

$$P_{DC\_diode} = (1 - D) \times I_{LED\_MAX} \times V_F \quad (14)$$

where

- V_F is the forward drop of the diode.

In the worst-case scenario, a short-circuit load condition is assumed, where the diode carries the output current almost continuously. The reverse breakdown voltage rating must be selected to exceed the maximum input voltage, including an additional safety margin to withstand ringing at the SW node. For this application, a 150V Schottky diode (V15PM53-M3/I) with a specified forward voltage of 0.6V at 5A (at a junction temperature of 25°C) is selected. For output loads of 5A or greater in high-input-voltage applications, a diode in a TO-277A package is recommended to support the worst-case power dissipation.

7.2.1.2.4 MOSFET Selection

The TPS922152 requires an external MOSFET (Q1) to serve as the main power switch for the regulator. The selection of the MOSFET involves balancing conduction losses, switching losses, and gate-drive losses. The conduction loss is given by Equation 15

$$P_{DC} = D \times \left(I^2_{LED\_MAX} + \frac{I^2_{L\_RIP}}{12} \right) \times R_{DS(ON)} \times 1.3 \quad (15)$$

where

- D is the duty cycle.
- I_{LED_MAX} is the maximum LED current
- I_{L_RIP} is the inductor ripple current

The factor 1.3 accounts for the temperature-dependent increase in $R_{DS(ON)}$. Alternatively, for a more precise calculation, the factor of 1.3 can be ignored and the on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs Temperature curves in the MOSFET datasheet.

The switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_{LED} \times (t_R + t_F) \times f_{SW} \quad (16)$$

where

- t_R is the rise time of the MOSFET
- t_F is the fall time of the MOSFET

The rise and fall times are typically mentioned in the MOSFET datasheet or can be empirically observed on the scope.

Gate charging loss results from the drive current charging the MSOFET gate capacitance from VCC. To minimize both switching and gate-drive losses, a MOSFET with low Q_g can be selected. The gate drive loss can be approximated as:

$$P_{GC} = VCC \times Q_g \times f_{sw} \quad (17)$$

where

- Q_g is gate charge.

For this example with the maximum input voltage of 66V, the V_{DS} breakdown rating of the selected MOSFET must be greater than 66V, plus any ringing across drain to source due to parasitics. To minimize switching time and gate drive losses, the selected MOSFET must also have low gate charge (Q_g). A good choice of MOSFET for this design example is the CSD19534Q5A which has a total gate charge of 17 nC and 12.6mohm Rdson

An input capacitor is required to reduce the surge current drawn from the gate driver. In this design, a 1µF, 25V X7R ceramic capacitor and a 0.1µF, 50V X7R ceramic capacitor are chosen.

7.2.1.2.5 Diode Selection

A Schottky diode is required for all TPS922152 applications. Schottky diodes are preferred due to excellent reverse recovery characteristics and low forward voltage drop, which are critical for high-input-voltage and low-output-voltage applications. The diode switching loss is minimized in a Schottky diode by the fast reverse recovery. The conduction loss can be approximated by Equation 18

$$P_{DC\_diode} = (1 - D) \times I_{LED\_MAX} \times V_F \quad (18)$$

where

- V_F is the forward drop of the diode.

In the worst-case scenario, a short-circuit load condition is assumed, where the diode carries the output current almost continuously. The reverse breakdown voltage rating must be selected to exceed the maximum input voltage, including an additional safety margin to withstand ringing at the SW node. For this application, a 150V Schottky diode (V15PM53-M3/I) with a specified forward voltage of 0.6V at 5A (at a junction temperature of 25°C) is selected. For output loads of 5A or greater in high-input-voltage applications, a diode in a TO-277A package is recommended to support the worst-case power dissipation.

7.2.1.2.6 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise generated by the device. Electrolytic capacitors are recommended for energy storage. These capacitors also provide parallel damping to mitigate resonance caused by the parasitic inductance of the supply lines and high-Q ceramics capacitors.

Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and stable temperature coefficients. For most applications, a combination of a 10µF or 22µF ceramic capacitor along and a 0.1µF capacitor should be placed between VIN and PGND to provide effective high-frequency filtering. Ensure that the input capacitor's voltage rating exceeds the maximum input voltage. The bus voltage ripple can be approximated as:

$$V_{BUS(ripple)} = I_{LED\_MAX} \times \left(\frac{V_{LED}}{C_{IN} \times f_{SW} \times V_{BUS\_MAX}} + R_{ESR\_IN} \right) \quad (19)$$

where

- R_{ESR_IN} is the ESR of input capacitor
- C_{IN} is derated capacitance in V_{BUS_MAX}

In this design, a 22µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen.

7.2.1.2.7 Output Capacitor Selection

The output capacitor is critical for minimizing high-frequency current ripple in the LED string. Excessive ripple increases the RMS current within the LEDs, leading to elevated junction temperatures and reduced lifespan. To ensure optimal performance, follow these design steps:

1. **Determine LED Dynamic Resistance R_{LED}**:Obtain the total dynamic resistance of the LED string from the LED manufacturer's datasheet.

2. **Define Target Ripple Current :** Determine the maximum acceptable peak-to-peak ripple current through the LED string I_{LED_RIP}.

3. **Calculate Required Impedance Z_{COUT}:** Using the target I_{LED_RIP} and the peak-to-peak inductor ripple current I_{L_RIP}, calculate the required output capacitor impedance.

given the acceptable peak-to-peak ripple current through the LED string, I_{LED_RIP} . I_{L_RIP} is the peak-to-peak inductor ripple currentI_{L_MAX} is the inductor maximum current as calculated with the selected inductor.

4. **Calculate Minimum Capacitance C_{OUT_MIN}**:Derive the minimum effective output capacitance required to meet the impedance target.

5. **Account for DC Bias Derating:** Increase the nominal capacitance value to compensate for the DC bias derating effect common in ceramic capacitors at the operating voltage.

Refer Equation 20, Equation 21, and Equation 22 for detailed calculation formulas.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \text{ \# of LEDs} \quad (20)$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED\_RIP}}{I_{L\_RIP} - I_{LED\_RIP}} \quad (21)$$

$$C_{OUT} = \frac{1}{2\pi \times F_{SW} \times K_{DR} \times Z_{COUT}} \quad (22)$$

Once the output capacitor is chosen, Equation 23 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED\_RIP} = \frac{Z_{COUT} \times I_{L\_RIP}}{Z_{COUT} + R_{LED}} \quad (23)$$

CREE WLED is used here. The dynamic resistance of the LED is 0.67Ω at 3A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. In this design, a 3.3µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 100mA.

7.2.1.2.8 Sense Resistor Selection

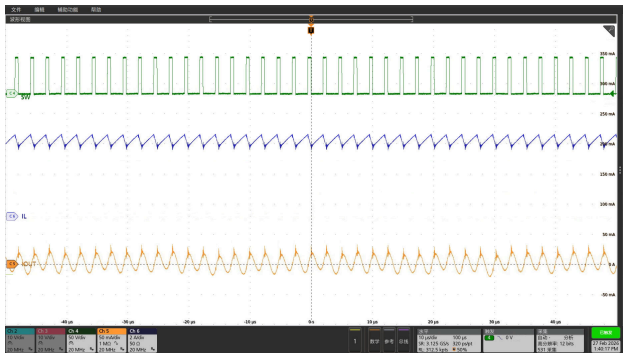
For a maximum LED current of 5A at 2.4V ADIM input, the voltage divider resistor R_{ZCD1} and R_{ZCD2} are selected as 105kΩ and 2kΩ. By using Equation 5, the sense resistance is calculated as 40mΩ.

Note that the power dissipation of the sense resistor is 1W, requiring an adequate margin of the resistor's power rating in selection.

7.2.1.2.9 Other External Components Selection

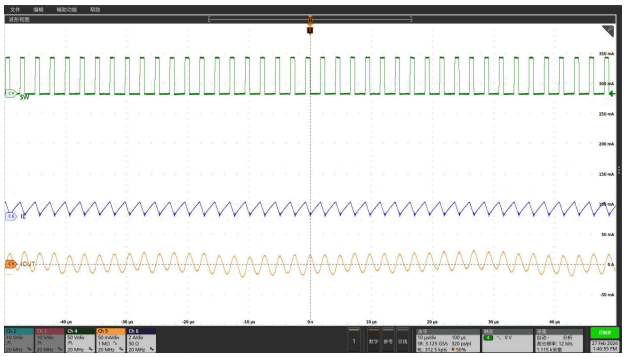
In this design, a 15Ω resistor R_{GATE} is chosen between GATE pin and the switching FET gate to limit the gate current and switching slew rate. A 25kΩ resistor is used to set 400kHz switching frequency.

7.2.1.3 Application Curves



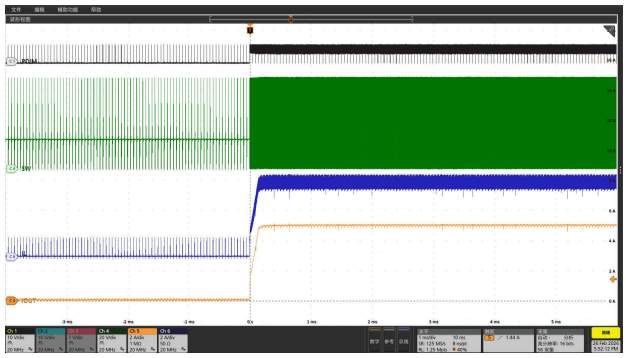
Green: SW, Blue: Inductor Current, Orange: LED Current Ripple (AC)

Figure 7-2. LED Current Ripple at ADIM = 2.4V and F_{SW} = 400kHz



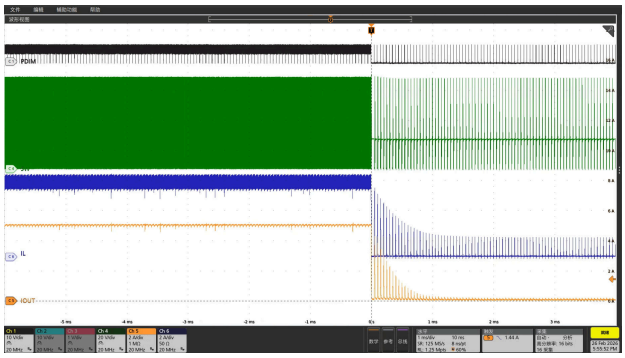
Green: SW, Blue: Inductor Current, Orange: LED Current Ripple (AC)

Figure 7-3. LED Current Ripple at ADIM = 0.42V and F_{SW} = 400kHz



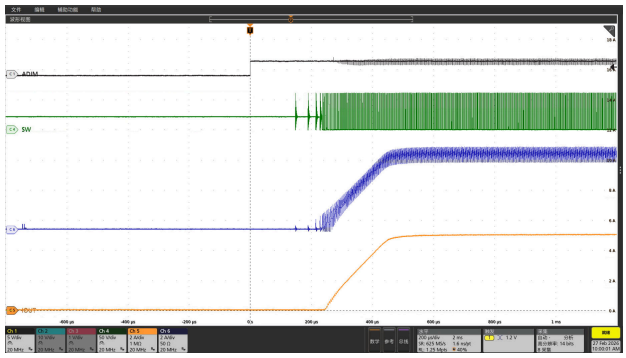
Black: PDIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-4. LED Current Transient for PDIM Transition from 1% to 99% @20kHz



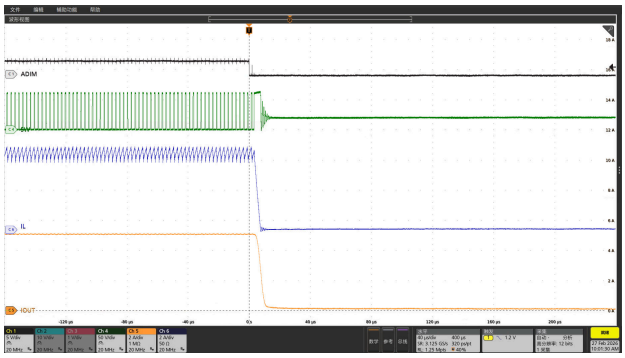
Black: PDIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-5. LED Current Transient for PDIM Transition from 99% to 1% @20kHz



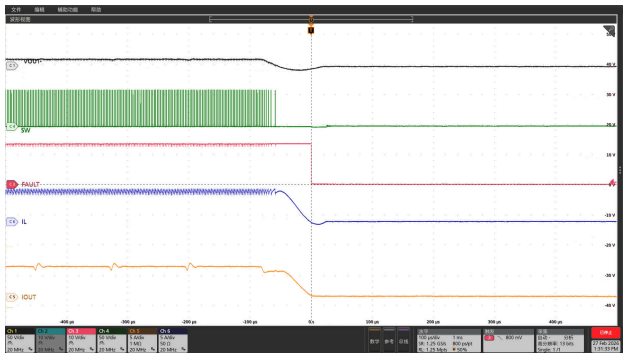
Black: ADIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-6. Start-Up at ADIM = 2.4V



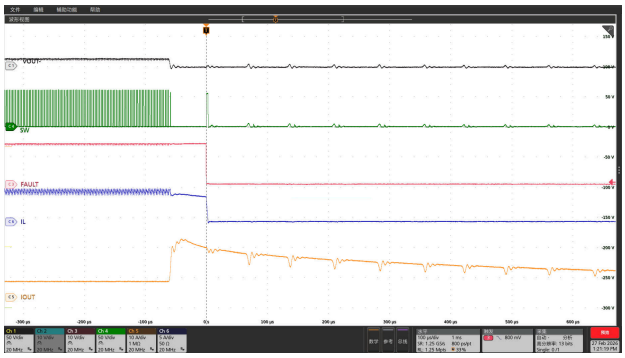
Black: ADIM, Green: SW, Blue: Inductor Current, Orange: LED Current

Figure 7-7. Shutdown at ADIM = 0V



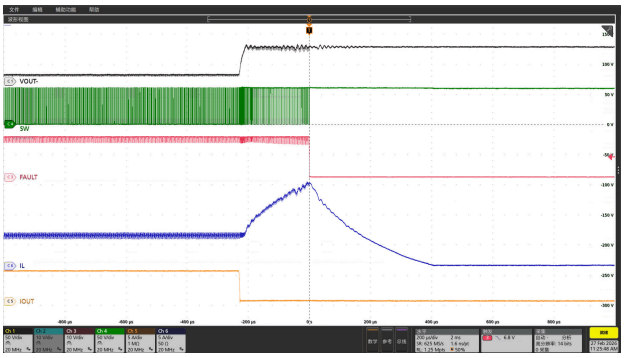
Black: VLED-, Green: SW, Red: FAULT, Blue: Inductor Current, Orange: LED Current

Figure 7-8. LED Open-Load Protection



Black: VLED-, Green: SW, Red: FAULT, Blue: Inductor Current, Orange: LED Current

Figure 7-9. LED– Short-to-PGND Protection



Black: VLED-, Green: SW, Red: FAULT, Blue: Inductor Current, Orange: LED Current

Figure 7-10. LED+ and LED– Short-Circuit Protection

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5V and 15V. This input supply must be well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 1µF or 2.2µF capacitor is enough.

7.4 Layout

The TPS922152 requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

7.4.1 Layout Guidelines

An example of a proper layout for the TPS922152 device is shown in Figure 7-11.

- **Thermal & Grounding**: Implement a large, continuous GND plane for superior electrical and thermal performance. Utilize thermal vias to create a low-impedance thermal path from the top-side GND to additional PCB layers.
- **Trace Impedance:**Minimize the impedance of VBUS , VLED+ and GND traces by maximizing their width, which also aids in heat dissipation.
- **Decoupling & Input:**To ensure stable operation, place the input capacitors C_{IN} and C_{VCC} in immediate proximity to their respective VBUS , VCC and GND pins.
- **Gate Drive:** The GATE trace must be minimized in length to reduce parasitic inductance, thereby preventing noise injection and reducing EMI.
- **Sensitive Signals:**The CSZCD trace is highly sensitive. It should be kept as short as possible and routed away from the high-voltage switching node (the junction of L, D1, and Q1) and any high di/dt paths to avoid interference.
- **Noise Isolation:**Ensure that high-frequency switching currents are not routed directly underneath the IC to prevent capacitive and inductive noise coupling into the device.

7.4.2 Layout Example

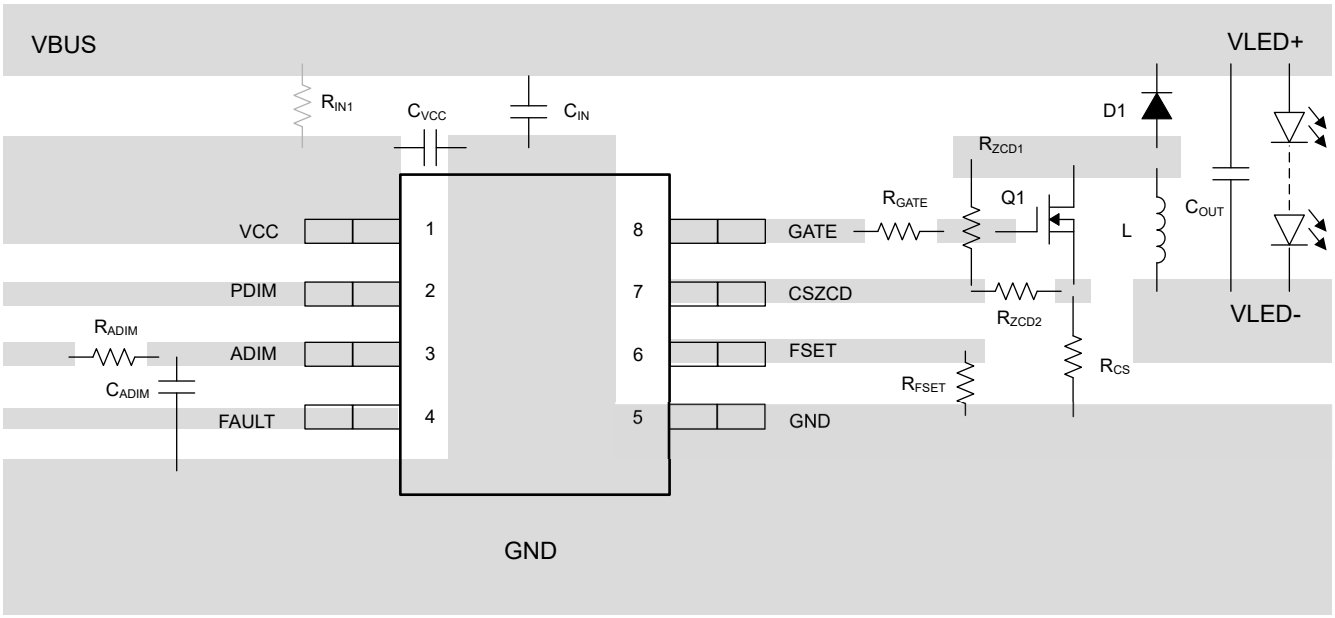


Figure 7-11. 8-Pin SOICTop View Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision * (March 2026) to Revision A (September 2026)	Page
• Updated device status from Advanced Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS922152DR	Active	Preproduction	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

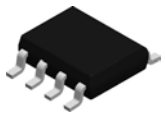
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

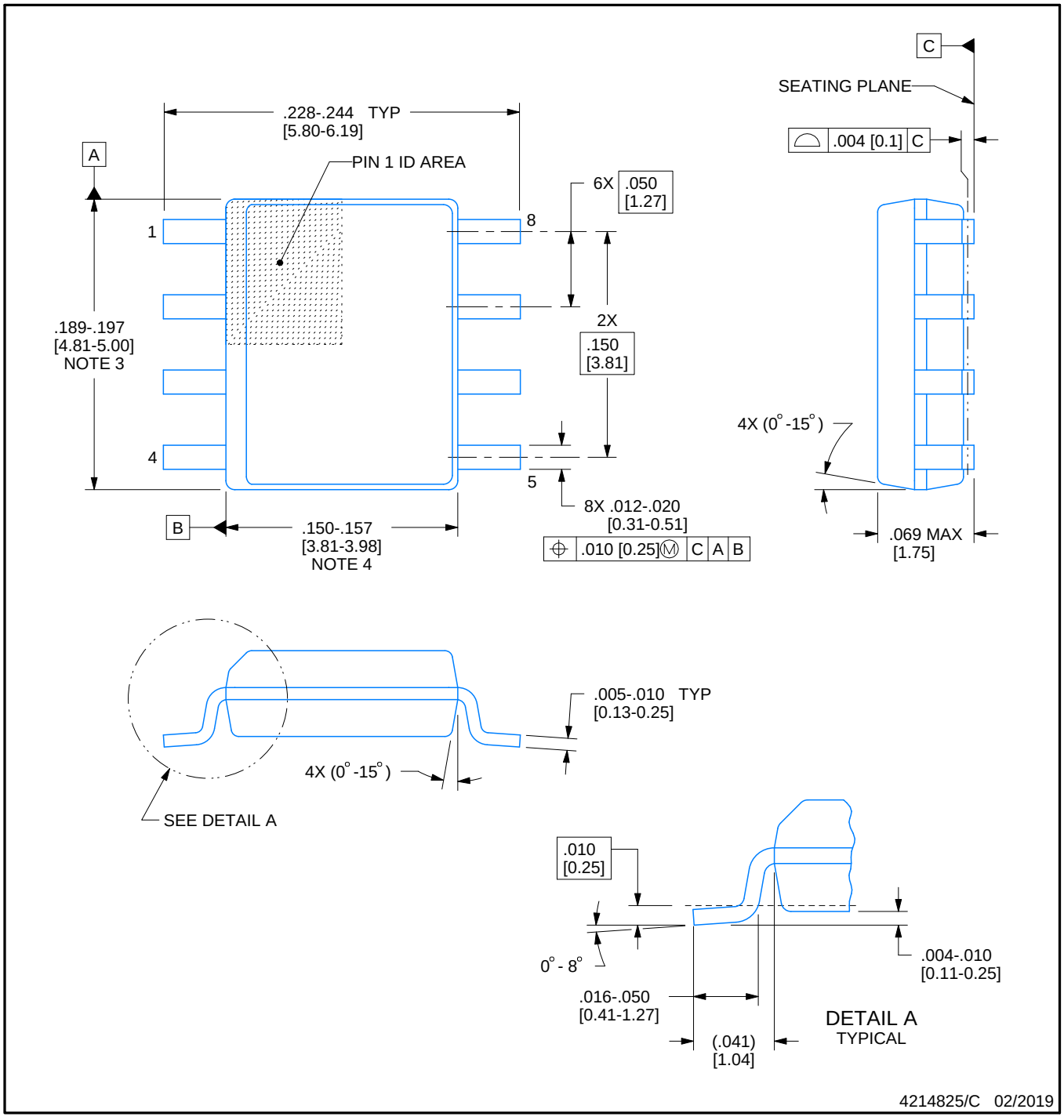


PACKAGE OUTLINE

D0008A

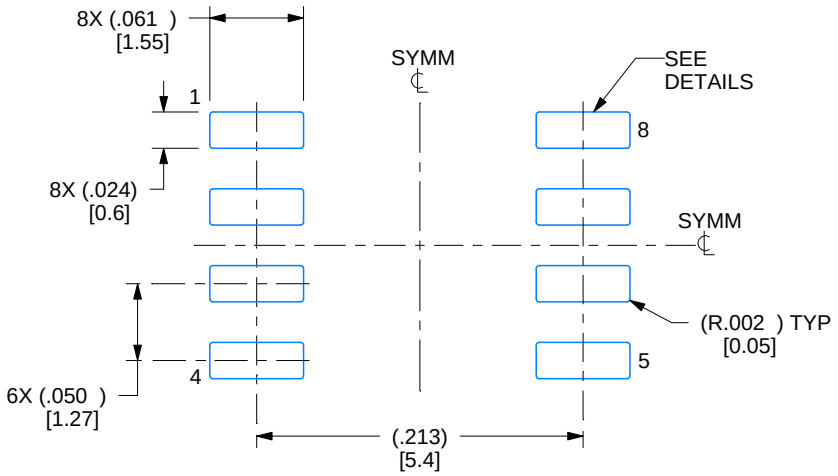
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

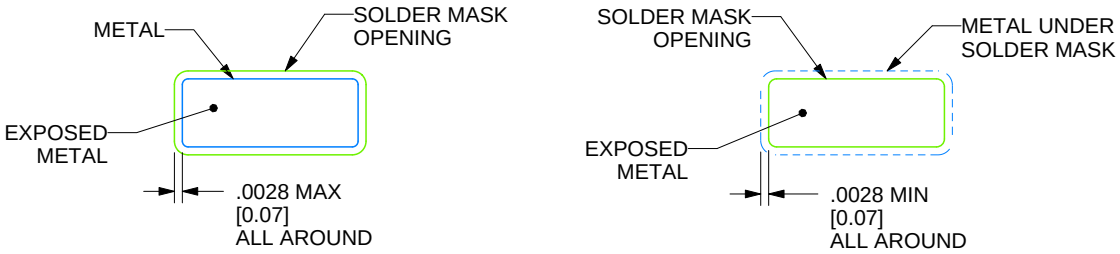


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

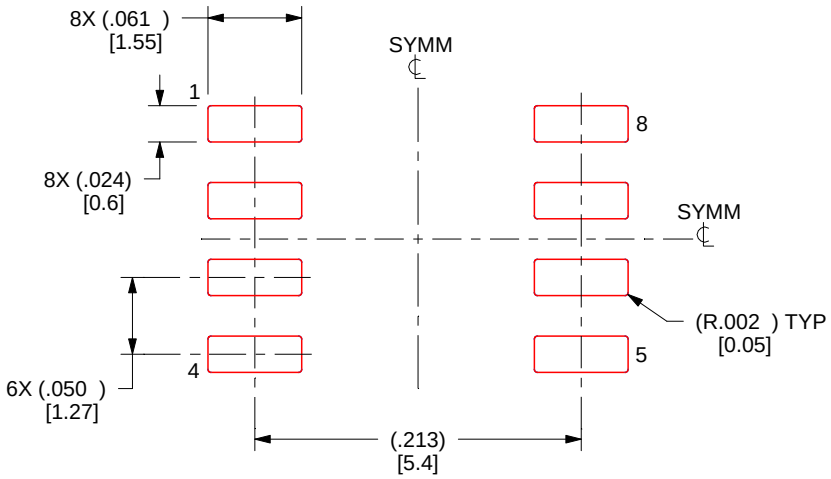
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025