TPSM265R1 65V 入力、100mA、超低 I_Q の電源モジュール

1 特長

- 広い入力電圧範囲：3V～65V
- 出力電圧オプション
  - 可変 1.223V～15V
  - 固定 3.3V または 5V
- 出力電流：100mA
- 静止電流：10.5µA
- 内部基準電圧精度：±1%
- PFM 動作モード
- -40℃～125℃の周囲温度範囲
- アクティブ・スルーレート制御による EMI 低減
- CISPR11 (EN55011) EMI 規格に準拠
- あらかじめ出力にバイアスが印加された状態でも単調にスタートアップ
- パワー・グッド・フラグ
- ヒステリシス付きの高精度イネーブルおよび入力 UVLO
- ヒステリシス付きのサーマル・シャットダウン保護
- 2.8mm × 3.7mm × 1.9mm のパッケージ
- WEBENCH® Power Designer により、TPSM265R1 を使用するカスタム・レギュレータ設計を作成

2 アプリケーション

- フィールド・トランスミッタとプロセス・センサ
- 位置センサと近接センサ
- PLC、DCS、PAC
- サーボ・ドライブ電源供給モジュール
- 負出力アプリケーション

3 概要

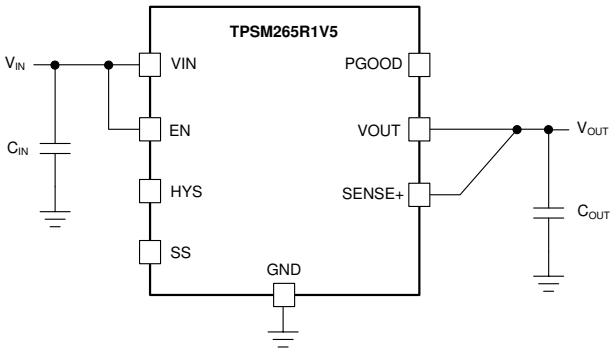
TPSM265R1 は、最高連続入力電圧 65V の広い入力電圧範囲で動作する小型で使いやすいモジュールです。このモジュールはコントローラ、MOSFET、出力インダクタをすべて内蔵しています。このモジュールは、小さな PCB フットプリントで電源の設計を迅速かつ簡単に実装できるよう設計されています。2 つの固定出力電圧 (3.3V、5V) オプションと 1 つの可変出力電圧 (1.223V～15V に設定可能) オプションを提供しています。どのオプションも負荷電流定格は 100mA です。TPSM265R1 はパルス周波数変調 (PFM) モードで動作し、軽負荷時に最高の効率を実現します。この制御方式はループ補償を必要としないため、ラインおよび負荷過渡が非常に優れています。

TPSM265R1 は小型かつ簡単であるように設計されていますが、多くの機能を備えています。高精度のイネーブル、可変 UVLO、ヒステリシスにより、特定の電源オンおよびオフ要件を満たすことができます。選択 / 設定可能なスタートアップ・タイミングとして、最小遅延 (ソフトスタートなし)、内部固定 (900µs)、外付けコンデンサで外部的にプログラム可能なソフトスタートを選択できます。オープン・ドレインの PGOOD インジケータを使用すると、シーケンシングと出力電圧監視が可能です。パッケージ・サイズが 2.8mm × 3.7mm × 1.9mm と非常に小さいため、スペースの制約が厳しいアプリケーションに最適です。

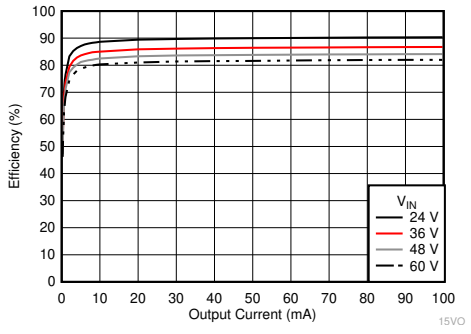
製品情報

部品番号(1) (1 ページ)	出力	パッケージ
TPSM265R1	1.223V～15V	uSiP
TPSM265R1V3	3.3V	
TPSM265R1V5	5V	

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的な回路図、固定出力



標準的な効率、V_{OUT} = 15V

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics (VIN = 5 V) ... 7
6.7 Typical Characteristics (VIN = 12 V) ... 8
6.8 Typical Characteristics (VIN = 24 V) ... 9
6.9 Typical Characteristics (VIN = 48 V) ... 10
6.10 Typical Characteristics (VIN = 65 V) ... 11
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 12
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 17
8 Applications and Implementation ... 18
8.1 Application Information ... 18
8.2 Typical Applications ... 18
9 Power Supply Recommendations ... 21
10 Layout ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
11 Device and Documentation Support ... 26
11.1 Device Support ... 26
11.2 Documentation Support ... 26
11.3 Receiving Notification of Documentation Updates ... 26
11.4 Support Resources ... 26
11.5 Trademarks ... 27
11.6 Electrostatic Discharge Caution ... 27
11.7 Glossary ... 27
12 Mechanical, Packaging, and Orderable Information ... 27

4 Revision History

Changes from Revision A (November 2019) to Revision B (December 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• デバイスのステータスを事前情報から量産データに変更	1

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5 Pin Configuration and Functions

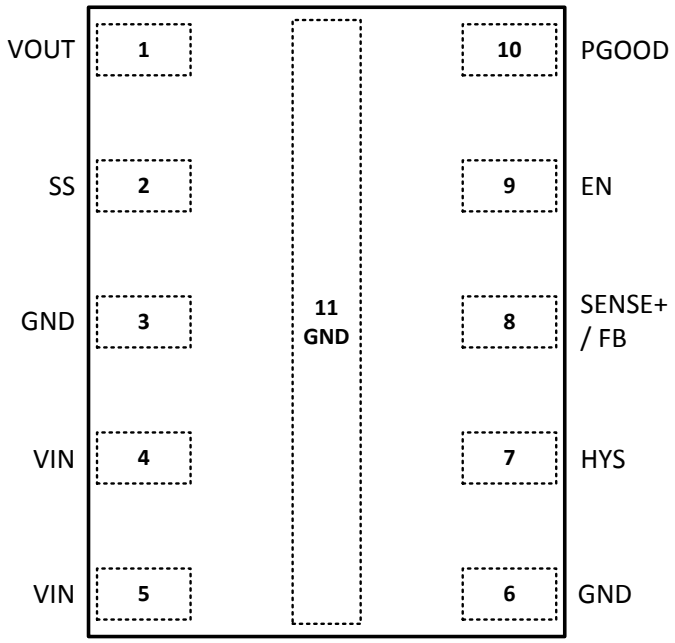


図 5-1. 10-Pin uSiP Exposed Thermal Pad SIL-10C Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VOUT	O	Output voltage pin. The VOUT pin is connected to the internal output inductor. Connect the VOUT pin to an external output capacitor and the output load. The output capacitor connections must be made as close as possible to the VOUT and GND pin 11 of the module. See *セクション 10.2*.
2	SS	I	Soft-start programming pin. If the SS pin is floating, the output voltage ramp up time is approximately 1 ms after the device is enabled by the EN pin. If a 100-kΩ resistor is placed from the SS pin to GND, the internal soft start is disabled and the output voltage ramps up immediately after the device is enabled with the EN pin. Other output voltage ramp up times can be obtained by connecting an appropriate capacitance from the SS pin to GND.
3, 6, 11	GND	G	Ground pins. Connect all GND pins to the system ground plane. **Pin 3 is not connected to GND internal to the module**. Connect pin 3 directly to pin 11 on the host PCB. See *セクション 10.2*.
4, 5	VIN	I	Input supply pins. The VIN pins are connected to the internal controller and power MOSFETs. Connect the VIN pins to an external input capacitor and the input power source. The input capacitor connections must be made as close as possible to the VIN pins and GND pin 6 of the module. See *セクション 10.2*.
7	HYS	O	Enable hysteresis pin. The open-drain HYS pin can be used along with external resistors to program the hysteresis of a user-defined UVLO using the EN pin. HYS is internally pulled to GND when EN is below its turnon threshold and HYS goes open drain when EN is above its turnon threshold.
8	SENSE+/FB	I	Output voltage feedback pin. For fixed output voltage options, the SENSE+ pin must be externally connected to VOUT. For the adjustable output voltage option, the FB pin must be connected to an external resistor divider that is connected between VOUT and GND.
9	EN	I	Enable pin. The module is enabled when the EN pin is pulled high and disabled when the EN pin is pulled low. An external resistor divider can be connected to the EN pin to act as an external UVLO.
10	PGOOD	O	Power Good pin. The open-drain PGOOD pin is pulled low when the SENSE+ or FB pin is below the VOUT regulation target. An external 10-kΩ to 100-kΩ pullup resistor can be used to pull the PGOOD pin high when VOUT meets the regulation target.

(1) G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	68	V
	SENSE+, PGOOD	–0.3	16	V
	HYS	–0.3	7	V
	FB, SS	–0.3	3.6	V
Output voltage	VOUT	–0.3	16	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Input voltage	VIN		3(1)		65	V
	PGOOD				12	V
	HYS				5	V
Output voltage	VOUT	Adjustable option	1.223		15	V
		Fixed 5 V option		5		V
		Fixed 3.3 V option		3.3		V
Output current	Iout				100	mA
T_A	Operating ambient temperature		–40		125	°C
C_{IN}	Input capacitance	Ceramic	1(2)			µF
C_{OUT}	Output capacitance	Ceramic	10(3)			µF

(1) The minimum input voltage is 3.0 V or (V_{OUT} + 1 V), whichever is greater.
(2) See *セクション 8.2.2.3* of the data sheet for more information.
(3) See *セクション 7.3.3* of the data sheet for more information.

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6.4 Thermal Information

THERMAL METRIC[1]		TPSM265R1 SIL-10C 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +125°C, V_{IN} = 12 V, V_{OUT} = 5 V, (unless otherwise noted); C_{IN1} = 1 µF, 100-V, 1206 ceramic, C_{IN2} = 33 µF, 100-V, electrolytic (optional), and C_{OUT} = 47 µF, 16-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VIN	Input supply voltage range	Over I_{OUT} range	3[1]		65	V
UVLO	VIN UVLO rising threshold	VIN rising	2.60	2.75	2.95	V
	VIN UVLO falling threshold	VIN falling	2.35	2.45	2.60	V
$I_{Q(VIN)}$	VIN operating non-switching supply current	V_{FB} = 1.5 V, T_A = 25°C		10.5	15	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V, T_A = 25°C		4.6	6.0	µA
ENABLE						
$V_{EN(rise)}$	EN voltage rising threshold	EN voltage rising	1.163	1.212	1.262	V
$V_{EN(fall)}$	EN voltage falling threshold	EN voltage falling	1.109	1.144	1.178	V
$V_{EN(hyst)}$	EN voltage hysteresis			68		mV
$V_{EN(sd)}$	EN shutdown threshold	EN voltage falling	0.3	0.6		V
R_{HYS}	HYS on-resistance	V_{EN} = 1 V		80	200	Ω
$I_{HYS(LKG)}$	HYS off-state leakage current	V_{EN} = 1.5 V, V_{HYS} = 5.5 V		10	100	nA
FEEDBACK (Adjustable option)						
V_{FB}	Feedback voltage[2] [4]	Lower regulation threshold	1.205	1.223	1.241	V
		Upper regulation threshold	1.220	1.233	1.246	V
		Hysteresis		10		mV
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0 A		0.3%		
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.3%		
	Temperature variation	-40°C ≤ T_A = T_J ≤ 125°C, I_{OUT} = 0 A		0.5%		
I_{FB}	Input bias current into FB pin	V_{FB} = 1 V			100	nA
OUTPUT VOLTAGE (Fixed 5 V option)						
V_{OUT}	Output voltage set-point	SENSE+ connected to VOUT	4.9	5.0	5.1	V
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0 A		0.3%		
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.3%		
	Temperature variation	-40°C ≤ T_A = T_J ≤ 125°C, I_{OUT} = 0 A		0.5%		
ISENSE+	SENSE+ input current			6.7		µA
eff	Efficiency	V_{OUT} = 5.0 V, I_{OUT} = 50 mA		83.0%		
OUTPUT VOLTAGE (Fixed 3.3 V option)						
V_{OUT}	Output voltage set-point	SENSE+ connected to VOUT	3.23	3.3	3.37	V
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0 A		0.3%		
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.3%		
	Temperature variation	-40°C ≤ T_A = T_J ≤ 125°C, I_{OUT} = 0 A		0.5%		
ISENSE+	SENSE+ input current			3.9		µA

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6.5 Electrical Characteristics (continued)

Limits apply over T_A = –40°C to +125°C, V_{IN} = 12 V, V_{OUT} = 5 V, (unless otherwise noted); C_{IN1} = 1 µF, 100-V, 1206 ceramic, C_{IN2} = 33 µF, 100-V, electrolytic (optional), and C_{OUT} = 47 µF, 16-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
eff	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 50 mA		77.2%		
CURRENT						
I_{OUT}	Output current	See SOA curves for any thermal derating	0		100	mA
I_{OCL}	Overcurrent limit threshold	V_{OUT} foldback		130		mA
SOFT-START						
I_{SS}	Soft-start charge current	V_{SS} = 1 V		10		µA
T_{SS}	Soft-start rise time	SS pin open		900		µs
POWER GOOD						
PGOOD	PGOOD threshold	PGOOD high, V_{OUT} rising		94%		
PGOOD	PGOOD threshold	PGOOD low, V_{OUT} falling		87%		
$I_{PGOOD(LKG)}$	PGOOD leakage current	V_{PGOOD} = 5.5 V, PGOOD high		10	100	nA
R_{PGOOD}	PGOOD ON-resistance	PGOOD low		80	200	Ω
	Min VIN for valid PGOOD output	I_{PGOOD} = 0.1 mA, V_{PGOOD} < 0.5 V		1.2	1.65	V
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (3)	Temperature rising		170		°C
T_{HYST}	Thermal shutdown hysteresis (3)			10		°C

(1) The recommended minimum input voltage is 3.0 V or (V_{OUT} + 1 V), whichever is greater.
(2) The FB pin has both lower and upper thresholds associated with the hysteretic control scheme of the module.
(3) Specified by design. Not production tested.
(4) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.

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6.6 Typical Characteristics (VIN = 5 V)

Refer to セクション 8.2 for circuit designs. T_A = 25°C unless otherwise noted.

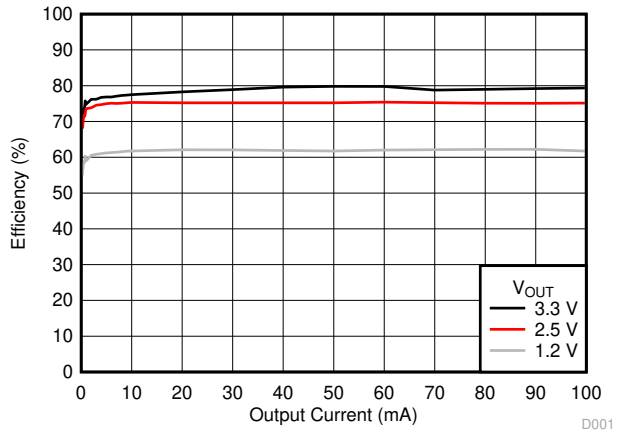


図 6-1. Efficiency

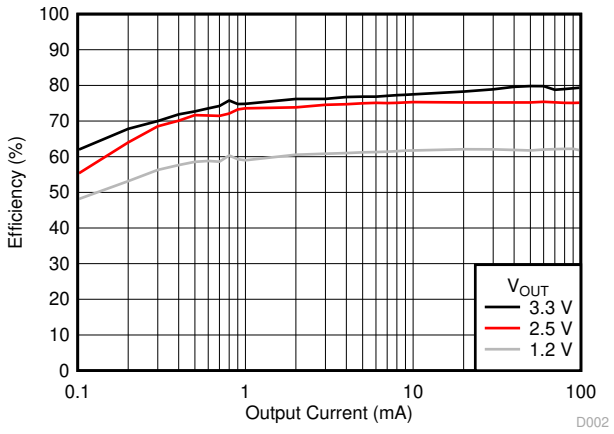


図 6-2. Efficiency Log Scale

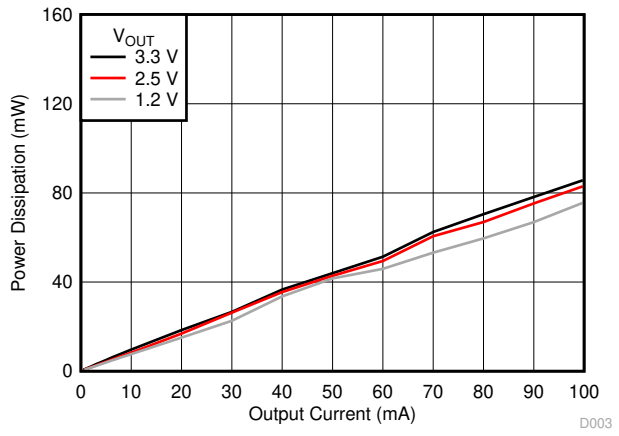
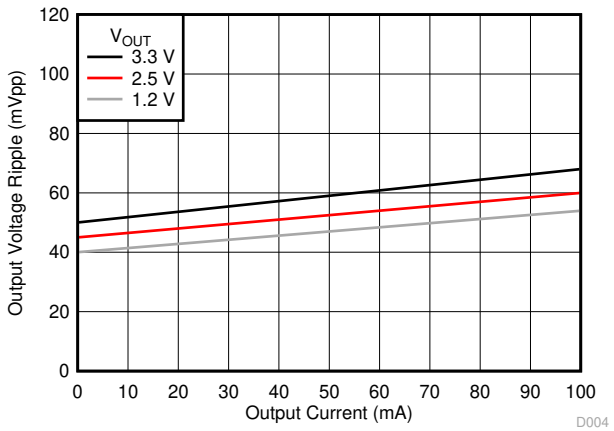
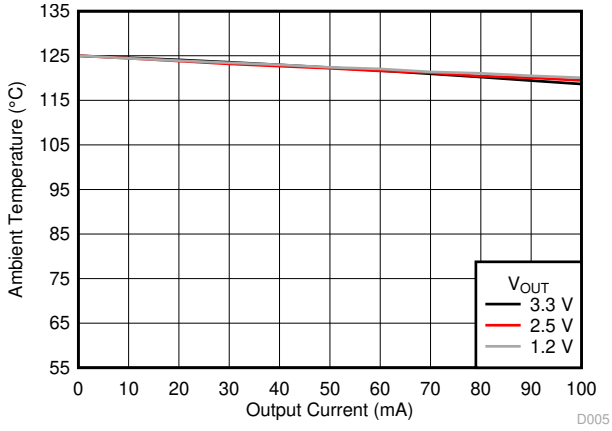


図 6-3. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

図 6-4. Output Voltage Ripple



Applies to a device soldered to a 50-mm × 75-mm, 4-layer PCB

図 6-5. Safe Operating Area

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6.7 Typical Characteristics (VIN = 12 V)

Refer to セクション 8.2 for circuit designs. T_A = 25°C unless otherwise noted.

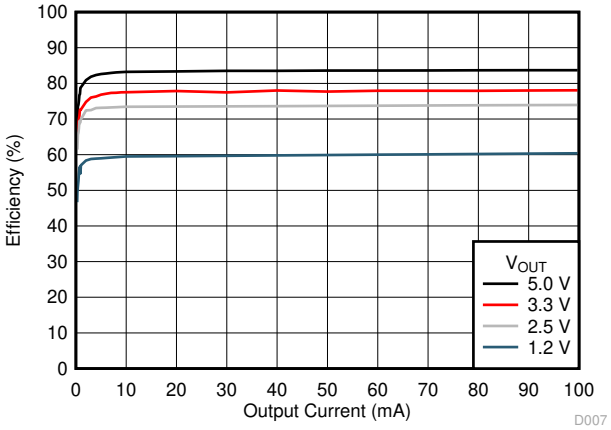


図 6-6. Efficiency

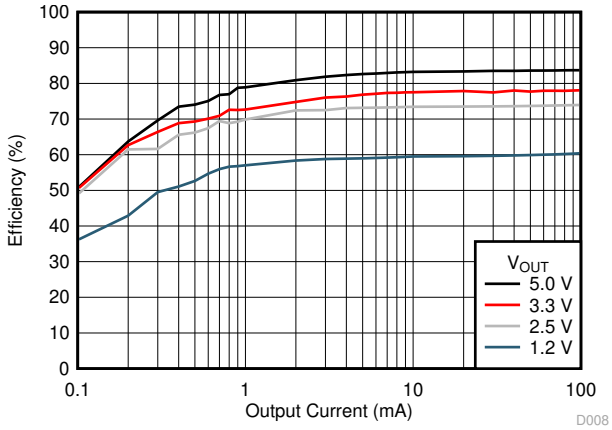


図 6-7. Efficiency Log Scale

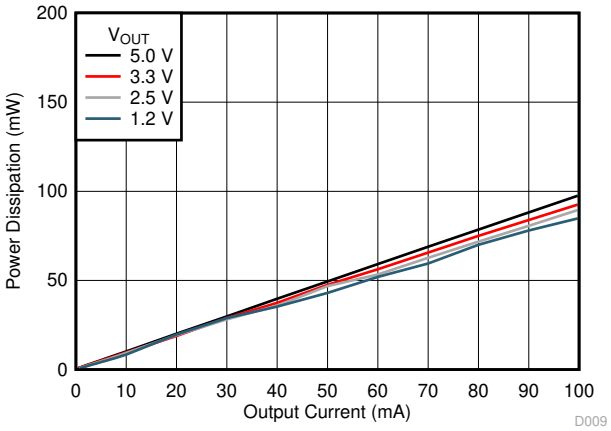
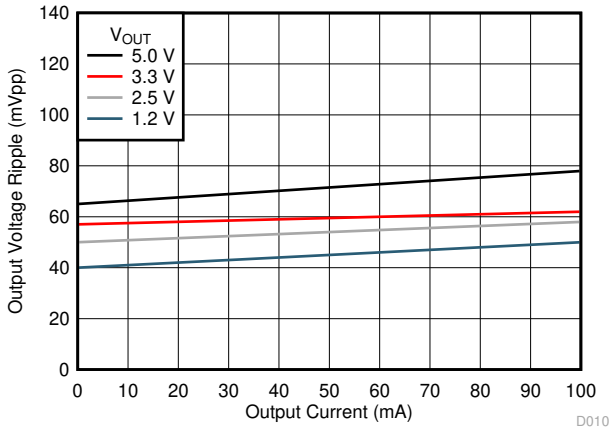
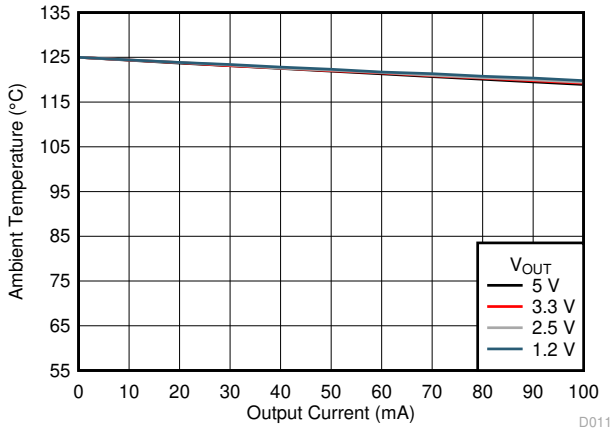


図 6-8. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

図 6-9. Output Voltage Ripple



Applies to a device soldered to a 50-mm × 75-mm, 4-layer PCB

図 6-10. Safe Operating Area

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6.8 Typical Characteristics (VIN = 24 V)

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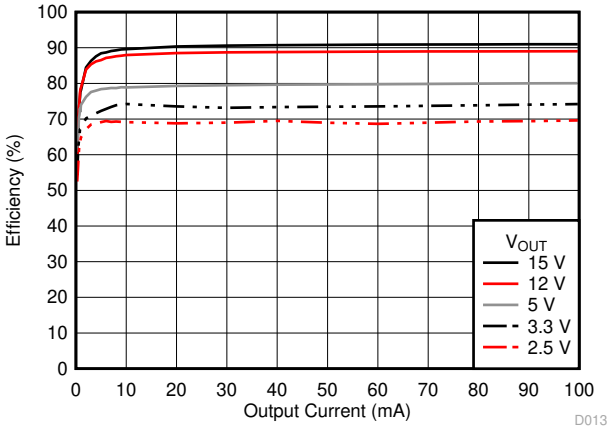


図 6-11. Efficiency

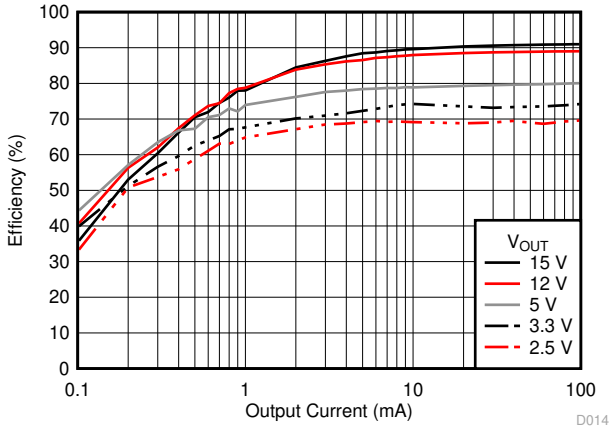


図 6-12. Efficiency Log Scale

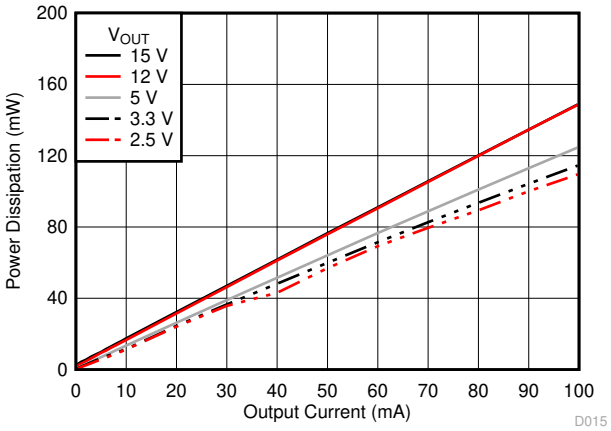
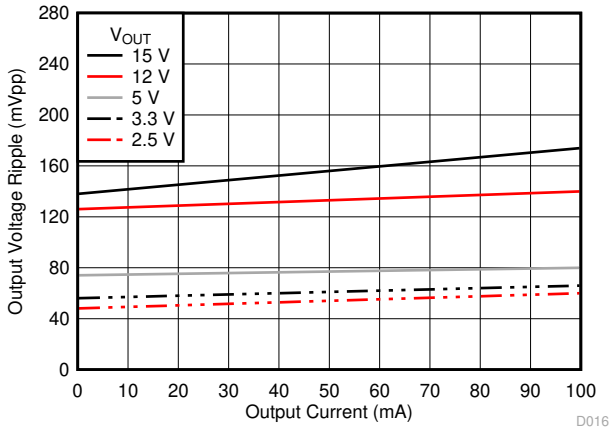
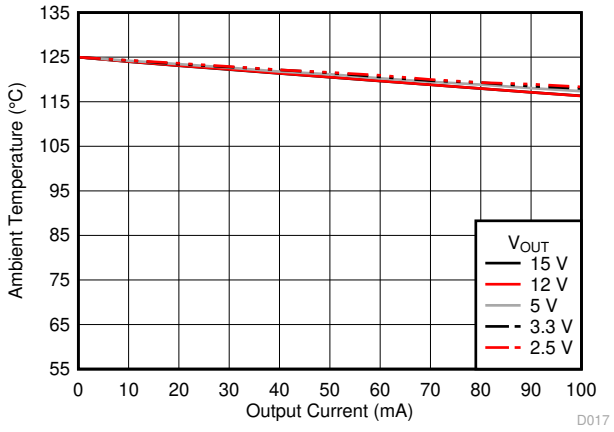


図 6-13. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

図 6-14. Output Voltage Ripple



Applies to a device soldered to a 50 mm × 75 mm, 4-layer PCB

図 6-15. Safe Operating Area

6.9 Typical Characteristics (VIN = 48 V)

Refer to セクション 8.2 for circuit designs. T_A = 25°C unless otherwise noted.

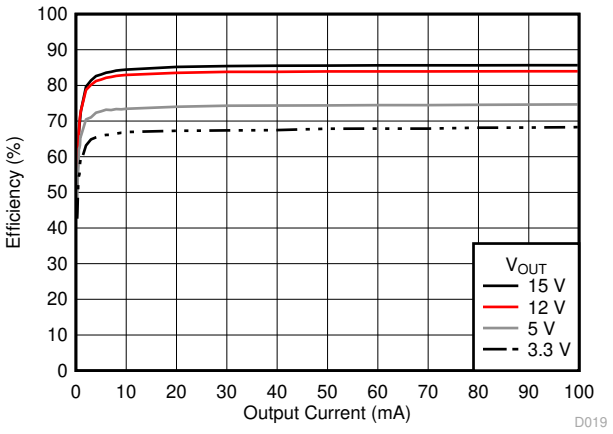


図 6-16. Efficiency

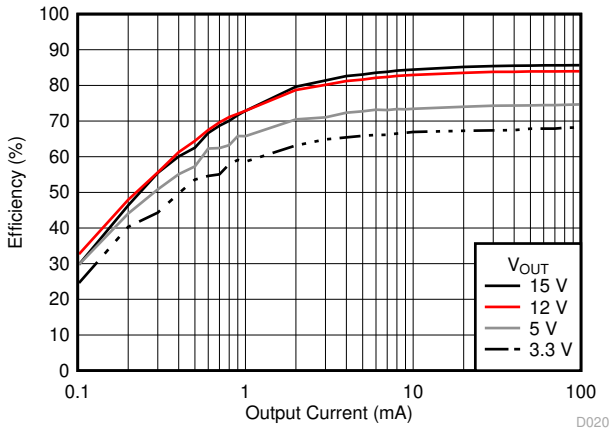


図 6-17. Efficiency Log Scale

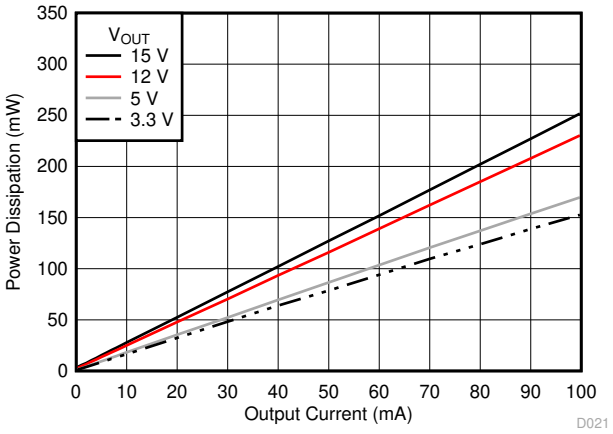
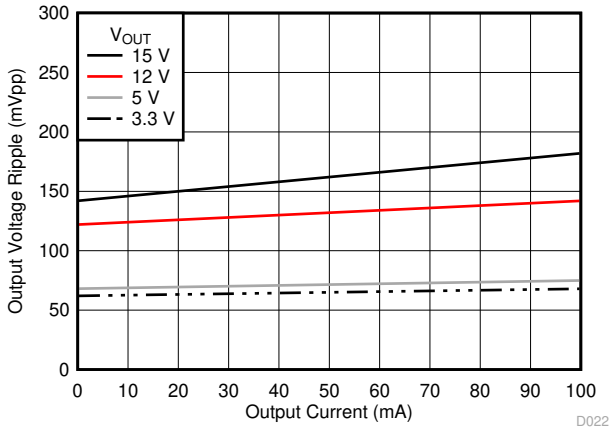
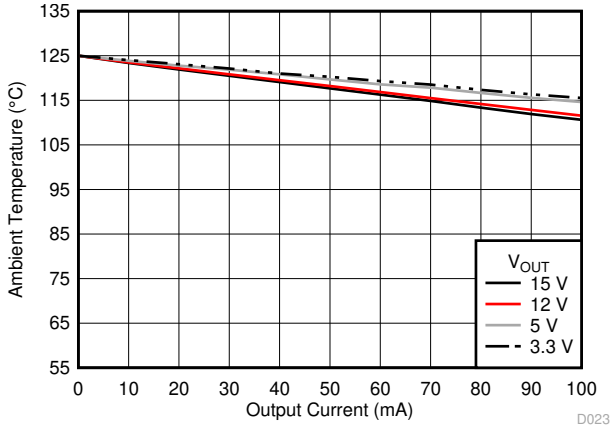


図 6-18. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

図 6-19. Output Voltage Ripple



Applies to a device soldered to a 50-mm × 75-mm, 4-layer PCB

図 6-20. Safe Operating Area

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6.10 Typical Characteristics (VIN = 65 V)

Refer to *セクション 8.2* for circuit designs. T_A = 25°C unless otherwise noted.

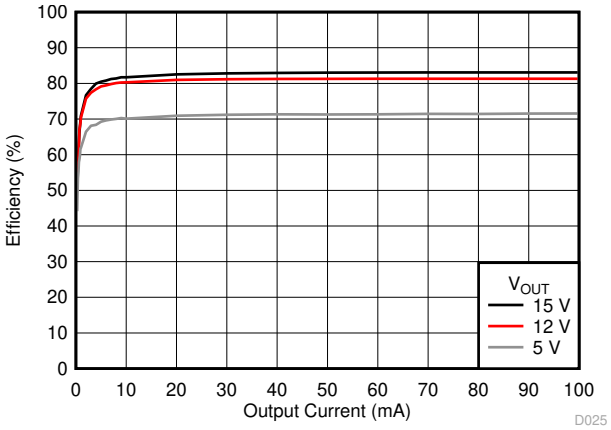


図 6-21. Efficiency

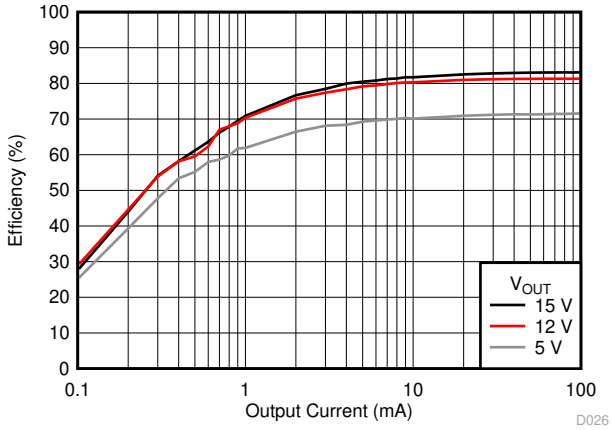


図 6-22. Efficiency Log Scale

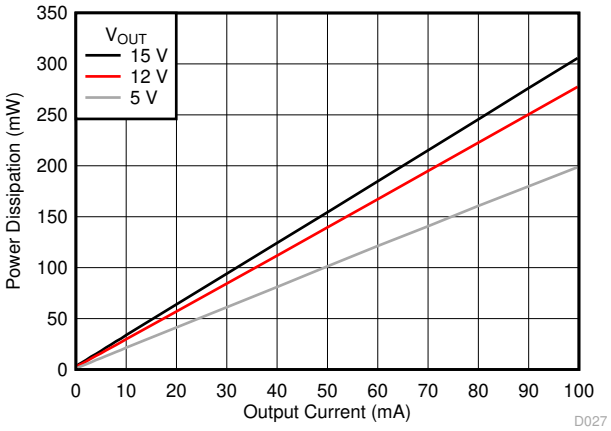
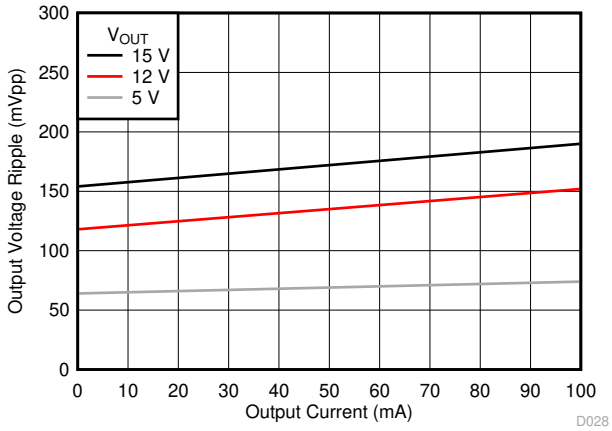
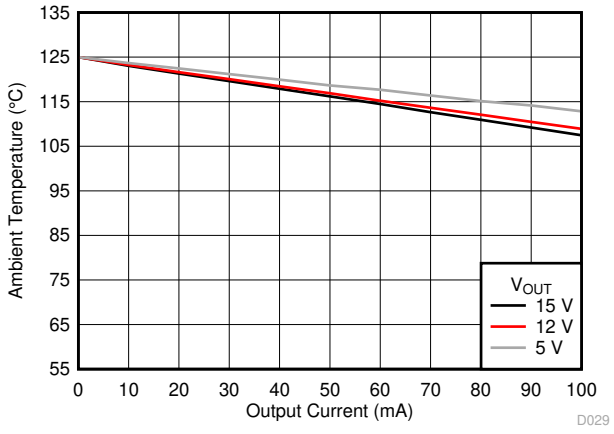


図 6-23. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

図 6-24. Output Voltage Ripple



Applies to a device soldered to a 50-mm × 75-mm, 4-layer PCB

図 6-25. Safe Operating Area

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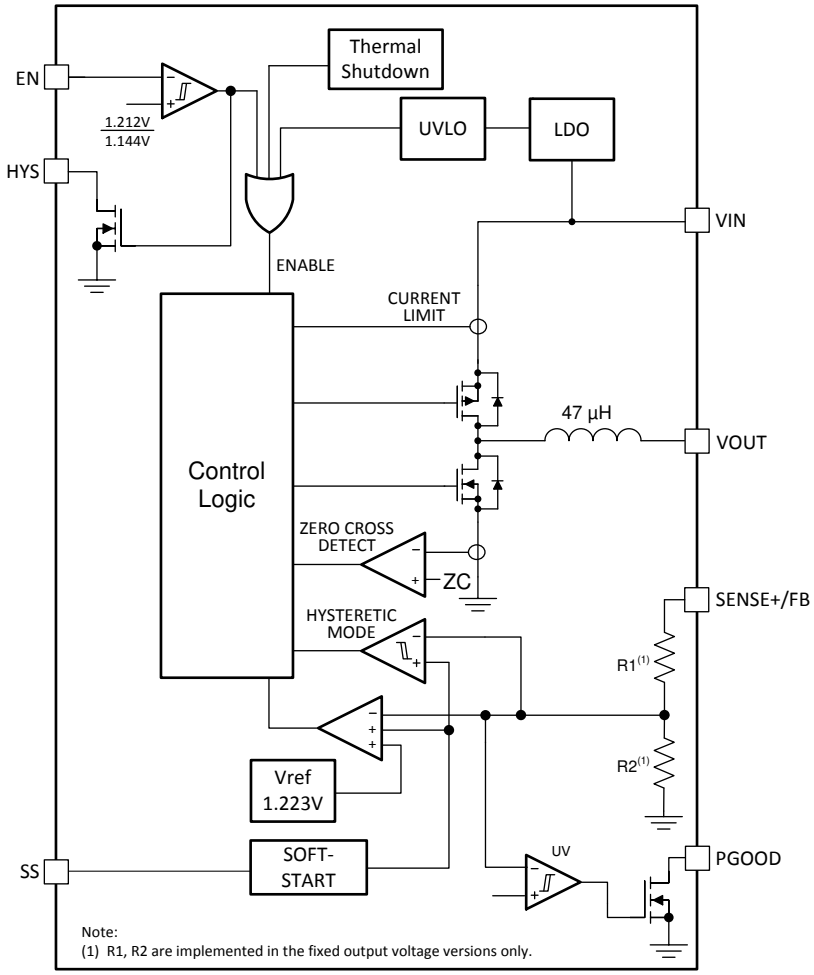
7 Detailed Description

7.1 Overview

The TPSM265R1 converter is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 3.3-V, 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated, or fully-regulated supply rails. With integrated power controller, inductor, and MOSFETs, the TPSM265R1 delivers up to 100-mA DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Operation in pulse frequency modulation (PFM) mode achieves exceptional light-load efficiency performance. Control-loop compensation is not required, reducing design time and external component count.

The TPSM265R1 incorporates several features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed, or externally-adjustable soft start, monotonic start-up into prebiased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple *layout*, requiring as few as two external components.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjustable Output Voltage (FB)

The TPSM265R1 has three voltage feedback options: fixed 3.3 V, fixed 5 V, and adjustable 1.223 V to 15 V. The fixed 3.3-V and 5-V versions include internal feedback resistors that sense the output directly through the SENSE+ pin; the adjustable voltage option senses the output through an external resistor divider connected from the output to the FB pin.

Setting the output voltage of the adjustable option requires two resistors: R_{FBT} and R_{FBB} (see 図 7-1). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and GND (pin 6). A resistor divider programs the ratio from output voltage V_{OUT} to FB. The recommended value of R_{FBT} is 100 kΩ. The value for R_{FBB} can be calculated using 式 1.

$$R_{FBB} = \frac{1.223}{V_{OUT} - 1.223} \times R_{FBT} \quad (1)$$

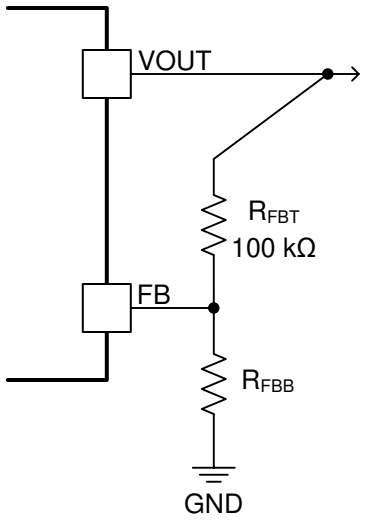


図 7-1. FB Resistor Divider

表 7-1. Standard R_{FBB} Values

VOUT (V)	R_{FBB} (kΩ) (1)		VOUT (V)	R_{FBB} (kΩ) (1)
1.223	open		3.3	59.0
1.5	442		5.0	32.4
1.8	210		7.5	19.6
2.0	158		10	14.0
2.5	95.3		12	11.3
3.0	68.1		15	8.87

(1) R_{FBT} = 100 kΩ

Selecting an R_{FBT} value of 100 kΩ is recommended for most applications. A larger R_{FBT} consumes less DC current, which is mandatory if light-load efficiency, is critical. However, R_{FBT} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see *セクション 10*.

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7.3.2 Input Capacitor Selection

The TPSM265R1 requires a minimum of 1 µF of ceramic type input capacitance. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. TI recommends adding additional capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. 表 7-2 includes a preferred list of capacitors by vendor.

表 7-2. Recommended Input Capacitors

VENDOR(1)	TEMPERATURE COEFFICIENT(3)	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)
Murata	X7R	GCJ21BR71H105KA01L	0805	50	1
TDK	X7R	CGA4J3X7R1H105K125AB	0805	50	1
Murata	X7S	GRJ21BC72A105KE11L	0805	100	1
TDK	X7S	CGA4J3X7S2A105K125AB	0805	100	1
Murata	X7S	GCM31CC72A225KE02L	1206	100	2.2
TDK	X7S	C3216X7S2A225K160AB	1206	100	2.2
TDK	X7R	CGA5L3X7R1H475K160AE	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values
(3) Maximum ESR at 100 kHz, 25°C

7.3.3 Output Capacitor Selection

The minimum amount of required output capacitance for the TPSM265R1 is 10 µF of ceramic type. TI recommends adding additional capacitance for applications with transient load requirements. See 表 7-3 for a preferred list of output capacitors by vendor.

表 7-3. Recommended Output Capacitors

VENDOR(1)	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE (µF)(2)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10
TDK	X5R	C3225X5R1C226M	1210	16	22
Murata	X5R	GRM32ER61C226K	1210	16	22
TDK	X5R	C3216X5R1E226M160AB	1206	25	22
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22
TDK	X5R	C3225X5R1A476M	1210	10	47
Murata	X5R	GRM32ER61C476K	1210	16	47

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in 表 7-3.
(2) Specified capacitance values

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7.3.4 Precision Enable (EN), Undervoltage Lockout (UVLO), and Hysteresis (HYS)

The EN pin provides precision ON and OFF control for the TPSM265R1. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. The simplest way to enable the TPSM265R1 is to connect EN directly to VIN. This allows the TPSM265R1 to start up when VIN is within its valid operating range. An external logic signal can also be used to drive the EN input to toggle the output on and off and for system sequencing or protection.

The TPSM265R1 implements internal undervoltage lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 2.95 V (max) with a typical hysteresis of 300 mV.

If an application requires a higher UVLO threshold, the EN input supports adjustable UVLO by connecting a resistor divider from VIN to the EN pin. The EN pin connects to an internal comparator referenced to a 1.212-V bandgap voltage with 68-mV hysteresis. However, applications requiring specific power-up and power-down requirements can program the hysteresis voltage independently using the HYS pin. 図 7-2 shows the resistor divider connection to establish a precision UVLO level with fixed internal hysteresis. 図 7-3 shows the resistor divider connection used to set the precision UVLO level as well as the adjustable hysteresis.

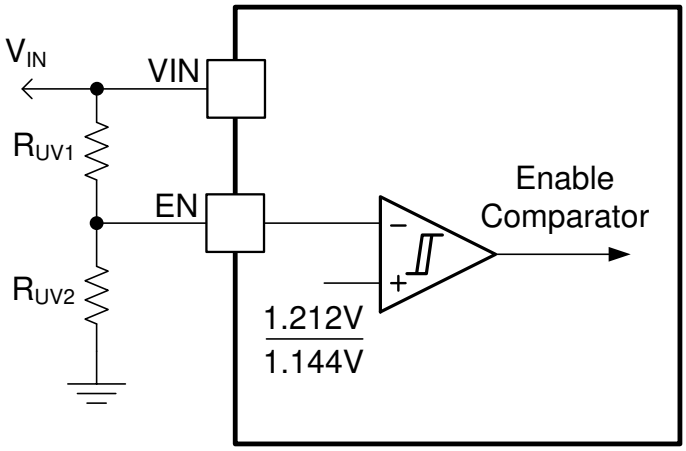


図 7-2. Programmable V_{IN} UVLO with Fixed Hysteresis

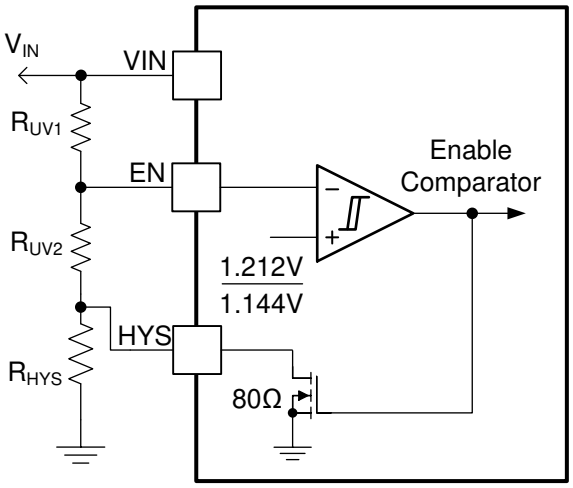


図 7-3. Programmable V_{IN} UVLO with Adjustable Hysteresis

Use 式 2 and 式 3 to calculate the input UVLO voltages turnon and turnoff voltages, respectively.

$$V_{IN(on)} = 1.212V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (2)$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \quad (3)$$

There is also a low I_Q shutdown mode when EN is pulled below 0.6 V (typ). If EN is below this shutdown threshold, the internal LDO regulator powers off, shutting down the bias currents of the TPSM265R1. The TPSM265R1 operates in standby mode when the EN voltage is between the shutdown and precision enable thresholds.

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7.3.5 PFM Operation

The TPSM265R1 operates in Pulse Frequency Modulation (PFM) mode. The TPSM265R1 behaves as a hysteretic voltage regulator operating within upper and lower feedback regulation thresholds with typical 10 mV of hysteresis. 図 7-4 is a representation of the relevant voltage waveforms and inductor current waveform. The TPSM265R1 provides the required switching pulses to recharge the output capacitance, followed by a sleep period where most of the internal circuits are shut off. The load current is supported by the output capacitor during this time, and the TPSM265R1 current consumption approaches the sleep quiescent current of 10.5 µA (typ). The sleep period duration depends on load current and output capacitance.

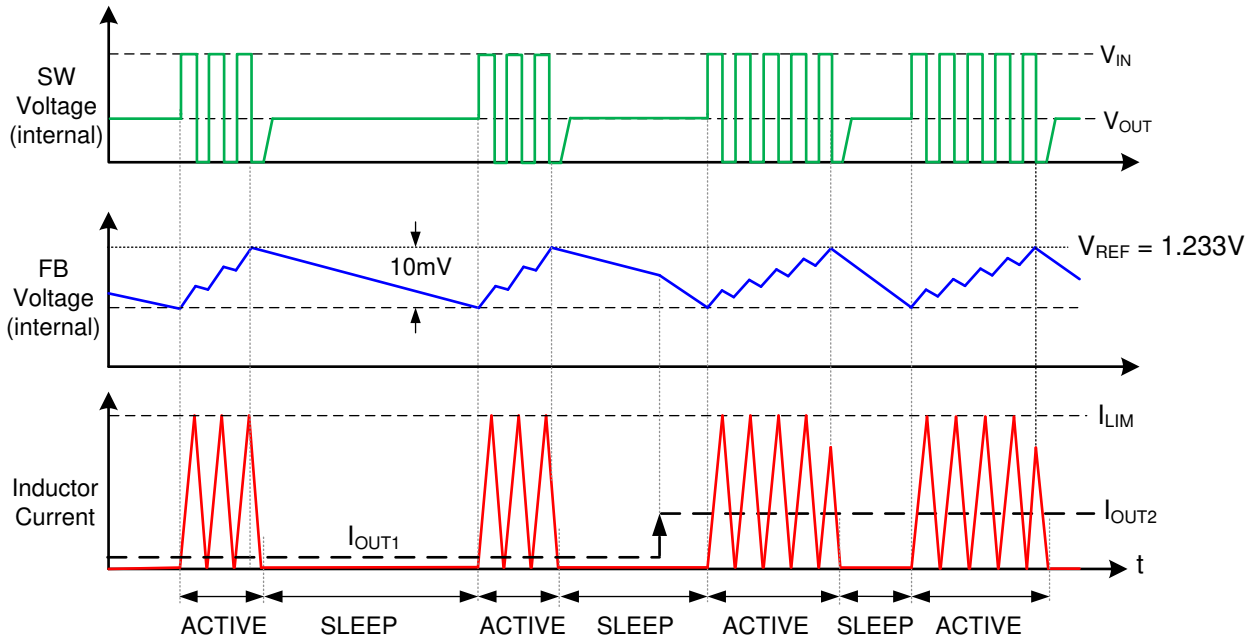


図 7-4. PFM Mode SW Node Voltage, Feedback Voltage, and Inductor Current Waveforms

7.3.6 Power Good (PGOOD)

The TPSM265R1 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 12 V. Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

When the output voltage exceeds 94% of the setpoint, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 87% of the setpoint, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 µs.

7.3.7 Configurable Soft Start (SS)

The TPSM265R1 has a flexible and easy-to-use soft-start control pin, SS. The soft-start feature prevents inrush current when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is powered up or enabled. Selectable and adjustable start-up timing options include minimum delay (no soft start), 900-µs internally fixed soft start, and an externally programmable soft start.

Leaving the SS pin open enables the internal soft-start control ramp with a soft-start interval of 900 µs. The soft-start time can be increased by connecting an external capacitor, C_{SS}, from SS to GND. Applications with a large amount of output capacitance or higher output voltage can benefit from increasing the soft-start time. Longer soft-start time reduces the supply current needed to charge the output capacitors and supply any output loading. An internal current source, I_{SS}, of 10 µA charges C_{SS} and generates a ramp to control the ramp rate of the output voltage. Use 式 4 to calculate the C_{SS} capacitance for a desired soft-start time, t_{SS}.

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$$C_{SS}\left[nF\right] = 8.1 \cdot t_{SS}\left[ms\right] \quad (4)$$

C_{SS} is discharged by an internal FET when V_{OUT} is shut down by EN, UVLO, or thermal shutdown.

It is desirable in some applications for the output voltage to reach its nominal setpoint in the shortest possible time. Connecting a 100-kΩ resistor from SS to GND disables the soft-start circuit, and the TPSM265R1 operates in current limit during start-up to rapidly charge the output capacitance.

7.3.7.1 Prebiased Start-up

To prevent discharge of a prebiased output voltage, the TPSM265R1 is capable of start-up into prebiased output conditions. When a prebiased voltage is present at start-up, the TPSM265R1 waits until the soft-start ramp voltage is above the prebiased voltage before it begins switching and then follows the soft-start ramp to the regulation setpoint.

7.3.8 Overcurrent Protection (OCP)

The TPSM265R1 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

7.3.9 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C (typ) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM265R1 restarts when the junction temperature falls to 160°C (typ).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM265R1. When V_{EN} is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4.6 µA at V_{IN} = 12 V. The TPSM265R1 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal bias rail LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 0.6 V and below the precision enable threshold (1.212 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UV threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode

The TPSM265R1 is in active mode when V_{EN} and the internal bias rail are above their relevant thresholds, FB has fallen below the lower hysteresis level, and boundary conduction mode is recharging the output capacitor to the upper hysteresis level. There is a 4-µs wake-up delay from sleep to active states.

7.4.4 Sleep Mode

The TPSM265R1 is in sleep mode when V_{EN} and the internal bias rail are above the relevant threshold levels, V_{FB} has exceeded the upper hysteresis level, and the output capacitor is sourcing the load current. In sleep mode, the TPSM265R1 operates with very low quiescent current.

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8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM265R1 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM265R1, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM265R1 power module.

As mentioned previously, the TPSM265R1 also integrates several optional features to meet system design requirements, including precision enable, UVLO, programmable soft start, and PGOOD indicator. The application circuit detailed below shows TPSM265R1 configuration options suitable for several application use cases. Refer to the *TPSM265R1EVM User's Guide* for more detail.

8.2 Typical Applications

図 8-1 shows the schematic diagram of a 5-V, 100-mA converter.

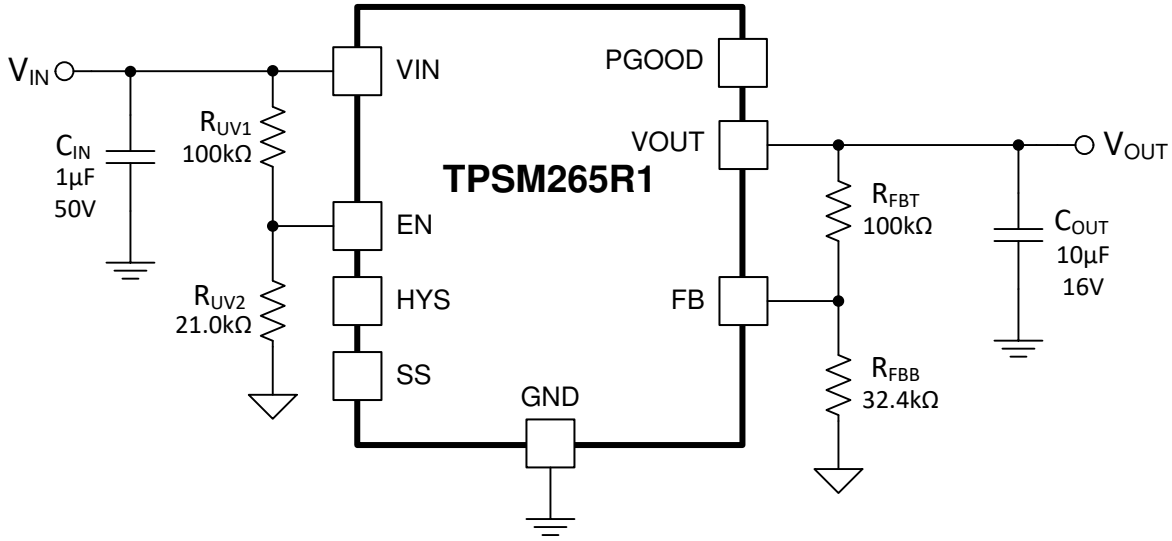


図 8-1. TPSM265R1 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters and follow the design procedures in the *セクション 8.2.2*.

表 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	100 mA (50 Ω)

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM265R1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM265R1 device is externally adjustable using a resistor divider. The recommended value of R_{FBT} is 100 kΩ. The value for R_{FBB} can be selected from 表 7-1 or calculated using 式 5:

$$R_{FBB} = \frac{1.223}{V_{OUT} - 1.223} \times R_{FBT} \tag{5}$$

For the desired output voltage of 5 V, the formula yields a value of 32.38 kΩ. Choose the closest available standard value of 32.4 kΩ for R_{FBB}.

8.2.2.3 Input Capacitors

The TPSM265R1 requires a minimum input capacitance of 1-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, a single, 1-µF, 50-V ceramic capacitor is selected.

8.2.2.4 Output Capacitor Selection

The TPSM265R1 requires a minimum of 10 µF of ceramic output capacitance for proper operation. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, a single 10-µF, 16-V, ceramic capacitor is used.

8.2.2.5 UVLO Programming

Applications requiring a higher UVLO threshold can benefit from applying a resistor divider on the EN pin. The values for the resistors can be calculated using 式 6 and 式 7.

$$V_{IN(on)} = 1.212V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \tag{6}$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \tag{7}$$

For this application, the UVLO was raised to 7 V (R_{UV1} = 100 kΩ, R_{UV2} = 21.0 kΩ, and R_{HYS} = 0 (not used)).

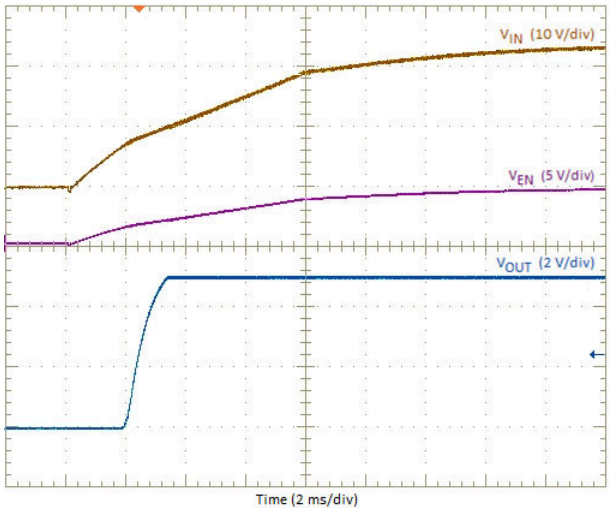
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8.2.2.6 Soft-Start Capacitor – C_{SS}

In this application, the SS pin was left open, resulting in a 900 µs soft-start rise time. Applications requiring a longer soft-start time can calculate the soft-start capacitor value using 式 8:

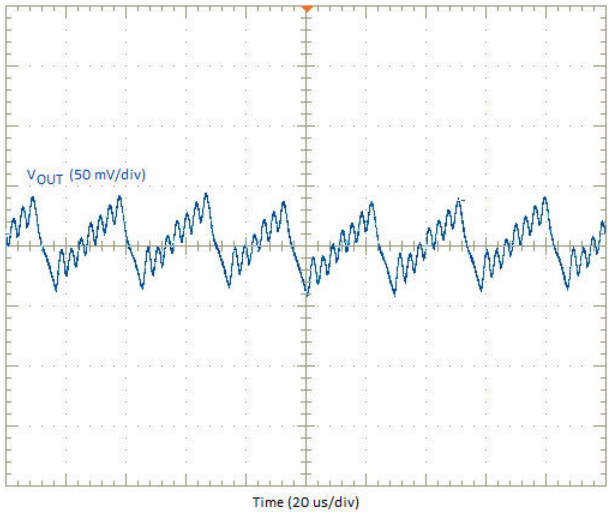
$$C_{SS}\left[nF\right] = 8.1 \cdot t_{SS}\left[ms\right] \tag{8}$$

8.2.3 Application Curves



V_{IN} = 24 V V_{OUT} = 5 V R_{LOAD} = 50 Ω
R_{UV1} = 100 kΩ R_{UV2} = 21.0 kΩ

図 8-2. Start-up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 10 µF
R_{LOAD} = 50 Ω

図 8-3. Output Voltage Ripple

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9 Power Supply Recommendations

The TPSM265R1 is designed to operate from an input voltage supply range between 3 V and 65 V. This input supply must be able to provide the maximum input current and maintain a voltage above the set UVLO voltage. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the TPSM265R1 supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPSM265R1, additional bulk capacitance can be required in addition to the ceramic input capacitance. A 4.7-µF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

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10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 10-1 and 図 10-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- **Connect all GND pins together using copper plane or thick copper traces.**
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place R_{FBT} and R_{FBB} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

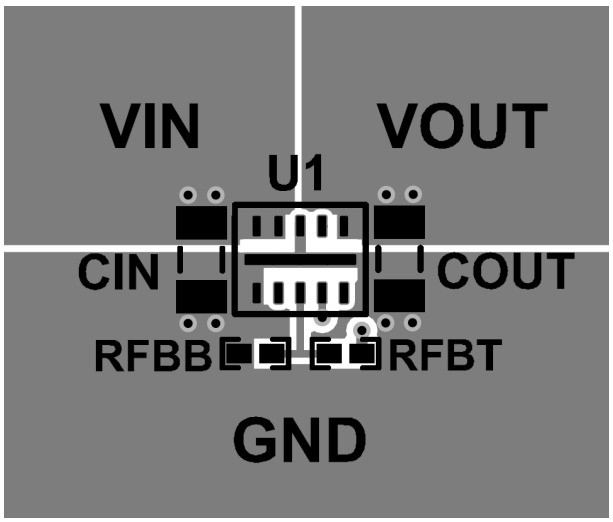


図 10-1. Typical Top-Layer Layout

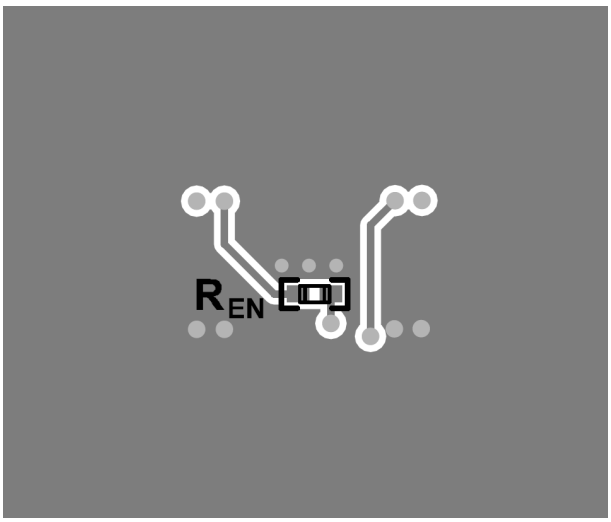


図 10-2. Typical Bottom-Layer Layout

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10.2.1 Theta JA versus PCB Area

The amount of PCB copper affects the thermal performance of the device. 図 10-3 shows the effects of copper area on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the TPSM265R1. The junction-to-ambient thermal resistance is plotted for a 4-layer PCB with an area from 0.5 cm^2 to 39 cm^2.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in *セクション 6.6* to *セクション 6.10*.
2. Calculate the maximum θ_{JA} using 式 9 and the maximum ambient temperature of the application.

$$\theta_{JA} = \frac{(125^{\circ}C - T_{A(max)})}{P_{D(max)}} \ (^{\circ}C/W) \tag{9}$$

3. Reference 図 10-3 to determine the minimum required PCB area for the application conditions.

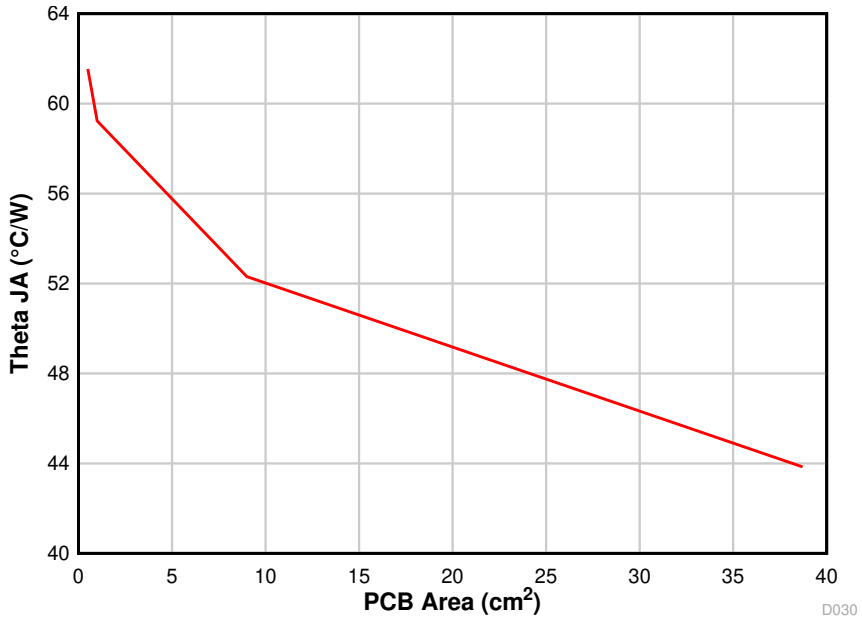


図 10-3. θ_{JA} versus PCB Area

10.2.2 Package Specifications

表 10-1. Package Specifications Table

TPSM265R1		VALUE	UNIT
Weight		37.7	mg
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	139	MHrs

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10.2.3 EMI

The TPSM265R1 is compliant with EN55011 radiated emissions. 図 10-4, 図 10-5, and 図 10-6 show typical examples of radiated emission plots for the TPSM265R1. The graphs include the plots of the antenna in the horizontal and vertical positions.

EMI plots were measured using the standard TPSM265R1EVM with no input filter.

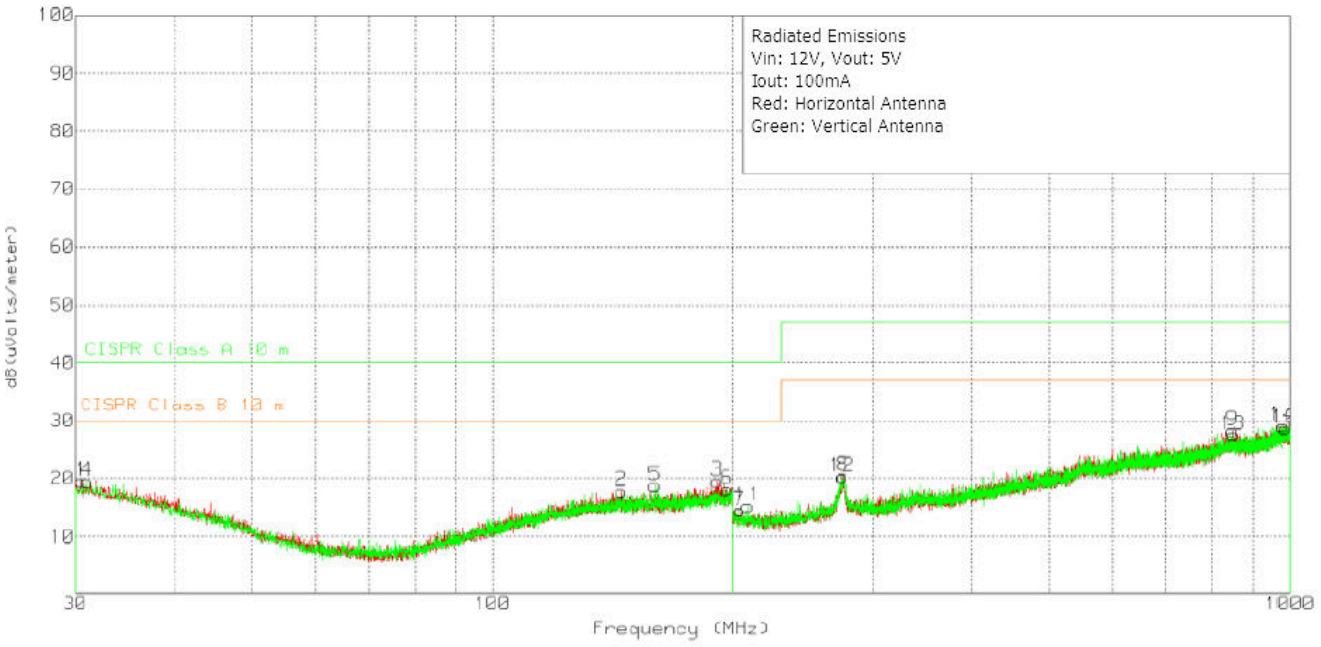


図 10-4. Radiated Emissions 12-V Input, 5-V Output, 100-mA Load

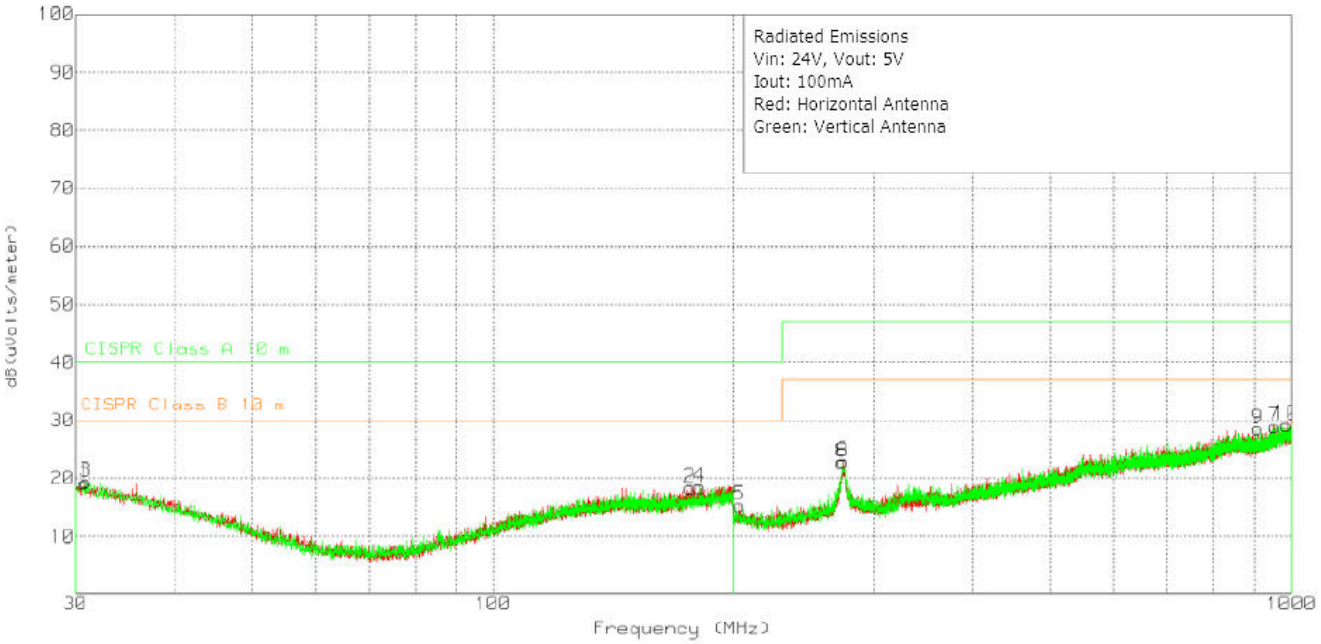


図 10-5. Radiated Emissions 24-V Input, 5-V Output, 100-mA Load

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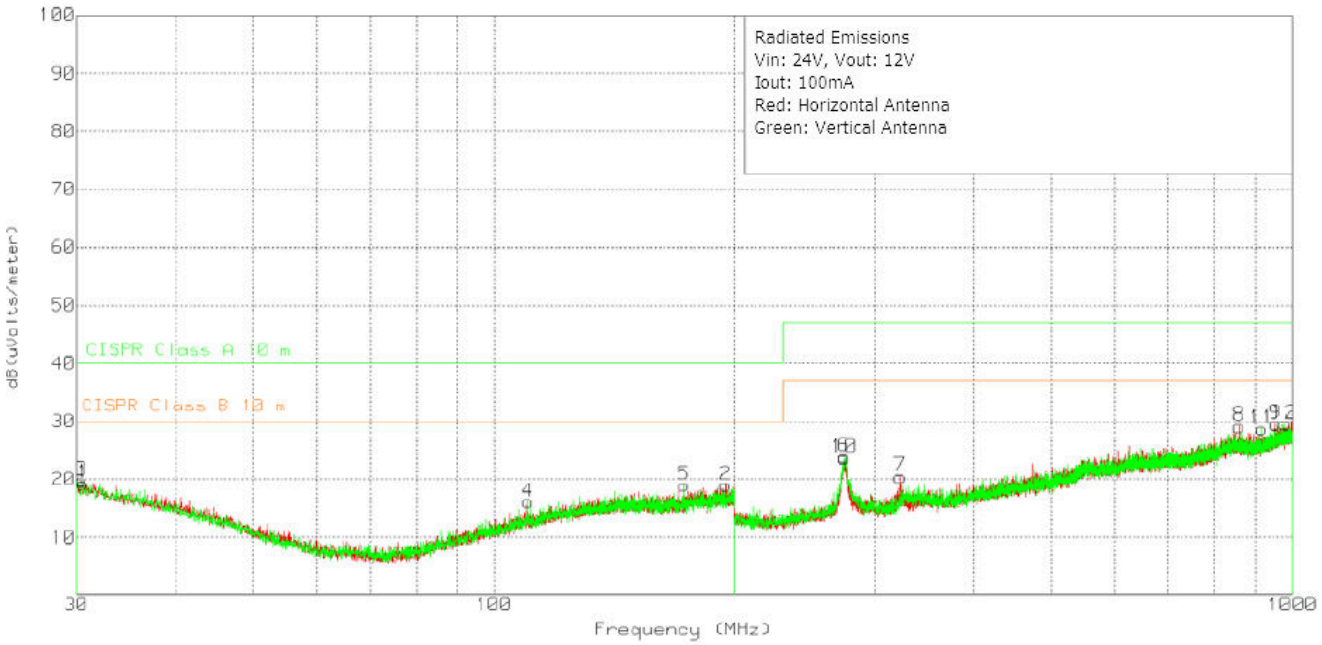


図 10-6. Radiated Emissions 24-V Input, 12-V Output, 100-mA Load

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For development support, see the following:

- For TI's reference design library, visit TI reference designs.
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center.
- To view a related device of this product, see the LM5166.

11.1.3 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM265R1 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPSM265R1EVM User's Guide*
- Texas Instruments, *Using the TPSM265R1 in an Inverting Buck-Boost Topology Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

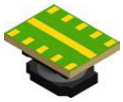
11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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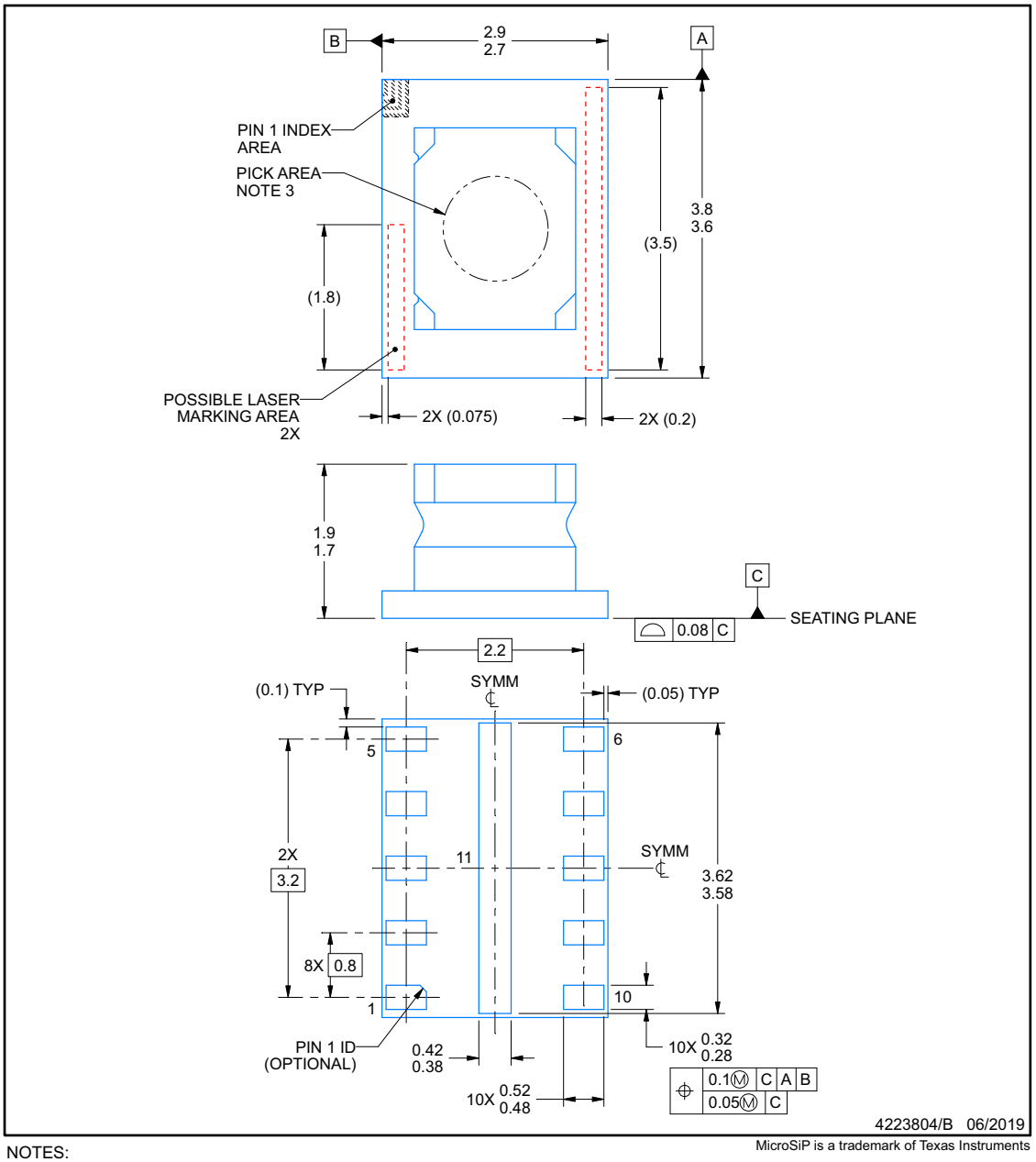


PACKAGE OUTLINE

SIL0010C

uSIP™ - 1.9 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

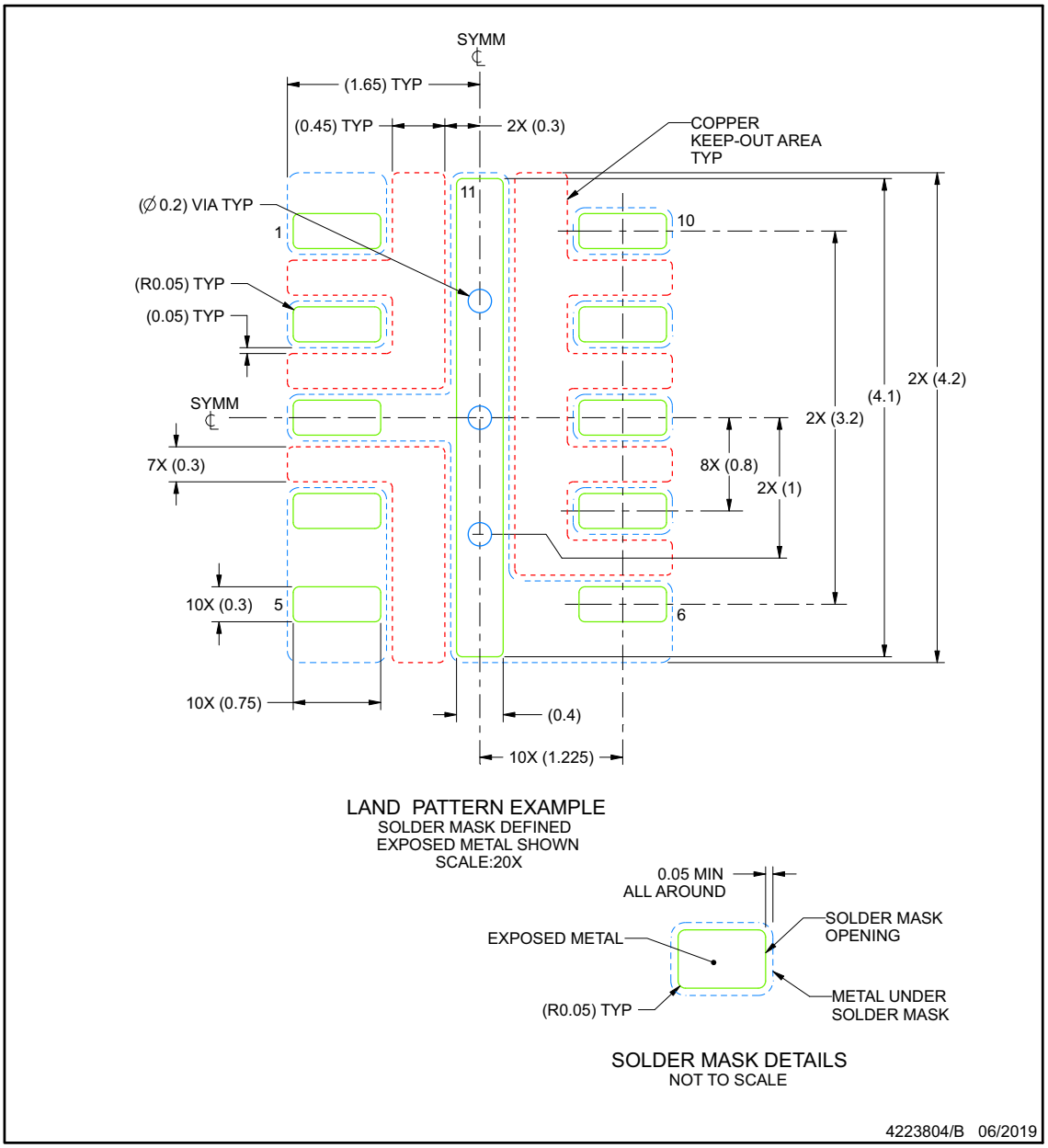
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EXAMPLE BOARD LAYOUT

SIL0010C

uSIP™ - 1.9 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

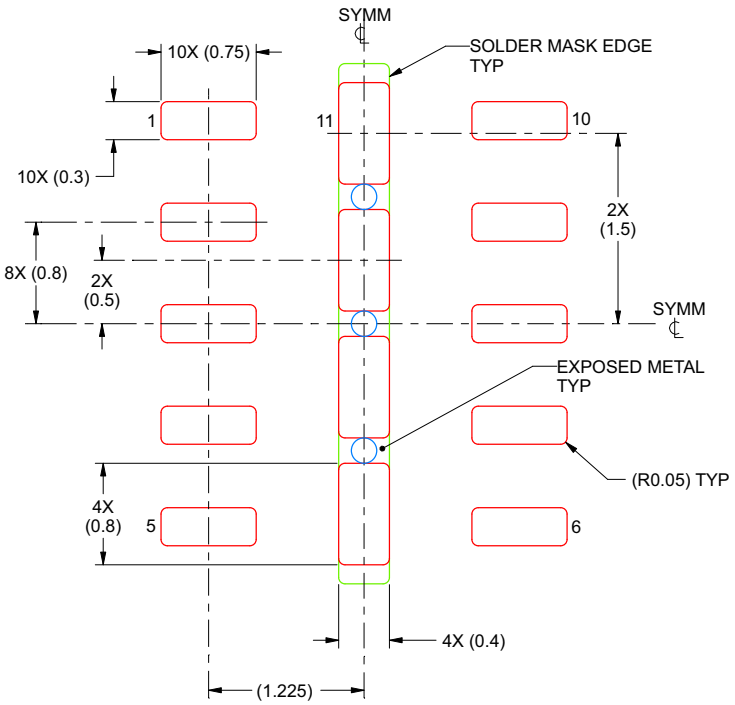
5. This package is designed to be soldered to thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

SIL0010C — **uSIP™ - 1.9 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

78% SOLDER COVERAGE BY PRINTED
AREA ON CENTER THERMAL PAD
SCALE:20X

4223804/B 06/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM265R1SILR	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM265R1
TPSM265R1SILR.A	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM265R1
TPSM265R1V3SILR	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM265R1V3
TPSM265R1V3SILR.A	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM265R1V3
TPSM265R1V5SILR	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM265R1V5
TPSM265R1V5SILR.A	Active	Production	uSiP (SIL) | 10	3000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM265R1V5

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

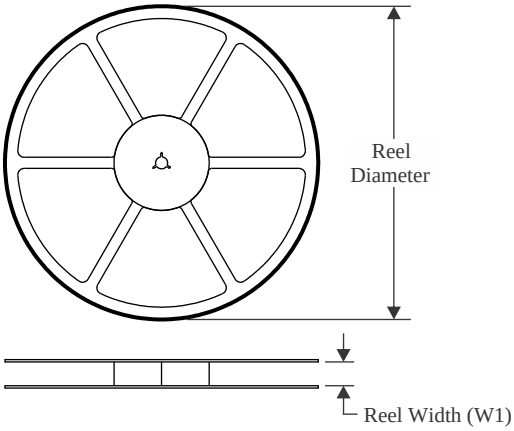
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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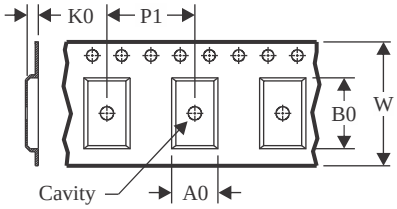
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

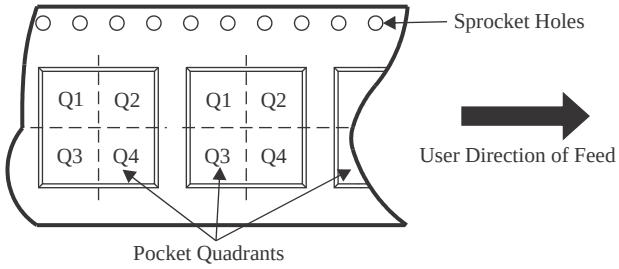


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

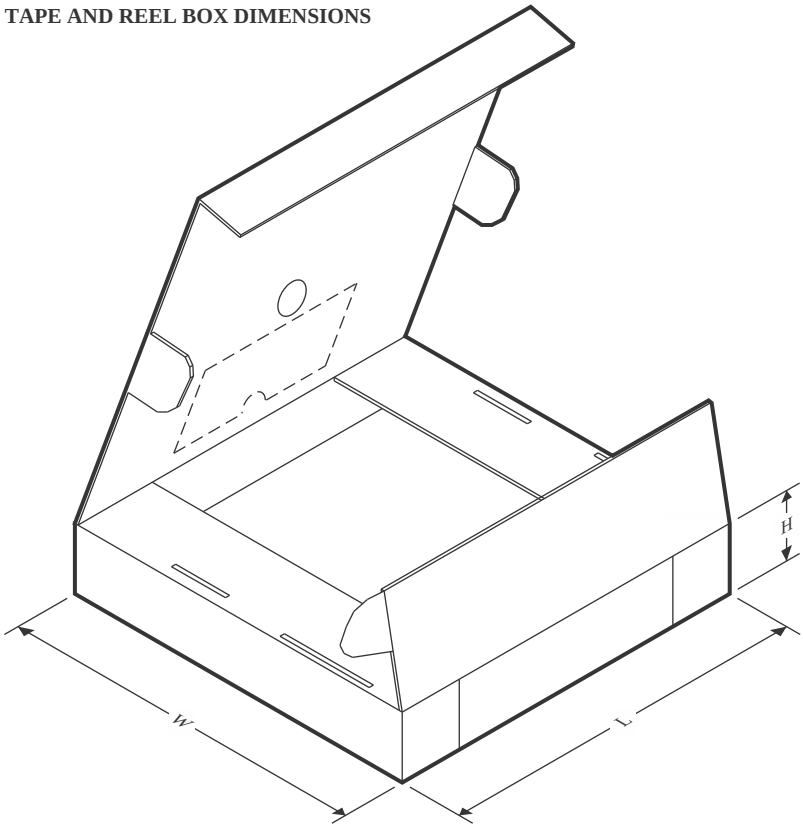
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM265R1SILR	uSiP	SIL	10	3000	330.0	12.4	3.15	4.05	2.15	8.0	12.0	Q1
TPSM265R1V3SILR	uSiP	SIL	10	3000	330.0	12.4	3.15	4.05	2.15	8.0	12.0	Q1
TPSM265R1V5SILR	uSiP	SIL	10	3000	330.0	12.4	3.15	4.05	2.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM265R1SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
TPSM265R1V3SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
TPSM265R1V5SILR	uSiP	SIL	10	3000	383.0	353.0	58.0

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