TEXAS INSTRUMENTS
TPSM365R1, TPSM365R15
JAJSPL6A – OCTOBER 2023 – REVISED DECEMBER 2023

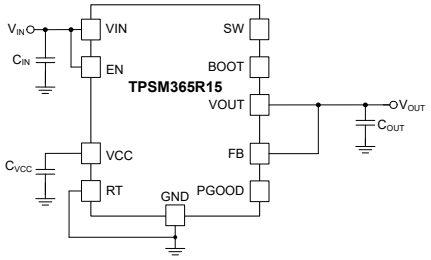
TPSM365R1x 3V～65V、100mA および 150mA、広い V_{IN}、サイズと軽負荷効率に最適化された同期整流降圧コンバータ電源モジュール

1 特長

- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- 多用途な同期整流降圧 DC/DC モジュール:
  - MOSFET、インダクタ、コントローラを内蔵
  - 3V～65V の広い入力電圧範囲
  - 最大 70V の入力過渡電圧
  - 接合部温度範囲:-40℃～+125℃
  - 4.5mm × 3.5mm × 2mm のオーバーモールド パッケージ
  - RT ピンを使用した 200kHz～2.2MHz の範囲の可変周波数
- 超低 EMI 要件に最適化:
  - 疑似ランダム スペクトラム拡散によりピーク エミッションを削減
  - 軽負荷時の固定周波数 FPWM モードを MODE/SYNC ピンで選択可能
  - MODE/SYNC ピンによる周波数同期
  - CISPR11 Class B 準拠
- スケーラブルな産業用電源に対応した設計:
  - TPSM365R3 (65V、300mA)、TPSM365R6 (65V、600mA)、TLVM23615 (36V、1.5A)、および TLVM23625 (36V、2.5A) とピン互換のファミリ
- 堅牢な設計のための本質的な保護機能
  - 高精度のイネーブル入力とオープン ドレインの PGOOD インジケータによる制御、シーケンシング、V_{IN} UVLO
  - 過電流およびサーマル シャットダウン保護機能
- WEBENCH® Power Designer により、TPSM365R15 を使用するカスタム設計を作成

2 アプリケーション

- ファクトリ オートメーション
- ビル オートメーション
- 家電製品



概略回路図

3 概要

TPSM365R1 および TPSM365R15 は、65V で 100mA および 150mA の同期整流降圧 DC/DC パワー モジュールで、パワー MOSFET、内蔵インダクタ、ブート コンデンサをコンパクトで使いやすい 3.5mm × 4.5mm × 2mm の 11 ピン QFN パッケージに統合しています。小型 HotRod ™ QFN パッケージ テクノロジーにより、放熱性能が向上し、EMI が低減されます。このデバイスは、無負荷時 4µA の超低動作 I_Q を実現します (V_{IN} = 24V、V_{OUT} = 3.3V)。TPSM365R1x は、3.3V および 5V の固定出力に加え、1V～16V の範囲の可変出力電圧をサポートしています。

TPSM365R1x は、ピーク電流モード制御アーキテクチャと内部補償により、最小の出力容量で安定した動作を維持します。RT ピンとグランドの間に抵抗を接続すると、スイッチング周波数は 200kHz～2.2MHz の広い範囲で任意の要求周波数で動作するようにプログラムされます。高精度の EN/UVLO 機能により、スタートアップおよびシャットダウン中もデバイスを精密に制御できます。PGOOD フラグは、内蔵グリッチ フィルタと遅延付き解除によってシステムの実際の状態を示すため、外部電圧のスーパーバイザは不要です。TPSM365R1x は設計サイズが小さく、豊富な機能セットがあるため、広範な産業用アプリケーションを簡単に実装できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPSM365R15	RDN (QFN-HR、11)	4.50mm × 3.50mm
TPSM365R1		

(1) 供給されているすべてのパッケージについては、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

製品情報

部品番号	定格出力電流 (1)
TPSM365R15	150mA
TPSM365R1	100mA

(1) 製品比較表を参照してください。

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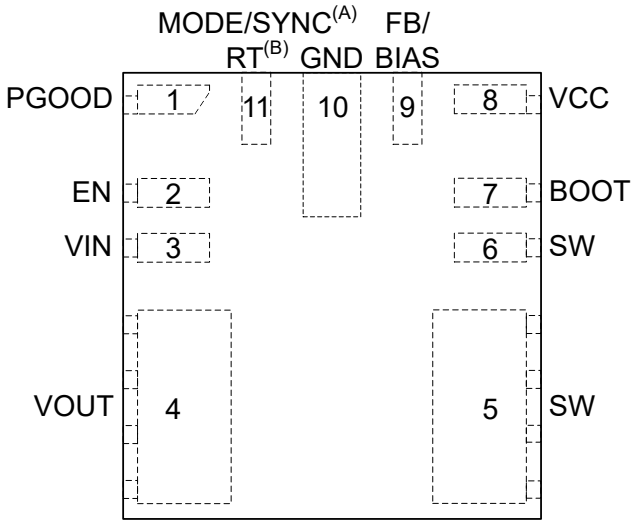
4 Device Comparison Table

ORDERABLE PART NUMBER (1)	RATED CURRENT	OUTPUT VOLTAGE	EXTERNAL SYNC	F_{SW}	SPREAD SPECTRUM
TPSM365R15RDNR	150 mA	Fixed 3.3 V / Adjustable (1 V – 16 V)	No (Default PFM at light load)	Adjustable with RT resistor	Yes
TPSM365R15FRDNR	150 mA	Fixed 5 V / Adjustable (1 V – 16 V)	Yes (PFM / FPWM Selectable)	Fixed 1 MHz	Yes
TPSM365R1RDNR	100 mA	Fixed 3.3 V / Adjustable (1 V – 16 V)	No (Default PFM at light load)	Adjustable with RT resistor	Yes
TPSM365R1FRDNR	100 mA	Fixed 5-V / Adjustable (1 V – 16 V)	Yes (PFM / FPWM Selectable)	Fixed 1 MHz	Yes

(1) For more information on device orderable part numbers, see *Device Nomenclature*. Contact TI for details and availability of other device options.

5 Pin Configuration and Functions



A. See *Device Comparison Table* for more details. Pin 11 trimmed and factory-set for externally adjustable switching frequency RT variants only

B. Pin 11 factory-set for fixed switching frequency MODE/SYNC variants only.

図 5-1. RDN Package, 11-Pin QFN-FCMOD, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	PGOOD	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. This pin goes low when EN = low. This pin can be open or grounded when not used.
2	EN	A	Enable input to regulator. High = ON, Low = OFF. Can be connected directly to VIN. *Do not float this pin.*
3	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor, C_{IN}, or capacitors directly to this pin and GND.
4	VOUT	P	Output voltage. The pin is connected to the internal output inductor. Connect the pin to the output load and connect external output capacitors between the pin and GND.
5, 6	SW	P	Power module switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
7	BOOT	P	Bootstrap pin for internal high-side driver circuitry. Do not place any external component on this pin or connect to any signal. A 100-nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage.
8	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
9	FB/BIAS	A	Feedback input. When operating as an adjustable output device, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to VOUT at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to GND. When connecting to a feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See *Output Voltage Selection* for how to select feedback resistor divider values. Check *Device Comparison Table* for more details. When operating with a fixed output voltage, connect this pin directly to the VOUT rail. This connection sets the output voltage to a fixed value and biases the internal circuitry. *Do not float this pin or connect to ground.*
10	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.

表 5-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NO.	NAME		
11	RT or MODE/SYNC	A	As the RT variant, the switching frequency can be adjusted from 200 kHz to 2.2 MHz. As the MODE/SYNC variant, the part can operate in user-selectable PFM/FPWM mode and can be synchronized to an external clock. See セクション 7.3.2 for details. *Do not float this pin.*
A = Analog, P = Power, G = Ground			

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VIN to GND	–0.3	70	V
	EN to GND	–0.3	70	V
	SW to GND	–0.3	70.3	V
	RT to GND	–0.3	5.5	V
Voltage	FB to GND	–0.3	16	V
Voltage	PGOOD to GND	0	20	V
	BOOT to SW	–0.3	5.5	V
Voltage	VCC to GND	–0.3	5.5	V
Voltage	VOUT to GND	–0.3	16	V
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G
T_J	Operating Junction Temperature	–40	125	°C
T_A	Operating Ambient temperature	–40	105	°C
T_{stg}	Storage Temperature	–55	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted). (1) (2)

			MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	Input voltage range after start-up	3		65	V
Output voltage	V_{OUT}	Adjustable output voltage range	1		16	V
Output current	I_{OUT}	(TPSM365R15) Load current range (3)	0		0.15	A
Output current	I_{OUT}	(TPSM365R1) Load current range (3)	0		0.1	A
Frequency setting	RT	Selectable frequency range with RT	0.2		2.2	MHz
Temperature	T_J	Operating Junction Temperature	–40		125	℃
Temperature	T_A	Operating Ambient Temperature	–40		105	℃

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the Electrical Characteristics table.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(3) Maximum continuous DC current can be de-rated when operating with high switching frequency or high ambient temperature. See Applications section for details.

6.4 Thermal Information

THERMAL METRIC[1]		TPSM365R15 / TPSM365R1 RDN 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM365R15EVM)	56.4	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	42.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter [3]	4.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter [4]	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The value of $R_{\theta JA}$ given in this table is valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. It does not represent the performance obtained in an actual application.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \cdot P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JB} \cdot P_{dis} + TB$; where P_{dis} is the power dissipated in the device and TB is the temperature of the board 1-mm from the device.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN_R}	Minimum operating input voltage (rising)	Rising threshold		3.4	3.55	V
V_{IN_F}	Minimum operating input voltage (falling)	Once operating; Falling threshold	2.45	3.0		V
I_{SD_13p5}	Shutdown quiescent current; measured at VIN pin [2]	V_{EN} = 0 V; V_{IN} = 13.5 V		0.55	1.1	µA
I_{SD_24p0}	Shutdown quiescent current; measured at VIN pin [2]	V_{EN} = 0 V; V_{IN} = 24 V		1	1.7	µA
$I_{Q\_13p5\_Fixed}$	Non-switching input current; measured at VIN pin [2]	V_{IN} = V_{EN} = 13.5 V; $V_{OUT/FB}$ = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed output	0.25	0.672	1.05	µA
$I_{Q\_13p5\_Adj}$	Non-switching input current; measured at VIN pin [2]	V_{IN} = V_{EN} = 13.5 V; V_{FB} = 1.05 V, $V_{MODE/SYNC}$ = 0 V; Adjustable output	13	17	23	µA
$I_{Q\_24p0\_Fixed}$	Non-switching input current; measured at VIN pin [2]	V_{IN} = V_{EN} = 24 V; $V_{OUT/FB}$ = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed output	0.8	1.2	1.7	µA
$I_{Q\_24p0\_Adj}$	Non-switching input current; measured at VIN pin [2]	V_{IN} = V_{EN} = 24 V; V_{FB} = 1.05 V, $V_{MODE/SYNC}$ = 0 V; Adjustable output	14	18	22	µA
I_{B_13p5}	Current into BIAS pin (not switching) [2]	V_{IN} = 13.5 V, $V_{OUT/FB}$ = 5.25 V, V_{RT} = 0 V; Fixed output	12	17	24	µA
I_{B_24p0}	Current into BIAS pin (not switching) [2]	V_{IN} = 24 V, $V_{OUT/FB}$ = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed output	12	18	24	µA
ENABLE (EN PIN)						
$V_{EN\text{-}WAKE}$	Enable wake-up threshold		0.4			V
$V_{EN\text{-}VOUT}$	Precision enable high level		1.16	1.263	1.36	V
$V_{EN\text{-}HYST}$	Enable threshold hysteresis		0.3	0.35	0.4	V
$I_{LKG\text{-}EN}$	Enable input leakage current	V_{EN} = 3.3 V		0.7	8	nA
INTERNAL LDO						

6.5 Electrical Characteristics (続き)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Internal VCC voltage	3.6 V ≤ V_{IN} ≤ 65 V; Adjustable output	3.1	3.15	3.26	V
I_{CC}	Bias regulator current limit			60	120	mA
$V_{CC-UVLO}$	Internal VCC undervoltage lockout	VCC rising under voltage threshold	3	3.3	3.65	V
$V_{CC-UVLO-HYST}$	Internal VCC under voltage lock-out hysteresis	Hysteresis below $V_{CC-UVLO}$	0.3	0.8	1.2	V
CURRENT LIMITS						
$I_{SC-100mA}$	Short circuit high side current limit (3)	100 mA version	140	167	200	mA
$I_{LS-LIMIT-100mA}$	Low side current limit (3)	100 mA version	99	116	135	mA
$I_{PEAK-MIN-100mA}$	Minimum peak inductor current limit (3)	PFM Operation, 100 mA version; Duty Cycle = 0%	30	40	50	mA
$I_{L-NEG-100mA}$	Sink current limit (negative) (3)	FPWM mode	-200	-175	-150	mA
$I_{SC-150mA}$	Short circuit high side current limit (3)	150 mA version	210	250	298	mA
$I_{LS-LIMIT-150mA}$	Low side current limit (3)	150 mA version	150	175	204	mA
$I_{PEAK-MIN-150mA}$	Minimum Peak Inductor Current (3)	PFM Operation, 150 mA version; Duty Cycle = 0%	55	70	85	mA
$I_{L-NEG-150mA}$	Sink current limit (negative) (3)	FPWM mode	-200	-175	-150	mA
I_{ZC}	Zero cross current (3)	Auto mode	0	2.5	5	mA
MOSFETS						
$R_{DSON-HS}$	High-side MOSFET on-resistance	Load = 100 mA		2.2		Ω
$R_{DSON-LS}$	Low-side MOSFET on-resistance	Load = 100 mA		1		Ω
$V_{BOOT-UVLO}$	BOOT - SW UVLO threshold (4)		2.14	2.3	2.42	V
OSCILLATOR (MODE/SYNC)						
$V_{SYNC-HIGH}$	Sync input and mode high level threshold		1.8			V
$V_{SYNC-LOW}$	Sync input and mode low level threshold				0.8	V
$V_{SYNC-HYS}$	Sync input hysteresis		230	300	380	mV
t_{PULSE_H}	High duration needed to be recognized as a pulse		100			ns
t_{PULSE_L}	Low duration needed to be recognized as a pulse		100			ns
t_{SYNC}	Maximum Pulse duration to sync to external CLK		6	9	12	µs
t_{MODE}	Time delay at one level needed to indicate FPWM or AUTO mode		18			µs
OSCILLATOR (RT)						
f_{OSC_2p2MHz}	Internal oscillator frequency	RT = GND	2.1	2.2	2.3	MHz
f_{OSC_1p0MHz}	Internal oscillator frequency	RT = VCC	0.93	1	1.05	MHz
f_{ADJ_400kHz}	Accuracy of external frequency, 400 kHz	RT = 39.2 kΩ	0.34	0.4	0.46	MHz
VOLTAGE FEEDBACK (VOUT/FB PIN)						
V_{OUT}	Output Voltage Accuracy for fixed V_{OUT}	V_{OUT} = 3.3-V, V_{IN} = 3.6 V to 65 V, FPWM	3.24	3.3	3.34	V
V_{OUT}	Output Voltage Accuracy for fixed V_{OUT}	V_{OUT} = 5-V, V_{IN} = 5.5 V to 65 V, FPWM	4.93	5	5.08	V
V_{REF}	Internal reference voltage	V_{IN} = 3.6 V to 65 V, FPWM mode	0.985	1	1.01	V

6.5 Electrical Characteristics (続き)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FB}	FB input current	Adjustable output, FB = 1 V		1	30	nA
SOFT START						
t_{SS}	Time from first SW pulse to V_{FB} at 90% of V_{REF}	V_{IN} ≥ 3.6 V	1.85	2.58	3.2	ms
POWER GOOD						
PG-OV	PGOOD upper threshold - rising	% of FB (Adjustable output) or % of VOUT/FB (Fixed output)	106	107	110	%
PG-UV	PGOOD lower threshold - falling	% of FB (Adjustable output) or % of VOUT/FB (Fixed output)	93	94	96.5	%
PG-HYS	PGOOD hysteresis - rising/falling	% of FB (Adjustable output) or % of VOUT/FB (Fixed output)	0.8	1.2	1.8	%
$V_{PG-VALID}$	Minimum input voltage for proper PG function		0.7	0.9	2	V
$R_{PG-EN5p0}$	PGOOD pulldown resistance	V_{EN} = 5.0 V, 1 mA pull-up current	20	40	70	Ω
R_{PG-EN0}	PGOOD pulldown resistance	V_{EN} = 0 V, 1 mA pull-up current	15	24	46	Ω
t_{RESET_FILTER}	Glitch filter time constant for PG function		15	25	40	µs
t_{PGOOD_ACT}	Delay time to PG high signal		1.7	1.956	2.16	ms
PWM LIMITS (SW)						
t_{ON-MIN}	Minimum switch on-time	V_{IN} = 24 V, I_{OUT} = 100 mA	40	57	80	ns
$t_{OFF-MIN}$	Minimum switch off-time		40	58	77	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	7.6	9	9.8	µs

(1) MIN and MAX limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.
(4) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turned on to recharge the boot capacitor.

6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 13.5 V, V_{BIAS} = 3.3-V V_{OUT}, I_{OUT} = 0 A, PFM mode (fixed output voltage)		6.5		µA
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24 V, V_{BIAS} = 3.3-V V_{OUT}, I_{OUT} = 0 A, PFM mode (fixed output voltage)		4		µA
D_{MAX}	Maximum switch duty cycle (1)			98		%
SPREAD SPECTRUM						
f_{SSS}	Frequency span of spread spectrum operation - largest deviation from center frequency (2)	Spread spectrum active		±2		%
f_{PSS}	Spread spectrum pseudo random pattern frequency (2)			0.98	1.5	Hz

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SD-R}	Thermal shutdown rising	Shutdown threshold	158	168	180	°C
T_{SD-HYS}	Thermal shutdown hysteresis		8	10	15	°C

(1) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $T_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} / (t_{ON-MAX} + $t_{OFF-MIN}$).
(2) Specified by design. Not production tested.

6.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 13.5 V.

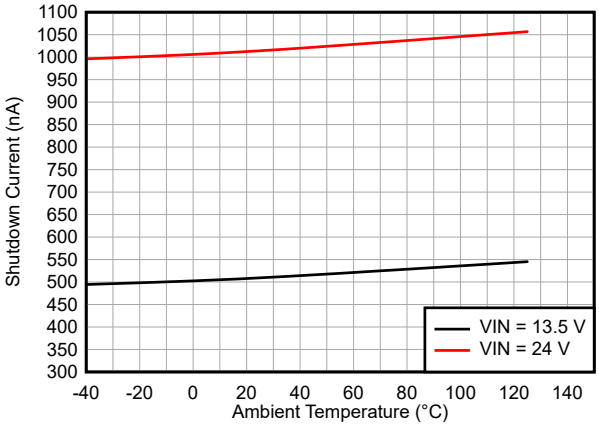


図 6-1. Shutdown Supply Current vs Ambient Temperature

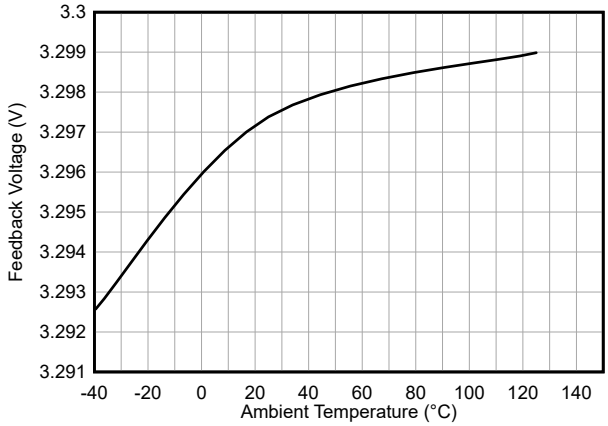


図 6-2. 3.3-V Feedback Voltage vs Temperature

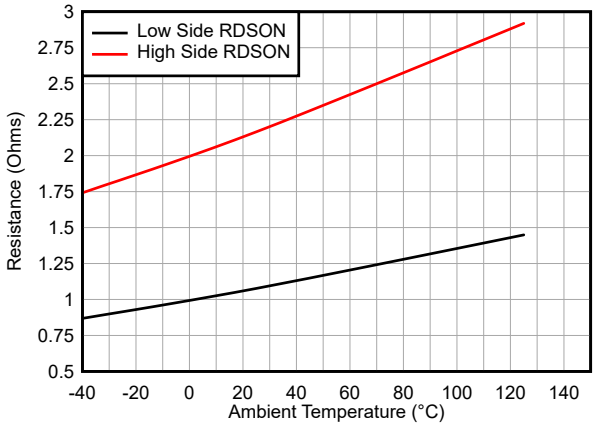


図 6-3. HSFET and LSFET R_{DSON} vs Temperature

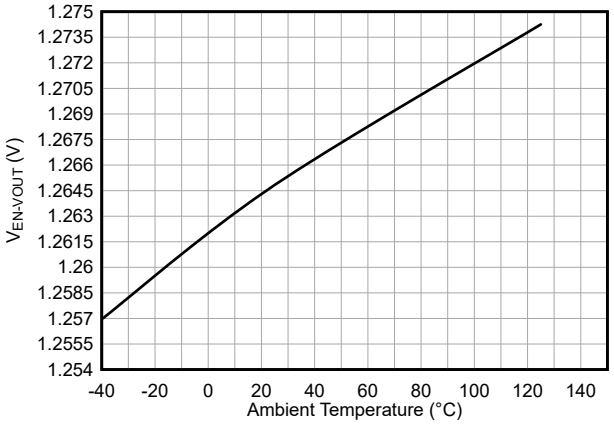


図 6-4. Precision Enable High Threshold vs Temperature

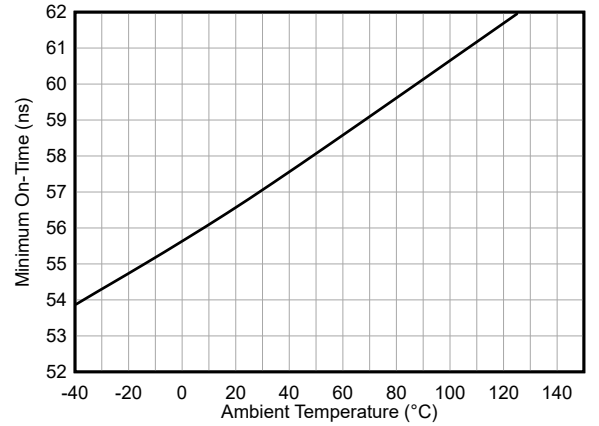


図 6-5. Minimum On-Time vs Temperature

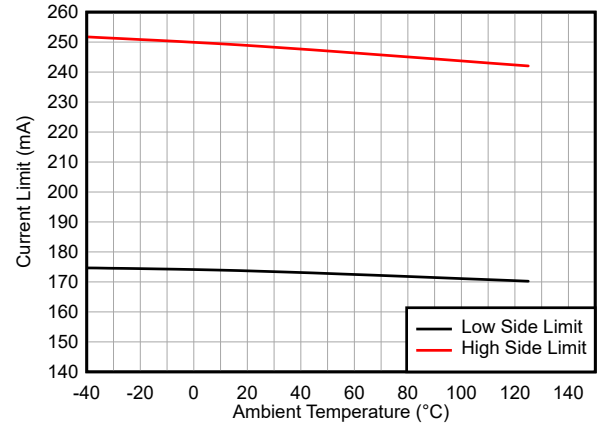


図 6-6. High-Side (Peak) and Low-Side Valley Current Limits

7 Detailed Description

7.1 Overview

The TPSM365R1x is an easy-to-use, synchronous buck, DC/DC power module that operates from a 3-V to 65-V supply voltage. With an integrated power controller, inductor, and MOSFETs, the TPSM365R1x delivers up to 150-mA or 100-mA DC load current with high efficiency and ultra-low input quiescent current in a very compact design size. The TPSM365R1x can operate over a wide range of switching frequencies and duty ratios. If the minimum ON-time or OFF-time cannot support the desired duty ratio, the switching frequency is reduced automatically, maintaining the output voltage regulation. Although designed for simple implementation, this device offers flexibility to optimize the usage according to the target application.

The TPSM365R1x module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing:
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Current limiting implemented by cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

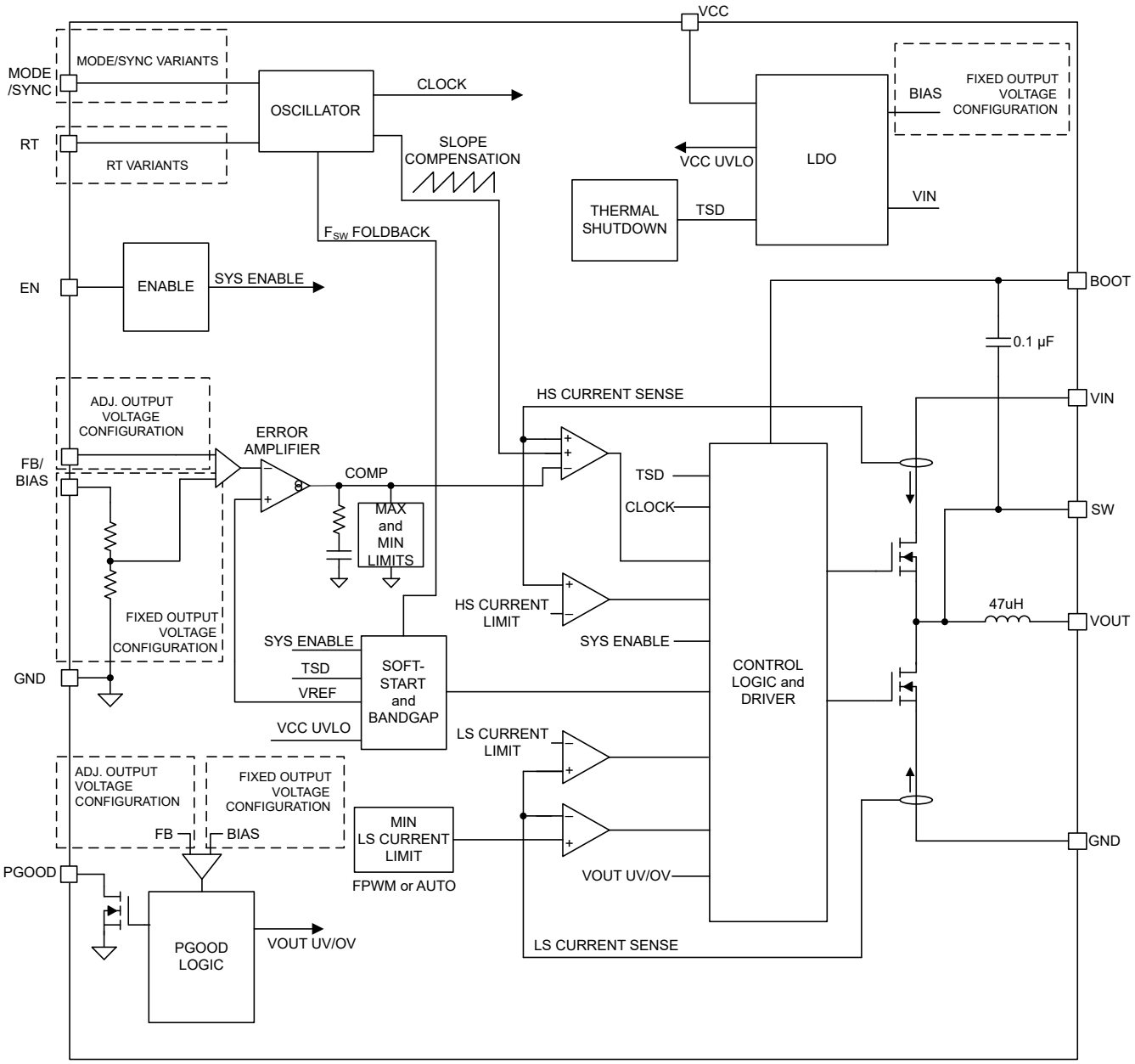
These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for a simple layout, requiring few external components. See *Layout* for a layout example.

The TPSM365R1x incorporates specific features to improve EMI performance in noise-sensitive applications:

- An optimized package that incorporates flip chip on lead (FCOL) technology and pinout design which enables a shielded switch-node layout that mitigates radiated EMI
- A programmable switching frequency from 200 kHz to 2.2 MHz enables optimization of external passives and promotes the avoidance of noise sensitive bands
- Pseudo-Random Spread Spectrum (PRSS) modulation reduces peak emissions
- Clock synchronization via the MODE/SYNC pin and FPWM mode enable constant switching frequency across the load current range

Together, these features reduce the need for any common-mode choke, shielding, and input filter inductor, greatly reducing the complexities and cost of the EMI/EMC mitigation measures.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable, Shutdown, and Start-Up

The voltage at the EN/UVLO pin controls the startup voltage and shut-down voltage of the TPSM365R1x. There are three distinct modes set by the EN/UVLO pin; shutdown, standby, and active. As long as the EN/UVLO pin voltage is less than $V_{EN-WAKE}$ the device is shutdown mode. During shutdown mode, the input current drawn by the device typically is 0.55 µA (V_{IN} = 13.5 V). The internal LDO regulator is not operational. When the voltage at the EN/UVLO pin is greater than the $V_{EN-WAKE}$ but less than $V_{EN-VOUT}$ the device enters the standby mode. In standby mode the internal LDO is enabled. As the EN/UVLO pin voltage increases above $V_{EN-VOUT}$, the device enters active mode starting the feedback resistor detection. After feedback detect is completed, soft-start functionality is released to slowly increases the output voltage and switching starts. To stop switching and enter standby mode the EN/UVLO pin must fall below ($V_{EN-VOUT}$ – $V_{EN-HYST}$). Any further decrease in the EN/UVLO pin voltage below $V_{EN-WAKE}$ the device is in shutdown. The various EN/UVLO threshold parameters and their values are listed in *セクション 6.5*. See セクション 7.3.7 for information about feedback resistor detection. 図 7-1 shows the precision enable behavior.

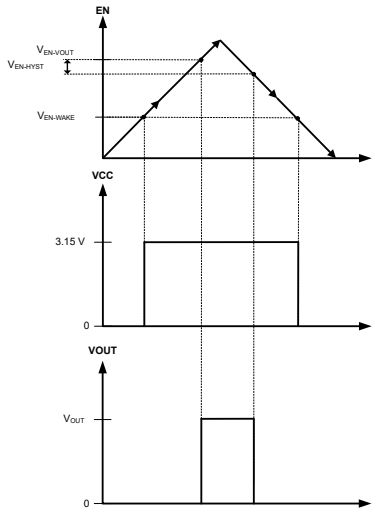


図 7-1. Precision Enable Behavior

Remote precision undervoltage lockout can be implemented with this functionality as shown in 図 7-2. See *セクション 8.2.2.8* for component selection.

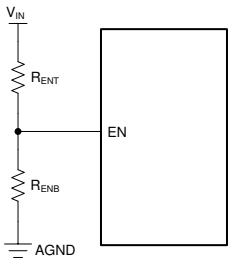


図 7-2. V_{IN} Undervoltage Lockout Using the EN/UVLO Pin

The high-voltage compliant EN/UVLO pin can be connected directly to the VIN input pin if remote precision control is not needed. The EN/UVLO pin must not be allowed to float. The various EN threshold parameters are listed in the セクション 6.5. 図 7-1 shows the precision enable behavior. After EN/UVLO goes above $V_{EN-VOUT}$ with a delay of about 1 ms, the output voltage begins to rise with a soft-start and reaches close to the final value in about 2.58 ms (t_{ss}). After a delay of about 2 ms (t_{PGOOD_ACT}), the PGOOD flag goes high. During startup, the

device is not allowed to enter FPWM mode until the soft-start time has elapsed. Check セクション 8.2.2.8 for component selection.

7.3.2 External CLK SYNC (With MODE/SYNC)

Synchronizing the operation of multiple regulators in a single system is often desirable, resulting in a well-defined system level performance. The select variants in the TPSM365R1x with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. The rising edge of the clock signal, provided to the MODE/SYNC pin of the TPSM365R1x, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL) eliminating any large glitches. The external clock fed into the TPSM365R1x replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided. If no external clock pulses are applied the MODE/SYNC pin can set the mode of operation, AUTO Mode or FPWM Mode.

The MODE/SYNC input pin of the TPSM365R1x can operate in one of three selectable modes:

- **AUTO Mode**: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See *セクション 7.4.3.2* for more details.
- **FPWM Mode**: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current. See *セクション 7.4.3.3* for more details.
- **SYNC Mode**: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off-time or minimum on-time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, it operates as though in FPWM mode: diode emulation is disabled allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

7.3.2.1 Pulse Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the TPSM365R1x are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-Dependent MODE/SYNC pin control is useful with these systems. To initiate Pulse-Dependent MODE/SYNC pin control, a valid sync signal must be applied. 表 7-1 shows a summary of the pulse dependent mode selection settings.

表 7-1. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{MODE_H}	FPWM with spread spectrum factory setting
< V_{MODE_L}	AUTO Mode with spread spectrum factory setting
Synchronization clock	SYNC mode

図 7-3 shows the transition between AUTO Mode and FPWM Mode while in Pulse-Dependent MODE/SYNC control. The TPSM365R1x transitions to a new mode of operation after the time, t_{MODE}. 図 7-3 and 図 7-4 show the details.

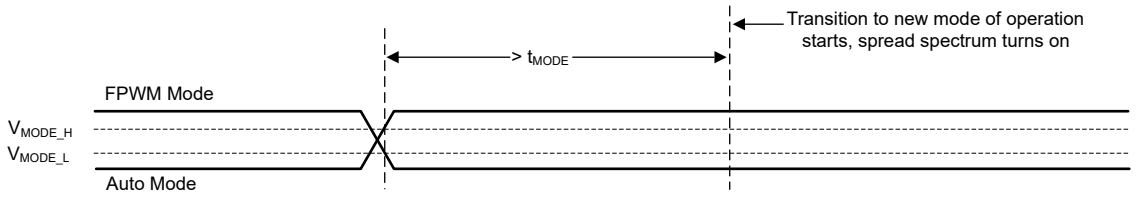


図 7-3. Transition from AUTO Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the TPSM365R1x enters either AUTO mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

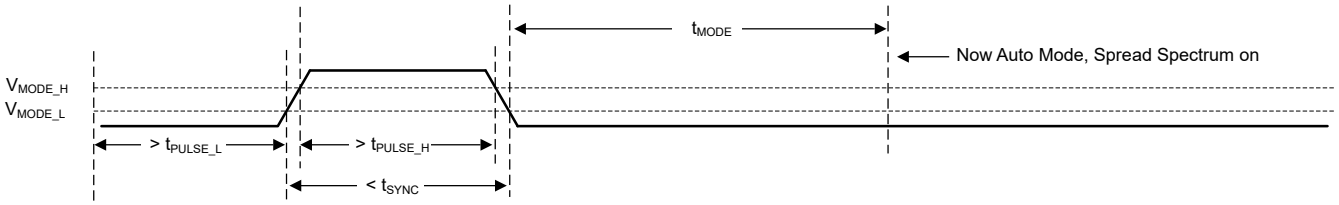


図 7-4. Transition from SYNC Mode to AUTO Mode

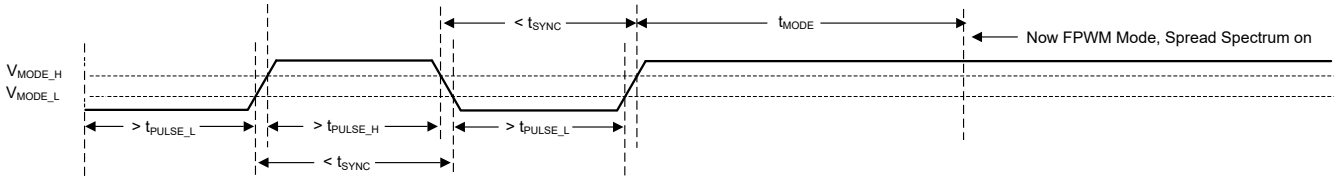


図 7-5. Transition from SYNC Mode to FPWM Mode

7.3.3 Adjustable Switching Frequency (with RT)

The select variants in the TPSM365R1x family with the RT pin allow the power designers to set any desired operating frequency between 200 kHz and 2.2 MHz in their applications. See 図 7-6 to determine the resistor value needed for the desired switching frequency. See 表 7-2 for selection on programming the RT pin.

表 7-2. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT to GND	Adjustable according to 図 7-6
Float (not recommended)	No switching

式 1 can be used to calculate the value of RT for a desired frequency.

$$RT = \frac{18286}{Fsw^{1.021}} \quad (1)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency (kHz).

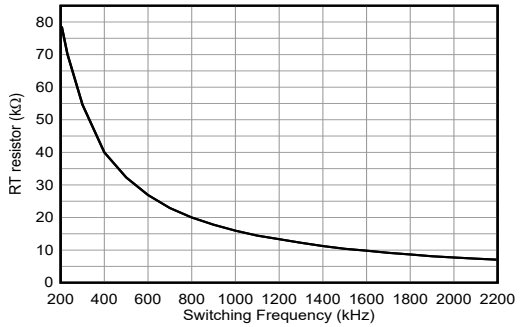


図 7-6. RT Values vs Frequency

7.3.4 Power-Good Output Operation

The power-good feature using the PGOOD pin of the TPSM365R1x can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal startup. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to 図 7-7. 表 7-3 gives a more detailed breakdown the PGOOD operation. Here, V_{PG-UV} is defined as the PG-UV scaled version of the $V_{OUT-Reg}$ (target regulated output voltage) and V_{PG-HYS} as the PG-HYS scaled version of the $V_{OUT-Reg}$, where both PG-UV and PG-HYS are listed in *セクション 6.5*. During the initial power up, a total delay of 5 ms (typical) is encountered from the time the $V_{EN-VOUT}$ is triggered to the time that the power-good is flagged high. This delay only occurs during the device startup and is not encountered during any other normal operation of the power-good function. When EN/UVLO is pulled low, the power-good flag output is also forced low. With EN/UVLO low, power-good remains valid as long as the input voltage ($V_{PG-VALID}$ is ≥ 0.9 V (typical)).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

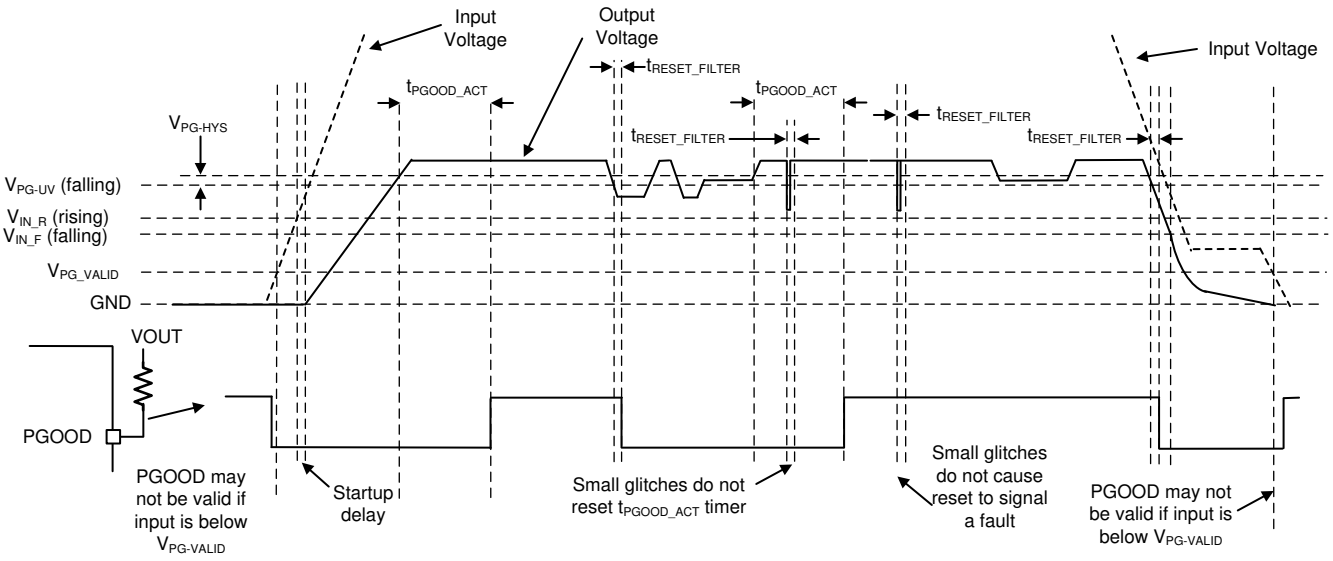


図 7-7. Power-Good Operation (OV Events Not Included)

表 7-3. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PG-UV}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PG-UV} + V_{PG-HYS} < V_{OUT} < V_{PG-OV} - V_{PG-HYS}$
$V_{OUT} > V_{PG-OV}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SD-R}$	$T_J < T_{SD-F}$ AND output voltage in regulation
$EN < V_{EN-VOUT} - V_{EN-HYST}$	$EN > V_{EN-VOUT}$ AND output voltage in regulation
$V_{CC} < V_{CC-UVLO} - V_{CC-UVLO-HYST}$	$V_{CC} > V_{CC-UVLO}$ AND output voltage in regulation

7.3.5 Internal LDO, VCC UVLO, and VOUT/FB Input

The TPSM365R1x uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the VIN (in adjustable output variants) or the VOUT/FB depending on how the output voltage is configured. In the fixed output configuration, after the TPSM365R1x is active but has yet to regulate, the VCC rail continues to draw power from the VIN pin, until the VOUT/FB voltage reaches greater than 3.15 V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.15 V in both adjustable and fixed output variants. To prevent unsafe operation, VCC has an undervoltage lockout, which prevents switching if the internal voltage is too low. See $V_{VCC-UVLO}$ and $V_{VCC-UVLO-HYST}$ in *セクション 6.5*. During start-up, VCC momentarily exceeds the normal operating voltage until $V_{VCC-UVLO}$ is exceeded, then drops to the normal operating voltage. Note that these undervoltage lockout values, when combined with the LDO dropout, drives the minimum input voltage rising and falling thresholds.

7.3.6 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to make sure the HS switch is turned on. The capacitor connected between BOOT and SW works as a charge pump to boost voltage on the BOOT terminal to (SW + VCC). A 100-nF boot capacitor is integrated in the TPSM365R1x to reduce overall external component count and minimize physical design size. The BOOT rail has an UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.3 V. If the C_{BOOT} capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

7.3.7 Output Voltage Selection

In the TPSM365R1x, each variant can be configured as a fixed output voltage or an adjustable output voltage. During device initialization the device configures the target output voltage to an internally selected value or an adjustable version by detecting if feedback resistors are present. When configuring the output voltage to be fixed value, simply connect the VOUT/FB pin to the system output voltage node. See *セクション 4* for the fixed output voltage setting of each variant.

To configure an adjustable output voltage, external feedback resistors are required as shown in 図 7-8. By connecting external feedback resistors with a parallel resistance greater than 5 kΩ but less than or equal to 10 kΩ (see *式 2*) the output voltage is set according as needed. The internal voltage reference is 1 V. Refer to セクション 8.2.2.3 for more details on how to adjust the output voltage.

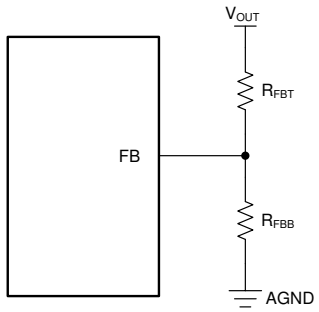


図 7-8. Setting Output Voltage for Adjustable Output Variant

$$5\ k\Omega\ <\ R_{FBT}||R_{FBB}\ \leq 10\ k\Omega \quad (2)$$

- R_{FBT} is the top resistor of the feedback divider
- R_{FBB} is the bottom resistor of the feedback divider

When configured in adjustable output voltage mode, an addition feed-forward capacitor, C_{FF}, in parallel with the R_{FBT}, can be used to optimize the phase margin and transient response. See *セクション 8.2.2.7* for more details. No additional resistor divider or feed-forward capacitor, C_{FF}, is needed in fixed-output variants.

Please refer to *表 7-4* for selecting passive component values for typical, output voltages.

表 7-4. Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)		V_{OUT} (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	10	DNP	300	47		3.3	33.2	14.3	1000	4.7
1.2	12.1	60.4	300	47		5.0	49.9	12.4	1000	4.7
1.5	15	30.1	400	33		7.5	75	11.5	1500	2.2
1.8	18.2	22.6	500	33		10	100	11	1800	2.2
2.0	20	20	500	22		12	121	10.7	2200	2.2
2.5	24.9	16.5	500	22		13	130	10.7	2200	2.2
3.0	30	15	800	4.7		15	150	10.7	2200	2.2

7.3.8 Spread Spectrum

The purpose of spread spectrum is to reduce peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The TPSM365R1x implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency can be easily filtered. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The TPSM365R1x uses a spread of frequencies, which can spread energy smoothly across the FM and TV bands, but is small enough to limit subharmonic emissions below the switching frequency of the part. Pseudo random frequency hopping allows the spread spectrum to be very effective at spreading the energy.

The TPSM365R1x uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo random pattern repeats at less than 1.5 Hz, which is below the audio band.

The spread spectrum is only available while the clock of the device is free running at the natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on time reaches minimum on time. See the *セクション 6.5*.
- The clock is synchronized with an external clock.

7.3.9 Soft Start and Recovery from Dropout

When designing with the TPSM365R1x, both soft start and recovery from dropout can cause slow rise in output voltage and must be considered as a two separate operating conditions, as shown in 図 7-9 and 図 7-10. These features ramp the output voltage at a controlled rate, keeping the output voltage from overshooting. See セクション 7.3.9.1 and セクション 7.3.9.2 for more details.

7.3.9.1 Soft Start

The soft-start feature allows the converter to gradually reach the steady state output voltage, reducing the startup stress in the system. Soft start is triggered by any of the following conditions:

- Appropriate voltage level is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN/UVLO voltage is sufficient to enter active mode while the voltage on VIN pin is at least V_{IN_R}.
- Recovery from shutdown due to overtemperature protection.

After soft start is triggered, the internal reference is slowly ramped up. Assuming the output voltage is initially 0 V, the reference is ramped to 90% of the target output voltage in t_{SS}. During the soft-start time, the switching

mode is set to AUTO mode. AUTO mode activates diode emulation for the low-side MOSFET, not allowing negative inductor current. This allows the output voltage to be pre-biased, voltage already present on the output, during start-up without discharging the output capacitor. 図 7-9 shows the difference between a non biased soft start and a pre-biased soft start.

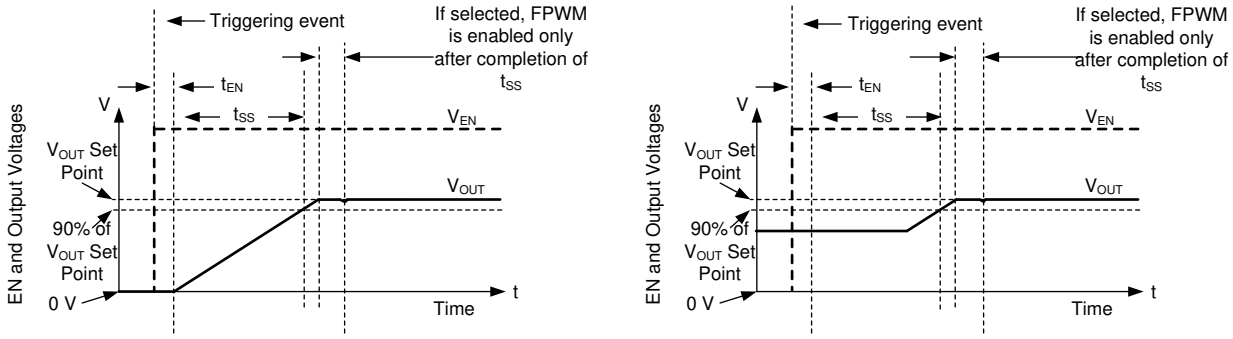


図 7-9. Soft Start With and Without Pre-biased Voltage

7.3.9.2 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device mode is set to FPWM, it continues to operate in that mode during the recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the TPSM365R1x can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

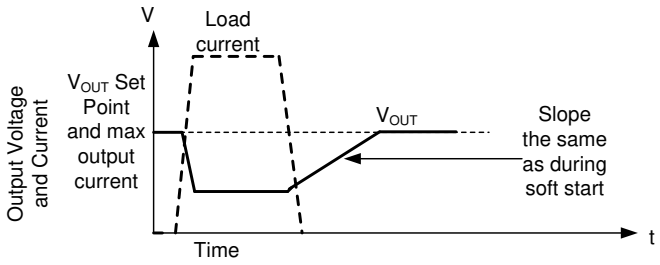


図 7-10. Recovery from Dropout

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below set point is removed, the output climbs at the same speed as during start-up.

7.3.10 Current Limit and Short Circuit

The TPSM365R1x are protected from overcurrent conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs.

High-side (HS) MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Because the output of the internal error amplifier loop

has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the low-side (LS) switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device has a turn-off commanded by the internal error amplifier loop. In the case of the low-side device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This limit is called the low-side current limit, $I_{LS-LIMIT}$ in 図 7-11. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed because the last time the HS device has turned on.

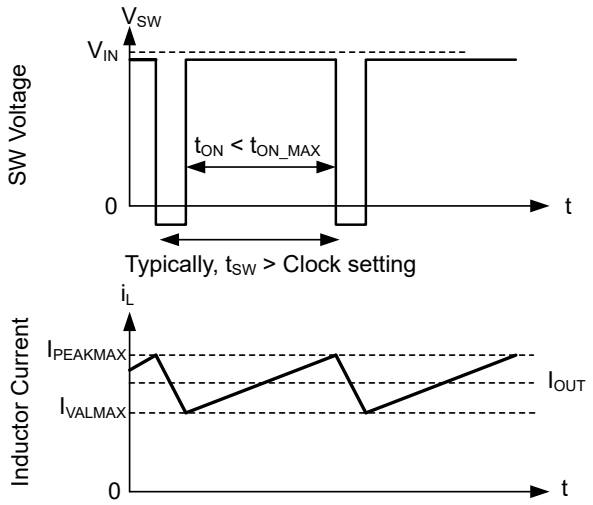


図 7-11. Current Limit Waveforms

Because the current waveform assumes values between I_{SC} and $I_{LS-LIMIT}$, the maximum output current is very close to the average of these two values unless duty factor is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If the duty factor is very high, current ripple must be very low to prevent instability. Because current ripple is low, the part is able to deliver full current. The current delivered is very close to $I_{LS-LIMIT}$.

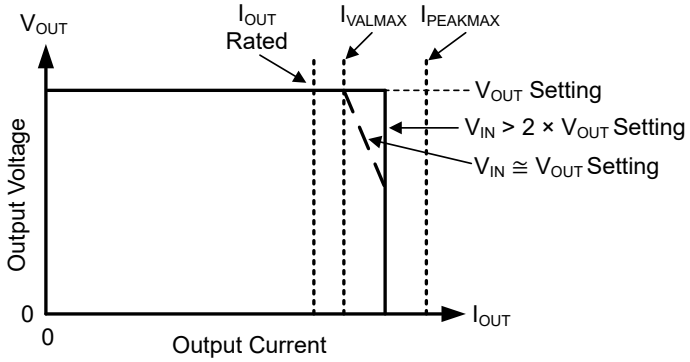


図 7-12. Output Voltage versus Output Current

7.3.11 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 158°C (typical). When the junction temperature falls below 158°C (typical), the TPSM365R1x attempts another soft start.

While the TPSM365R1x is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.3.12 Input Supply Current

The TPSM365R1x is designed to have very low input supply current when regulating light loads. When configured as a fixed output voltage, the FB/BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the FB/BIAS input pin to the output node of the regulator, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN}.

When configured as an adjustable output voltage, the internal LDO is powered by VIN. This action results in higher power loss through the internal LDO which results in lower efficiency compared to a fixed output configuration.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN/UVLO pin provides electrical on and off control of the device. When the EN/UVLO pin voltage is below 0.4 V, the internal LDO is disabled and there is no switching of the internal power MOSFETs. In shutdown mode, the quiescent current drops to 0.55 µA (typical) when V_{IN} is 13.5 V.

7.4.2 Standby Mode

When the EN/UVLO pin voltage is greater than the $V_{EN-WAKE}$ but less than $V_{EN-VOUT}$, the internal LDO is enabled. The precision enable circuitry is enabled after VCC is above the undervoltage threshold ($V_{CC-UVLO}$). The internal power MOSFETs remain off unless the voltage on EN/UVLO pin voltage goes above the precision enable threshold ($V_{EN-VOUT}$) and the input voltage on VIN pin is greater than V_{IN_R}.

7.4.3 Active Mode

The TPSM365R1x is in active mode whenever the EN/UVLO pin is above $V_{EN-VOUT}$, V_{IN} is high enough to satisfy V_{IN_R}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN/UVLO pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{IN_R}.

In active mode, depending on the load current, input voltage, and output voltage, the TPSM365R1x is in one of five modes:

- ***Continuous conduction mode*** (CCM) with fixed switching frequency when load current is above half of the inductor current ripple
- ***AUTO Mode*** - Light Load Operation: PFM when switching frequency is decreased at very light load
- ***FPWM Mode*** - Light Load Operation: Continuous conduction mode (CCM) when the load current is lower than half of the inductor current ripple
- ***Minimum on-time***: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation.
- ***Dropout mode***: When switching frequency is reduced to minimize voltage dropout between input and output.

7.4.3.1 CCM Mode

The following operating description of the TPSM365R1x refers to *セクション 7.2* and to the waveforms in 図 7-13. The TPSM365R1x has two behaviors while lightly loaded, AUTO mode and FPWM mode. Regardless of the

light load operation configuration the converter operates in CCM when the load current is greater than half the inductor ripple current.

In CCM, the TPSM365R1x supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on-time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. Duty cycle is defined by the on-time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (3)$$

In an ideal buck converter where losses are ignored, duty cycle is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (4)$$

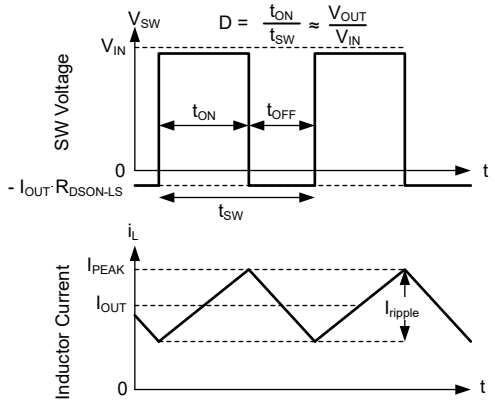


図 7-13. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

7.4.3.2 AUTO Mode - Light Load Operation

AUTO mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the TPSM365R1x operates in depends on which variant from this family is selected. Note that variants with a MODE/SYNC pin operate in FPWM mode when synchronizing frequency to an external signal.

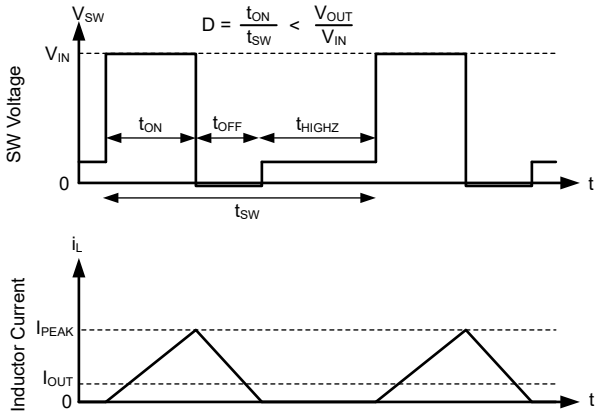
The light load operation is employed in the TPSM365R1x only in the AUTO mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation. See 図 7-14.
- Frequency reduction. See 図 7-15.

Note that while these two features operate together to improve light load efficiency, they operate independent of each other.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



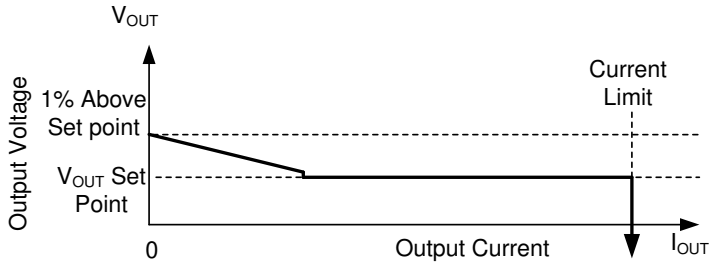
In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple can be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

図 7-14. PFM Operation

The TPSM365R1x has a minimum peak inductor current setting (see $I_{PEAK-MIN}$ in *セクション 6.5*) while in auto mode. After current is reduced to a low value with fixed input voltage, on-time is held constant. Regulation is then achieved by adjusting frequency. This mode of operation is called Pulse Frequency Modulation (PFM) mode.

7.4.3.2.2 Frequency Reduction

The TPSM365R1x reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



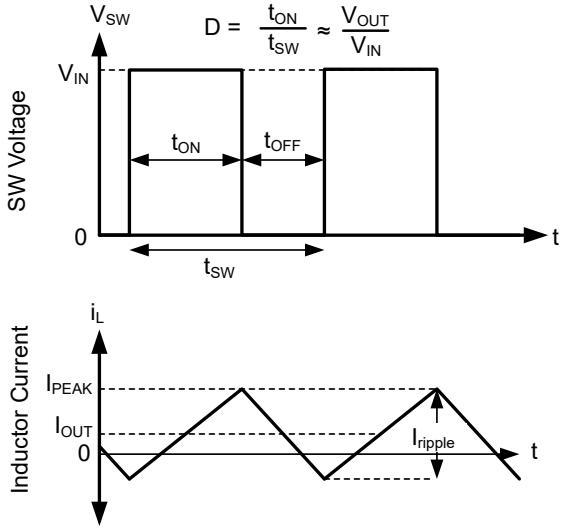
In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

図 7-15. Steady State Output Voltage versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM Mode can be used to reduce or eliminate this offset.

7.4.3.3 FPWM Mode - Light Load Operation

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see *セクション 6.5* for reverse current limit values (I_{L-NEG}).



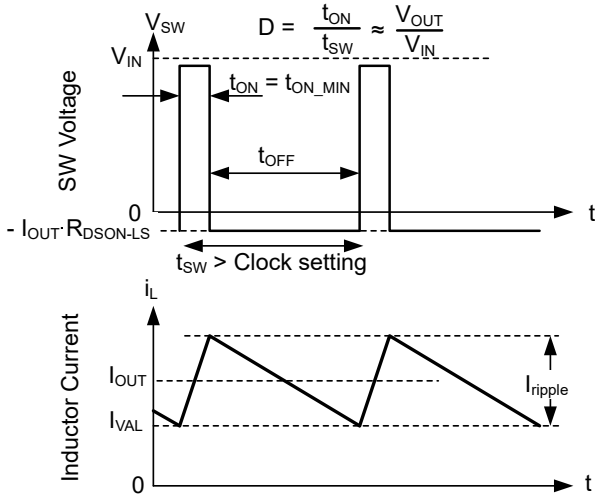
In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

図 7-16. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

7.4.3.4 Minimum On-time Operation

The TPSM365R1x continue to regulate output voltage even if the input-to-output voltage ratio requires an on-time less than the minimum (t_{ON-MIN}). This action is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on-time is fixed at the minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see 図 7-17.

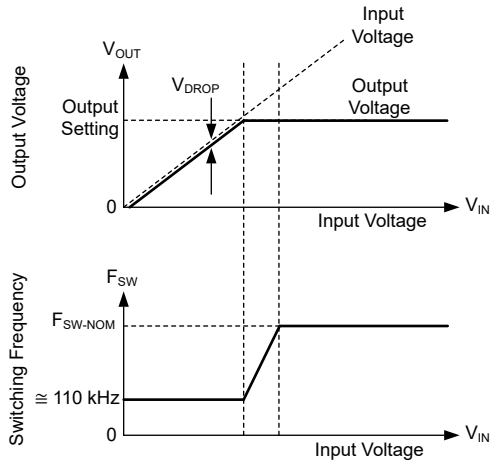


In valley control mode, minimum inductor current is regulated, not peak inductor current.

図 7-17. Valley Current Mode Operation

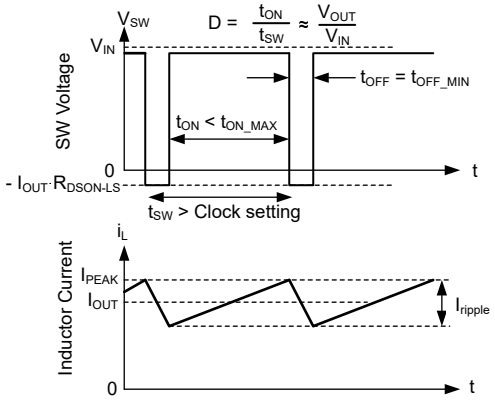
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off-time. After this limit is reached as shown in 図 7-19 if clock frequency was to be maintained, the output voltage falls. Instead of allowing the output voltage to drop, the TPSM365R1x extends the high side switch on-time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on-time, t_{ON-MAX}, of approximately 9 µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. As shown in 図 7-18 if input voltage is low enough so that output voltage cannot be regulated even with an on-time of t_{ON-MAX}, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer back to 図 7-10.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

図 7-18. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON-MAX}.

図 7-19. Dropout Waveforms

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM365R15 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM365R15, WEBENCH online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM365R15 power module.

The TPSM365R15 integrates several optional features to meet system design requirements, including precision enable, UVLO, and PGOOD indicator. The application circuit detailed below shows TPSM365R15 configuration options designed for several application use cases. Refer to the *TPSM365R15EVM, TPSM365R15FEVM User's Guide* for more detail.

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All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This action can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

図 8-1 and 図 8-2 show two typical application circuits for the TPSM365R15.

図 8-1 switching frequency can be programmed from 200 kHz to 2.2 MHz with a RT resistor. Connecting RT to VCC or GND (or comparable source) programs the frequency for either 1 MHz or 2.2 MHz, respectfully. The output voltage can be configured for fixed, 3.3-V configuration by shorting VOUT to FB and depopulating R_{FBB}.

図 8-2 pin 11 definition changes to MODE/SYNC. This pin can be connected to VCC or GND (or comparable source) for FPWM or auto mode operation, respectfully.

Both designs are capable of having an output voltage ranging from 1 V to 16 V. *Detailed Design Procedure* outlines the procedure to designing a 5-V output with TPSM365R15F. This design can be used in a factory automation, 4-20 mA loop design due to the low-noise, small design size, and modest efficiency over the entire load range.

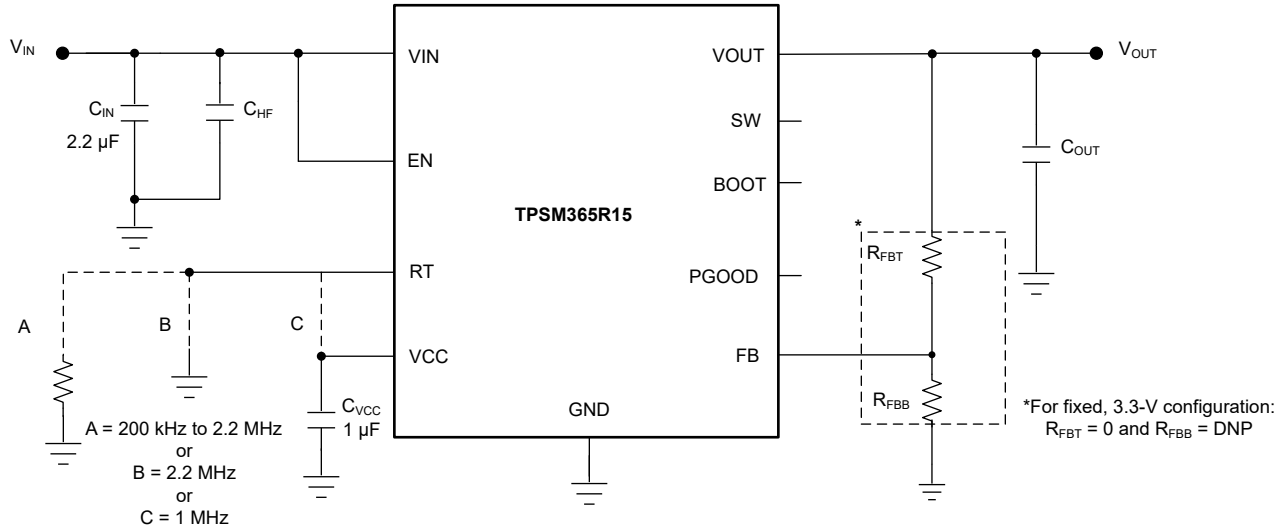


図 8-1. Example Application Circuit (TPSM365R15)

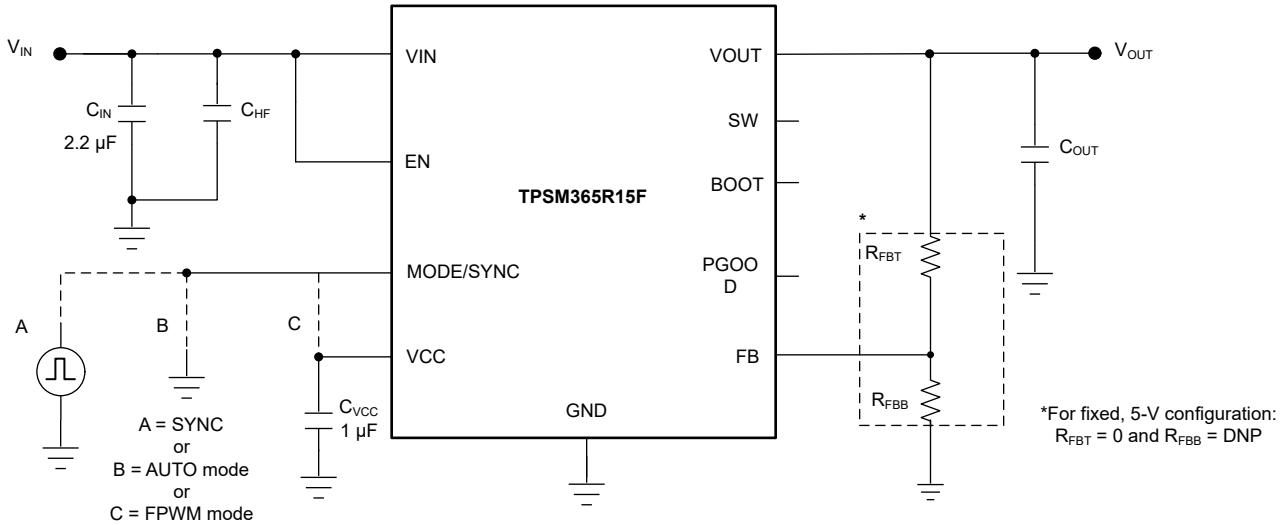


図 8-2. Example Application Circuit (TPSM365R15F)

8.2.1 Design Requirements

セクション 8.2.2 provides instructions to design and select components according to 表 8-1.

表 8-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5.5 V to 65 V
Output voltage	5 V
Maximum output current	0 to 150 mA
Switching frequency	1 MHz

8.2.2 Detailed Design Procedure

The design procedure that follows and the resulting component selection is illustrated in 図 8-3.

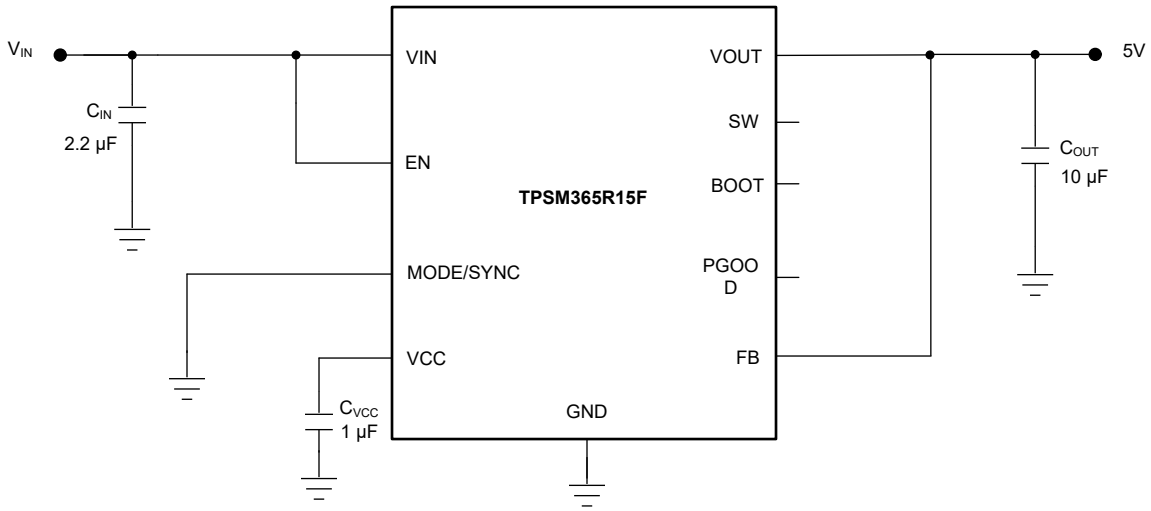


図 8-3. 5-V Output Design Example

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM365R1x with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible devices from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability. In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Choosing the Switching Frequency

The recommended switching frequency for standard output voltages can be found in Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT} . For a 5-V output, the recommended switching frequency is 1 MHz, which TPS365R15F operates at by default.

8.2.2.3 Setting the Output Voltage

Fixed output configuration allows the feedback resistors to be eliminated and the layout to be simplified. TPSM365R15F can be configured for 5 V, fixed configuration by shorting V_{OUT} to FB, for which this design does. See Device Comparison Table for the selection of fixed output voltage versions.

The device can be configured for adjustable output voltage in the case a different output voltage is required, as example. For more information on how to choose the feedback resistor values, please see *セクション 7.3.7*. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be selected from Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT} or calculated using 式 5:

$$R_{FBT}[k\Omega] = R_{FBB}[k\Omega] \times \left(\frac{V_{OUT}[V]}{1V} - 1 \right) \quad (5)$$

8.2.2.4 Input Capacitor Selection

The TPSM365R15(F) design uses a 2.2-µF input capacitor to keep the input, voltage ripple small. TI recommends an additional 0.1-µF capacitor in parallel for improved bypassing (lower noise). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage. For this design, a 2.2-µF, 100-V rated capacitor is used.

Using an electrolytic capacitor on the input in parallel with the ceramics is often desirable. This fact is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

8.2.2.5 Output Capacitor Selection

For a 5-V output, the TPSM365R15(F) requires a minimum of 4.7-µF effective output capacitance for proper operation (see Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT}). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

This design uses a 10-µF, 10-V, 1206 capacitor which is approximately 5 µF at 5-V DC bias. A smaller case size capacitor, or lower DC rating, does not provide adequate, effective capacitance for this design.

8.2.2.6 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see *Power-Good Output Operation*). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3 V; see *セクション 6.5* for limits.

8.2.2.7 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor application report* is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of C_{FF} must be limited to make sure that the desired output voltage is established when configuring for adjustable output voltages. 式 6 must be followed to make sure C_{FF} remains below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}}}{1.2 \times 10^{6}} \quad (6)$$

8.2.2.8 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This need can be accomplished by using the circuit shown in 図 8-4. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 式 7and 式 8 are used to calculate R_{ENT} and V_{OFF}, respectively.

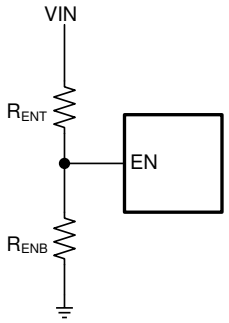


図 8-4. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1\right) \times R_{ENB} \quad (7)$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYS}}{V_{ENVOUT}}\right) \quad (8)$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.

8.2.2.9 Power-Good Signal

Applications requiring a power-good signal to indicate that the output voltage is present and in regulation must use a pullup resistor between the PGOOD pin and a valid voltage source. This voltage source can be VCC or VOUT, as example.

8.2.2.10 Maximum Ambient Temperature

As with any power conversion device, the TPSM365R15(F) dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the power module above ambient. The internal die and inductor temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the module and PCB combination. The maximum junction temperature for the TPSM365R15(F) must be limited to 125°C. This limit establishes a limit on the maximum module power dissipation and, therefore, the load current. 式 9 shows the relationships between the important parameters. Seeing that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current is easy. Being that the power dissipation is relatively low in this module, this device must be capable of supporting the maximum ambient temperature rating, across the majority of power conditions with a modest size 2 layer or 4 layer PCB. Further thermal analysis can be done by measuring the top case temperature on the EVM which is nearly equivalent to the junction due to the thin case.

As stated in the *Semiconductor and IC Package Thermal Metrics application report* the values given in *セクション 6.4* section are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT,\,max} = \frac{\left(T_J - T_A\right)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{\eta} \tag{9}$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ (TPSM365R15 approximately 56°C/W at 24 V_{IN}, 5 V_{OUT}, 150 mA, 1 MHz,) is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The IC Power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC resistance. The overall power loss can be approximated by using WEBENCH for a specific operating condition and temperature.

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight application report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application report*
- *Semiconductor and IC Package Thermal Metrics application report*
- *Thermal Design Made Simple with LM43603 and LM43602 application report*
- *PowerPAD™ Thermally Enhanced Package application report*
- *PowerPAD™ Made Easy application report*
- *Using New Thermal Metrics application report*
- *PCB Thermal Calculator*

8.2.2.11 Other Connections

- The RT pin can be connected to AGND for a switching frequency of 2.2 MHz or tied to VCC for a switching frequency of 1 MHz. A resistor connected between the RT pin and GND can be used to set the desired operating frequency between 200 kHz and 2.2 MHz.
- For the MODE/SYNC pin variant, connecting this pin to an external clock forces the device into SYNC operation. Connecting the MODE/SYNC pin low allows the device to operate in PFM mode at light load. Connecting the MODE/SYNC pin high puts the device into FPWM mode and allows full frequency operation independent of load current.
- A resistor divider network on the EN pin can be added for a precision input undervoltage lockout (UVLO)
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.
- A pullup resistor between the PGOOD pin and a valid voltage source to generate a power-good signal.

8.2.3 Application Curves

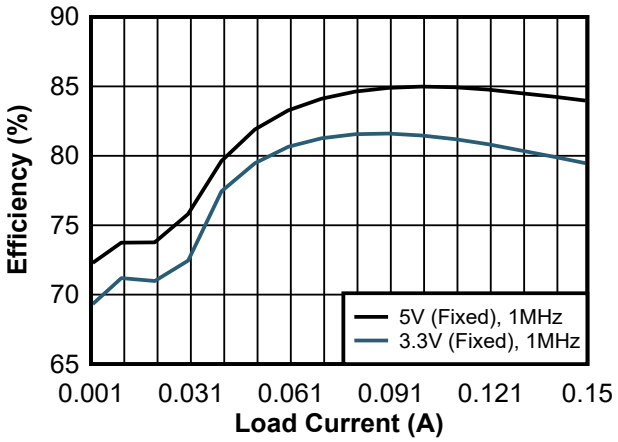


図 8-5. 12VIN Efficiency

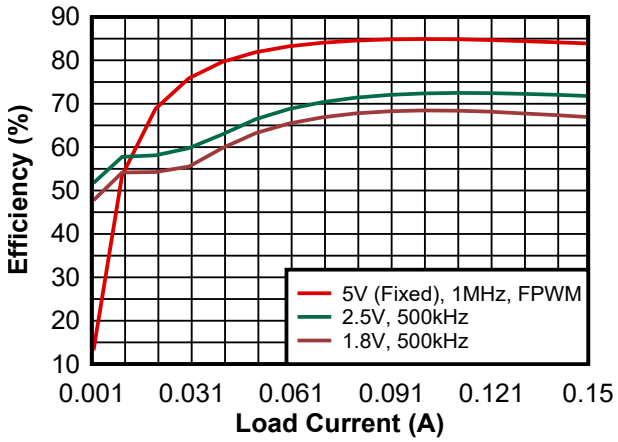


図 8-6. 12VIN Efficiency

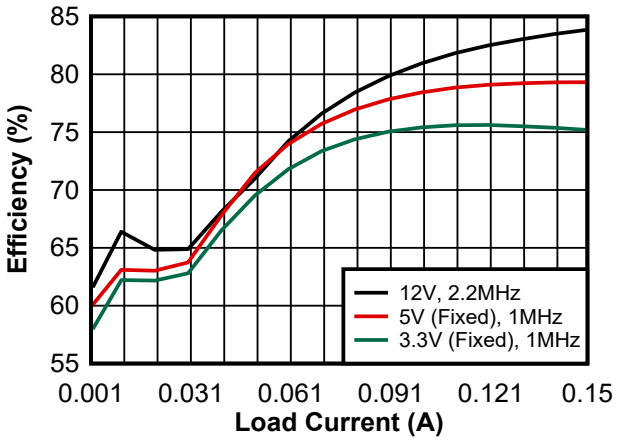


図 8-7. 24VIN Efficiency

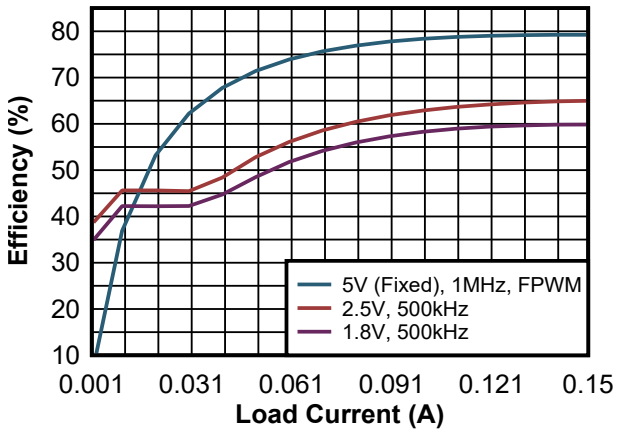


図 8-8. 24VIN Efficiency

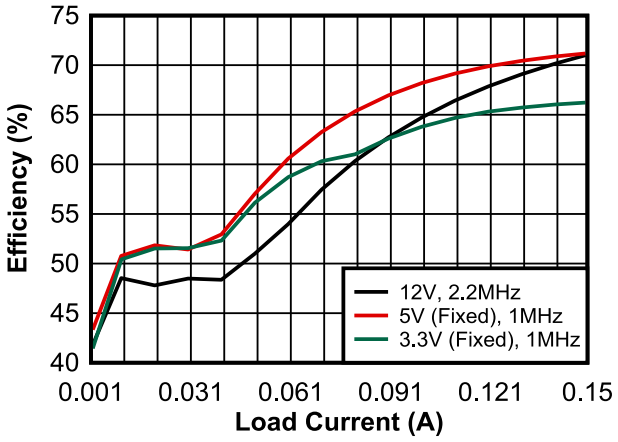


図 8-9. 48VIN Efficiency

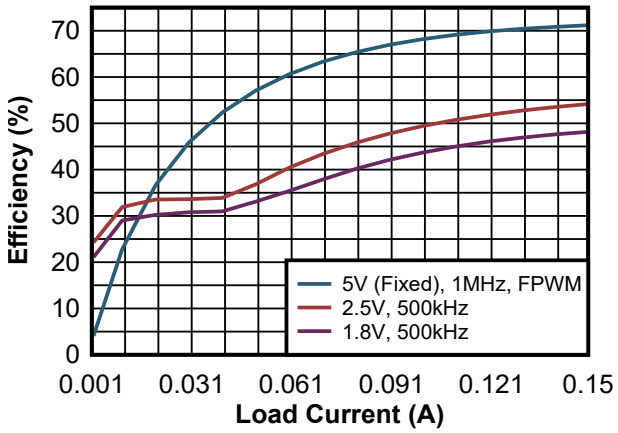
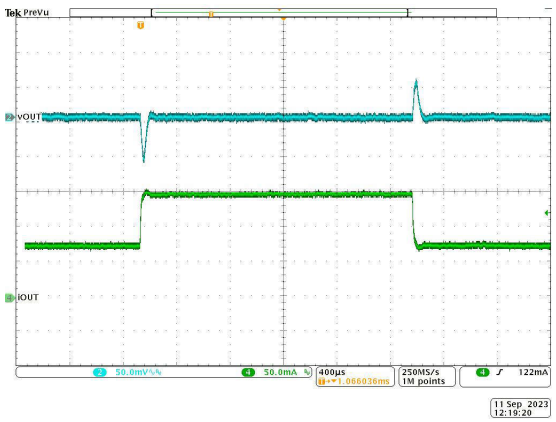


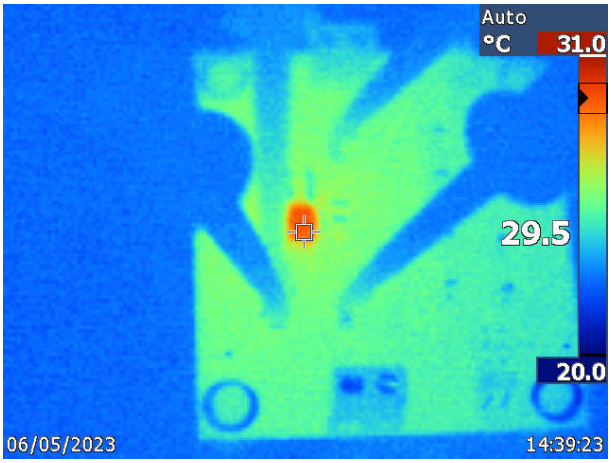
図 8-10. 48VIN Efficiency

8.2.3 Application Curves (continued)



V_{IN} = 24 V　　V_{OUT} = 3.3 V (Fixed)　　2.2 MHz
75 mA to 150 mA,　　COUT = 1 × 10 uF
50 mA/µs　　(1206, 10VDC)

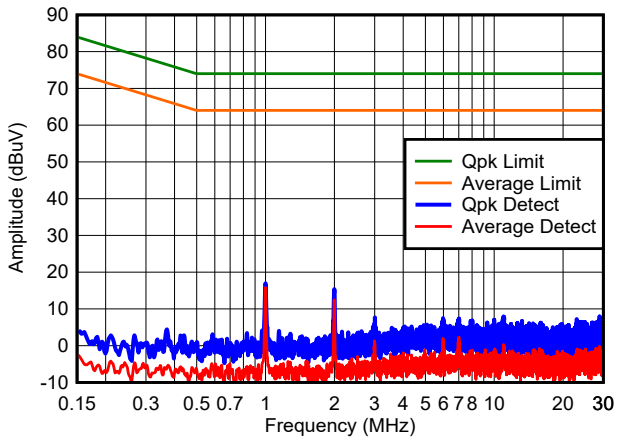
図 8-11. Load Transient



V_{IN} = 24 V　　V_{OUT} = 5 V　　150 mA, 1 MHz

図 8-12. EVM Thermal Performance

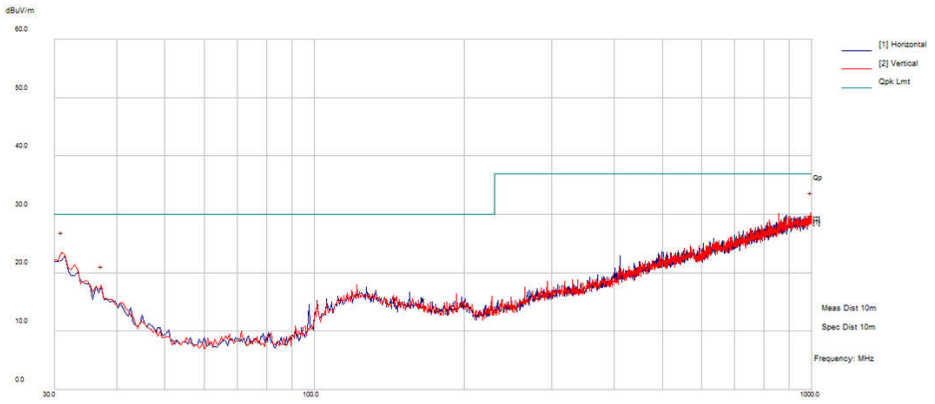
CISPR 11/32 Class B Conducted Emmissions



V_{IN} = 24 V　　V_{OUT} = 5 V　　Fsw = 1 MHz
Board = TPSM365R15EVM (Unmodified)　　Load = 150 mA

図 8-13. CISPR 11, Class B, CE Scan 150 kHz – 30 MHz

8.2.3 Application Curves (continued)



V_{IN} = 24 V V_{OUT} = 5 V Fsw = 1 MHz

Board = TPSM365R15EVM (Unmodified) Load =150 mA

図 8-14. CISPR 11/32, Class B, RE, 10-Meter Scan 30 MHz – 1 GHz

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

8.4 Power Supply Recommendations

The TPSM365R15 buck module is designed to operate over a wide input voltage range of 3 V to 65 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with 式 10.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{10}$$

where

- η is the efficiency

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

8.5 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

8.5.1 Layout Guidelines

The PCB layout of any DC/DC module is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the module regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter module, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 図 8-15. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the power module. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. *Layout Example* shows a recommended layout for the critical components of the TPSM365R15.

1. *Place the input capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
4. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
5. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the power module and maximizes efficiency.
6. *Provide enough PCB area for proper heat-sinking.* Sufficient amount of copper area must be used to make sure of a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
7. *Use multiple vias* to connect the power planes to internal layers.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies application report*
- *Simple Switcher PCB Layout Guidelines application report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x application report*

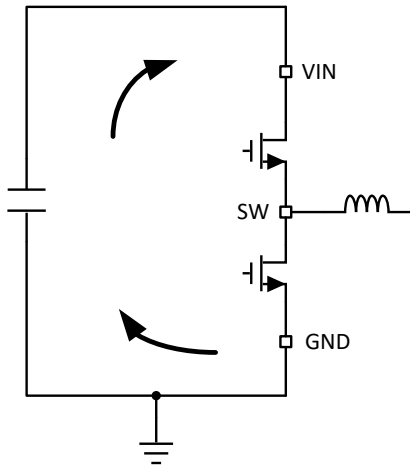


図 8-15. Current Loops with Fast Edges

8.5.2 Layout Example

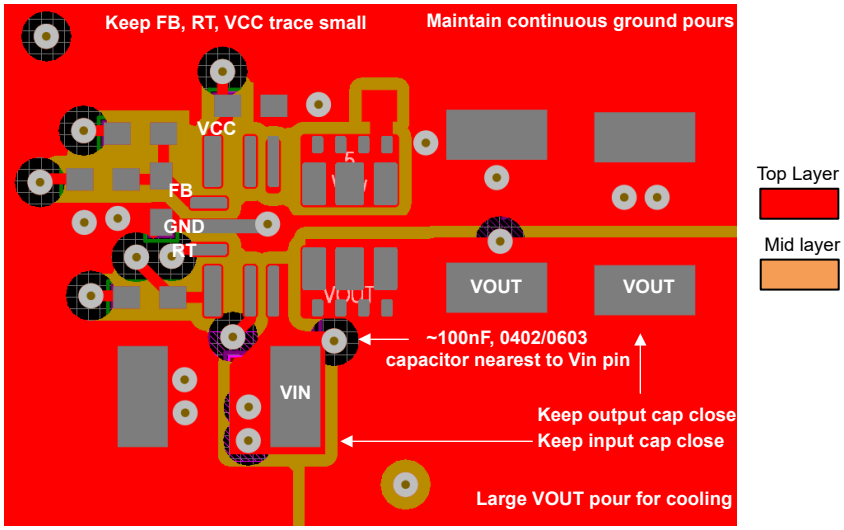


図 8-16. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

図 9-1 shows the device naming nomenclature of the TPSM365R1x. See セクション 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

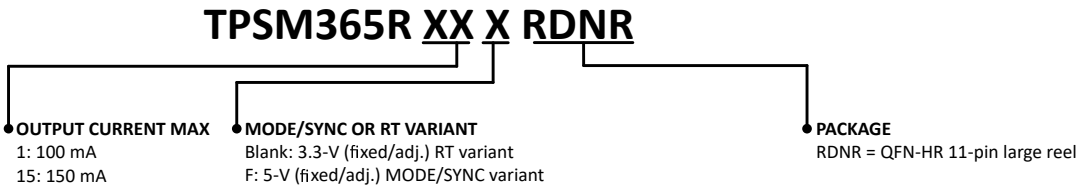


図 9-1. Device Naming Nomenclature

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM365R1x with the WEBENCH® Power Designer.

1. Start by entering the input voltage (VIN), output voltage (VOUT), and output current (IOUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible devices from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability. In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- For TI's WEBENCH Power Designer environment, visit the WEBENCH design center
- Texas Instruments, *Thermal Design by Insight not Hindsight application report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics application report*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602 application report*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package application report*
- Texas Instruments, *PowerPAD™ Made Easy application report*
- Texas Instruments, *Using New Thermal Metrics application report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies application report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines application report*
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x application report*
- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed forward Capacitor application report*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (December 2023)	Page
• 「パッケージ情報」表と「製品情報」表の TPSM365R1 から「プレビュー」のタグを削除	1
• Deleted *Preview information* tag from TPSM365R15FRDNR, TPSM365R1RDNR, and TPSM365R1FRDNR in the *Device Comparison* table	3
• Added 100-mA current limit information	7
• Added MODE/SYNC limits	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM365R15FRDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R15F
TPSM365R15FRDNR.A	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R15F
TPSM365R15FRDNR.B	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM365R15RDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R15
TPSM365R15RDNR.A	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R15
TPSM365R15RDNR.B	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM365R1FRDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R1F
TPSM365R1FRDNR.A	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R1F
TPSM365R1FRDNR.B	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM365R1RDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R1
TPSM365R1RDNR.A	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	365R1
TPSM365R1RDNR.B	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

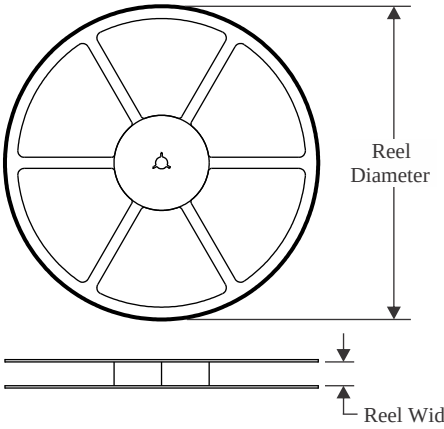
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

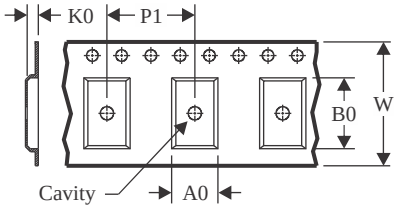
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

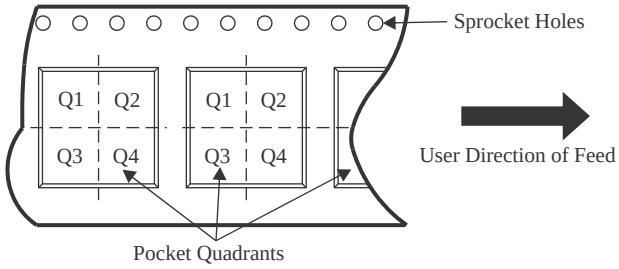


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

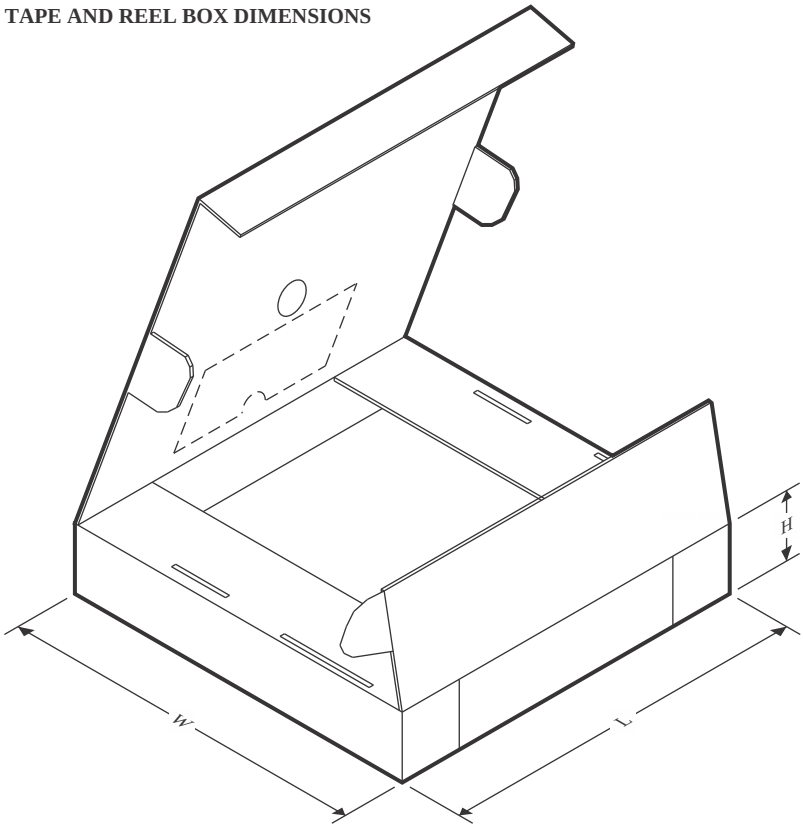
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM365R15FRDNR	QFN-FCMOD	RDN	11	3000	330.0	12.4	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R15RDNR	QFN-FCMOD	RDN	11	3000	330.0	12.4	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R1FRDNR	QFN-FCMOD	RDN	11	3000	330.0	12.4	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R1RDNR	QFN-FCMOD	RDN	11	3000	330.0	12.4	3.8	4.8	2.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM365R15FRDNR	QFN-FCMOD	RDN	11	3000	367.0	367.0	38.0
TPSM365R15RDNR	QFN-FCMOD	RDN	11	3000	367.0	367.0	38.0
TPSM365R1FRDNR	QFN-FCMOD	RDN	11	3000	367.0	367.0	38.0
TPSM365R1RDNR	QFN-FCMOD	RDN	11	3000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

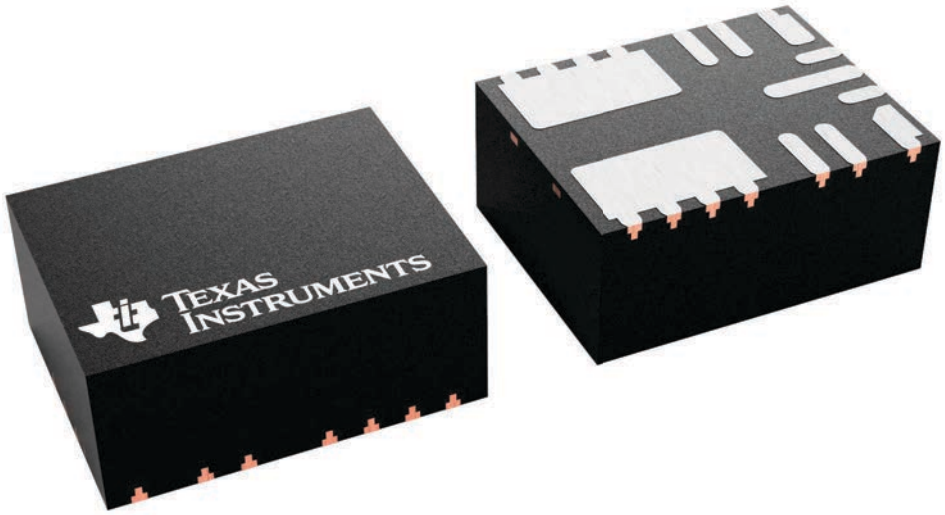
RDN 11

QFN-FCMOD - 2.1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



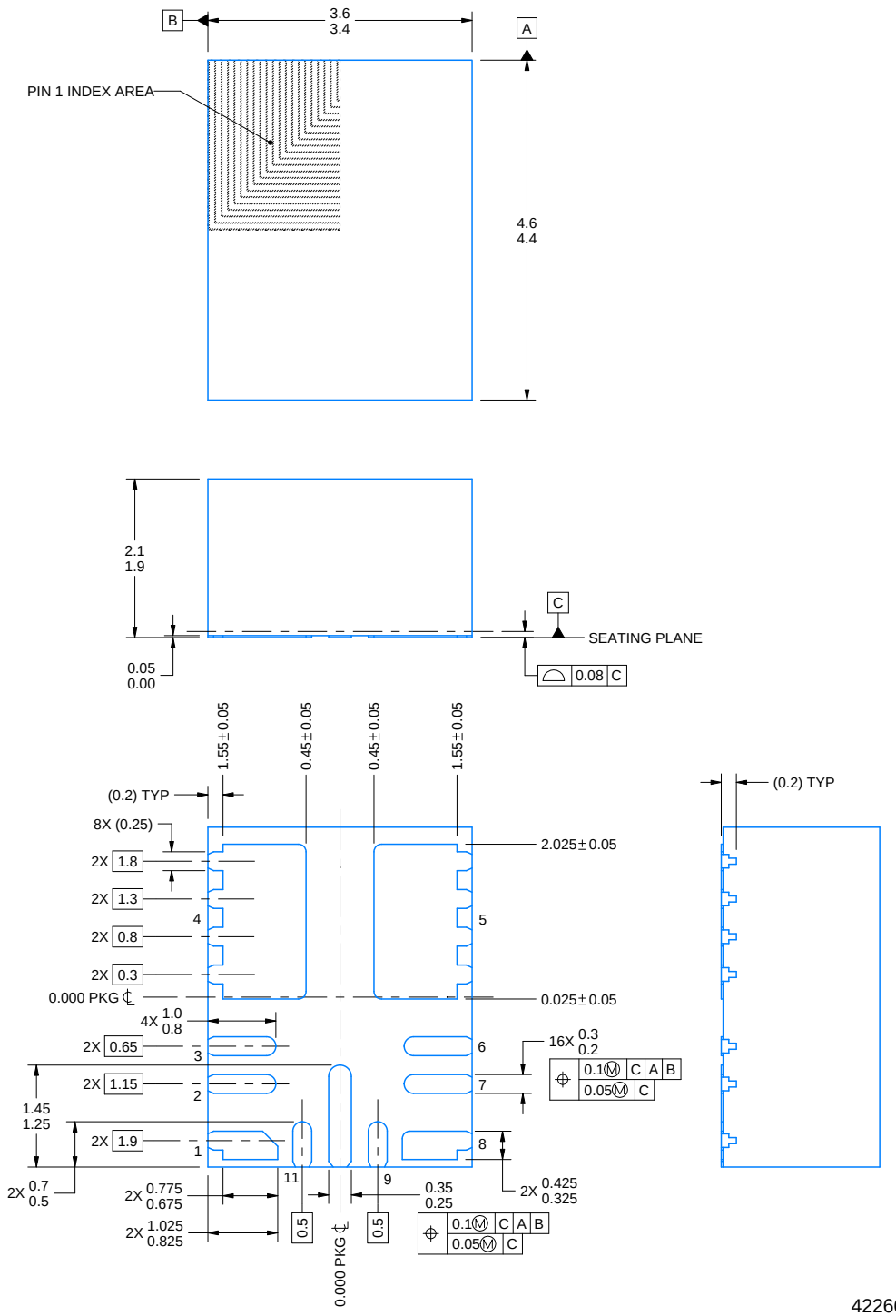
4231226/A

PACKAGE OUTLINE

RDN0011A

QFN-FCMOD - 2.1 mm max height

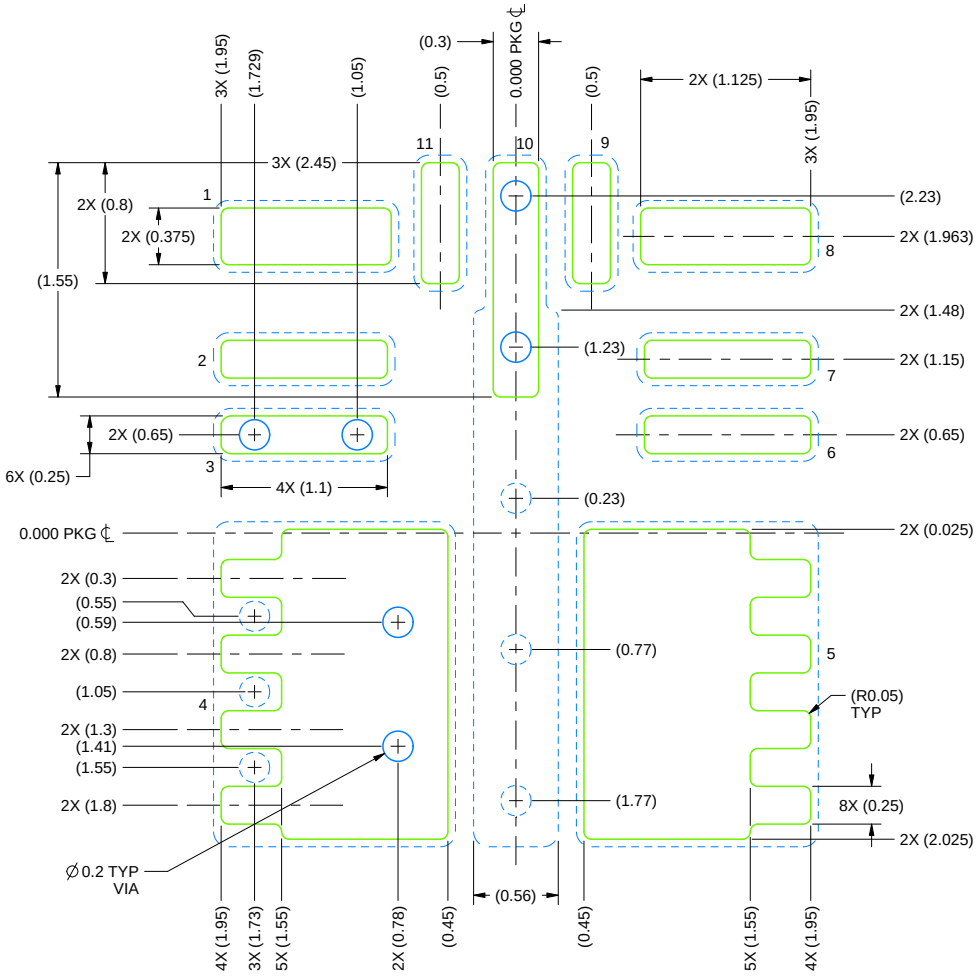
PLASTIC QUAD FLATPACK - NO LEAD



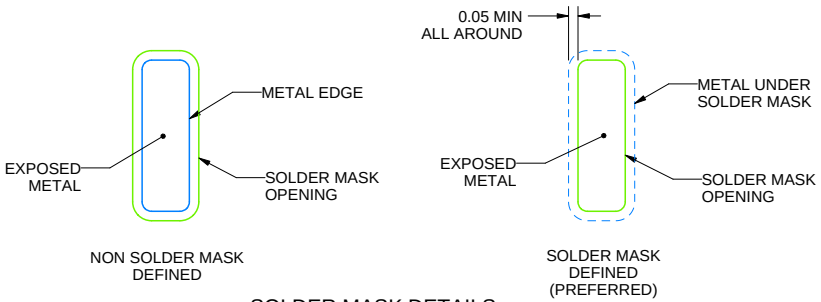
4226623/F 09/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

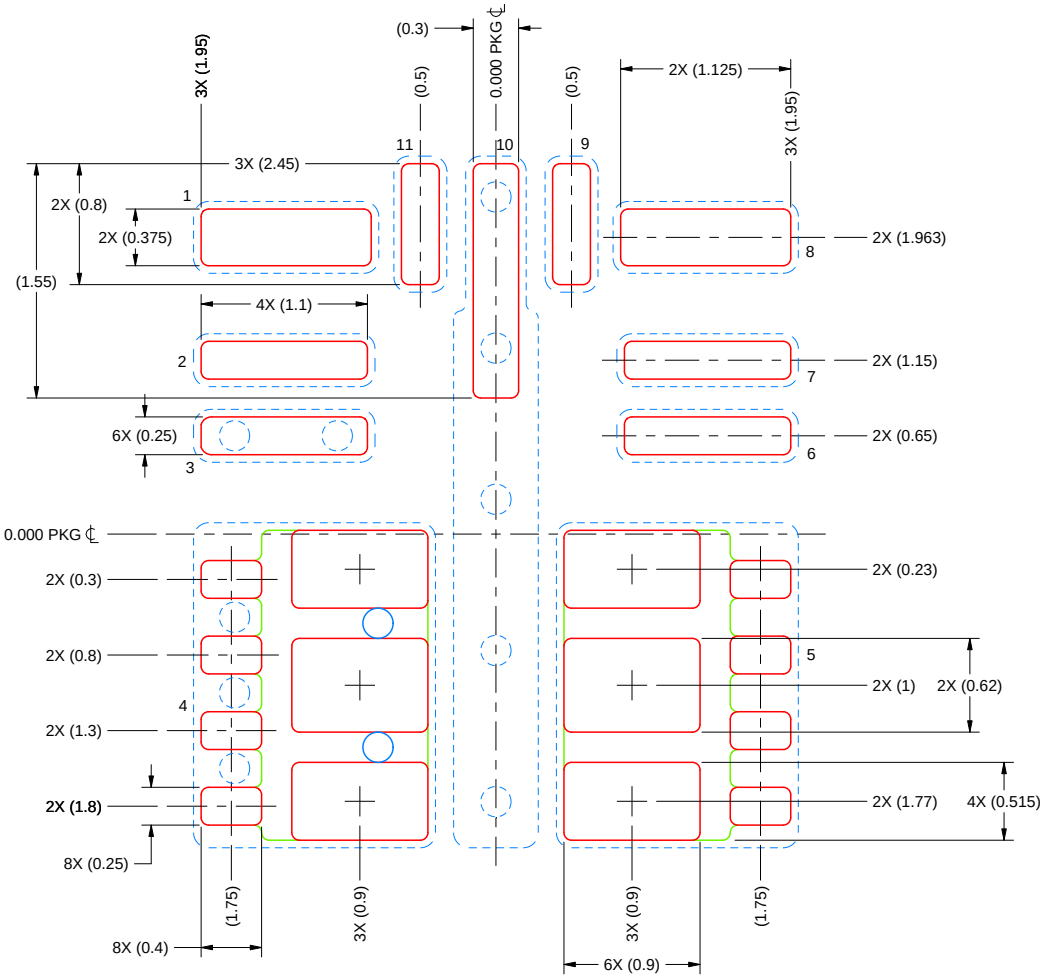
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RDN0011A

QFN-FCMOD - 2.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 4 & 5: 72%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月