TEXAS INSTRUMENTS
TPSM41625
JAJSJQ7A – SEPTEMBER 2020 – REVISED DECEMBER 2020

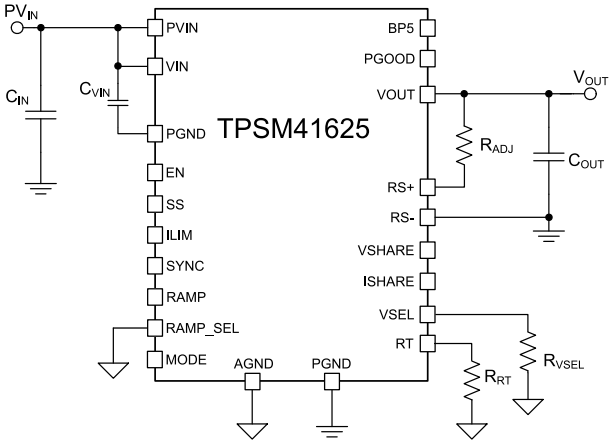
TPSM41625 4V～16V 入力、25A DC/DC パワー・モジュール、電流共有機能付き

1 特長

- インダクタ内蔵の電源ソリューション
- 11mm × 16mm × 4.2mm の QFN パッケージ
  - すべてのピンにパッケージの周囲からアクセス可能
- 入力電圧範囲:4V～16V
- 広い出力電圧範囲:0.6V～7.1V
- 選択可能な内部リファレンス (精度 ±0.5%)
- 最大 2 つのデバイスをスタック可能
  - 並列出力による大電流化
  - 位相インターリーブによるリップルの低減
- 最大 97% の効率
- 調整可能な固定スイッチング周波数 (300kHz～1MHz)
- 外部クロックに同期可能
- 高度な電流モードにより、超高速負荷ステップ応答を実現
- パワー・グッド出力
- EN55011 放射 EMI の規制条件に準拠
- 動作時の周囲温度範囲:-40℃～+105℃
- 動作時の IC 接合部温度範囲:-40℃～+125℃
- 次の製品とピン互換 15A TPSM41615
- WEBENCH® Power Designer により、TPSM41625 を使用するカスタム設計を作成

2 アプリケーション

- 電気通信および無線インフラ
- 産業用自動化試験装置
- エンタープライズ向けスイッチング / ストレージ・アプリケーション
- 高密度の分散電源システム



概略回路図

3 概要

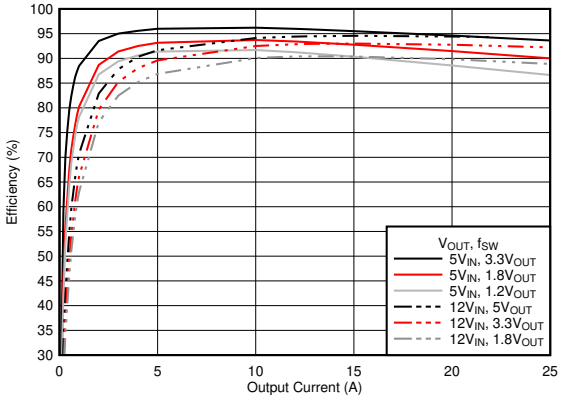
TPSM41625 パワー・モジュールは、DC/DC コンバータをパワー MOSFET、シールド付きインダクタ、およびパッシブ部品とともに小型の QFN パッケージに実装した、使いやすい集積電源です。この電源ソリューションは、特定の設計要件に応じて主要なパラメータを変更する機能を維持しているにもかかわらず、外付け部品をほとんど必要としません。大電流を必要とするアプリケーションでは、2 つの TPSM41625 デバイスを並列に接続できることは有効です。

11mm × 16mm × 4.2mm の 69 ピン QFN パッケージは、最適なパッケージ・レイアウトを行った場合、熱的性能を高める優れた電力散逸能力を達成します。本パッケージのフットプリントには、信号ピン (すべて周囲からアクセス可能) と大きなサーマル・パッド (デバイスの下) が含まれます。TPSM41625 はパワー・グッド信号、クロック同期、プログラマブル UVLO、ソフトスタート・タイミング選択、プリバイアス・スタートアップ、過電流および過熱保護など、数多くの機能を備えた柔軟性の高い製品であるため、多種多様なデバイスやシステムの駆動に適しています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPSM41625	QFN (69)	11mm × 16mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率代表値

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2020) to Revision A (December 2020)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

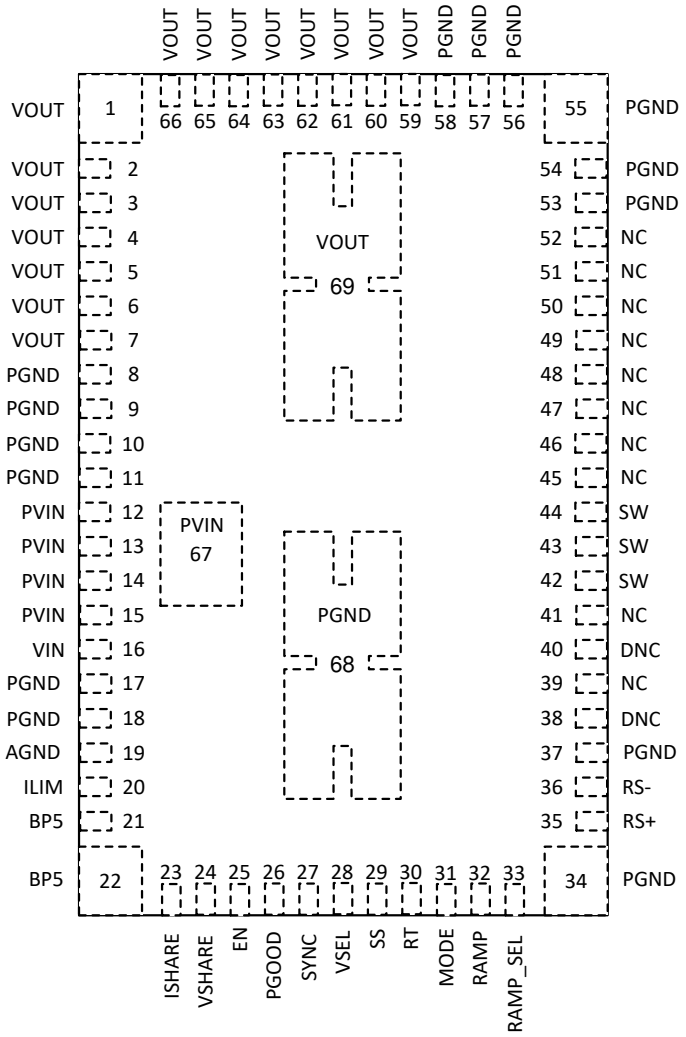


図 5-1. 69-Pin QFN MOV Package (Top View)

表 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
AGND	19	G	Analog ground. Zero voltage reference for internal references and logic. Do not connect this pin to PGND; the connection is made internal to the device.
BP5	21, 22	O	Output of an internal 5-V regulator used for the controller driver stage within the module. This output can be used to connect a pullup resistor to the PGOOD pin. Leave these pins open if not used as a pullup for PGOOD.
DNC	38, 40	–	Do Not Connect. Do not connect these pins to AGND, PGND, another DNC pin, or any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
EN	25	I	Enable pin. This pin turns the converter on when floated or opened. This pin is internally pulled up to the BP5 voltage when left open. The converter can be turned off by either driving it directly with a logic input or an open drain/collector device to connect this pin to AGND. An external voltage divider can be placed between this pin, AGND, and PVIN/VIN to create an external UVLO.
ILIM	20	I	Current limit setting pin. This pin sets the current limit threshold of the converter. Leave this pin open for the full current limit threshold. The current limit threshold can be lowered by connecting an appropriate resistor from this pin to AGND.
ISHARE	23	O	Current sharing pin. This pin is interconnected between modules for multi-phase configurations. Leave this pin open for single-phase configurations.

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表 5-1. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
MODE	31	I	Mode select pin. This pin is used to configure the module for single-phase or multi-phase operation. For single-phase operation, this pin is used to select the API and Body Brake functions. For multi-phase operation, this pin selects the primary/secondary and SYNC configurations.
NC	39, 41, 45-52	–	Not connected. These pins are not connected to any circuitry within the module. It is recommended that these pins be connected to the PGND plane on the application board to enhance shielding and thermal performance.
PGND	8-11, 17, 18, 34, 37, 53-58, 68	G	This is the return path for the power stage of the device. Connect these pins to the input supply return, load return, and bypass capacitors associated with the PVIN and VOUT pins.
PGOOD	26	O	Power Good pin. Open-drain output that asserts low if the remote sense feedback voltage is not within the specified PGOOD thresholds. When using this signal as an output, a pullup resistor is required. If unused, leave this pin open. The BP5 output can be used as the pullup voltage source.
PVIN	12-15, 67	I	Input switching voltage. Supplies voltage to the power switches of the converter. Connect these pins to the input supply. Connect bypass capacitors between these pins and PGND, close to the module.
RAMP	32	I	Internal ramp selection. This pin is used to select an internal ramp amplitude. See 表 7-3 for recommended settings. An internal 78.7-kΩ resistor is connected between RAMP and RAMP_SEL within the module. To select the internal resistor, it is recommended to leave this pin open and to connect the RAMP_SEL pin to AGND.
RAMP_SEL	33	I	Internal default ramp selection. This pin is used to select the internal default ramp selection for the control loop. An internal 78.7-kΩ resistor is connected between RAMP and RAMP_SEL pins. Connect the RAMP_SEL pin to AGND and leave the RAMP pin open to select the internal resistor.
RS+	35	I	Positive input to the internal differential remote sense amplifier. This pin is used for the feedback connection to VOUT. Connect this pin to the output voltage at the load. This connection can be made using a direct connection or an external upper feedback resistor, depending on the magnitude of VOUT and the VSEL selection. A 1-kΩ lower feedback resistor is connected across RS+ and RS– internal to the module. The RS+ connection is not needed for secondary devices in multi-phase configurations, and should be left open.
RS–	36	I	Negative input to the internal differential remote sense amplifier. This pin is used for the feedback connection to VOUT return. Connect this pin to the output voltage return at the load. A 1-kΩ lower feedback resistor is connected across RS+ and RS– internal to the module. The RS- connection is not needed for secondary devices in multi-phase configurations, and should be left open.
RT	30	I	Switching frequency setting pin. This analog pin is used to set the switching frequency of the converter by placing an external resistor from this pin to AGND. This pin also selects the phase interleaving of the module when used in multi-phase configurations.
SS	29	I	Soft-start selection pin. This pin is used to select the soft-start time. Ten possible selections are available by connecting an appropriate resistor from this pin to AGND. The selections range from 0.5 ms to 32 ms.
SW	42-44	O	Switch node. These pins are connected to the internal output inductor and switching MOSFETs. Connect these pins together using a small copper island beneath the device. Keep this copper island to a minimum to prevent issues with noise and EMI.
SYNC	27	I	Frequency synchronization pin. MODE can be used to configure this pin as a sync input or a sync output for external clock and multi-phase primary/secondary configurations.
VIN	16	I	Input bias voltage. Supplies the control circuitry of the power converter. Connect a 1-µF bypass capacitor from this pin to PGND (pins 17 and 18) in close proximity to the module. For split rail applications, connect this pin to an input bias supply. For strapped rail applications, connect this pin to PVIN through a 0 Ω to 10 Ω resistor.
VOUT	1-7, 59-66, 69	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND in close proximity to the module.
VSEL	28	I	Internal reference voltage selection. This pin is used to select the desired internal reference voltage. Ten possible selections are available by connecting an appropriate resistor from this pin to AGND. The selections range from 0.6 V to 1.1 V.
VSHARE	24	O	Voltage sharing pin. This pin is interconnected between modules for multi-phase configurations. Leave this pin open for single-phase configurations.

(1) G = Ground, I = Input, O = Output, – = Not Connected

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input voltage	PVIN		–0.3	17	V
	PVIN to SW	DC	–0.3	25	V
		<10 ns	–5	25	V
	VIN		–0.3	18	V
	VSEL, SS, MODE, RT, SYNC, EN, ISHARE, ILIM		–0.3	7	V
	RS+		–0.3	3.6	V
	RS-		–0.3	0.3	V
	AGND, PGND		–0.3	0.3	V
	SW	DC	–0.3	20	V
		<10 ns	–5.0	20	V
Output voltage	VOUT		–0.3	8	V
	BP5, PGOOD, RAMP		–0.3	7	V
	VSHARE		–0.3	3.6	V
Mechanical shock	Mil-STD-883H, Method 2002.5, 1 msec, 1/2 sine, mounted			500	G
Mechanical vibration	Mil-STD-883H, Method 2007.3, 20 to 2000 Hz			20	G
Operating IC junction temperature, T_J (2)			–40	125	°C
Operating ambient temperature, T_A (2)			–40	105	°C
Storage temperature, T_{stg}			–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	PV_{IN}, V_{IN}	4	16	V
	VSEL, SS, MODE, RT, SYNC, EN, ISHARE, ILIM	–0.1	5.5	V
	RS+	–0.1	1.7	V
	RS-	–0.1	0.1	V
	AGND, PGND	–0.1	0.1	V
Output voltage	V_{OUT}	0.6	7.1	V
	BP5, PGOOD, RAMP	–0.3	5.5	V
	VSHARE	–0.3	3.3	V
Output current	I_{OUT}	0	25	A
Operating IC junction temperature, T_J		–40	125	°C
Operating ambient temperature, T_A		–40	105	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPSM41625 MOV (QFN) 69 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	4.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	9.8	°C/W
T_{SHDN}	Thermal Shutdown Temperature	165	°C
	Thermal Shutdown Hysteresis	30	°C

(1) For more information about thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 90 mm × 90 mm, 6-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

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6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +105°C, PV_{IN}= 12 V, V_{IN} = 12 V, V_{OUT} = 1.8 V, V_{REF} = 1.0 V, F_{SW} = 500 kHz, IOUT = 25 A, (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
PV_{IN}	Input switching voltage		4		16	V
V_{IN}	Input bias voltage		4		16	V
UVLO	PV_{IN} undervoltage lockout	PV_{IN} increasing, I_{OUT} = 0 A		3.2		V
		PV_{IN} decreasing, I_{OUT} = 2.5 A		3.0		V
	V_{IN} undervoltage lockout	V_{IN} increasing, I_{OUT} = 0 A		3.8		V
		V_{IN} decreasing, I_{OUT} = 2.5 A		3.6		V
I_{VIN}	V_{IN} bias current(1)	V_{RS+} = 1.2 V, I_{OUT} = 0 A, EN = OPEN, T_A = 25°C		4.3		mA
$I_{VIN-STBY}$	V_{IN} standby current	I_{OUT} = 0 A, EN = 0 V, T_A = 25°C		4.3		mA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage adjust	RS+ connected directly to V_{OUT}	0.6		1.1	V
		RS+ connected to V_{OUT} feedback divider			7.1(1) (2)	V
	V_{OUT} accuracy	0.6V ≤ V_{REF} ≤ 1.1V, V_{RS+} = V_{OUT}, I_{OUT} = 0A, -40°C ≤ T_J = T_A ≤ 125°C(1)	-1.0		1.0	%
	Line regulation	Over PV_{IN} range, PV_{IN} = V_{IN}, I_{OUT} = 0 A, T_A = 25°C		0.01		%
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.03		%
OUTPUT CURRENT						
I_{OUT}	Output current	Natural convection, T_A = 25°C	0		25(2)	A
	Overcurrent threshold			32		A
I_{SHARE}	Current sharing for multi-phase operation(1)	I_{OUT} ≤ 20 A/phase		±3		A
		I_{OUT} ≥ 20 A/phase		±15%		
BP5 REGULATOR						
V_{BP5}	BP5 regulator output voltage		4.5	5	5.5	V
$V_{BP5-DROPOUT}$	BP5 regulator dropout voltage(1)	V_{IN} = 4.5 V, f_{SW} = 750 kHz, T_A = 25°C			365	mV
PERFORMANCE						
η	Efficiency	I_{OUT} = 12.5 A		91		%
RS+						
$R_{RS+-RS-}$	Lower feedback resistor from RS+ to RS-		0.995	1	1.005	kΩ
ENABLE						
V_{EN-H}	EN rising threshold	I_{OUT} = 0 A	1.45	1.6	1.75	V
V_{EN-L}	EN falling threshold	I_{OUT} = 2.5 A		1.3		V
I_{EN_LKG}	EN input leakage current	V_{IN} = 4.5 V, I_{OUT} = 0 A	–1	0	1	µA
SOFT START						
t_{SS}	Soft-start time(1)	SS = OPEN		4		ms
$t_{SS-Range}$	Soft-start range(1)	Programmable using SS pin	0.5		32	ms

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Limits apply over T_A = –40°C to +105°C, PV_{IN}= 12 V, V_{IN} = 12 V, V_{OUT} = 1.8 V, V_{REF} = 1.0 V, F_{SW} = 500 kHz, IOUT = 25 A, (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD						
V_{PGOOD}	PGOOD thresholds(1)	V_{RS+} rising (fault)		112%		
		V_{RS+} falling (good)		105%		
		V_{RS+} rising (good)		95%		
		V_{RS+} falling (fault)		88%		
$V_{PGOOD-LOW}$	PGOOD low voltage with no supply voltage	PV_{IN} = V_{IN} = 0 V, I_{PGOOD} = 80 µA			0.8	V
$I_{PGOOD-LKG}$	PGOOD leakage current	V_{IN} = 4.5 V, V_{PGOOD} = 5 V, I_{OUT} = 0 A			15	µA
OVP / UVP						
V_{OVP}	Overvoltage protection threshold(1)	V_{RS+} rising		117%		
V_{UVP}	Under-voltage protection threshold(1)	V_{RS+} falling		83%		
FREQUENCY and SYNC						
f_{SW}	Switching frequency	VSEL = OPEN, RT = 44.2 kΩ, I_{OUT} = 2.5 A	450	500	550	kHz
	Switching frequency range(1)	I_{OUT} = 2.5 A	300		1000	kHz
ton_min	Minimum on-time of SW(1)			30		ns
toff_min	Minimum off-time of SW(1)			340		ns
V_{CLK-H}	Logic-high for SYNC(1)		2			V
V_{CLK-L}	Logic-low for SYNC(1)				0.8	V
$T_{CLK-MIN}$	Minimum pulse width for SYNC(1)	SYNC F_{SW} = 500 kHz	100			ns

(1) Ensured by design, not production tested.
(2) To determine IOUT range for a given set of conditions, see the Safe Operating Area graphs in "Typical Characteristics" section of the datasheet for more information.

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6.6 Typical Characteristics (PV_{IN} = 12 V)

T_A = 25°C, unless otherwise noted.

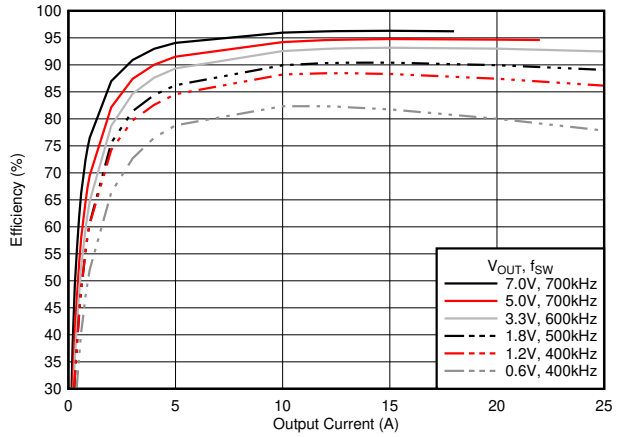


図 6-1. Efficiency vs Output Current

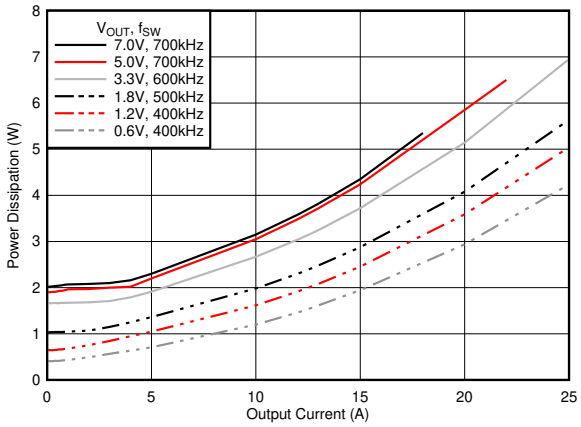
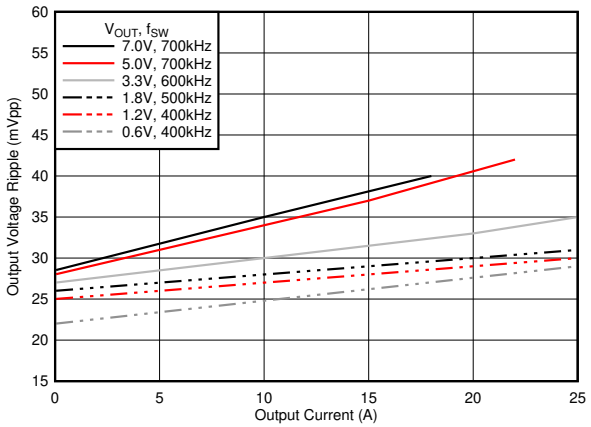
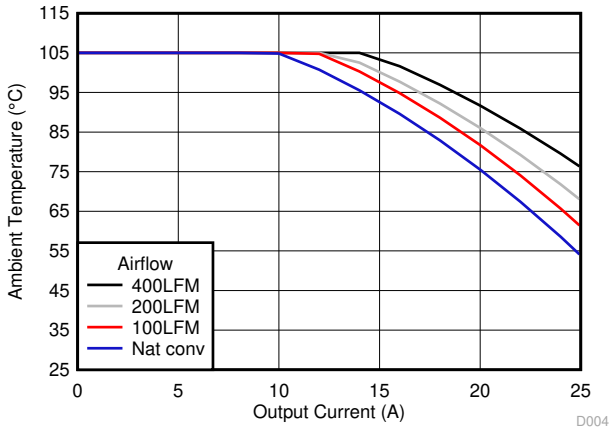


図 6-2. Power Dissipation vs Output Current



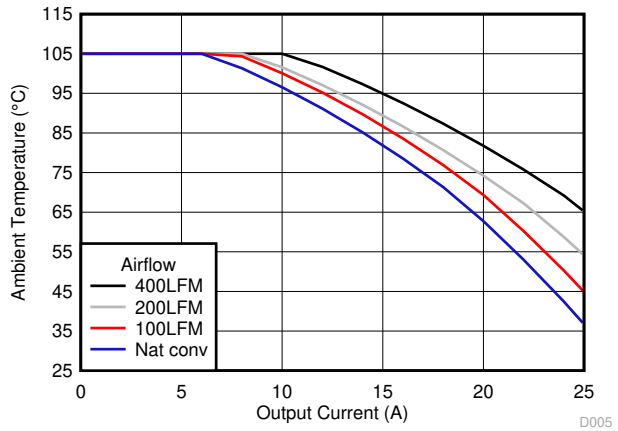
C_{OUT} = C_{OUT}min

図 6-3. Output Voltage Ripple



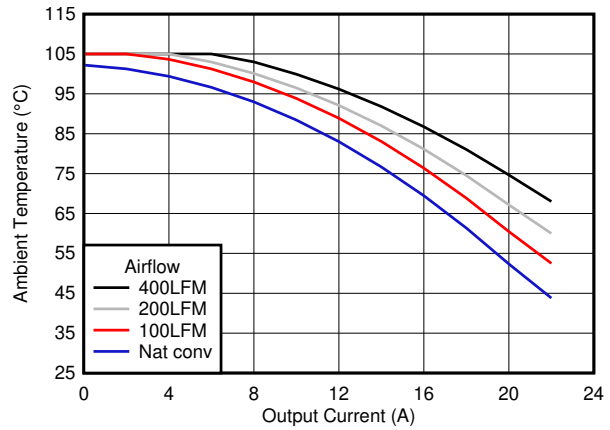
V_{OUT} = 1.8 V f_{SW} = 500 kHz

図 6-4. Safe Operating Area



V_{OUT} = 3.3 V f_{SW} = 600 kHz

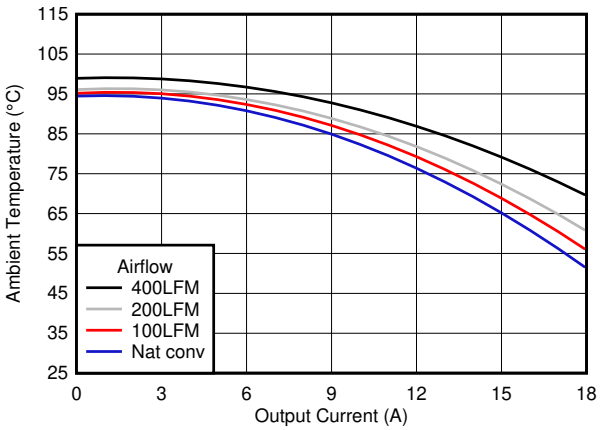
図 6-5. Safe Operating Area



V_{OUT} = 5 V f_{SW} = 700 kHz

図 6-6. Safe Operating Area

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V_{OUT} = 7.1 V f_{SW} = 700 kHz

図 6-7. Safe Operating Area

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6.7 Typical Characteristics (PV_{IN} = 5 V)

T_A = 25°C, unless otherwise noted.

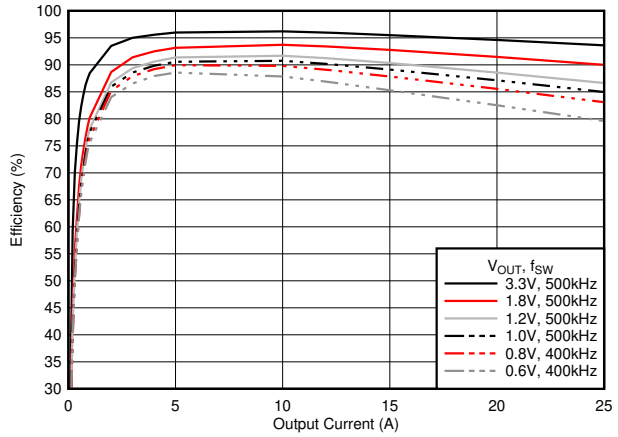


図 6-8. Efficiency vs Output Current

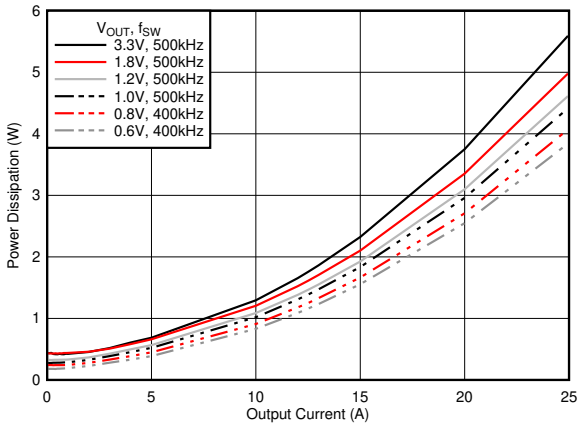
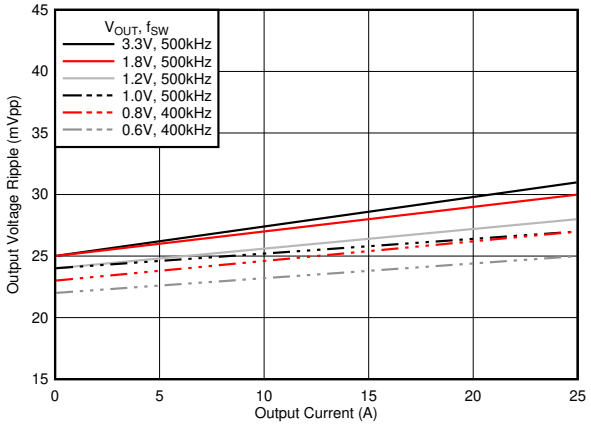
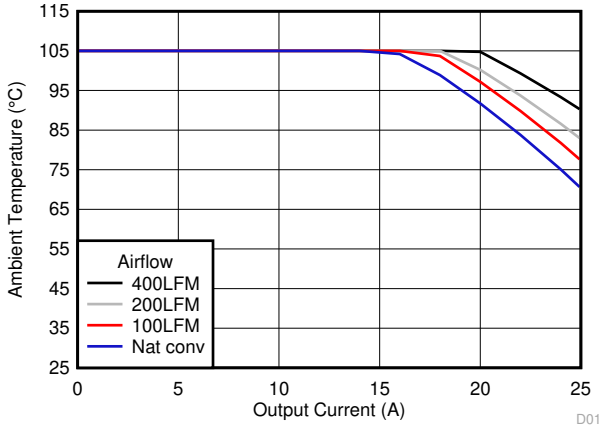


図 6-9. Power Dissipation vs Output Current



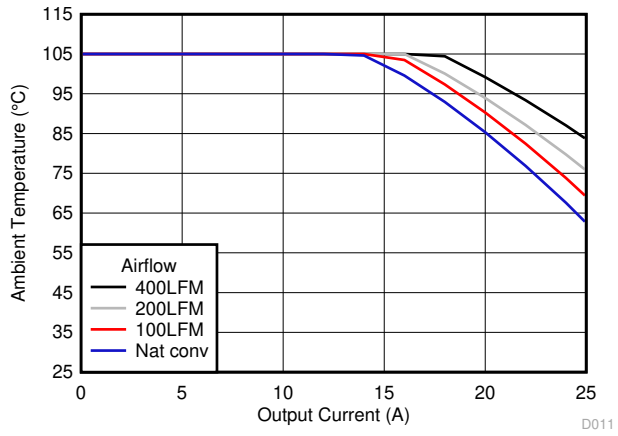
C_{OUT} = C_{OUT}min

図 6-10. Output Voltage Ripple



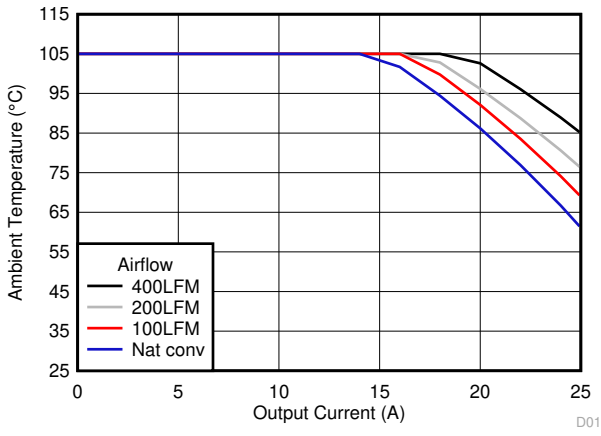
V_{OUT} = 1 V f_{SW} = 500 kHz

図 6-11. Safe Operating Area



V_{OUT} = 1.8 V f_{SW} = 500 kHz

図 6-12. Safe Operating Area



V_{OUT} = 2.5 V f_{SW} = 500 kHz

図 6-13. Safe Operating Area

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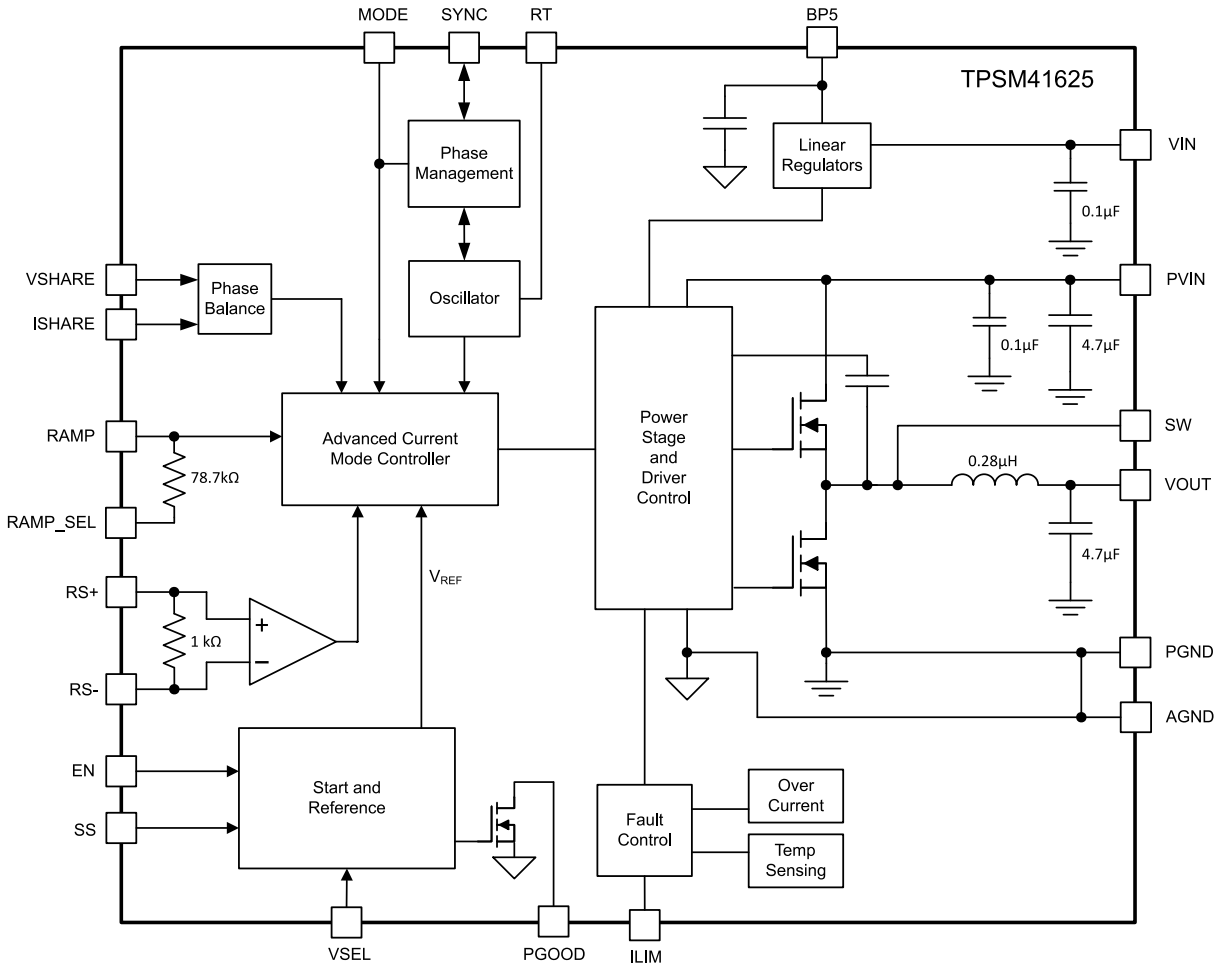
7 Detailed Description

7.1 Overview

The TPSM41625 is a full-featured, 4-V to 16-V input, 25-A, synchronous step-down converter with PWM, MOSFETs, inductor, and control circuitry integrated into a QFN package. The device integration enables small designs, while still leaving the ability to adjust key parameters to meet specific design requirements. The TPSM41625 provides an output voltage range of 0.6 V to 7.1 V, with a selectable internal reference form 0.6 V to 1.1 V, for greater accuracy. An external resistor is used to adjust the output voltage to the desired output. The switching frequency is also adjustable by using an external resistor or a synchronization clock to accommodate various input and output voltage conditions and to optimize efficiency. Applications requiring increased current can benefit from the stackability (parallel outputs and phase-interleaving) of the TPSM41625 device.

The TPSM41625 has been designed for safe start-up into pre-biased loads. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the internal pullup current of the EN pin allows the device to operate with the EN pin floating. The EN pin can also be pulled low to put the device in standby mode to reduce input quiescent current. The device provides a power-good (PGOOD) signal to indicate when the output voltage is within regulation. Thermal shutdown and current limit features protect the device during an overload condition. A 69-pin QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Setting the Output Voltage

The output voltage adjustment range of the TPSM41625 is 0.6 V to 7.1 V. Setting the output voltage requires first setting the internal reference voltage (V_{REF}). The internal reference voltage can be set from 0.6 V to 1.1 V using a resistor (R_{VSEL}) connected from VSEL (pin 28) to AGND (pin 19). 表 7-1 lists reference voltage selections and their corresponding setting resistors. If the required output voltage is the same as the reference voltage, connect the RS+ pin (pin 35) directly to VOUT to set the output voltage as shown in 図 7-1. Output voltages greater than the reference voltage require an external voltage setting resistor (R_{ADJ}) between the RS+ pin and VOUT to set the output voltage as shown in 図 7-2. The value for R_{ADJ} can be calculated using 式 1 or simply selected from the recommended values given in 表 7-2. Additionally, 表 7-3 includes the recommended switching frequency (F_{SW}), the recommended Ramp resistor (R_{RAMP}), and the minimum output capacitance for several output voltage ranges.

$$R_{ADJ} = \left(\frac{V_{OUT}}{V_{ref}} - 1 \right) \text{ (k}\Omega\text{)} \quad (1)$$

When setting the output voltage, selecting the highest reference voltage will result in the most accurate output voltage set point. The output voltage will be regulated at the connection point of RS+ or R_{ADJ} to VOUT. Making the connection near the load improves regulation at the load.

表 7-1. Setting the Reference Voltage

V_{REF} (V)	0.6	0.7	0.75	0.8	0.85	0.9	0.95	1.0	1.05	1.1
R_{VSEL} Value (kΩ)(1)	0	8.66	15.4	23.7	34.8	51.1	78.7	open	121	187

(1) Resistors with ≤ 1% tolerance are recommended.

表 7-2. Setting the Output Voltage

V_{OUT} (V)	0.6 - 1.1	1.2	1.5	1.8	2.5	3.3	5.0	6.0	7.0
V_{REF} (V) (1)	0.6 - 1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
R_{ADJ} Value (Ω)(1)	short	90.9	365	634	1270	2000	3570	4420	5360

(1) Selecting the highest reference voltage will result in the most accurate output voltage set point.

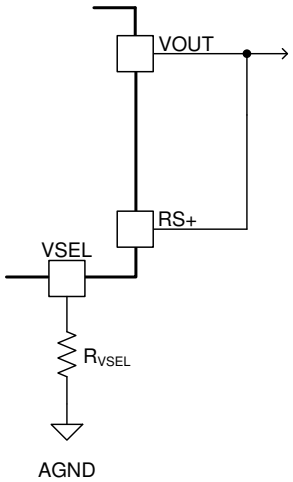


図 7-1. Setting the Output Voltage ($V_{OUT} = V_{REF}$)

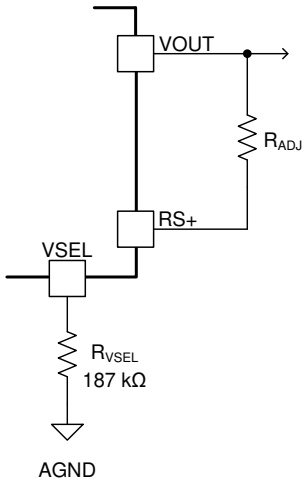


図 7-2. Setting the Output Voltage ($V_{OUT} > V_{REF}$)

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表 7-3. Recommended F_{SW}, RAMP, and Required C_{OUT}

PV_{IN} = 5 V						
V_{OUT} RANGE (V)		RECOMMENDED F_{SW} (kHz)(1)	ALLOWABLE F_{SW} RANGE (KHZ)	R_{RAMP} (kΩ)	MINIMUM REQUIRED C_{OUT} (µF)(4)	
MIN	MAX				MINIMUM CERAMIC(3)	ADDITIONAL REQUIRED CAPACITANCE(5)
0.6	< 0.8	**400**	300 - < 450	78.7	294(2)	610
		500	450 - < 550	187		490
		600	550 - < 700	187		300
		700	700 - 1000	78.7		280
0.8	< 1.0	**400**	300 - < 450	78.7	289(2)	600
		500	450 - < 850	78.7		420
		900	850 - 1000	78.7		240
1.0	< 1.2	**500**	400 - 1000	187	284(2)	190
1.2	< 1.5	**500**	400 - 1000	187	277(2)	100
1.5	< 1.8	**500**	400 - 1000	187	266(2)	90
1.8	< 2.5	**500**	400 - 1000	187	254(2)	85
2.5	3.3	**500**	400 - 1000	78.7	224(2)	65
PV_{IN} = 12 V						
V_{OUT} RANGE (V)		RECOMMENDED F_{SW} (kHz) (1)	ALLOWABLE F_{SW} RANGE (kHz)	R_{RAMP} (kΩ)	MINIMUM REQUIRED C_{OUT} (µF) (4)	
MIN	MAX				MINIMUM CERAMIC (3)	ADDITIONAL REQUIRED CAPACITANCE (5)
0.6	< 1.0	**400**	350 - < 450	78.7	294(2)	760
		500	450 - < 550	78.7		430
		600	550 - 750	78.7		250
1.0	< 1.2	**400**	350 - < 500	78.7	284(2)	760
		550	500 - < 600	78.7		430
		600	600 - 1000	78.7		250
1.2	< 1.8	**400**	350 - < 500	78.7	277(2)	760
		500	500 - < 600	121		185
		600	600 - 1000	121		100
1.8	< 2.5	**400**	350 - < 500	78.7	254(2)	600
		500	500 - < 600	187		430
		600	600 - < 850	187		250
		700	850 - 1000	78.7		90
2.5	< 3.3	**500**	450 - < 650	78.7	224(2)	450
		700	650 - < 950	187		80
		1000	950 - 1000	121		80
3.3	< 5.0	**600**	550 - 1000	187	191(2)	65
5.0	7.1	**700**	600 - 1000	187	134(2)	0

(1) The recommended F_{SW} is shown in **bold** text. Increasing the frequency can reduce the required output capacitance as well as reduce ripple, however it may also reduce efficiency.
(2) This value of minimum ceramic is the effective amount of 6x 47 µF after taking into account DC bias and temperature derating.
(3) The minimum required ceramic output capacitance must account for DC bias and temperature derating.
(4) The Minimum Required output capacitance ensures start-up and stability. Additional output capacitance can be needed to meet transient response requirements.
(5) The Additional Required Capacitance can be either ceramic or low-ESR polymer type. The total required output capacitance must include at least the amount of ceramic type listed in the *Minimum Ceramic* column.

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7.3.2 Output Voltage Current Rating

The rated output current of the TPSM41625 depends on the output voltage required for an application. The output current derates at output voltages above 3.3 V. The area under the curve in 図 7-3 shows the operating range of the TPSM41625.

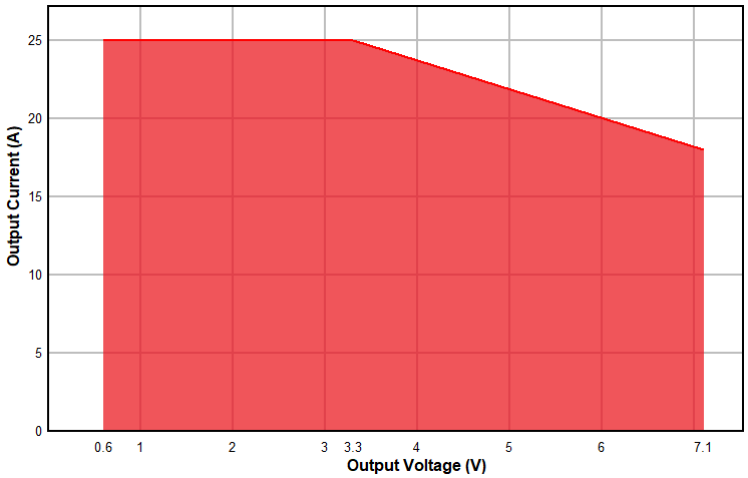


図 7-3. Output Voltage versus Output Current

7.3.3 RS+/RS- Remote Sense Function

RS+ and RS- pins are the remote sensing inputs to the internal differential remote sense amplifier. A 1-kΩ lower feedback resistor is connected across RS+ and RS– internal to the module. The RS+ pin is used for the feedback connection to VOUT. Connect this pin to the output voltage at the load. This connection can be made using a direct connection or an external upper feedback resistor, depending on the magnitude of VOUT and the VSEL selection. The RS- pin is used for the feedback connection to VOUT return. Connect this pin to the output voltage return at the load. The RS- connection is not needed for secondary devices in multi-phase configurations, and should be left open.

7.3.4 Ramp Select (RAMP and RAMP_SEL)

The RAMP and RAMP_SEL pins set the ramp amplitude for the internal control loop. Internal to the device, a 78.7-kΩ resistor is connected between RAMP and RAMP_SEL. Applications requiring 78.7-kΩ ramp setting should connect the RAMP_SEL pin to AGND and leave the RAMP pin open. Applications requiring a larger ramp setting resistor should connect it between the RAMP pin to AGND and leave the RAMP_SEL pin open. The recommended ramp setting resistor can be found in 表 7-3.

7.3.5 Switching Frequency (RT)

The switching frequency range of the TPSM41625 is 300 kHz to 1 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin (pin 30) and AGND. Select R_{RT} from 表 7-4 based on input voltage and desired switching frequency.

The switching frequency must be selected based on the input voltage and output voltage of the application. See 表 7-3 for the allowable switching frequency range for each output voltage.

表 7-4. R_{RT} Frequency Setting Resistor (kΩ)

INPUT VOLTAGE	SWITCHING FREQUENCY														
	300 kHz	350 kHz	400 kHz	450 kHz	500 kHz	550 kHz	600 kHz	650 kHz	700 kHz	750 kHz	800 kHz	850 kHz	900 kHz	950 kHz	1 MHz
5 V	69.8	59.0	52.3	45.3	40.2	36.5	33.2	30.1	28.0	26.1	23.7	22.1	21.0	19.6	18.2
8 V	73.2	61.9	53.6	47.5	42.2	38.3	34.8	32.4	29.4	27.4	25.5	23.7	22.1	21.0	19.6
10 V - 16 V	75.0	63.4	54.9	48.7	43.2	39.2	35.7	33.2	30.1	28.0	26.1	24.3	23.2	21.5	20.5

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7.3.6 Synchronization (SYNC)

The TPSM41625 device can be synchronized to an external clock. When synchronizing, the external clock signal must be applied to the SYNC pin before the device reaches its VIN UVLO threshold. In a stand-alone configuration, the external clock frequency must be within ±20% of the frequency set by the R_{RT} resistor.

In stackable configuration: (see *セクション 7.3.7.1.1* for information on configuring the SYNC pins.)

1. When there is no external system clock applied, the SYNC pin of the primary device should be configured as Sync-Out and the SYNC pin of the secondary device should be configured as Sync-In. Connecting the SYNC pins of the primary and any secondary devices will synchronize all devices to the frequency of the primary.
2. When an external system clock is applied, the SYNC pin of the primary and secondary devices should be configured as Sync-In and both devices will synchronize to the external system clock.

7.3.6.1 Loss of Synchronization

This device does not support the dynamic application or removal of an external SYNC signal. If the external SYNC signal is removed, the device treats this as a clock fault and stops power conversion.

7.3.7 Stand-alone/Stackable Operation

The TPSM41625 can be operated as a single stand-alone device or two devices can be combined to operate together in a stackable configuration for increased current. These operation modes are selected using a resistor connected from MODE pin to AGND. In stand-alone mode, the resistor value connected to the MODE pin also selects whether the transient response feature is ON or OFF (see 表 7-8). In stackable mode, the transient response feature is not available. In stackable mode, the MODE resistor sets the device as primary or secondary, as well as SYNC pin function (sync in or sync out) of the primary device (see 表 7-5).

表 7-5. MODE Pin Selections

OPERATION MODE	TRANSIENT FEATURE	SYNC MODE	MODE RESISTOR VALUE (kΩ)
Stand-alone	ON	Sync in	78.7
			187
	OFF		open
Stackable	OFF	Primary sync out	23.7
		Primary sync in	34.8
		Secondary sync in	51.1

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7.3.7.1 Stackable Synchronization

7.3.7.1.1 Sync Configuration

In stackable mode, a resistor between the MODE pin and AGND sets the device as primary or secondary, as well as SYNC pin function (sync in or sync out) of the primary device. See 表 7-6 for Mode resistor values.

表 7-6. MODE Setting for SYNC Function

SYNC FUNCTION	MODE RESISTOR VALUE (kΩ)	NOTE
Primary sync out	23.7	• Sync pin to send out clock • RT pin to set frequency
Primary sync in	34.8	• Sync pin to receive clock • RT pin to set sync point
Secondary sync in	51.1	• Sync pin to receive clock • RT pin to set sync point

7.3.7.1.2 Clock Sync Point Selection

The TPSM41625 device implements a unique clock synchronization scheme for phase interleaving between devices. This is only used when stacking multiple devices. The device will receive a clock signal through the SYNC pin and generate sync points to achieve phase interleaving. Sync point options can be selected with a resistor from the RT pin to AGND. 図 7-4 shows the clock signals for a primary and a secondary device with a 180° phase shift. See 表 7-7 for clock sync options and the corresponding RT resistor value.

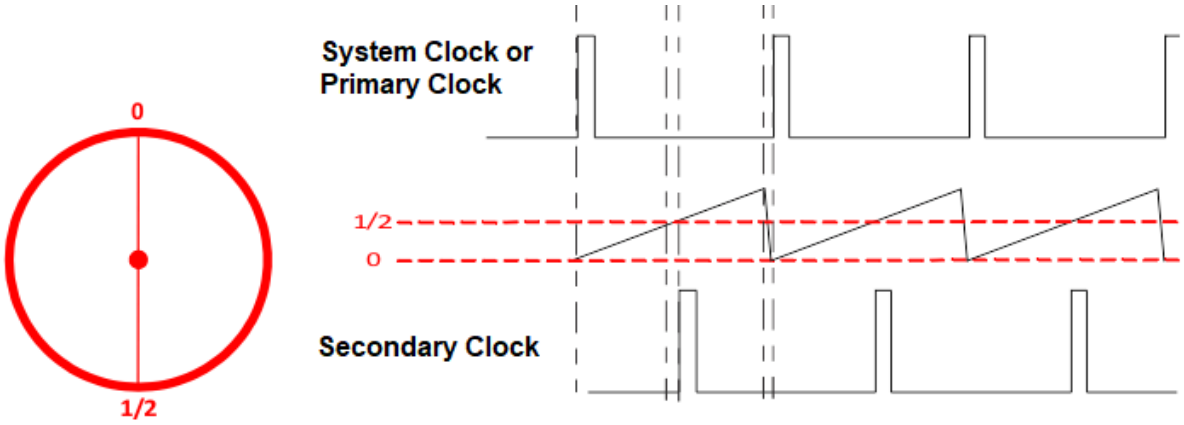


図 7-4. 2-Phase Stackable with 180° Clock Phase Shift

表 7-7. Sync Point Selection

CLOCK SYNC OPTIONS	RT RESISTOR VALUE (kΩ)
0 (0° Interleaving)	SHORT
1/2 (180° Interleaving)	OPEN

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7.3.7.1.3 Configuration 1: Dual Phase, Primary Sync-Out Clock to Secondary

- Direct SYNC, VSHARE, and ISHARE connections between primary and secondary.
- Switching frequency is set by RT pin of primary, and pass to secondary through SYNC pin. SYNC pin of primary will be configured as sync out by its MODE pin.
- Secondary receives clock from SYNC pin. Its RT pin determines the sync point for clock phase shift.

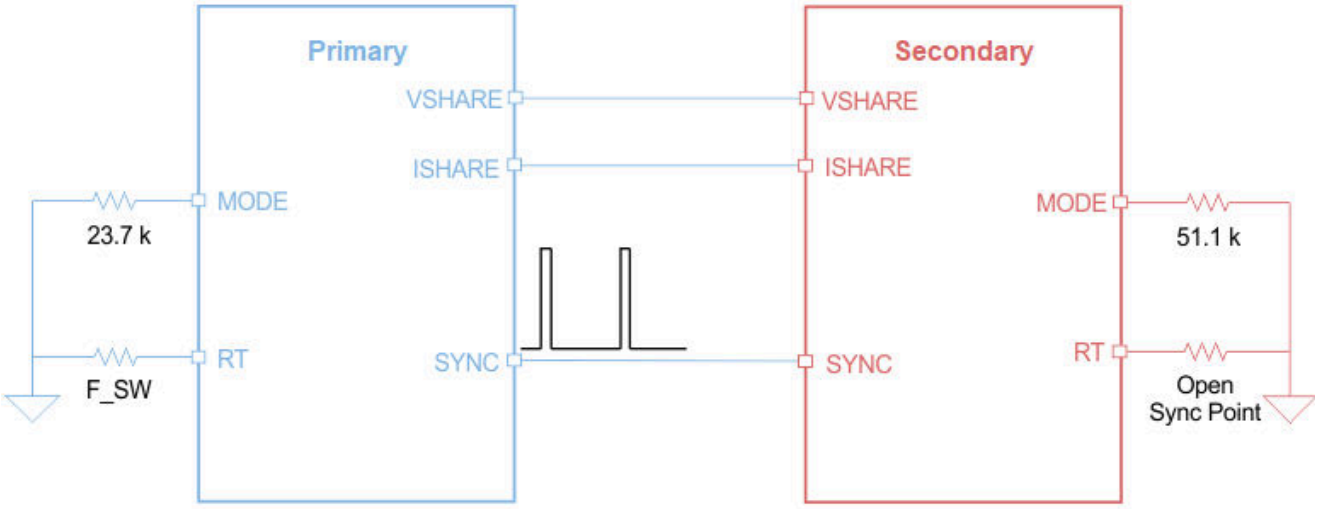


図 7-5. 2-Phase Stackable, 180° Phase Shift: Primary Sync-Out Clock to Secondary

7.3.7.1.4 Configuration 2: Dual Phase, Primary and Secondary Sync to External System Clock

- Direct connection between external clock and SYNC pin of primary and secondary.
- Direct VSHARE and ISHARE connections between primary and secondary.
- SYNC pin of primary is configured as sync in by its MODE pin.
- Primary and secondary receive external system clock from SYNC pin. Their RT pin determine the sync point for clock phase shift.

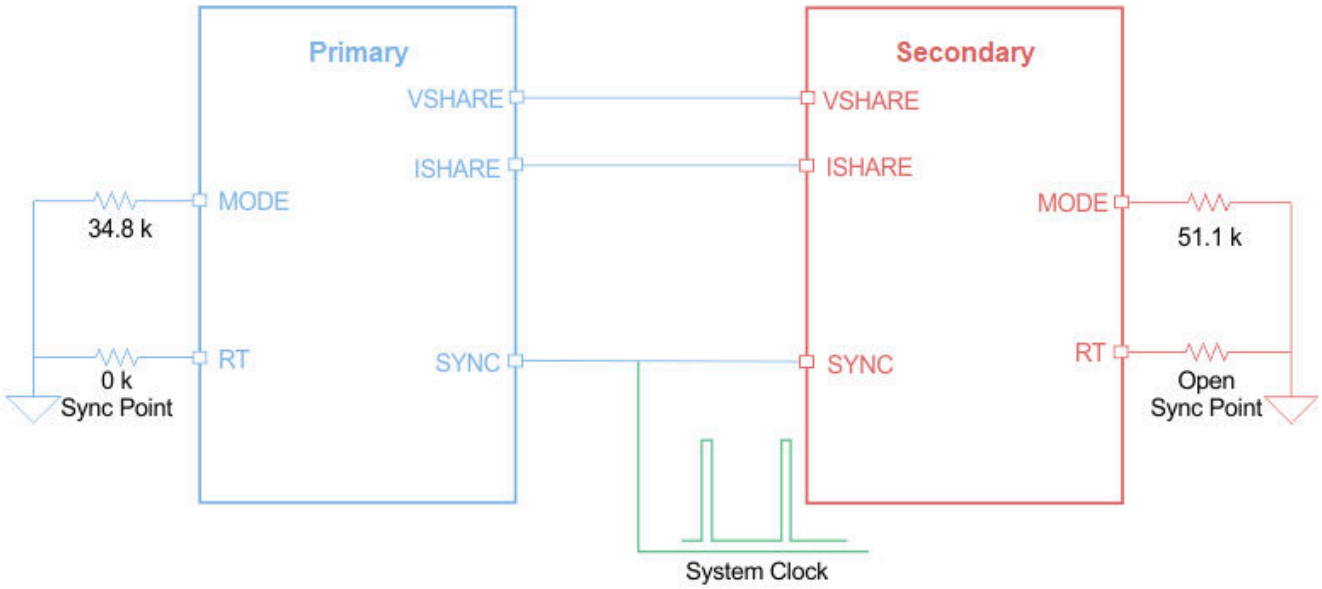


図 7-6. 2-Phase Stackable, 180° Phase Shift: Primary and Secondary Sync to External System Clock

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7.3.8 Improved Transient Performance versus Fixed Frequency (Stand-alone Operation Only)

The TPSM41625 is a fixed frequency converter. The major limitation for any fixed frequency converter is that during transient load step up, the output voltage drops until the next clock cycle of the converter before it can respond to the load change. The TPSM41625 implements a special circuitry to improve transient performance. During a load step up, the converter can issue an additional PWM pulse before the next available clock cycle to stop output voltage from further dropping, thus reducing the undershoot voltage. The additional pulse during a transient means that the device is not fixed frequency during the transient.

During load step-down, the TPSM41625 implements a body-brake function that turns off both high-side and low-side FET, and allows power to dissipate through the low-side body diode, reducing overshoot. This approach is very effective while having some impact on efficiency during transient.

In stand-alone mode, choose whether the transient response feature is enabled by placing either a 78.7-kΩ or 187-kΩ resistor between the MODE pin and AGND. A 78.7-kΩ MODE resistor is recommended when the output voltage is 0.6 V to 1.8 V or in applications that are more susceptible to noise. Leave the MODE pin open to operate in fixed frequency during a load step, (see 表 7-8).

表 7-8. Stand-Alone Operation Feature Selections

STAND-ALONE OPERATION	MODE RESISTOR VALUE (kΩ)
Transient Feature	78.7
	187
Fixed Frequency	open

7.3.9 Output On/Off Enable (EN)

The EN pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low operating current state. The EN pin has an internal pullup to BP5, allowing the user to float the EN pin for enabling the device.

If an application requires controlling the EN pin, either drive it directly with a logic input or use an open drain/collector device to interface with the pin. Applying a low voltage to the enable control (EN) pin disables the output of the supply. When the EN pin voltage exceeds the threshold voltage, the supply executes a soft-start power-up sequence.

7.3.10 Power Good (PGOOD)

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. Once the output voltage is between 92% and 108% of the set-point voltage, the PGOOD pin pulldown is released and the pin floats. A pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source of 5.5 V or less is recommended. The PGOOD pin is pulled low when the output voltage is lower than 88% or greater than 112% of the set-point voltage.

7.3.11 Soft-Start Operation

For the TPSM41625 device, the soft-start time controls the inrush current required to charge the output capacitors during start-up. When the device is enabled, the output voltage ramps from 0 V to the set-point voltage in the time selected by the SS pin. The device offers 10 selectable soft start options ranging from 0.5 ms to 32 ms. See 表 7-9 for details.

表 7-9. SS Pin Configuration

SS TIME	0.5 ms	1 ms	2 ms	4 ms	5 ms	8 ms	12 ms	16 ms	24 ms	32 ms
RESISTOR VALUE (kΩ)	0	8.66	15.4	OPEN	23.7	34.8	51.1	78.7	121	187

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7.3.12 Input Capacitor Selection

The TPSM41625 requires a minimum input capacitance of 88 µF of ceramic type. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. An additional 100 µF of non-ceramic, bulk capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. 表 7-10 includes a preferred list of capacitors by vendor.

表 7-10. Recommended Input Capacitors

VENDOR(1)	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF) (3)	ESR (mΩ) (2)
TDK	X7R	C3225X7R1E226M250AB	25	22	2
Murata	X7R	GRM32ER71E226KE15L	25	22	2
Panasonic	ZA	EEHZA1H101P	50	100	28

(1) **Capacitor Supplier Verification , RoHS, Lead-free and Material Details** Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR at 100 kHz, 25°C
(3) Specified capacitance values

7.3.13 Output Capacitor Selection

The minimum required output capacitance of the TPSM41625 is a function of the output voltage and is shown in 表 7-3. The required capacitance can be comprised of all ceramic capacitors or a combination of ceramic and low-ESR polymer type capacitors. When adding additional capacitors, low-ESR capacitors like the ones recommended in 表 7-11 are required. The required capacitance above the minimum is determined by actual transient deviation requirements.

表 7-11. Recommended Output Capacitors

VENDOR(1)	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF) (3)	ESR (mΩ) (2)
Murata	X7R	GCM32ER70J476K	6.3	47	2
Taiyo Yuden	X7R	LMK325B7476MM-PR	10	47	2
Murata	X7R	GRM32ER71A476K	10	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Murata	X6S	GRM32EC80G227ME05L	4.0	220	2
Panasonic	POSCAP	4TPE220MF	4.0	220	15
Kemet	T520	T520D227M006ATE015	6.3	220	15
Panasonic	POSCAP	6TPE330MAA	6.3	330	10
Kemet	T520	T520D337M006ATE010	6.3	330	10
Kemet	T520	T520X337M010ATE010	10	330	10

(1) **Capacitor Supplier Verification , RoHS, Lead-free and Material Details** Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR at 100 kHz, 25°C
(3) Specified capacitance values

7.3.14 Current Limit (ILIM)

The current limit of the TPSM41625 is internally set to 32 A (typ.) by leaving the ILIM pin open. Connecting a resistor between the ILIM pin and AGND adjusts the current limit threshold lower. Refer to 表 7-12 for current limit adjustment values.

表 7-12. Current Limit Adjust

CURRENT LIMIT REDUCTION	10 %	20 %	30 %	40 %	50 %
R_{ILIM} (kΩ)	191	118	78.7	54.9	37.4

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7.3.15 Safe Start-up into Pre-Biased Outputs

The TPSM41625 device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During pre-biased start-up, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than the FB pin voltage and the high-side MOSFET begins to switch.

7.3.16 Overcurrent Protection

For protection against load faults, the TPSM41625 is protected from overcurrent conditions by cycle-by-cycle current limiting. In an extended overcurrent condition, the device enters hiccup mode to reduce power dissipation. In hiccup mode, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced, which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.17 Output Overvoltage and Undervoltage Protection

The device includes both output overvoltage protection and output undervoltage protection capability. The devices compare the RS+ pin voltage to internal selectable pre-set voltages. If the RS+ voltage with respect to RS- voltage rises above the output overvoltage protection threshold, the device terminates normal switching and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. Then, the device enters continuous restart hiccup.

If the RS+ pin voltage falls below the undervoltage protection level, after soft start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, then enters hiccup time-out delay prior to restart.

7.3.18 Overtemperature Protection

An internal temperature sensor protects the device from thermal runaway. The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 135°C typically.

7.4 Device Functional Modes

7.4.1 Active Mode

The TPSM41625 is in active mode when VIN is above the UVLO threshold and the EN pin voltage is above the EN high threshold. The EN pin has an internal current source to enable the output when the EN pin is left floating. If the EN pin is pulled low the device is put into a low quiescent current state.

7.4.2 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPSM41625. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode, the device is put into a low quiescent current state. The TPSM41625 also employs undervoltage lockout protection. If V_{IN} is below the UVLO level, the output of the regulator turns off.

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8 Application and Implementation

注

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8.1 Application Information

The TPSM41625 is a synchronous step-down DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 25 A. The following design procedure can be used to select components for the TPSM41625. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com/webench for more details.

8.2 Typical Application

The TPSM41625 requires only a few external components to convert from a wide input voltage supply range to a wide range of output voltages. 図 8-1 shows a typical TPSM41625 schematic with only the minimum required components.

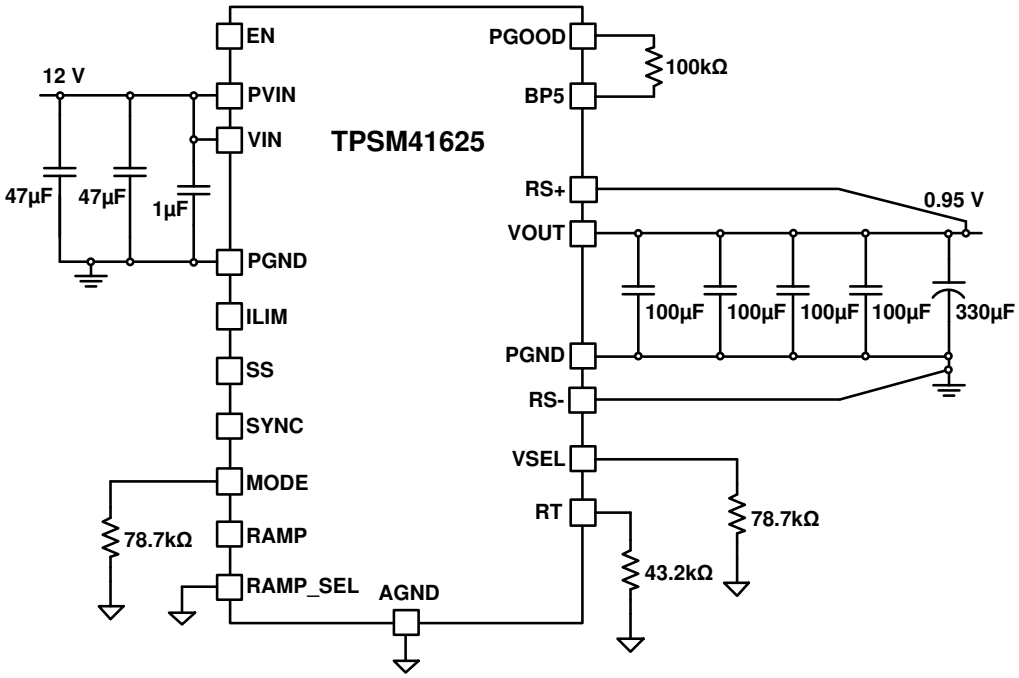


図 8-1. TPSM41625 Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1. Follow the design procedures in *セクション 8.2.2*.

表 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	12 V typical
Output voltage V_{OUT}	0.95 V
Output current rating	25 A

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表 8-1. Design Example Parameters (continued)

DESIGN PARAMETER	VALUE
Key care-abouts	Small solution size

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM41625 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM41625 is externally adjustable by first setting the reference voltage, V_{REF}, using the VSEL pin and then, if needed, setting the output voltage adjust resistor R_{ADJ}. For this application, V_{REF} is the same as the output voltage, so R_{ADJ} is not needed and RS+ should be connected to the output rail, near the load.

To set the output voltage to 0.95 V, select V_{REF} of 0.95 V by connecting a 78.7-kΩ resistor between VSEL pin and AGND and connect RS+ pin to the output voltage rail. VSEL resistor values for setting VREF can be found in 表 7-1.

8.2.2.3 Setting the Switching Frequency

To set the switching frequency of the TPSM41625, a resistor (R_{RT}) between the RT pin and AGND is required. Select the value of R_{RT} from 表 7-4. Before selecting the switching frequency, reference 表 7-3 for the allowable switching frequency range, required output capacitance, and RAMP setting for the desired output voltage.

For this application, after referencing 表 7-3, 500 kHz was selected and a 43.2-kΩ RT resistor is required for a 12-V input according to 表 7-4.

8.2.2.4 RAMP Setting

The value of the RAMP resistor, R_{RAMP}, must be selected based on the switching frequency and output capacitance of the application, as shown in 表 7-3. For this application, the required R_{RAMP} is 78.7 kΩ. There is a 78.7-kΩ resistor internal to the device connected between RAMP and RAMP_SEL. To select the internal 78.7-kΩ resistor, leave the RAMP pin open and connect RAMP_SEL to AGND.

8.2.2.5 Input Capacitors

The TPSM41625 requires a minimum of 88 µF of ceramic input capacitance. Applications with load transient requirements can benefit from adding addition bulk input capacitance.

For this design, two 47-µF ceramic capacitors rated for 25 V are used for the input decoupling capacitors.

Additionally, a 1-µF bypass capacitor is required on the VIN pin, close to the device pins.

8.2.2.6 Output Capacitors

The minimum required output capacitance for a 12-V input and 0.95-V output at 500 kHz switching frequency is 294 µF of ceramic capacitance, as well as an additional 430 µF of either ceramic or low-ESR polymer, as shown in 表 7-3.

For this design, four 100-µF ceramic capacitors plus a 330-µF polymer capacitor where used to meet the requirements.

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8.2.3 Application Waveforms

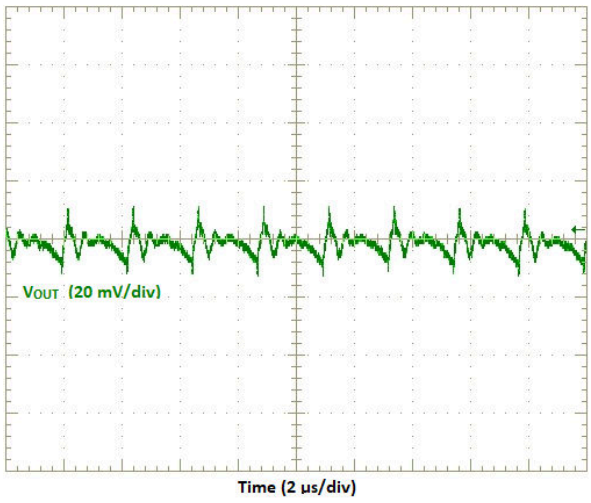


図 8-2. Output Ripple Waveform

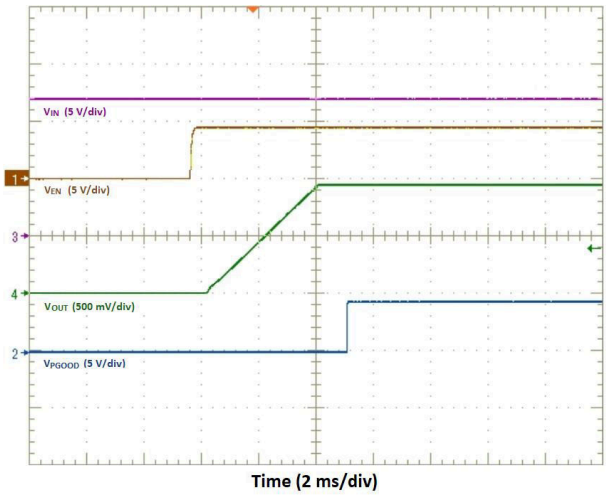


図 8-3. Start-Up Waveforms

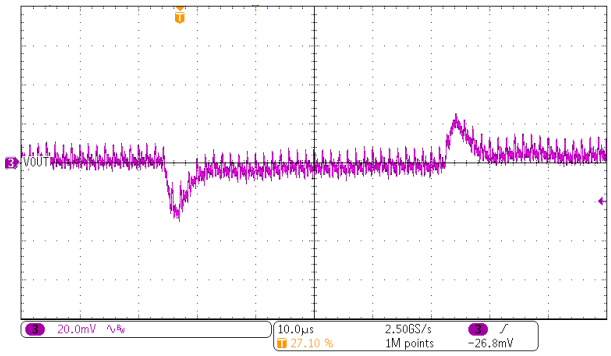


図 8-4. 10-A Transient Load Step

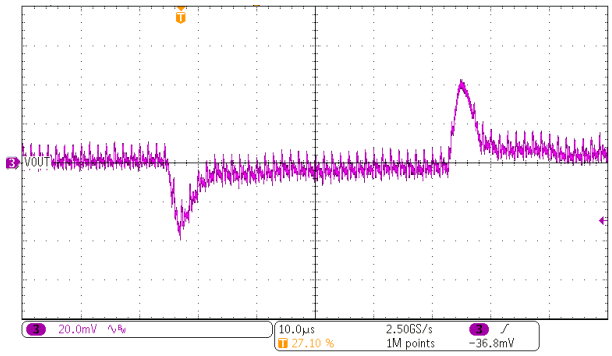


図 8-5. 15-A Transient Load Step

9 Power Supply Recommendations

The TPSM41625 is designed to operate from an input voltage supply range between 4 V and 16 V. The input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPSM41625 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the TPSM41625 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. Typically, a 47-µF or 100-µF electrolytic capacitor will suffice.

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10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 10-1 through 図 10-4 shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Place R_{VSEL}, R_{ADJ}, R_{RT}, R_{MODE}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes (PVIN, VOUT, and PGND) to internal layers.

10.2 Layout Examples

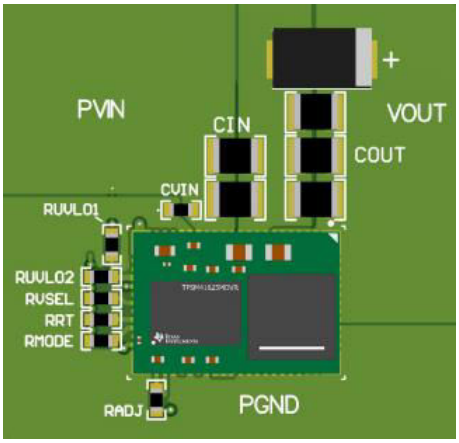


図 10-1. Top-Layer Components (Top View)

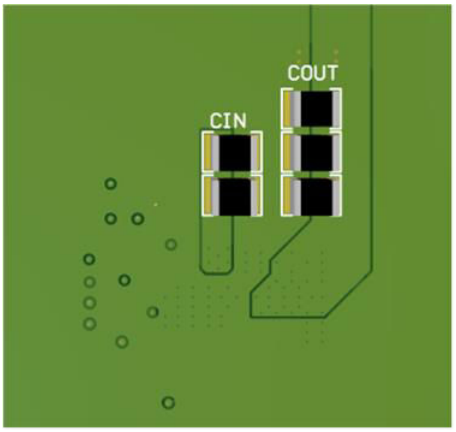


図 10-2. Bottom-Layer Components (Top View)

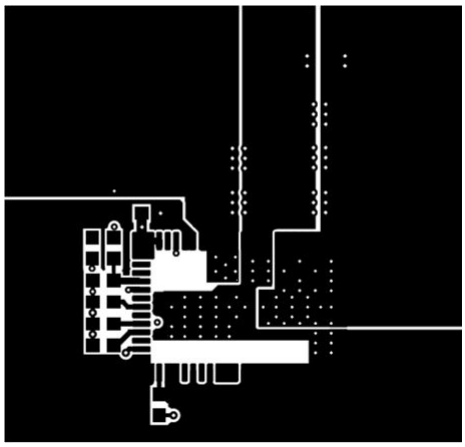


図 10-3. Top-Layer Layout (Top View)

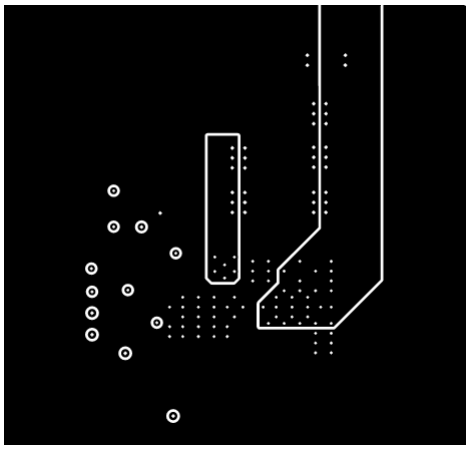


図 10-4. Bottom-Layer Layout (Top View)

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10.2.1 Package Specifications

TPSM41625		VALUE	UNIT
Weight		1.32	grams
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	39.7	MHrs

10.2.2 EMI

The TPSM41625 is compliant with EN55011 Class B radiated emissions. 図 10-5, 図 10-6, and 図 10-7 show typical examples of radiated emissions plots for the TPSM41625. The graphs include the plots of the antenna in the horizontal and vertical positions.

10.2.2.1 EMI Plots

EMI plots were measured using the standard TPSM41625EVM with an input filter in series with the input wires.

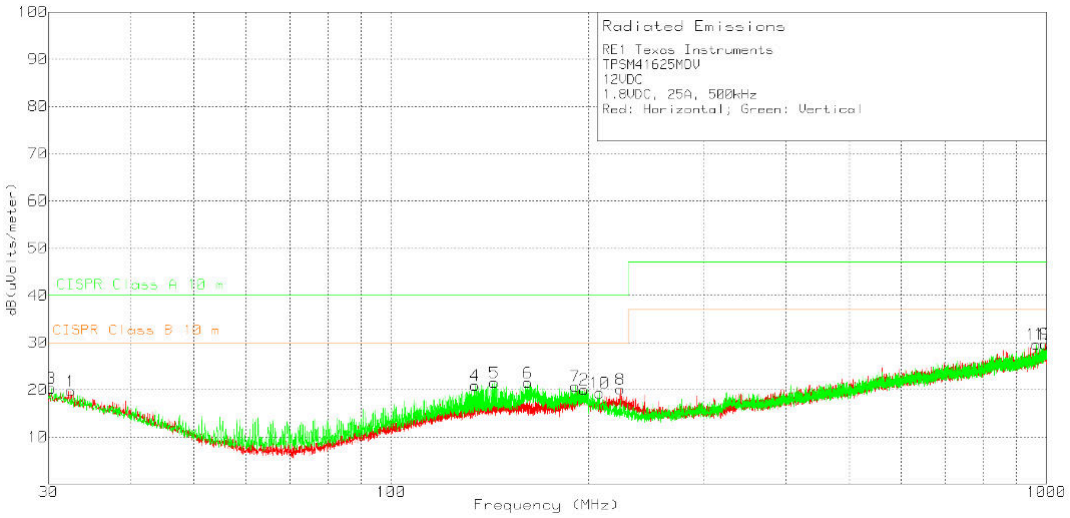


図 10-5. Radiated Emissions 12-V Input, 1.8-V Output, 25-A Load (EN55011 Class B)

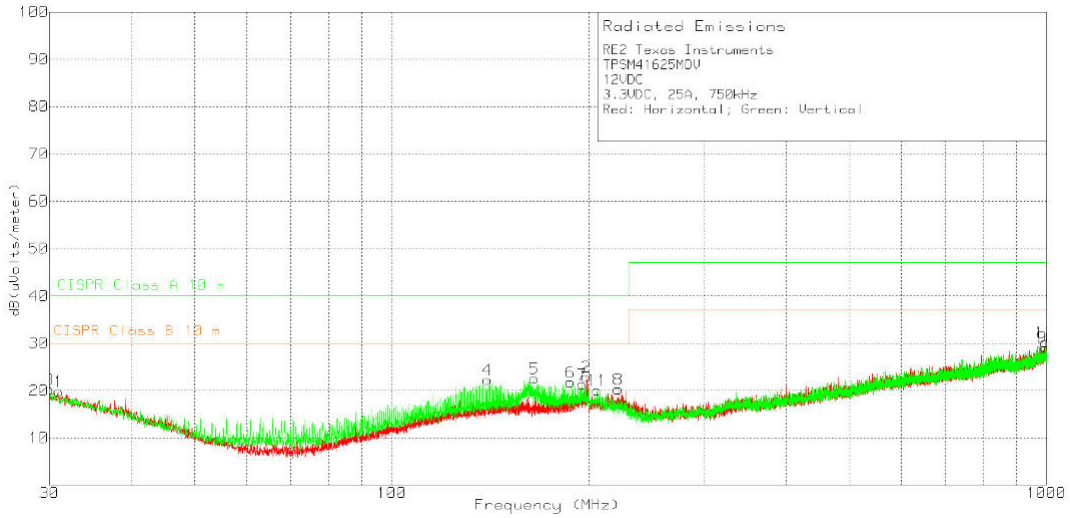


図 10-6. Radiated Emissions 12-V Input, 3.3-V Output, 25-A Load (EN55011 Class B)

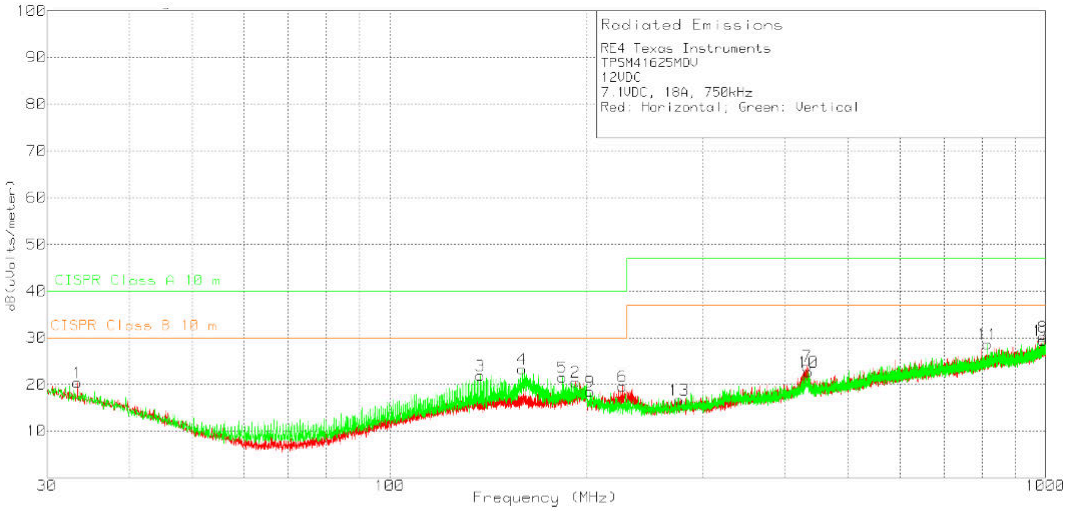


図 10-7. Radiated Emissions 12-V Input, 7.1-V Output, 18-A Load (EN55011 Class B)

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM41625 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM41625MOVR	Active	Production	QFM (MOV) | 69	500 | LARGE T&R	Exempt	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM41625 MOV
TPSM41625MOVR.A	Active	Production	QFM (MOV) | 69	500 | LARGE T&R	Exempt	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM41625 MOV
TPSM41625MOVR.B	Active	Production	QFM (MOV) | 69	500 | LARGE T&R	Exempt	NIAU	Level-3-260C-168 HR	-40 to 125	TPSM41625 MOV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

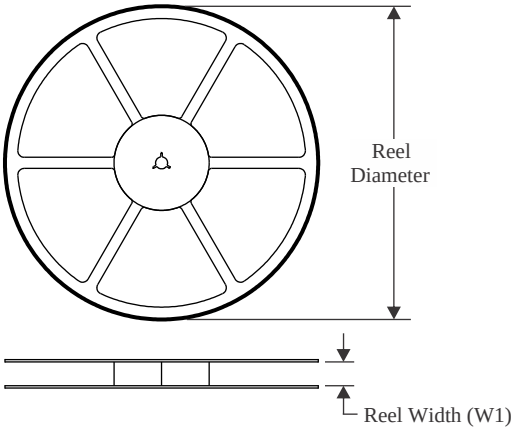
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

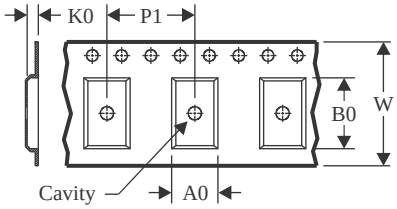
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

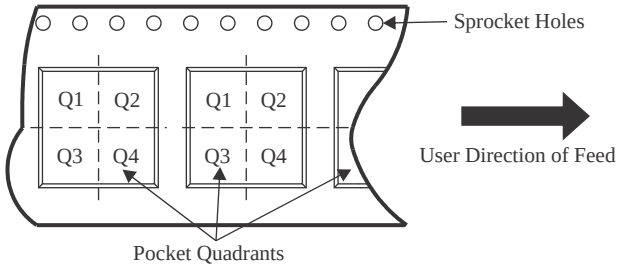


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

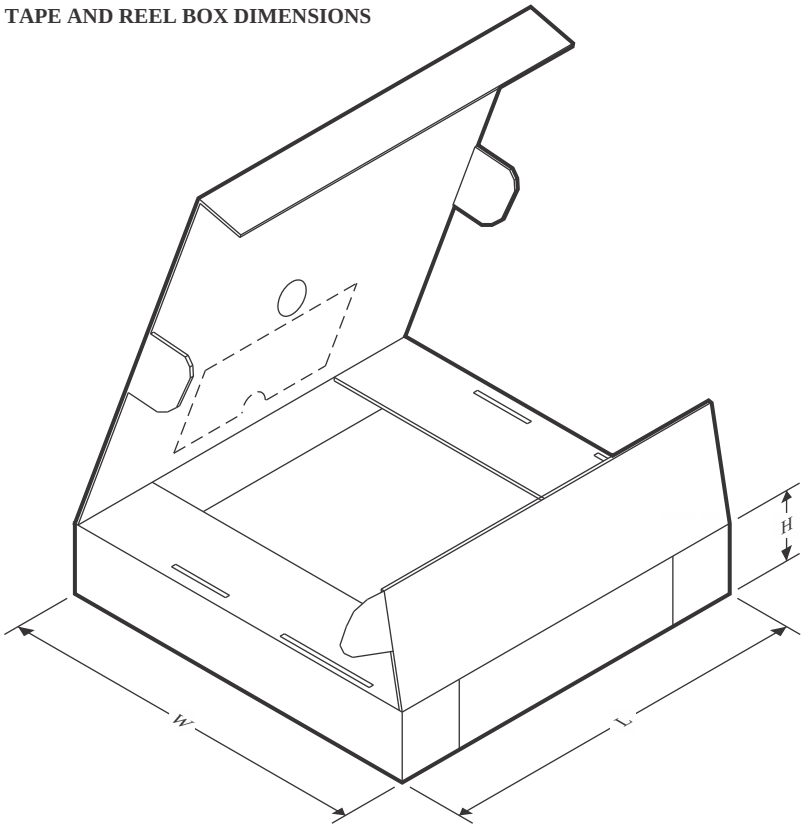
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM41625MOVR	QFM	MOV	69	500	330.2	32.4	11.4	16.4	4.69	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

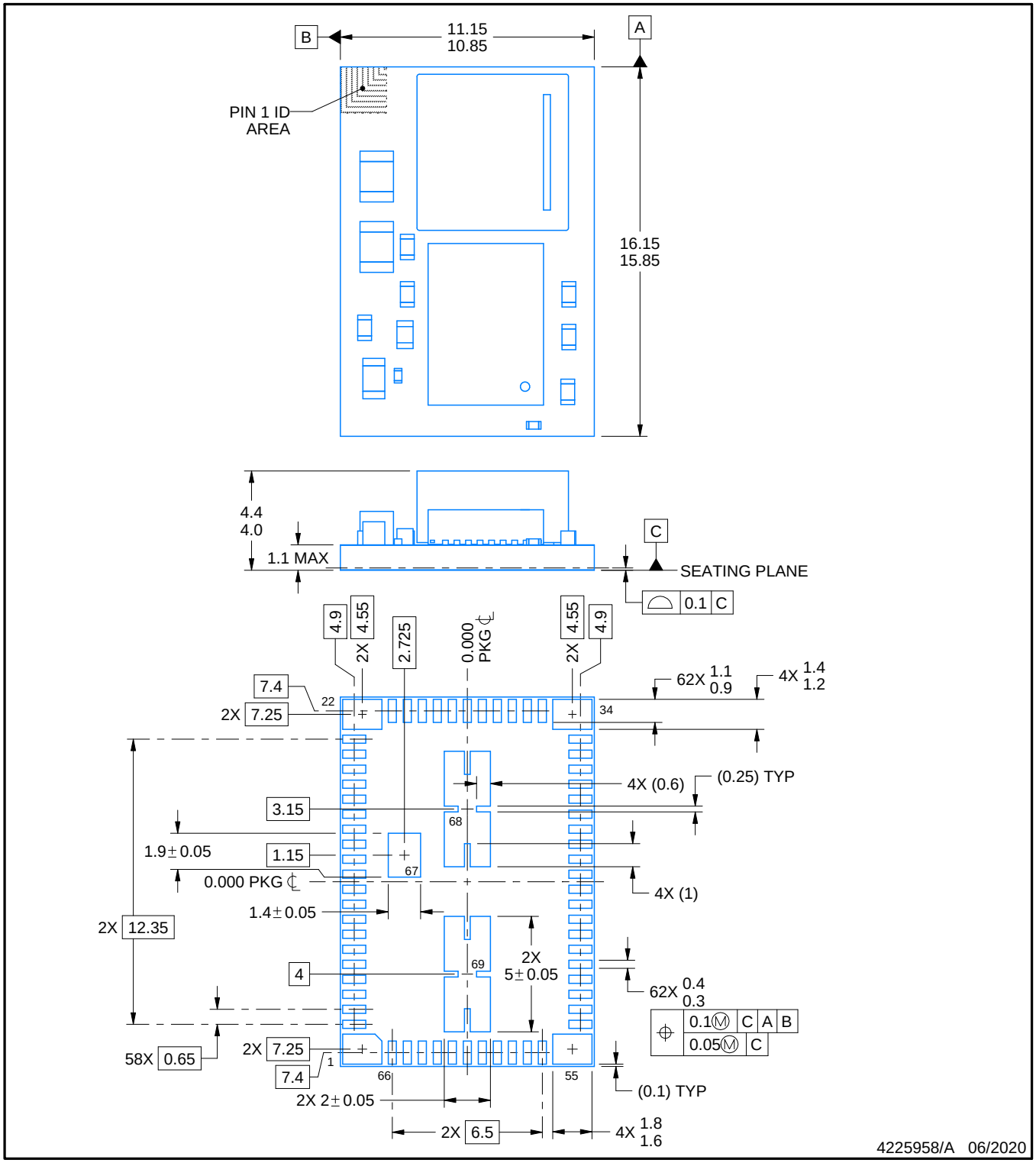
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM41625MOVR	QFM	MOV	69	500	381.0	381.0	101.6

PACKAGE OUTLINE

MOV0069A

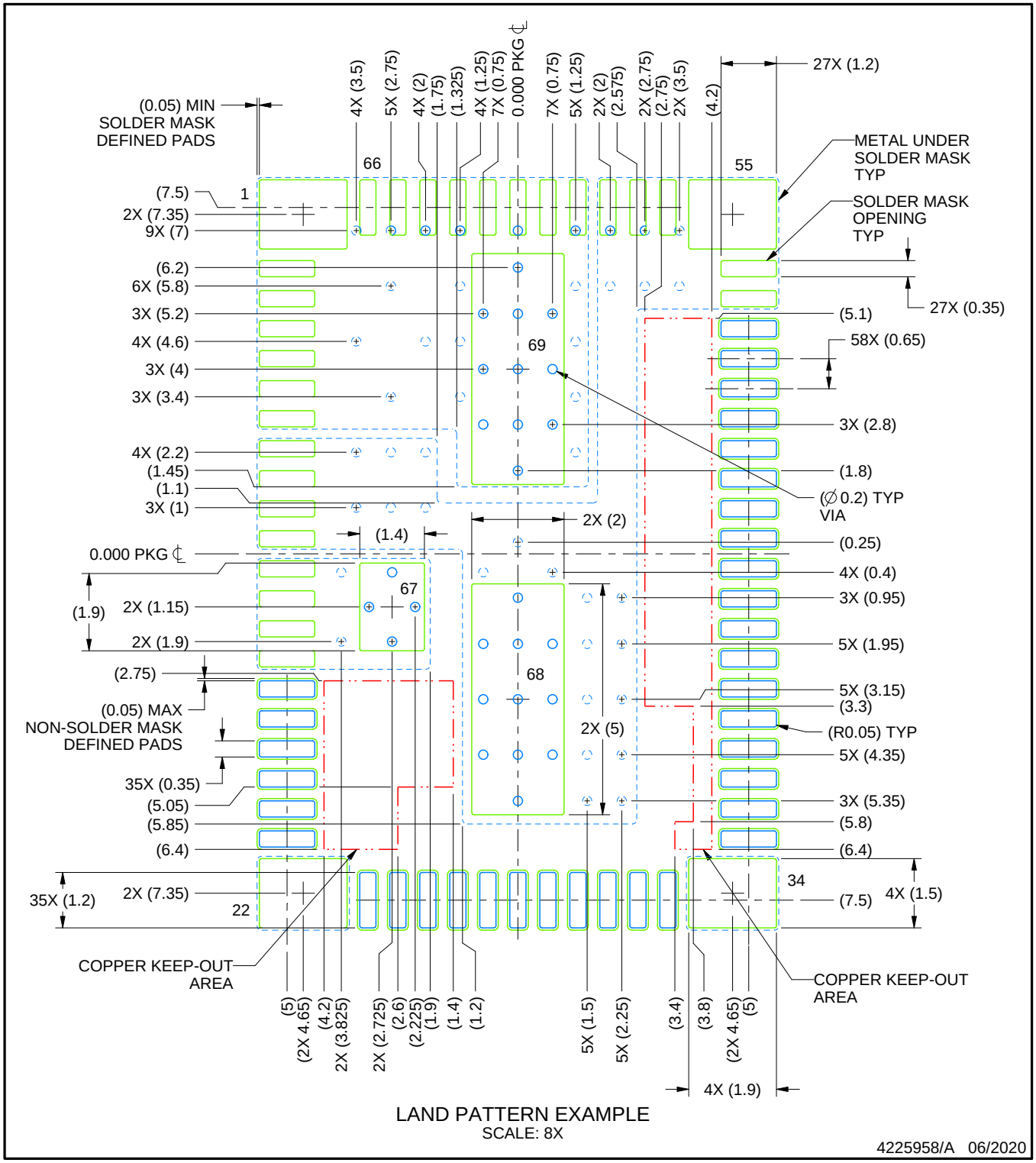
QFM - 4.4 mm max height

QUAD FLAT MODULE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

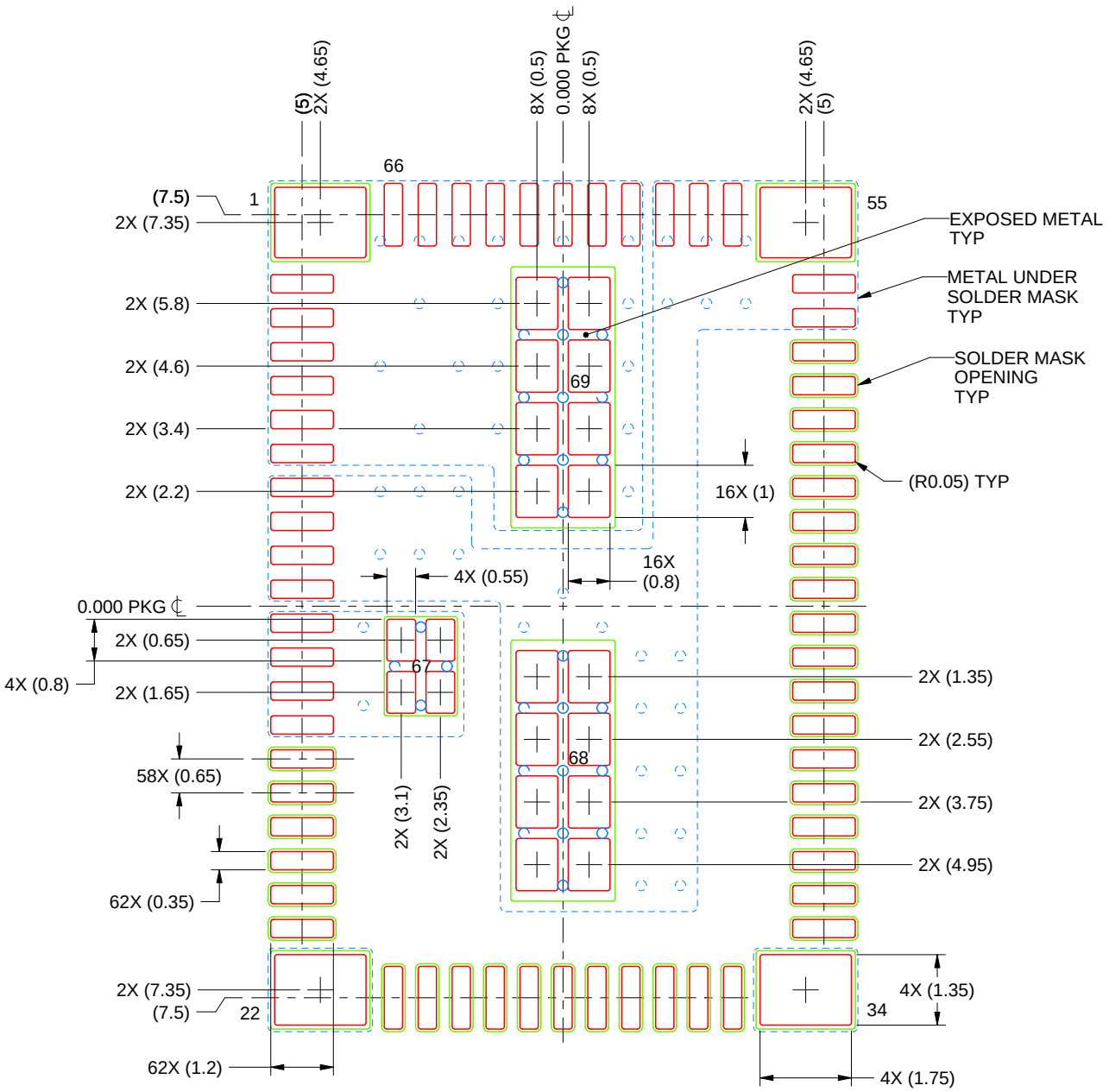


LAND PATTERN EXAMPLE
SCALE: 8X

4225958/A 06/2020

NOTES: (continued)

4. This package is designed to be soldered to the thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

66% SOLDER COVERAGE BY PRINTED AREA ON PAD 67
64% SOLDER COVERAGE BY PRINTED AREA ON PADS 68 & 69

4225958/A 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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