TEXAS INSTRUMENTS
TPSM560R6
JAJSLL6 – SEPTEMBER 2021

TPSM560R6、Enhanced HotRod™ QFN パッケージ封止、60V 入力、1V～6V 出力、600mA パワー・モジュール

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 5.0mm × 5.5mm × 4.0mm の Enhanced HotRod™ QFN
  - 優れた熱性能：85℃でエアフローなしのとき、最大 18W の出力
  - 標準的なフットプリント：1 つの大型サーマル・パッド、すべてのピンに外周から接続可能
- 高信頼性の堅牢なアプリケーション用に設計
  - 広い入力電圧範囲：4.2V～60V
  - 最大 66V の入力電圧過渡保護
  - 動作時の接合部温度範囲：-40℃～+125℃
  - 「EXT」サフィックスの接合部温度範囲：-55℃～+125℃
- 400kHz の固定スイッチング周波数
- FPWM 動作モード
- 超低 EMI 要件に最適化
  - シールド付きインダクタと高周波バイパス・コンデンサを内蔵
  - EN55011 EMI 規格に準拠
  - スペクトラム拡散オプションによって放射を低減
- 非スイッチング時の静止電流：26μA
- あらかじめ出力にバイアスが印加された状態でも単調にスタートアップ
- ループ補償またはブートストラップ部品が不要
- ヒステリシス付きの高精度イネーブルおよび入力 UVLO
- ヒステリシス付きのサーマル・シャットダウン保護
- WEBENCH® Power Designer を使用してカスタム・レギュレータ設計を作成

2 アプリケーション

- フィールド・トランスミッタおよびセンサ、PLC モジュール
- サーモスタット、ビデオ監視、HVAC システム
- AC およびサーボ・ドライブ、ロータリー・エンコーダ
- 産業用輸送、アセット・トラッキング
- 負出力アプリケーション

3 概要

TPSM560R6 電源モジュールは、60V 入力の降圧型 DC/DC コンバータとパワー MOSFET、シールド付きインダクタ、受動素子を、放熱特性の優れた QFN パッケージに統合した高集積 600mA 電源ソリューションです。5.0mm x 5.5mm x 4.0mm の 15 ピン QFN パッケージに Enhanced HotRod QFN テクノロジを採用し、熱性能の強化、小さなフットプリント、低 EMI を実現しています。1 つの大型サーマル・パッドを搭載し、パッケージのすべてのピンに外周からアクセスできるため、レイアウトが単純で製造時の扱いも簡単です。

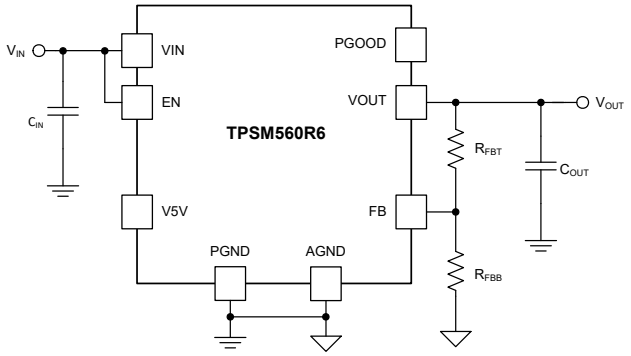
TPSM560R6 は、1.0V～6V と広い調整可能な出力電圧範囲を持つコンパクトで使いやすいパワー・モジュールです。ソリューション全体に必要な外付け部品はわずか 4 つであり、設計プロセスではループ補償と磁気部品選択は不要です。パワー・グッド、プログラム可能な UVLO、プリバイアス・スタートアップ、過電流および過熱保護などの完全な機能セットを備えているため、TPSM560R6 は広範なアプリケーションの電源として非常に優れたデバイスです。5.0mm × 5.5mm のパッケージは、スペースに制約のあるアプリケーションに適しています。

デバイス情報

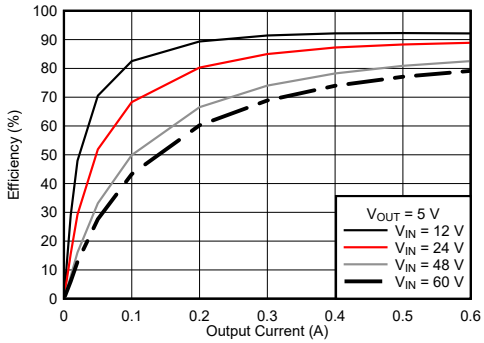
部品番号	パッケージ(1)	本体サイズ (公称)
TPSM560R6	QFN (15)	5.0mm × 5.5mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。



代表的な回路図



標準的な効率、V_{OUT} = 5V

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 3
5 Pin Configuration and Functions ... 4
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 6
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 7
6.6 Typical Characteristics (V_{IN} = 12 V) ... 8
6.7 Typical Characteristics (V_{IN} = 24 V) ... 9
6.8 Typical Characteristics (V_{IN} = 48 V) ... 10
6.9 Typical Characteristics (V_{IN} = 60 V) ... 11
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 12
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 15
8 Applications and Implementation ... 17
8.1 Application Information ... 17
8.2 Typical Application ... 17
9 Power Supply Recommendations ... 19
10 Layout ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 20
11 Device and Documentation Support ... 24
11.1 Device Support ... 24
11.2 Documentation Support ... 24
11.3 Receiving Notification of Documentation Updates ... 24
11.4 サポート・リソース ... 24
11.5 Trademarks ... 24
11.6 Electrostatic Discharge Caution ... 25
11.7 Glossary ... 25
12 Mechanical, Packaging, and Orderable Information ... 25

4 Revision History

DATE	REVISION	NOTES
September 2021	*	Initial release

5 Pin Configuration and Functions

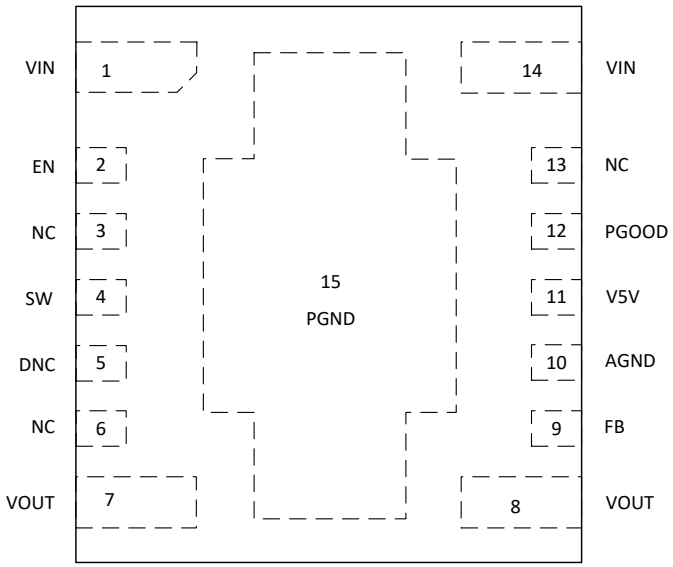

図 5-1. 15-Pin QFN RDA Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
10	AGND	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. *This pin must be connected to PGND at a single point.* See セクション 10.2 for a recommended layout.
5	DNC	—	Do not connect. Do not connect this pin to ground, to another pin, or to any other voltage. This pin is connected to the internal bootstrap capacitor. This pin must be soldered to an isolated pad.
2	EN	I	Enable pin. This pin turns the converter on when pulled high and turns off the converter when pulled low. This pin can be connected directly to VIN. *Do not float.* This pin can be used to set the input undervoltage lockout with two resistors. See セクション 7.3.4.
9	FB	I	Feedback input. Connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND.
3, 6, 13	NC	—	Not connected. These pins are not connected to any circuitry within the module. Leaving these pins unconnected to any other signal increases spacing near the high voltage pins (VIN, SW, EN, and DNC). However, if the high voltage spacing is not needed in the application, connecting these pins to the PGND plane can help enhance shielding and thermal performance.
15	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, load return, and capacitors associated with the VIN and VOUT pins. See セクション 10.2 for a recommended layout.
12	PGOOD	O	Power-good pin. An open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required and can be tied to the V5V pin or other DC voltage less than 18 V. If not used, this pin can be left open or connected to PGND.
4	SW	O	Switch node. Do not place any external component on this pin or connect to any signal.
1, 14	VIN	I	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.
7, 8	VOUT	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
11	V5V	O	Internal 5-V LDO output. Supplies internal control circuits. Do not connect to external loads. This pin can be used as logic supply for the PGOOD pin.

(1) G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over the operating ambient temperature range[1]

PARAMETER		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	66	V
	EN to AGND[2]	–0.3	V_{IN} + 0.3	
	PGOOD to AGND[2]	–0.3	22	
	FB to AGND	–0.3	5.5	
	AGND to PGND	–0.3	0.3	
Output voltage	VOUT to PGND[2]	–0.3	30	
	VCC to AGND	0	5.5	
Operating IC junction temperature, T_J [3]		–40	125	°C
Storage temperature, T_{stg}		–55	150	
Peak reflow case temperature			245	
Maximum number or reflows allowed			3	
Mechanical vibration	Mil-STD-883H, Method 2007.3, 1 msec, 1/2 sine, mounted		20	G
Mechanical shock	Mil-STD-883H, Method 2002.5, 20 to 2000Hz		500	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the *Typical Characteristics* sections, makes sure that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)[1]	±1500	V
		Charged-device model (CDM)[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Input voltage, V_{IN}	4.2	60	V
Output voltage, V_{OUT}	1	6 (3)	V
Output current, I_{OUT}	0	0.6	A
EN voltage, V_{EN} (2)	0	V_{IN}	V
PGOOD pullup voltage, V_{PGOOD} (2)	0	18	V
Operating ambient temperature, T_A	–40	105	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For specifications, see the *Electrical Characteristics*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The recommended maximum output voltage varies depending input voltage.

6.4 Thermal Information

THERMAL METRIC(1)			TPSM560R6 RDA (QFN) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	Nat Conv	20.4	°C/W
		100 LFM	18.9	°C/W
		200 LFM	17.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)		3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)		15.3	°C/W
T_{SHDN}	Thermal shutdown temperature		170	°C
	Recovery temperature		158	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 6.35-cm × 8.25-cm, four-layer PCB with 2-oz. copper. Additional airflow and PCB copper area reduces $R_{\theta JA}$. See セクション 10.2.1 for more information.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

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6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +105°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 600 mA, (unless otherwise noted); minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN}	Input voltage range	Over I_{OUT} range	4.2 (1)		60	V
	V_{IN} turn on	V_{IN} increasing, I_{OUT} = 0 A, V_{EN} = V_{IN}		3.8		V
	V_{IN} turn off	V_{IN} decreasing, I_{OUT} = 0 A, V_{EN} = V_{IN}		3.3		V
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, I_{OUT} = 0 A		5		µA
INTERNAL LDO (V5V)						
V5V	Internal LDO output voltage appearing at the V5V pin	6 V ≤ V_{IN} ≤ 60 V	4.75	5	5.25	V
FEEDBACK						
V_{FB}	Load regulation	T_A = +25°C, 0 A ≤ I_{OUT} ≤ 0.6 A		0.057%		
V_{FB}	Line regulation	T_A = +25°C, I_{OUT} = 0 A, 6 V ≤ V_{IN} ≤ 60 V		0.024%		
I_{FB}	Current into the FB pin	FB = 1 V		0.2		nA
CURRENT						
I_{OUT}	Output curren	T_A = 25ºC	0		0.6	A
I_{OUT}	Overcurrent threshold	V_{OUT} = 3.3 V, T_A = 25ºC		0.89		A
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
ENABLE (EN PIN)						
$V_{EN-VCC-H}$	EN input level required to turn on internal LDO	Rising threshold			1.14	V
$V_{EN-VCC-L}$	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V_{EN-H}	EN input level required to start switching	Rising threshold	1.157	1.231	1.30	V
V_{EN-HYS}	Hysteresis below V_{EN-H}	Hysteresis below V_{EN-H}; falling		110		mV
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.2		nA
POWER GOOD (PGOOD PIN)						
$V_{PG-LOW-UP}$	V_{OUT} rising (fault)	% of FB voltage		107%		
$V_{PG-HIGH-DN}$	V_{OUT} falling (good)	% of FB voltage		105%		
$V_{PG-HIGH-UP}$	V_{OUT} rising (good)	% of FB voltage		95%		
$V_{PG-LOW-DN}$	V_{OUT} falling (fault)	% of FB voltage		93%		
R_{PG}	Power-good flag R_{DSON}	V_{EN} = 0 V		35		Ω
V_{IN-PG}	Minimum input voltage for proper PGOOD function	I_{PG} = 50 µA, EN = 0 V			2	V
PERFORMANCE						
η	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 0.75 A, T_A = 25ºC		81%		
η	Efficiency	V_{OUT} = 5.0 V, I_{OUT} = 0.75 A, T_A = 25ºC		86%		
SOFT START						
t_{SS}	Internal soft-start time			4.5		ms
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	I_{OUT} = 0.75 A, T_A = 25ºC	340	400(2)	460	kHz

(1) The recommended minimum V_{IN} is 4.2 V or (V_{OUT} + 600 mV), whichever is greater.
(2) The typical switching frequency of this device changes based on operating conditions.

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6.6 Typical Characteristics (V_{IN} = 12 V)

T_A = 25°C, unless otherwise noted.

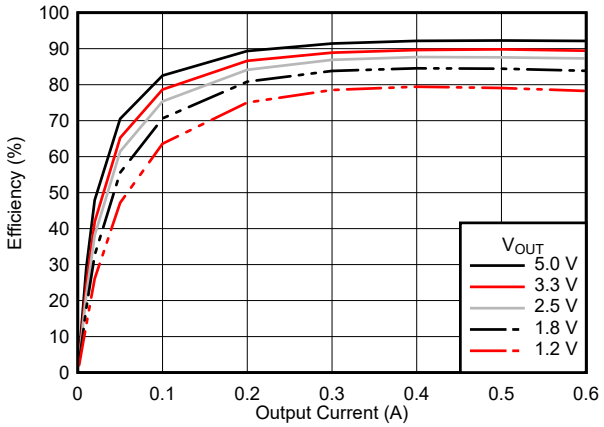


図 6-1. Efficiency

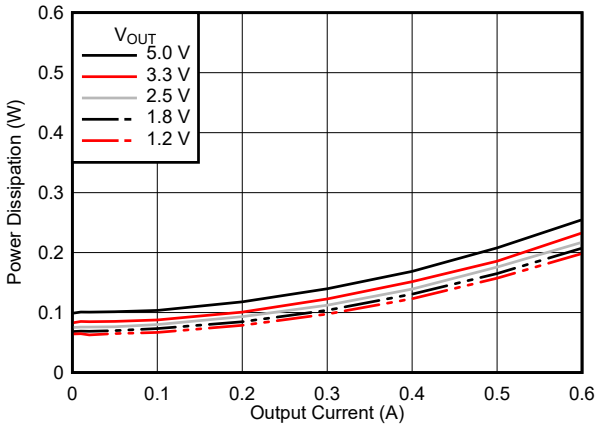
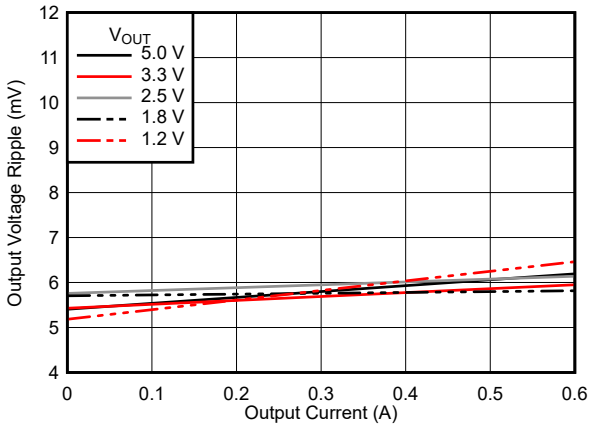
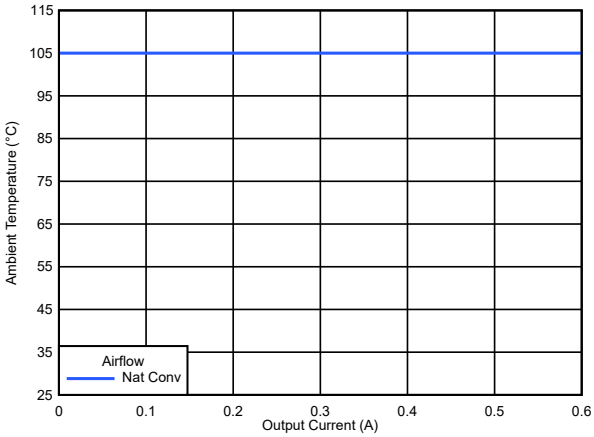


図 6-2. Power Dissipation



C_{OUT} = 2 × 47 µF, 25-V, ceramic

図 6-3. Output Voltage Ripple



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

図 6-4. Safe Operating Area (All V_{OUT})

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6.7 Typical Characteristics (V_{IN} = 24 V)

T_A = 25°C, unless otherwise noted.

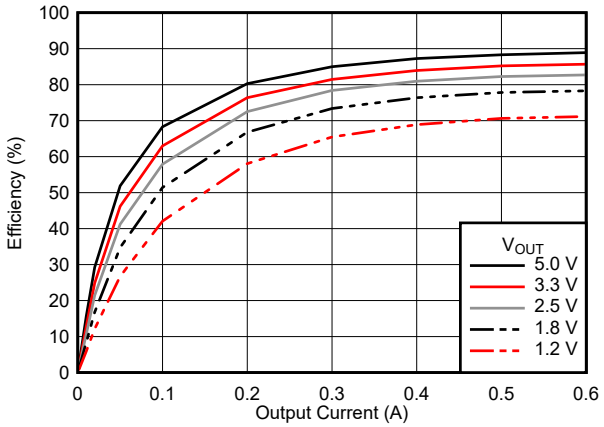


図 6-5. Efficiency

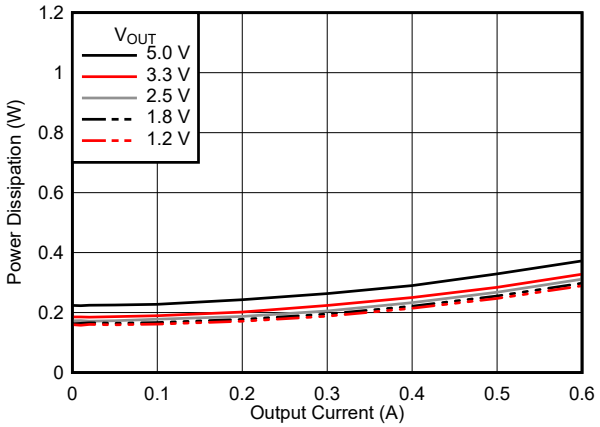
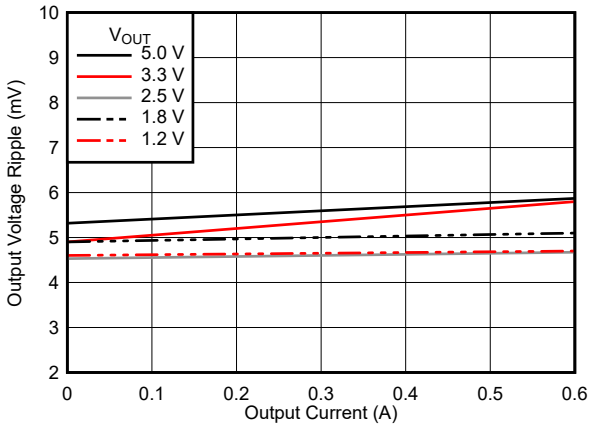
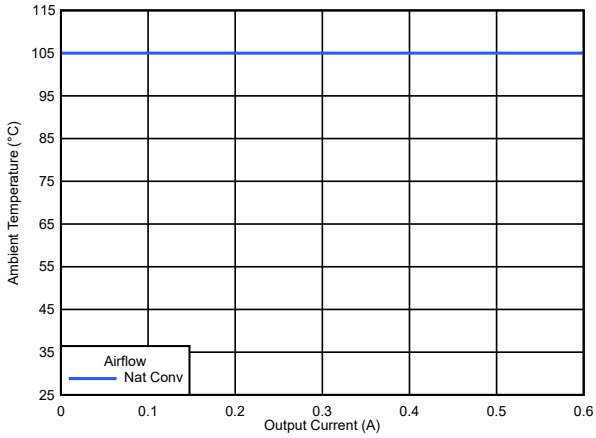


図 6-6. Power Dissipation



C_{OUT} = 2 × 47-µF, 25-V, ceramic

図 6-7. Output Voltage Ripple



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

図 6-8. Safe Operating Area (All V_{OUT})

6.8 Typical Characteristics (V_{IN} = 48 V)

T_A = 25°C, unless otherwise noted.

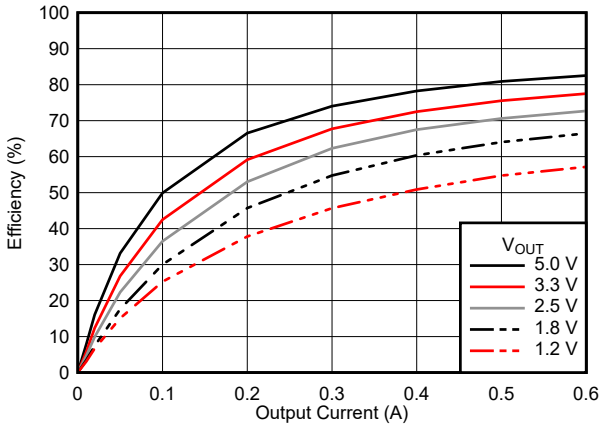


図 6-9. Efficiency

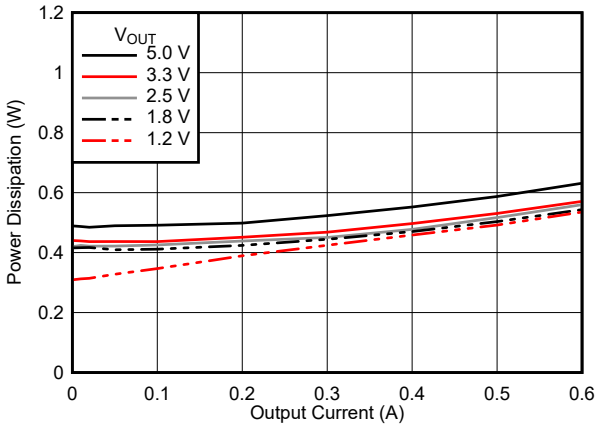
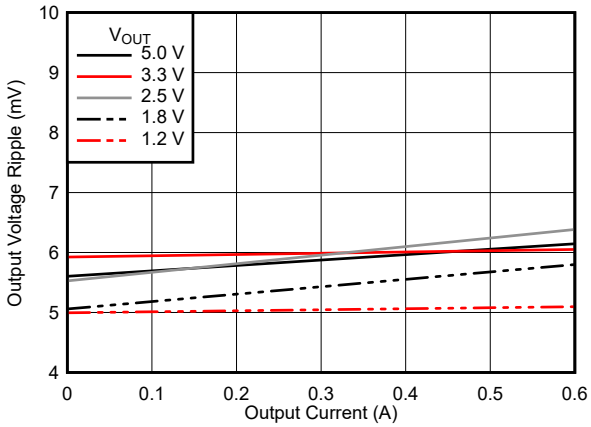
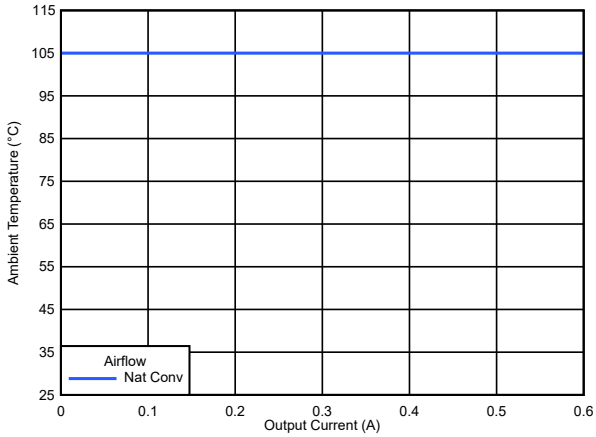


図 6-10. Power Dissipation



C_{OUT} = 2 × 47-µF, 25-V, ceramic

図 6-11. Output Voltage Ripple



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

図 6-12. Safe Operating Area (All V_{OUT})

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6.9 Typical Characteristics (V_{IN} = 60 V)

T_A = 25°C, unless otherwise noted.

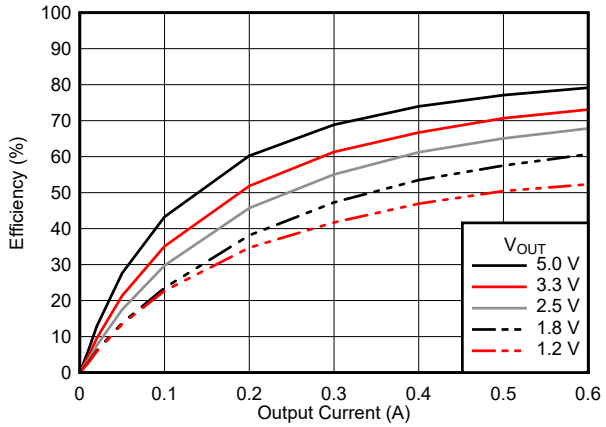


図 6-13. Efficiency

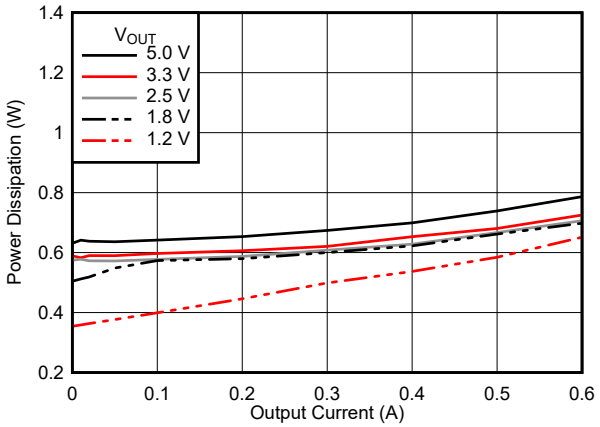
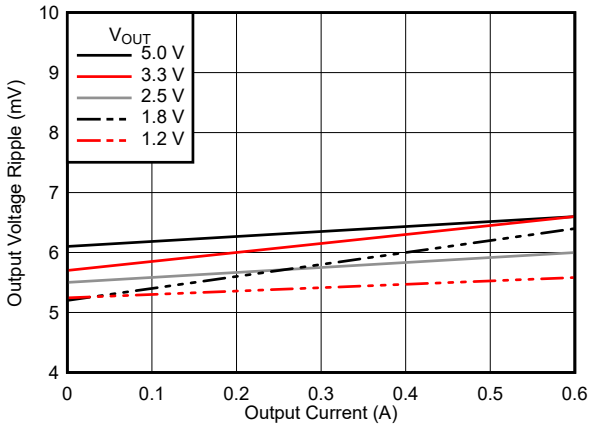
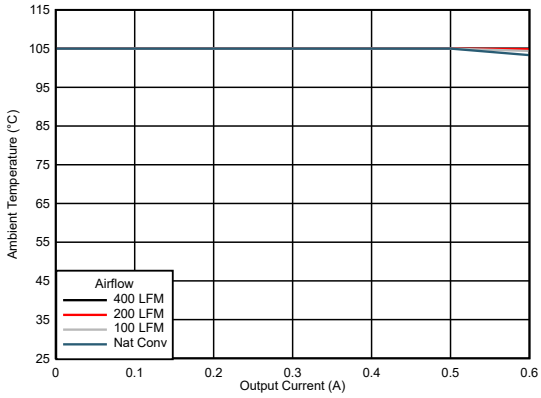


図 6-14. Power Dissipation



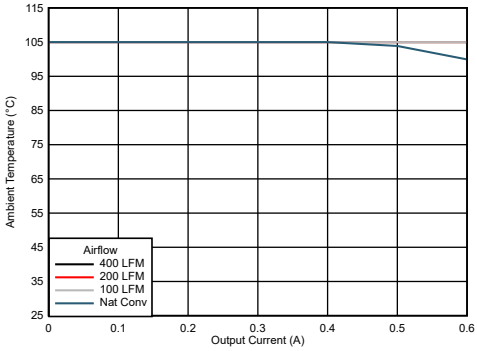
C_{OUT} = 2 × 47-µF, 25-V, ceramic

図 6-15. Output Voltage Ripple



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

図 6-16. Safe Operating Area (V_{OUT} = 3.3 V)



Device soldered to a 63.5-mm × 82.5-mm, 4-layer PCB

図 6-17. Safe Operating Area (V_{OUT} = 5.0 V)

7 Detailed Description

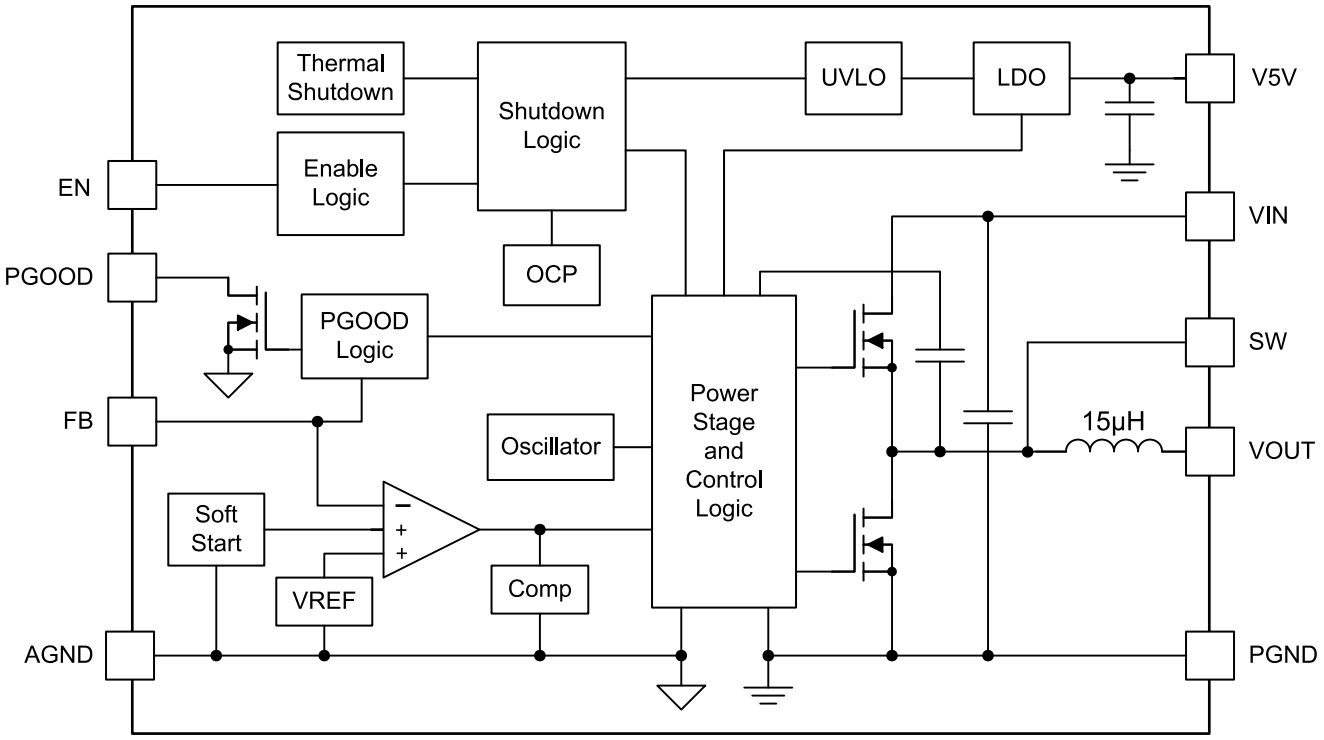
7.1 Overview

The TPSM560R6 converter is an easy-to-use, synchronous buck, DC-DC power module that operates from a 4.2-V to 60-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated, or fully-regulated supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM560R6 delivers up to 600-mA DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

The TPSM560R6 incorporates several features for comprehensive system requirements, including the following:

- An open-drain power-good circuit for power-rail sequencing and fault reporting
- Monotonic start-up into prebiased loads
- Precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO)
- Overcurrent and thermal shutdown with automatic recovery

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjustable Output Voltage (FB)

The TPSM560R6 has an adjustable output voltage range of 1.0 V to 6 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see 図 7-1). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be calculated using 式 1.

$$R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT} \quad (1)$$

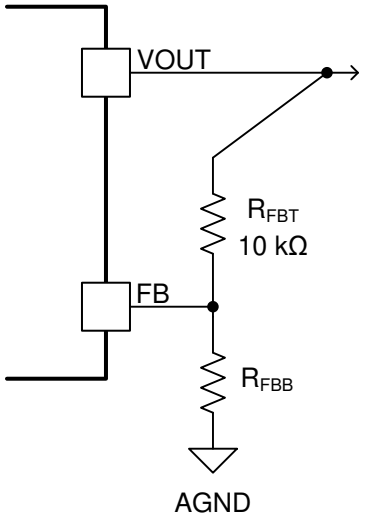

図 7-1. FB Resistor Divider

表 7-1. Standard R_{FBB} Values

VOUT (V)	R_{FBB} (kΩ) (1)
1.0	open
1.2	49.9
1.5	20.0
1.8	12.4
2.0	10.0
2.5	6.65
3.0	4.99
3.3	4.32
5.0	2.49
6.0	2.0

(1) R_{FBT} = 10 kΩ

Select an R_{FBT} value of 10 kΩ for most applications. Larger R_{FBT} consumes less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see セクション 10.

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7.3.2 Minimum Input Capacitance

The TPSM560R6 requires a minimum input capacitance of 9.4 µF (2 × 4.7 µF) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are required. Place the input capacitors, as close as possible to both VIN pins of the device between VIN and PGND, as shown in セクション 10.1. Applications with transient load requirements can benefit from adding additional bulk capacitance to the input as well.

7.3.3 Minimum Output Capacitance

The TPSM560R6 requires a minimum amount of ceramic output capacitance depending on the output voltage setting. The amount of required output capacitance is shown in 図 7-2 and is the amount of *effective* capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contributes to differences between the standard rated value and the actual effective value of the capacitance. Additional output capacitance above the minimum can be added to reduce output voltage ripple and to improve transient response. When adding additional capacitance above the minimum, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two.

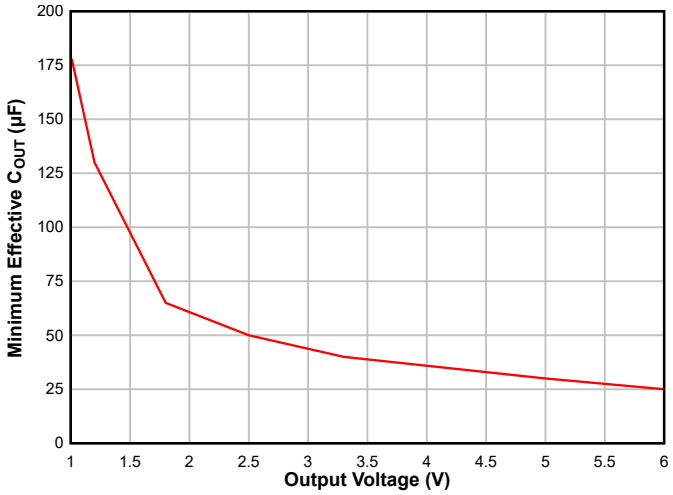

図 7-2. Minimum Required Output Capacitance

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7.3.4 Precision Enable (EN), Undervoltage Lockout (UVLO), and Hysteresis (HYS)

The EN pin provides precision ON and OFF control for the TPSM560R6. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. The simplest way to enable the device is to connect EN directly to VIN. This allows the device to start up when V_{IN} is within its valid operating range. An external logic signal can also be used to drive the EN input to toggle the output on and off and for system sequencing or protection. *This input must not be allowed to float.*

The TPSM560R6 implements internal undervoltage lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.8 V (typical) with a typical hysteresis of 500 mV.

If an application requires a higher UVLO threshold, the EN input supports adjustable UVLO by connecting a resistor divider from VIN to the EN pin. Applying a voltage greater than or equal to 1.14 V causes the device to enter Standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to 1.231 V (typical) fully enables the device, allowing it to enter Start-up mode and start the soft-start period. When the EN input is brought below 1.121 V (110-mV hysteresis), the regulator stops running and enters Standby mode. Further decrease in the EN voltage to below 0.3 V completely shuts down the device.

The TPSM560R6 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. The rise time of the output voltage is approximately 4 ms.

7.3.5 Power Good (PGOOD)

The TPSM560R6 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 18 V. V5V or VOUT can be used as the pullup voltage source. A typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. If this function is not needed, the PGOOD pin must be grounded.

When the output voltage exceeds 95% (rising) or decreases below 105% (falling) of the setpoint, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 93% or rises above 107% of the setpoint, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation.

Note that during initial power up, a delay of approximately 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

7.3.6 Overcurrent Protection (OCP)

The TPSM560R6 is protected from overcurrent conditions using cycle-by-cycle current limiting for overload conditions and Hiccup mode for short circuits. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

7.3.7 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM560R6 restarts when the junction temperature falls to 158°C (typical).

7.4 Device Functional Modes

7.4.1 Active Mode

The TPSM560R6 is in Active mode when VIN is above the turn-on threshold and the EN pin voltage is above the EN high threshold. Connect the EN pin to VIN to allow the device to start up when a valid input voltage is applied. This allows self start-up of the TPSM560R6 when the input voltage is in the operation range of 4.2 V to 60 V. Connecting a resistor divider between VIN, EN, and AGND adjusts the UVLO to delay the turn on until VIN is closer to its regulated voltage.

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7.4.2 Standby Mode

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO. Applying a voltage greater than or equal to 1.14 V causes the device to enter Standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to 1.231 V (typical) fully enables the device, allowing it to enter Start-up mode and starting the soft-start period. When the EN input is brought below 1.121 V (110-mV hysteresis), the regulator stops running and enters Standby mode. Further decrease in the EN voltage to below 0.3 V completely shuts down the device.

7.4.3 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM560R6. When V_{EN} is below the EN low threshold, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 5 µA at V_{IN} = 24 V.

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8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM560R6 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM560R6, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM560R6 power module.

As mentioned previously, the TPSM560R6 also integrates several optional features to meet system design requirements, including precision enable, UVLO, and PGOOD indicator. The following application circuit shows the TPSM560R6 configuration options suitable for several application use cases. Refer to the *TPSM560R6EVM User's Guide* for more detail.

8.2 Typical Application

図 8-1 shows the schematic diagram of a 24-V input, 5-V output, 600-mA converter.

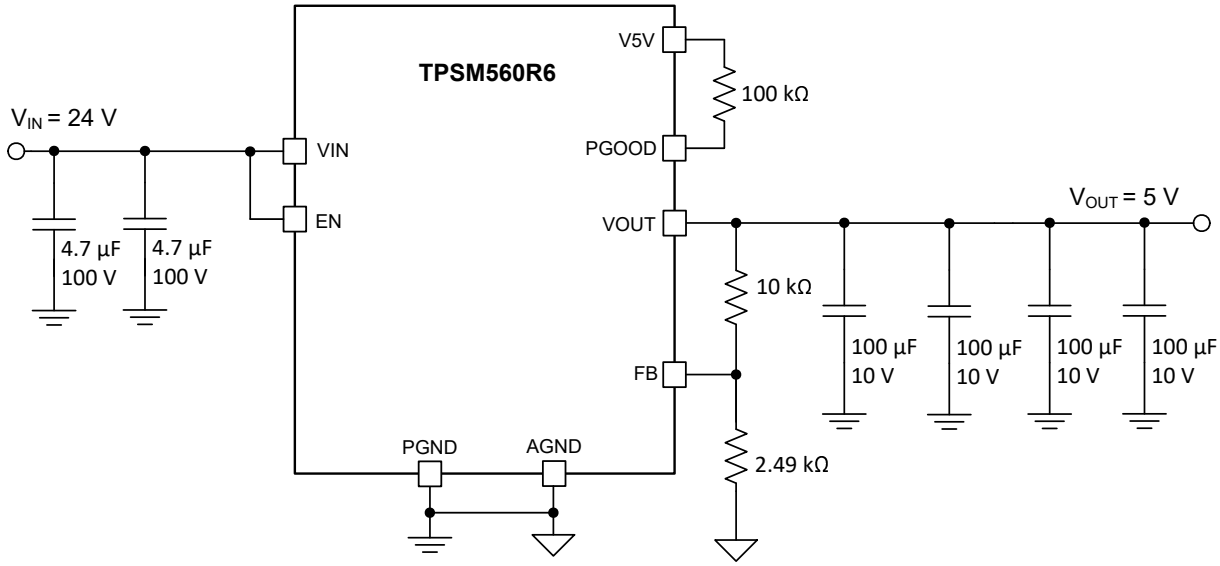

図 8-1. TPSM560R6 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters and follow the design procedures in セクション 8.2.2.

表 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	600 mA

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM560R6 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM560R6 device is externally adjustable using a resistor divider. The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be selected from 表 7-1 or calculated using 式 2:

$$R_{FBB} = \frac{1.0}{V_{OUT} - 1.0} \times R_{FBT} \quad (2)$$

For the desired output voltage of 5 V, the formula yields a value of 2.5 kΩ. Choose the closest available standard value of 2.49 kΩ for R_{FBB}.

8.2.2.3 Input Capacitors

The TPSM560R6 requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, 2 × 4.7-µF, 100-V ceramic capacitors are selected.

8.2.2.4 Output Capacitor Selection

The TPSM560R6 requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies with the output voltage. See 図 7-2 for the required output capacitance. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, 4× 100-µF, 10-V, ceramic capacitors are used.

8.2.2.5 Power-Good Signal

Applications requiring a power-good signal to indicate that the output voltage is present and in regulation must use a pullup resistor between the PGOOD pin and a valid voltage source.

For this design a 100-kΩ resistor is placed between the PGOOD pin and the V5V pin (the internal 5-V LDO output).

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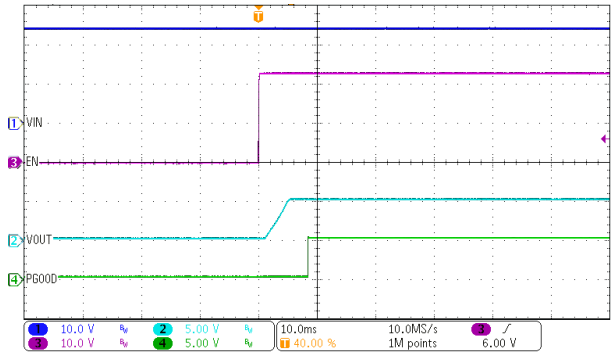
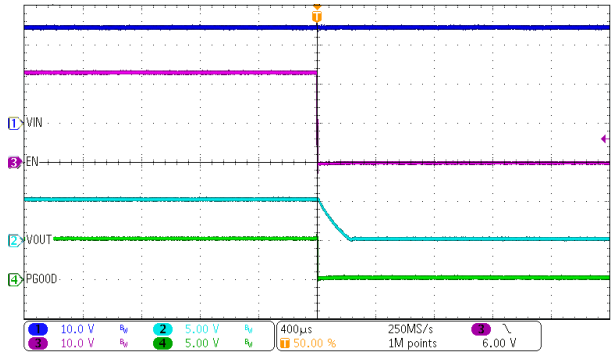
8.2.3 Application Curves



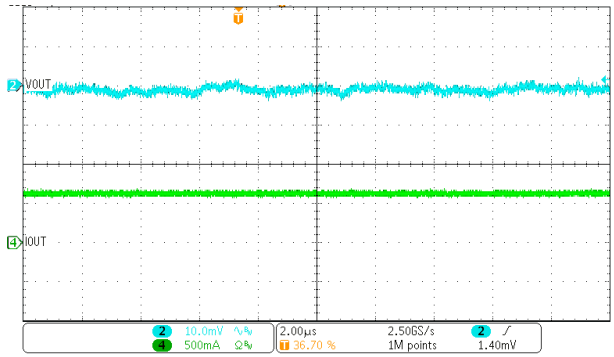
V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 600 mA

図 8-2. Start-Up Waveforms



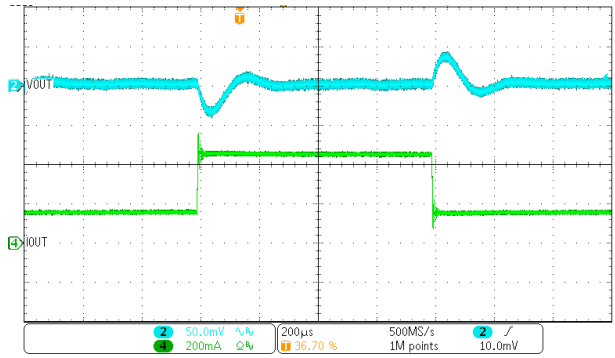
V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 600 mA

図 8-3. Enable Shutdown Waveforms



C_{OUT} = 4 × 100 µF I_{OUT} = 600 mA

図 8-4. Output Ripple Waveform



C_{OUT} = 4 × 100 µF 300-mA load step 2.5 A/µs

図 8-5. Transient Response Waveform

9 Power Supply Recommendations

The TPSM560R6 is designed to operate from an input voltage supply range between 4.2 V and 60 V. This input supply must be able to provide the maximum input current and maintain a voltage above the set UVLO voltage. Make sure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the TPSM560R6 supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPSM560R6, additional bulk capacitance can be required in addition to the ceramic input capacitance. A 47-µF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

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10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 10-1 and 図 10-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- *Connect all PGND pins together using copper plane.*
- Connect AGND pin to the PGND copper at a single point near the pin.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place R_{FBT} and R_{FBB} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

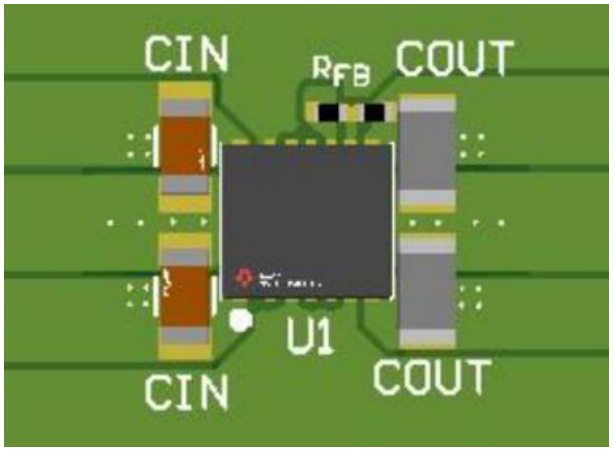

図 10-1. Typical Layout

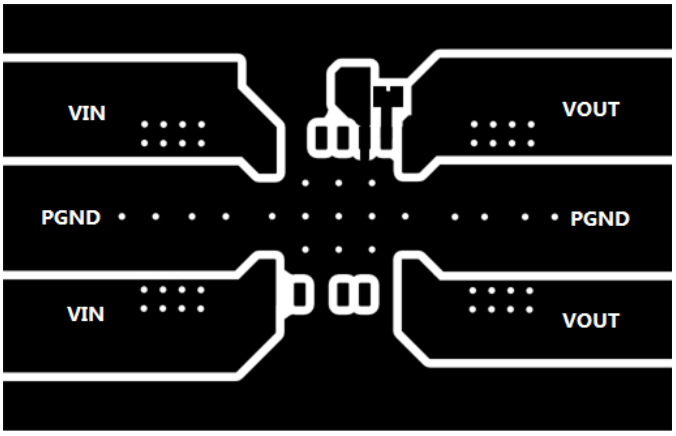

図 10-2. Typical Top-Layer

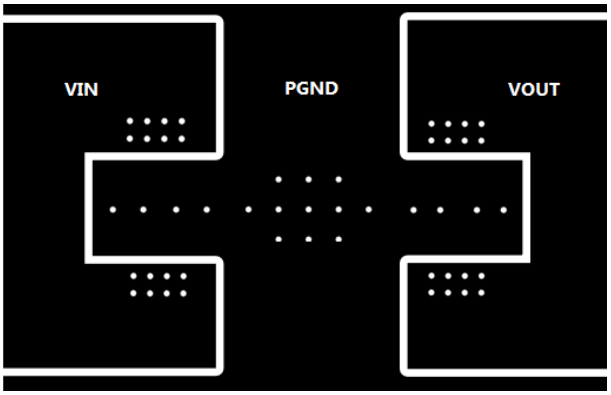

図 10-3. Typical Mid-Layer

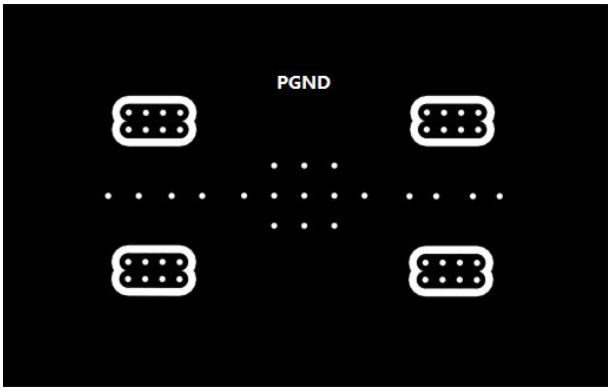

図 10-4. Typical PGND-Layer

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10.2.1 Theta JA Versus PCB Area

The amount of PCB copper as well as airflow effects the thermal performance of the device. 図 10-5 shows the effects of copper area and airflow on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the TPSM560R6. The junction-to-ambient thermal resistance versus PCB area is plotted for a 4-layer PCB.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in the *Typical Characteristics*.
2. Calculate the maximum θ_{JA} using 式 3 and the maximum ambient temperature of the application.

$$\theta_{JA} = \frac{(125^{\circ}C - T_{A(max)})}{P_{D(max)}} \ (^{\circ}C/W) \tag{3}$$

3. Reference 図 10-5 to determine the minimum required PCB area for the application conditions.

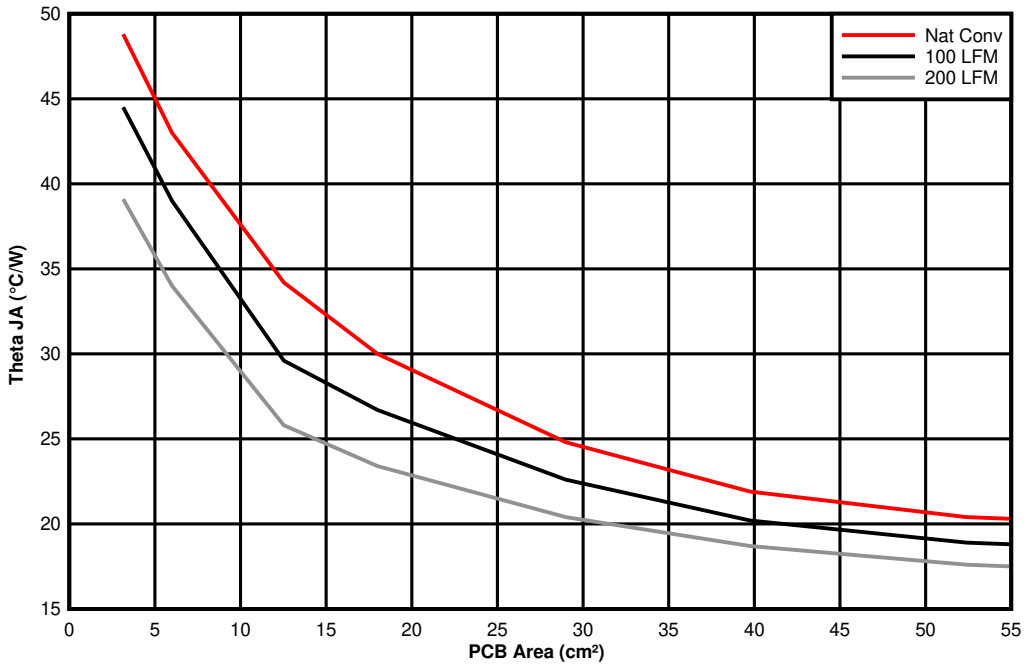

図 10-5. θ_{JA} vs PCB Area

10.2.2 Package Specifications

表 10-1. Package Specifications Table

TPSM560R6		VALUE	UNIT
Weight		429	mg
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	87.7	MHrs

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10.2.3 EMI

The TPSM560R6 is compliant with EN55011 radiated emissions. 図 10-6 through 図 10-9 show typical examples of radiated emission plots for the TPSM5601R5H (1.5-A, 1-MHz version). Expect similar results for the TPSM560R6. The graphs include the plots of the antenna in the horizontal and vertical positions.

10.2.3.1 EMI Plots

EMI plots were measured using the standard TPSM5601R5HEVM.

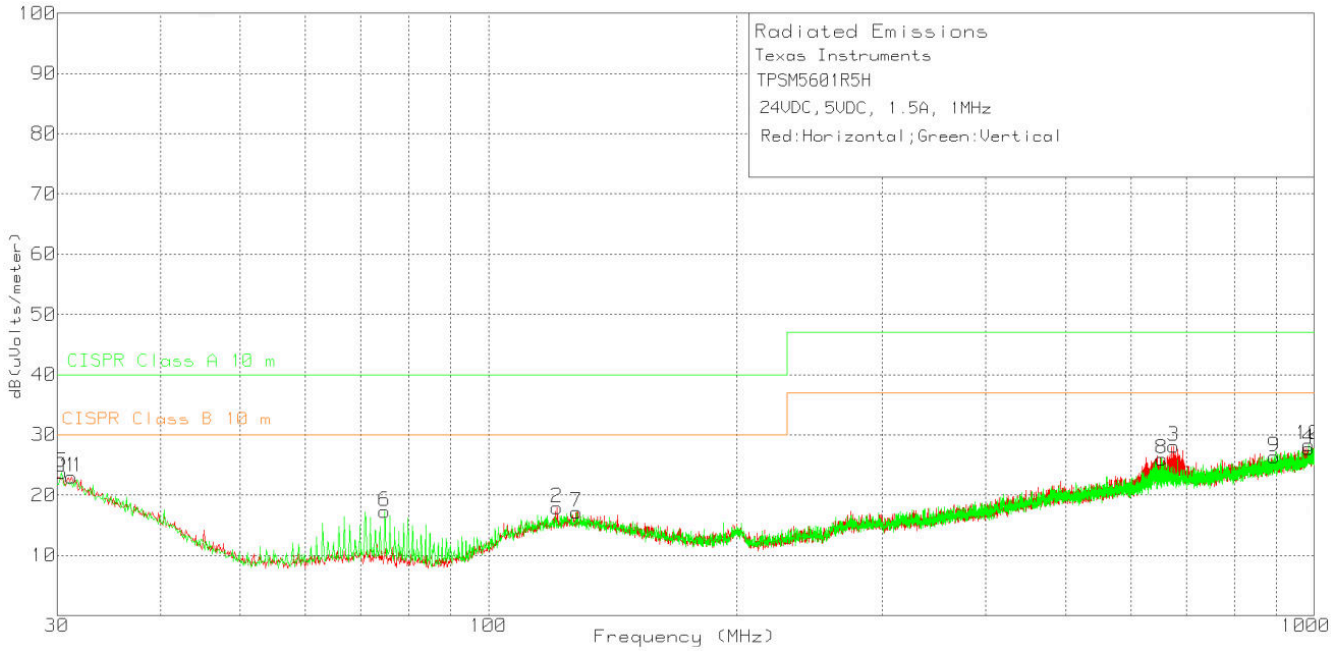

図 10-6. Radiated Emissions 24-V Input, 5-V Output, 1.5-A Load

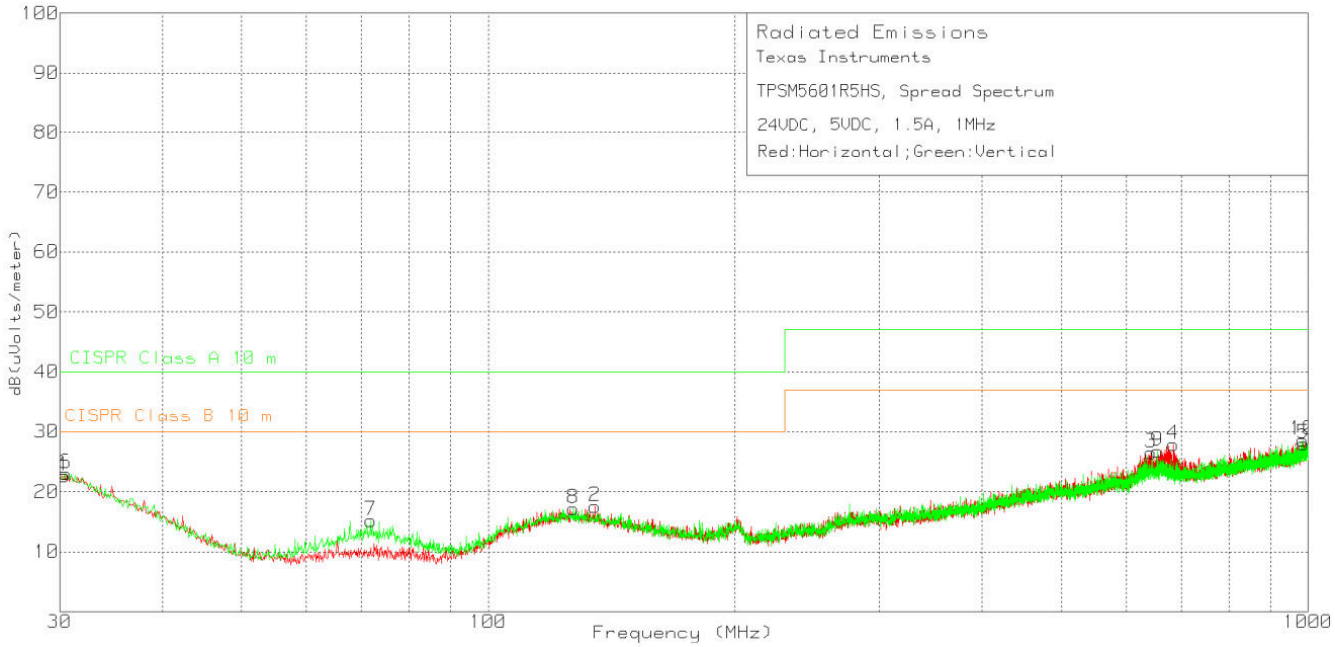

図 10-7. Radiated Emissions 24-V Input, 5-V Output, 1.5-A Load (Spread Spectrum)

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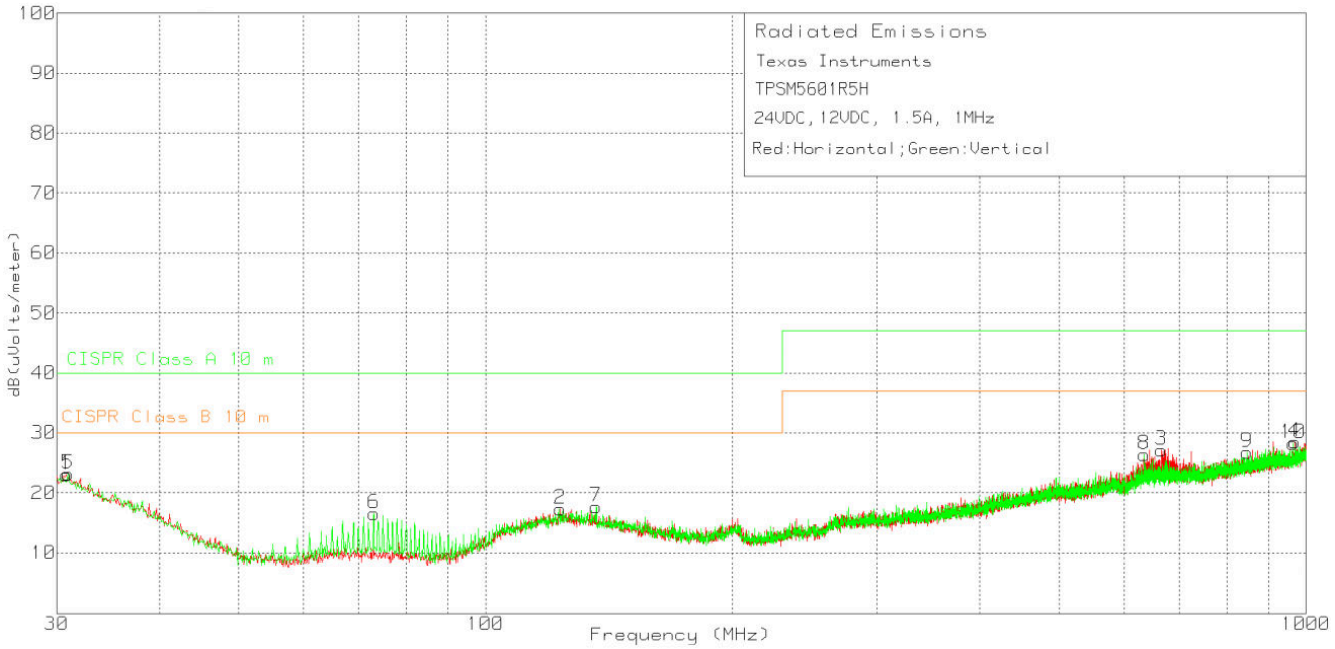

図 10-8. Radiated Emissions 24-V Input, 12-V Output, 1.5-A Load

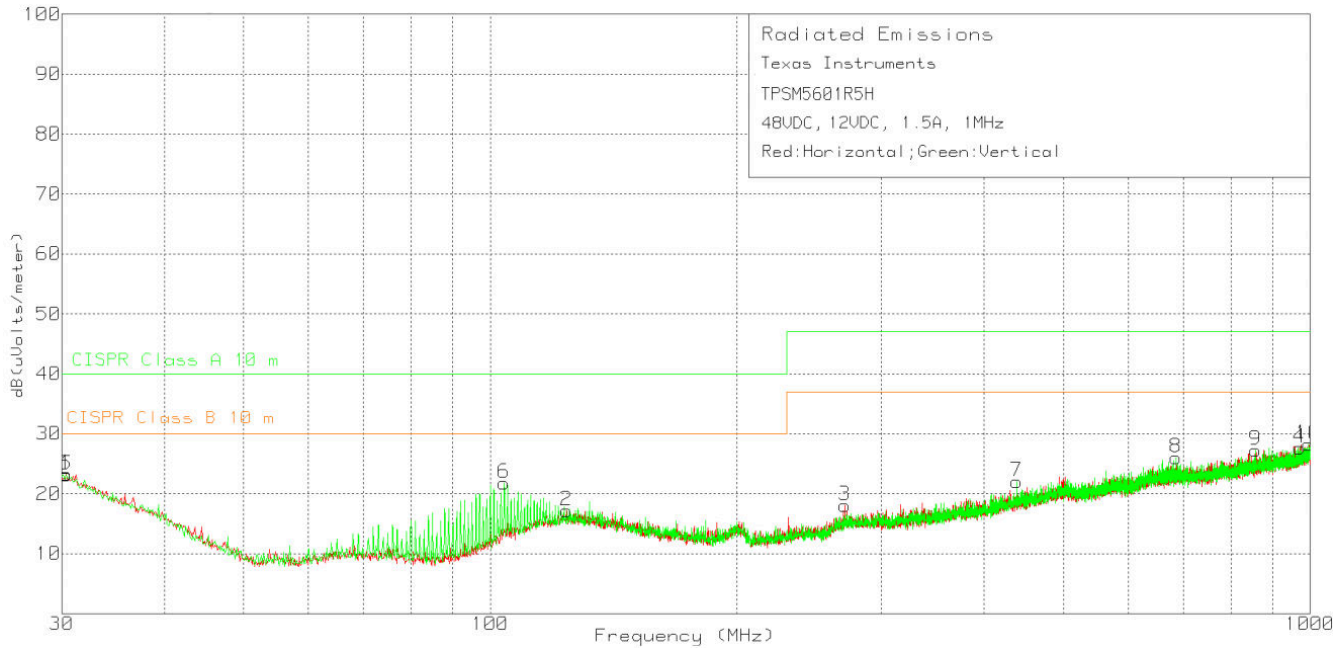

図 10-9. Radiated Emissions 48-V Input, 12-V Output, 1.5-A Load

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Designs.
- To view a related device of this product, see the TPSM5601R5Hx.

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM560R6 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPSM560R6EVM User's Guide*
- Texas Instruments, *Using the TPSM5601R5Hx in an Inverting Buck-Boost Topology Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM560R6RDAR	Active	Production	B3QFN (RDA) | 15	1000 | LARGE T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 125	560R6
TPSM560R6RDAR.A	Active	Production	B3QFN (RDA) | 15	1000 | LARGE T&R	Yes	NIPDAU	Level-3-245C-168 HR	-40 to 125	560R6

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

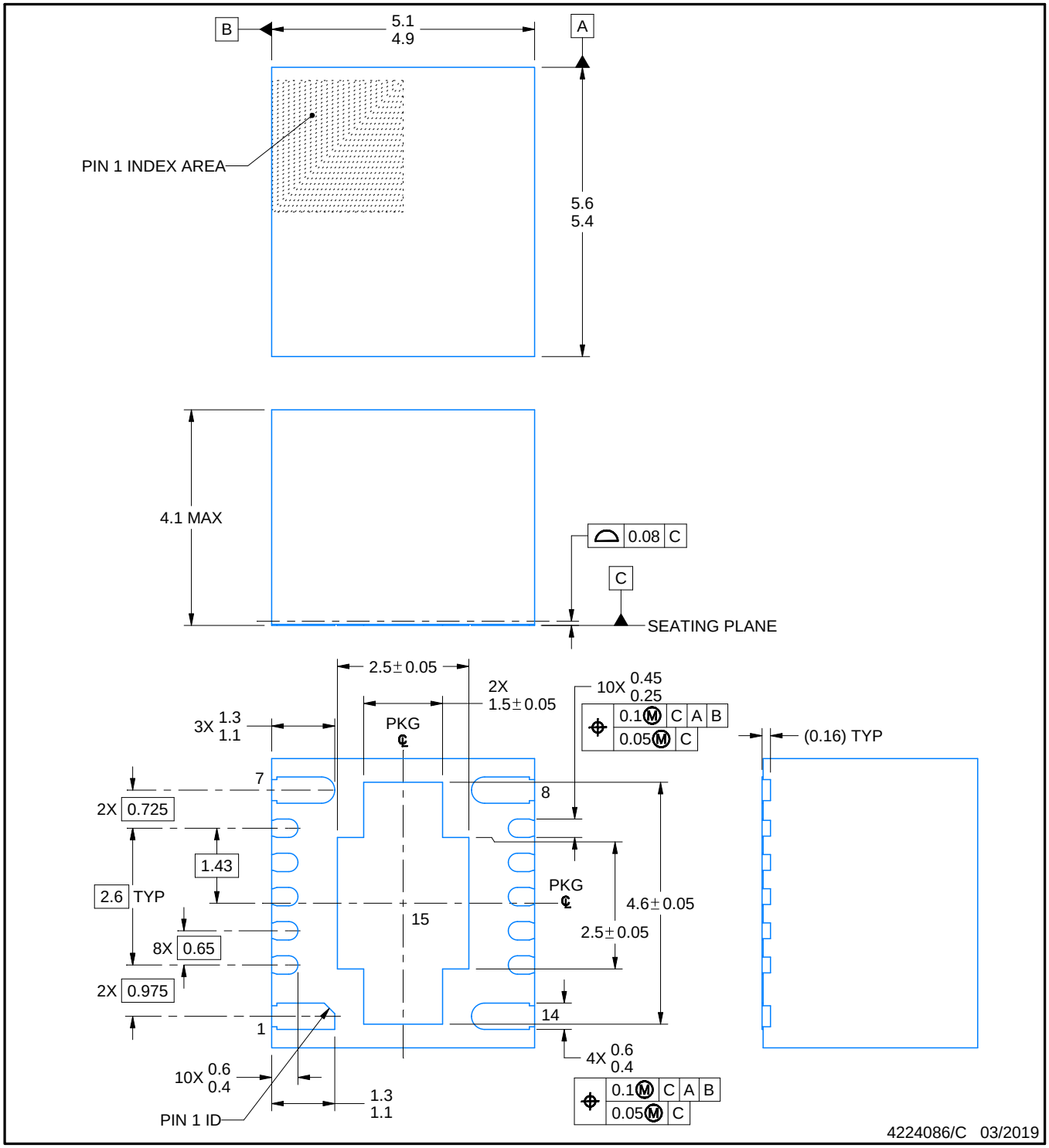
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RDA0015A

PACKAGE OUTLINE

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

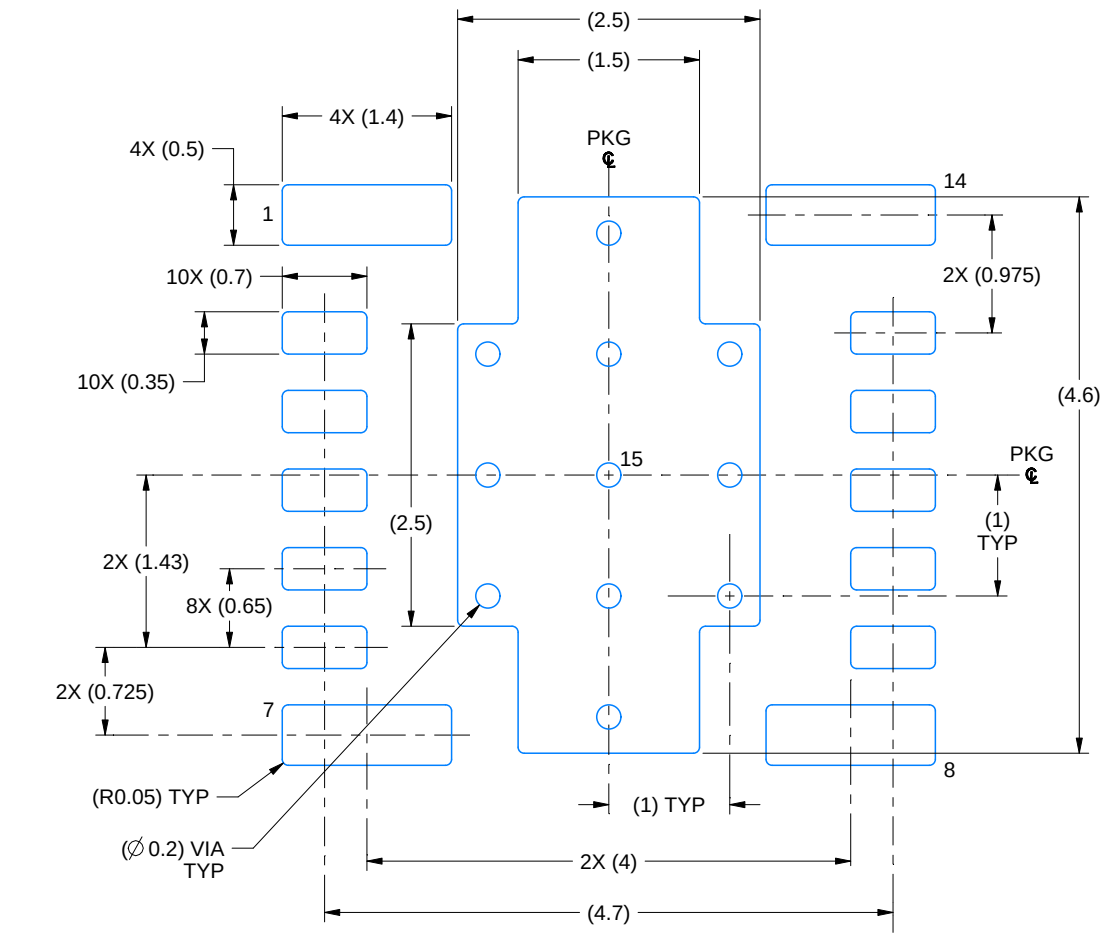
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RDA0015A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 16X



SOLDER MASK DETAILS

4224086/C 03/2019

NOTES: (continued)

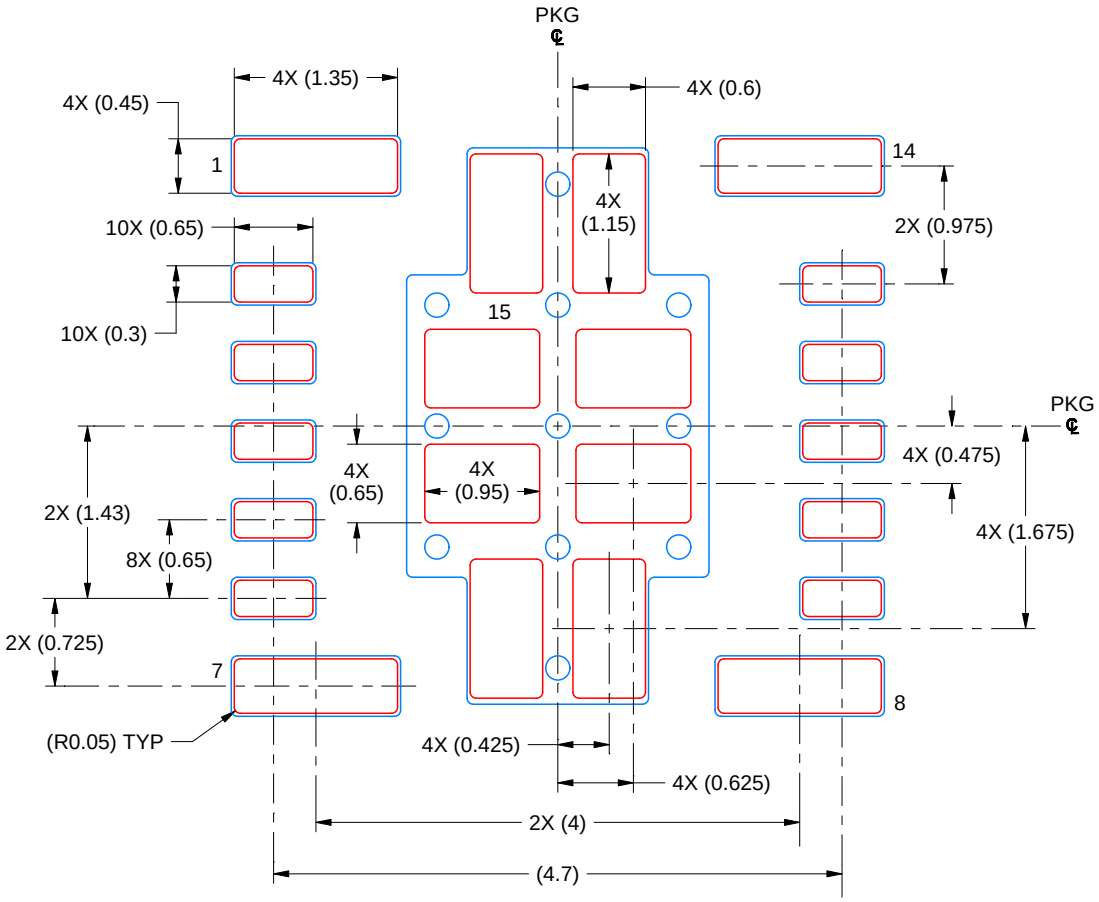
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RDA0015A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15:
56% PRINTED SOLDER COVERAGE BY AREA
SCALE: 16X

4224086/C 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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