TEXAS INSTRUMENTS
TPSM5D1806E
JAJSN49 – JANUARY 2022

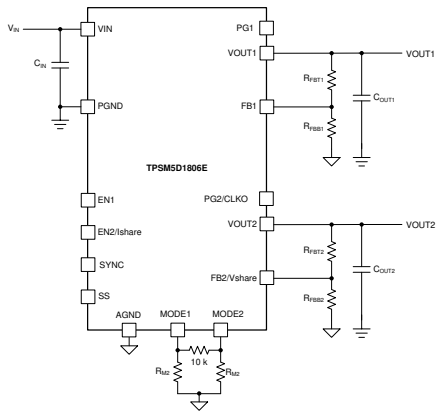
TPSM5D1806E –55℃～+125℃の範囲を持つ、4.5V～15V 入力、デュアル 6A / シングル 12A 出力のパワー・モジュール

1 特長

- 独立したデュアル 6A 出力
- パラレル構成のシングル 12A 出力
- 出力電圧範囲:0.5V～5.5V
- 全温度範囲にわたって、0.5V、±1.25% の基準電圧精度
- 位相遅延を使った周波数同期
- 出力ごとに独立したイネーブルとパワー・グッド
- プリバイアスされた出力へのスタートアップ
- UV および OV パワー・グッド
- 選択可能なスイッチング周波数オプション:500kHz、1.0MHz、1.5MHz、2.0MHz
- EN55011 放射 EMI の規制条件に準拠
- 動作時の接合部温度範囲:–55℃～+125℃
- 動作時の周囲温度範囲:–55℃～+105℃
- 8mm × 5.5mm × 1.8mm の標準 QFN パッケージ
- WEBENCH® Power Designer により、TPSM5D1806E を使用するカスタム設計を作成

2 アプリケーション

- 航空宇宙 / 防衛をサポート
- 医療用画像処理
- 高耐久性通信
- アビオニクスおよび航空機制御



デュアル出力の概略回路図

3 概要

TPSM5D1806E デュアル 6A 出力パワー・モジュールは、小型 (8mm × 5.5mm × 1.8mm) の QFN パッケージに封止された柔軟な高集積 DC-DC 電源です。4.5V～15V の入力電圧範囲は、標準的な 5V および 12V レールだけでなく幅広い中間バスからの変換を可能にします。2 つの 6A 出力は、2 つの独立した電源レールとして別々に構成することも、1 つの 2 相 12A 出力として結合することもできます。

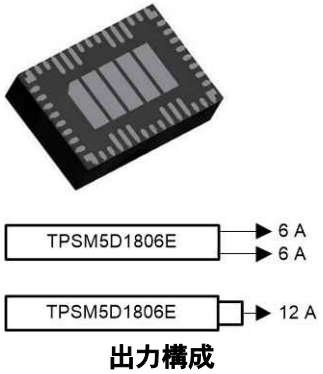
薄型 51 ピン QFN パッケージは、最適に配置することで高い熱性能を発揮します。–55℃に拡張された低温性能は、室外設置モジュールまたはフライト制御ユニットなどの環境の航空宇宙アプリケーションを可能にします。基板レイアウトを単純にし製造時の取り扱いを簡単にするため、本デバイスのすべての信号ピンは外周から接続できるように配置され、真下には大型サーマル・パッドが設けられています。

この統合型電源設計を使うと、ループ補償も磁気部品の選択も設計プロセスから取り除くことができます。本デバイスは、出力ごとに独立したイネーブル制御とパワー・グッド信号を備えています。スイッチング周波数と位相オフセットは、ピン・ストラップを使って設定できます。本デバイスは、過電流およびサーマル・シャットダウン保護機能も備えています。

製品情報

デバイス番号	パッケージ(1)	本体サイズ (公称)
TPSM5D1806E	QFN	8mm × 5.5mm × 1.8mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



出力構成

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2022	*	Initial release

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5 Pin Configuration and Functions

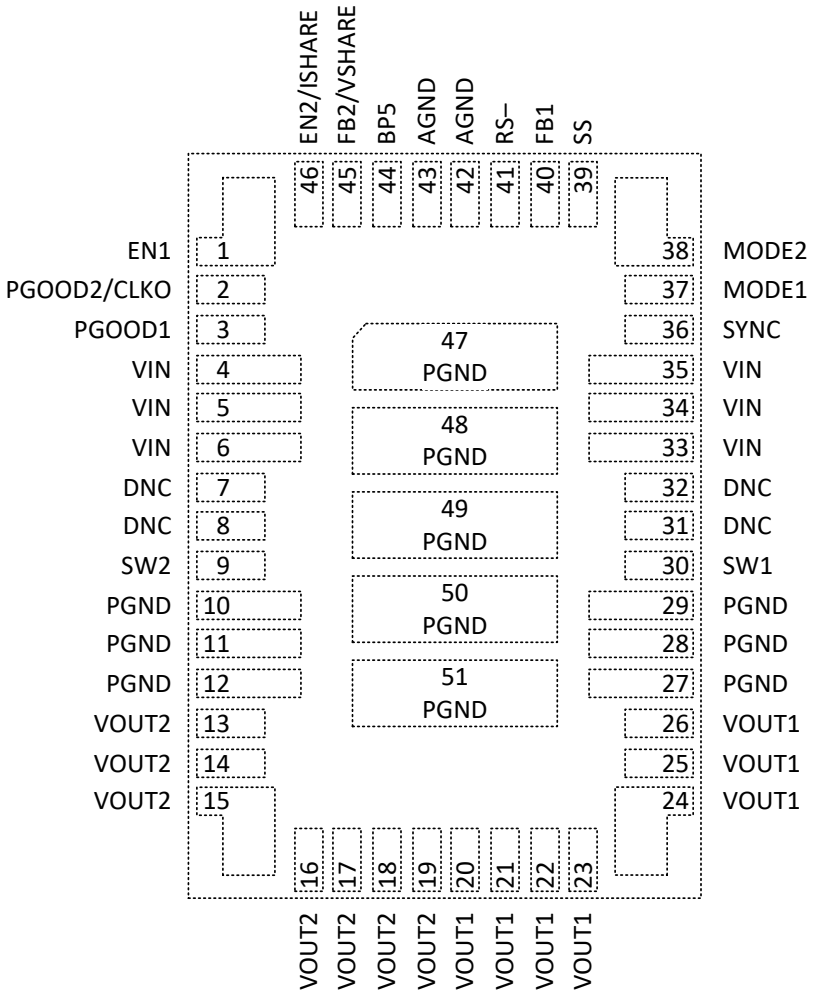


図 5-1. 51-Pin RDB QFN Package (Top View)

表 5-1. Pin Functions

Pin		Type[1]	Description
Name	No.		
AGND	42, 43	G	Analog ground for the internal analog control circuit. Connect to PGND at one single point, away from noisy circuitry.
BP5	44	O	Output of the internal 5-V regulator. Bypass this pin with a minimum of 1.5 µF of effective capacitance to AGND. Can be used as a pullup voltage for PGOOD signals.
DNC	7, 8, 31, 32	—	Do not connect. Do not connect these pins to AGND, PGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
EN1	1	I	Channel 1 enable input. Float or pull high to enable. Can also be used to externally adjust EN UVLO by connecting a resistor divider between VIN and AGND.
EN2/ISHARE	46	I/O	*Multi-function pin* Dual output configuration: Channel 2 enable input. Float or pull high to enable. Can also be used to externally adjust EN UVLO by connecting resistor divider between VIN and AGND. Parallel output configuration: Current balance node of the internal regulators. Leave this pin open.
FB1	40	I	Channel 1 feedback input. Connect to the output voltage of channel 1 with a resistor divider.

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表 5-1. Pin Functions (continued)

Pin		Type[1]	Description
Name	No.		
FB2/VSHARE	45	I/O	*Multi-function pin* Dual output configuration: Channel 2 Feedback input. Connect to the output voltage of channel 2 with a resistor divider. Parallel output configuration: The COMP voltage of the internal regulators. Leave this pin open.
MODE1	37	I	Mode setting pin. Programs channel configuration as either dual or parallel outputs and programs channel interleaving using a resistor between the MODE1 pin and AGND. A 10-kΩ resistor is required between the MODE1 pin and MODE2 pin.
MODE2	38	I	Mode setting pin. Select from four pre-set switching frequencies using a resistor between the MODE2 pin and AGND. A 10-kΩ resistor is required between MODE1 pin and MODE2 pin.
PGND	10–12, 27–29, 47–51	G	Power ground of the device. This is the return current path for the power stage of the device. Connect these pins to the bypass capacitors associated with VIN and VOUT. Connect pads 47, 48, 49, 50, and 51 to the PCB ground planes using multiple vias for optimal thermal performance. All pins must be connected together externally with a copper plane or pour directly under the device.
PGOOD1	3	O	Channel 1 power-good indicator output. This pin is an open-drain output, which asserts low during any fault condition. When used, a pullup resistor to BP5 or other external supply is required. Leave this pin open if unused.
PGOOD2/CLKO	2	O	*Multi-function pin* Dual output configuration: Channel 2 power-good indicator output. This pin is an open-drain output, which asserts low during any fault condition. When used, a pullup resistor to BP5 or another external supply is required. Leave this pin open if unused. Parallel output configuration: 180° clock output. Leave this pin open if unused.
RS–	41	G	For parallel output applications, this pin functions as remote sense negative input to the differential amplifier. Connect this pin to the point of ground regulation using a kelvin trace. For dual output configurations, this pin must be tied to AGND.
SS	39	I	External soft start when configured for parallel output operation. Place a capacitor from SS to AGND to set output voltage rise time. For independent dual channel configurations, leave this pin open.
SW1	30	O	Channel 1 power stage switch node. Can be used to monitor the switch node.
SW2	9	O	Channel 2 power stage switch node. Can be used to monitor the switch node.
SYNC	36	I	This pin synchronizes to external clock or the CLKO pin of another device.
VIN	4–6, 33–35	I	Power conversion input pins. Pins 4, 5, and 6 are not internally connected to pins 33, 34, and 35. Connection must be made using the PCB VIN plane. Bypass VIN pins with ceramic capacitance to PGND, close to the device.
VOUT1	20–26	O	Channel 1 output voltage. These pins are connected to the internal output inductor. Connect to the output load. Place external bypass capacitors between these pins and PGND.
VOUT2	13–19	O	Channel 2 output voltage. These pins are connected to the internal output inductor. Connect to the output load. Place external bypass capacitors between these pins and PGND.

(1) G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	16	V
	BP5, EN1, EN2/ISHARE, FB1, FB2/VSHARE, MODE1, MODE2, PGOOD1, PGOOD2/CLKO, SS, SYNC	–0.3	6	
	RS–, PGND to AGND	–0.3	0.3	
Output voltage	VOUT1, VOUT2	–0.3	6	V
	SW1, SW2	–0.3	16	
	SW1, SW2 transient (10ns)	–3	18	
T_J	Operating IC junction temperature	–55	125	°C
T_{stg}	Storage temperature	–55	125	°C
	Peak reflow case temperature		260	°C
	Maximum number or reflows allowed		3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5(2)		15	V
V_{OUT}	Output voltage	0.5		5.5	V
I_{OUT}	Output current per channel, continuous			6	A
V_{EN}	EN voltage	0		5.5	V
V_{PGOOD}	PGOOD pull-up voltage			5.5	V
T_A	Operating ambient temperature	–55		125	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the *Electrical Characteristics* table.
(2) See the *Minimum Input Voltage* section for the recommended minimum input voltage at higher output voltages.

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6.4 Thermal Information

THERMAL METRIC(1)		TPSM5D1806 RDB (QFN) 51 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	13.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (3)	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (4)	9.4	°C/W
T_{SHDN}	Thermal Shutdown Temperature	165	°C
T_{SHDN}	Thermal Shutdown Hysteresis	20	°C

(1) For more information about thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 100 mm × 100 mm, 6-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1 mm from the device.

6.5 Electrical Characteristics

Limits apply over T_A = –55°C to +125°C, V_{IN} = 12 V (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
V_{IN}	Operating input voltage range		4.5(1)		15	V
UVLO	V_{IN} turn on	V_{IN} increasing	3.5	3.7	3.9	V
	Hysteresis			200		mV
I_Q	Quiescent current	Non-switching, V_{FB1}, V_{FB2} > 0.5 V, T_A = 25°C, EN1 = EN2 = 5 V		4		mA
I_{SHDN}	Shutdown supply current	T_A = 25°C, EN1 = EN2 = 0 V		270		µA
INTERNAL LDO (BP5)						
BP5	Regulation voltage	6 V ≤ V_{IN} ≤ 15 V, I_{LOAD} = 70 mA	4.8	5.0	5.2	V
FEEDBACK						
$V_{(FB1)}$, $V_{(FB2)}$	Feedback voltage	T_J = 25°C		0.5		V
	Temperature accuracy	T_J = –55°C to 125°C	–1.25%		+1.25%	
	Load regulation	T_A = +25°C, over I_{OUT} range		0.2%		
	Line regulation	T_A = +25°C, I_{OUT} = 0 A, over V_{IN} range		0.1%		
OUTPUT CURRENT						
I_{OUT}	Output current	Per channel	0		6(2)	A
	Overcurrent threshold source current	DC current		6.6		A
	Overcurrent threshold sink current	DC current		-2.8		A
$I_{SH(acc)}$	Output current sharing accuracy	I_{OUT} ≥ 3 A per channel		15%		
		I_{OUT} < 3 A per channel		1		A
	OCP hiccup wait time	Wait time to attempt re-start		7		ms
	OCP hiccup entry time	Cycles before hiccup		16		cycles

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6.5 Electrical Characteristics (continued)

Limits apply over T_A = –55°C to +125°C, V_{IN} = 12 V (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
t_{SS}	Default soft-start time	Time from switching to PGOOD high without C_{SS}		1		ms
I_{SS}	Soft-start charge current	T_{SS} ≤ 50 ms, C_{SS} < 0.3 µF		2		µA
Rss	Soft-start discharge resistance			600		Ω
ENABLE (EN)						
V_{EN}	Enable threshold voltage	EN rising		1.2	1.3	V
		EN falling	1	1.1		V
	Hysteresis on Enable			100		mV
	Enable pullup current	EN floating		1.4		µA
	Enable to start switching time	VIN ≥ 4.5 V, toggle EN		0.3		ms
SWITCH NODE (SW)						
	SW1, SW2 Discharge FET			32		Ω
	SW1, SW2 minimum on time			40	50	ns
	SW1, SW2 minimum off time			150	200	ns
SWITCHING FREQUENCY						
	Fsw1	MODE2 resistor = 10.7 kΩ	450	500	550	kHz
	Fsw2	MODE2 resistor = 17.4 kΩ	900	1000	1100	kHz
	Fsw3	MODE2 resistor = 28.7 kΩ	1350	1500	1650	kHz
	Fsw4	MODE2 resistor = 53.6 kΩ	1800	2000	2200	kHz
SYNCHRONIZATION (SYNC)						
$V_{IH(SYNC)}$	High-level input		2			V
$V_{IL(sync)}$	Low-level input				0.6	V
	Input duty cycle		20%		80%	
	Sync frequency versus internal oscillator setting		-20%		+20%	
CLOCK OUTPUT (CLKO)						
$V_{OH(CLKO)}$	High-level output	I_O = 20 µA	2.2			V
$V_{OL(CLKO)}$	Low-level output	I_O = 20 µA			0.4	V
	Pulse width output			80		ns
POWER GOOD WARNING (PGOOD1, PGOOD2)						
PGOOD	PGOOD thresholds	V_{FB1}, V_{FB2} falling (warning)	87%	90%	93%	
		V_{FB1}, V_{FB2} rising (good)	90%	93%	96%	
		V_{FB1}, V_{FB2} falling (good)	104%	107%	110%	
		V_{FB1}, V_{FB2} rising (warning)	107%	110%	113%	
	PGOOD leakage current	V_{PGOOD} = 5.5 V			1	µA
	PGOOD output low voltage	BP5 = 5 V, I_{PGOOD} = 6mA			0.5	V
	Minimum VIN for asserted output	V_{PGOOD} ≤ 0.5 V, I_{PGOOD} = 1 mA			1.5	V
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE FAULT PROTECTION						
	OV fault threshold	V_{FB1}, V_{FB2} rising (fault)		120%		
	UV fault threshold	V_{FB1}, V_{FB2} falling (fault)		80%		

(1) See the *Minimum and Maximum Input Voltage* section for the recommended minimum input voltage at higher output voltages.
(2) See Safe Operating Area plots in the *Typical Characteristics* sections of the data sheet.

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6.6 Typical Characteristics (V_{IN} = 12 V)

T_A = 25°C, unless otherwise noted

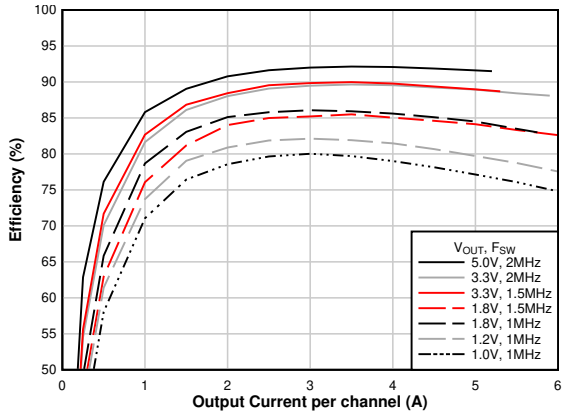


図 6-1. Efficiency vs Output Current

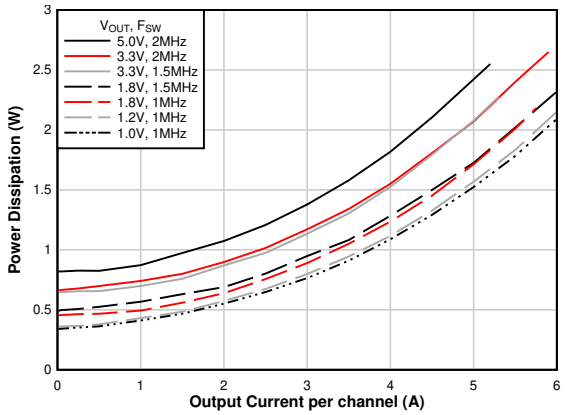
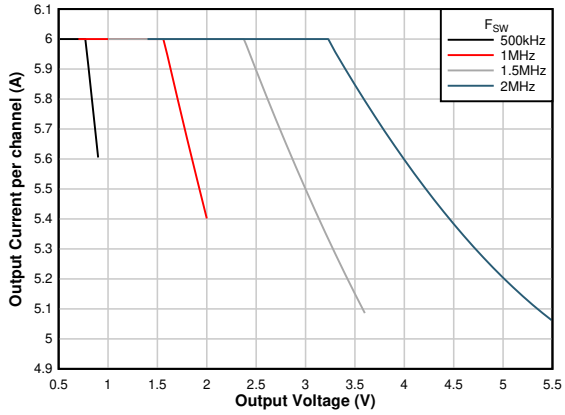
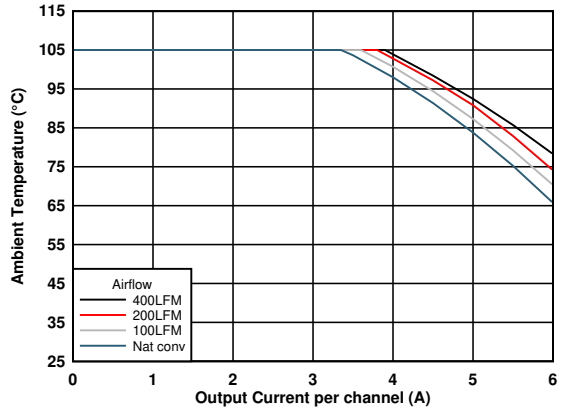


図 6-2. Power Dissipation vs Output Current



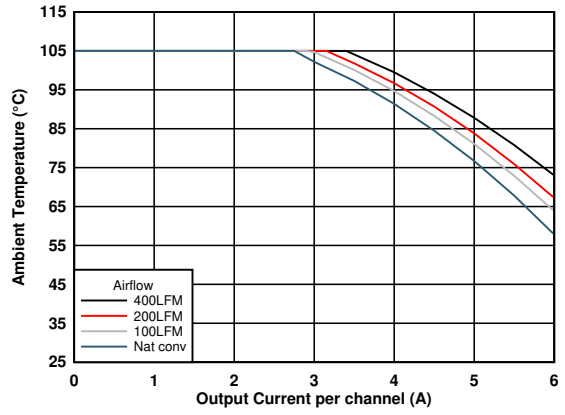
Refer to 表 7-1

図 6-3. Maximum Output Current



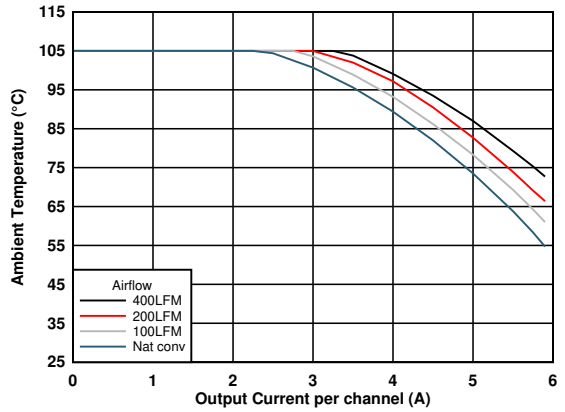
F_{sw} = 1.0 MHz Dual 1.2-V outputs $I_{OUT1} = I_{OUT2}$

図 6-4. Safe Operating Area (V_{OUT} = 1.2 V)



F_{sw} = 1.5 MHz Dual 1.8-V outputs $I_{OUT1} = I_{OUT2}$

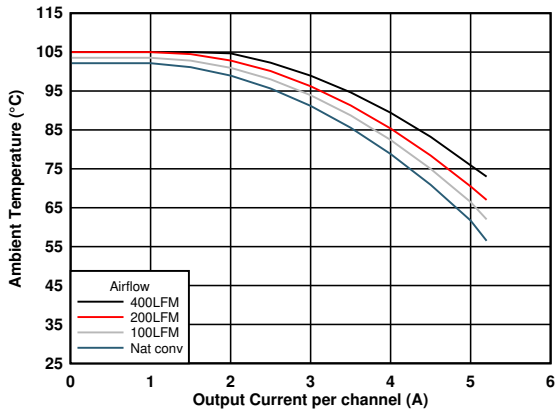
図 6-5. Safe Operating Area (V_{OUT} = 1.8 V)



F_{sw} = 2.0 MHz Dual 3.3-V outputs $I_{OUT1} = I_{OUT2}$

図 6-6. Safe Operating Area (V_{OUT} = 3.3 V)

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F_{sw} = 2.0 MHz　　Dual 5-V outputs　　$I_{OUT1} = I_{OUT2}$

図 6-7. Safe Operating Area (V_{OUT} = 5 V)

6.7 Typical Characteristics (V_{IN} = 5 V)

T_A = 25°C unless otherwise noted

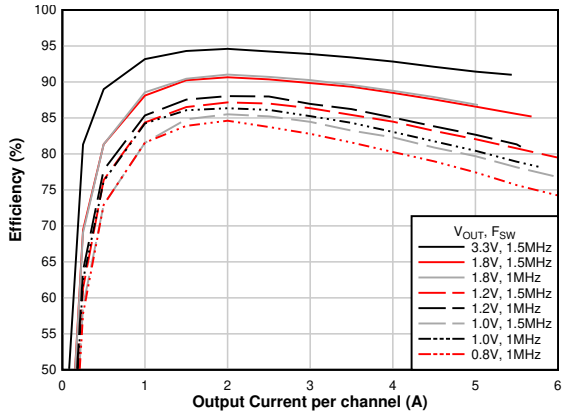


図 6-8. Efficiency vs Output Current

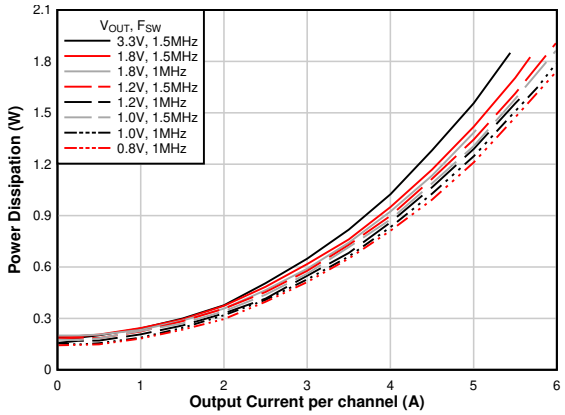
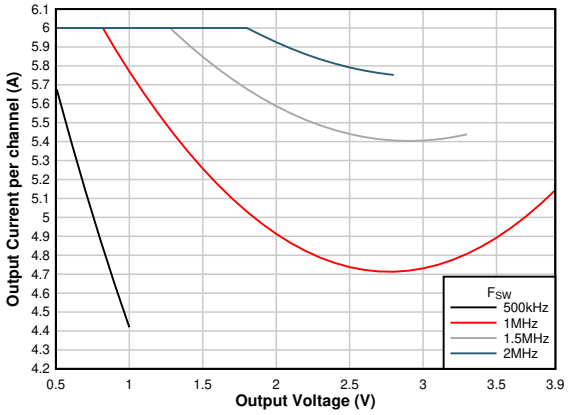
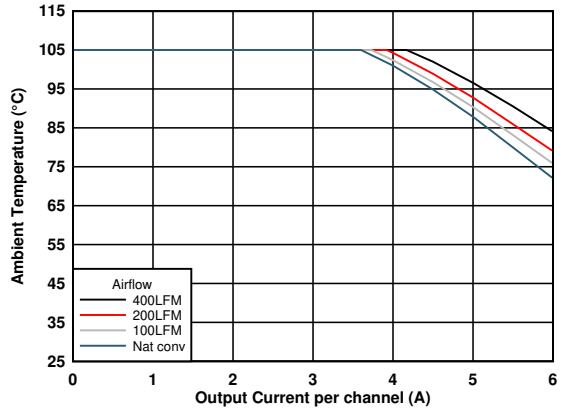


図 6-9. Power Dissipation vs Output Current



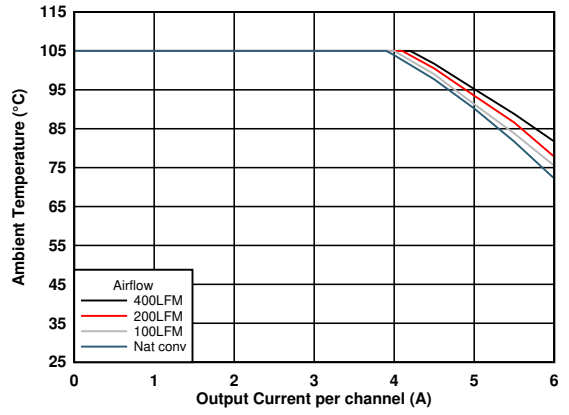
Refer to 表 7-1

図 6-10. Maximum Output Current



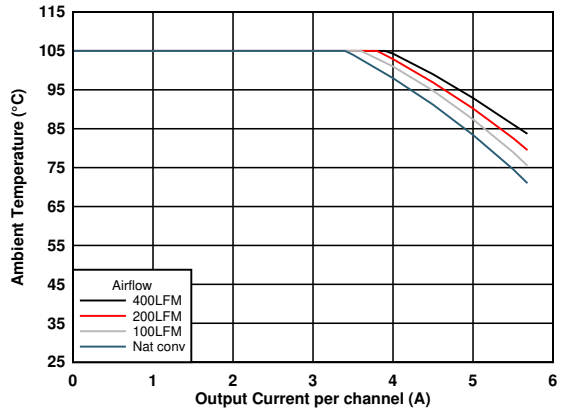
F_{sw} = 1.0 MHz Dual 0.8-V outputs $I_{OUT1} = I_{OUT2}$

図 6-11. Safe Operating Area (V_{OUT} = 0.8 V)



F_{sw} = 1.5 MHz Dual 1.2-V outputs $I_{OUT1} = I_{OUT2}$

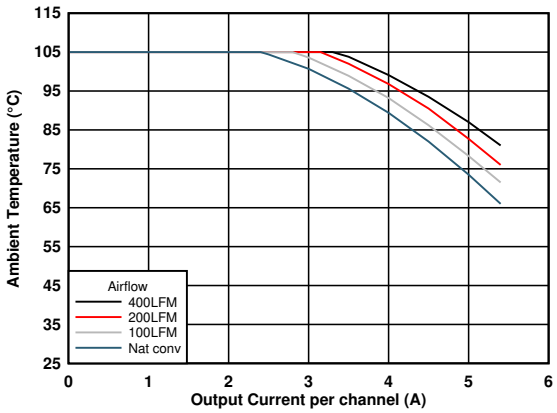
図 6-12. Safe Operating Area (V_{OUT} = 1.2 V)



F_{sw} = 1.5 MHz Dual 1.8-V outputs $I_{OUT1} = I_{OUT2}$

図 6-13. Safe Operating Area (V_{OUT} = 1.8 V)

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F_{sw} = 2.0 MHz Dual 3.3-V outputs $I_{OUT1} = I_{OUT2}$

図 6-14. Safe Operating Area (V_{OUT} = 3.3 V)

7 Detailed Description

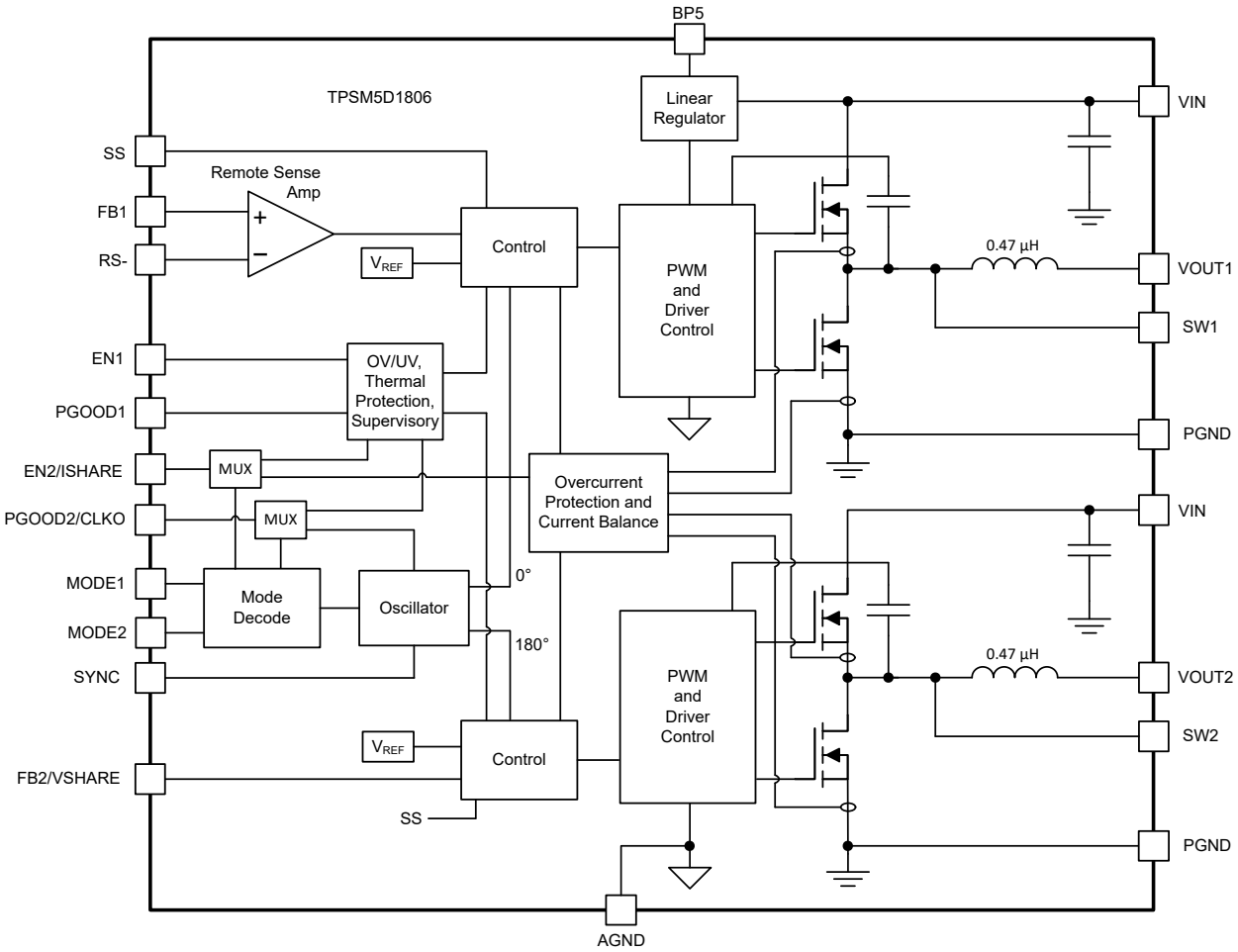
7.1 Overview

The TPSM5D1806E device is a dual output, step-down DC-DC power module with 4.5-V to 15-V input voltage range. Each device has two output channels and is capable of delivering up to 6-A of load current per channel. The device features exceptional efficiency and thermal performance in a very small solution size. The device is configurable as two independent 6-A outputs or a single 2-phase output to deliver up to 12 A. The TPSM5D1806E uses a fixed frequency, proprietary advanced current mode control architecture. The device operates in forced PWM (FPWM) operation to maintain constant switching frequency over the load range. The device is internally compensated, which reduces design time and requires fewer external components. The switching frequency and the phase operation are configured using pin strapping. The MODE1 pin sets the phase operation. 表 7-4 shows the resistor values that are required to set the phase operation and the correct phase offset. The switching frequency can be selected from pre-set values of 500 kHz, 1.0 MHz, 1.5 MHz, and 2.0 MHz through pin-strapping on the MODE2 pin. The TPSM5D1806E is also capable of synchronization to an external clock. The four switching frequency options allow the device to meet a wide range of design requirements. The module also features the following:

- Power-good (PGOOD) flag for each channel
- Precision enable for each channel
- Internal or adjustable soft-start rate
- Start-up into pre-bias voltage

The device has a pinout designed for simple, optimum PCB layout, low EMI, and excellent thermal performance.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjustable Output Voltage

When operating the TPSM5D1806E as a dual output device, the two output voltages (VOUT1 and VOUT2) are set using resistor dividers between the output voltages and AGND with the mid-point of the resistor divider connecting to the corresponding feedback pin (FB1 and FB2). See 図 7-4.

Select a bottom feedback resistor of 10 kΩ and calculate the value for the top feedback resistor (R_{FBT}) using the following equation. Use divider resistors with 1% tolerance or better and with a temperature coefficient of 100 ppm or lower.

$$R_{FBT} = 20 \times \left(V_{OUT} - 0.5 \right) (k\Omega) \quad (1)$$

When connecting the two outputs of the TPSM5D1806E for current sharing, the output voltage is set using only a single feedback divider connected to FB1. The FB pin of the second channel, FB2, must be left floating as shown in 図 7-2. Use 式 1 to calculate the R_{FBT}.

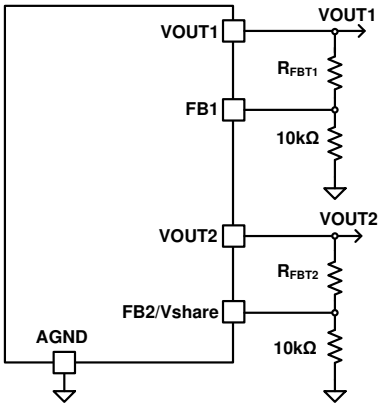


図 7-1. Single Device, Dual Output

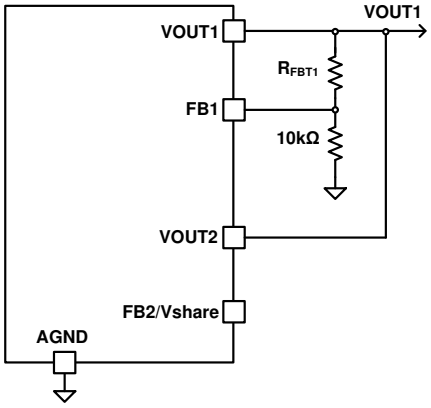


図 7-2. Single Device, Current Sharing

7.3.2 Frequency Selection

The TPSM5D1806E can be set to one of four switching frequencies:

- 500 kHz
- 1.0 MHz
- 1.5 MHz
- 2.0 MHz

The switching frequency is set using the MODE2 pin on the device. When setting the switching frequency, both channels of the device are set to the same frequency. Not all input voltage and output voltage combinations can operate at all switching frequencies. Check 表 7-1 for allowable switching frequencies. Select the appropriate resistor from 表 7-5 to set the switching frequency.

7.3.2.1 Synchronization

The TPSM5D1806E can also be synchronized to an external clock that is within ±20% of the switching frequency set by the MODE2 pin. The external clock signal can be applied to the SYNC pin before or after powering up. When the device is synchronized to an external clock signal, if the clock signal is removed, the device transitions to an intermediate frequency, which is 75% of the programmed frequency for approximately eight clock cycles. After eight clock cycles, the device transitions to the switching frequency set by the MODE2 pin.

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7.3.2.2 Allowable Switching Frequency

The TPSM5D1806E can be operated over a wide input voltage range with a wide output voltage setting range and at four selectable switching frequencies. However, not all input voltage, output voltage, and switching frequency combinations can be achieved due to timing and current limitations.

When setting the switching frequency, both channels of the device are set to the same frequency. When operating in dual output configuration, make sure that both channels can be operated at the desired switching frequency by referencing 表 7-1.

表 7-1. Allowable Switching Frequency

Output Current per Channel	Switching Frequency (kHz)	V_{IN} = 5 V		V_{IN} = 12 V	
		V_{OUT} Range		V_{OUT} Range	
		Min	Max	Min	Max
6 A	500	—	—	0.5	0.8
	1000	0.5	0.8	0.7	1.6
	1500	0.5	1.3	1.0	2.4
	2000	0.6	1.8	1.4	3.2
5 A	500	0.5	0.8	0.5	0.9
	1000	0.5	1.8	0.7	2.0
	1500	0.5	3.3	1.0	3.6
	2000	0.6	2.8	1.4	5.5
≤ 4 A	500	0.5	0.9	0.5	0.9
	1000	0.5	3.9	0.7	2.0
	1500	0.5	3.5	1.0	3.6
	2000	0.6	2.8	1.4	5.5

7.3.3 Minimum and Maximum Input Voltage

The minimum input voltage of the TPSM5D1806E is 4.5 V, however, the minimum recommended input voltage increases at higher output voltages. Refer to 表 7-2 to determine the minimum recommended input voltage for each switching frequency. Also reference 表 7-1 to ensure that the output voltage can be operated at the selected switching frequency. Control the turn ON and turn OFF of the device at an input voltage greater than the minimum using a resistor divider on the EN1 (EN2) pin between VIN and AGND (see セクション 7.3.10).

表 7-2. Minimum Input Voltage

Switching Frequency (kHz)	Minimum Input Voltage
500	4.5 V
1000	4.5 V or VOUT × 1.3 (whichever is greater)
1500	4.5 V or VOUT × 1.6 (whichever is greater)
2000	4.5 V or VOUT × 1.75 (whichever is greater)

Additionally, the maximum input voltage of the TPSM5D1806E is 15 V, however, the maximum recommended input voltage decreases at lower output voltages and higher switching frequencies. See 図 7-3 for the maximum recommended input voltage for each of the allowable switching frequencies across the output voltage range.

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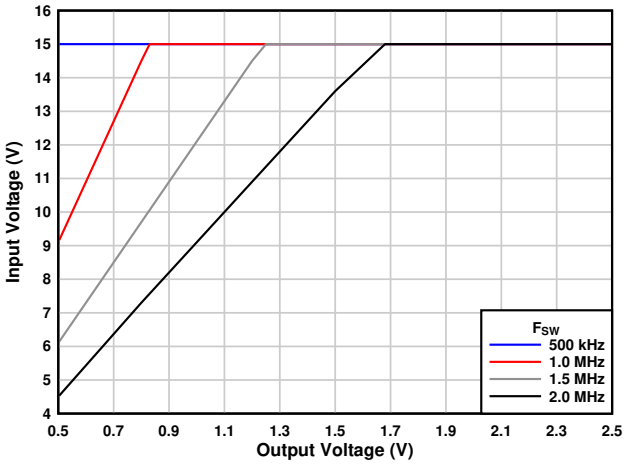


図 7-3. Maximum Input Voltage

7.3.4 Recommended Settings

表 7-3 lists the recommended operating settings for several common output voltages. The table takes into account the minimum and maximum input voltage limits along with timing and current limitations. The table also lists the minimum required effective output capacitance for each output voltage. Also included in this table is the minimum required input voltage and required enable divider resistors to ensure safe turn ON at the minimum input voltage.

Refer to 表 7-1 for the allowable switching frequency. The recommended switching frequency typically results in the highest efficiency. When operating at a switching frequency other than the recommended, consult セクション 7.3.3 for the minimum and maximum allowable input voltage.

When setting the switching frequency, both channels of the device are set to the same frequency. When operating in dual output configuration, make sure that both channels can be operated at the desired switching frequency by referencing.

表 7-3. Recommended Settings

Output Voltage (V)	Top Feedback Resistor R_{FBT} (1) (kΩ)	F_{SW} (kHz)	MODE2 Resistor (kΩ)	Minimum C_{OUT} (2) (µF)	Minimum Input Voltage (V)	Bottom Enable Resistor R_{ENB} (3) (kΩ)
0.5	open	500	10.7	400	4.5	— (4)
0.8	6.04	500	10.7	280	4.5	—
0.9	8.06	1000	17.4	265	4.5	—
1.0	10.0	1000	17.4	250	4.5	—
1.1	12.1	1000	17.4	235	4.5	—
1.2	14.0	1000	17.4	220	4.5	—
1.5	20.0	1000	17.4	180	4.5	—
1.8	26.1	1000	17.4	140	4.5	—
2.5	40.2	1500	28.7	100	4.5	—
3.0	49.9	1500	28.7	85	4.8	29.4
3.3	56.2	1500	28.7	75	5.3	26.1
4.0	69.8	2000	53.6	65	7.1	18.2
4.5	80.6	2000	53.6	60	7.9	16.2
5.0	90.9	2000	53.6	50	8.8	14.3

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表 7-3. Recommended Settings (continued)

Output Voltage (V)	Top Feedback Resistor R_{FBT} (1) (kΩ)	F_{SW} (kHz)	MODE2 Resistor (kΩ)	Minimum C_{OUT} (2) (µF)	Minimum Input Voltage (V)	Bottom Enable Resistor R_{ENB} (3) (kΩ)
5.5	100	2000	53.6	45	9.6	13.0

(1) R_{FBB} = 10 kΩ
(2) Minimum C_{OUT} listed is the effective value, taking into account the effects of DC bias and temperature variation.
(3) R_{ENT} = 100 kΩ
(4) "—" means not required.

7.3.5 Device Mode Configuration

The TPSM5D1806E provides a wide range of configurations through pin strapping of two pins: MODE1 and MODE2. These pins are used to configure the device outputs, set the phase offset, and set the switching frequency. The operating mode of the device can be either two independent 6-A outputs or both outputs connected together in parallel for increased current up to 12 A. In either application, a 10-kΩ resistor is required from MODE1 to MODE2.

7.3.5.1 MODE1 (Operating Mode and Phase Position)

Place a 10-kΩ resistor from MODE1 to MODE2.

Place a resistor from MODE1 to AGND to set the device in the desired operating mode. The MODE1 resistor also selects the phase position for each channel. See 表 7-4 for MODE1 resistor values and the corresponding settings.

表 7-4. Operating Mode and Phase Position Settings

Operating Mode	Channel 1 Phase Position (°)	Channel 2 Phase Position (°)	Mode1 Resistor (kω)	Comments
Dual outputs	0	180	**15.4**	Sets phase position for both channels to 0° and 180°.
	90(1)	270(1)	**24.9**	Sets phase position for both channels to 90° and 270° from SYNC signal.
Paralleled outputs (2 phase)	0	180	**10.7**	Sets phase positions for both channels of the device.

(1) Requires synchronization to an external clock signal.

7.3.5.2 MODE2 (Setting the Switching Frequency)

Place a resistor from MODE2 to AGND to set the switching frequency of the device. See 表 7-5 for MODE2 resistor values and the corresponding settings. For dual-output applications, check 表 7-1 to make sure both outputs can operate at the selected switching frequency.

If synchronizing to an external clock, the TPSM5D1806E can only be synchronized to a frequency that is within ±20% of the switching frequency set by the MODE2 pin.

表 7-5. Switching Frequency Settings

Switching Frequency (kHz)	MODE2 Resistor (kΩ)
500	**10.7**
1000	**17.4**
1500	**28.7**
2000	**53.6**

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7.3.6 Input Capacitors

The TPSM5D1806E requires a minimum input capacitance of 88 µF (4 × 22 µF or 2 × 47 µF) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are required. Place input capacitors, as close as possible to both VIN sides of the device, between VIN and PGND as shown in 図 7-4. Applications with transient load requirements can benefit from adding additional bulk capacitance to the input as well.

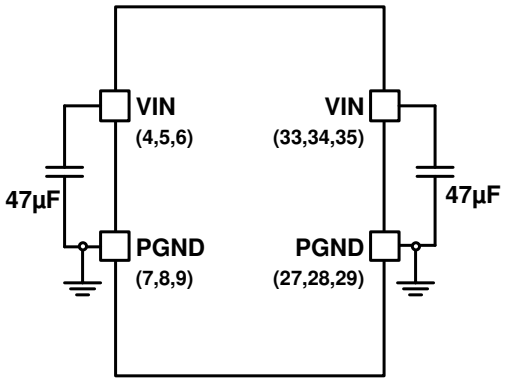


図 7-4. Input Capacitors Pin Connections

7.3.7 Minimum Required Output Capacitance

The TPSM5D1806E requires a minimum amount of ceramic output capacitance (per phase) depending on the output voltage setting. The amount of required output capacitance is shown in 図 7-5 and is the amount of *effective* capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contributes to differences between the standard rated value and the actual effective value of the capacitance. When adding additional capacitance above the minimum, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two.

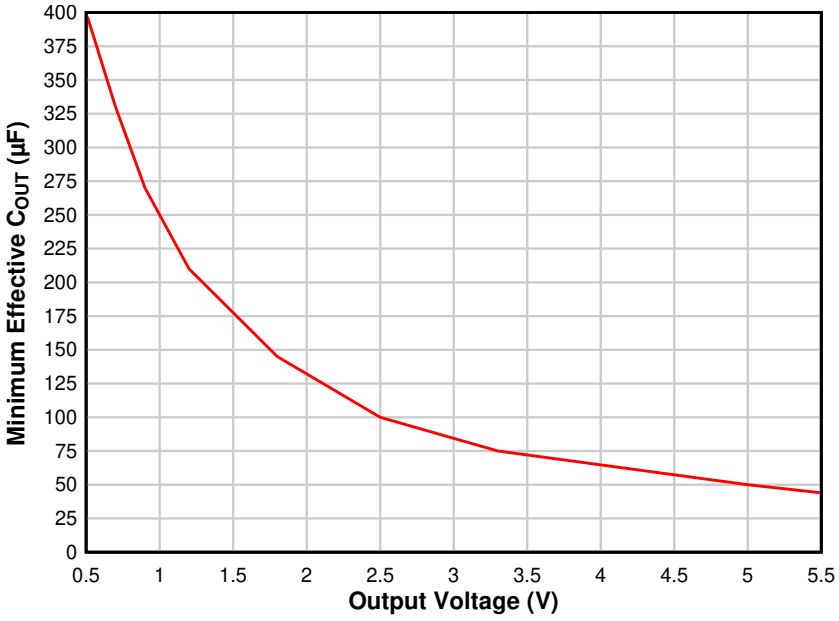


図 7-5. Minimum Required Output Capacitance (per Phase)

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7.3.8 Ambient Temperature Versus Total Power Dissipation

When operating the TPSM5D1806E in dual channel configuration with different output voltages, the maximum operating ambient temperature can be determined using the total power dissipation of both channels. Refer to the power dissipation curves, 図 6-2 and 図 6-9, to determine the power dissipation for each output. Sum the power dissipation of both outputs to calculate the total power dissipation. Refer to 図 7-6 to determine the maximum allowable operating ambient temperature for a given total power dissipation. Increasing the airflow allows operation at a higher ambient temperature.

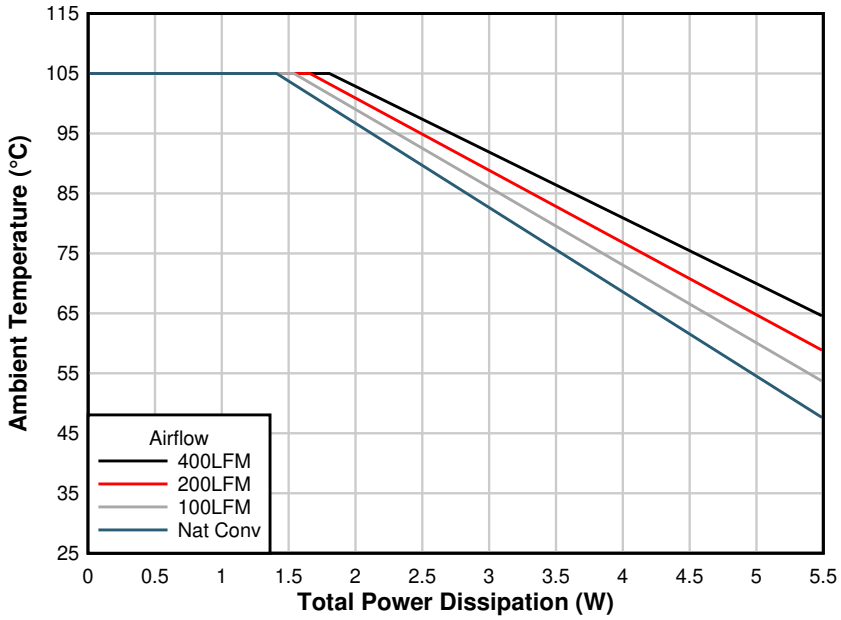


図 7-6. Ambient Temperature Versus Total Power Dissipation

7.3.9 Remote Sense

The TPSM5D1806E supports differential remote sense for accurate output regulation when operated in multi-phase configuration. In multi-phase configuration, FB1 and RS– pins are used for remote sensing. The FB1 pin must be connected to the mid-point of the resistor divider. Additionally, the RS– pin must be connected to the negative sensing point. The FB1 and RS– pins are extremely high-impedance input terminals of the true differential remote sense amplifier. The feedback resistor divider must use resistor values much less than 100 kΩ to reduce susceptibility to noise. A simple rule of thumb is to use a 10-kΩ lower divider resistor and then size the upper resistor to achieve the desired ratio.

When configured as a dual-output device, connect the RS– pin to AGND.

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7.3.10 Enable (EN) and Undervoltage Lockout (UVLO)

The precision enable feature of the TPSM6D1806E allows the voltage on the EN pin (V_{EN}) to control the ON/OFF functionality of the device. The EN pin has an internal pullup. Floating the EN pin allows the device to start up when a valid input voltage is applied. The TPSM5D1806 switching action and output regulation are enabled when V_{EN} is greater than 1.2 V (typical). While the device is switching, if the EN voltage falls below 1.1 V (typical), the device stops switching.

It is recommended to control the turn-on and turn-off of the device at a voltage greater than the minimum input voltage as shown in 表 7-2. An external UVLO control can be added using a resistor divider on the EN1 (EN2) pin, between VIN and AGND (see 図 7-7). Select a top enable resistor of 100 kΩ and calculate the value for the bottom enable resistor (R_{ENB}) using 式 2. It is recommended to use divider resistors with 1% tolerance or better and with temperature coefficient of 100 ppm or lower.

$$R_{ENB} = 110 \div \left(V_{IN} - 1.1 \right) (k\Omega) \quad (2)$$

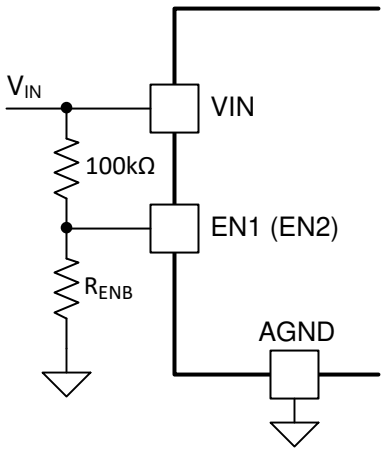


図 7-7. Adjustable UVLO Control

7.3.11 Soft Start

The TPSM5D1806E soft-start feature limits the inrush current from the input supply when the device is powered up. For dual-output configuration, the soft-start time is internally programmed to 1 ms. The soft-start pin must be left floating in dual-output configuration.

The external soft start is enabled when the device is configured in parallel-output operation. In parallel-output applications, if the SS pin is left open, the default soft-start time is also 1 ms. Applications that deliver high load current can have a large amount of capacitance at the output and can require longer soft-start time. The soft-start time for such applications can be extended by connecting an external capacitor, C_{SS}, from the soft-start pin to AGND. With external C_{SS}, the soft-start time is the longer of 1 ms or the programmed external soft-start time. An internal current source (I_{SS} = 2 µA) charges C_{SS} and generates a ramp from 0 V to V_{FB} (0.5 V) to control the ramp-up rate of the output voltage. The external soft-start time can be selected from 表 7-6 or calculated using 式 3.

$$t_{SS} = \frac{0.5 \times C_{SS}}{2\ \mu A} \quad (3)$$

表 7-6. C_{SS} Values and Soft-Start Times

C_{SS} (nF)	Open	6.2	8.2	10	12	20
t_{SS} (ms)	1	1.5	2	2.5	3	5

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The soft-start capacitor is discharged when VOUT is shut down by either fault protection or when V_{EN} is below the enable threshold.

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7.3.12 Power Good

The Power Good pins (PGOOD1, PGOOD2) are open-drain outputs that require a pullup resistor of 1 kΩ to 100 kΩ to a voltage source of 5.5 V or less to indicate the output voltage is within the PGOOD range. The BP5 output can be used as the pullup voltage source. The PGOOD detection is activated after soft start is completed. When the output voltage is within a range of ±10% of the target, the PGOOD goes high after a 50-µs internal delay. During operation, if the output voltage falls outside of ±10% of target voltage, PGOOD is pulled low after a 10-µs delay. The PGOOD feature is active while the voltage at the VIN pin is either equal to or greater than 1.5 V.

7.3.13 Safe Start-Up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output.

7.3.14 BP5

The BP5 pin is the output of an internal 5-V regulator. Bypass this pin with a minimum of 1.5 µF of effective capacitance to AGND. Place the capacitor as close as possible to the BP5 pin. This pin can be used as a pullup voltage for power-good signals.

7.3.15 Overcurrent Protection

For protection against load faults, the TPSM5D1806E implements a cycle-by-cycle peak current protection. When the inductor current hits the peak current limit threshold, the high-side FET turns off and the low-side FET turns on. The device monitors the valley current threshold during the high-side FET off time. If the inductor current clears the valley current threshold, the high-side FET will turn on at the next clock edge. However, if the inductor current remains higher than the valley current threshold, the next high-side FET cycle is skipped, the low-side FET remains on, and an internal counter is incremented. This counter increments every clock edge as long as the inductor current remains higher than the valley current threshold. If the current falls below the valley current threshold at the next clock edge, the counter is reset. If the counter increments 16 consecutive clock cycles, a current limit fault is identified and the device enters hiccup mode to reduce power dissipation. In hiccup mode, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced, which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. The device re-initiates the power-up sequence when the junction temperature drops below 145°C typically.

7.4 Device Functional Modes

7.4.1 Active Mode

The TPSM5D1806E is in active mode when V_{IN} is above the turn-on threshold and the EN pin voltage is above the EN high threshold. Floating the EN pin allows the device to start-up when a valid input voltage is applied. This allows self start-up of the TPSM5D1806E when the input voltage is in the operation range of 4.5 V to 15 V. Connecting a resistor divider between VIN, EN, and AGND increases the UVLO threshold.

7.4.2 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPSM5D1806E. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode, the standby current is 250 µA typical.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM5D1806E is a dual 6-A output, step-down, DC/DC power module. It is used to convert a higher DC voltage to two separate 6-A power rails or one combined 12-A power rail. The following design procedure can be used to select components for the TPSM5D1806. Alternately, the WEBENCH® software can be used to generate complete designs. When generating a design, the WEBENCH® software uses an iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

8.2 Typical Application (Dual Outputs)

図 8-1 shows a typical TPSM5D1806M-ET schematic for a dual-output design.

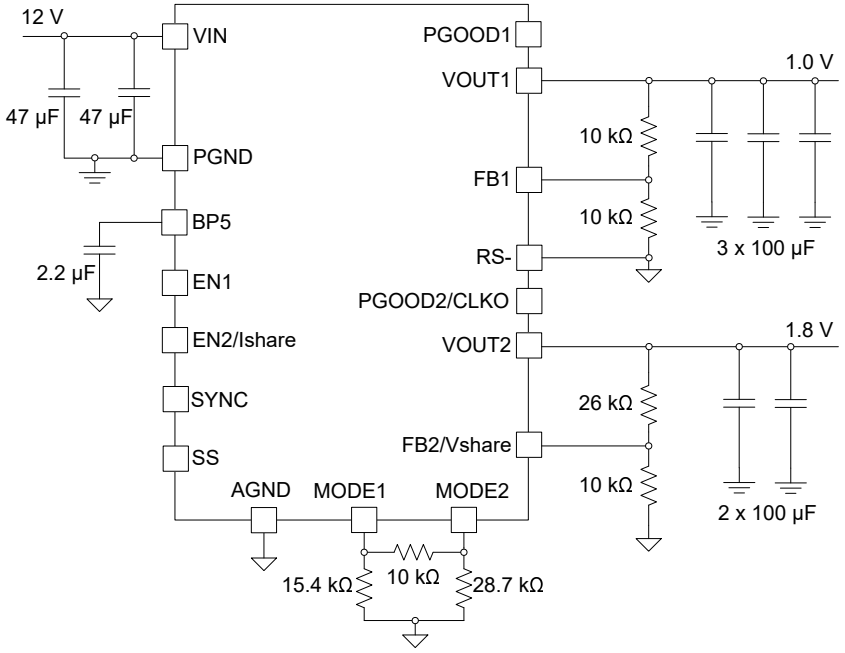


図 8-1. TPSM5D1806E Dual Output Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters and follow the design procedures in セクション 8.2.2.

表 8-1. Design Example Parameters

Design Parameter	Value
Input voltage V_{IN}	12 V typical
Output voltage V_{OUT1}	1.0 V
Output voltage V_{OUT2}	1.8 V
Switching frequency	1.5 MHz
Output current rating	Up to 6 A / output

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM5D1806E device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM5D1806E device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using 式 4:

$$R_{FBT} = 20 \times \left(V_{OUT} - 0.5 \right) (k\Omega) \quad (4)$$

For the desired output voltage of 1.0 V, the formula yields a value of 10 kΩ. Choose the closest available value of 10.0 kΩ for R_{FBT}.

For the desired output voltage of 1.8 V, the formula yields a value of 26 kΩ. Choose the closest available value of 26.1 kΩ for R_{FBT}.

8.2.2.3 Input Capacitors

The TPSM5D1806E requires a minimum input capacitance of 88 µF of ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage.

For this design example, two 47-µF, 25-V ceramic capacitors are used.

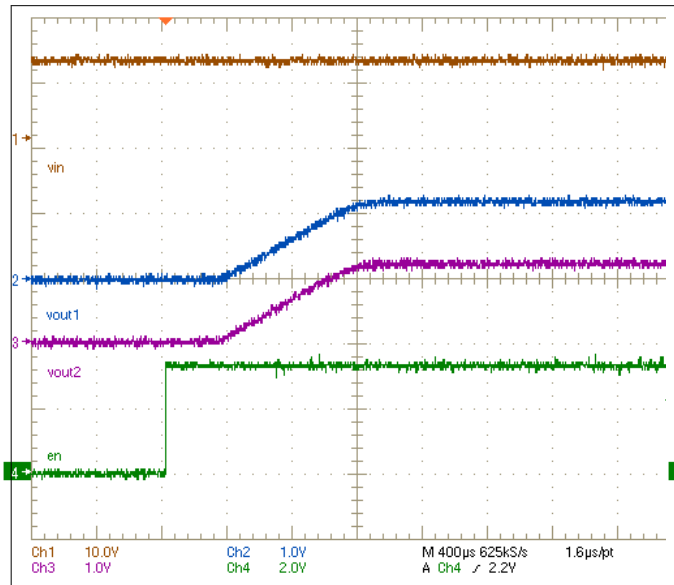
8.2.2.4 Output Capacitor Selection

The TPSM5D1806E requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See 図 7-5 for the required output capacitance.

For this design example, three 100-µF, 6.3-V ceramic capacitors are selected for the 1.0-V output. For the 1.8-V output, two 100-µF, 6.3-V ceramic capacitors are selected. Additional output capacitance can be needed to meet transient requirements.

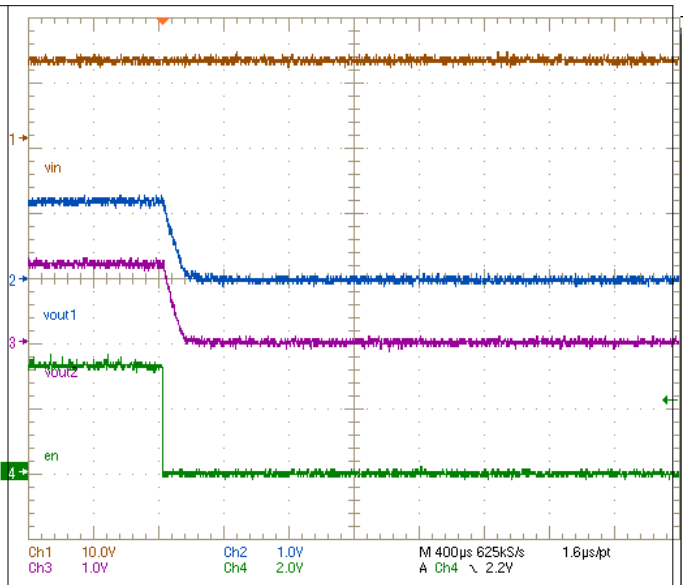
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8.2.3 Application Curves



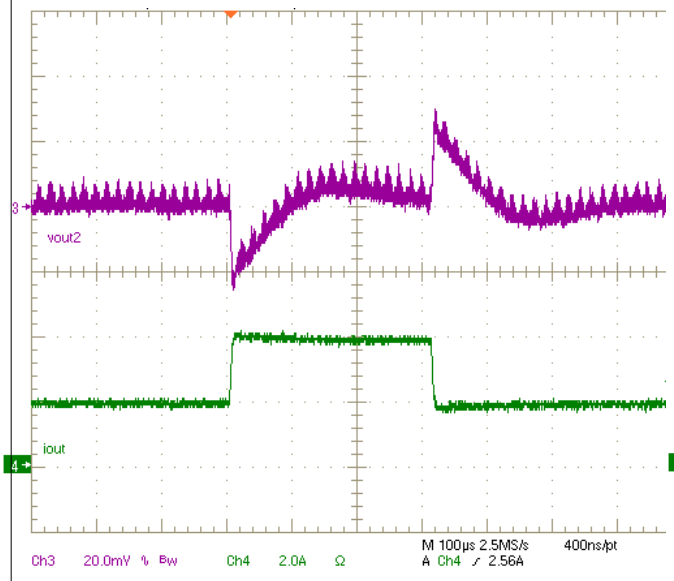
V_{IN} = 12 V I_{OUT1} = 3 A I_{OUT2} = 3 A
V_{OUT} = 1.2 V C_{OUT} = 4 × 100 µF

図 8-2. Enable Turn-On with Load



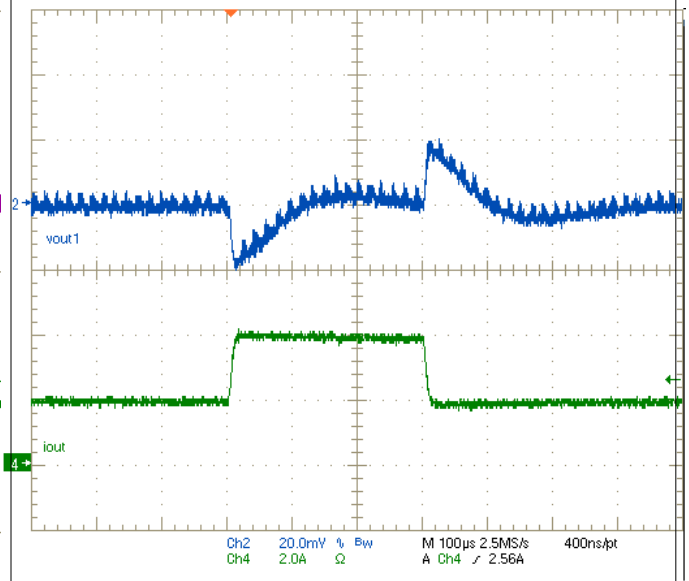
V_{IN} = 12 V I_{OUT1} = 3 A I_{OUT2} = 3 A
V_{OUT} = 1.2 V C_{OUT} = 4 × 100 µF

図 8-3. Enable Turn-Off with Load



V_{IN} = 12 V V_{OUT} = 1.2 V C_{OUT} = 4 × 100 µF (Nominal)
Slew rate: 1 A/µs I_{OUT} = 2 A to 4 A

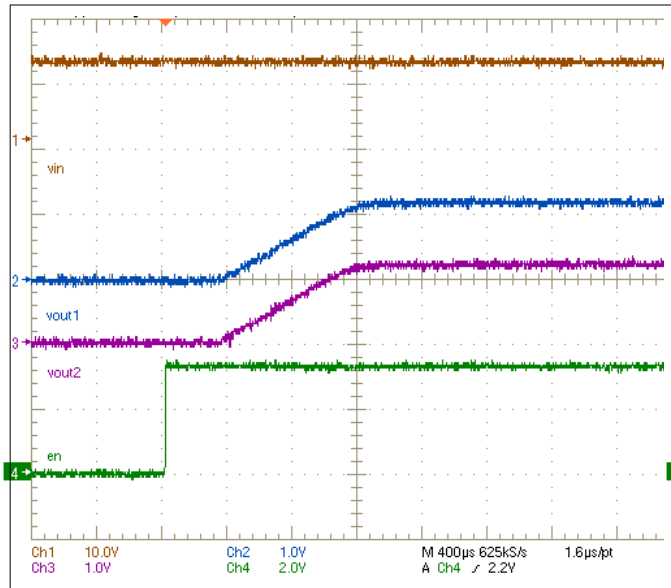
図 8-4. Transient Response V_{OUT2}



V_{IN} = 12 V V_{OUT} = 1.2 V C_{OUT} = 4 × 100 µF (Nominal)
Slew rate: 1 A/µs I_{OUT} = 2 A to 4 A

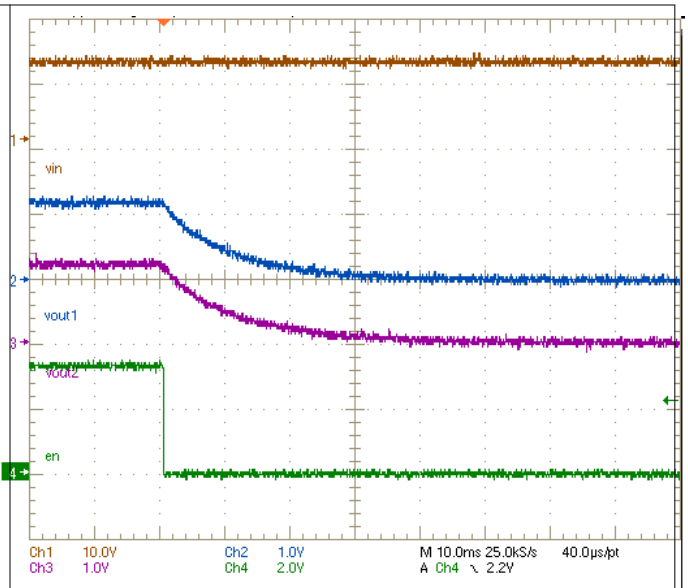
図 8-5. Transient Response V_{OUT1}

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V_{IN} = 12 V V_{OUT} = 1.2 V C_{OUT} = 4 × 100 µF (Nominal)

図 8-6. Enable Turn-On Without Load



V_{IN} = 12 V V_{OUT} = 1.2 V C_{OUT} = 4 × 100 µF (Nominal)

図 8-7. Enable Turn-Off Without Load

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8.2.4 Typical Application (Paralleled Outputs)

The dual outputs of the TPSM5D1806E can be combined to create a higher current (up to 12 A), single output. 図 8-8 shows a typical TPSM5D1806E schematic for a paralleled output design.

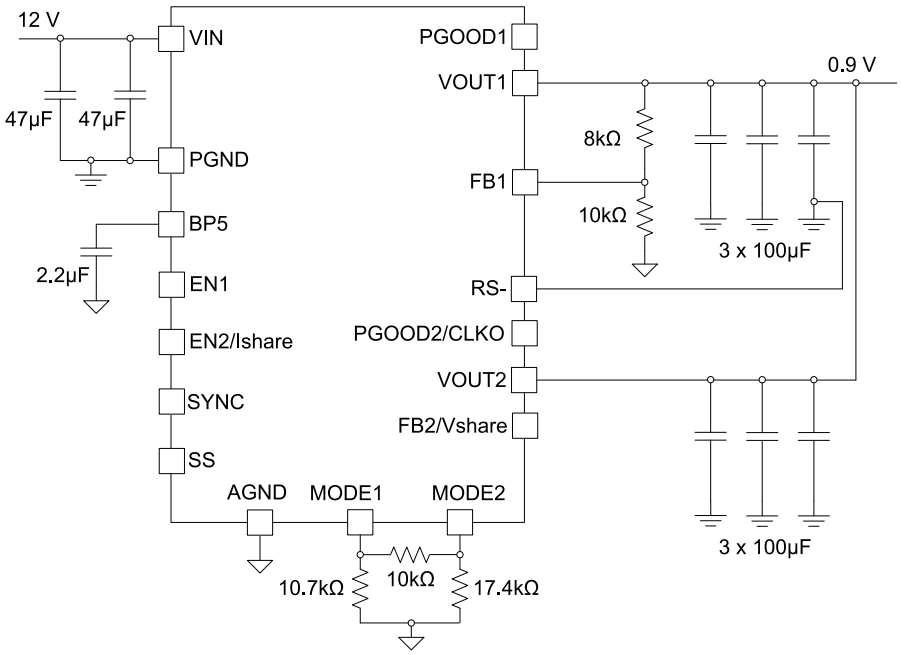


図 8-8. TPSM5D1806E Parallel Outputs Typical Schematic

8.2.4.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters and follow the design procedures in セクション 8.2.4.2.

表 8-2. Design Example Parameters

Design Parameter	Value
Input voltage V_{IN}	12 V typical
Output voltage	0.9 V
Switching frequency	1.0 MHz
Output current rating	Up to 12 A

8.2.4.2 Detailed Design Procedure

8.2.4.2.1 Output Voltage Setpoint

The output voltage of the TPSM5D1806E device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using 式 5:

$$R_{FBT} = 20 \times \left(V_{OUT} - 0.5 \right) (k\Omega) \quad (5)$$

For the desired output voltage of 0.9 V, the formula yields a value of 8 kΩ. Choose the closest available value of 8.06 kΩ for R_{FBT} or place two resistors in series to come closer to the exact value.

8.2.4.2.2 Input Capacitors

The TPSM5D1806E requires a minimum input capacitance of 88 µF of ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage.

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For this design example, two 47-µF, 25-V ceramic capacitors are used.

8.2.4.2.3 Output Capacitor Selection

The TPSM5D1806E requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See 図 7-5 for the required output capacitance.

For this design example, six 100-µF, 6.3-V ceramic capacitors are selected for the 0.9-V output. Additional output capacitance can be needed to meet transient requirements.

9 Power Supply Recommendations

The TPSM5D1806E is designed to operate from an input voltage supply range between 4.5 V and 15 V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPSM5D1806E supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few centimeters from the TPSM5D1806E, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is a 47-µF electrolytic type capacitor.

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10 Layout

The performance of any switching power supply depends as much on the layout of the PCB as the component selection. The following guidelines help users design a PCB with the best power conversion performance, optimal thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 10-1 and 図 10-2 show typical PCB layouts. The following are some considerations for an optimized layout.

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Examples

Single Device Dual Output

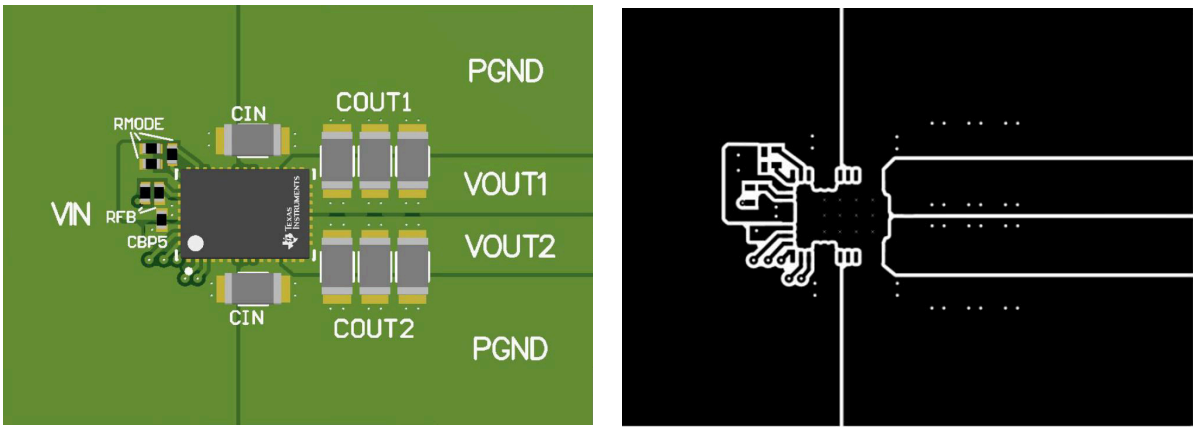


図 10-1. Typical Dual-Output Layout

Single Device Parallel Output

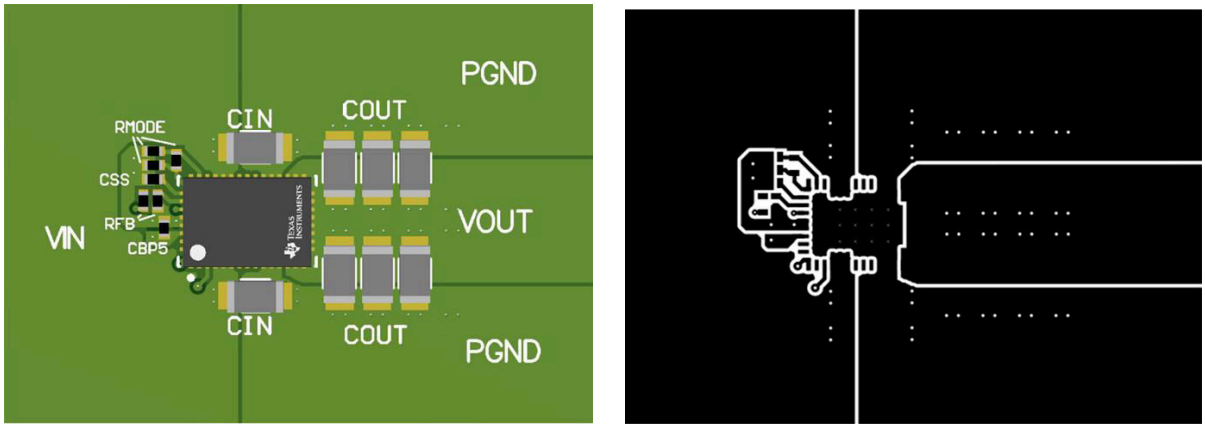


図 10-2. Typical Parallel-Output Layout

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10.2.1 Package Specifications

TPSM5D1806		Value	Unit
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	89.3	MHrs

10.2.2 EMI

The TPSM5D1806E is compliant with EN55011 Class-B radiated emissions. 図 10-3 and 図 10-4 show typical examples of radiated emissions plots for the TPSM5D1806E. The graphs include the plots of the antenna in the horizontal and vertical positions.

EMI plots were measured using the standard TPSM5D1806EVM with ferrite beads (Murata, BLM18SG330SN1) in series with the input wires.

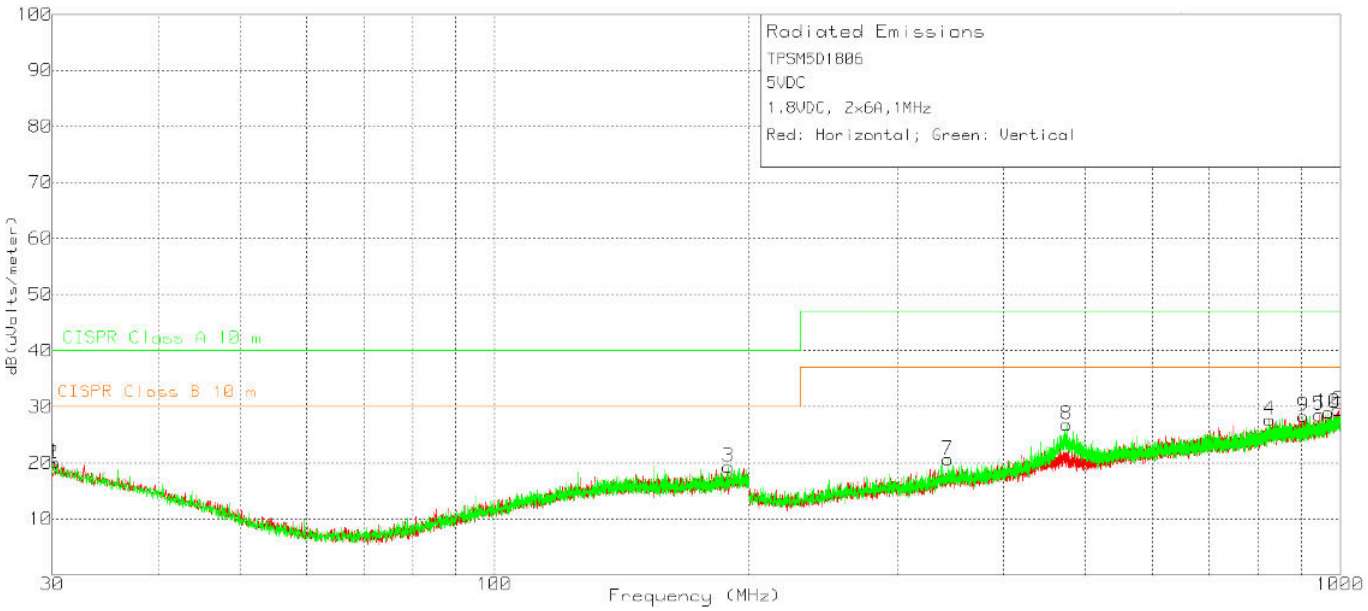


図 10-3. Radiated Emissions 5-V Input, 1.8-V Outputs, 6-A/Output Load

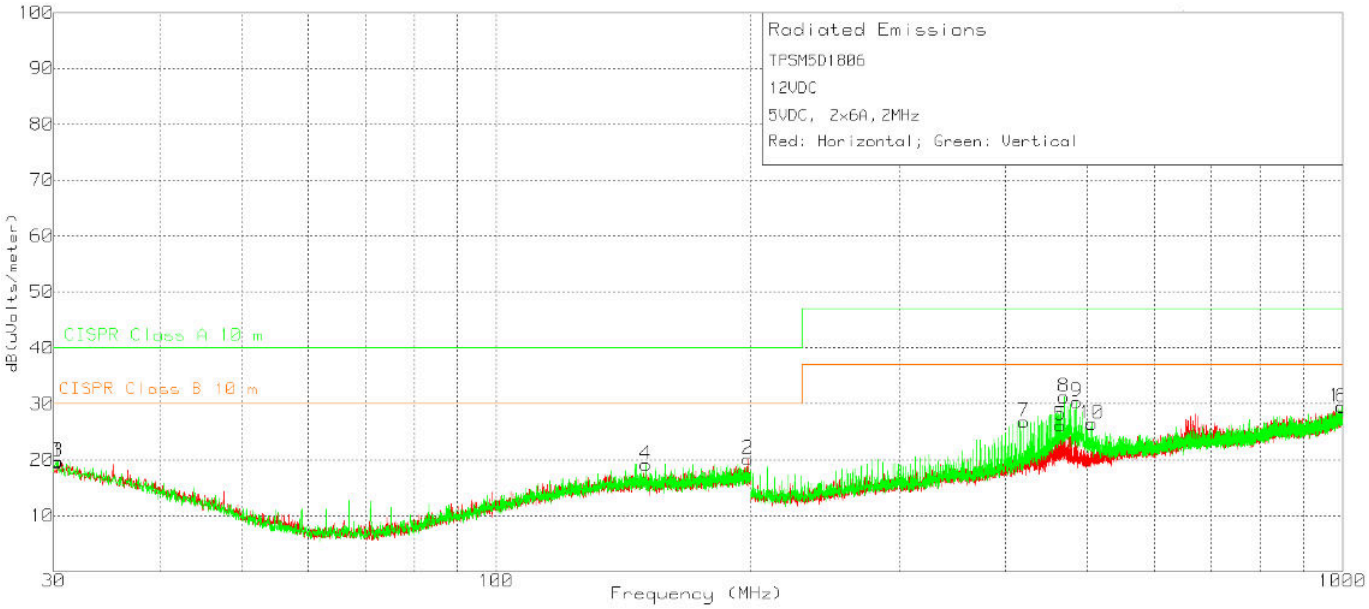


図 10-4. Radiated Emissions 12-V Input, 5-V Output, 6-A/Output Load

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM5D1806E device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
2UM5D1806MRDBRETG4	Active	Production	B0QFN (RDB) | 51	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPSM5D1806M ET
2UM5D1806MRDBRETG4.A	Active	Production	B0QFN (RDB) | 51	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPSM5D1806M ET
TPSM5D1806MRDBR-ET	Active	Production	B0QFN (RDB) | 51	2000 | LARGE T&R	Exempt	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPSM5D1806M ET
TPSM5D1806MRDBR-ET.A	Active	Production	B0QFN (RDB) | 51	2000 | LARGE T&R	Exempt	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPSM5D1806M ET

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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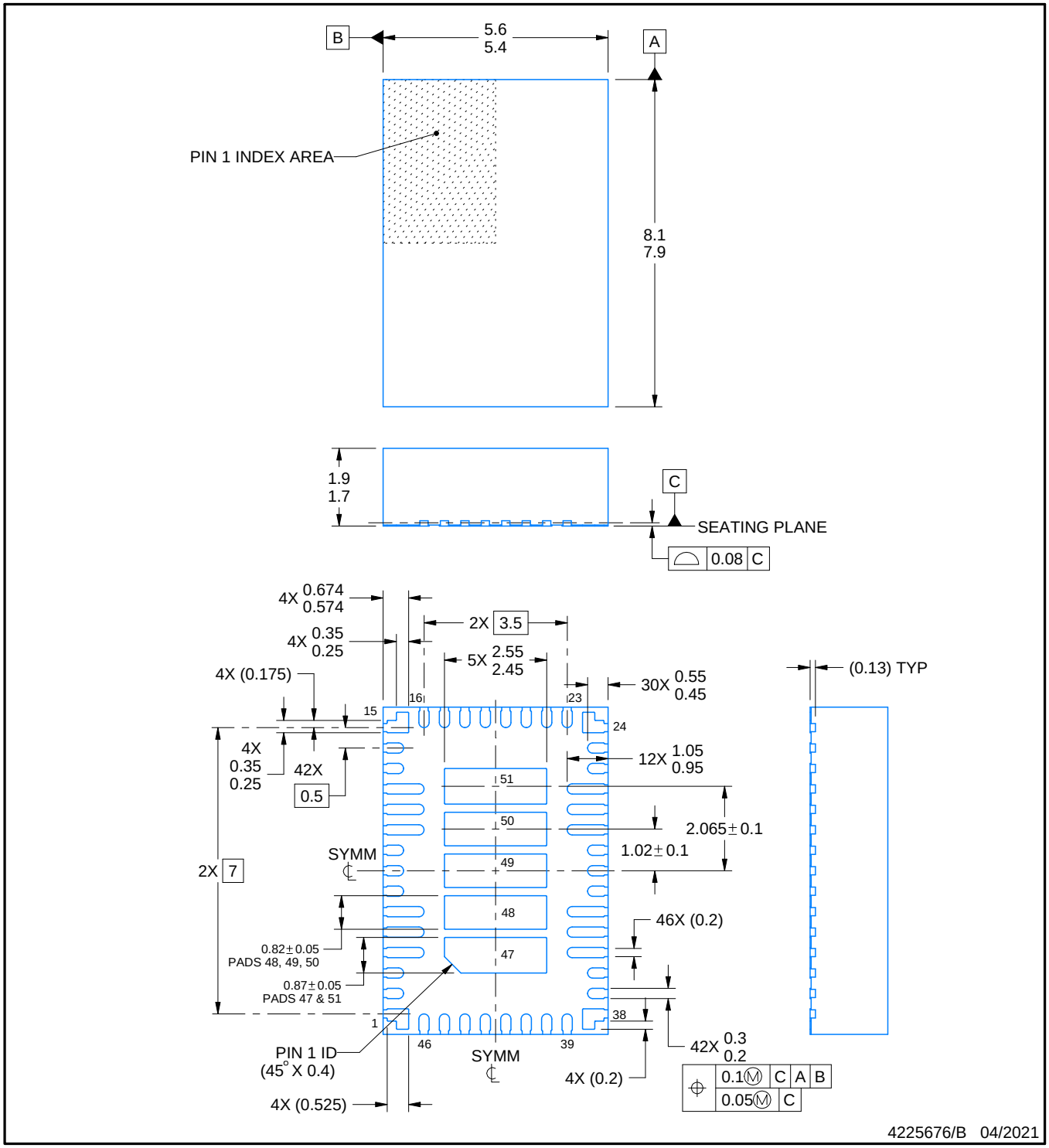
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RDB0051A

PACKAGE OUTLINE

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

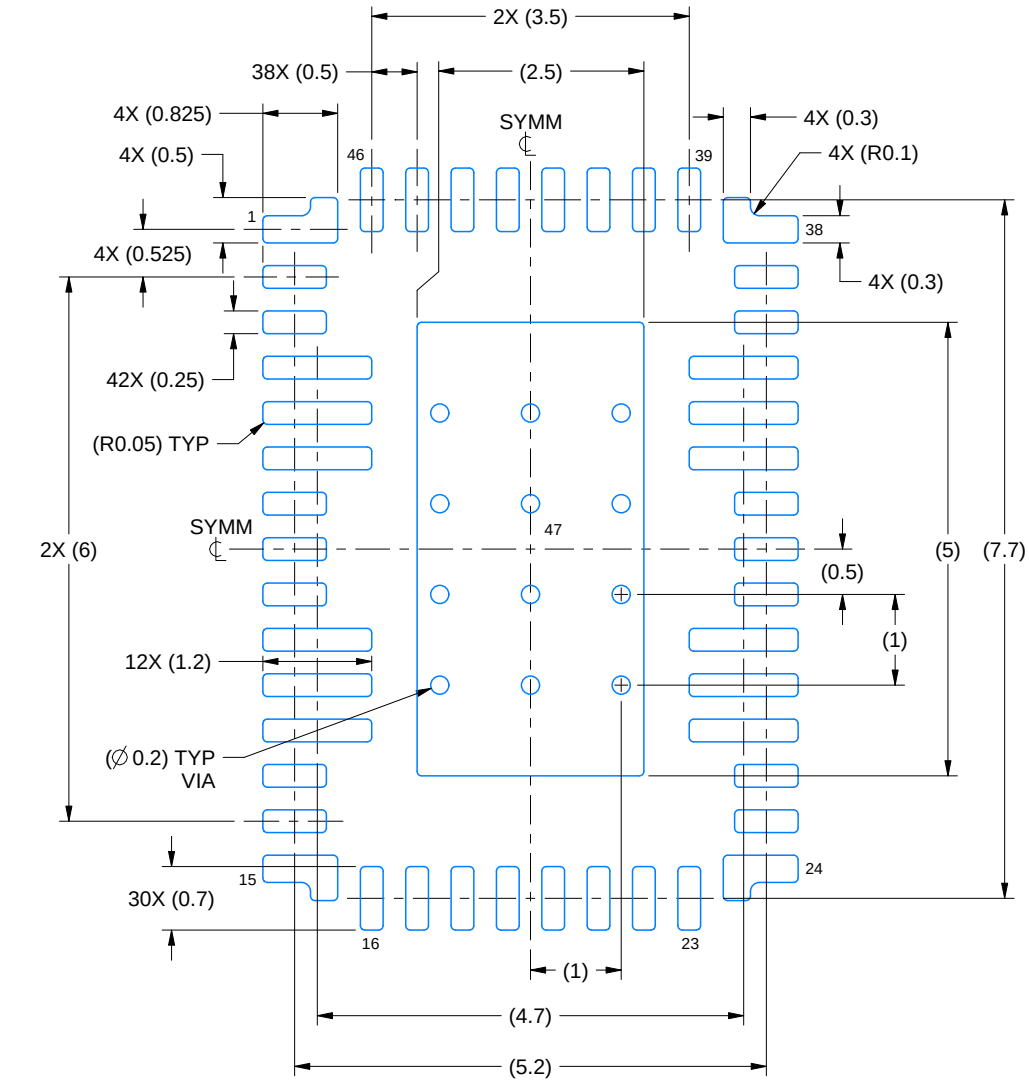
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

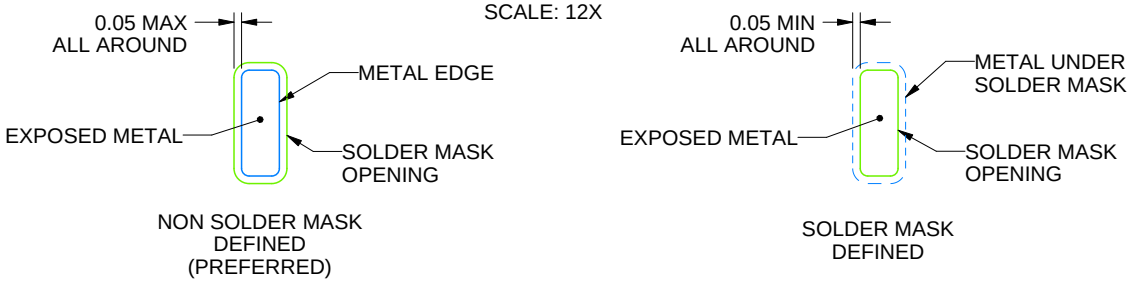
RDB0051A

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

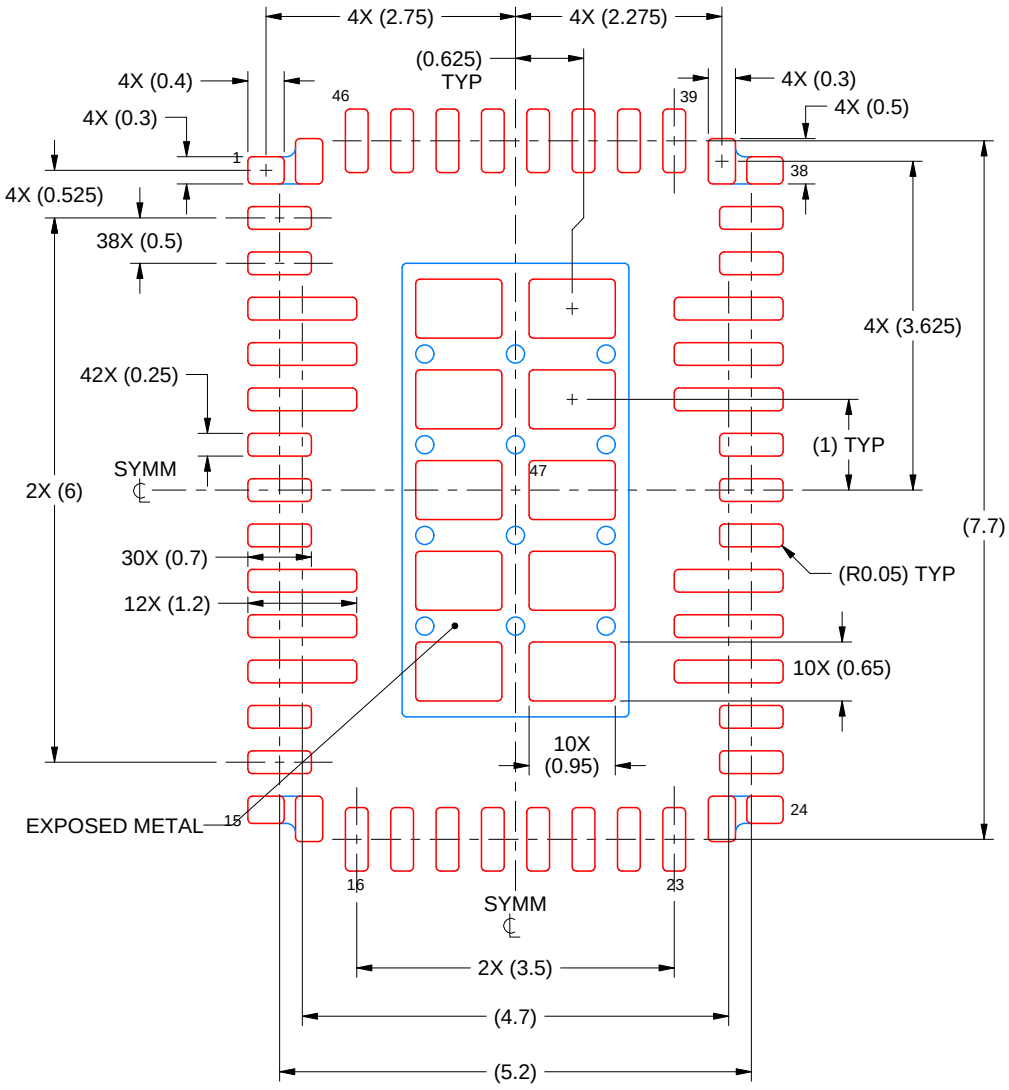


SOLDER MASK DETAILS

4225676/B 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 12X

SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 47: 49%

4225676/B 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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