TPSM63610 高密度、3V～36V 入力、1V～20V 出力 8A (10A ピーク)、 Enhanced HotRod™ QFN パッケージ採用、同期整流式降圧 DC/DC 電源モジュール、

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 用途の広い 36V_{IN}、8A_{OUT} 同期整流式降圧モジュール
  - MOSFET、インダクタ、コントローラを内蔵
  - 出力電圧を調整可能、1V～20V
  - 6.5mm × 7.5mm × 4mm のオーバーモールド・パッケージ
  - -40℃～125℃の接合部温度範囲
  - 200kHz～2.2MHz の範囲で周波数を調整可能
  - 負電圧出力に対応可能
- 全負荷範囲にわたって極めて高い効率を実現
  - 95% 以上のピーク効率
  - 外部バイアス・オプションによる効率向上
  - 放熱パッドによる熱インピーダンスの低減。EVM θ_{JA} = 18.2℃/W
  - シャットダウン時静止電流：0.6μA (標準値)
- 非常に小さい伝導および放射 EMI シグネチャ
  - デュアル入力パスと内蔵コンデンサを備えた低ノイズ・パッケージにより、スイッチのリンギングが減少
  - 抵抗により調整可能なスイッチ・ノードのスルーレート
  - CISPR 11 および 32 Class B の放射規格に準拠
- スケーラブルな電源に対応した設計
  - TPSM63608 (36V、6A) とピン互換
- 堅牢な設計のための本質的な保護機能
  - 高精度のイネーブル入力とオープン・ドレインの PGOOD インジケータによるシーケンシング、制御、V_{IN} UVLO
  - 過電流およびサーマル・シャットダウン保護機能
- WEBENCH® Power Designer により、TPSM63610 を使用するカスタム設計を作成

2 アプリケーション

- 試験および測定、航空宇宙および防衛
- ファクトリ・オートメーション / 制御
- 降圧および反転型の昇降圧電源

3 概要

同期整流式降圧モジュール ファミリから派生した TPSM63610 は、パワー MOSFET、シールド付きインダクタ、受動部品を Enhanced HotRod™ QFN パッケージで組み合わせた高集積 36V、8A DC/DC 設計です。このモジュールは、VIN および VOUT ピンをパッケージの角に配置し、入力および出力コンデンサの配置を最適化しています。モジュールの下面には大きな 4 つのサーマル・パッドがあるため、単純なレイアウトが可能で、製造時の扱いも容易です。

出力電圧が 1V～20V の TPSM63610 は、小さな PCB フットプリントで低 EMI の設計を迅速かつ容易に実装できるよう設計されています。このトータル・ソリューションを使用すると、外付け部品はわずか 4 個で済み、設計プロセスで磁気および補償のための部品選択も不要です。

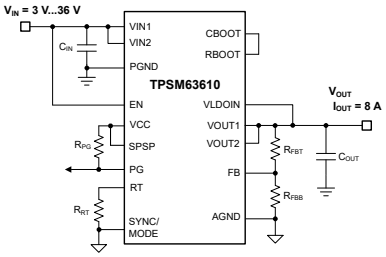
TPSM63610 デバイスはスペースに制約のあるアプリケーション向けに小型でシンプルな設計となっていますが、調整可能な入力電圧 UVLO 用のヒステリシス付き高精度イネーブル、抵抗によりプログラム可能なスイッチ ノードのスルーレート、EMI 改善のためのスペクトラム拡散機能など、堅牢な性能を実現するための多くの機能を備えています。また、VCC、ブートストラップ、入力コンデンサを内蔵しているため、信頼性と密度が向上します。このデバイスは、全負荷電流範囲 (FPWM) にわたって一定のスイッチング周波数に設定することも、可変周波数 (PFM) に設定して軽負荷時の効率を高めることもできます。シーケンシング、フォルト保護、出力電圧監視用の PGOOD インジケータも内蔵しています。

パッケージ情報

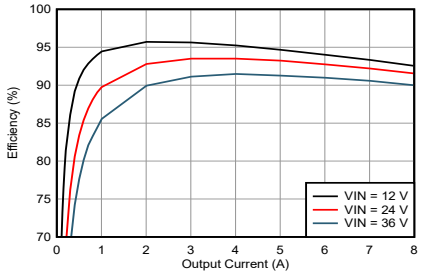
部品番号	パッケージ (1)	パッケージ サイズ (2)
TPSM63610	RDF (B3QFN、22)	7.50mm × 6.50mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



代表的な回路図



代表的な効率、V_{OUT} = 5V、F_{SW} = 1MHz

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Device Comparison Table ... 4
5 Pin Configuration and Functions ... 4
6 Specifications ... 6
6.1 Absolute Maximum Ratings ... 6
6.2 ESD Ratings ... 6
6.3 Recommended Operating Conditions ... 6
6.4 Thermal Information ... 7
6.5 Electrical Characteristics ... 7
6.6 System Characteristics ... 10
6.7 Typical Characteristics ... 11
7 Detailed Description ... 13
7.1 Overview ... 13
7.2 Functional Block Diagram ... 14
7.3 Feature Description ... 14
7.4 Device Functional Modes ... 22
8 Applications and Implementation ... 23
8.1 Application Information ... 23
8.2 Typical Applications ... 23
8.3 Power Supply Recommendations ... 31
8.4 Layout ... 31
9 Device and Documentation Support ... 34
9.1 Device Support ... 34
9.2 Documentation Support ... 35
9.3 ドキュメントの更新通知を受け取る方法 ... 35
9.4 サポート・リソース ... 35
9.5 Trademarks ... 35
9.6 静電気放電に関する注意事項 ... 35
9.7 用語集 ... 35
10 Revision History ... 36
11 Mechanical, Packaging, and Orderable Information ... 36

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4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	RATED OUTPUT CURRENT	PEAK OUTPUT CURRENT (TRANSIENT CONDITIONS)	JUNCTION TEMPERATURE RANGE
TPSM63610	TPSM63610RDFR	8 A	10 A	–40°C to 125°C
TPSM63610E	TPSM63610EXTRDFR	8 A	10 A	–55°C to 125°C
TPSM63608	TPSM63608RDFR	6 A	8 A	–40°C to 125°C

5 Pin Configuration and Functions

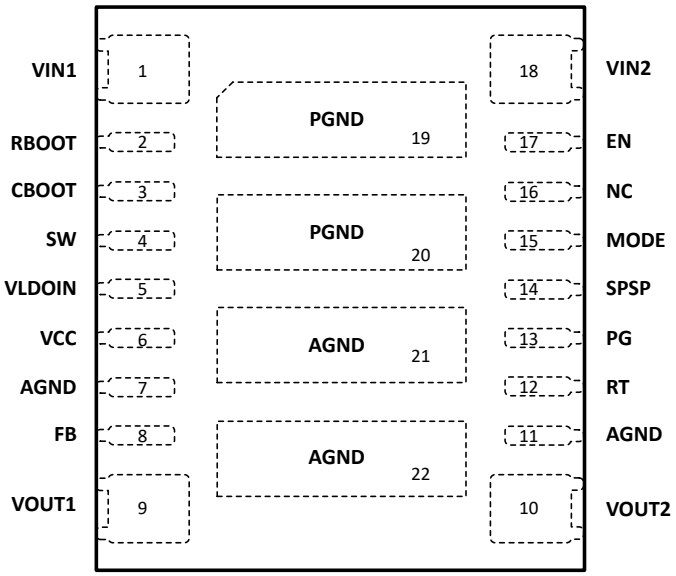


図 5-1. 22-Pin B3QFN RDF Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1, 18	VIN1, VIN2	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.
2	RBOOT	I	External bootstrap resistor connection. RBOOT is brought out to use in conjunction with CBOOT to effectively lower the value of the internal series bootstrap resistance to adjust the switch-node slew rate, if necessary. A resistance from 0 to 500 Ω can be connected between RBOOT and CBOOT. A resistance of 0 Ω has the fastest slew rate and highest efficiency. A value of 100 Ω creates a nice balance between efficiency and EMI. Leaving open sets the slew rate to 20 ns and TI does not recommend due to increased self heating.
3	CBOOT	O	Bootstrap pin for the internal high-side gate driver. A 100-nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage. CBOOT is brought out to use in conjunction with RBOOT to effectively lower the value of the internal series bootstrap resistance to adjust the switch-node slew rate, if necessary.
4	SW	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on this pin must be kept to a minimum to prevent issues with noise and EMI.
5	VLDOIN	P	Input bias voltage. Input to the internal LDO that supplies the internal control circuits. Connect to an output voltage point to improve efficiency. Connect an optional high-quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If the output voltage is above 12 V, connect this pin to ground.
6	VCC	P	Internal LDO output. Used as a supply to the internal control circuits. Do not connect to any external loads. A 1-µF capacitor internally connects from VCC to AGND.

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表 5-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
7, 11, 21, 22	AGND	G	Analog ground. Zero-voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. *These pins must be connected to PGND*. See *Layout Example* for a recommended layout.
8	FB	I	Feedback input. Connect the midpoint of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. Do not leave open or connect to ground.
9, 10	VOUT1, VOUT2	P	Output voltage. These pins are connected to the internal buck inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
12	RT	I	Frequency setting pin used to set the switching frequency between 200 kHz and 2.2 MHz by placing an external resistor from RT to AGND. Connect to VCC for 400 kHz. Connect to ground for 2.2 MHz. Do not leave open.
13	PG	O	Open-drain power-good monitor output that asserts low if the FB voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor to a suitable voltage is required . If not used, PG can be left open or connected to GND.
14	SPSP	I	Connect to VCC or through a resistor to ground to enable spread spectrum. Connect to GND to disable spread spectrum. If using spread spectrum, a VCC connection turns off the spread spectrum tone correction while a resistor to ground (10-30 kΩ) adjusts the tone correction to lower the output voltage ripple. Do not float this pin.
15	SYNC/ MODE	I	This pin controls the mode of operation of the device. Modes include Auto mode (automatic PFM/PWM operation), forced pulse width modulation (FPWM), and synchronized to an external clock. The clock triggers on the rising edge of an applied external clock. Pull low to enable PFM operation, pull high to enable FPWM, or connect to a clock to synchronize to an external frequency in FPWM mode. Do not float this pin. When synchronized to an external clock, use the RT pin to set the internal frequency close to the synchronized frequency to avoid disturbances if the external clock is turned on and off
16	NC	—	No connection. Tie to GND or leave open.
17	EN	I	Precision enable input to regulator. High = on, low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Do not float
19, 20	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect these pads to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See *Layout Example* for a recommended layout.

(1) P = Power, G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	Transient VIN to AGND, PGND(2)	–0.3	42	V
Voltages	Continuous VIN to AGND, PGND(2)	–0.3	36	V
Voltages	SW to AGND, PGND	–0.3	V_{IN} + 0.3	V
Voltages	RBOOT, CBOOT to SW	–0.3	5.5	V
Voltages	Transient EN or SYNC/MODE to AGND, PGND(2)	–0.3	42	V
Voltages	Continuous EN or SYNC/MODE to AGND, PGND(2)	–0.3	36	V
Voltages	BIAS to AGND, PGND	–0.3	16	V
Voltages	FB to AGND, PGND: Adjustable Versions	–0.3	5.5	V
Voltages	$\overline{\text{RESET}}$ to AGND, PGND	0	20	V
Current	$\overline{\text{RESET}}$ sink current(4)	0	10	mA
Voltages	RT to AGND, PGND	–0.3	5.5	V
Voltages	VCC to AGND, PGND	–0.3	5.5	V
Voltages	PGND to AGND(3)	–1	2	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A maximum of 42 V can be sustained at this pin for duration of ≤ 100 ms at a duty cycle of ≤ 0.01%. 36 V can be sustained for the life of this device.
(3) This specification applies to voltage durations of 100 ns or less. The maximum D.C. voltage must not exceed +/- 0.3 V.
(4) Do not exceed the pin voltage rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	Input Voltage Range(1)	3	36	V
Output voltage	Output Adjustment Range for adjustable output versions (2)	1	20	V
Frequency	Frequency adjustment range	200	2200	kHz
Sync Frequency	Synchronization frequency range	200	2200	kHz
Output current	I_{OUT}	0	8	A
Temperature	Operating ambient temperature, T_A	–40	105	°C

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Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Temperature	Operating junction temperature, T_J	–40	125	°C

(1) 3.7 V is required at VIN for start-up, an extended input voltage range down to 3.0 V is possible after start-up; See Minimum input voltage for start-up conditions.
(2) Under no conditions can the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

THERMAL METRIC (1)		TPSM636XX RDF 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM63610EVM) (3)	18	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7) (2)	25	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, the EVM $R_{\Theta JA}$ = 21.6 °C/W. For design information please see the thermal design and layout section.
(3) Refer to the EVM User's Guide for board layout and additional information. For thermal design information please see the thermal design and layout section.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +125°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Minimum operating input voltage	Needed to start up			3.7	V
		Once Operating			3	V
$V_{IN_OP_H}$	Minimum voltage hysteresis			1		V
I_Q	Non-switching input current; measured at VIN pin (3)	V_{FB} = +5%, V_{BIAS} = 5 V		0.5	10	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0 V, V_{IN} = 12 V		0.57	7.5	µA
I_B	Current into BIAS pin (not switching)	V_{FB} = +5%, V_{BIAS} = 5 V, Auto Mode Enabled		18.5	26	µA
ENABLE (EN PIN)						
V_{EN}	Enable input-threshold voltage - rising	V_{EN} rising	1.0	1.263	1.365	V
V_{EN_HYST}	Enable threshold hysteresis		0.1	0.35	0.5	V
V_{EN_WAKE}	Enable Wake-up threshold		0.4			V
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 12 V		1.5	50	nA
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal VCC voltage	V_{BIAS} = 0V		3.4		V
		V_{BIAS} = 3.3 V, 20 mA		3.2		

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Limits apply over the recommended operating junction temperature range of -40°C to +125°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC_UVLO}	V_{IN} voltage at which Internal VCC under voltage lock-out is released	I_{VCC} = 0A			3.75	V
$V_{CC_UVLO_HYST}$	Internal VCC under voltage lock-out hysteresis	Hysteresis below V_{CC_UVLO}		1.2		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Initial reference voltage accuracy for adjustable (1 V FB) versions	V_{IN} = 3.0 V to 36 V, FPWM Mode	0.985	1	1.015	V
I_{FB}	Input current from FB to AGND	Adjustable versions only, V_{FB} = 1 V			50	nA
CURRENT LIMITS						
I_{SC_8}	Short circuit high-side current Limit	8 A Variant, Duty cycle approaches 0%	11.5	13.8	15.7	A
$I_{LS\text{-}LIMIT_8}$	Low-side current limit		8	9.2	10.5	A
$I_{PEAK\text{-}MIN_8}$	Minimum Peak Inductor Current			1.9		A
$I_{L\text{-}NEG_8}$	Negative current limit		–6.4	–5.3	–3.9	A
$I_{L\text{-}ZC}$	Zero-cross current limit. Positive current direction is out of SW pin.	Auto Mode, static measurement		70		mA
V_{HICCUP}	Hiccup threshold on FB pin		0.36	0.4	0.44	V
POWER GOOD (/RESET PIN)						
$V_{\overline{RESET}\text{-}OV}$	$\overline{RESET}$ upper threshold - Rising	% of FB voltage	109.5	112	114.5	%
$V_{\overline{RESET}\text{-}UV}$	$\overline{RESET}$ lower threshold - Falling	% of FB voltage	93	95	97.5	%
$V_{\overline{RESET}_GUARD}$	$\overline{RESET}$ UV threshold as percentage of steady state output voltage with output voltage and UV threshold, falling, read at the same T_J, and V_{IN}.	Falling			97	%
$V_{\overline{RESET}\text{-}HYS\text{-}FALLING}$	$\overline{RESET}$ fallling threshold hysteresis	% of FB voltage		1.3		%
$V_{\overline{RESET}\text{-}HYS\text{-}RISING}$	$\overline{RESET}$ rising threshold hysteresis	% of FB voltage		1.3		%
$V_{\overline{RESET}_VALID}$	Minimum input voltage for proper $\overline{RESET}$ function	Measured when $V_{\overline{RESET}}$ < 0.4 V with 10 kOhm pullup to external 5 V			1.2	V
V_{OL}	$\overline{RESET}$ Low-level function output voltage	46.0 µA pull up to $\overline{RESET}$ pin, V_{IN} = 1.0 V, V_{EN} = 0 V			0.4	V
		1 mA pull up to $\overline{RESET}$ pin, V_{IN} = 12 V, V_{EN} = 0 V			0.4	
		2 mA pull up to $\overline{RESET}$ pin, V_{IN} = 12 V, V_{EN} = 3.3 V			0.4	
R_{RESET}	$\overline{RESET}$ ON resistance,	V_{EN} = 5 V, 1mA pull up current		44	125	Ω
$R_{\overline{RESET}}$	$\overline{RESET}$ ON resistance,	V_{EN} = 0 V, 1mA pull up current		18	40	Ω
t_{RESET_FILTER}	$\overline{RESET}$ edge deglitch delay		10	26	45	µs
t_{RESET_ACT}	$\overline{RESET}$ active time	Time FB must be valid before $\overline{RESET}$ is released.	1.2	2.1	3.75	ms
OSCILLATOR (RT and SYNC PINS)						
f_{OSC}	Internal oscillator frequency	RT = GND	1.90	2.2	2.42	MHz
f_{OSC}	Internal oscillator frequency	RT = VCC	320	400	450	kHz
$f_{FIXED_2.2MHz}$	Oscillator frequency measured using maximum value of RT resistor to select 2.2 MHz	RT = 6.81 kΩ	1.95	2.2	2.42	MHz

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Limits apply over the recommended operating junction temperature range of -40°C to +125°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{FIXED_0.4MHz}$	Oscillator frequency measured using minimum value of RT resistor to select 0.4 MHz	RT = 40.2 kΩ	352	400	448	kHz
f_{ADJ}	Center Trim oscillator frequency	RT = 22.6 kΩ	630	700	770	kHz
V_{SYNCDL}	SYNC/MODE input voltage low		0.4			V
V_{SYNCDH}	SYNC/MODE input voltage high				1.7	V
V_{SYNCD_HYST}	SYNC/MODE input voltage hysteresis		0.185		1	V
R_{SYNC}	Internal pulldown resistor to ensure SYNC/MODE doesn't float			100		kΩ
t_{SYNC_EDGE}	High and Loww duration needed for synchronizing clock to be recognized on SYNC/MODE pin		100			ns
t_{MSYNC}	Time at one level needed to indicate FPWM or Auto Mode		7		20	µs
t_{LOCK}	Time needed for clock to lock to a valid synchronization signal	RT = 39.2 kΩ		4.3		ms
SPREAD SPECTRUM						
ΔFc+	Frequency increase of internal oscillator from spread spectrum		1	4	7.5	%
ΔFc-	Frequency decrease of internal oscillator from spread spectrum		-8	-4	-1	%
HIGH SIDE DRIVE (CBOOT PIN)						
V_{CBOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turnoff high-side switch			1.9		V
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	Load = 1 A, $C_{BOOT-SW}$ = 3.2 V		21	39	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	Load = 1 A, $C_{BOOT-SW}$ = 3.2 V		13	25	mΩ
PWM LIMITS (SW PIN)						
t_{ON-MIN}	Minimum HS switch on-time	V_{IN} =18 V, $V_{SYNC/MODE}$ = 5 V, I_{OUT} = 2A, R_{BOOT} = 0 Ω		62	81	ns
$t_{OFF-MIN}$	Minimum HS switch off-time	V_{IN} = 5 V		70	103	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	6.9	8.9	11	µs
D_{MAX}	Maximum switch duty cycle	While in frequency fold-back	98			%
		fsw =1.85 MHz		87		
START UP						
t_{EN}	Turn-on delay	V_{IN} = 12 V, C_{VCC} = 1 µF, time from EN high to first SW pulse if output starts at 0 V		0.82	1.2	ms
t_{SS}	Time from first SW pulse to V_{REF} at 90%, of set point.		1.6	2.2	2.7	ms
t_W	Short circuit wait time ("hiccup" time)			40		ms

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6.6 System Characteristics

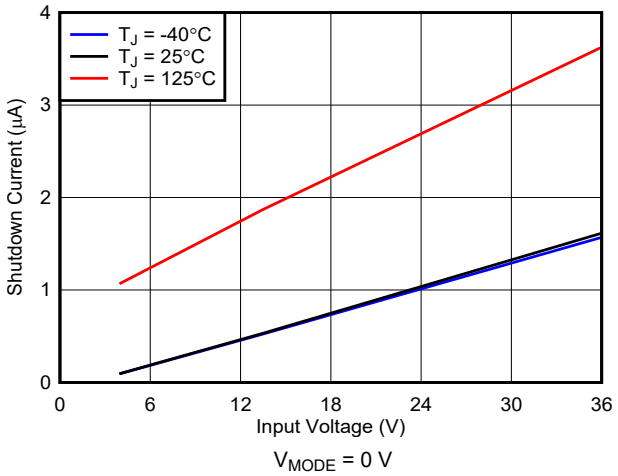
The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = $V_{EN/SYNC}$ = 24 V, V_{OUT} = V_{VLDOIN} = 3.3 V, V_{MODE} = 0 V, F_{SW} = 1 MHz, I_{OUT} = 0 A		8		µA
OUTPUT VOLTAGE						
ΔV_{OUT1}	Load regulation	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 0.1 A to 8 A		4		mV
ΔV_{OUT2}	Line regulation	V_{OUT} = 3.3 V, V_{IN} = 4 V to 36 V, I_{OUT} = 8 A		1		mV
ΔV_{OUT3}	Load transient	V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 0 A to 4 A at 1 A/µs, $C_{OUT(derated)}$ = 100 µF		150		mV
EFFICIENCY						
η	Efficiency	V_{IN} = 12 V, V_{OUT} = V_{VLDOIN} = 3.3 V, I_{OUT} = 4 A, F_{SW} = 1 MHz		92.1		%
η	Efficiency	V_{IN} = 24 V, V_{OUT} = V_{VLDOIN} = 3.3 V, I_{OUT} = 4 A, F_{SW} = 1 MHz		91		%
η	Efficiency	V_{IN} = 12 V, V_{OUT} = V_{VLDOIN} = 5 V, I_{OUT} = 4 A, F_{SW} = 1 MHz		94.3		%
η	Efficiency	V_{IN} = 24 V, V_{OUT} = V_{VLDOIN} = 5 V, I_{OUT} = 4 A, F_{SW} = 1 MHz		93		%

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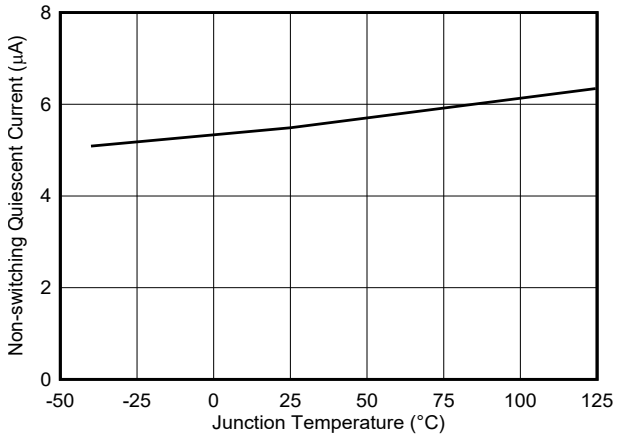
6.7 Typical Characteristics

V_{IN} = 12 V, unless otherwise specified.



V_{MODE} = 0 V

図 6-1. Shutdown Supply Current



V_{LDOIN} = 3.3 V

図 6-2. Non-Switching Input Supply Current

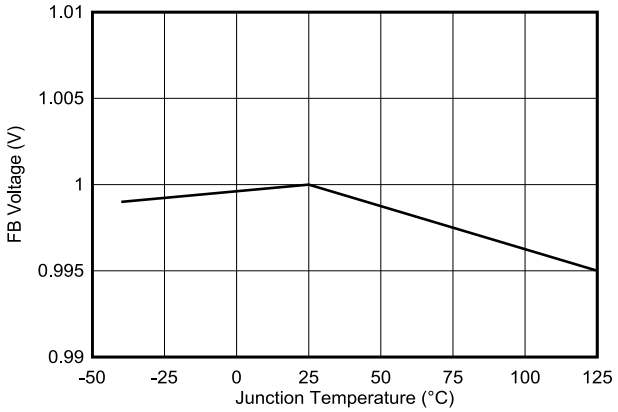


図 6-3. Feedback Voltage

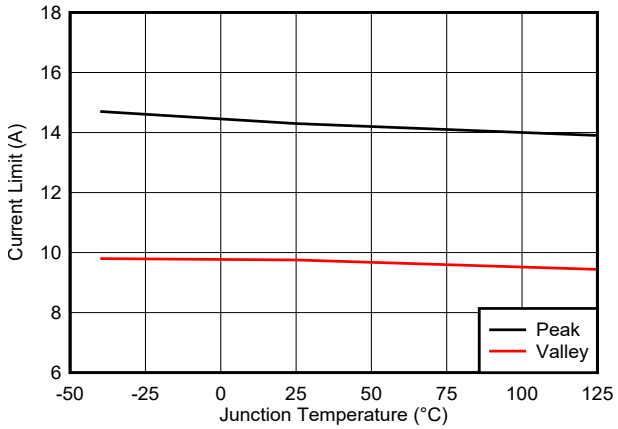


図 6-4. High-Side (Peak) and Low-Side (Valley) Current Limits TPSM63610

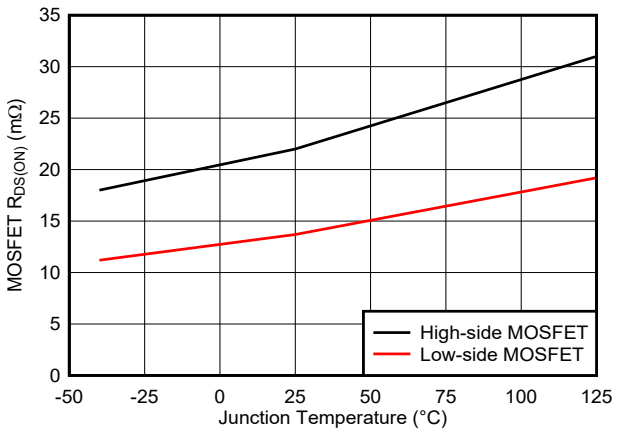


図 6-5. High-Side and Low-Side MOSFET $R_{DS(on)}$

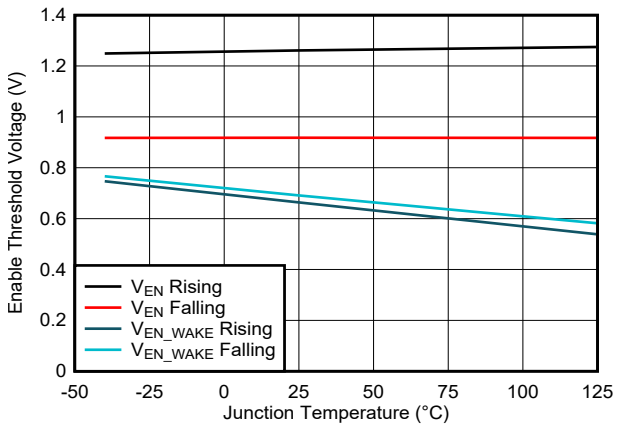


図 6-6. Enable Thresholds

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6.7 Typical Characteristics (continued)

V_{IN} = 12 V, unless otherwise specified.

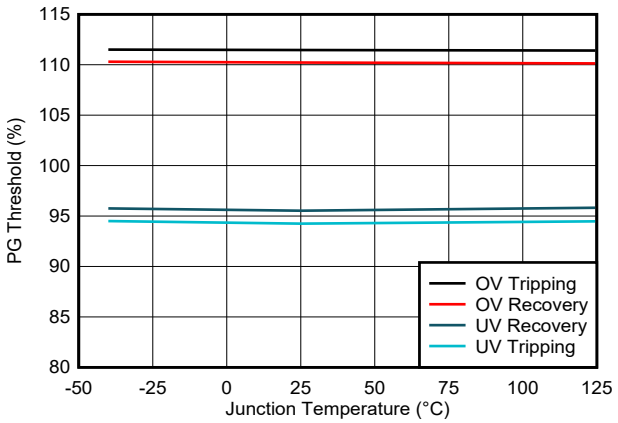


図 6-7. Power-Good (PG) Thresholds

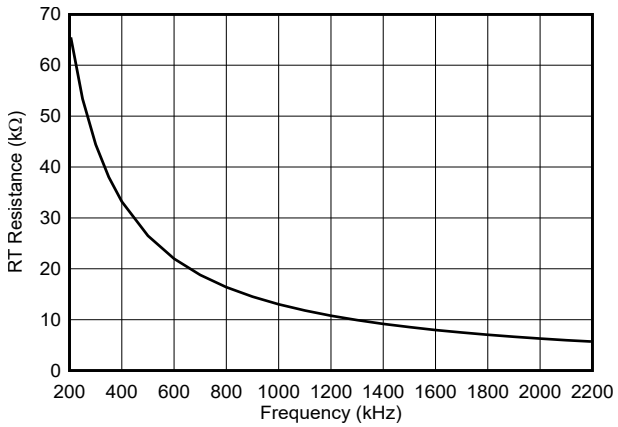


図 6-8. Switching Frequency Set by RT Resistor

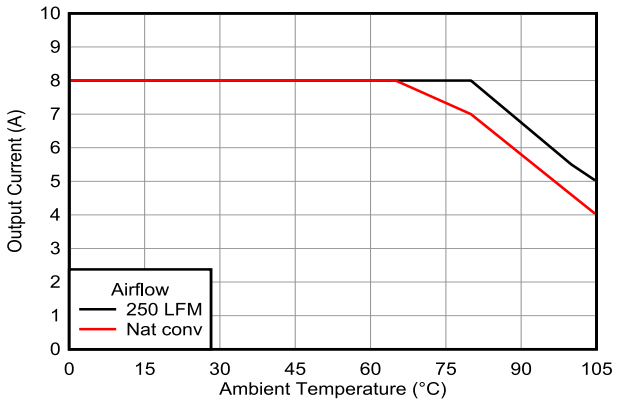


図 6-9. EVM Thermal Performance (V_{IN} = 12 V, V_{OUT} = 5 V, F_{SW} = 1 MHz)

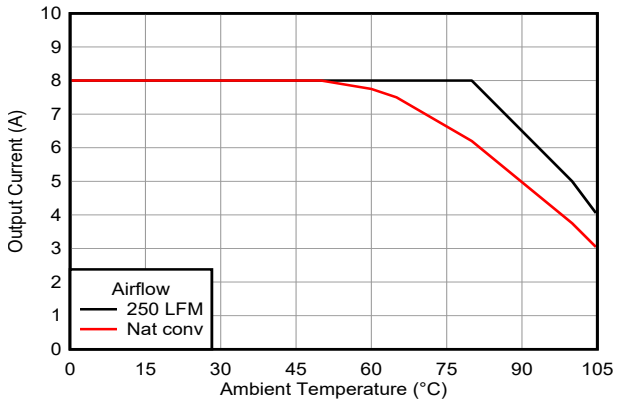


図 6-10. EVM Thermal Performance (V_{IN} = 24 V, V_{OUT} = 5 V, F_{SW} = 1 MHz)

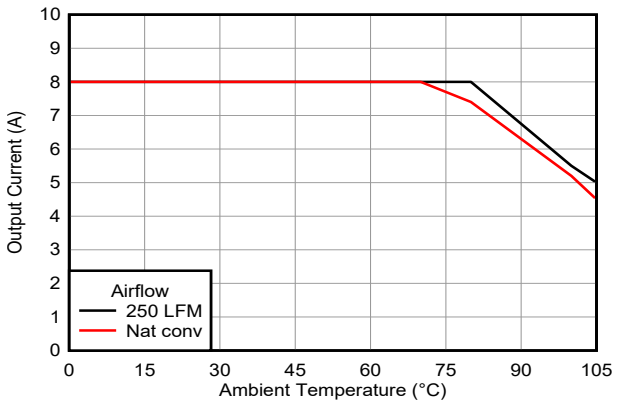


図 6-11. EVM Thermal Performance (V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 700 kHz)

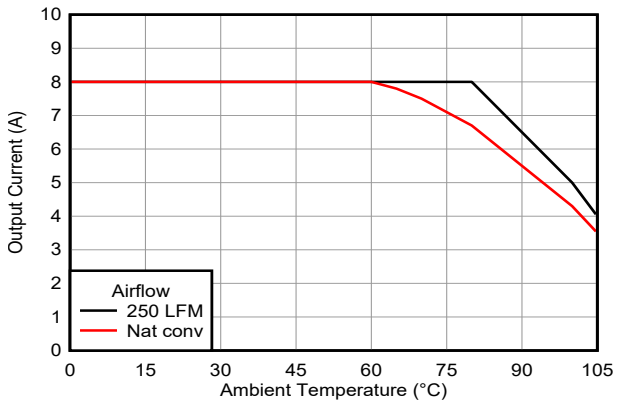


図 6-12. EVM Thermal Performance (V_{IN} = 24 V, V_{OUT} = 3.3 V, F_{SW} = 700 kHz)

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7 Detailed Description

7.1 Overview

The TPSM63610 is an easy-to-use, synchronous buck DC/DC power module designed for a wide variety of applications where reliability, small design size, and low EMI signature are of paramount importance. With integrated power MOSFETs, a buck inductor, and PWM controller, the TPSM63610 operates over an input voltage range of 3 V to 36 V with transients as high as 42 V. The module delivers up to 8-A (10-A peak) DC load current with high conversion efficiency and ultra-low input quiescent current in a very small design footprint. Control loop compensation is not required, reducing design time and external component count.

With a programmable switching frequency from 200 kHz to 2.2 MHz using the RT pin or an external clock signal, the TPSM63610 incorporates specific features to improve EMI performance in noise-sensitive applications:

- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling
- Dual-random spread spectrum (DRSS) modulation reduces peak emissions
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching

Together, these features significantly reduce EMI filtering requirements, while helping to meet CISPR 11 and CISPR 32 Class B EMI limits for conducted and radiated emissions.

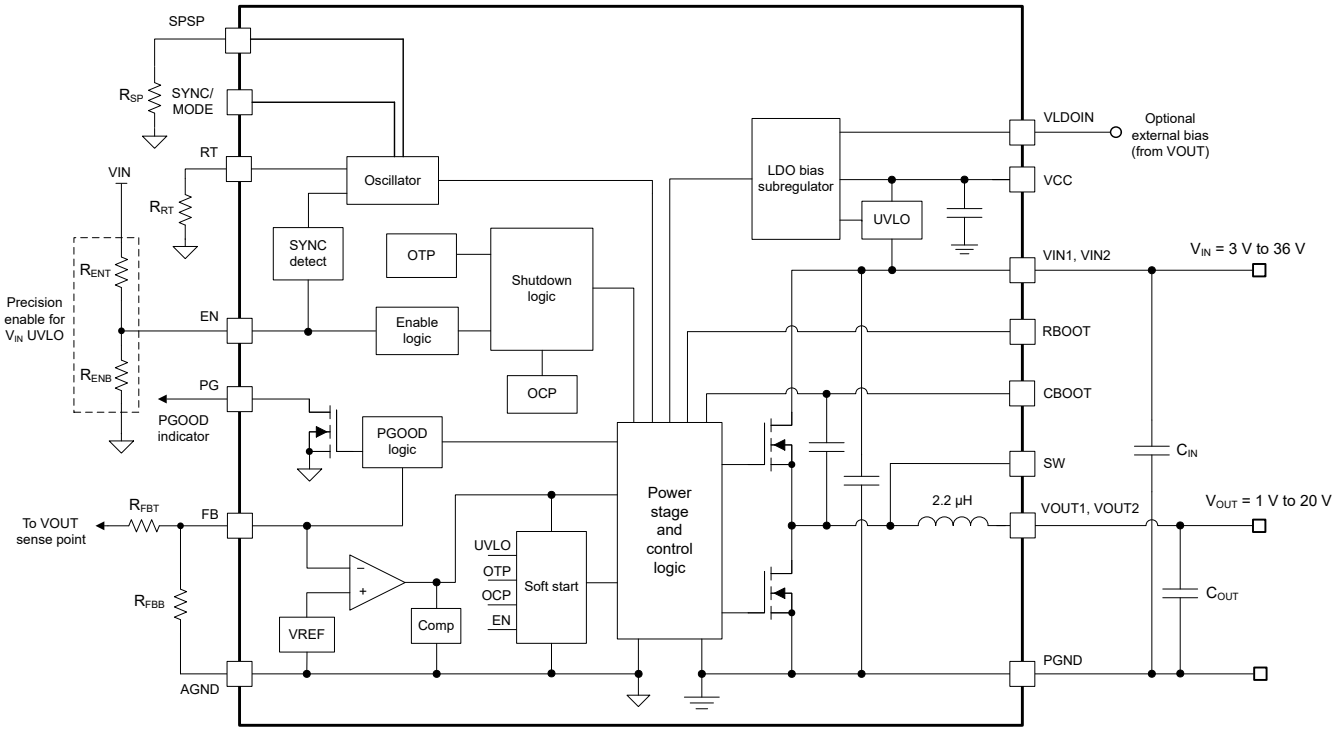
The TPSM63610 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery.

Leveraging a pin arrangement designed for simple layout that requires only a few external components, the TPSM63610 is specified to maximum junction temperatures of 125°C. See typical performance curves to estimate suitability in a given ambient environment.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range (VIN1, VIN2)

With a steady-state input voltage range from 3 V to 36 V, the TPSM63610 module is intended for step-down conversions from typical 12-V, 24-V, and 28-V input supply rails. The schematic circuit in 図 7-1 shows all the necessary components to implement a TPSM63610-based buck regulator using a single input supply.

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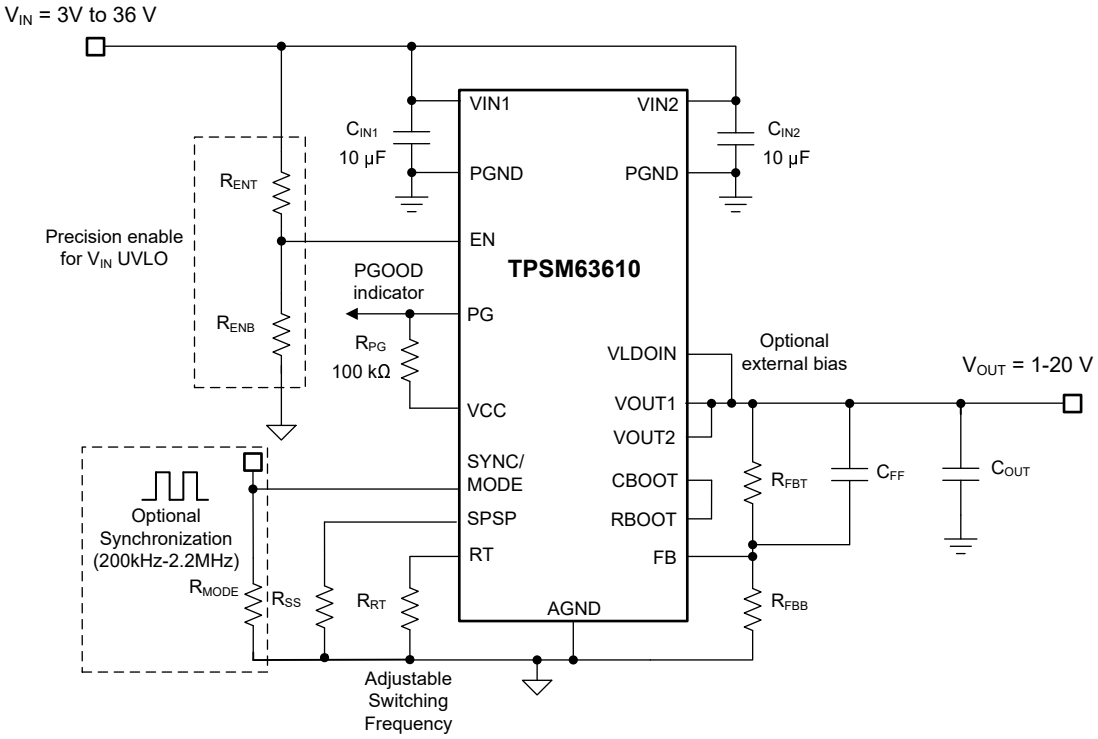


図 7-1. TPSM63610 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

The minimum input voltage required for start-up is 3.7 V. Take extra care to make sure that the voltage at the VIN pins of the module (VIN1 and VIN2) does not exceed the absolute maximum voltage rating of 42 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the *Absolute Maximum Ratings* can damage the IC.

7.3.2 Adjustable Output Voltage (FB)

The TPSM63610 has an adjustable output voltage range from 1 V up to a maximum of 20 V or slightly less than V_{IN}, whichever is lower. Setting the output voltage requires two feedback resistors, designated as R_{FBT} and R_{FBB} in 図 7-1. The reference voltage at the FB pin is set at 1 V with a feedback system accuracy over the full junction temperature range of ±1%. The junction temperature range for the device is –40°C to 125°C.

Calculate the value for R_{FBB} using 式 1 below based on a recommended value for R_{FBT} of 100 kΩ.

$$R_{FBB}(k\Omega) = \frac{R_{FBT}(k\Omega)}{\frac{V_{OUT}}{1} - 1} \quad (1)$$

表 7-1 lists the standard resistor values for several output voltages and the recommended switching frequency range to maintain reasonable peak-to-peak inductor ripple current. This table also includes the minimum required output capacitance for each output voltage setting to maintain stability. The capacitances as listed represent *effective* values for ceramic capacitors derated for DC bias voltage and temperature. Furthermore, place a feedforward capacitor, C_{FF}, in parallel with R_{FBT} to increase the phase margin when the output capacitance is close to the minimum recommended value.

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表 7-1. Standard R_{FBT} Values, Recommended F_{SW} Range and Minimum C_{OUT}

V_{OUT} (V)	R_{FBB} (kΩ) (1)	SUGGESTED F_{SW} RANGE (kHz)	$C_{OUT(min)}$ (µF) (EFFECTIVE)	BOM(2)	C_{FF} (pF)	V_{OUT} (V)	R_{FBB} (kΩ) (1)	SUGGESTED F_{SW} RANGE (MHz)	$C_{OUT(min)}$ (µF) (EFFECTIVE)	BOM(2)	C_{FF} (pF)
1	Open	200 to 750	400	4 × 100 µF (6.3 V)	—	9	12.5	0.75 to 1.5	66	4 × 47 µF (16 V)	—
1.8	125	300 to 900	350	4 × 100 µF (6.3 V)	100	12	9.09	1 to 1.7	30	3 × 22 µF (25 V)	—
3.3	43.4	400 to 1100	100	4 × 47 µF (10 V)	47	15	7.14	1 to 1.9	20	3 × 22 µF (25 V)	—
5	25	500 to 1400	75	3 × 47 µF (10 V)	22	20	5.26	1.2 to 2.2	15	3 × 22 µF (25 V)	—

(1) R_{FBT} = 100 kΩ.
(2) Refer to 表 7-3 for the output capacitor list.

Note that higher feedback resistances consume less DC current. However, an upper R_{FBT} resistor value higher than 1 MΩ renders the feedback path more susceptible to noise. Higher feedback resistances generally require more careful layout of the feedback path. Make sure to locate the feedback resistors close to the FB and AGND pins, keeping the feedback trace as short as possible (and away from noisy areas of the PCB). See *Layout Example* guidelines for more detail.

7.3.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. 式 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \times \left({I_{OUT}}^2 \times (1 - D) + \frac{{\Delta i_L}^2}{12} \right)} \tag{2}$$

where

- D = V_{OUT} / V_{IN} is the module duty cycle.

Ideally, the DC and AC components of input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} – I_{IN}) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, 式 3 gives the peak-to-peak ripple voltage amplitude:

$$\Delta V_{IN} = \left(\frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \right) \tag{3}$$

式 4 gives the input capacitance required for a particular load current:

$$C_{IN} \geq \left(\frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})} \right) \tag{4}$$

where

- ΔV_{IN} is the input voltage ripple specification.

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The TPSM63610 requires a minimum of two 10-µF ceramic input capacitors, preferably with X7R or X7S dielectric and in 1206 or 1210 footprint. Additional capacitance can be required for applications to meet conducted EMI specifications, such as CISPR 11 or CISPR 32.

表 7-2 includes a preferred list of capacitors by vendor. To minimize the parasitic inductance in the switching loops, position the ceramic input capacitors in a symmetrical layout close to the VIN1 and VIN2 pins and connect the capacitor return terminals to the PGND pins using a copper ground plane under the module.

表 7-2. Recommended Ceramic Input Capacitors

VENDOR(1)	DIELECTRIC	PART NUMBER	CASE SIZE	CAPACITANCE (µF)(2)	RATED VOLTAGE (V)
TDK	X7R	C3216X7R1H106K160AC	1206	10	50
Murata	X7S	GCM32EC71H106KA03K	1210	10	50
AVX	X7R	12105C106MAT2A	1210	10	50
Murata	X7R	GRM32ER71H106KA12L	1210	10	50

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

As discussed in *Power Supply Recommendations*, an electrolytic bulk capacitance (68 µF to 100 µF) provides low-frequency filtering and parallel damping to mitigate the effects of input parasitic inductance resonating with the low-ESR, high-Q ceramic input capacitors.

7.3.4 Output Capacitors

表 7-1 lists the TPSM63610 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors in particular, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When including additional capacitance above $C_{OUT(min)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See 表 7-3 for a preferred list of output capacitors by vendor.

表 7-3. Recommended Ceramic Output Capacitors

VENDOR(1)	DIELECTRIC	PART NUMBER	CASE SIZE	CAPACITANCE (µF)(2)	VOLTAGE (V)
Murata	X7R	GRM31CZ71C226ME15L	1206	22	16
TDK	X7R	C3225X7R1C226M250AC	1210	22	16
Murata	X7R	GRM32ER71C226KEA8K	1210	22	16
TDK	X6S	C3216X6S1E226M160AC	1206	22	25
AVX	X7R	12103C226KAT4A	1210	22	25
Murata	X7R	GRM32ER71E226ME15L	1210	22	25
AVX	X7R	1210ZC476MAT2A	1210	47	10
Murata	X7R	GRM32ER71A476ME15L	1210	47	10
Murata	X6S	GRM32EC81C476ME15L	1210	47	16
TDK	X6S	C3216X6S0G107M160AC	1206	100	4
Murata	X6T	GRM31CD80J107MEA8L	1206	100	6.3
Murata	X7S	GRM32EC70J107ME15L	1210	100	6.3

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in the table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.5 Switching Frequency (RT)

Connect a resistor, designated as R_{RT} in 図 7-1, between RT and AGND to set the switching frequency within the range of 200 kHz to 2.2 MHz. Refer to 式 5 to calculate R_{RT} for a desired frequency.

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$$R_{RT}(k\Omega) = \frac{16.4}{F_{SW}\,[MHz]} - 0.633 \quad (5)$$

Refer to 表 7-1 or use the simplified expression in 式 5 to find a switching frequency that sets an inductor ripple current of 25% to 40% of the 8-A module current rating at nominal input voltage: Refer to *Frequency Synchronization (SYNC/MODE)* if clock synchronization is required.

7.3.6 Precision Enable and Input Voltage UVLO (EN)

The EN pin provides precision ON and OFF control for the TPSM63610. After the EN pin voltage exceeds the rising threshold and V_{IN} is above its minimum turn-on threshold, the device starts operation. The simplest way to enable the TPSM63610 is to connect EN directly to VIN. This action allows the TPSM63610 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the use of an enable divider network as shown in 図 7-1, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

Calculate R_{ENB} using 式 6:

$$R_{ENB}[k\Omega] = R_{ENT}[k\Omega] \times \left(\frac{V_{EN_RISE}\,[V]}{V_{IN(on)}[V] - V_{EN_RISE}\,[V]} \right) \quad (6)$$

where

- A typical value for R_{ENT} is 100 kΩ.
- V_{EN_RISE} is enable rising threshold voltage of 1.263 V (typical).
- $V_{IN(on)}$ is the desired start-up input voltage.

7.3.7 Frequency Synchronization (SYNC/MODE)

Synchronize the internal oscillator of the TPSM63610 with a positive clock edge to SYNC/MODE, as shown in 図 7-1. The synchronization frequency range is 200 kHz to 2.2 MHz.

TI recommends to tie a resistor from SYNC/MODE to either VCC or ground to keep the pin from floating if the sync signal is lost or off at start-up. A value in the 100-kΩ range. After a valid synchronization signal is applied for 2048 cycles, the clock frequency changes to that of the applied signal.

Referring to 図 7-2, the voltage edge at the SYNC/MODE pin must exceed the SYNC amplitude threshold, V_{SYNCDH}, of 1.8 V to trip the internal synchronization pulse detector. In addition, the minimum SYNC/MODE rising and falling pulse durations must be longer than the SYNC signal hold time, t_{SYNC_EDGE}, of 100 ns.

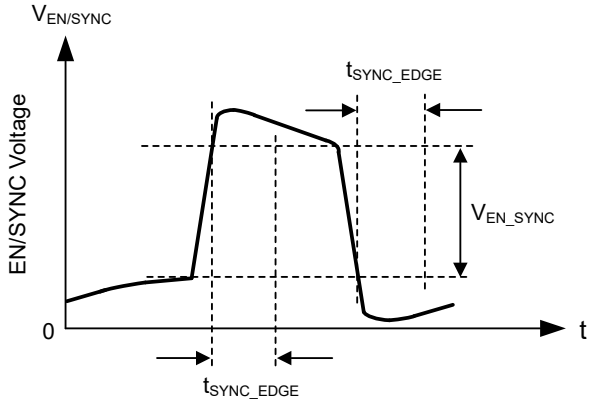


図 7-2. Typical SYNC Waveform

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7.3.8 Spread Spectrum

Spread spectrum is configurable using the SPSP pin. Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The TPSM63610 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The TPSM63610 uses a ±4% (typical) spread of frequencies which can spread energy smoothly across the FM and TV bands. The device implements Dual Random Spread Spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional psuedorandom jumps at the switching frequency

The advantage of DRSS is its equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the TPSM63610 also allows further reduction of the output voltage ripple caused by the spread spectrum modulating pattern. With the SPSP pin grounded, the spread spectrum is disabled. With the SPSP pin tied to VCC, the spread spectrum is on. With the SPSP pin tied through a resistor to ground, the spread spectrum is on. Also, a modulating tone correction is applied to the switcher to reduce the output voltage ripple caused by the frequency modulation. The resistor is usually around 20 kΩ, and can be more precisely calculated using 式 7. Where I_{RATED} = 8 A for TPSM63610, L = 2.2μH.

$$R_{SPSP}[k\Omega] = \frac{14.17 \times \frac{V_{IN}}{V_{OUT}}}{\frac{V_{IN} - V_{OUT}}{I_{RATED} \times L \times F_{SW}}} + 1.22 \quad (7)$$

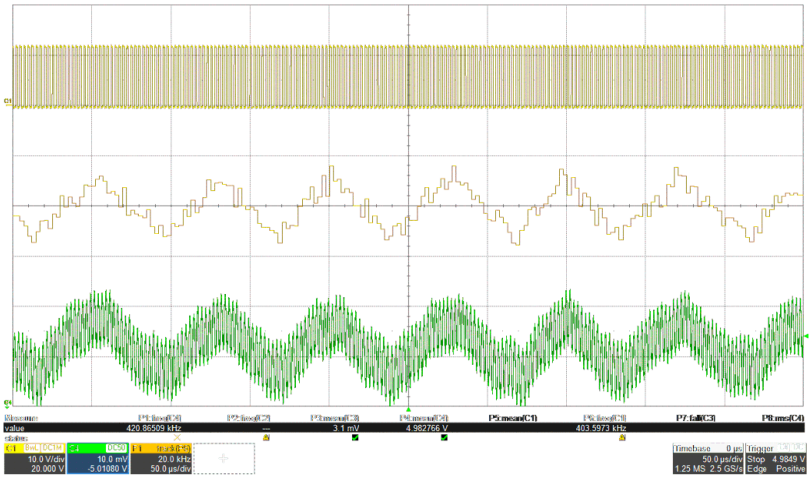


図 7-3. Output Ripple Without Ripple Cancellation Showing V_{SW} (Top), F_{SW} (Middle), V_{OUT} (Bottom)

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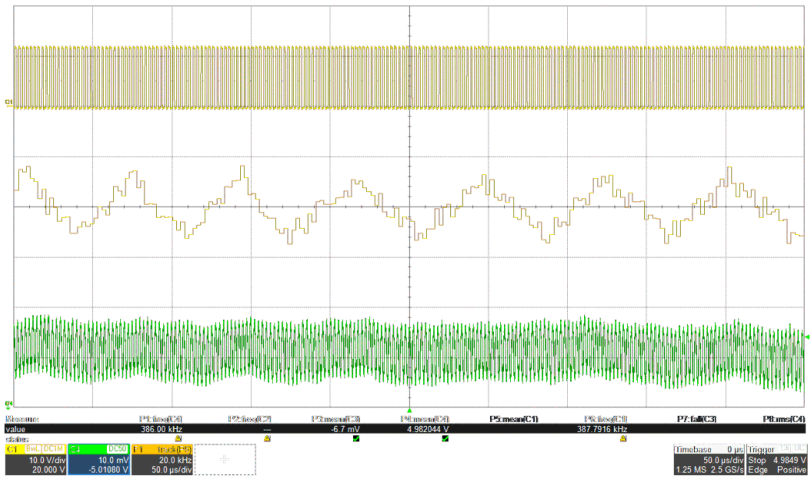


図 7-4. Output Ripple with Ripple Cancellation Showing V_{SW} (Top), F_{SW} (Middle), V_{OUT} (Bottom)

The spread spectrum is only available while the clock of the TPSM63610 are free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed due to operation at low input voltage. This is operation in dropout.
- The clock is slowed under light load in auto mode. This is normally not seen above 750-mA load. Note that if the device is operating in FPWM mode, spread spectrum is active, even if there is no load.
- The clock is slowed due to high input-to-output voltage ratio. This mode of operation is expected if on-time reaches minimum on time.

7.3.9 Power-Good Monitor (PG)

The TPSM63610 provides a power-good status signal to indicate when the output voltage is within a regulation window of 94% to 112%. The PG voltage goes low when the feedback (FB) voltage is outside of the specified PGOOD thresholds (see 図 6-7). This action can occur during current limit and thermal shutdown, as well as when disabled and during start-up.

PG is an open-drain output, requiring an external pullup resistor to a DC supply, such as VCC or V_{OUT}. To limit current supplied by VCC, the recommended range of pullup resistance is 20 kΩ to 100 kΩ. A 26-µs deglitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. When EN is pulled low, PG is forced low and remains remains valid as long as the input voltage is above 1 V (typical). Use the PG signal for start-up sequencing of downstream regulators, as shown in 図 7-5, or for fault protection and output monitoring.

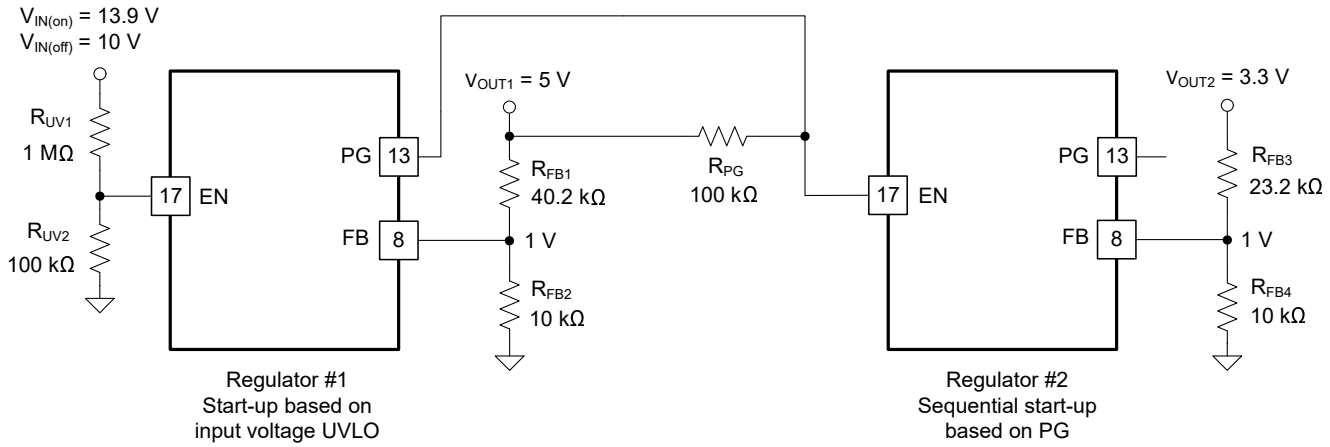


図 7-5. TPSM63610 Sequencing Implementation Using PG and EN

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7.3.10 Adjustable Switch-Node Slew Rate (RBOOT, CBOOT)

Adjust the switch-node slew rate of the TPSM63610 to slow the switch-node voltage rise time and improve EMI performance at high frequencies. However, slowing the rise time decreases efficiency. Care must be taken to balance the improved EMI versus the decreased efficiency.

Place a resistor from RBOOT and CBOOT to allow adjustment of the internal resistance to balance EMI and efficiency performance. If improved EMI is not required, connect RBOOT to CBOOT to short the internal resistor, thus resulting in highest efficiency. If lower EMI is required, connect a resistor from 100 Ω – 500 Ω to. Floating the R_{BOOT} pin results in 20-ns rise time and TI does not recommend due to increased power loss for higher load currents.

7.3.11 Bias Supply Regulator (VCC, VLDOIN)

VCC is the output of the internal LDO subregulator used to supply the control circuits of the TPSM63610. The nominal VCC voltage is 3.3 V. The VLDOIN pin is the input to the internal LDO. Connect this input to V_{OUT} to provide the lowest possible input supply current. If the VLDOIN voltage is less than 3.1 V, VIN1 and VIN2 directly power the internal LDO.

To prevent unsafe operation, VCC has UVLO protection that prevents switching if the internal voltage is too low. See V_{CC_UVLO} and $V_{CC_UVLO_HYS}$ in the *Electrical Characteristics*.

VCC must not be used to power external circuitry. Do not load VCC or short it to ground. VLDOIN is an optional input to the internal LDO. Connect an optional high quality 0.1-µF to 1-µF capacitor from VLDOIN to AGND for improved noise immunity.

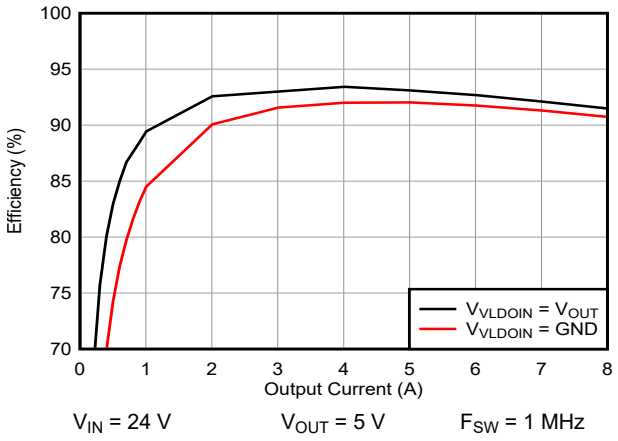
The LDO provides the VCC voltage from one of two inputs: V_{IN} or VLDOIN. When VLDOIN is tied to ground or below 3.1 V, the LDO derives power from V_{IN}. The LDO input becomes VLDOIN when VLDOIN is tied to a voltage above 3.1 V. The VLDOIN voltage must not exceed both V_{IN} and 12 V.

式 8 specifies the LDO power loss reduction as:

$$P_{LDO\text{-}LOSS} = I_{LDO} \times (V_{IN\text{-}LDO} - V_{VCC}) \quad (8)$$

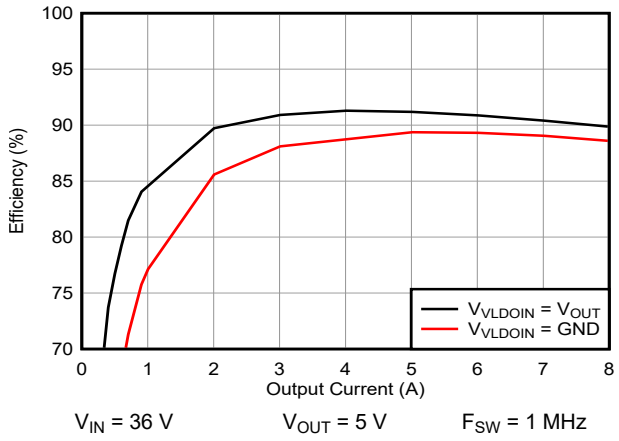
The VLDOIN input provides an option to supply the LDO with a lower voltage than V_{IN}, thus minimizing the LDO input voltage relative to VCC and reducing power loss. For example, if the LDO current is 10 mA at 1 MHz with V_{IN} = 24 V and V_{OUT} = 5 V, the LDO power loss with VLDOIN tied to ground is 10 mA × (24 V – 3.3 V) = 207 mW, while the loss with VLDOIN tied to V_{OUT} is equal to 10 mA × (5 V – 3.3 V) = 17 mW – a reduction of 190 mW.

図 7-6 and 図 7-7 show typical efficiency plots with and without VLDOIN connected to VOUT.



V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz

図 7-6. Efficiency Increase with External Bias



V_{IN} = 36 V V_{OUT} = 5 V F_{SW} = 1 MHz

図 7-7. Efficiency Increase with External Bias

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7.3.12 Overcurrent Protection (OCP)

The TPSM63610 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TPSM63610 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the TPSM63610 module is shut down and kept off for 40 ms (typical) before a restart is attempted. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, thus preventing overheating and potential damage to the device. After the fault is removed, the module automatically recovers and returns to normal operation.

7.3.13 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM63610 attempts to restart when the junction temperature falls to 159°C (typical).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM63610. When V_{EN} is below approximately 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 0.6 µA (typical). The TPSM63610 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal LDO for the VCC bias supply has a lower enable threshold than the regulator itself. When V_{EN} is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on after the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode

The TPSM63610 is in active mode when V_{VCC} and V_{EN} are above their relevant thresholds and no fault conditions are present. The simplest way to enable operation is to connect EN to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

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8 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM63610 synchronous buck module requires only a few external components to convert from a wide range of supply voltages to an output voltage at an output current up to 8 A. To expedite and streamline the process of designing a TPSM63610-based regulator, a comprehensive TPSM63610 quickstart calculator tool is available by download to assist the system designer with component selection for a given application.

8.2 Typical Applications

For the circuit schematic, bill of materials, PCB layout files, and test results of a TPSM63610-powered implementation, see the TPSM63610EVM.

8.2.1 Design 1 – High-Efficiency 8-A (10-A peak) Synchronous Buck Regulator for Industrial Applications

The following figure shows the schematic diagram of a 5-V, 8-A buck regulator with a switching frequency of 1 MHz. In this example, the target half-load and full-load efficiencies are 93.4% and 91.5%, respectively, based on a nominal input voltage of 24 V that ranges from 9 V to 36 V. A resistor R_{RT} of 15.8 kΩ sets the free-running switching frequency at 1 MHz. An optional SYNC input signal allows adjustment of the switching frequency from 500 kHz to 1.4 MHz for this specific application.

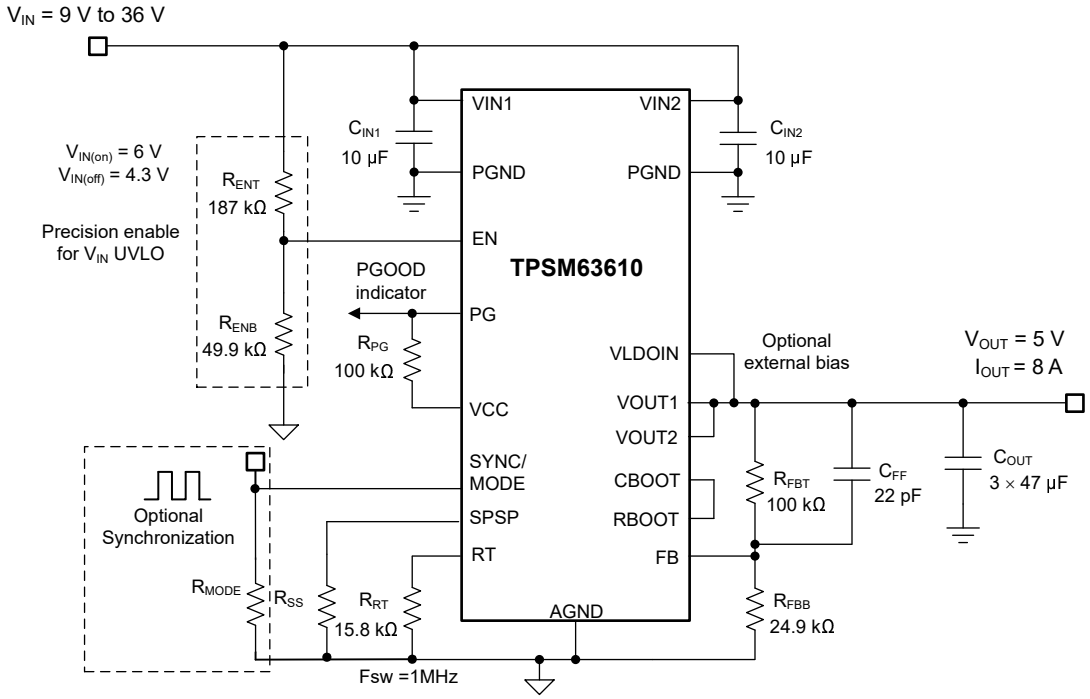


図 8-1. Circuit Schematic

8.2.1.1 Design Requirements

表 8-1 shows the intended input, output, and performance parameters for this application example. Note that if the input voltage decreases below approximately 6 V, the regulator operates in dropout with the output voltage below its 5-V setpoint.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	9 V to 36 V
Input voltage UVLO turn on, off	6 V, 4.3 V
Output voltage	5 V
Maximum output current	8 A
Switching frequency	1 MHz
Output voltage regulation	±1%
Module shutdown current	< 1 µA

表 8-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

表 8-2. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
C_{IN1}, C_{IN2}	2	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
			TDK	CNA6P1X7R1H106K
		10 µF, 50 V, X7S, 1210, ceramic	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_{OUT1}, C_{OUT2},C_{OUT3}	3	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GRM32ER70J476ME20K
			AVX	12106C476MAT2A
		47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
		100 µF, 6.3 V, X7S, 1210, ceramic	Murata	GRM32EC70J107ME15L
U_1	1	TPSM63610 36-V, 8-A synchronous buck module	Texas Instruments	TPSM63610RDLR

(1) See the *Third-Party Products Disclaimer*.

More generally, the TPSM63610 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63610 module with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.

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- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Setpoint

The output voltage of a TPSM63610 module is externally adjustable using a resistor divider. A recommended value for R_{FBT} of 100 kΩ for improved noise immunity compared to 1 MΩ and reduced current consumption compared to lower resistance values. Calculate R_{FBB} using the following equation:

$$R_{FBB} = \frac{R_{FBT} \times V_{REF}}{V_{OUT} - V_{REF}} \quad (9)$$

Choose the closest standard value of 24.9 kΩ for R_{FBB}.

8.2.1.2.3 Switching Frequency Selection

Connect a 15.8-kΩ resistor from RT to AGND to set a switching frequency of 1 MHz, which is designed for an output of 5 V as it establishes an inductor peak-to-peak ripple current in the range of 20% to 40% of the 8-A rated output current at a nominal input voltage of 24 V.

8.2.1.2.4 Input Capacitor Selection

The TPSM63610 requires a minimum input capacitance of 2 × 10-µF ceramic, preferably with X7R dielectric. The voltage rating of input capacitors must be greater than the maximum input voltage. For this design, select two 10-µF, X7R, 50-V, 1210 case size, ceramic capacitors connected from VIN1 and VIN2 to PGND as close as possible to the module. See 図 8-18 for recommneded layout placement.

8.2.1.2.5 Output Capacitor Selection

From 表 7-1, the TPSM63610 requires a minimum of 33 µF of effective output capacitance for proper operation at an output voltage of 5 V at 2.2 MHz. Use high-quality ceramic type capacitors with sufficient voltage and temperature rating. If needed, connect additional output capacitance to reduce ripple voltage or for applications with specific load transient requirements.

For this design example, use three 47-µF, 6.3-V or 10-V, X7R, 1210, ceramic capacitors connected close to the module from the VOUT1 and VOUT2 pins to PGND. The total effective capacitance at 5 V is approximately 78 µF and 57 µF at 25°C and –40°C, respectively.

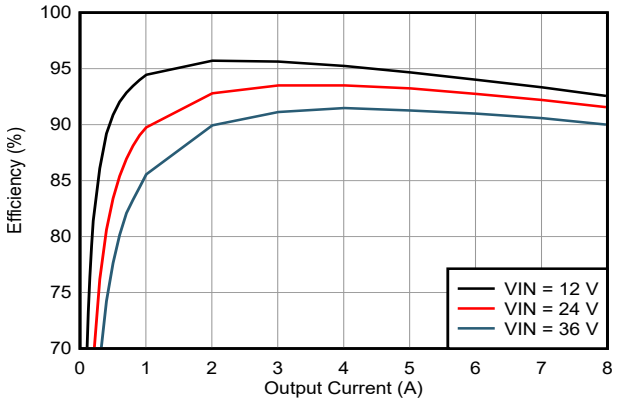
8.2.1.2.6 Other Connections

Short RBOOT to CBOOT and connect VLDOIN to the 5-V output for best efficiency. To increase phase margin when using an output capacitance close to the minimum in 表 7-1, a feedforward capacitor, designated as C_{FF} can be placed across the upper feedback resistor. Place the zero created by C_{FF} and R_{FBT} higher than one fifth the switching so that it boosts phase but does not significantly increase the crossover frequency. Because this C_{FF} capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 4.99-kΩ resistor, R_{FF}, must be placed in series with C_{FF}. If the ESR zero of the output capacitor is below 200 kHz, do not use CFF.

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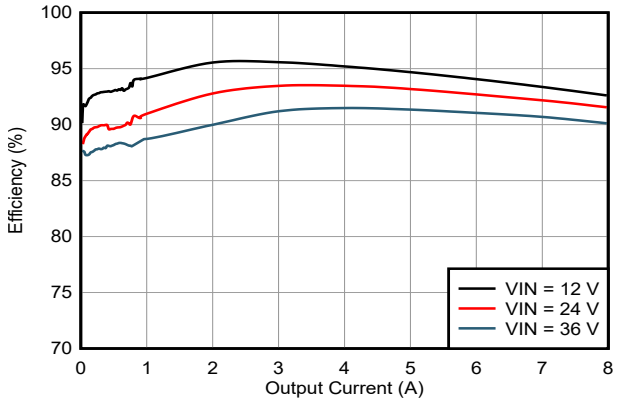
8.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 8 A, and F_{SW} = 1 MHz.



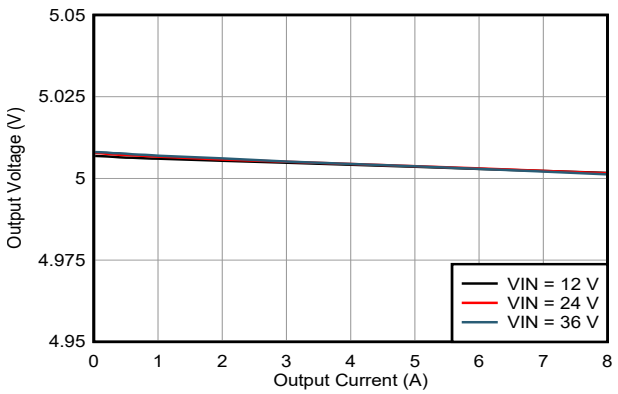
V_{OUT} = 5 V FPWM mode F_{SW} = 1 MHz

図 8-2. Efficiency for V_{OUT} = 5 V



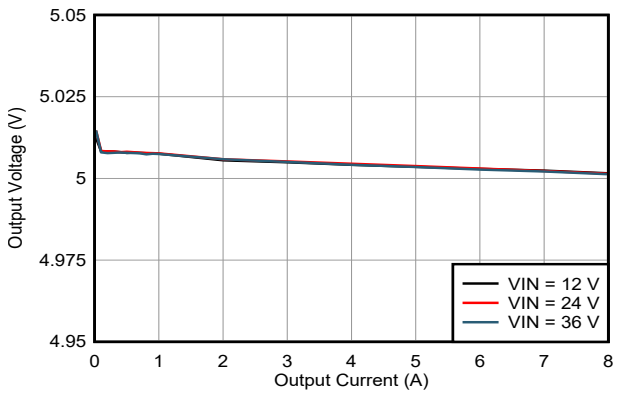
V_{OUT} = 5 V Auto mode F_{SW} = 1 MHz

図 8-3. Efficiency for V_{OUT} = 5 V



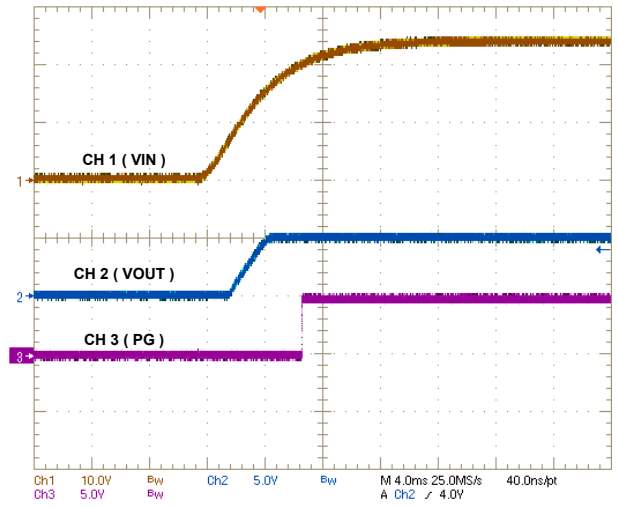
V_{OUT} = 5 V FPWM mode F_{SW} = 1 MHz

図 8-4. Load Regulation for V_{OUT} = 5 V



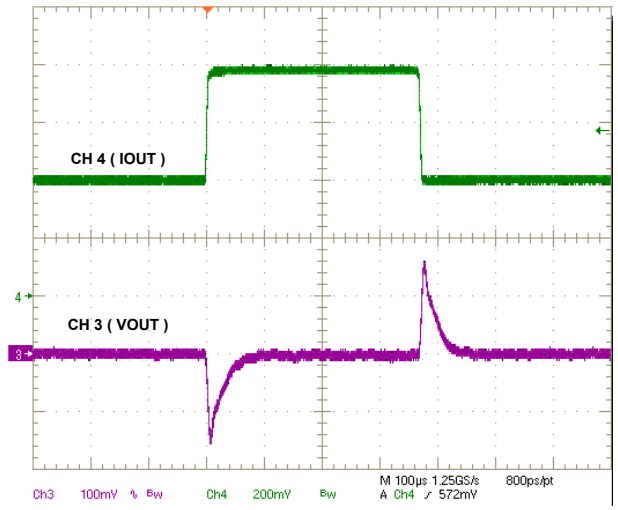
V_{OUT} = 5 V Auto mode F_{SW} = 1 MHz

図 8-5. Load Regulation for V_{OUT} = 5 V



V_{IN} = 24 V I_{OUT} = 6 A F_{SW} = 1 MHz

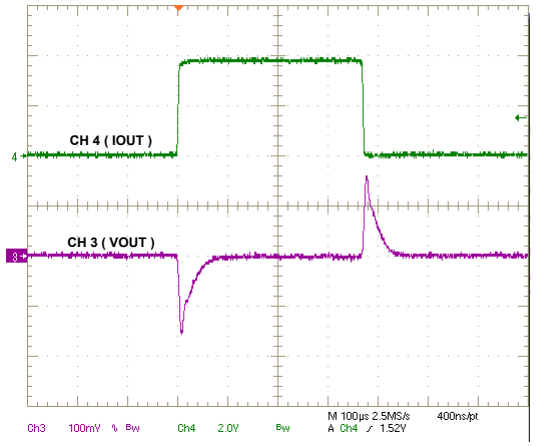
図 8-6. Start-up



V_{OUT} = 5 V FPWM mode F_{SW} = 1 MHz
T_R= T_F = 4 µs V_{IN} = 24 V Slew rate = 1 A/µs

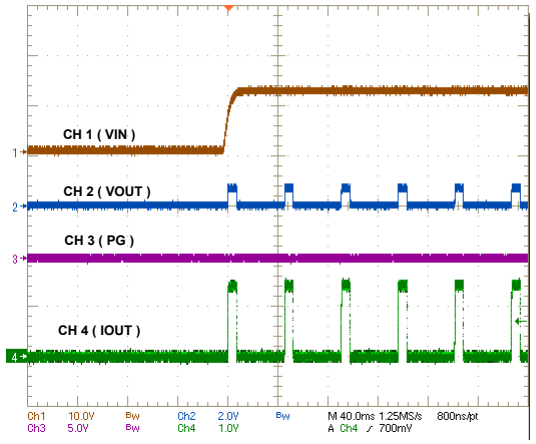
図 8-7. Load Transient, 4 A to 8 A, 1 A/µs

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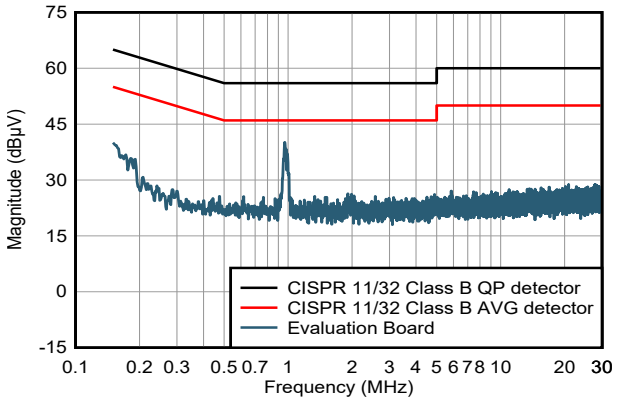
V_{OUT} = 5 V　　FPWM mode　　F_{SW} = 1 MHz
T_R = T_F = 4 µs　　V_{IN} = 24 V　　Slew rate = 1 A/µs

図 8-8. Load Transient, 0 A to 4 A, 1 A/µs



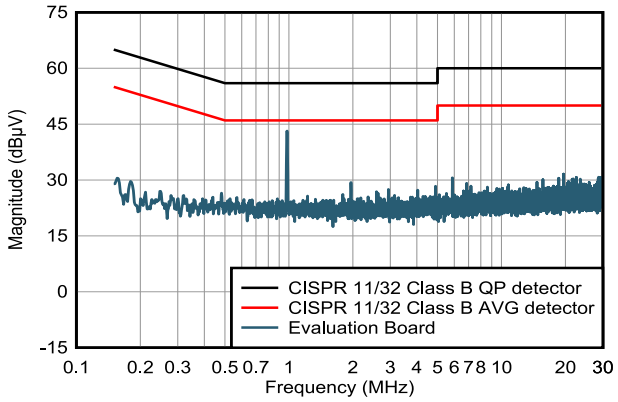
V_{OUT} = 5 V　　F_{SW} = 1 MHz

図 8-9. Start-up into Short Circuit



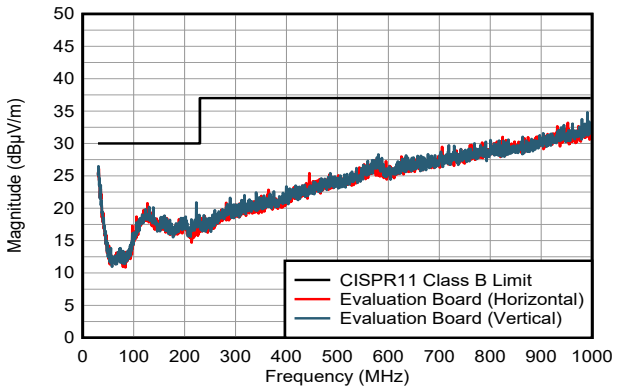
Default EVM　　V_{OUT} = 5 V　　F_{SW} = 1 MHz

図 8-10. CISPR 11/32 Class B Conducted Emissions: V_{IN} = 24 V, SPSP ON



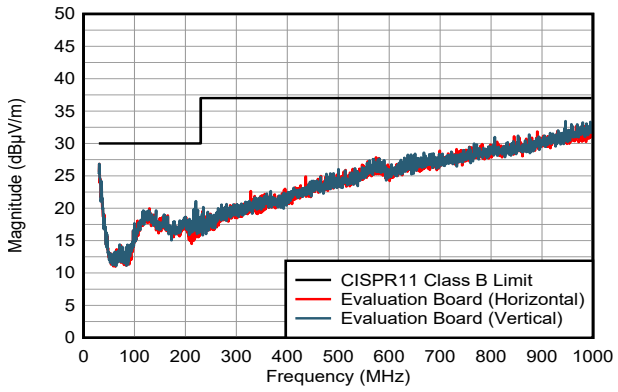
Default EVM　　V_{OUT} = 5 V　　F_{SW} = 1 MHz

図 8-11. CISPR 11/32 Class B Conducted Emissions: V_{IN} = 24 V, SPSP OFF



Additional 2 x 10pF C_{IN} with EMI filter removed　　V_{OUT} = 5 V　　F_{SW} = 1 MHz

図 8-12. CISPR 11 Class B Radiated Emissions: V_{IN} = 24 V, SPSP ON



Additional 2 x 10pF C_{IN} with EMI filter removed　　V_{OUT} = 5 V　　F_{SW} = 1 MHz

図 8-13. CISPR 11 Class B Radiated Emissions: V_{IN} = 24 V, SPSP OFF

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8.2.2 Design 2 – Inverting Buck-Boost Regulator with Negative Output Voltage

図 8-14 shows the schematic diagram of an inverting buck-boost (IBB) regulator with an output of –12 V and a switching frequency of 1 MHz with a nominal input voltage of 12 V that ranges from 9 V to 24 V.

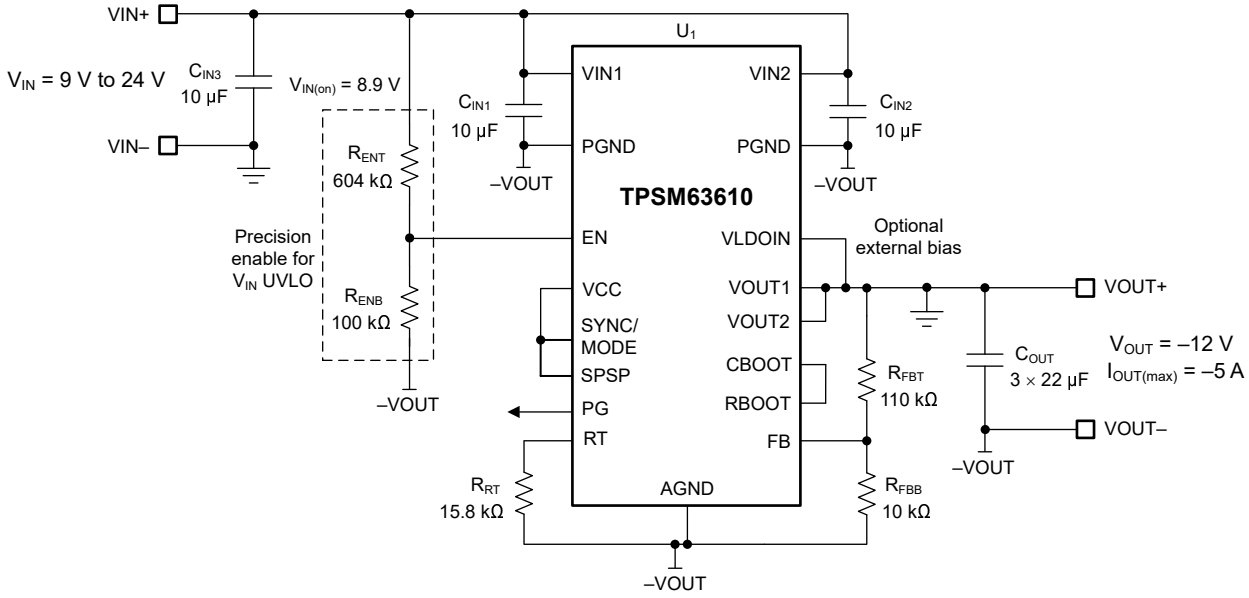


図 8-14. Circuit Schematic

8.2.2.1 Design Requirements

表 8-3 shows the intended input, output, and performance parameters for this application example. With an IBB topology, the module sees a total current of $I_{IN} + |–I_{OUT}|$, which is highest at minimum input voltage.

表 8-3. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	9 V to 24 V
Input voltage UVLO turn on	8.9 V
Output voltage	–12 V
Full-load current	–5 A
Switching frequency	1 MHz
Output voltage regulation	±1%

表 8-4 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

表 8-4. List of Materials for Application Circuit 2

REF DES	QTY	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
C_{IN1}, C_{IN2}, C_{IN3}	3	10 µF, 50 V, X7R, 1210, ceramic	Kemet	C1210C106K5RACTU
			TDK	CNA6P1X7R1H106K
C_{OUT1}, C_{OUT2}, C_{OUT3}	3	22 µF, 16 V, X7R, 1206, ceramic	Murata	GRM31CZ71C226ME15L
		22 µF, 25 V, X7R, 1210, ceramic	Murata	GRM32ER71E226ME15L
			AVX	12103C226KAT4A
		47 µF, 16 V, X6S, 1210, ceramic	Murata	GRM32EC81C476ME15L
U_1	1	TPSM63610 36-V, 8-A synchronous buck module	Texas Instruments	TPSM63610RDLR

(1) See the *Third-Party Products Disclaimer*.

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8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Voltage Setpoint

For an output voltage of –12 V, choose upper and lower feedback resistance of 110 kΩ and 10 kΩ, respectively, using Adjustable Output Voltage Equation.

8.2.2.2.2 IBB Maximum Output Current

The achievable output current with an *IBB topology* using the TPSM63610 is $I_{OUT(max)} = I_{LDC(max)} \times (1 - D)$, where $I_{LDC(max)}$ = 8 A is the rated current of the module and $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the IBB duty cycle. 図 8-15 provides the maximum output current capability as a function of input voltage for output voltage setpoints of –3.3 V, –5 V and –12 V.

8.2.2.2.3 Switching Frequency Selection

Connect a 15.8-kΩ resistor from RT to AGND to set a switching frequency of 1 MHz, which is designed for an output of –12 V.

8.2.2.2.4 Input Capacitor Selection

Use two 10-µF, 50-V, X7R-dielectric ceramic capacitors in 1210 case size connected symmetrically from the VIN1 and VIN2 pins to PGND as close as possible to the module. More specifically, these capacitors appear from the drain of the internal high-side MOSFET to the source of the low-side MOSFET, effectively connecting from the positive input voltage to the negative output voltage terminals.

The sum of the input and output voltages, $V_{IN} + |–V_{OUT}|$, is the effective applied voltage across the capacitors. The total effective capacitance at 25°C and input voltages of 12 V and 24 V (corresponding to applied voltages of 24 V and 36 V) is approximately 12 µF and 8 µF, respectively. Check the capacitance versus voltage derating curve in the capacitor data sheet.

Use an additional 10-µF, 50-V capacitor directly across the input. This capacitor is designated as C_{IN3} and connects across the VIN+ and VIN– terminals as shown in 図 8-14.

8.2.2.2.5 Output Capacitor Selection

For this IBB design example, use three 22-µF, 25-V, X7R-dielectric ceramic capacitors in 1210 case size connected symmetrically close to the module from the VOUT pins (Pin 9 and Pin 10) to PGND. The total effective capacitance is approximately 25 µF with DC bias of 12 V.

8.2.2.2.6 Other Considerations

Short RBOOT to CBOOT and connect VLDOIN to the power stage GND terminal, which corresponds to VOUT pins (Pin 9 and Pin 10) of the module, for best efficiency.

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8.2.2.3 Application Curves

Unless otherwise indicated, V_{IN} = 12 V, V_{OUT} = –12 V, and F_{SW} = 1 MHz.

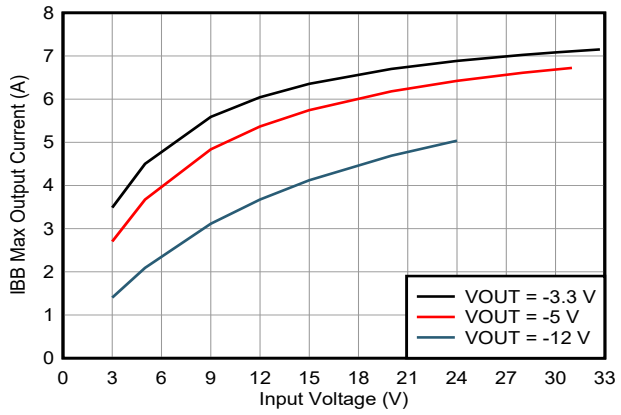


図 8-15. IBB Maximum Output Current

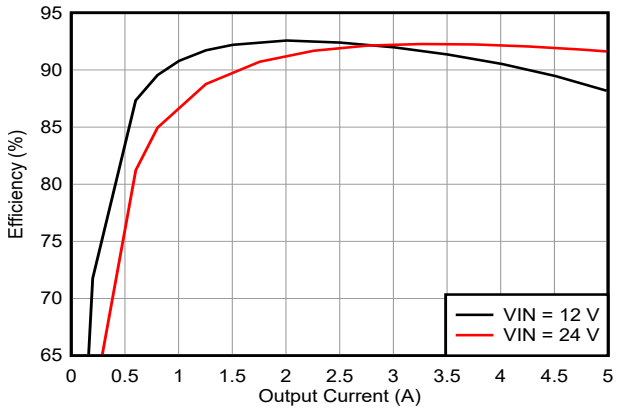


図 8-16. Efficiency for V_{OUT} = –12 V, FPWM Mode

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8.3 Power Supply Recommendations

The TPSM63610 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with 式 10.

$$I_{IN} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}\right) \quad (10)$$

where

- η is the efficiency.

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability or voltage transients each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

8.4 Layout

Proper PCB design and layout is important in high-current, fast-switching module circuits (with high internal voltage and current slew rates) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the module depends to a large extent on PCB layout.

8.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimze DC/DC module performance, including thermals and EMI signature. 図 8-17 and 図 8-18 show a recommended PCB layout for the TPSM63610 with optimized placement and routing of the power-stage and small-signal components.

- *Place input capacitors as close as possible to the VIN pins.* Note the dual and symmetrical arrangement of the input capacitors based on the VIN1 and VIN2 pins located on each side of the module package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.
  - Use low-ESR 1206 or 1210 ceramic capacitors with X7R or X7S dielectric. The module has integrated dual 0402 input capacitors for high-frequency bypass.
  - Ground return paths for the input capacitors must consist of localized top-side planes that connect to the PGND pads under the module.
  - Even though the VIN pins are connected internally, use a wide polygon plane on a lower PCB layer to connect these pins together and to the input supply.
- *Place output capacitors as close as possible to the VOUT pins.* A similar dual and symmetrical arrangement of the output capacitors enables magnetic field cancellation and EMI mitigation.
  - Ground return paths for the output capacitors must consist of localized top-side planes that connect to the PGND pads under the module.
  - Even though the VOUT pins are connected internally, use a wide polygon plane on a lower PCB layer to connect these pins together and to the load, thus reducing conduction loss and thermal stress.

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- *Keep the FB trace as short as possible by placing the feedback resistors close to the FB pin.* Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. FB is the input to the voltage-loop error anplifier and represents a high-impedance node sensitive to noise. Route a trace from the upper feedback resistor to the required point of output voltage regulation.
- *Use a solid ground plane on the PCB layer directly below the top layer with the module.* This plane acts as a noise shield by minimizing the magnetic fields associated with the currents in the switching loops. Connect AGND pins 6 and 11 directly to PGND pin 19 under the module.
- *Provide enough PCB area for proper heatsinking.* Use sufficient copper area to acheive a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heatsinking for the TPSM63610 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pads (PGND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce).

8.4.1.1 Thermal Design and Layout

For a DC/DC module to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The TPSM63610 module is available in a small 6.5-mm × 7.55-mm 22-pin QFN (RDL) package to cover a range of application requirements. The *Thermal Information* table summarizes the thermal metrics of this package with related detail provided by the *Semiconductor and IC Package Thermal Metrics application report*.

The 22-pin QFN package offers a means of removing heat through the exposed thermal pads at the base of the package. This allows a significant improvement in heatsinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and one or more ground planes to complete the heat removal subsystem. The exposed pads of the TPSM63610 are soldered to the ground-connected copper lands on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Preferably, use a four-layer board with 2-oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias with a 0.3-mm diameter connected from the thermal lands to the internal and solder-side ground planes are vital to promote heat transfer. In a multi-layer PCB stack-up, a solid ground plane is typically placed on the PCB layer below the power-stage components. Not only does this provide a plane for the power-stage currents to flow, but it also represents a thermally conductive path away from the heat-generating device.

8.4.2 Layout Example

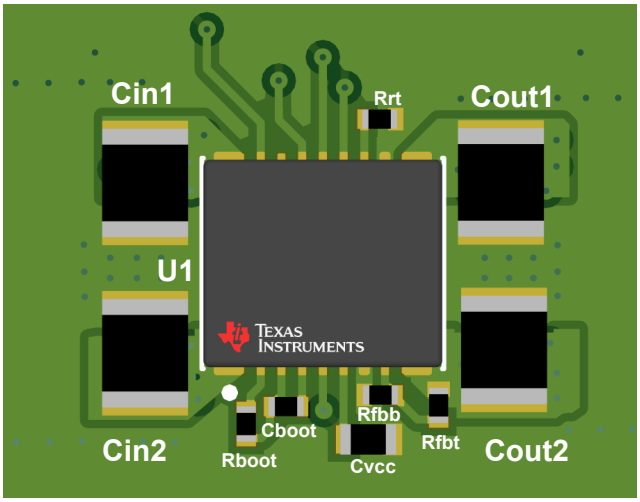


図 8-17. Typical Layout

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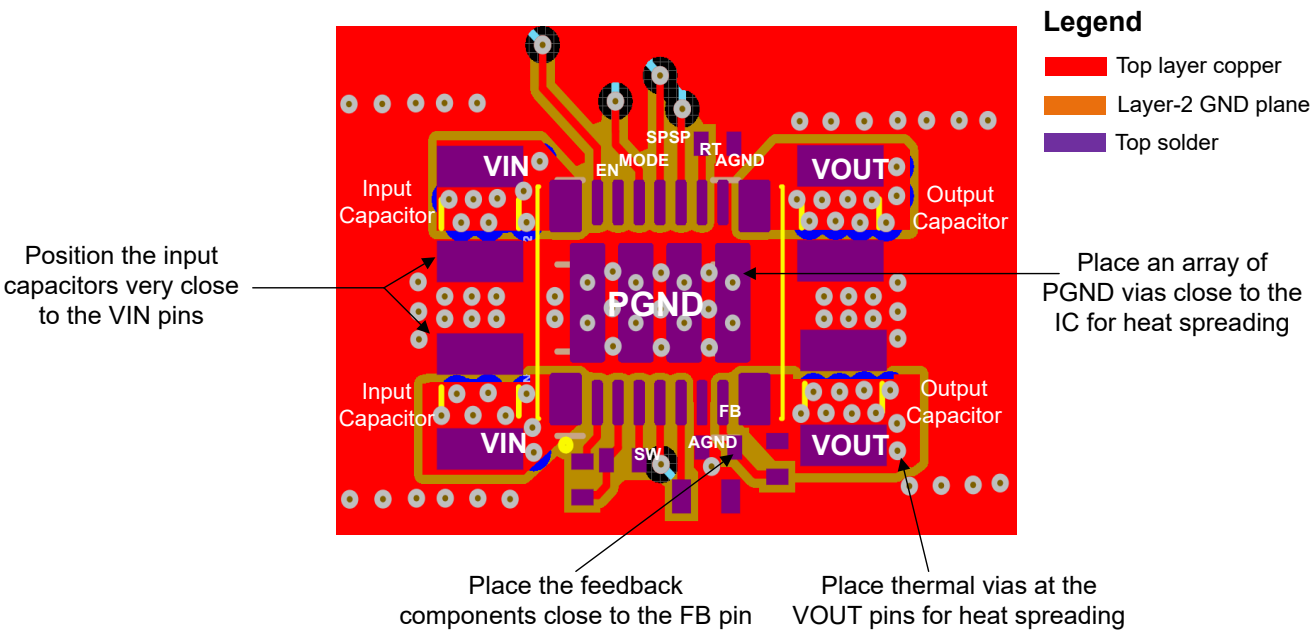


図 8-18. Typical Top Layer Design

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

With an input operating voltage from 3 V to 36 V and rated output current up to 10 A, the TPSM63610 family of synchronous buck power modules provides flexibility, scalability and optimized design size for a range of applications. These devices enable DC/DC designs with high density, low EMI and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS), RBOOT-configured switch-node slew rate control, and integrated input bypass capacitors.

表 9-1. Synchronous Buck DC/DC Power Module Family

DC/DC MODULE	RATED I_{OUT}	PACKAGE	DIMENSIONS	FEATURES	EMI MITIGATION
TPSM63610	8 A	B3QFN (22)	6.5 mm × 7.5 mm × 4 mm	RT adjustable F_{SW}, external synchronization,MODE adjustable (PFM/FPWM)	DRSS, RBOOT, integrated input, VCC and BOOT capacitors
TPSM63608	6 A				

For development support see the following:

- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-V_{IN}, –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*
- To view a related device of this product, see the LM61495 36-V, 10-A synchronous buck converter.

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63610 module with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

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Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Quick Reference Guide to TI Buck Switching DC/DC Application Notes* Compilation of Application Notes
- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application report

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision * (November 2022) to Revision A (December 2023)	Page
• 概要のテキストを更新	1
• Added junction temperature range in the *Absolute Maximum Ratings* table	6
• Added ambient temperature range in the *Recommended Operating Conditions* table	6
• Changed from EN/SYNC to EN	18
• Deleted /SYNC from EN pin description	22
• Deleted / from VEN	22
• Change from two to three 47-µF to account for de-rating of output capacitors	25

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM63610RDFR	Active	Production	B3QFN (RDF) | 22	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	63610
TPSM63610RDFR.A	Active	Production	B3QFN (RDF) | 22	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	63610
TPSM63610RDFRG4	Active	Production	B3QFN (RDF) | 22	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	63610
TPSM63610RDFRG4.A	Active	Production	B3QFN (RDF) | 22	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	63610

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

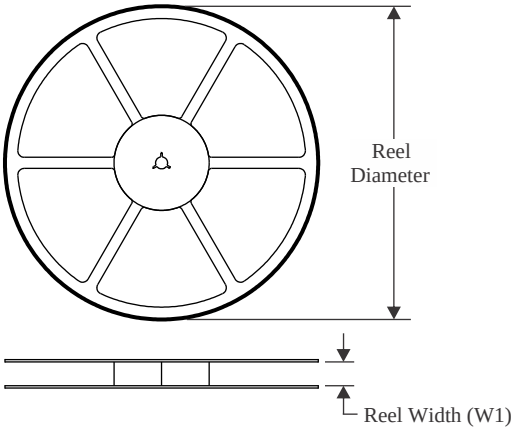
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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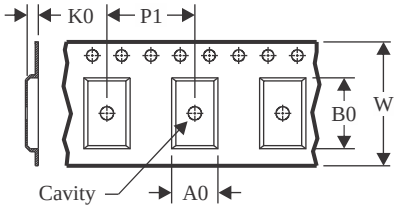
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

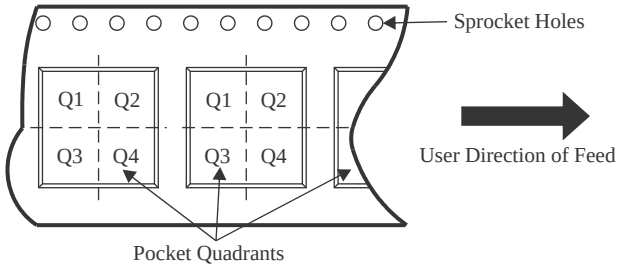


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

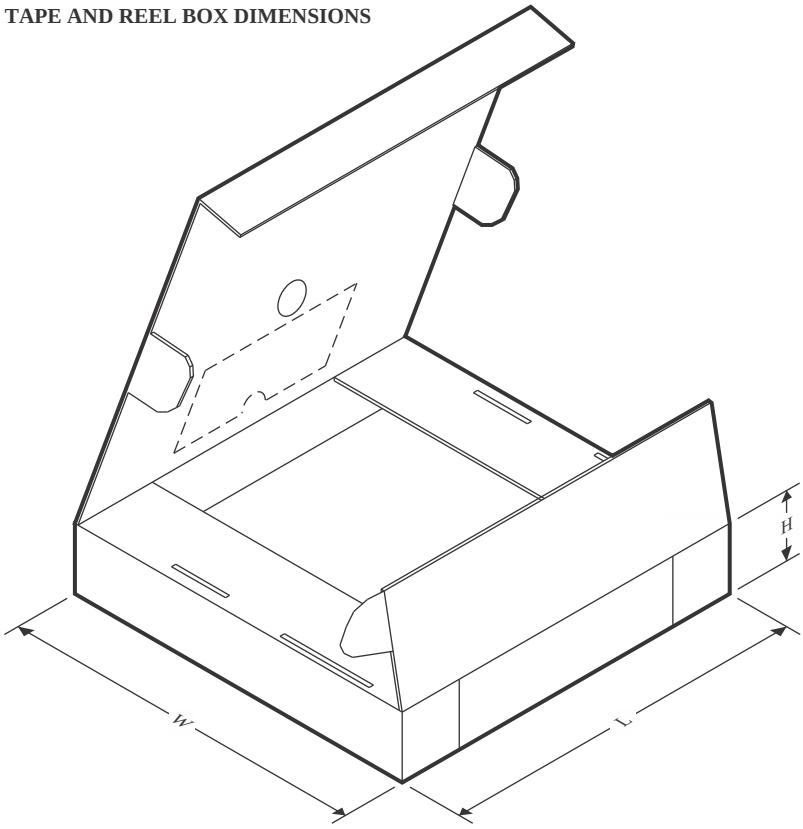
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM63610RDFR	B3QFN	RDF	22	1000	330.0	16.4	6.9	7.9	4.3	12.0	16.0	Q1
TPSM63610RDFRG4	B3QFN	RDF	22	1000	330.0	16.4	6.9	7.9	4.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

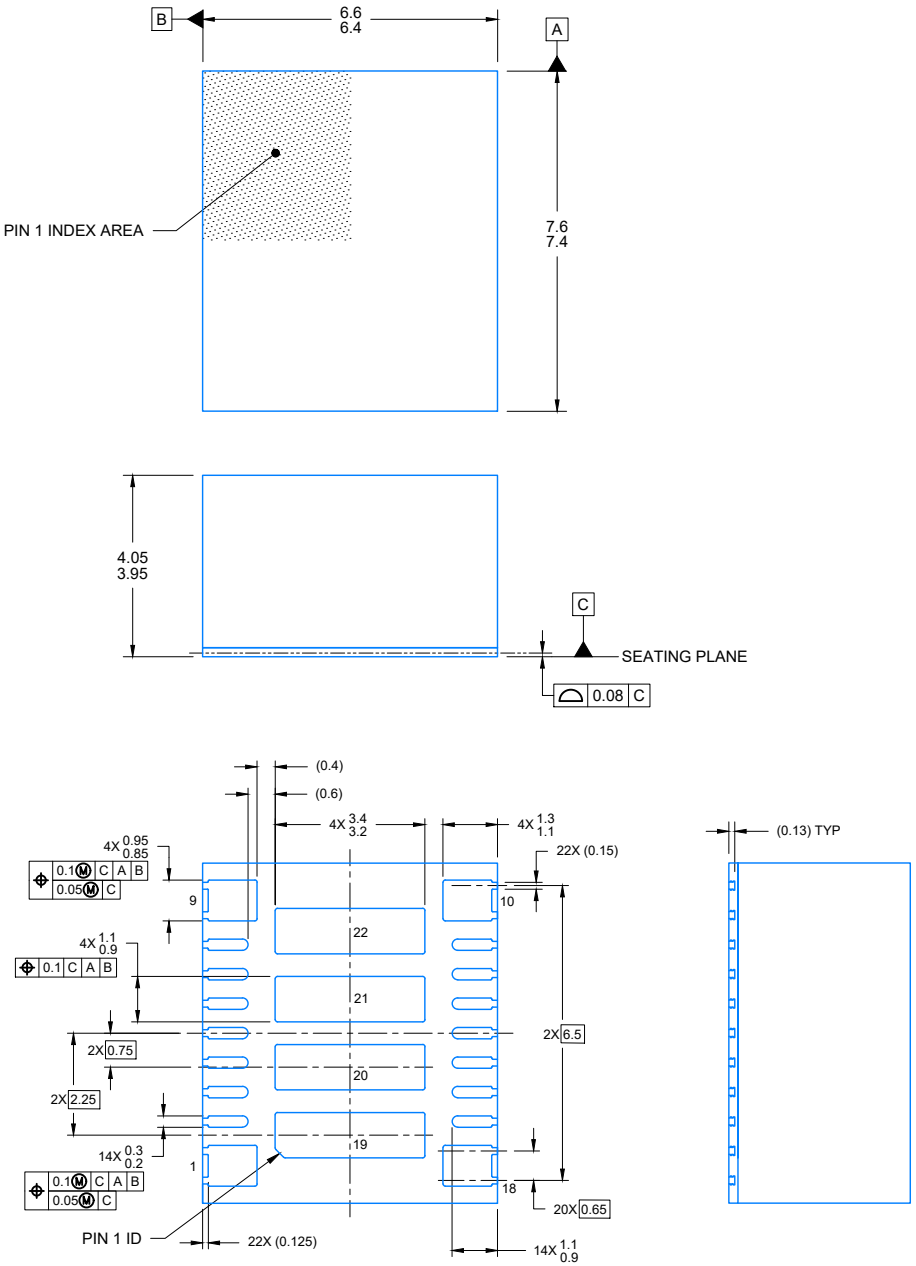
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM63610RDFR	B3QFN	RDF	22	1000	336.0	336.0	48.0
TPSM63610RDFRG4	B3QFN	RDF	22	1000	336.0	336.0	48.0

PACKAGE OUTLINE

RDF0022A

B3QFN - 4.05 mm max height

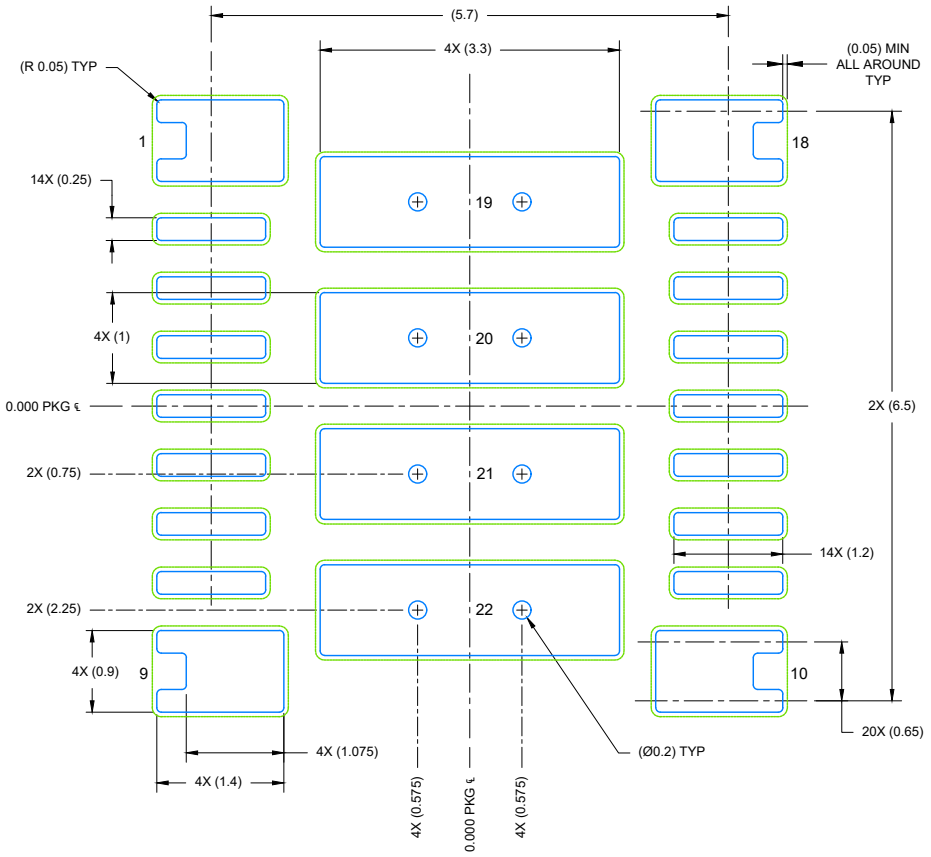
PLASTIC QUAD FLAT PACK- NO LEAD



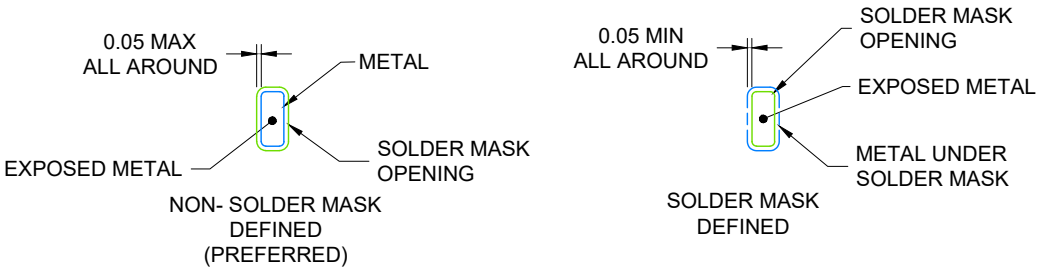
4226290/A 09/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

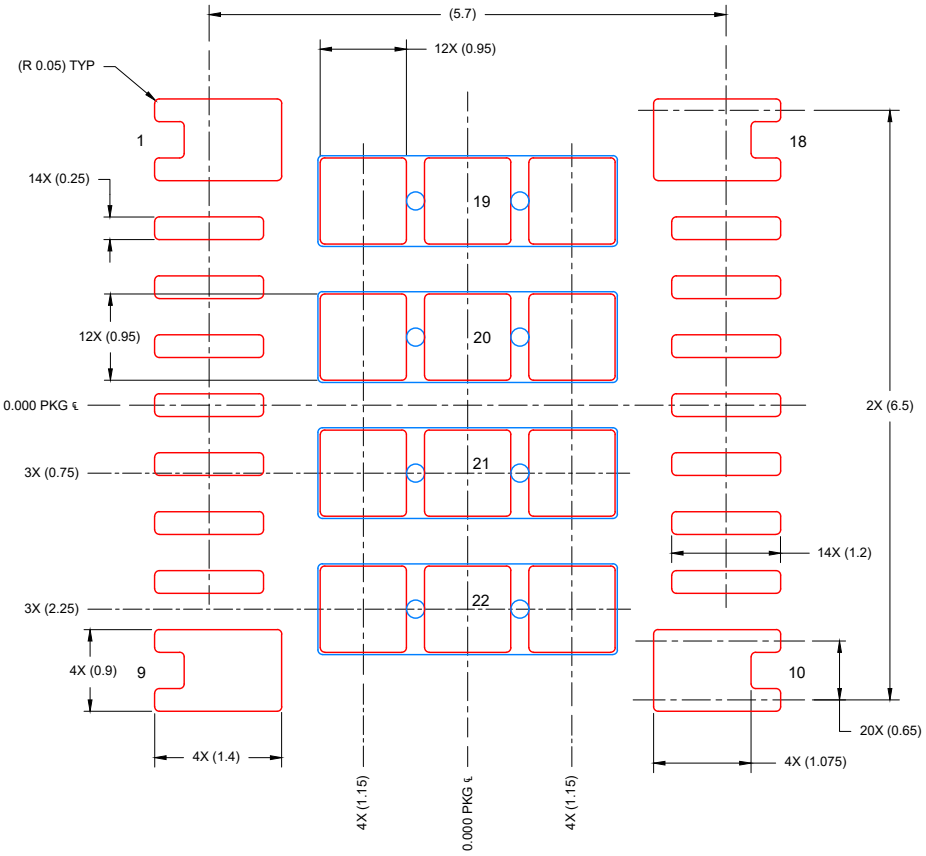


SOLDER MASK DETAILS

4226290/A 09/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE:
PIN 19 TO 22 : 82%

SCALE: 12X

4226290/A 09/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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