TPSM8281x 2.7V～6V 入力、4A/6A 降圧パワー モジュール、インダクタ内蔵、周波数同期機能付き、MicroSiP™ および MagPack™ パッケージ

1 特長

- 1.8MHz～4MHz の調整可能で同期可能なスイッチング周波数
- 拡散スペクトラム クロック処理 (オプション)
- 強制 PWM または PFM/PWM 動作を選択可能
- 出力電圧精度 ±1% (PWM 動作)
- 入力電圧範囲:2.7V～6V
- 出力電圧範囲:0.6V～5.5V
- 調整可能なソフト スタートまたはトラッキング
- ウィンドウ コンパレータによるパワー グッド出力
- 高精度の ENABLE 入力が可能
  - ユーザー定義の低電圧誤動作防止機能
  - 正確なシーケンシング
- 低 EMI 要件に対して最適化
  - ボンド ワイヤ パッケージなし
  - MagPack テクノロジーはインダクタと IC をシールド
  - 最適化されたピン配置によるレイアウトの簡素化
- 100% デューティ サイクル
- 出力放電
- 標準静止電流:18µA
- 動作温度範囲:-40℃～125℃
- パッケージの最大高さ:1.6mm (SIE) / 2.0mm (VCA)
- 優れた放熱対策
- 次のデバイスとピン互換
  - SIE:TPSM82813 (3A) および TPSM82810 (4A)
  - VCA (MagPack):TPSM82811 (1A)、TPSM82812 (2A)、TPSM82813 (3A)

2 アプリケーション

- 光モジュール、データ センターの相互接続
- 試験および測定機器
- メディカル モニタと診断
- ワイヤレス インフラ
- 航空宇宙および防衛

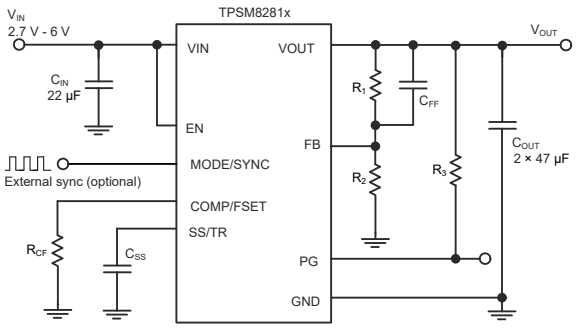
3 概要

TPSM8281x はピン互換で 1A、2A、3A、4A、および 6A の、高効率で使いやすい、インダクタ内蔵の同期整流降圧型 DC/DC パワー モジュールのファミリです。これらのデバイスは、固定周波数のピーク電流モードの制御トポロジに基づいています。高い電力密度と使いやすさが要件である、テレコミュニケーション、テストと測定、医療用アプリケーションで使用されます。抵抗値の低いスイッチにより、高い周囲温度でも最大 6A の連続出力電流を供給できます。スイッチング周波数は 1.8MHz～4MHz の範囲で外部から変更でき、同じ周波数範囲の外部クロックと同期することもできます。パワー セーブ モードでは、負荷が軽いとき TPSM8281x は自動的に PFM へ移行するため、負荷範囲全体にわたって高い効率が維持されます。TPSM8281x は PWM モードで 1% の出力電圧精度を実現するため、出力電圧精度の高い電源の設計に役立ちます。SS/TR ピンを使用して、スタートアップ時間を設定したり、出力電圧が外部ソースに追従するよう設定したりできます。この動作により、各種の電源レールの外部シーケンシングが可能で、スタートアップ時の突入電流が制限されます。

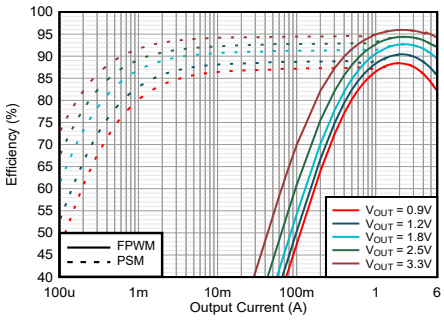
製品情報

部品番号(3)	出力電流	パッケージ(1)	本体サイズ (公称)
TPSM82814(2)	4A	VCA (QFN-FCMOD、13)	2.5mm × 3.0mm
TPSM82816	6A		
TPSM82816	6A	SIE (uSiP、14)	3.0mm × 4.0mm

(1) 詳細については、セクション 11 を参照してください。
(2) プレビュー情報 (量産データではありません)。
(3) デバイス比較表を参照してください。



回路図



TPSM82816PVCA の効率 (V_{IN} = 5V)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Device Comparison Table ... 3
5 Pin Configuration and Functions ... 4
6 Specifications ... 6
6.1 Absolute Maximum Ratings ... 6
6.2 ESD Ratings ... 6
6.3 Recommended Operating Conditions ... 6
6.4 Thermal Information ... 7
6.5 Electrical Characteristics ... 7
6.6 Typical Characteristics ... 9
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 15
8 Application and Implementation ... 17
8.1 Application Information ... 17
8.2 Typical Application ... 17
8.3 System Examples ... 25
8.4 Power Supply Recommendations ... 26
8.5 Layout ... 27
9 Device and Documentation Support ... 29
9.1 Device Support ... 29
9.2 Documentation Support ... 29
9.3 ドキュメントの更新通知を受け取る方法 ... 29
9.4 サポート・リソース ... 29
9.5 Trademarks ... 29
9.6 静電気放電に関する注意事項 ... 29
9.7 用語集 ... 29
10 Revision History ... 30
11 Mechanical, Packaging, and Orderable Information ... 30

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4 Device Comparison Table

DEVICE NUMBER(1)	OUTPUT CURRENT	SPREAD SPECTRUM CLOCKING	BODY SIZE (NOM)
TPSM82814PVCAR(2)	4 A	Set by COMP / FSET pin	2.5 mm × 3.0 mm × 1.95 mm
TPSM82816PVCAR	6 A		
TPSM82816SIER	6 A		3.0 mm × 4.0 mm × 1.6 mm

(1) For all available packages, see セクション 11.
(2) Preview information (not Production Data).

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5 Pin Configuration and Functions

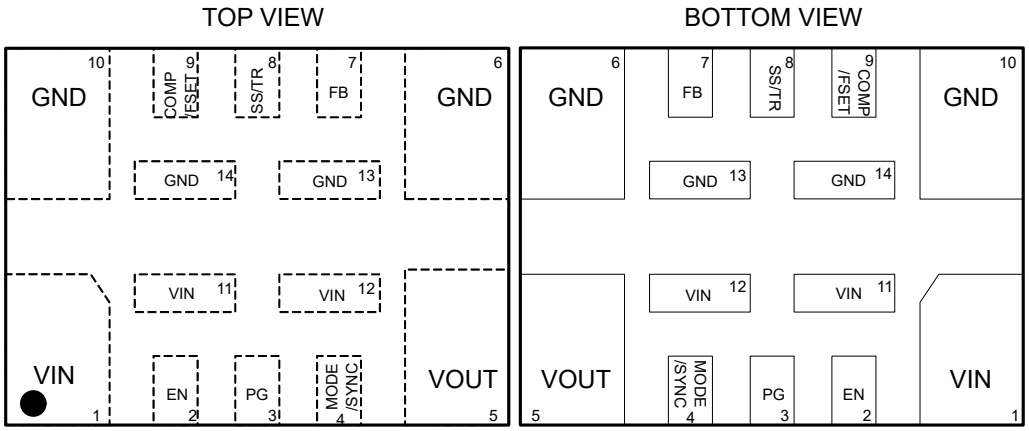


図 5-1. uSiP 14-Pin SIE Package

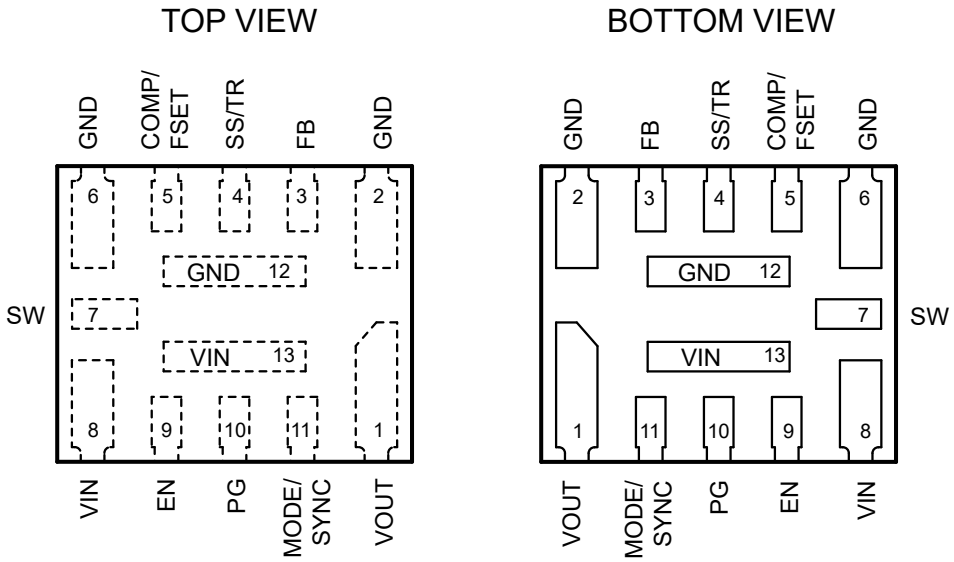


図 5-2. QFN-FCMOD 13-Pin VCA Package

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表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SIE	VCA		
EN	2	9	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	7	3	I	Voltage feedback input. Connect the output voltage resistor divider to this pin.
GND	6, 10, 13, 14	2, 6, 12		Ground pin
MODE/ SYNC	4	11	I	The device runs in PSM (auto PFM/PWM transition) mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See *Synchronizing to an External Clock*.
COMP/ FSET	9	5	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. The switching frequency is set to 2.25 MHz if the pin is tied to GND or VIN. Spread spectrum is also enabled and disabled by this pin. See *COMP/FSET*. Do not leave this pin unconnected.
PG	3	10	O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN.
SS/TR	8	4	I	Soft-start, tracking pin. A capacitor connected from this pin to GND defines the output voltage rise time. The pin can also be used as an input for tracking and sequencing - see *Voltage Tracking*.
VOUT	5	1		Output voltage pin. This pin is internally connected to the integrated inductor.
VIN	1, 11, 12	8, 13		Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins.
SW	—	7	O	Switch pin of the power stage. This pin can be left floating.

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, MODE/SYNC	–0.3	6.5	V
	SW	–0.3	V_{IN}+0.3	V
	SW (transient for less than 10 ns)(3)	-3	10	V
	FB	–0.3	4	V
	COMP/FSET, PG, SS/TR, VOUT	–0.3	V_{IN} + 0.3	V
I_{SINK_PG}	Sink Current at PG pin		10	mA
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
I_{OUT}	Output current	0		6	A
C_{OUT}	Effective output capacitance(1)	32 × V / V_{OUT}		470	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
R_{CF}		4.5		100	kΩ
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.

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6.4 Thermal Information

THERMAL METRIC[1]		TPSM8281x				UNIT
		SIE (14 PINS)		VCA (13 PINS)		
		JEDEC 51-5	EVM	JEDEC 51-7	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.3	32.2	72.1	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29	n/a [2]	37.2	n/a [2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	n/a [2]	21.2	n/a [2]	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.7	7.2	(-0.4)[3]	(-1.9)[3]	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.2	12.7	20.8	10.1	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Not applicable to an EVM.
(3) The junction temperature is lower than the inductor temperature leading to a temperature increase towards the top of the package

6.5 Electrical Characteristics

Over operating junction remperature range (T_J = –40°C to +125°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching, MODE/SYNC = GND, V_{OUT} = 0.6 V		18	36	µA
I_{SD}	Shutdown current	EN = GND		0.15	90	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.45	2.6	2.7	V
		V_{IN} falling	2.1	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		180		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{IH,EN}$	Input threshold voltage	EN rising	1.05	1.1	1.15	V
$V_{IL,EN}$	Input threshold voltage	EN falling	0.96	1.0	1.05	V
$I_{IH,EN}$	Input leakage current into EN	EN = VIN or GND			125	nA
V_{IH}	Input-threshold voltage at MODE/SYNC		1.1			V
V_{IL}	Input-threshold voltage at MODE/SYNC				0.3	V
I_{IH}	Input leakage current into MODE/SYNC				250	nA
f_{SW}	PWM switching frequency range	MODE/SYNC = high	1.8	2.25	4	MHz
f_{SW}	PWM switching frequency	COMP/FSET = GND or V_{IN}	2.08	2.25	2.4	MHz
f_{SW}	PWM switching frequency tolerance	using a resistor from COMP/FSET to GND	–12%		12%	
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
t_{Sync_lock}	Time to lock to external frequency			50		µs
	Duty cycle of synchronization signal at MODE/SYNC		20%		80%	
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already	135	270	520	µs
t_{Ramp}	Output voltage ramp time, SS/TR pin open	I_{OUT} = 0 mA, time from device starts switching to power good; device not in current limit	90	150	220	µs
$I_{SS/TR}$	SS/TR source current		8	10	12	µA
$R_{DIS,SS/TR}$	Internal discharge resistance on SS/TR	EN = low	0.7	1.1	1.5	kΩ
	Tracking gain	V_{FB} / $V_{SS/TR}$		1		

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6.5 Electrical Characteristics (続き)

Over operating junction remperature range (T_J = –40°C to +125°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Tracking offset	V_{FB} when $V_{SS/TR}$ = 0 V		±1		mV
V_{TH_PG}	UVP Power-good threshold voltage; dc level	V_{OUT} rising (%V_{FB})	92%	95%	98%	
		V_{OUT} falling (%V_{FB})	87%	90%	93%	
V_{TH_PG}	OVP Power-good threshold voltage; dc level	V_{OUT} rising (%V_{FB})	107%	110%	113%	
		V_{OUT} falling (%V_{FB})	104%	107%	111%	
$V_{OL,PG}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.01	0.3	V
$I_{IH,PG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
$t_{PG,DLY}$	PG deglitch time	for a high level to low level transition on the Power-good output		40		µs
OUTPUT						
V_{FB}	Feedback voltage			0.6		V
	Feedback voltage accuracy	PWM mode, V_{IN} ≥ V_{OUT} + 1 V	–1%		1%	
		PFM mode, V_{IN} ≥ V_{OUT} + 1 V, V_{OUT} ≥ 1.5 V, Co,eff ≥ 47 µF	–1%		2%	
		PFM mode, V_{IN} ≥ V_{OUT} + 1 V, V_{OUT} < 1.5 V, Co,eff ≥ 68 µF	–1%		2.5%	
	Feedback voltage accuracy with voltage tracking	V_{IN} ≥ V_{OUT} + 1 V, $V_{SS/TR}$ = 0.3 V, PWM mode	–5%		5%	
$I_{IH,FB}$	Input leakage current into FB	V_{FB} = 0.6 V		1	70	nA
	Load regulation	PWM mode		0.05		%/A
R_{DIS}	Output discharge resistance			30	50	Ω
$t_{on,min}$	Minimum on-time of high-side FET	V_{IN} ≥ 3.3 V		45	67	ns
R_{DP}	Dropout resistance TPSM82816SIE	100% mode		27		mΩ
R_{DP}	Dropout resistance TPSM82814PVCA, TPSM82816PVCA	100% mode		23		mΩ
I_{LIMH}	High-side FET switch current limit TPSM82814	DC value, V_{IN} = 3 V to 6 V	5.3	7.2	8.4	A
I_{LIMH}	High-side FET switch current limit TPSM82816	DC value, V_{IN} = 3 V to 6 V	7.3	9.2	10.4	A
I_{LIMNEG}	Low-side FET negative current limit	DC value, MODE/SYNC = high		–3		A

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6.6 Typical Characteristics

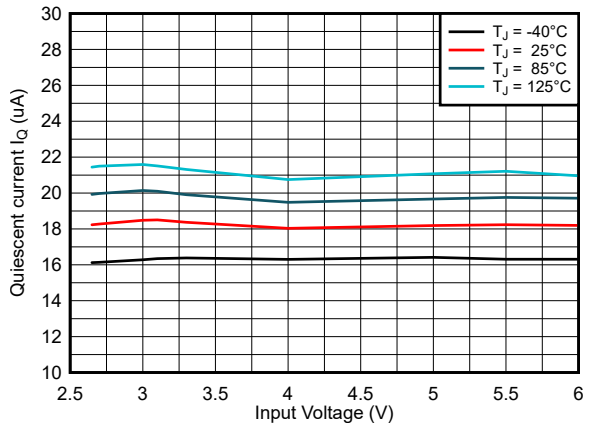


図 6-1. Quiescent Current

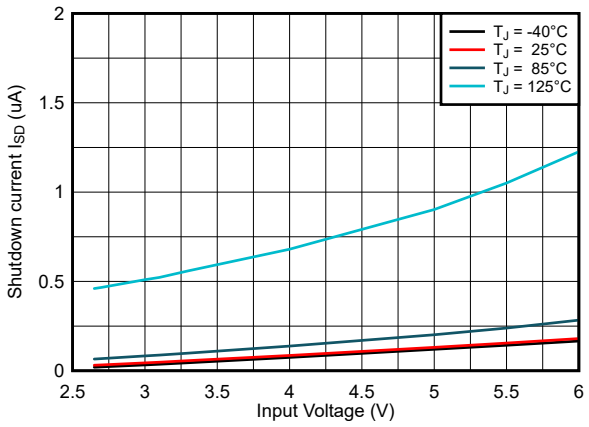


図 6-2. Shutdown Current

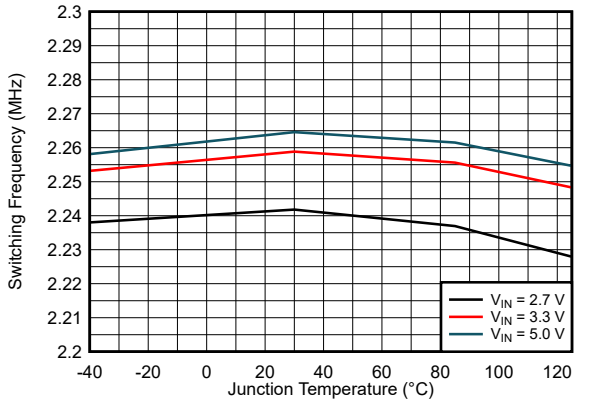


図 6-3. Oscillator Frequency (COMP/FSET = VIN)

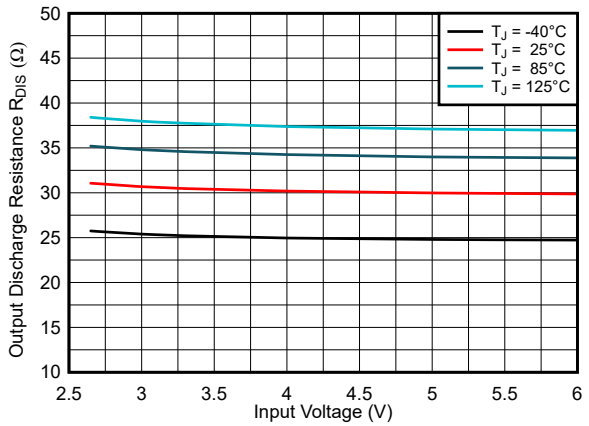


図 6-4. Discharge Resistance

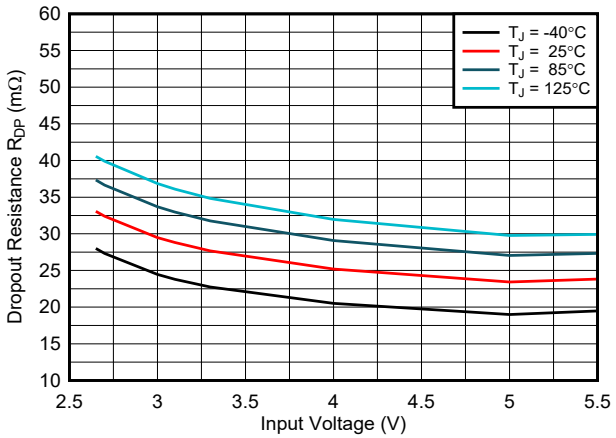


図 6-5. Dropout Resistance TPSM8281xPVCA

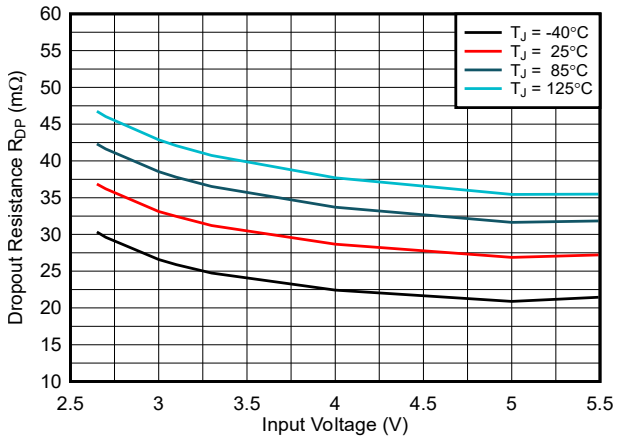


図 6-6. Dropout Resistance TPSM82816SIE

7 Detailed Description

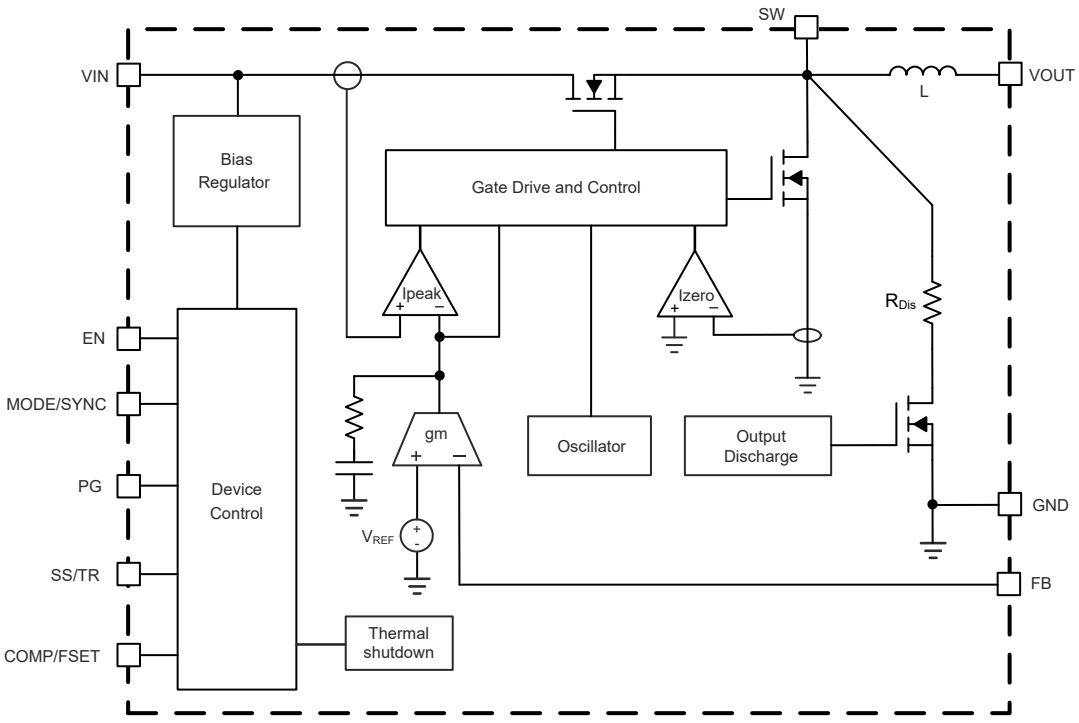
7.1 Overview

The TPSM8281x synchronous switch mode DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPSM8281x, one of two internal compensation settings can be selected. See *COMP/FSET*. The compensation setting is selected either by a resistor from COMP/FSET to GND or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The device supports forced fixed frequency operation (FPWM) with the MODE/SYNC pin tied to a logic high level. The frequency is defined as either 2.25 MHz (internally fixed when COMP/FSET is tied to GND or VIN) or in a range of 1.8 MHz to 4 MHz (defined by a resistor from COMP/FSET to GND). Alternatively, the device can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE/SYNC pin with no need for additional passive components. An internal PLL allows the device to change from internal clock to external clock during operation. The synchronization to the external clock is done on the falling edge of the clock applied at MODE/SYNC to the rising edge on the internal SW node. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PSM). At low output current, the device operates in PFM mode and automatically transitions to fixed-frequency PWM mode at higher output current. In PFM operation, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current (see *Power Save Mode Operation (PSM)* for more details).

The TPSM8281xP versions in the VCA package use MagPack technology to deliver the highest-performance power module design. Leveraging our proprietary integrated-magnetics MagPack packaging technology, these power modules deliver industry-leading power density, high efficiency and good thermal performance, ease of use, and reduced EMI emissions.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Precise Enable (EN)

The TPSM8281x starts operation when the rising EN threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off. The voltage applied at the EN pin of the TPSM8281x is compared to a fixed threshold of 1.1 V for a rising voltage.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin. The Precise Enable input also allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. See the *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal for more details.

7.3.2 Output Discharge

The purpose of the discharge function is to make sure of a defined down-ramp of the output voltage when the device is being disabled, but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPSM8281x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2 V. Output discharge is not activated during a current limit event.

7.3.3 COMP/FSET

This pin allows the user to set three different parameters independently:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable / disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at the start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency, but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency or compensation. Do not leave the pin floating.

The switching frequency has to be selected based on the maximum input voltage in the application and the output voltage to meet the specifications for the minimum on time.

Example: V_{IN} = 5.5 V, V_{OUT} = 1 V

$$f_{Sw,max} = \frac{V_{OUT}}{V_{IN} \times t_{ON,min}} = \frac{1\,V}{5.5\,V \times 67\,ns} = 2.71\,MHz \quad (1)$$

The compensation range has to be chosen based on the effective minimum capacitance used. The capacitance can be increased from the minimum value as given in 表 7-1, up to the maximum of 470 µF in both compensation ranges. If the capacitance of an output changes during operation, for example when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. If the output capacitance exceeds 72 µF × V / VOUT[V], use the second compensation setting to get the best load transient response. If the output capacitance only exceeds 32 µF × V / VOUT[V], use the first compensation setting. Compensating for large output capacitance but having too little effective capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

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For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

$$R_{CF}\left[k\Omega\right] = \frac{18\ MHz \times k\Omega}{f_S[MHz]} \quad (2)$$

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

$$R_{CF}\left[k\Omega\right] = \frac{60\ MHz \times k\Omega}{f_S[MHz]} \quad (3)$$

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:

$$R_{CF}\left[k\Omega\right] = \frac{180\ MHz \times k\Omega}{f_S[MHz]} \quad (4)$$

表 7-1. Switching Frequency and Compensation

COMPENSATION	R_{CF}	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE
For smallest output capacitance (comp setting 1) SSC disabled	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to 式 2	32 µF × V / V_{OUT}[V]
For smallest output capacitance (comp setting 1) SSC enabled	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to 式 3	32 µF × V / V_{OUT}[V]
For best transient response (larger output capacitance) (comp setting 2) SSC disabled	100 kΩ ... 45 kΩ	1.8 MHz (100 kΩ) ... 4 MHz (45 kΩ) according to 式 4	72 µF × V / V_{OUT}[V]
For smallest output capacitance (comp setting 1) SSC disabled	Tied to GND	Internally fixed 2.25 MHz	32 µF × V / V_{OUT}[V]
For best transient response (larger output capacitance) (comp setting 2) SSC enabled	Tied to V_{IN}	Internally fixed 2.25 MHz	72 µF × V / V_{OUT}[V]

The minimum output capacitance required for stability depends on the output voltage as stated in 表 7-1. Refer to *Output Capacitor* for further details on the output capacitance required depending on the output voltage.

A too-high resistor value for R_{CF} is decoded as "tied to V_{IN}" and a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in 表 7-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

7.3.4 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. When an external clock is applied, the device only operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. When using external synchronization, TI recommends to set the switching frequency (as set by R_{CF}) to a similar value as the externally applied clock. This action makes sure that, if the external clock fails, the switching frequency stays in the same range and the settling time to the internal clock is reduced. When there is no resistor from COMP/FSET to GND, but the pin is pulled high or low, external synchronization is not possible. An internal PLL allows you to change from an internal clock to external clock during operation. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin (see *Synchronizing to an External Clock*). The MODE/SYNC pin can be changed during operation.

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7.3.5 Spread Spectrum Clocking (SSC)

The device offers spread spectrum clocking as an option, set by the COMP/FSET pin. When SSC is enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized, the TPSM8281x follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

7.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

7.3.7 Power-Good Output (PG)

The device has a power-good output with window comparator. The PG pin goes high impedance after the FB pin voltage is above 95% and less than 107% of the nominal voltage, and is driven low after the voltage falls below 90% or rises higher than 110% of the nominal voltage (typical). 表 7-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pullup resistor connected to any voltage rail less than VIN. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND.

表 7-2. Power-Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN = High)	$0.95 \times V_{FB_NOM} \le V_{FB} \le 1.07 \times V_{FB_NOM}$	√	
	$V_{FB} < 0.9 \times V_{FB_NOM}$ or $V_{FB} > 1.1 \times V_{FB_NOM}$		√
Shutdown (EN = Low)			√
UVLO	$2\ V \le V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 2\ V$	undefined	

The PG pin has a 40-µs deglitch time on the falling edge. See 図 7-1.

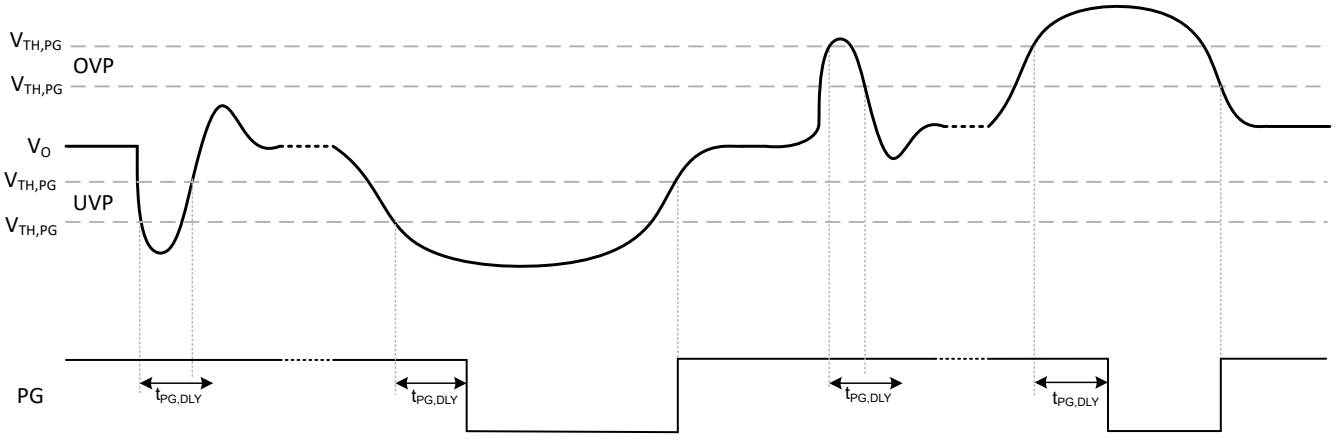


図 7-1. Power-Good Transient and Delay Behavior

7.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 180°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and

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PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM the thermal shutdown is not active.

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7.4 Device Functional Modes

7.4.1 Pulse Width Modulation (PWM) Operation

The TPSM8281x have two operating modes: Forced PWM mode (FPWM) and Power Save Mode (PSM).

With the MODE/SYNC pin set to high, the TPSM8281x operates with pulse width modulation (PWM) in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP/FSET pin to GND or by an external clock signal applied to the MODE/SYNC pin.

With the MODE/SYNC pin set to low, the TPSM8281x operates with pulse frequency modulation (PFM) during light load and automatically transitions into PWM as the load current increases.

7.4.2 Power Save Mode Operation (PSM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 1.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. The frequency set with the resistor on COMP/FSET must be in a range of 1.8 MHz to 3.5 MHz.

In power save mode, the switching frequency decreases linearly with the load current to maintain high efficiency. The linear behavior of the switching frequency in power save mode is shown in 図 7-2.

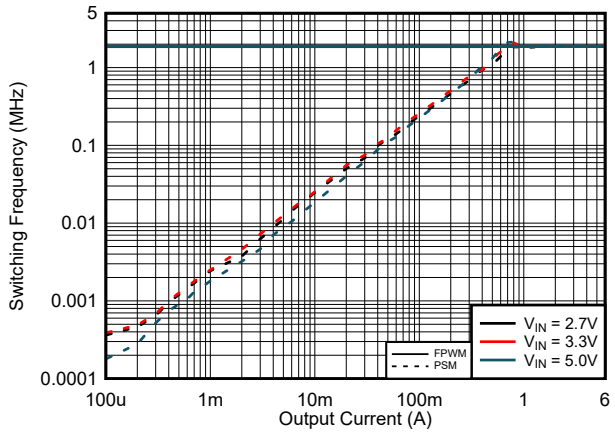


図 7-2. Switching Frequency versus Output Current (V_{OUT} = 1.8 V, R_{CF} = 10 kΩ)

7.4.3 100% Duty-Cycle Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. When the minimum off-time of typically 15 ns is reached, the TPSM8281x skips switching cycles while approaching 100% mode. In 100% mode, the high-side MOSFET switch is constantly turned on. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (5)$$

where:

- R_{DP} is the resistance from VIN to VOUT, which includes the high-side MOSFET on-resistance and DC resistance of the inductor
- $V_{OUT(min)}$ is the minimum output voltage the load can accept

This operation mode is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

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7.4.4 Current Limit and Short-Circuit Protection

The TPSM8281x is protected against overload and short circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak\ (typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (6)$$

where

- I_{LIMH} is the static current limit, as specified in the electrical characteristics
- L is the effective inductance
  - SIE: typically 220 nH
  - VCA (MagPack): typically 200 nH
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay of typically 50 ns

The dynamic peak current is calculated as follows:

$$I_{peak\ (typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \times 50\ ns \quad (7)$$

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in Forced PWM mode.

7.4.5 Soft Start / Tracking (SS/TR)

The soft-start circuitry controls the output voltage slope during start-up. This action avoids excessive inrush current and makes sure of a controlled output voltage rise time. This action also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high, the device starts switching after a delay of about 270 µs. Then V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

A capacitor connected from SS/TR to GND is charged with 10 µA by an internal current source during soft start until it reaches the reference voltage of 0.6 V. After reaching 0.6 V, the SS/TR pin voltage is clamped internally while the SS/TR pin voltage keeps rising to a maximum of about 3.3 V. The capacitance required to set a certain ramp-time (t_{ramp}) is:

$$C_{SS}[nF] = \frac{10\mu A \times t_{ramp}[ms]}{0.6\ V} \quad (8)$$

Leaving the SS/TR pin disconnected provides the fastest start-up ramp of 150 µs typically. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor of about 1.1 kΩ pulls the SS/TR pin to GND to make sure of a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at the SS/TR pin can also be used to track a controller voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PSM mode, the output voltage decreases based on the load current. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6 V). TI recommends to set the final value of the external voltage on SS/TR to be slightly above 0.6 V to make sure the device operates with the internal reference voltage when the power-up sequencing is finished. See *Voltage Tracking*.

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8 Application and Implementation

注

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8.1 Application Information

The TPSM8281x are synchronous step-down converter power modules. The power inductor is integrated inside the module. The SIE package variant has a shielded inductor with an inductance of 220 nH ±20%.

The VCA MagPack package not only has a 200nH shielded Inductor but also shields the IC for a better EMI performance. With its smaller package size, it also offers a higher power density compared to the SIE package. The 4A and 6A versions in the VCA package give the same efficiency and performance and are different only in their rated output current. The efficiency of the VCA package is up to 4% higher than the SIE package.

The TPSM82813SIL (3A), TPSM82810SIL (4A), and TPSM82816SIE (6A) are pin-to-pin compatible with each other. The TPSM82811PVCA (1A), TPSM82812PVCA (2A), TPSM82813PVCA (3A), TPSM82814PVCA (4A), and TPSM82816PVCA (6A) are also pin-to-pin compatible with each other.

8.2 Typical Application

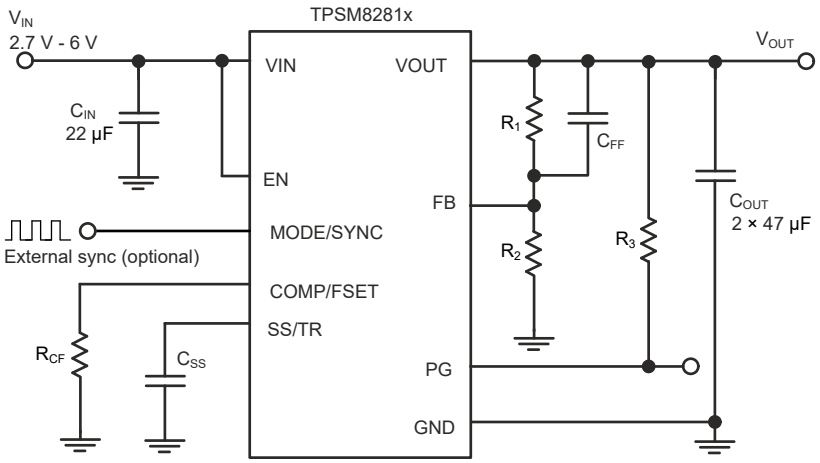


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

表 8-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPSM82816	Texas Instruments
C_{IN}	22 µF / X7R / 6.3 V; GRM21BZ1AJ226ME15L	Murata
C_{OUT} for V_{OUT} < 1 V	3 × 47 µF / X6S / 6.3 V; GRM21BC80J476ME01L	Murata
C_{OUT} for V_{OUT} ≥ 1 V	2 × 47 µF / X6S / 6.3 V; GRM21BC80J476ME01L	Murata
C_{SS}	4.7 nF	Any
R_{CF}	10 kΩ	Any
C_{FF}	10 pF	Any

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表 8-1. List of Components (続き)

REFERENCE	DESCRIPTION	MANUFACTURER (1)
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

(1) See the *Third-party Products Disclaimer*.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage of the TPSM8281x is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6 V to 5.5 V according to 式 9. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R_2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (9)$$

表 8-2. Examples for setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	Max C_{FF} at min C_{out}	OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	15 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	13 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	6.8 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	3.9 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	3.3 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	3.3 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	5.6 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	3 pF	3.315 V

8.2.2.2 Feedforward Capacitor

A feedforward capacitor (C_{FF}) is required in parallel with R_1 to improve the transient response. The maximum value for the feedforward capacitor C_{FF} at the minimum output capacitance is determined by 式 10:

$$C_{ff,\,max}\left[nF\right] = \frac{266.1\,nF \times \Omega}{R_1} \quad (10)$$

For examples of feedforward capacitor values for common output voltages when using the minimum required output capacitance, refer to 表 8-2.

To improve the load transient performance, more output capacitance can be added. Increasing the C_{FF} above values given by 式 10 can also improve the response with larger C_{OUT}. The converter's loop response must be evaluated either through a simple load step or by a phase margin measurement. For details, please refer to: *AN-1733 Load Transient Testing Simplified application note*.

8.2.2.3 Input Capacitor

For most applications, TI recommends a 22-µF nominal ceramic capacitor. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A X7R or X7T multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For applications with ambient temperatures below 85°C, a capacitor with X5R dielectric

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can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. The minimum required input capacitance is 5 µF.

8.2.2.4 Output Capacitor

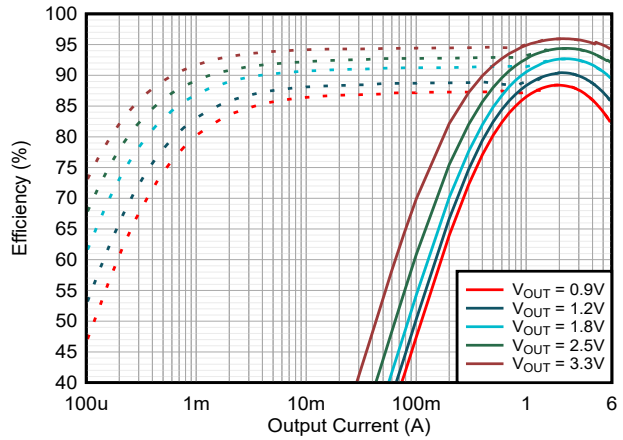
The architecture of the TPSM8281x allows the use of ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get a narrow capacitance variation with temperature, TI recommends to use an X7R or X7T dielectric. At temperatures below 85°C, an X5R dielectric can be used.

Using a higher capacitance value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in two steps based on the minimum capacitance used on the output. The maximum capacitance is 470 µF in any of the compensation settings. The minimum capacitance required on the output depends on the compensation setting and output voltage as shown in 表 7-1. For output voltages below 1 V, the minimum required capacitance increases linearly from 32 µF at 1 V to 53 µF at 0.6 V with the compensation setting for smallest output capacitance. The other compensation setting scales the same. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating.

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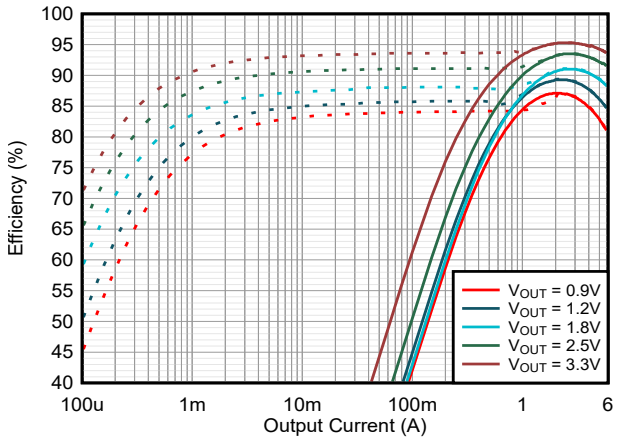
8.2.3 Application Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, 1.8 MHz, PWM mode, BOM = 表 8-1 unless otherwise noted.



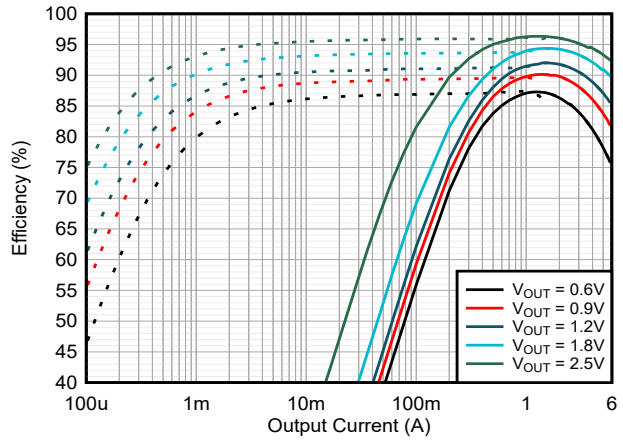
TPSM82816PVCA PSM and FPWM

図 8-2. Efficiency V_{IN} = 5.0 V and T_A = 25°C



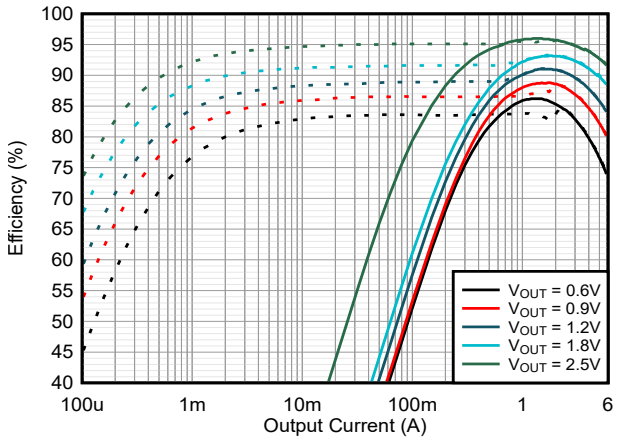
TPSM82816SIE PSM and FPWM

図 8-3. Efficiency V_{IN} = 5.0 V and T_A = 25°C



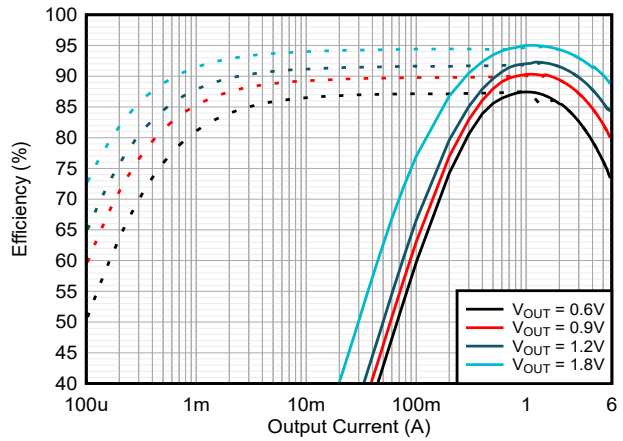
TPSM82816PVCA PSM and FPWM

図 8-4. Efficiency V_{IN} = 3.3 V and T_A = 25°C



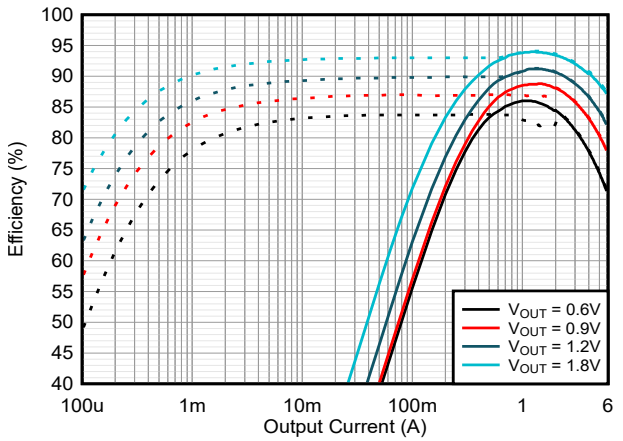
TPSM82816SIE PSM and FPWM

図 8-5. Efficiency V_{IN} = 3.3 V and T_A = 25°C



TPSM82816PVCA PSM and FPWM

図 8-6. Efficiency V_{IN} = 2.7 V and T_A = 25°C



TPSM82816SIE PSM and FPWM

図 8-7. Efficiency V_{IN} = 2.7 V and T_A = 25°C

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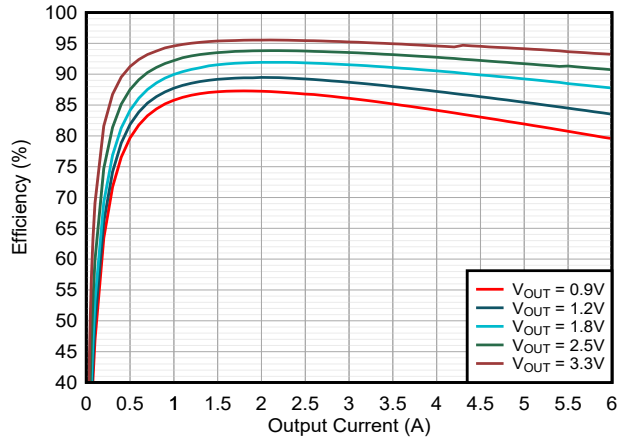


図 8-8. Efficiency V_{IN} = 5.0 V and T_A = 85°C

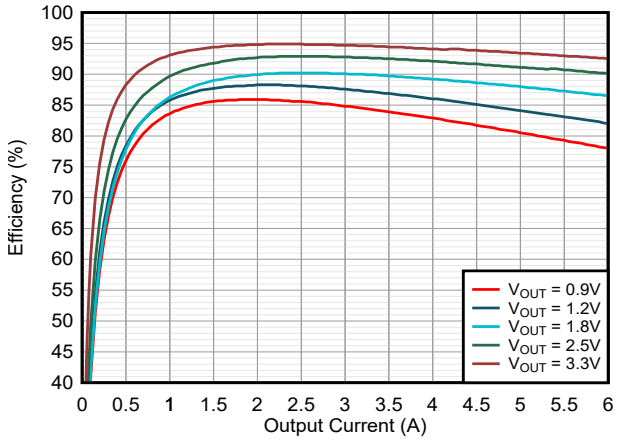


図 8-9. Efficiency V_{IN} = 5.0 V and T_A = 85°C

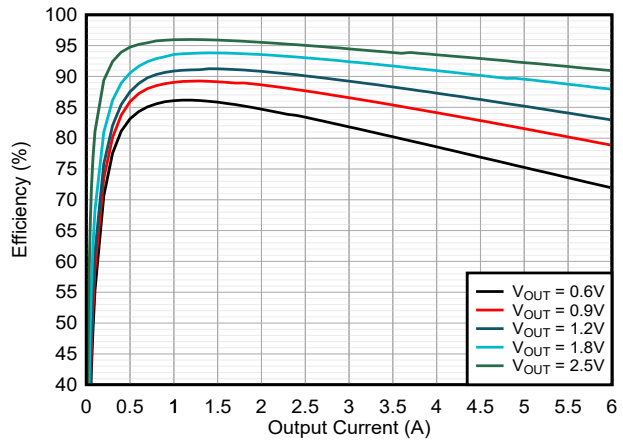


図 8-10. Efficiency V_{IN} = 3.3 V and T_A = 85°C

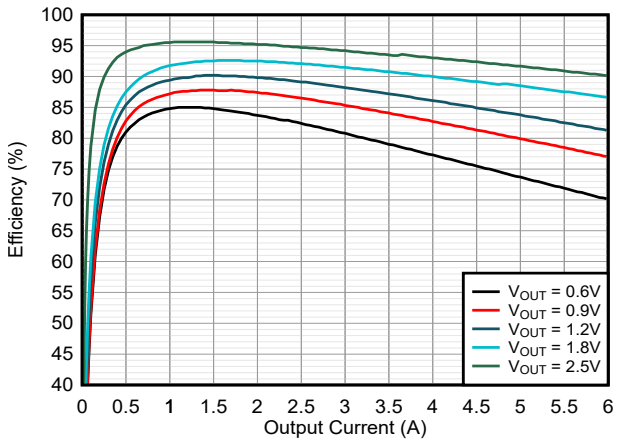


図 8-11. Efficiency V_{IN} = 3.3 V and T_A = 85°C

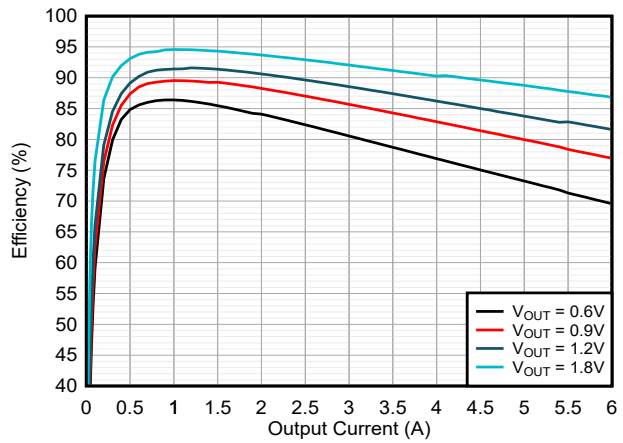


図 8-12. Efficiency V_{IN} = 2.7 V and T_A = 85°C

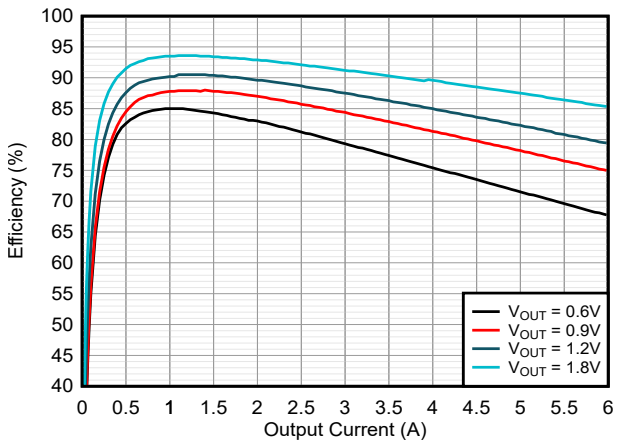
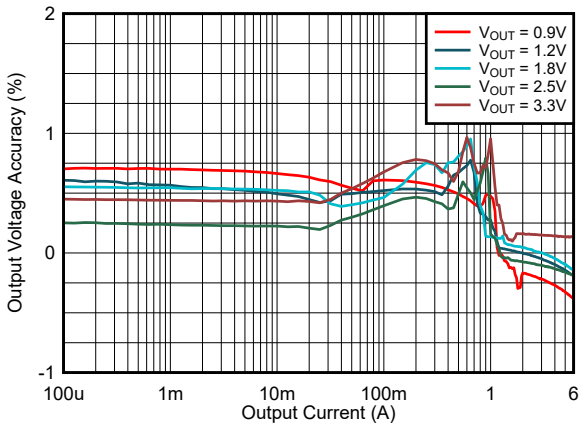


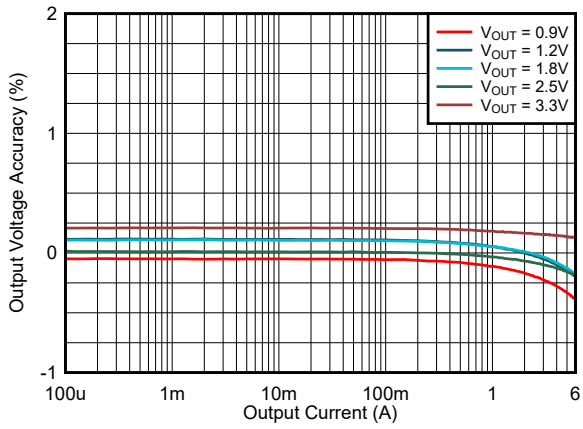
図 8-13. Efficiency V_{IN} = 2.7 V and T_A = 85°C

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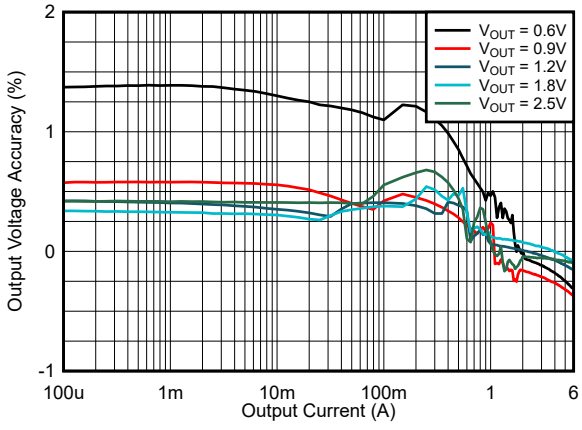
T_A = 25°C

図 8-14. Load Regulation V_{IN} = 5.0 V (PSM)



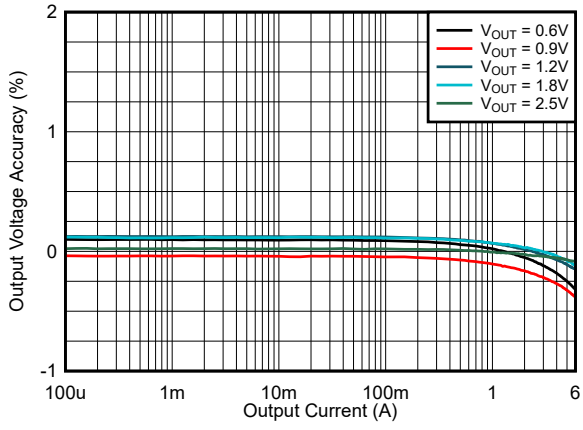
T_A = 25°C

図 8-15. Load Regulation V_{IN} = 5.0 V (FPWM)



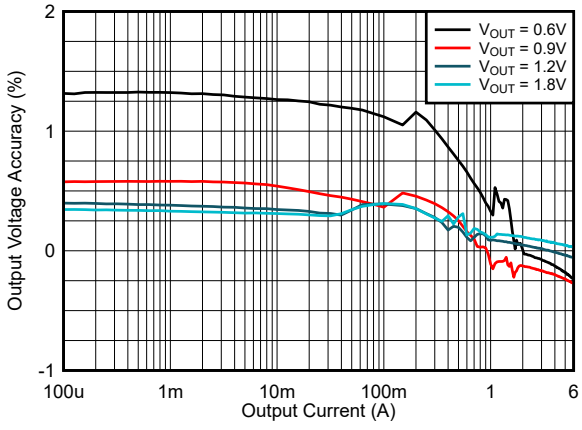
T_A = 25°C

図 8-16. Load Regulation V_{IN} = 3.3 V (PSM)



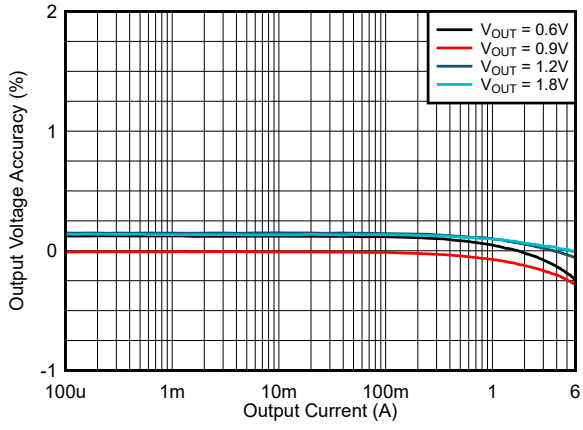
T_A = 25°C

図 8-17. Load Regulation V_{IN} = 3.3 V (FPWM)



T_A = 25°C

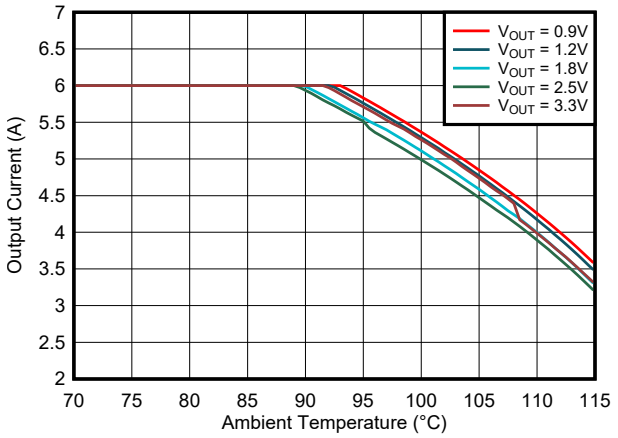
図 8-18. Load Regulation V_{IN} = 2.7 V (PSM)



T_A = 25°C

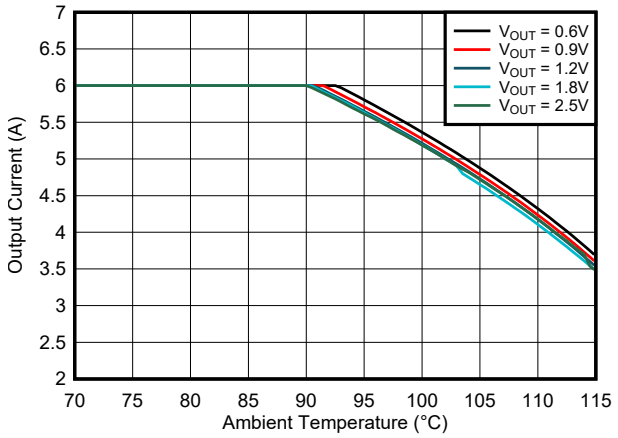
図 8-19. Load Regulation V_{IN} = 2.7 V (FPWM)

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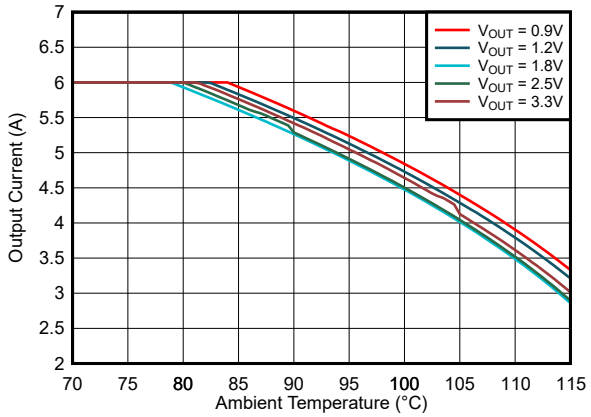
$R_{\theta JA}$ = 26.6°C/W f_{SW} = 1.8 MHz $T_{J,max}$ = 125 °C

図 8-20. TPSM82816PVCA Safe Operating Area V_{IN} = 5.0 V



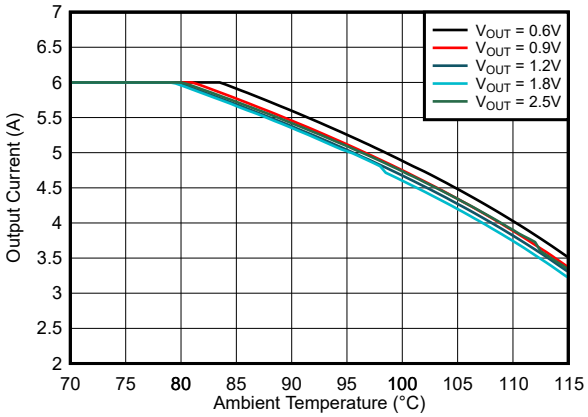
$R_{\theta JA}$ = 26.6°C/W f_{SW} = 1.8 MHz $T_{J,max}$ = 125 °C

図 8-21. TPSM82816PVCA Safe Operating Area V_{IN} = 3.3 V



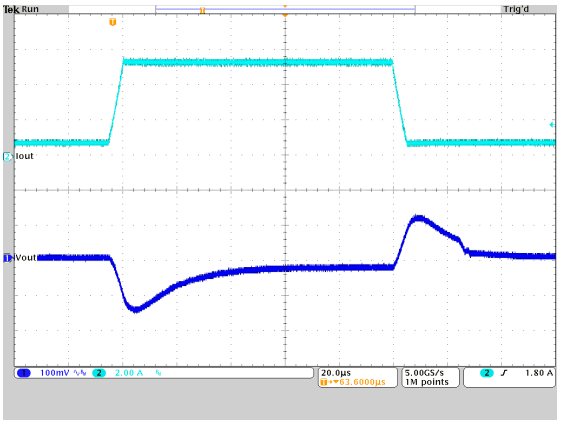
$R_{\theta JA}$ = 32.2 °C/W f_{SW} = 1.8 MHz $T_{J,max}$ = 125 °C

図 8-22. TPSM82816SIE Safe Operating Area V_{IN} = 5.0 V



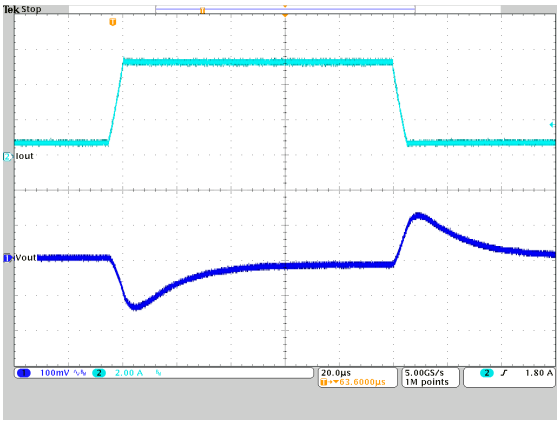
$R_{\theta JA}$ = 32.2 °C/W f_{SW} = 1.8 MHz $T_{J,max}$ = 125 °C

図 8-23. TPSM82816SIE Safe Operating Area V_{IN} = 3.3 V



V_{OUT} = 1.8 V PSM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

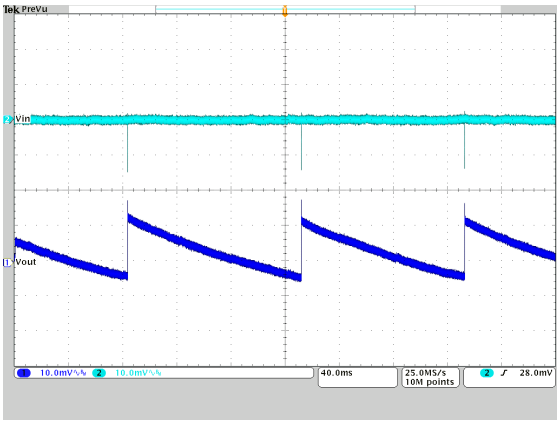
図 8-24. Load Transient Response



V_{OUT} = 1.8 V FPWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

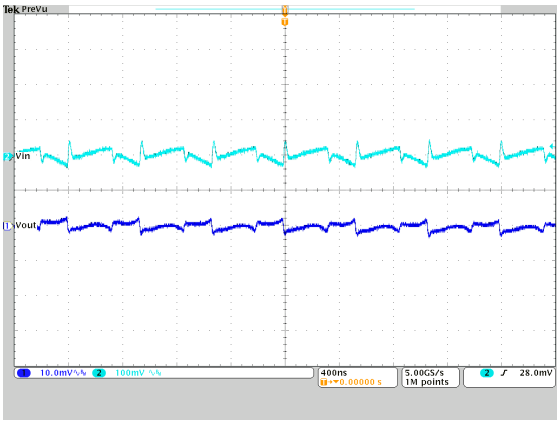
図 8-25. Load Transient Response

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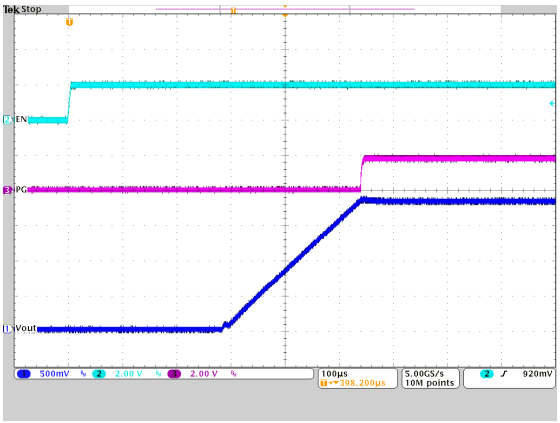
V_{OUT} = 1.8 V　PSM　T_A = 25 °C
I_{OUT} = 0 A　V_{IN} = 5.0 V　BW = 20 MHz

図 8-26. Output and Input Voltage Ripple



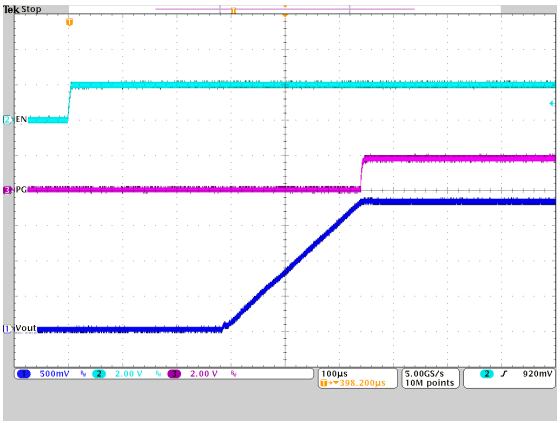
V_{OUT} = 1.8 V　PWM　T_A = 25°C
I_{OUT} = 4 A　V_{IN} = 5.0 V　BW = 20 MHz

図 8-27. Output and Input Voltage Ripple



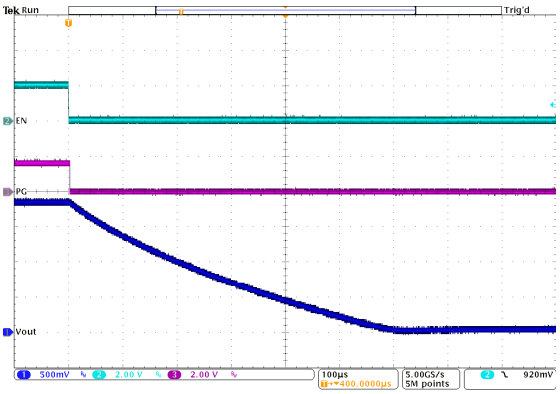
V_{OUT} = 1.8 V　PSM　T_A = 25°C
I_{OUT} = 0 A　V_{IN} = 5 V　C_{SS} = 4.7 nF

図 8-28. Start-Up Timing



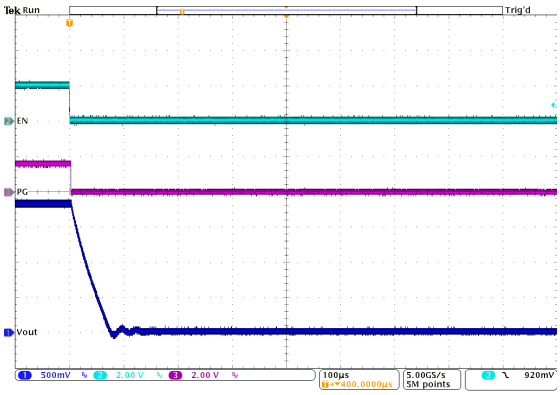
V_{OUT} = 1.8 V　FPWM　T_A = 25°C
I_{OUT} = 4 A　V_{IN} = 5 V　C_{SS} = 4.7 nF

図 8-29. Start-Up Timing



V_{OUT} = 1.8 V　PSM　T_A = 25°C
I_{OUT} = 0.1 A　V_{IN} = 5 V　C_{SS} = 4.7 nF

図 8-30. Shut-Down Timing



V_{OUT} = 1.8 V　FPWM　T_A = 25°C
I_{OUT} = 1A　V_{IN} = 5 V　C_{SS} = 4.7 nF

図 8-31. Shut-Down Timing

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8.3 System Examples

8.3.1 Voltage Tracking

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 図 8-32. From 0 V to 0.6 V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.6 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.6 V. The device achieves ratiometric, as shown in 図 8-33 or coincidental (simultaneous) output tracking, as shown in 図 8-33.

The R_2 value must be set properly to achieve accurate voltage tracking by taking the 10-µA charging current into account. 1 kΩ or smaller is a sufficient value for R_2. For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PSM. The resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light.

In case both devices need to run in forced PWM mode after start-up, TI recommends to tie the MODE/SYNC pin of the secondary device to the output voltage or the power-good signal of the primary device. The TPSM8281x has a duty cycle limitation defined by the minimum on time, which can cause the secondary device to not track when the output voltage is very low. Delaying FPWM mode until the output voltage is higher operates the device in PSM mode, with improved tracking at very low output voltages

When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin.

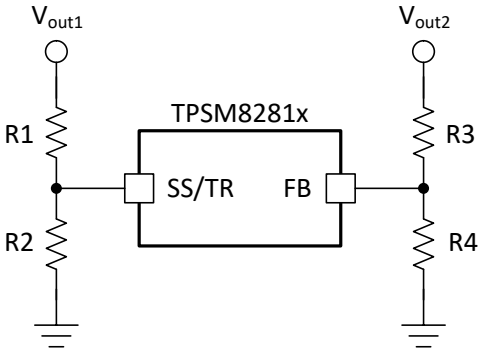


図 8-32. Schematic for Output Voltage Tracking

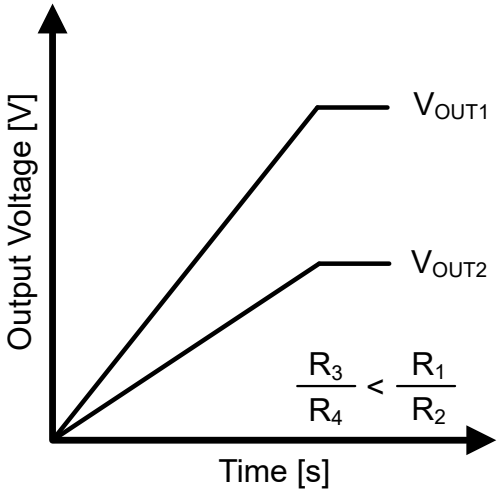


図 8-33. Ratiometric Voltage Tracking

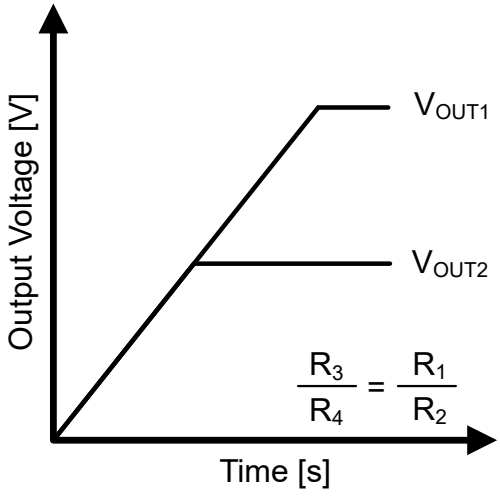


図 8-34. Coincidental Voltage Tracking

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8.3.2 Synchronizing to an External Clock

The TPSM8281x can be synchronized by applying a clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. See 図 8-35. The clock can be applied, changed, and removed during operation. TI recommends the value of the R_{CF} resistor be chosen such that the internally defined frequency and the externally-applied frequency are close to each other to have a fast settling time to the external clock. Synchronizing to a clock is not possible if the COMP/FSET pin is connected to Vin or GND. 図 8-36 and 図 8-37 show the external clock being applied and removed. When an external clock is applied, the device operates in PWM mode.

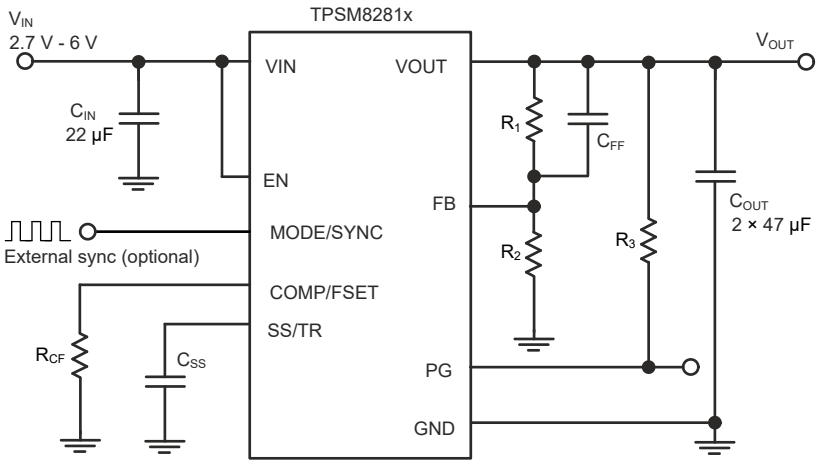
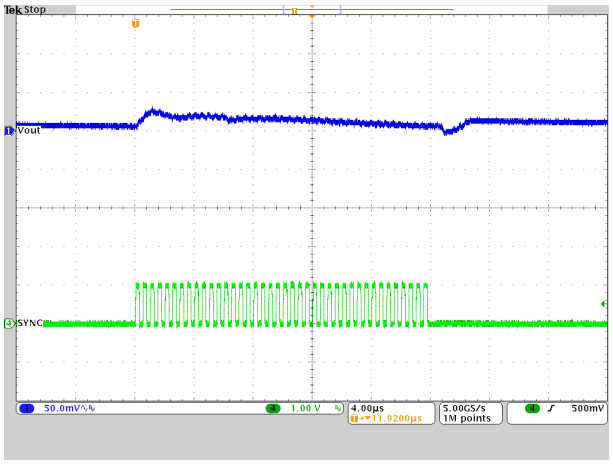
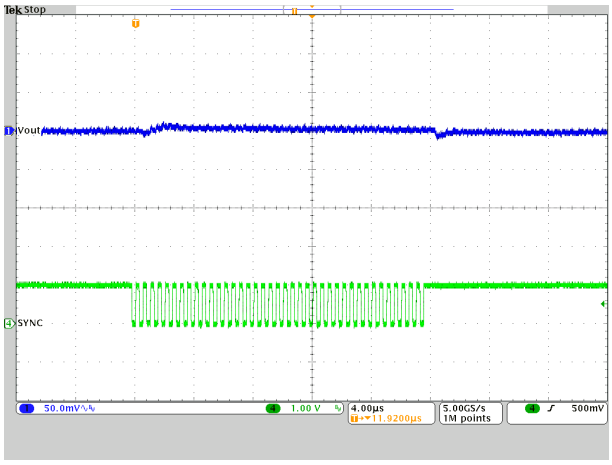


図 8-35. Frequency Synchronization



V_{IN} = 5 V R_{CF} = 10 kΩ I_{OUT} = 0.01 A
V_{OUT} = 1.8 V f_{EXT} = 2.0 MHz

図 8-36. Applying and Removing the Synchronization Signal (PSM)



V_{IN} = 5 V R_{CF} = 10 kΩ I_{OUT} = 1 A
V_{OUT} = 1.8 V f_{EXT} = 2.0 MHz

図 8-37. Applying and Removing the Synchronization Signal (FPWM)

8.4 Power Supply Recommendations

The TPSM8281x device family has no special requirements for the input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPSM8281x.

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8.5 Layout

8.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8281x demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- Place the input capacitor as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin and place C_{SS} close to the SS/TR pin to minimize noise pickup.
- Place the R_{CF} resistor close to the COMP/FSET pin to minimize the parasitic capacitance.
- Note that the recommended layout is implemented on the EVM and shown in the *TPSM8281xEVM-089 Evaluation Module* EVM user's guide, *MagPack™ Technology 3A/6A Power Module with Frequency Sync Evaluation Module* EVM user's guide, and in *Layout Example*.
- Note that the recommended land pattern for the TPSM8281x is shown at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

8.5.2 Layout Example

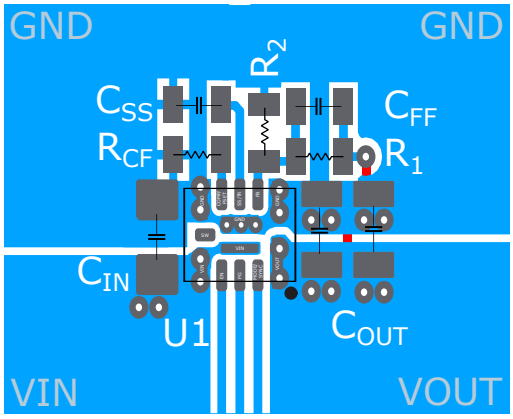


図 8-38. Example Layout VCA

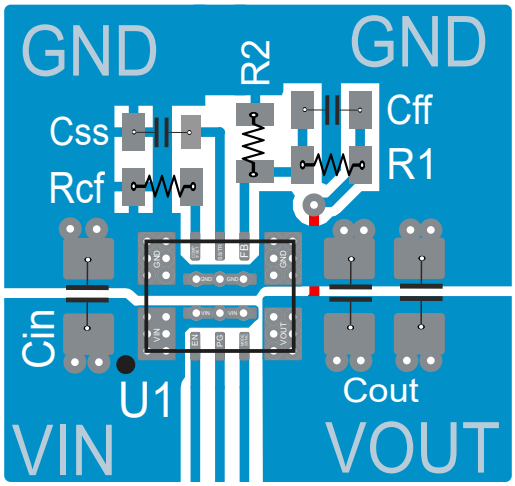


図 8-39. Example Layout SIE

8.5.2.1 Thermal Consideration

The TPSM8281x module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design
- Improve the thermal coupling of the component to the PCB
- Introduce airflow into the system

To estimate the approximate module temperature of the TPSM8281x, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

The thermal values in *Thermal Information* used the recommended land pattern, shown at the end of this data sheet, including the vias as shown. The TPSM8281x was simulated on a PCB defined by JEDEC 51-7. For the SIE package, the vias on the GND pins were connected to copper on other PCB layers, while the remaining vias were not connected to other layers.

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9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPSM8281xEVM-089 Evaluation Module EVM user's guide*
- Texas Instruments, *MagPack™ Technology 3A/6A Power Module with Frequency Sync Evaluation Module EVM user's guide*
- Texas Instruments, *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin analog design journal*
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter analog design journal*
- Texas Instruments, *AN-1733 Load Transient Testing Simplified application report*
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal*
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application note*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2024) to Revision B (December 2024)	Page
• TPSM82816PVCAR を「事前情報」から「量産データ」に変更	1

Changes from Revision * (December 2022) to Revision A (June 2024)	Page
• データシートに TPSM82814PVCAR (製品プレビュー) および TPSM82816PVCAR (事前情報) を追加	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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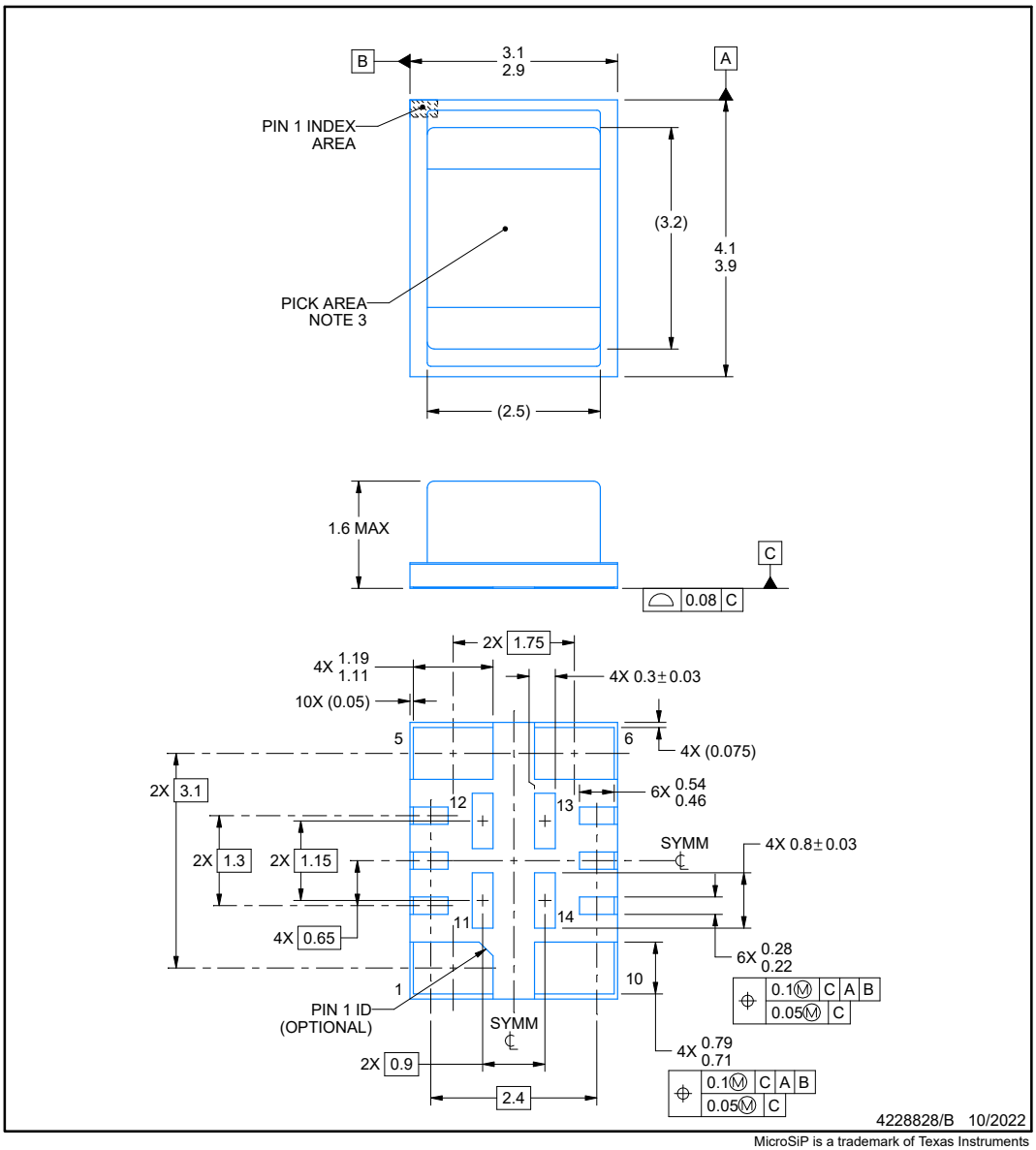
PACKAGE OUTLINE

SIE0014A-C01



uSIP™ - 1.6 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅1.3 mm or smaller recommended.
4. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

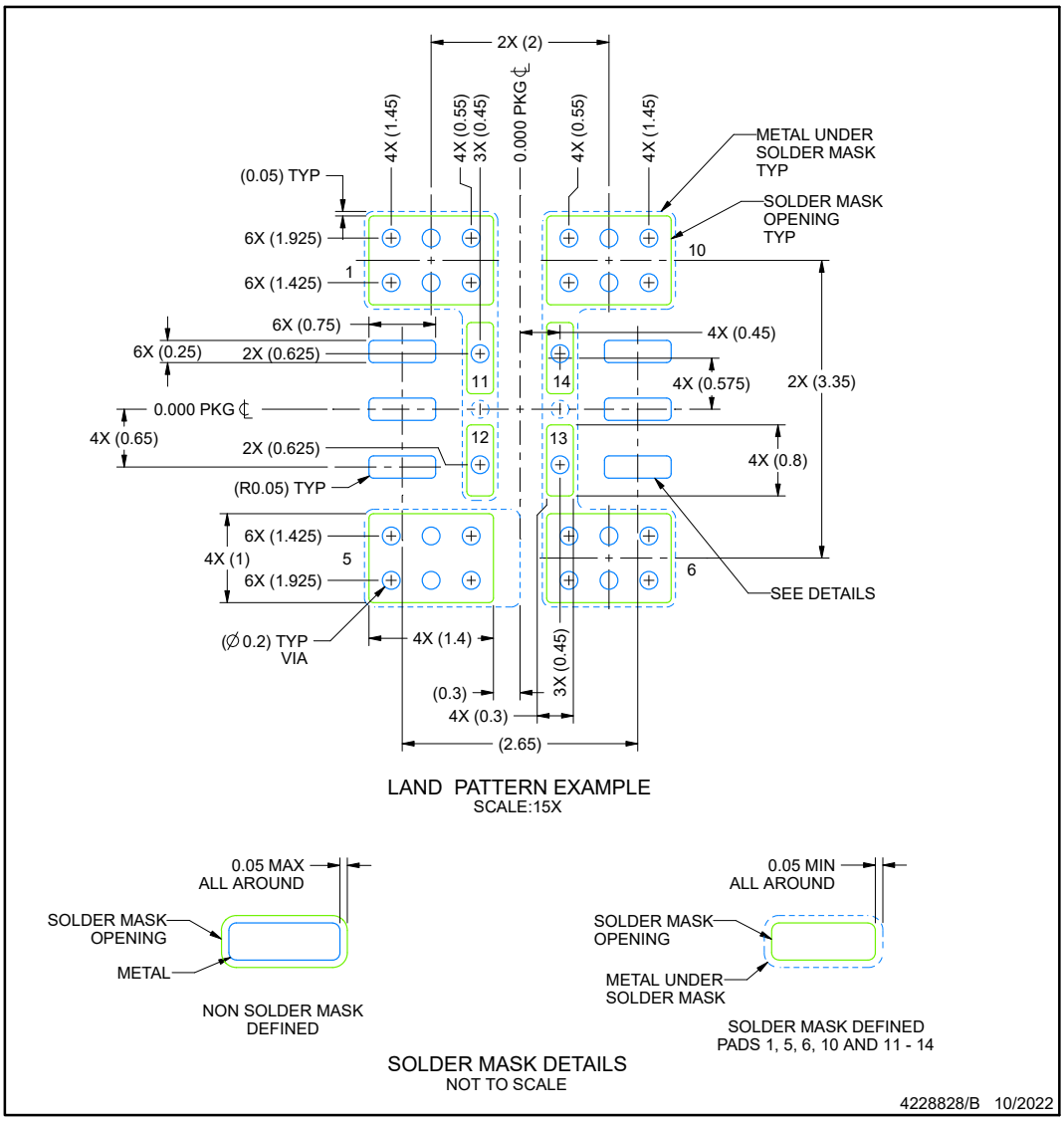
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EXAMPLE BOARD LAYOUT

SIE0014A-C01

uSIP™ - 1.6 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

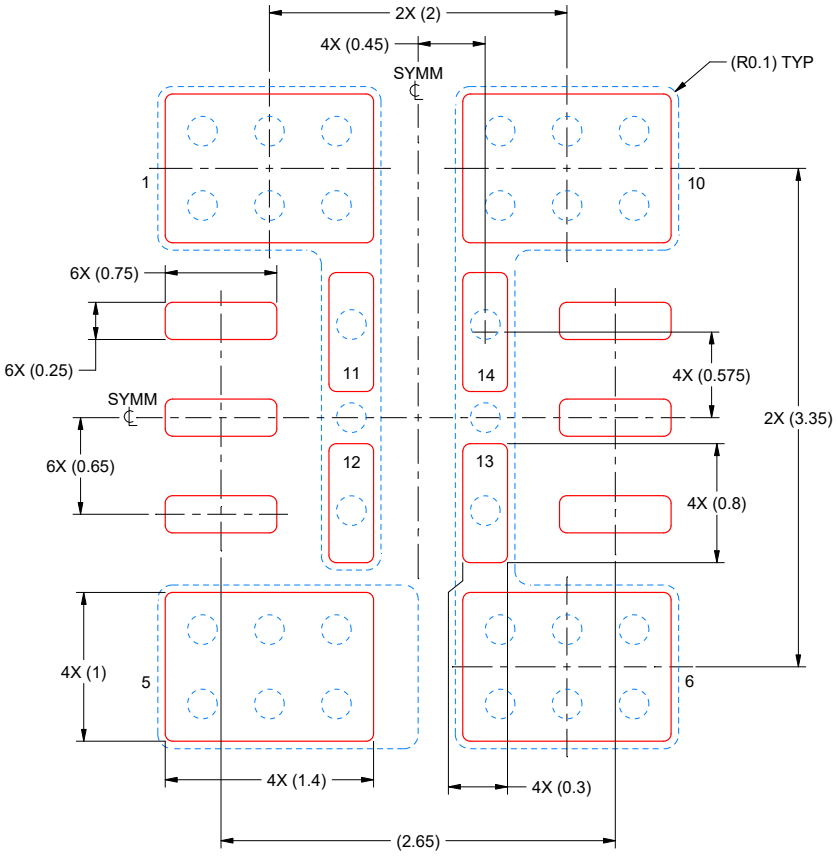
5. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

SIE0014A-C01 **uSIP™ - 1.6 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228828/B 10/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

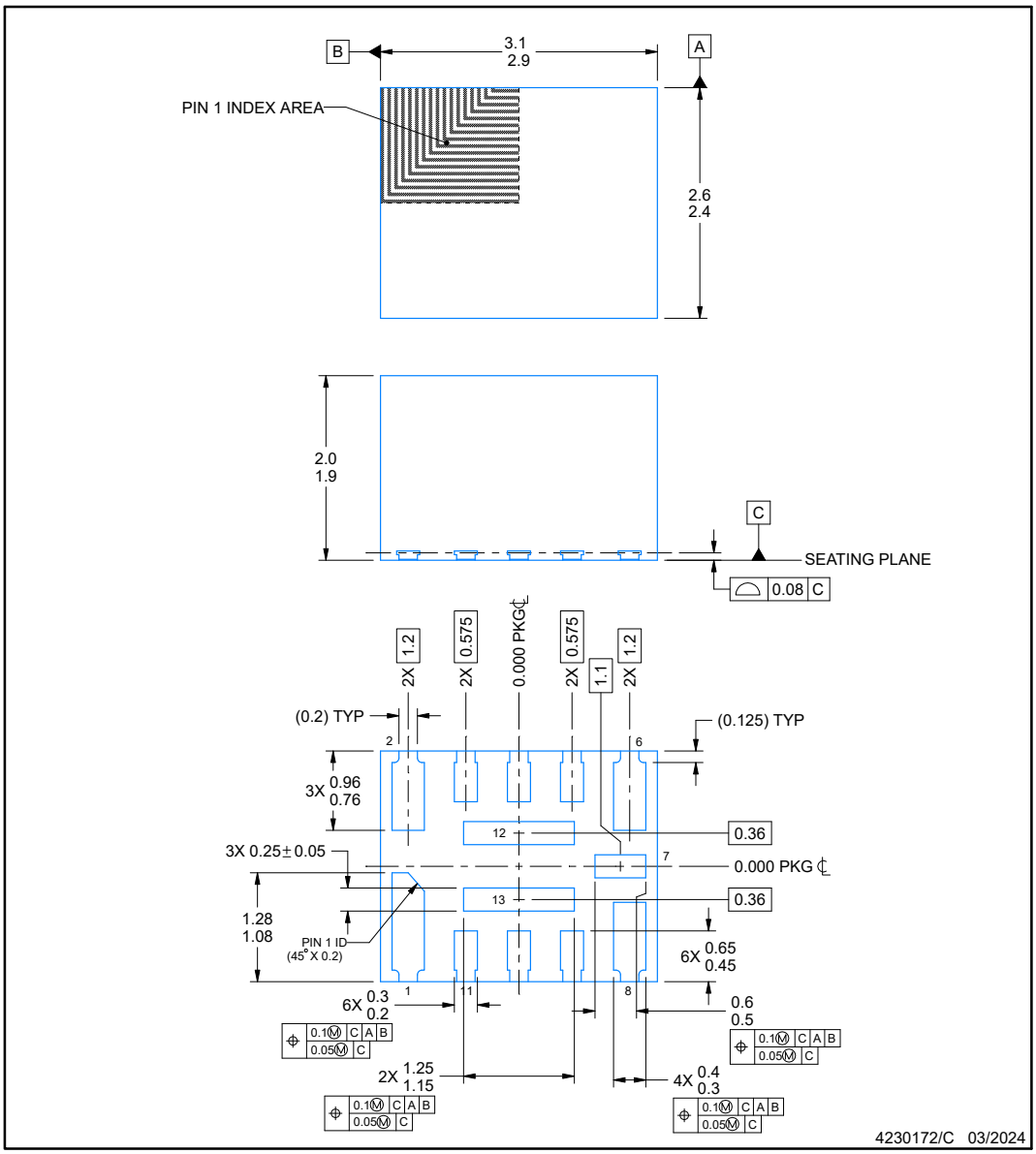
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PACKAGE OUTLINE

VCA0013A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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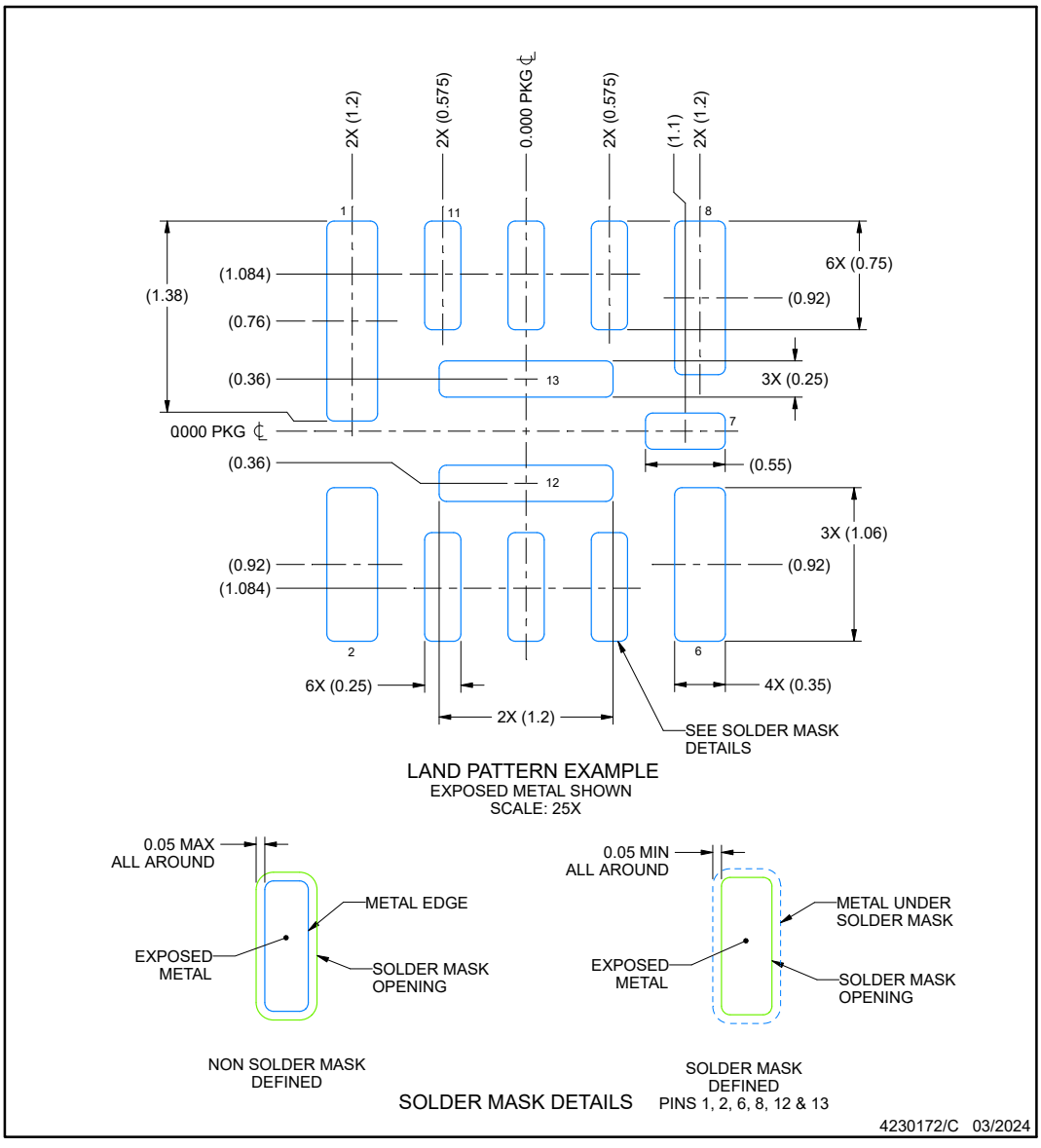
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EXAMPLE BOARD LAYOUT

VCA0013A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

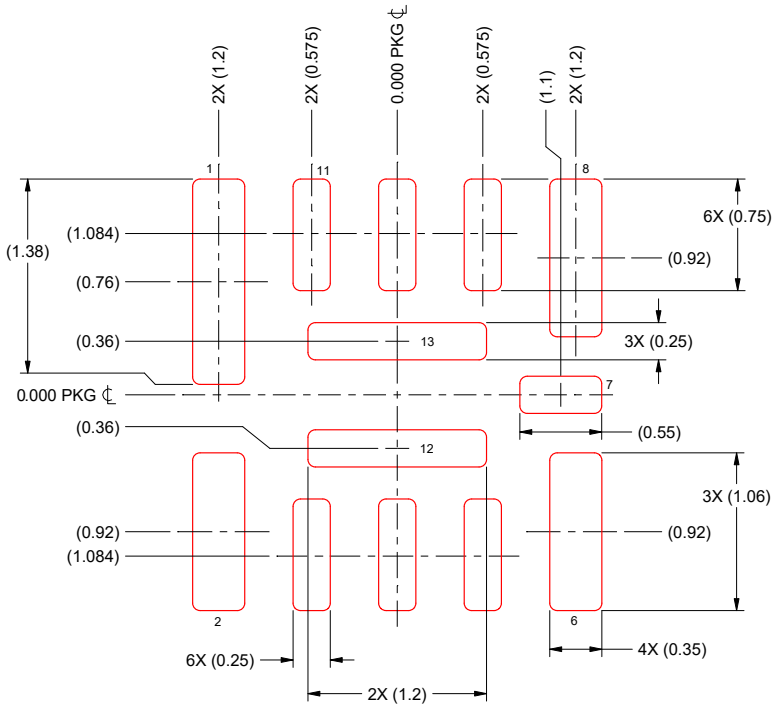
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271)

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EXAMPLE STENCIL DESIGN

VCA0013A — **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4230172/C 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM82816PVCAR	Active	Production	QFN-FCMOD (VCA) | 13	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3HCI
TPSM82816PVCAR.A	Active	Production	QFN-FCMOD (VCA) | 13	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3HCI
TPSM82816SIER	Active	Production	uSiP (SIE) | 14	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	
TPSM82816SIER.A	Active	Production	uSiP (SIE) | 14	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

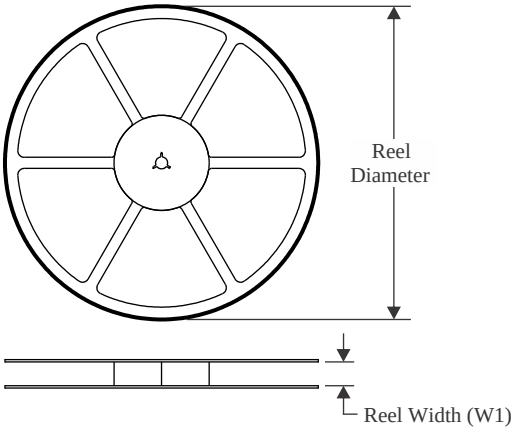
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

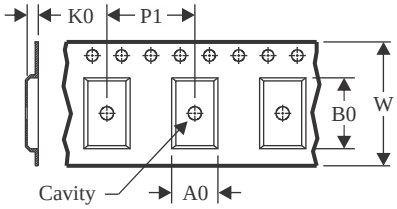
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

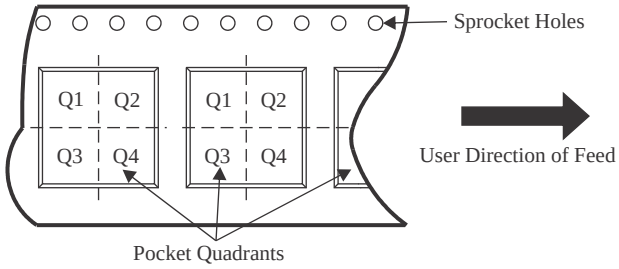


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

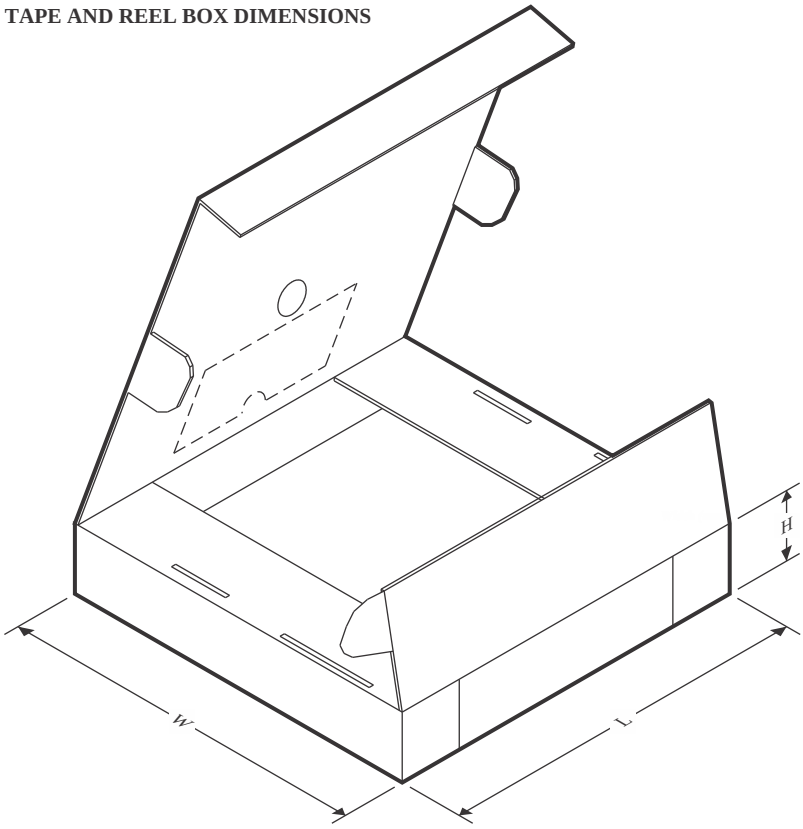
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM82816PVCAR	QFN-FCMOD	VCA	13	2500	330.0	12.4	3.3	2.8	2.2	8.0	12.0	Q1
TPSM82816SIER	uSiP	SIE	14	3000	178.0	13.2	3.27	4.07	1.78	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM82816PVCAR	QFN-FCMOD	VCA	13	2500	367.0	367.0	35.0
TPSM82816SIER	uSiP	SIE	14	3000	383.0	353.0	58.0

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