TPSM843320 インダクタ内蔵、内部補償型高度電流モード制御搭載、4V～18V 入力、3A 同期整流式 SWIFT™ 降圧コンバータ MicroSiP™ パワー モジュール

1 特長

- 固定周波数、内部補償型の高度な電流モード (ACM) 制御
- 小型フォーム・ファクタ、3.5mm × 3.5mm × 1.6mm、15 ピン DFM パッケージ MicroSiP パワー モジュール
- 高効率性を実現する、25mΩ と 6.5mΩ の MOSFET、インダクタ、および基本的なパッシブ部品の内蔵
- 入力電圧範囲:4V～18V
- 出力電圧範囲:0.5V～5.5V
- 制御ループ性能を最適化する 3 つの選択可能な PWM ランプ・オプション
- 5 つの選択可能なスイッチング周波数:500kHz、750kHz、1MHz、1.5MHz、2.2MHz
- 外部クロックに同期可能
- 全温度範囲にわたって、0.5V、±0.5% の基準電圧精度
- ソフトスタート時間を選択可能:0.5ms、1ms、2ms、4ms
- プリバイアス出力への単調スタートアップ
- 低電流動作をサポートする選択可能な電流制限
- 可変入力低電圧誤動作防止を利用可能
- パワー・グッド出力監視
- 出力過電圧、出力低電圧、入力低電圧、過電流、過熱保護
- 8A - TPSM843820 6A - TPSM843620 とピン互換
- -40℃～125℃の動作時接合部温度

2 アプリケーション

- ワイヤレス・インフラと有線通信機器
- 光およびファイバ・ネットワーク
- 試験 / 測定機器
- 医療 / ヘルスケア
- 航空宇宙および防衛

3 概要

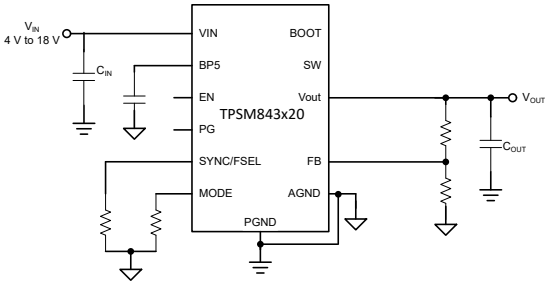
TPSM843320 は、使いやすい MicroSiP パワー・モジュール・パッケージで供給される、高効率、小型でフレキシブルな同期整流式降圧 DC/DC コンバータです。このモジュールは、固定周波数で動作する最大 18V の入力について、システム設計者が抵抗を使用して調整できます。内蔵 IC は内部的に補償されているため、外付け部品を減らし、設計サイズを縮小できます。内蔵の高周波コンデンサにより、スイッチング・ノードでの過渡ピークを低減しています。

TPSM843320 モジュールは、内部補償された固定周波数の高度な電流モード制御を採用しています。このデバイスは、最大 2.2MHz のスイッチング周波数で動作しながら高効率を実現できます。固定周波数コントローラは 500kHz～2.2MHz で動作でき、SYNC ピンを使用して外部クロックに同期できます。追加機能として、高精度の基準電圧、選択可能なソフト・スタート時間、プリバイアス出力への単調なスタートアップ、選択可能な電流制限、EN ピンにより調整可能な UVLO、多岐にわたるフォルト保護があります。

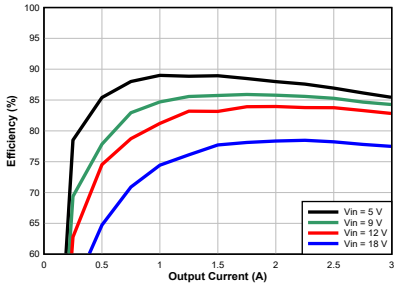
パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TPSM843320	SIT (uSiP、15)	3.50mm × 3.50mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



効率

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

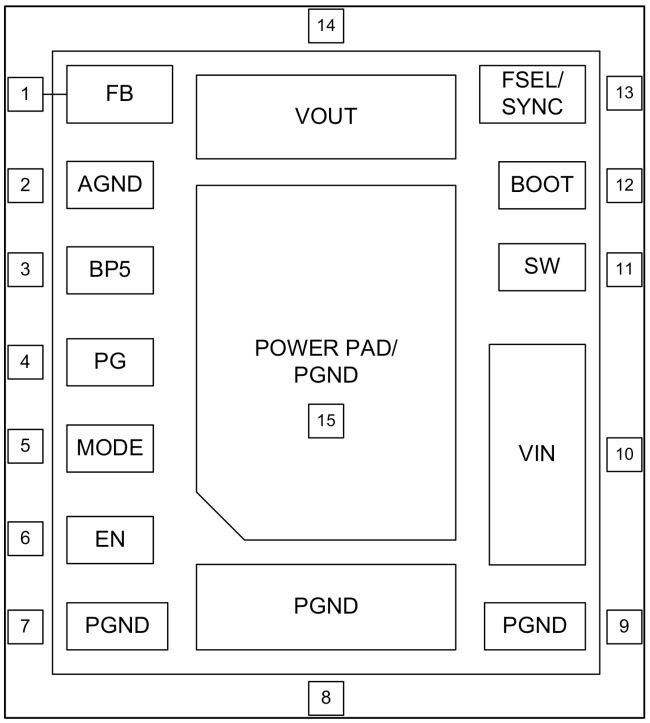


図 4-1. SIT Package 15-Pin uSiP (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback pin for output voltage regulation. Connect this pin to the midpoint of a resistor divider to set the output voltage.
AGND	2	—	Ground return for internal analog circuits
BP5	3	O	Internal 5-V regulator output. Bypass this pin with a 2.2-µF capacitor to AGND.
PG	4	O	Open-drain power-good indicator
MODE	5	I	A resistor to ground selects the current limit, soft-start rate, and PWM ramp amplitude.
EN	6	I	Enable pin. Float to enable, enable and disable with an external signal, or adjust the input undervoltage lockout with a resistor divider.
PGND	7, 8, 9	—	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET.
VIN	10	I	Input power to the power stage. Low impedance bypassing of these pins to PGND is critical. A 47-nF to 100-nF capacitor from VIN to PGND close to IC is required.
SW	11	DNC	Switch node of the module, used for monitoring only
BOOT	12	DNC	Supply for the internal high-side MOSFET gate driver. This pin is monitoring only because the capacitor to SW pin is integrated
SYNC/ FSEL	13	I	Frequency select and external clock synchronization. A resistor to ground sets the switching frequency of the device. An external clock can also be applied to this pin to synchronize the switching frequency.
VOUT	14	O	Buck output voltage. Connect output capacitors to this node.
PAD/ PGND	15	—	Thermal pad connected to PGND

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	20	V
Input voltage	VIN to SW, DC	–0.3	20	V
Input voltage	VIN to SW, transient 20ns	–6	25	V
Input voltage	BOOT	–0.3	25	V
Input voltage	BOOT to SW	–0.3	6	V
Input voltage	EN, PGOOD, MODE, SYNC/FSEL, FB	–0.3	6	V
Output voltage	SW, DC	–0.3	20	V
Output voltage	SW, transient 20 ns	–5	22	V
Operating junction temperature, T_J	Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	4		18	V
Input voltage	SYNC/FSEL, EN, PGOOD	–0.1		5.5	V
Output voltage	V_{OUT}	0.5		5.5	V
Output current	I_{OUT}			3	A
T_J	Operating junction temperature	–40		125	°C
f_{SYNC}	External clock frequency	400		2600	kHz

5.4 Thermal Information

THERMAL METRIC(1)		TPSM843x20 uSiP (TI EVM) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.08	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.08	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics (Module)

T_J = –40°C to +125°C, V_{VIN} = 4 V - 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$I_{Q(VIN)}$	VIN operating non-switching supply current	V_{EN} = 1.3 V, V_{FB} = 550 mV, V_{VIN} = 12 V, 1 MHz		1200	1600	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V, V_{VIN} = 12 V		15	25	µA
	VIN UVLO rising threshold	VIN rising	3.9	4	4.1	V
	VIN UVLO hysteresis			150		mV
ENABLE AND UVLO						
$V_{EN(rise)}$	EN voltage rising threshold	EN rising, enable switching		1.2	1.25	V
$V_{EN(fall)}$	EN voltage falling threshold	EN falling, disable switching	1.05	1.1		V
$V_{EN(hyst)}$	EN voltage hysteresis			100		mV
	EN pin sourcing current	V_{EN} = 1.1 V	0.4	1.5		µA
	EN pin sourcing current	V_{EN} = 1.3 V		11.6		µA
INTERNAL LDO BP5						
V_{BP5}	Internal LDO BP5 output voltage	V_{VIN} = 12 V		4.5		V
	BP5 dropout voltage	V_{VIN} – V_{BP5}, V_{VIN} = 3.8 V			350	mV
	BP5 short-circuit current limit	V_{VIN} = 12 V		75		mA
REFERENCE VOLTAGE						
V_{FB}	Feedback Voltage	T_J = –40°C to 125°C	495	500	505	mV
$I_{FB(LKG)}$	Input leakage current into FB pin	V_{FB} = 500 mV, non-switching, V_{VIN} = 12 V, V_{EN} = 0 V		1		nA
SWITCHING FREQUENCY AND OSCILLATOR						
f_{SW}	Switching frequency	RFSEL = 24.3 kΩ	450	500	550	kHz
f_{SW}	Switching frequency	R_{FSEL} = 17.4 kΩ	675	750	825	kHz
f_{SW}	Switching frequency	RFSEL = 11.8 kΩ	900	1000	1100	kHz
f_{SW}	Switching frequency	R_{FSEL} = 8.06 kΩ	1350	1500	1650	kHz
f_{SW}	Switching frequency	R_{FSEL} = 4.99 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
$V_{IH(sync)}$	High-level input voltage		1.8			V
$V_{IL(sync)}$	Low-level input voltage				0.8	V
SOFT-START						
t_{SS1}	Soft-start time	R_{MODE} = 1.78 kΩ		0.5		ms
t_{SS2}	Soft-start time	R_{MODE} = 2.21 kΩ		1		ms
t_{SS3}	Soft-start time	R_{MODE} = 2.74 kΩ		2		ms
t_{SS4}	Soft-start time	R_{MODE} = 3.32 kΩ		4		ms
POWER STAGE						
$R_{DS(on)HS}$	High-side MOSFET on-resistance	T_J = 25°C, V_{VIN} = 12 V, $V_{BOOT-SW}$ = 4.5 V		25		mΩ
$R_{DS(on)LS}$	Low-side MOSFET on-resistance	T_J = 25°C, V_{BP5} = 4.5 V		13.9		mΩ
$V_{VIN(TH_r)}$	VIN throttle rising threshold(2)	T_J = 25°C. Weaken high-side gate drive upon VIN rising	15.7	16	16.3	V
$V_{BOOT-SW(UV_r)}$	BOOT-SW UVLO rising threshold	$V_{BOOT-SW}$ rising		3.2		V
$V_{BOOT-SW(UV_f)}$	BOOT-SW UVLO falling threshold	$V_{BOOT-SW}$ falling		2.8		V
$T_{ON(min)}$	Minimum ON pulse width	I_{OUT} > ½ I_{L_PK-PK}		30	37	ns
$T_{OFF(min)}$	Minimum OFF pulse width (1)			115	140	ns
CURRENT SENSE AND OVERCURRENT PROTECTION						
$I_{OC_HS_pk1}$	High-side peak current limit(3A)	R_{MODE} = 1.78 kΩ	4.6	4.9	5.1	A
$I_{OC_HS_pk2}$	High-side peak current limit(3A)	R_{MODE} = 22.1 kΩ	2.9	3.3	3.5	A
$I_{OC_LS_src1}$	Low-side sourcing current limit(3A)	R_{MODE} = 1.78 kΩ	3.8	4.2	4.5	A
$I_{OC_LS_src2}$	Low-side sourcing current limit(3A)	R_{MODE} = 22.1 kΩ	2.7	3.0	3.3	A
$I_{OC_LS_snk}$	Low-side sinking current limit	Current into SW pin	1.9			A

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5.5 Electrical Characteristics (Module) (続き)

T_J = –40°C to +125°C, V_{VIN} = 4 V - 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTIONS						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising		120		% V_{REF}
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	V_{FB} falling		80		% V_{REF}
POWER GOOD						
	PGOOD threshold	V_{FB} rising (Fault)	113	116	119	% V_{REF}
	PGOOD threshold	V_{FB} falling (Good)	105	108	111	% V_{REF}
	PGOOD threshold	V_{FB} rising (Good)	89	92	95	% V_{REF}
	PGOOD threshold	V_{FB} falling (Fault)	81	84	87	% V_{REF}
$I_{PGOOD(LKG)}$	Leakage current into PGOOD pin when open drain output is high	V_{PGOOD} = 4.7 V			5	µA
$V_{PG(low)}$	PGOOD low-level output voltage	I_{PGOOD} = 2 mA, V_{IN} = 12 V			0.5	V
	Min VIN for valid PGOOD output			0.9	1	V
HICCUP						
	Hiccup time before re-start			7*t_{SS}		ms
OUTPUT DISCHARGE						
R_{Dischg}	Output discharge resistance	V_{VIN} = 12 V, V_{SW} = 0.5 V, power conversion disabled.		100		Ω
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising		165	175	°C
T_{HYST}	Thermal shutdown hysteresis (1)			12		°C

(1) Specified by design. Not production tested.
(2) Specified by correlation. Not production tested.

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5.6 Typical Characteristics

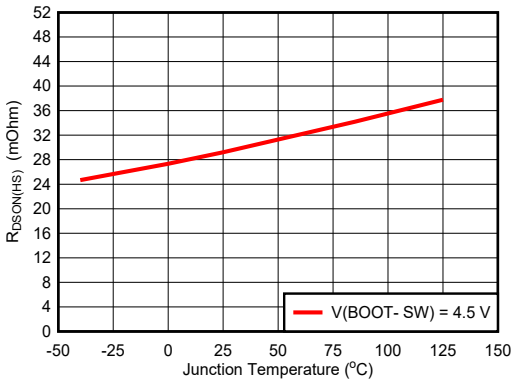


図 5-1. High-Side FET RdsON

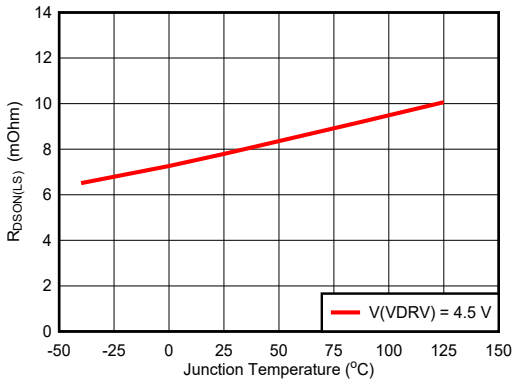


図 5-2. Low-Side FET RdsON

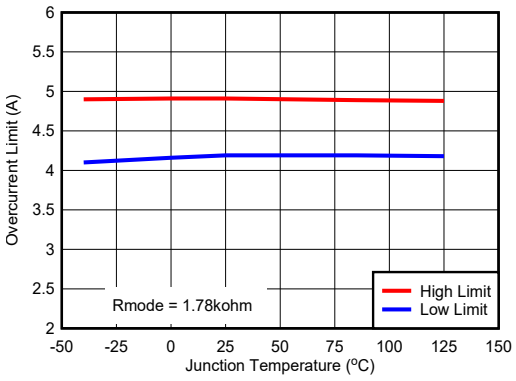


図 5-3. Overcurrent Limit : R = 1.78kOhm

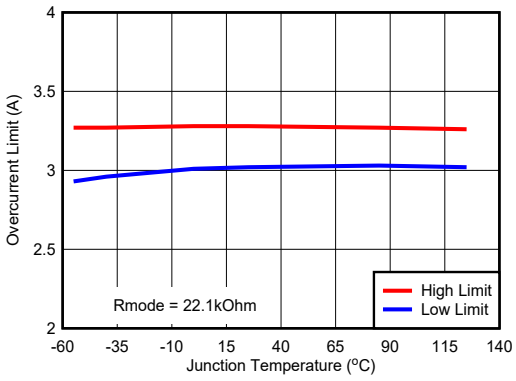


図 5-4. Overcurrent Limit : R = 22.1kOhm

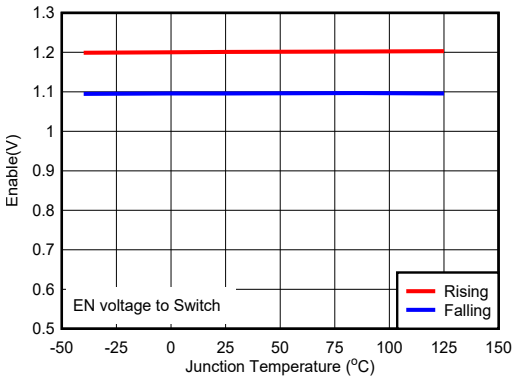


図 5-5. Enable Voltage

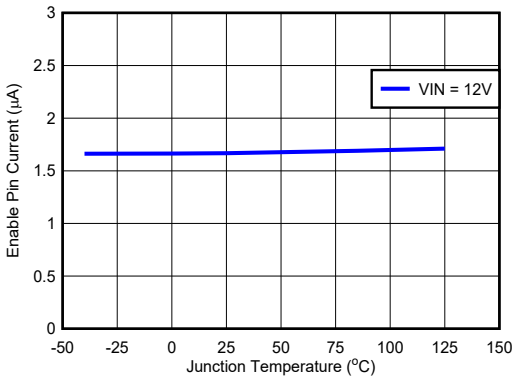


図 5-6. Enable Pin Current

5.6 Typical Characteristics (continued)

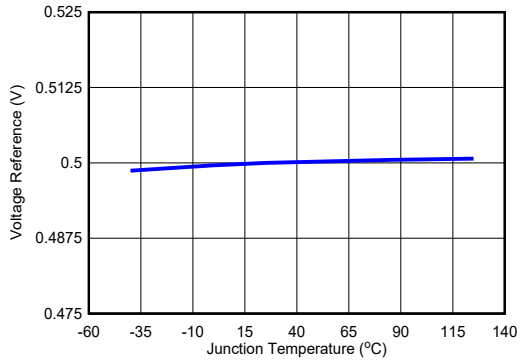


図 5-7. Voltage Reference

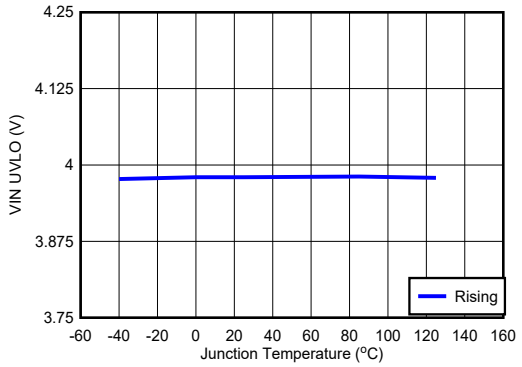


図 5-8. Vin UVLO

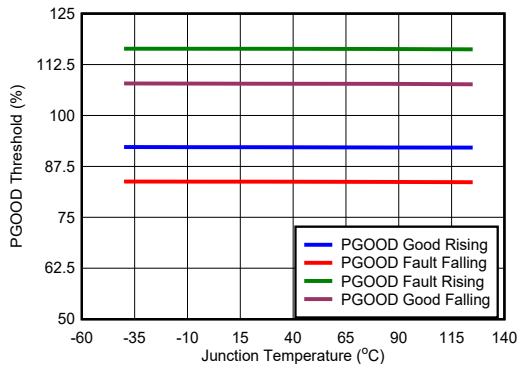


図 5-9. PG Threshold

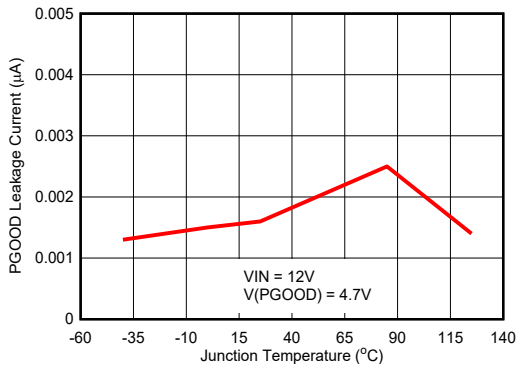


図 5-10. PG Leakage

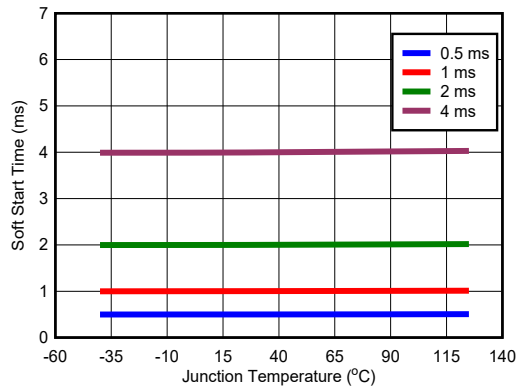


図 5-11. Soft Start

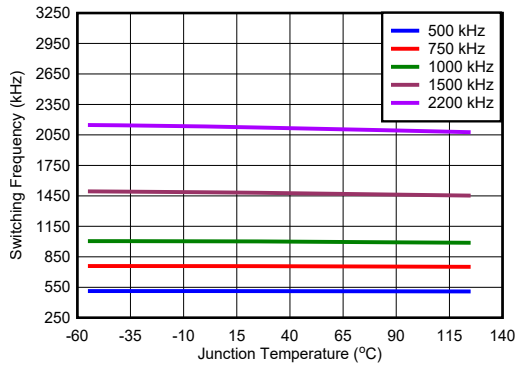


図 5-12. Switching Frequency

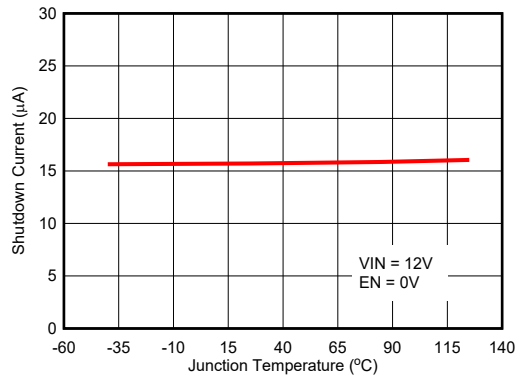


図 5-13. Shutdown Current

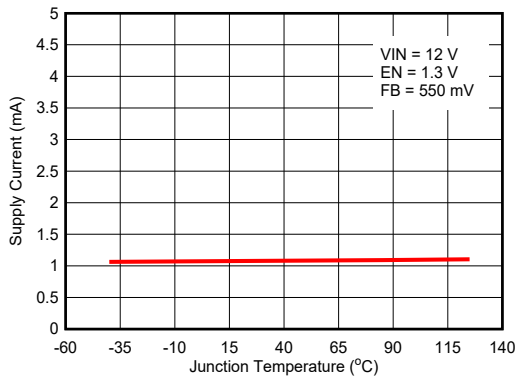


図 5-14. Non-Switching Supply Current

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5.6 Typical Characteristics (continued)

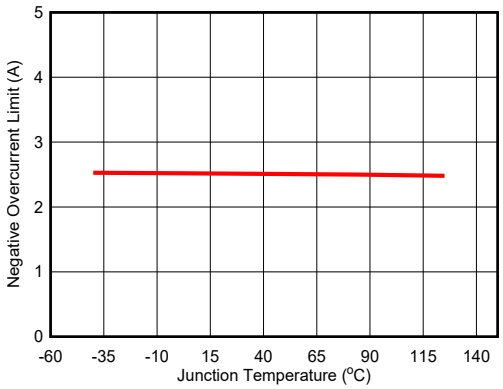


図 5-15. Negative Overcurrent

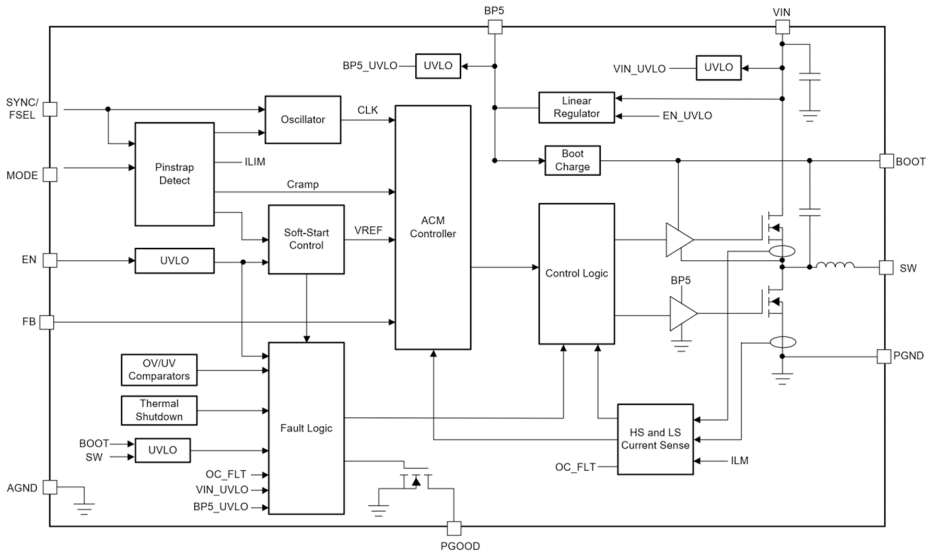
6 Detailed Description

6.1 Overview

The TPSM843320 device is a 3-A, high-performance, synchronous buck converter module with integrated inductor and discretes. The TPSM843320 has a maximum operating junction temperature of 125°C, making the device an excellent choice for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V and the output voltage range is 0.5 V to 5.5 V. The device features a fixed-frequency Advanced Current Mode control with a switching frequency of 500 kHz to 2.2 MHz, allowing for efficiency and size optimization when selecting output filter components. The switching frequency of the device can be synchronized to an external clock applied to the SYNC pin.

Advanced Current Mode (ACM) is an emulated peak current control topology. Advanced Current Mode supports stable static and transient operation without complex external compensation design. This control architecture includes an internal ramp generation network that emulates inductor current information, enabling the use of low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). The internal ramp also creates a high signal-to-noise ratio for good noise immunity. The TPSM843320 has three ramp options (see *セクション 6.3.6* for details) to optimize the internal loop for various inductor and output capacitor combinations with only a single resistor to AGND. The TPSM843320 is easy-to-use and allows low external component count with fast load transient response. Fixed-frequency operation also provides ease-of-filter design to overcome EMI noise.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VIN Pins and VIN UVLO

The VIN pin voltage supplies the internal control circuits of the device and provides the input voltage to the power stage. The input voltage for VIN can range from 4 V to 18 V. The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV. A voltage divider connected to the EN pin can adjust the input voltage UVLO as appropriate. See *セクション 6.3.2* for more details.

6.3.2 Enable and Adjustable UVLO

The EN pin provides on and off control of the device. After the EN pin voltage exceeds the threshold voltage, the device begins the start-up sequence. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low operating current state. The EN pin has an internal pullup current source, Ip,

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allowing the pin to be floated to enable the device by default. Make that leakage currents of anything connected to the EN pin do not exceed the minimum EN pullup current or the device can not be able to start. If an application requires controlling the EN pin, an open drain or open collector output logic can be interfaced with the pin.

When the EN pin voltage exceeds the threshold voltage and the VIN pin voltage exceeds the VIN UVLO threshold, the device begins the start-up sequence. First, the BP5 LDO is enabled and charges the external BP5 capacitor. After the voltage on the BP5 pin exceeds the UVLO threshold, the device enters a power-on delay. During the power-on delay, the values of the pinstrap resistors on the MODE pin (see *セクション 6.3.8*) and SYNC/FSEL pin (see *セクション 6.3.4*) are determined and the control loop is initialized. The power-on delay is typically 600 µs. After the power-on delay, soft start begins.

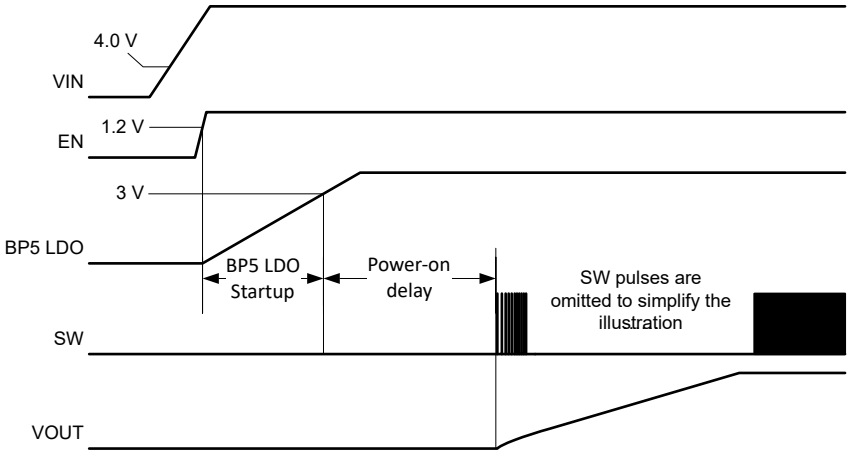


図 6-1. Start-Up Sequence

An external resistor divider can be added from VIN to the EN pin for adjustable UVLO and hysteresis as shown in 図 6-2. The EN pin has a small pullup current, Ip, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by Ih after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 式 1 and 式 2. When using the adjustable UVLO function, TI recommends 500 mV or greater hysteresis. For applications with very slow input voltage slew rate, a capacitor can be placed from the EN pin to ground to filter any glitches on the input voltage.

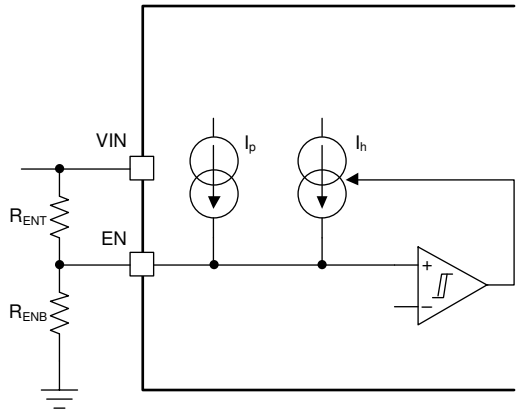


図 6-2. Adjustable UVLO Using EN

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$$R_{ENT} = \frac{V_{START} \times \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (1)$$

$$R_{ENB} = \frac{R_{ENT} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{ENT} \times \left(I_p + I_h \right)} \quad (2)$$

6.3.3 Adjusting the Output Voltage

The output voltage is programmed with a resistor divider from the output (V_{OUT}) to the FB pin shown in 図 6-3. TI recommends to use 1% tolerance or better divider resistors. Starting with a fixed value for the bottom resistor, typically 10 kΩ, use 式 3 to calculate the top resistor in the divider.

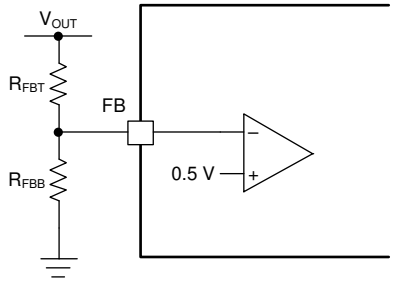


図 6-3. FB Resistor Divider

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (3)$$

6.3.4 Switching Frequency Selection

The switching frequency of the device can be selected by connecting a resistor (R_{FSEL}) between the SYNC/FSEL pin and AGND. The frequency options and their corresponding programming resistors are listed in 表 6-1. Use a 1% tolerance resistor or better.

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表 6-1. Switching Frequency Selection

R_{FSEL} ALLOWED NOMINAL RANGE (1%) (kΩ)	RECOMMENDED E96 STANDARD VALUE (1%) (kΩ)	RECOMMENDED E12 STANDARD VALUE (1%) (kΩ)	Fsw (kHz)
≥ 24.0	24.3	27	500
17.4-18.0	17.4	18	750
11.8-12.1	11.8	12	1000
8.06-8.25	8.06	8.2	1500
≤ 5.11	4.99	4.7	2200

6.3.5 Switching Frequency Synchronization to an External Clock

The device can be synchronized to an external clock by applying a square wave clock signal to the SYNC/FSEL pin with a duty cycle from 20% to 80%. The clock can either be applied before the device starts up or during operation. If the clock is to be applied before the device starts, a resistor between SYNC/FSEL and AGND is not needed. If the clock is to be applied after the device starts, then the clock frequency must be within ±20% of the frequency set by the SYNC/FSEL resistor. When the clock is applied after the device starts, the device begins synchronizing to this clock after counting four consecutive switching cycles with a clock pulse present. This is shown in 図 6-4.

6.3.5.1 Internal PWM Oscillator Frequency

When the external clock is present, the device synchronizes the switching frequency to the clock. Any time the external clock is not present, the device defaults to the internal PWM oscillator frequency.

If the device starts up before an external clock signal is applied, then the internal PWM oscillator frequency is set by the R_{FSEL} resistor according to 表 6-1. The device switches at this frequency until the external clock is applied or anytime the external clock is not present.

If the external clock is applied before the device starts up, then the R_{FSEL} resistor is not needed. The device determines the internal clock frequency by decoding the external clock frequency. 表 6-2 shows the decoding of the internal PWM oscillator frequency based on the external clock frequency.

表 6-2. Internal Oscillator Frequency Decode

EXTERNAL SYNC CLOCK FREQUENCY (kHz)	DECODED INTERNAL PWM OSCILLATOR FREQUENCY (kHz)
400 - 600	500
600 - 857	750
857 - 1200	1000
1200 - 1810	1500
1810 - 2640	2200

The thresholds for the external SYNC clock frequency ranges have approximately a ±5% tolerance. If the external clock frequency is to be within that tolerance range, it is possible for the internal PWM oscillator frequency to be decoded as either the frequency above or below that threshold. Because the internal frequency is what is used in case of the loss of the synchronization clock, TI recommends that the output LC filter and ramp selection are chosen to be stable for either frequency. 表 6-3 shows the tolerance range of the decode thresholds. If the external clock is to be within any of these ranges, TI recommends to ensure converter stability for both possible internal PWM oscillator frequencies.

表 6-3. Frequency Decode Thresholds

MINIMUM (kHz)	TYPICAL (kHz)	MAXIMUM (kHz)
570	600	630
814	857	900
1140	1200	1260
1736	1810	1884

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6.3.5.2 Loss of Synchronization

If at any time during operation, there is a loss of synchronization, the device defaults to the internal PWM oscillator frequency until the synchronization clock returns. After the clock is no longer present, the device switches at 70% of the internal clock frequency for four consecutive cycles. After four consecutive cycles without clock pulses, the device operates at the normal internal PWM oscillator frequency. This action is demonstrated in 図 6-4.

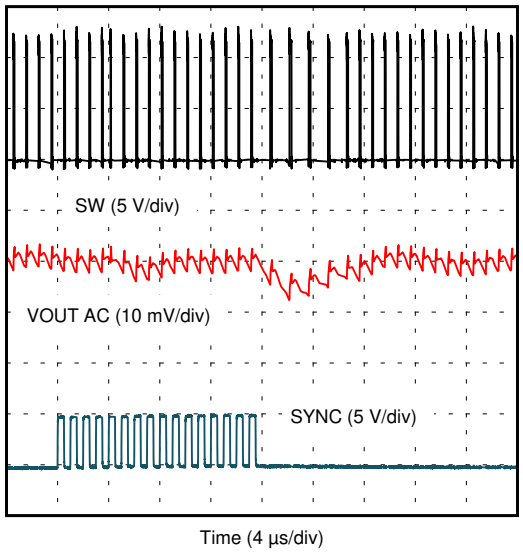


図 6-4. Clock Synchronization Transitions

6.3.5.3 Interfacing the SYNC/FSEL Pin

If an application requires synchronizing to a SYNC clock but the clock is unavailable before the device is enabled, TI recommends a high impedance buffer to ensure proper detection of the R_{FSEL} value. 図 6-5 shows the recommended implementation. The leakage current into the buffer output must be less than 5 µA to ensure proper detection of the R_{FSEL} value. Power the buffer from the BP5 output of the device to ensure its VCC voltage is available and the buffers output is high impedance before the device tries to detect the R_{FSEL} value. When powering the buffer from the BP5 pin, the external load on the BP5 pin must be less than 2 mA.

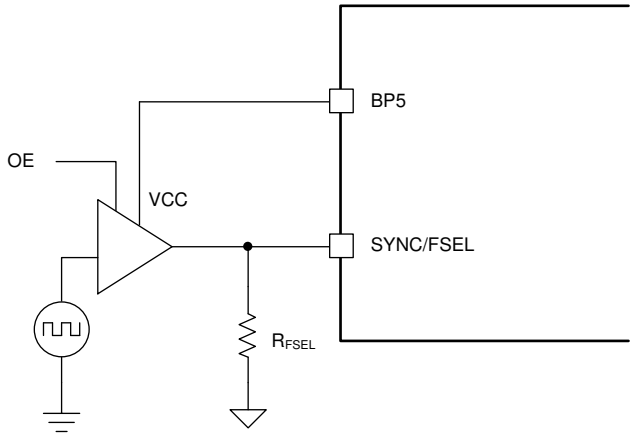


図 6-5. Interfacing the SYNC/FSEL Pin With a Buffer

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6.3.6 Ramp Amplitude Selection

The TPSM843320 uses V_{IN}, duty cycle, and low-side FET current information to generate an internal ramp. The ramp amplitude is determined by an internal ramp generation capacitor, C_{RAMP}. Three different values for C_{RAMP} can be selected with a resistor to AGND on the MODE pin (see *セクション 6.3.8*). The capacitor options are 1 pF, 2 pF, and 4 pF. A larger ramp capacitor results in a smaller ramp amplitude, which results in a higher control loop bandwidth. 図 6-6 and 図 6-7 show how the loop changes with each ramp setting for the schematic in *Typical Applications*.

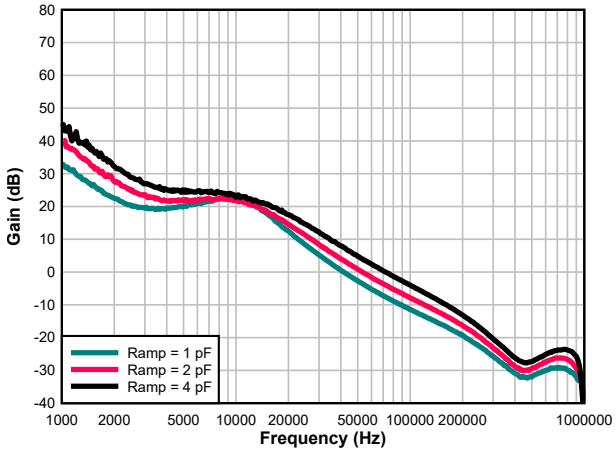


図 6-6. Loop Gain vs Ramp Settings

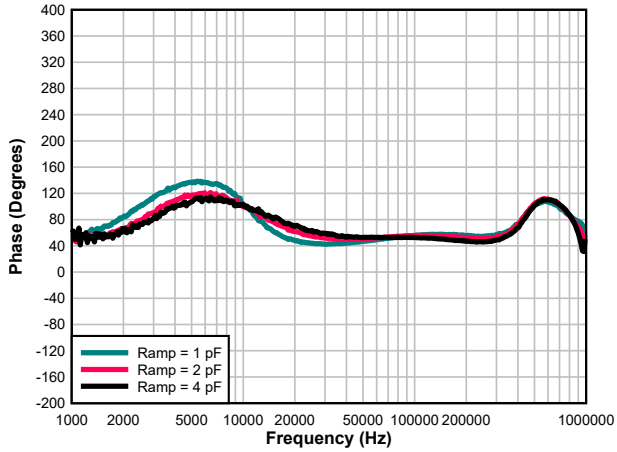


図 6-7. Loop Phase vs Ramp Settings

6.3.7 Soft Start and Prebiased Output Start-Up

During start-up, the device softly ramps the reference voltage to reduce inrush currents. There are four options for the soft-start time, which is the time it takes for the reference to ramp to 0.5 V: 0.5 ms, 1 ms, 2 ms, and 4 ms. The soft-start time is selected with a resistor to AGND on the MODE pin (see *セクション 6.3.8*).

The device prevents current from being discharged from the output during start-up when a prebiased output condition exists. The device does this by operating in discontinuous conduction mode (DCM) during the first 16 cycles to prevent the device from sinking current. This action ensures the output voltage is smooth and monotonic during soft start.

6.3.8 Mode Pin

The ramp amplitude, soft-start time, and current limit settings are programmed with a single resistor, R_{MODE}, between MODE and AGND. 表 6-4 lists the resistor values for the available options. Use a 1% tolerance resistor or better. See *セクション 6.3.10* for the corresponding current limit thresholds for the "High" and "Low" settings.

表 6-4. MODE Pin Selection

R_{MODE} (kΩ)	CURRENT LIMITS	C_{RAMP} (pF)	SOFT-START TIME (ms)
1.78	High	1	0.5
2.21	High	1	1
2.74	High	1	2
3.32	High	1	4
4.02	High	2	0.5
4.87	High	2	1
5.9	High	2	2
7.32	High	2	4
9.09	High	4	0.5
11.3	High	4	1

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表 6-4. MODE Pin Selection (続き)

R_{MODE} (kΩ)	CURRENT LIMITS	C_{RAMP} (pF)	SOFT-START TIME (ms)
14.3	High	4	2
18.2	High	4	4
22.1	Low	1	0.5
26.7	Low	1	1
33.2	Low	1	2
40.2	Low	1	4
49.9	Low	2	0.5
60.4	Low	2	1
76.8	Low	2	2
102	Low	2	4
137	Low	4	0.5
174	Low	4	1
243	Low	4	2
412	Low	4	4

6.3.9 Power Good (PGOOD)

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. After the FB pin is between 92% and 108% of the internal voltage reference, soft start is complete, and after a 256-µs deglitch time, the PGOOD pin is de-asserted and the pin floats. TI recommends a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. PGOOD is in a defined state after the VIN input voltage is greater than 1 V but with reduced current sinking capability. When the FB is lower than 84% or greater than 116% of the nominal internal reference voltage, after a 8-µs deglitch time, the PGOOD pin is pulled low. PGOOD is immediately pulled low if VIN falls below its UVLO, the EN pin is pulled low or the device enters thermal shutdown.

6.3.10 Current Protection

The protects against overcurrent events by cycle-by-cycle current limiting both the high-side MOSFET and low-side MOSFET. In an extended overcurrent condition, the device enters hiccup. Different protections are active during positive inductor current and negative inductor current conditions.

6.3.10.1 Positive Inductor Current Protection

The current is sensed in the high-side MOSFET while conducting after a short blanking time to allow noise to settle. Whenever the high-side overcurrent threshold is exceeded, the high-side MOSFET is immediately turned off and the low-side MOSFET is turned on. The high-side MOSFET does not turn back on until the current falls below the low-side MOSFET overcurrent threshold. This action effectively limits the peak current in the case of a short circuit condition. If a high-side overcurrent is detected for 15 consecutive cycles, the device enters hiccup.

The current is also sensed in the low-side MOSFET while it is conducting after a short blanking time to allow noise to settle. If the low-side overcurrent threshold is exceeded when the next incoming PWM signal is received from the controller, the device skips processing that PWM pulse. The device does not turn the high-side MOSFET on again until the low-side overcurrent threshold is no longer exceeded. If the low-side overcurrent threshold remains exceeded for 15 consecutive cycles, the device enters hiccup. There are two separate counters for the high-side and low-side overcurrent events. If the off-time is too short, the low-side overcurrent can not trip. The low-side overcurrent, however, begins tripping after the high-side peak overcurrent limit is hit as hitting the peak current limit shortens the on-time and lengthens the off-time.

Both the high-side and low-side positive overcurrent thresholds are programmable using the MODE pin. Two sets of thresholds are available ("High" and "Low"), which are summarized in 表 6-5. The values for these thresholds are obtained using open-loop measurements with a DC current to accurately specify the values. In real applications, the inductor current ramps and the ramp rate is a function of the voltage across the inductor

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(V_{IN} – V_{OUT}) as well as the inductance value. This ramp rate combined with delays in the current sense circuitry can result in slightly different values than specified. The current at which the high-side overcurrent limit takes effect can be slightly higher than specified, and the current at which the low-side overcurrent limit takes effect can be slightly lower than specified.

表 6-5. Overcurrent Thresholds

MODE PIN CURRENT LIMIT SETTING	HIGH-SIDE OVERCURRENT TYPICAL VALUE (A)	LOW-SIDE OVERCURRENT TYPICAL VALUE (A)
High	4.9	4.2
Low	3.3	3.0

6.3.10.2 Negative Inductor Current Protection

Negative current is sensed in the low-side MOSFET while it is conducting after a short blanking time to allow noise to settle. Whenever the low-side negative overcurrent threshold is exceeded, the low-side MOSFET is immediately turned off. The next high-side MOSFET turn-on is determined by the clock and PWM comparator. The negative overcurrent threshold minimum value is 2.95 A. Similar to the positive inductor current protections, the actual value of the inductor current when the current sense comparators trip is a function of the current ramp rate. As a result the current at which the negative inductor current limit takes effect can be slightly more negative than specified.

6.3.11 Output Overvoltage and Undervoltage Protection

The device incorporates both output overvoltage and undervoltage protection. If an overvoltage is detected, the device tries to discharge the output voltage to a safe level before attempting to restart. When the overvoltage threshold is exceeded, the low-side MOSFET is turned on until the low-side negative overcurrent threshold is reached. At this point, the high-side MOSFET is turned on until the inductor current reaches zero. Then, the low-side MOSFET is turned back on until the low-side negative overcurrent threshold is reached. This process repeats until the output voltage falls back into the PGOOD window. After this happens, the device restarts and goes through a soft start cycle. The device does not wait the hiccup time before restarting.

When an undervoltage condition is detected, the device enters hiccup where it waits seven soft-start cycles before restarting. Undervoltage protection is enabled after soft start is complete.

6.3.12 Overtemperature Protection

When the die temperature exceeds 165°C, the device turns off. After the die temperatures falls below the hysteresis level, typically 12°C, the device restarts. While waiting for the temperature to fall below the hysteresis level, the device does not switch or attempt to hiccup to restart. After the temperature falls below this level, the device restarts without going through hiccup.

6.3.13 Output Voltage Discharge

When the device is enabled, but the high-side FET and low-side FET are disabled due to a fault condition, the output voltage discharge mode is enabled. This mode turns on the discharge FET from SW to PGND to discharge the output voltage. The discharge FET is turned off when the converter is ready to resume switching, either after the fault clears or after the wait time before hiccup is over.

The output voltage discharge mode is activated by any of below fault events:

1. High-side or low-side positive overcurrent
2. Thermal shutdown
3. Output voltage undervoltage
4. VIN UVLO

6.4 Device Functional Modes

6.4.1 Forced Continuous-Conduction Mode

The TPSM843320 operates in forced continuous-conduction mode (FCCM) throughout normal operation.

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6.4.2 Discontinuous Conduction Mode during Soft Start

During soft start, the converter operates in discontinuous conduction mode (DCM) during the first 16 PWM cycles. During this time, a zero-cross detect comparator is used to turn off the low-side MOSFET when the current reaches zero amps. This prevents the discharge of any pre-biased conditions on the output. After 16 cycles of DCM, the converter enters FCCM mode.

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7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPSM843320 is a synchronous buck regulator designed for 4-V to 18-V input and 3-A load. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors.

7.2 Typical Applications

7.2.1 1.0-V Output, 1-MHz Application

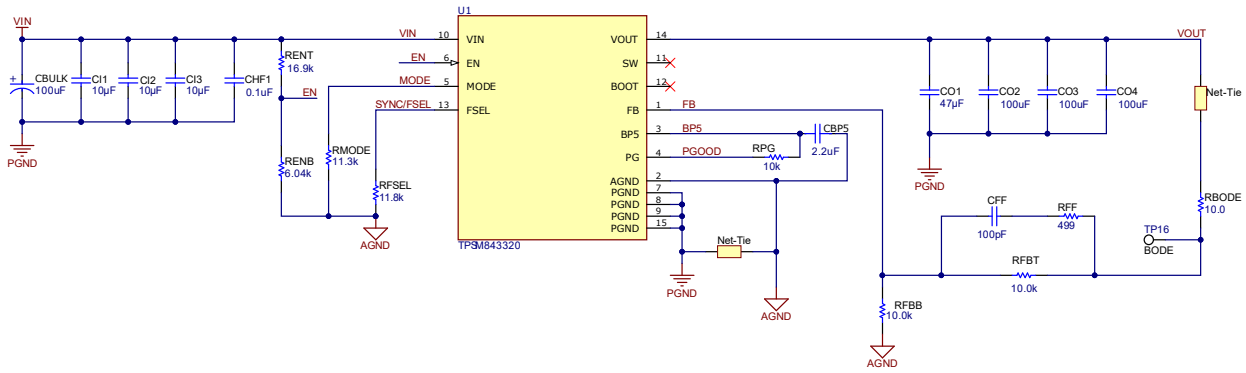


図 7-1. 12-V Input, 1.0-V Output, 1-MHz Schematic

7.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 7-1.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4 to 18 V, 12-V nominal
Output voltage (V_{OUT})	1.0 V
Output current rating (I_{OUT})	3 A
Switching frequency (f_{SW})	1000 kHz
Steady state output ripple voltage	10 mV
Output current load step	1.5 A
Transient response	± 30 mV (± 3%)

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7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Switching Frequency

The first step is to decide on a switching frequency. The TPSM843320 can operate at five different frequencies from 500 kHz to 2.2 MHz. The f_{SW} is set by the resistor value from the FSEL pin to ground. Typically the highest switching frequency possible is desired because it produces the smallest design size. A high switching frequency allows for smaller inductors and output capacitors compared to a power supply that switches at a lower frequency. The main tradeoff made with selecting a higher switching frequency is extra switching power loss, which hurts the efficiency of the regulator.

The maximum switching frequency for a given application can be limited by the minimum on-time of the regulator. The maximum f_{SW} can be estimated with 式 4. Using the minimum on-time of 40 ns and 18-V maximum input voltage for this application, the maximum switching frequency is 1390 kHz. The selected switching frequency must also consider the tolerance of the switching frequency. A switching frequency of 1000 kHz was selected for a good balance of design size and efficiency. To set the frequency to 1000 kHz, the selected FSEL resistor is 11.8 kΩ per 表 6-1.

$$f_{SW}(max) = \frac{1}{t_{on\,min}} \times \frac{V_{OUT}}{V_{IN}(max)} \tag{4}$$

図 7-2 shows the maximum recommended input voltage versus output voltage for each FSEL frequency. This graph uses a minimum on-time of 40 ns and includes the 10% tolerance of the switching frequency. A minimum on-time of 40 ns is used in this graph to provide margin to the minimum controllable on-time to ensure pulses are not skipped at no load. At light loads, the dead-time between the low-side MOSFET turning off and high-side MOSFET turning on contributes to the minimum SW node pulse-width.

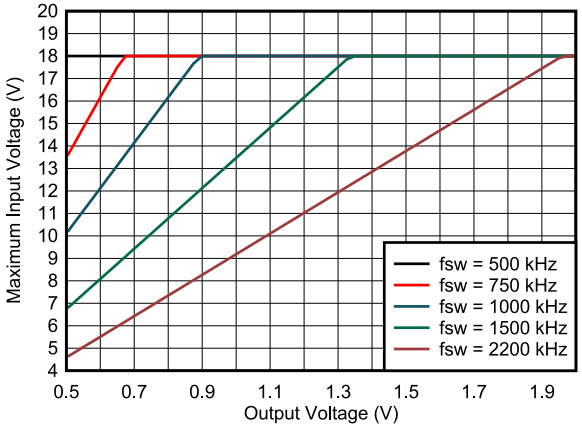


図 7-2. Maximum Input Voltage vs Output Voltage

In high output voltage applications, the minimum off-time must also be considered when selecting the switching frequency. When hitting the minimum off-time limits, the operating duty cycle maxes out and the output voltage begins to drop with the input voltage. 式 5 calculates the maximum switching frequency to avoid this limit. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the following step. A preliminary estimate of 10 mΩ can be used but this must be recalculated based on the specifications of the inductor selected. If operating near the maximum f_{SW} limited by the minimum off-time, the increase in resistance at higher temperature must be considered.

$$f_{SW}(max) = \frac{V_{IN}(min) - V_{OUT} - I_{OUT}(max) \times \left(R_{DCR} + R_{DS(ON)_HS}\right)}{t_{OFF_MIN}(max) \times \left(V_{IN}(min) - I_{OUT}(max) \times \left(R_{DS(ON)_HS} - R_{DS(ON)_LS}\right)\right)} \tag{5}$$

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7.2.1.2.2 Output Inductor Selection

An optimized 1-uF inductor is integrated inside the module.

7.2.1.2.3 Output Capacitor

The output voltage ripple and how the regulator responds to a large change in load current are the two primary considerations for selecting the value of the output capacitor. The output capacitance must be selected based on the more stringent of these criteria.

The desired response to a large change in the load current is the first criteria and is typically the most stringent. A regulator does not respond immediately to a large, fast increase or decrease in load current. The output capacitor supplies or absorbs charge until the regulator responds to the load step. The control loop must sense the change in the output voltage then adjust the peak switch current in response to the change in load. The minimum output capacitance is selected based on an estimate of the loop bandwidth. Typically the loop bandwidth is near f_{SW} / 10. 式 6 estimates the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current and ΔV_{OUT} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 3% change in V_{OUT} for a load step of 1.5 A. Therefore, ΔI_{OUT} is 1.5 A and ΔV_{OUT} is 30 mV. Using this target gives a minimum capacitance of 80 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the effect of the ESR can be small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response.

$$C_{OUT} > \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{2\pi \times \frac{f_{SW}}{10}} \tag{6}$$

In addition to the loop bandwidth, the inductor current slew rate limiting how quickly the regulator responds to the load step is possible. For low duty cycle applications, the time it takes for the inductor current to ramp down after a load step down can be the limiting factor. 式 7 estimates the minimum output capacitance necessary to limit the change in the output voltage after a load step down. Using the 1.0-µH inductance selected gives a minimum capacitance of 38 µF.

$$C_{OUT} > \frac{L_{OUT} \times \Delta I_{OUT}^{2}}{2 \times \Delta V_{OUT} \times V_{OUT}} \tag{7}$$

式 8 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the target maximum steady state output voltage ripple is 10 mV. Under this requirement, 式 8 yields 14 µF.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \tag{8}$$

where

- ΔI_{OUT} is the change in output current
- ΔV_{OUT} is the allowable change in the output voltage
- *f*sw is the regulators switching frequency
- Voripple is the maximum allowable steady state output voltage ripple
- Iripple is the inductor ripple current

Lastly, if an application does not have a strict load transient response or output ripple requirement, a minimum amount of capacitance is still required to ensure the control loop is stable with the lowest gain ramp setting on the MODE pin. 式 9 estimates the minimum capacitance needed for loop stability. This equation sets the

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minimum amount of capacitance by keeping the LC frequency relative to the switching frequency at a minimum value. See 図 7-3 for the limit versus output voltage with the lowest gain ramp setting of 1 pF. With a 1-V output, the minimum ratio is 35 and with this ratio, 式 9 gives a minimum capacitance of 31 µF.

$$C_{OUT} > \left(\frac{Ratio}{2\pi \times f_{SW}} \right)^2 \times \frac{1}{L_{OUT}} \tag{9}$$

式 10 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification and this shows the ESR must be less than 6 mΩ. In this case, ceramic capacitors are used and the combined ESR of the ceramic capacitors in parallel is much less than is needed to meet the ripple. Capacitors also have limits to the amount of ripple current they can handle without producing excess heat and failing. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheet specifies the RMS value of the maximum ripple current. 式 11 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 式 11 yields 273 mA and ceramic capacitors typically have a ripple current rating much higher than this.

$$Resr < \frac{Voripple}{Iripple} \tag{10}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{11}$$

Select X5R and X7R ceramic dielectrics or equivalent for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias and AC voltage derating taken into account. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the capacitor manufacturer's website. For this application example, one 47-µF, 10-V, X5R, 0805 and three 100-µF, 10-V, X5R, 1206 ceramic capacitors each with 2 mΩ of ESR are used. The one 47-µF capacitor is used because it has a higher resonance frequency and can help reduce the output ripple caused by parasitic inductance. With the four parallel capacitors, the estimated effective output capacitance after derating using the capacitor manufacturer's website is 327 µF. There is about a -7% DC bias derating at 1 V. This design was able to use less than the calculated minimum because the loop crossover frequency was above the f_{SW} / 10 estimate as shown in the Load Transient graph in the *Application Curves*.

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7.2.1.2.4 Input Capacitor

Input decoupling ceramic capacitors type X5R, X7R, or similar from VIN to PGND that are placed as close as possible to the IC are required. A total of at least 10 µF of capacitance is required and some applications can require a bulk capacitance. TI recommends at least 1 µF of bypass capacitance as close as possible to the VIN pin to minimize the input voltage ripple. A 0.1-µF to 1-µF capacitor must be placed as close as possible to VIN pin 10 on the same side of the board of the device to provide high frequency bypass to reduce the high frequency overshoot and undershoot on VIN and SW pins. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum RMS input current. The RMS input current can be calculated using 式 12.

For this example design, a ceramic capacitor with at least a 16-V voltage rating is required to support the maximum input voltage. Three 10-µF, 0805, X7S, 25-V and one 0.1-µF, 0402, X7R 25-V capacitors in parallel have been selected to be placed the sides of the IC near the VIN and PGND pins. Based on the capacitor manufacturer's website, the total ceramic input capacitance derates to 8 µF at the nominal input voltage of 12 V. A 100-µF bulk capacitance is also used to bypass long leads when connected a lab bench top power supply.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 13. The maximum input ripple occurs when operating nearest to 50% duty cycle. Using the nominal design example values of Ioutmax = 3 A, C_{IN} = 8 µF, and f_{SW} = 1000 kHz, the input voltage ripple with the 12 V nominal input is 28 mV and the RMS input ripple current with the 4 V minimum input is 2.6 A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vinmin}} \times \frac{(\text{Vinmin} - \text{Vout})}{\text{Vinmin}}} \tag{12}$$

$$\Delta\text{Vin} = \frac{\text{Ioutmax} \times \left(1 - \frac{\text{Vout}}{\text{Vin}}\right) \times \frac{\text{Vout}}{\text{Vin}}}{\text{Cin} \times f_{SW}} \tag{13}$$

7.2.1.2.5 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply is set to turn on and start switching after the input voltage increases above 4 V (UVLO start or enable). After the regulator starts switching, it continues to do so until the input voltage falls below 3.95 V (UVLO stop or disable). In this example, these start and stop voltages set by the EN resistor divider were selected to have more hysteresis than the internally fixed VIN UVLO.

式 1 and 式 2 can be used to calculate the values for the upper and lower resistor values. For these equations to work, V_{START} must be 1.1 × V_{STOP} due to the EN pin voltage hysteresis. For the voltages specified, the standard resistor value used for R_{ENT} is 16.9 kΩ and for R_{ENB} is 6.04 kΩ.

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7.2.1.2.6 Output Voltage Resistors Selection

The output voltage is set with a resistor divider created by R_{FBT} and R_{FBB} from the output node to the FB pin. TI recommends to use 1% tolerance or better resistors. For this example design, 10 kΩ was selected for R_{FBB}. Using 式 14, R_{FBT} is calculated as 10 kΩ. This is a standard 1% resistor.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{14}$$

If the PCB layout does not use the recommended AGND to PGND connection in *セクション 7.4.1*, noise on the feedback pin can degrade the output voltage regulation at maximum load. Using a smaller R_{FBB} of 1.00 kΩ minimizes the impact of this noise.

7.2.1.2.7 Bootstrap Capacitor Selection

A 0.1-uF ceramic capacitor is integrated inside the module connected between the BOOT and SW pin.

7.2.1.2.8 BP5 Capacitor Selection

A 2.2-µF ceramic capacitor must be connected between the BP5 pin and AGND for proper operation. The capacitor must be rated for at least 10 V to minimize DC bias derating.

7.2.1.2.9 PGOOD Pullup Resistor

A 10-kΩ resistor is used to pull up the power good signal when FB conditions are met. The pullup voltage source must be less than the 6-V absolute maximum of the PGOOD pin.

7.2.1.2.10 Current Limit Selection

The MODE pin is used to select between two current limit settings. Select the current limit setting whose minimum is greater than at least 1.1 times the maximum steady state peak current. This selection is to provide margin for component tolerance and load transients. For this design, the minimum current limit must be greater than 4.14 A so the high current limit setting is selected.

7.2.1.2.11 Soft-Start Time Selection

The MODE pin is used to select between four different soft-start times. This selection is useful if a load has specific timing requirements for the output voltage of the regulator. A longer soft-start time is also useful if the output capacitance is very large and requires large amounts of current to quickly charge the output capacitors to the output voltage level. The large currents necessary to charge the capacitor can reach the current limit or cause the input voltage rail to sag due excessive current draw from the input power supply. Limiting the output voltage slew rate solves both of these problems. The example design has the soft-start time set to 1.0 ms. With this soft-start time the current required to charge the output capacitors to the nominal output voltage is only 0.14 A.

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7.2.1.2.12 Ramp Selection and Control Loop Stability

The MODE pin is used to select between three different ramp settings. The most optimal ramp setting depends on V_{OUT}, f_{SW}, L_{OUT}, and C_{OUT}. To get started, calculate LC double pole frequency using 式 15. The ratio between f_{SW} and f_{LC} must then be calculated. Based on this ratio and the output voltage, the recommended ramp setting must be selected using 図 7-3. With a 1-V output, TI recommends the 1-pF ramp for ratios between approximately 35 and 58, TI recommends the 2-pF ramp for ratios between approximately 58 and 86, and TI recommends the 4-pF ramp for ratios greater than approximately 86. In general, use the largest ramp capacitor the design supports. Increasing the ramp capacitor improves transient response but can reduce stability margin or increase on-time jitter.

For this design, f_{LC} is 8.54 kHz and the ratio is 117 which is in the 4-pF ramp setting. Through bench evaluation, it was found that the design had sufficient stability margin with the 4-pF ramp so this setting was selected for the best transient response. The recommended ramp settings given by 図 7-3 include margin to account for potential component tolerances and variations across operating conditions so it is possible to use a higher ramp setting as shown in this example.

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{15}$$

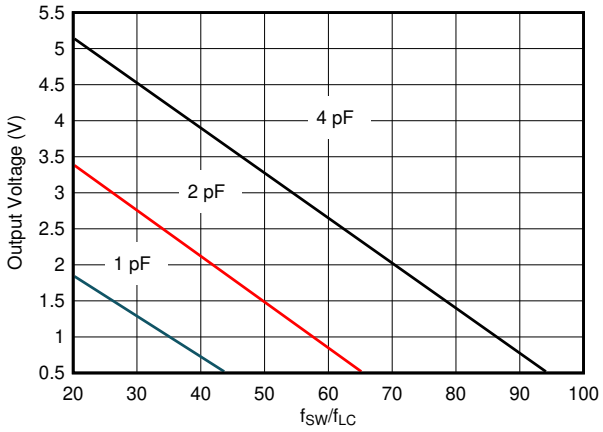


図 7-3. Recommended Ramp Settings

Use a feedforward capacitor (C_{FF}) in parallel with the upper feedback resistor (R_{FBT}) to add a zero into the control loop to provide phase boost. Include a placeholder for this capacitor as the zero it provides can be required to meet phase margin requirements. This capacitor also adds a pole at a higher frequency than the zero. The pole and zero frequency are not independent so as a result, after the zero location is chosen, the pole is fixed as well. The zero is placed at 1/4 the f_{SW} by calculating the value of C_{FF} with 式 16. The calculated value is 64 pF.

Using bench measurements of the AC response, the feedforward capacitor for this example design was increased to 100 pF to improve the transient response.

$$C_{FF} = \frac{1}{\pi \times R_{FBT} \times \frac{f_{SW}}{2}} \tag{16}$$

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Using larger feedforward capacitors to further improve the transient response but take care to ensure there is a minimum of –9-dB gain margin in all operating conditions is possible. The feedforward capacitor injects noise on the output into the FB pin. This added noise can result in increased on-time jitter at the switching node. Too little gain margin can cause a repeated wide and narrow pulse behavior. Adding a 499-Ω resistor in series with the feedforward capacitor can help reduce the impact of noise on the FB pin in case of non-ideal PCB layout. The value of this resistor must be kept small as larger values bring the feedforward pole and zero closer together degrading the phase boost the feedforward capacitor provides.

When using higher ESR output capacitors, such as polymer or tantalum, their ESR zero (f_{ESR}) must be accounted for. The ESR zero can be calculated using 式 17. If the ESR zero frequency is less than the estimated bandwidth of 1/10th the f_{SW}, it can affect the gain margin and phase margin. A series R-C from the FB pin to ground can be used to add a pole into the control loop if necessary. All ceramic capacitors are used in this design so the effect of the ESR zero is ignored.

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} \tag{17}$$

7.2.1.2.13 MODE Pin

The MODE resistor is set to 11.3 kΩ to select the high current limit setting, 1.0-ms soft start and the 4-pF ramp. See 表 6-4 for the full list of the MODE pin settings.

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7.2.1.3 Application Curves

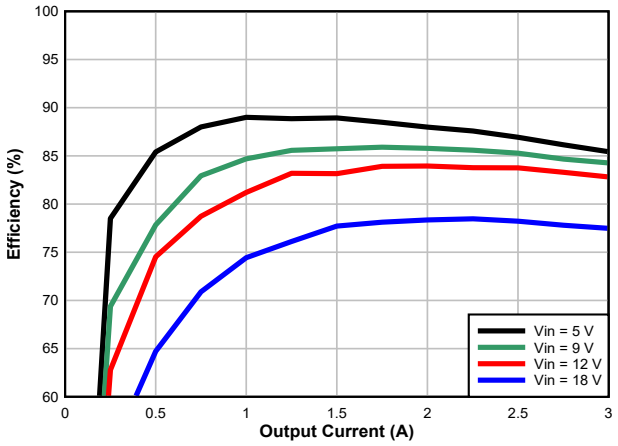


図 7-4. Efficiency

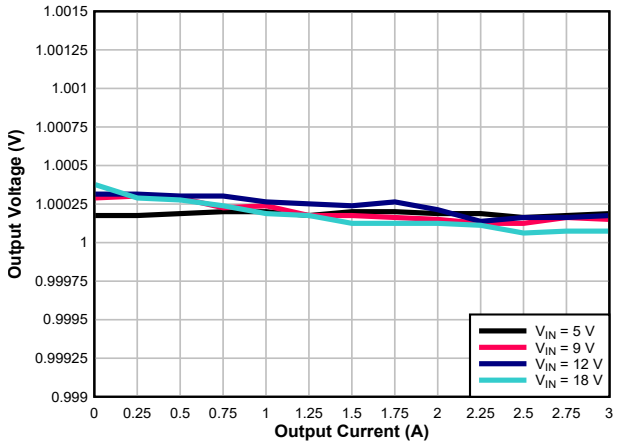


図 7-5. Load Regulation

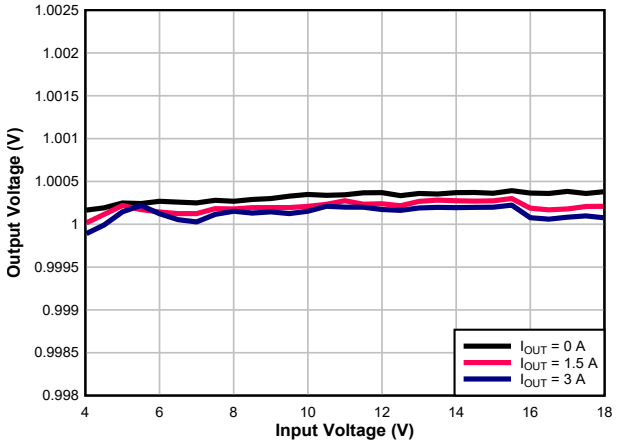
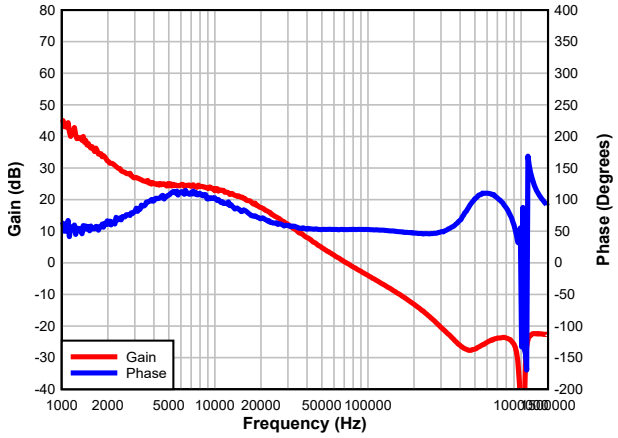
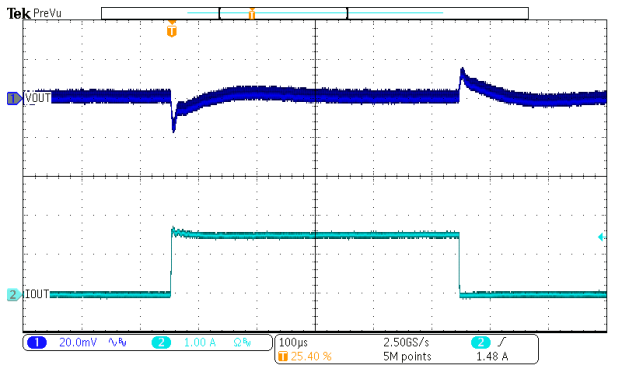


図 7-6. Line Regulation



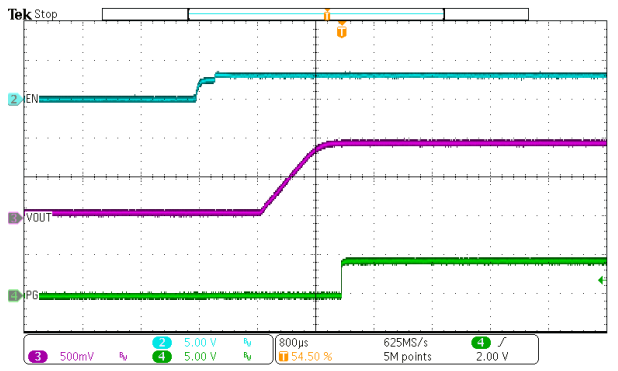
VIN = 12 V IOUT = 3 A

図 7-7. Bode Plot



VIN = 12 V IOUT(DC) = 0.75 A ISTEP = 1.5 A at 1A/µs

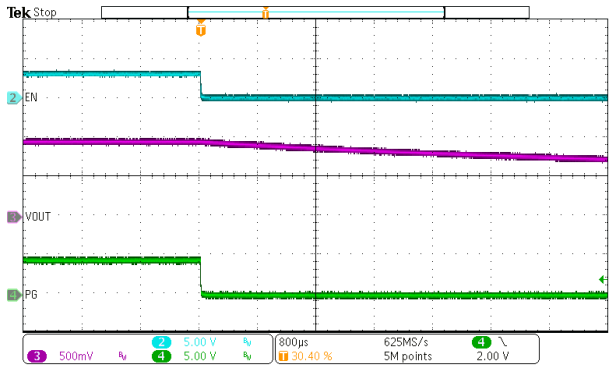
図 7-8. Load Transient



VIN = 12 V IOUT = 0 A

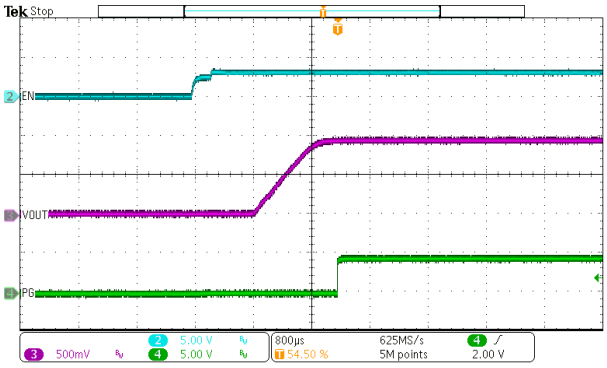
図 7-9. EN Start-Up – No Load

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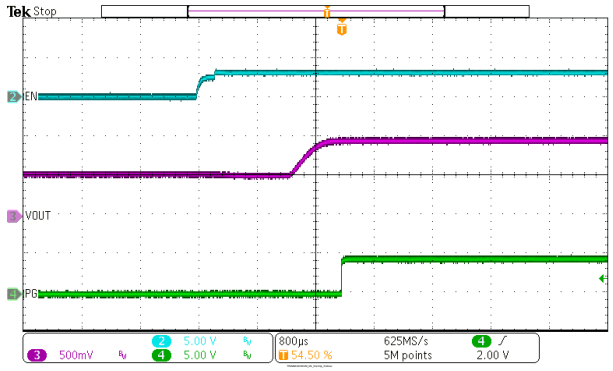
V_{IN} = 12 V I_{OUT} = 0 A

図 7-10. EN Shutdown No Load



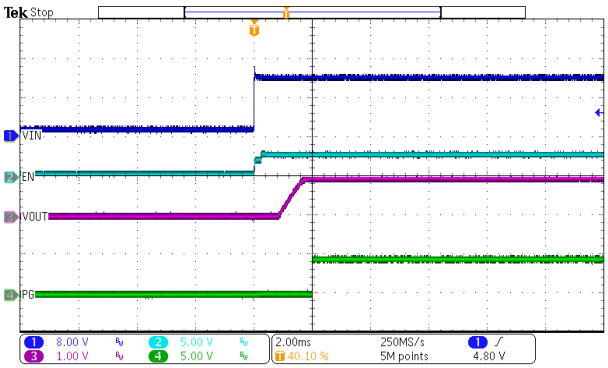
V_{IN} = 12 V I_{OUT} = 3 A

図 7-11. EN Start-Up – With Load



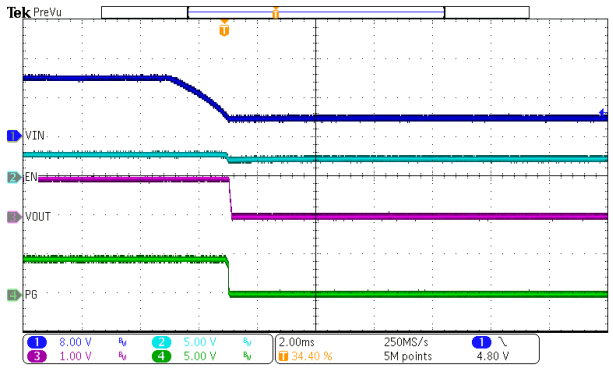
V_{IN} = 12 V I_{OUT} = 0 A

図 7-12. EN Start-Up – 0.5-V Prebias



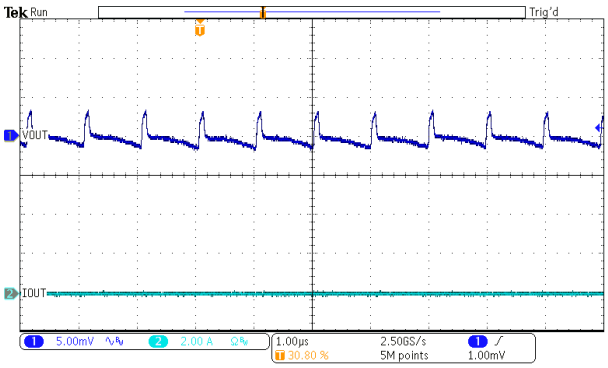
I_{OUT} = 0 A

図 7-13. VIN Start-Up



I_{OUT} = 3 A

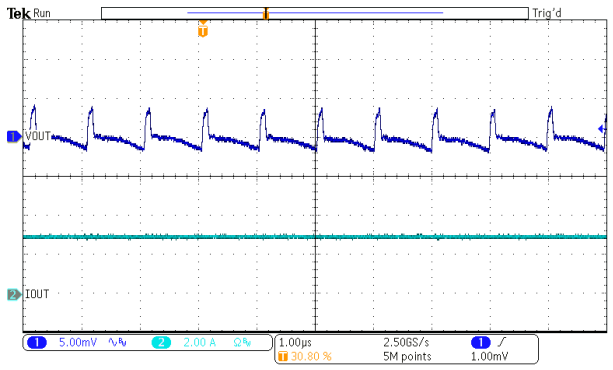
図 7-14. VIN Shutdown



V_{IN} = 12 V I_{OUT} = 0 A

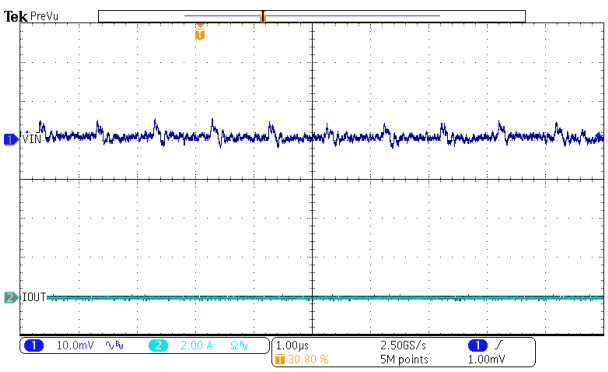
図 7-15. Output Ripple – No Load

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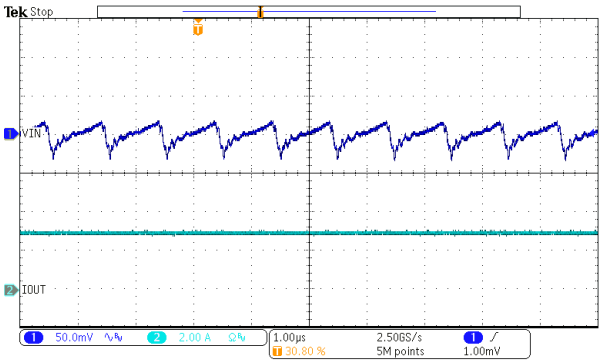
V_{IN} = 12 V I_{OUT} = 3 A

図 7-16. Output Ripple – 3-A Load



V_{IN} = 12 V I_{OUT} = 0 A

図 7-17. Input Ripple – No Load



V_{IN} = 12 V I_{OUT} = 3 A

図 7-18. Input Ripple – 3-A Load

7.3 Power Supply Recommendations

The TPSM843320 is designed to operate from an input voltage supply range between 4 V and 18 V. This supply voltage must be well regulated. Proper bypassing of the input supply is critical for proper electrical performance, as is the PCB layout and the grounding scheme. A minimum of 4 µF (after derating) ceramic capacitance, type X5R or better, must be placed near the device. TI recommends splitting the ceramic input capacitance equally between the VIN and PGND pins on each side of the device resulting in at least 2 µF of ceramic capacitance on each side of the device.

7.4 Layout

7.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. See 図 7-19 for a PCB layout example. Key guidelines to follow for the layout are:

- Make VIN, PGND, and SW traces as wide as possible to reduce trace impedance and improve heat dissipation.
- Place a 10-nF to 100-nF capacitor at the VIN pin to PGND and place it as close as possible to the device on the same side of the PCB. Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Use multiple vias near the PGND pins and use the layer directly below the device to connect them together. This action helps to minimize noise and can help heat dissipation.
- Use vias near the VIN pin and provide a low impedance connection between them through an internal layer.
- Place the BP5 capacitor as close as possible to the BP5 and AGND pins.

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- Place the bottom resistor in the FB divider as close as possible to the FB and AGND pins of the IC. Also keep the upper feedback resistor and the feedforward capacitor near the IC. Connect the FB divider to the output voltage at the desired point of regulation.
- Use multiple vias in the AGND island to connect it back to internal PGND layers. Do not place these vias between the BP5 capacitor and the AGND pin. These vias conduct switching currents between the BP5 capacitor and PGND. Placing the vias near the AGND pin can add noise to the FB divider.
- Return the FSEL and MODE resistors to a quiet AGND island.

7.4.2 Layout Example



図 7-19. Example PCB Layout

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7.4.2.1 Thermal Performance

Test Conditions: f_{SW} = 1 MHz, Vin = 12 V, Vout = 1 V, Iout = 3 A, Ambient temperature = 25°C

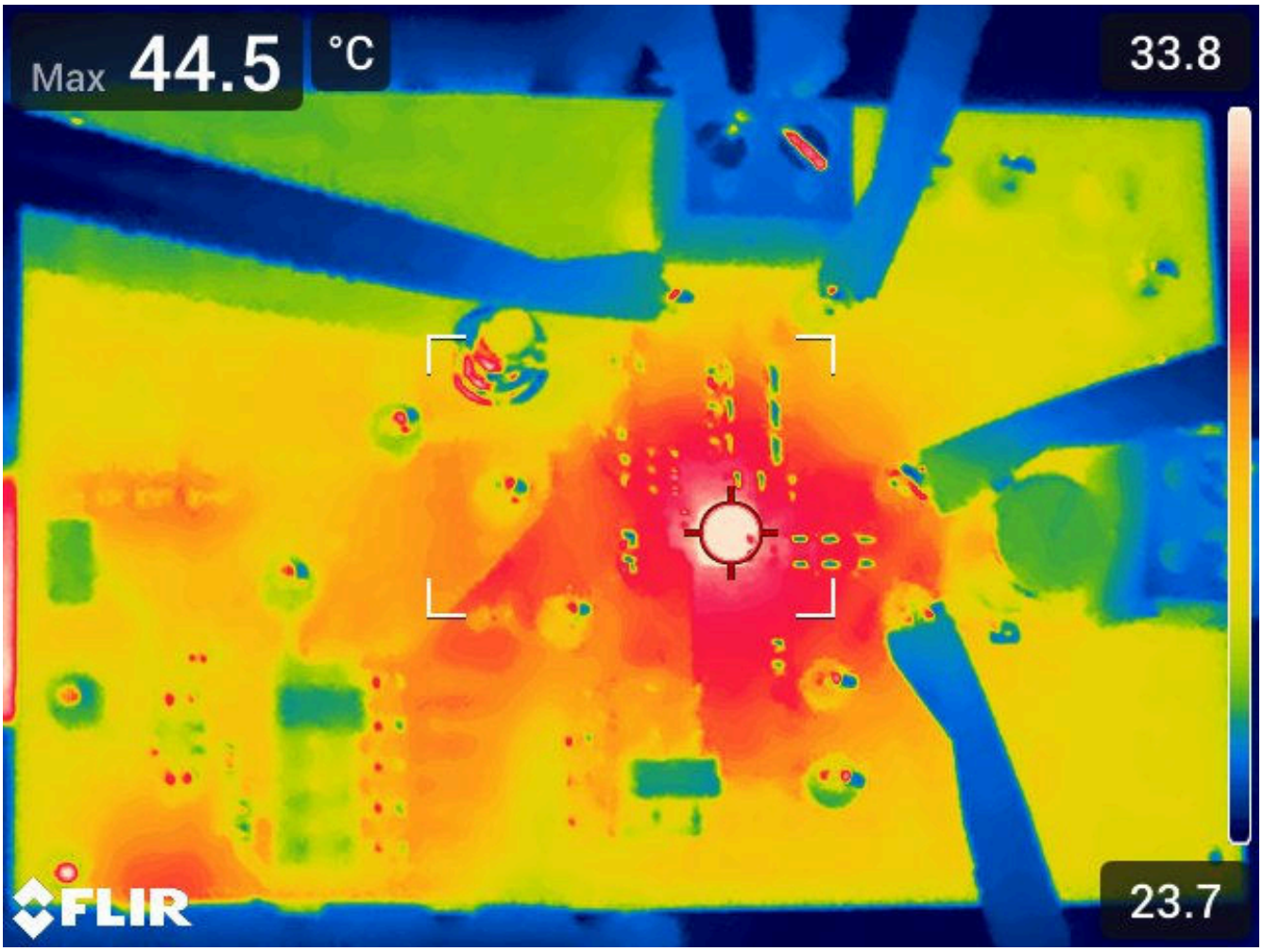


図 7-20. Thermal Image at 25°C Ambient

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (December 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM843320SITR	Active	Production	uSiP (SIT) | 15	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	T43320
TPSM843320SITR.A	Active	Production	uSiP (SIT) | 15	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	T43320

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

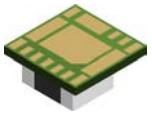
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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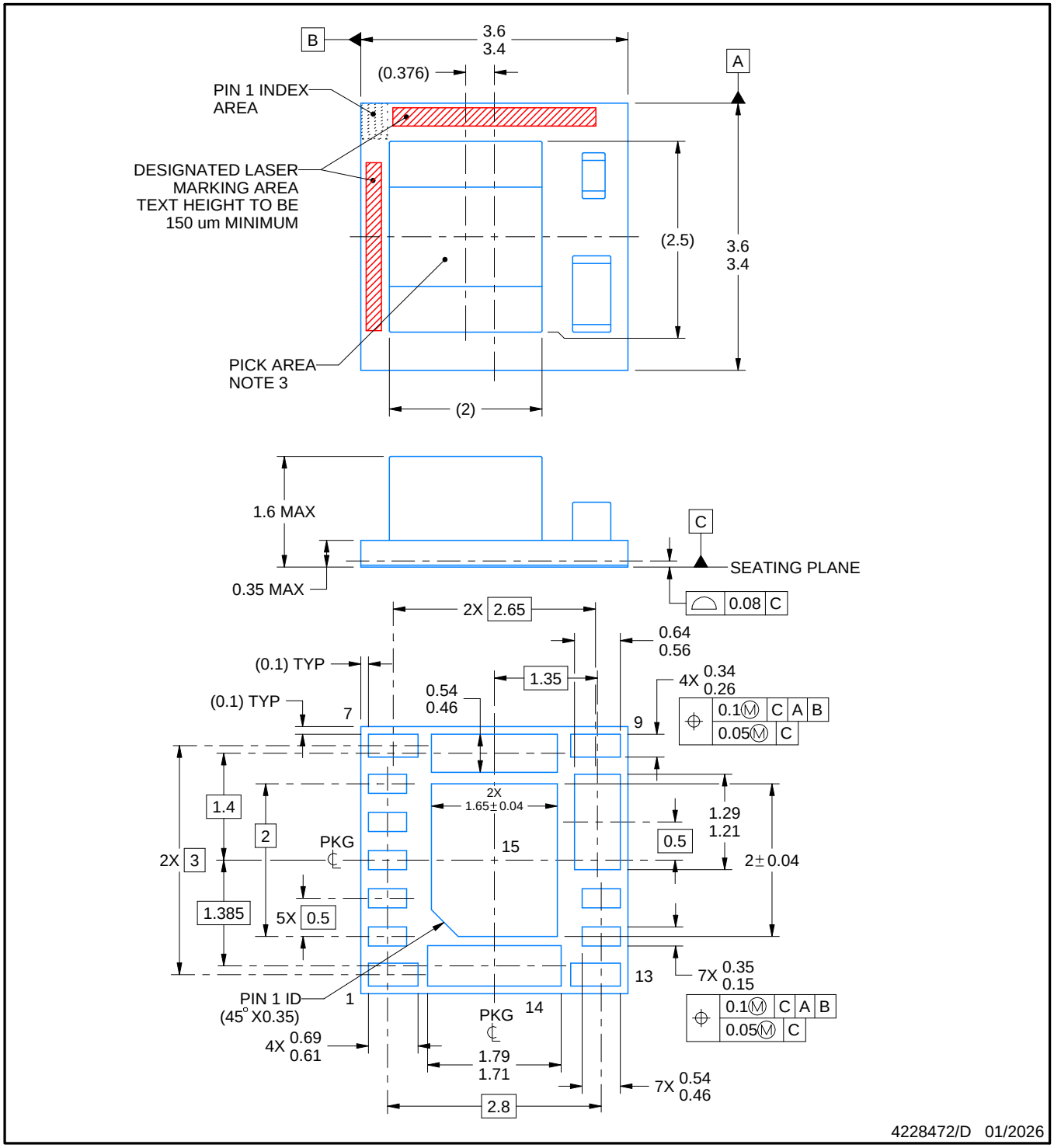


PACKAGE OUTLINE

SIT0015A

MicroSiP™ - 1.6 mm max height

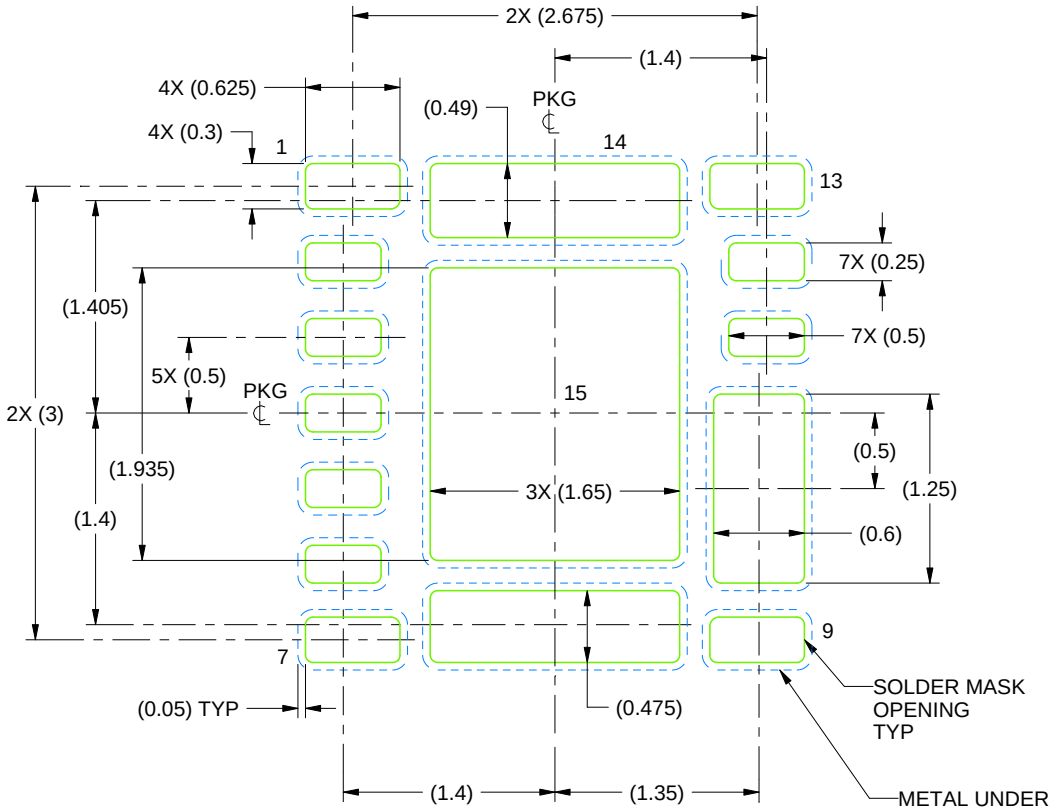
MICRO SYSTEM IN PACKAGE



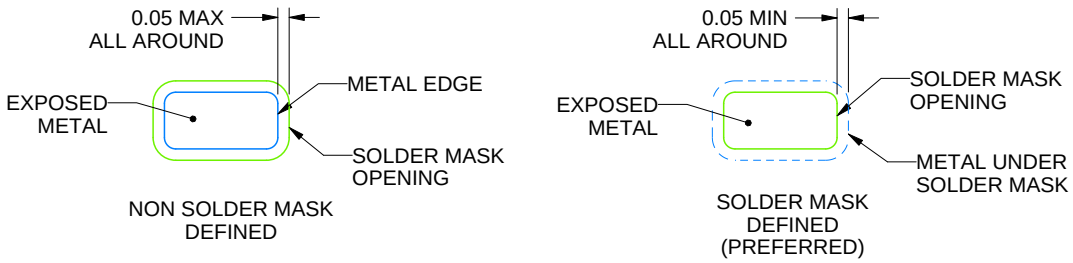
MicroSiP is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

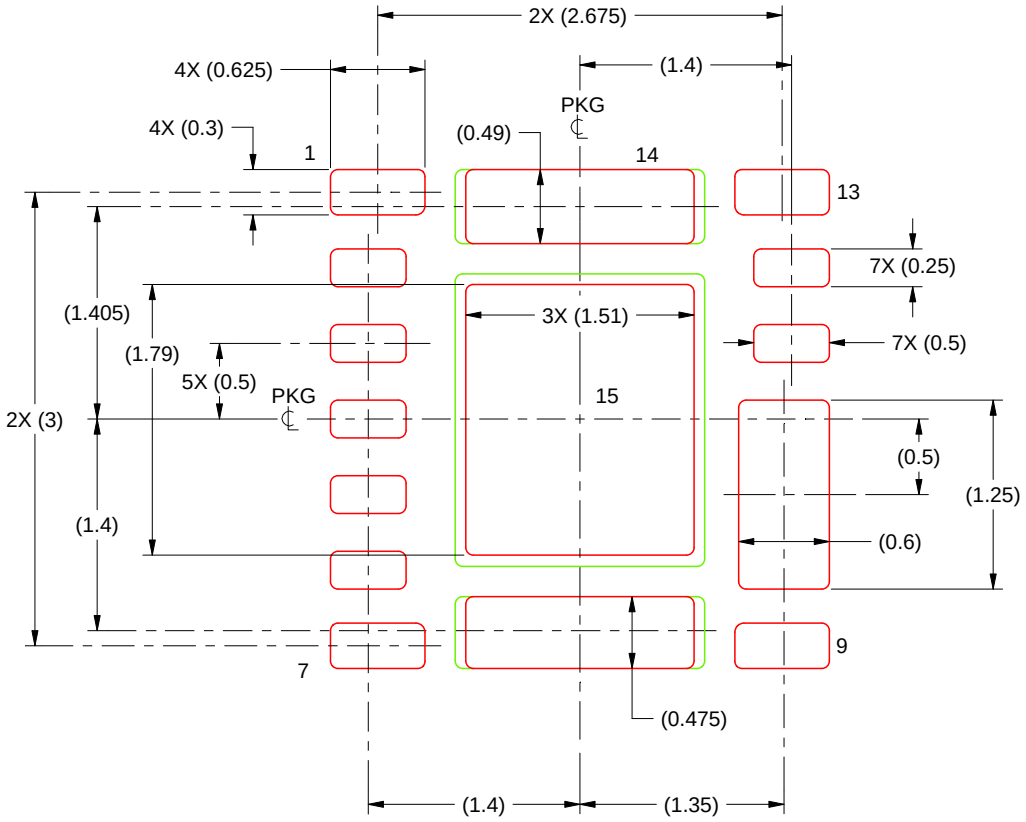


SOLDER MASK DETAILS
NOT TO SCALE

4228472/D 01/2026

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 8: 92%
PAD 14: 92%
PAD: 15: 85%

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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