TEXAS INSTRUMENTS
TPSM84624
JAJSER3B – FEBRUARY 2018 – REVISED APRIL 2018

# TPSM84624 4.5V～17V入力、0.6V～10V出力、6A電源モジュール

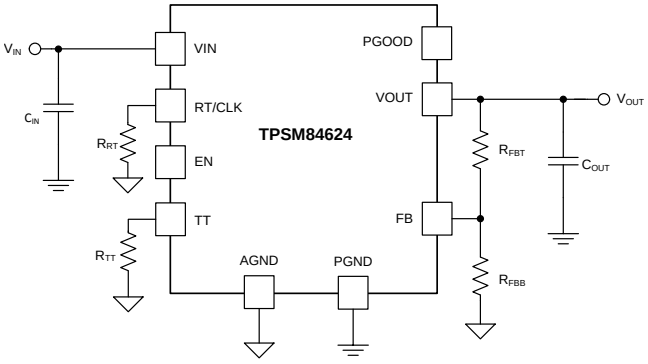
## 1 特長

- インダクタ内蔵の電源ソリューション
- 7.5mm×7.5mm×5.3mm QFNパッケージ
  - すべてのピンはパッケージ周辺からアクセス可能
- 入力電圧範囲: 4.5V～17V
- 広い出力電圧範囲: 0.6V～10V
- 最高96%の効率
- 調整可能な固定スイッチング周波数 (200kHz～1.6MHz)
- 外部クロックに同期可能
- 超高速の負荷ステップ応答 (TurboTrans™)
- パワー・グッド出力
- EN55011 Class B放射EMI制限に合致
- 動作時周囲温度範囲: -40℃～+105℃
- 動作時IC接合部温度範囲: -40℃～+150℃
- WEBENCH® Power Designerにより、TPSM84624を使用するカスタム設計を作成

## 2 アプリケーション

- 電気通信および無線インフラストラクチャ
- 産業用自動化試験装置
- エンタープライズ向けスイッチング/ストレージ・アプリケーション
- 高密度分散電源システム

### 概略回路図




Copyright © 2018, Texas Instruments Incorporated

## 3 概要

TPSM84624電源モジュールは、6AのDC/DCコンバータをパワーMOSFET、シールド付きインダクタ、パッシブ部品とともに小型のQFMパッケージに実装した、使いやすい集積電源です。この電源ソリューションは、わずか6個の外付け部品で動作し、個々の設計要件に応じて主要なパラメータを変更することもできます。また TurboTrans™機能を使用して、超高速の過渡応答を実現できます。TurboTransによって、出力電圧偏差を低減するように過渡応答を最適化し、必要な出力容量を削減することができます。

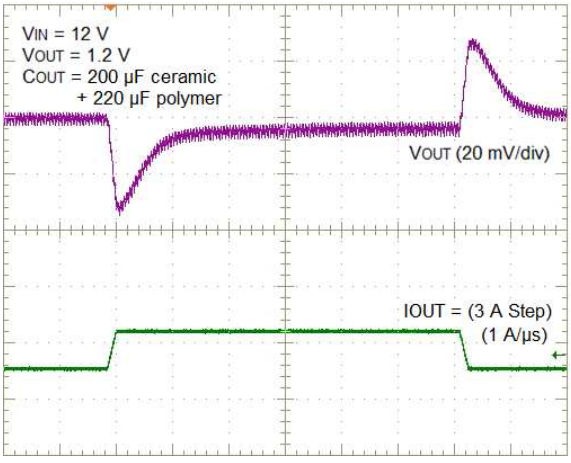
7.5mm×7.5mm×5.3mm、24ピンのQFMパッケージはプリント基板に簡単にハンダ付けでき、消費電力特性が非常に優れています。TPSM84624はパワー・グッド、プログラマブルUVLO、トラッキング、プリバイアス・スタートアップ、過電流および過熱保護など、数多くの機能を備えた柔軟性の高い製品であるため、多種多様なデバイスやシステムの電源に適しています。

### 製品情報(1)

| デバイス番号 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| TPSM84624 | QFM (24) | 7.50mm×7.50mm |

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 過渡応答




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# 目次

**1** 特長 ... 1
**2** アプリケーション ... 1
**3** 概要 ... 1
**4** 改訂履歴 ... 2
**5** **Pin Configuration and Functions** ... 3
**6** **Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 7
6.7 Typical Characteristics ($V_{IN}$ = 12 V) ... 8
6.8 Typical Characteristics ($V_{IN}$ = 5 V) ... 9
**7** **Detailed Description** ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 20
**8** **Application and Implementation** ... 21
8.1 Application Information ... 21
8.2 Typical Application ... 21
**9** **Power Supply Recommendations** ... 23
**10** **Layout** ... 24
10.1 Layout Guidelines ... 24
10.2 Layout Examples ... 24
10.3 EMI ... 25
10.4 Package Specifications ... 26
**11** デバイスおよびドキュメントのサポート ... 27
11.1 デバイス・サポート ... 27
11.2 WEBENCH®ツールによるカスタム設計 ... 27
11.3 ドキュメントの更新通知を受け取る方法 ... 27
11.4 コミュニティ・リソース ... 27
11.5 商標 ... 27
11.6 静電気放電に関する注意事項 ... 27
11.7 Glossary ... 28
**12** メカニカル、パッケージ、および注文情報 ... 28

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision A (March 2018)** から **Revision B** に変更 **Page**

- 追加 inductor value to the block diagram ... 10
- 変更 $V_{OUT}$ Range vs Switching Frequency table ... 12
- 追加 270 µF capacitor to the Allowable Polymer Capacitor table ... 15
- 追加 *EMI* section ... 25

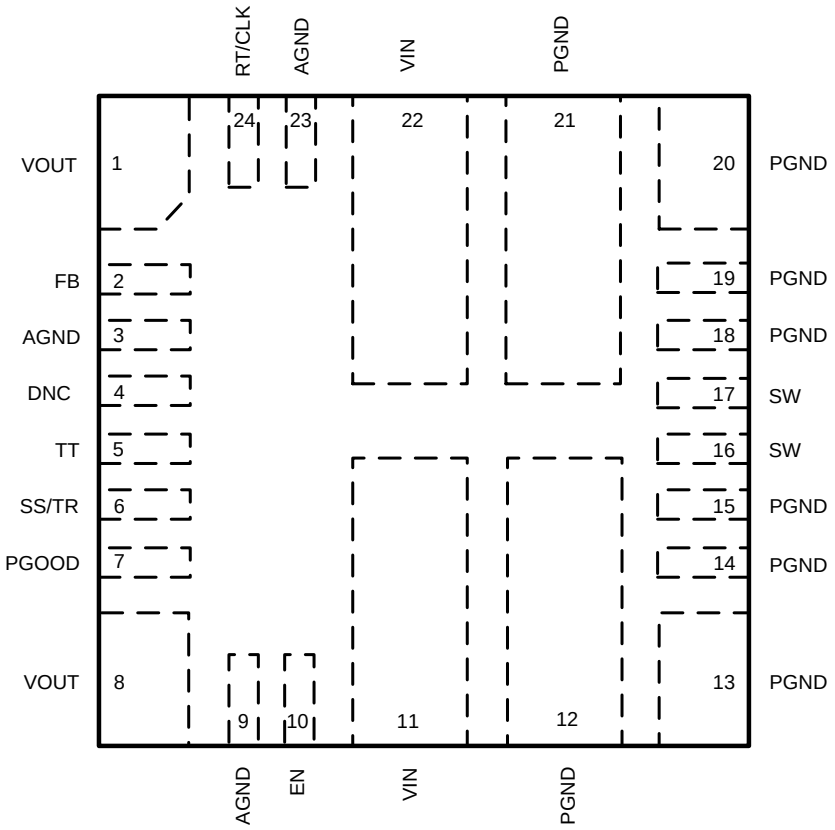
**2018年2月**発行のものから更新 **Page**

- 生産データを用いたデータシートの初版 ... 1


Copyright © 2018, Texas Instruments Incorporated

# 5 Pin Configuration and Functions

**MOL Package**
**24-Pin QFM**
**Top View**




**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 3, 9, 23 | G | Analog ground. Zero voltage reference for internal references and logic. These pins should be connected to one another externally using an analog ground plane on the PCB. Do not connect this pin to PGND; the connection is made internal to the device. |
| DNC | 4 | | Do Not Connect. Do not connect this pin to AGND, PGND, or to any other voltage. This pin is connected to internal circuitry. |
| EN | 10 | I | Enable. Float or pull high to enable the device. Connect a resistor divider to this pin to implement adjustable undervoltage lockout and hysteresis. |
| FB | 2 | I | Feedback input of the regulator. Connect the output voltage feedback resistor divider to this pin. |
| PGND | 12, 13, 14, 15, 18, 19, 20, 21 | G | Power ground. This is the return current path for the power stage of the device. Connect these pins to the input source, the load, and to the bypass capacitors associated with VIN and VOUT using power ground planes on the PCB. Pads 12 and 21 should be connected to the ground planes using multiple vias for improved thermal performance. |
| PGOOD | 7 | O | Power-Good flag. This open drain output asserts low if the output voltage is outside of the PGOOD thresholds, VIN is lower than its UVLO threshold, EN is low, device is in thermal shutdown or device is in soft-start. Use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 6.5 V. |
| RT/CLK | 24 | I | Switching frequency setting pin. In RT mode, an external timing resistor adjusts the switching frequency. In CLK mode, the device synchronizes to an external clock input to this pin. |
| SS/TR | 6 | I | Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.25-ms default setting. A voltage applied to this pin allows for tracking and sequencing control. |

(1) G = Ground, I = Input, O = Output

Copyright © 2018, Texas Instruments Incorporated

## Pin Functions (continued)

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SW | 16, 17 | O | Switch node. Do not place any external components on these pins or tie them to a pin of another function. |
| TT | 5 | I | TurboTrans pin. Internal loop compensation network. Connect the required TurboTrans resistor between this pin and AGND. See the *TurboTrans (TT)* section for the value of the resistor. Do not leave this pin floating. |
| VIN | 11, 22 | I | Input voltage. Supplies voltage to the power switches of the converter and all of the internal circuitry. Connect these pins to the input source and connect external input capacitors between these pins and PGND, close to the device. These pins should be connected to internal VIN layers using multiple vias for improved thermal performance. |
| VOUT | 1, 8 | O | Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND, close to the device, and connect these pins to internal VOUT layers using multiple vias for improved thermal performance. |


Copyright © 2018, Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN | –0.3 | 19 | V |
| | EN, PGOOD, SS/TRK, RT/CLK, FB | –0.3 | 6.5 | V |
| | AGND to PGND | –0.3 | 0.3 | V |
| Output voltage | SW | –1 | $V_{IN}$ + 1 | V |
| | SW (< 10-ns transients) | –3 | $V_{IN}$ + 3 | V |
| | VOUT | –0.3 | $V_{IN}$ | V |
| Mechanical shock | Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted | | 500 | G |
| Mechanical vibration | Mil-STD-883D, Method 2007.2, 20 to 2000 Hz | | 10 | G |
| Operating IC junction temperature, $T_J$ (2) | | –40 | 150 | °C |
| Operating ambient temperature, $T_A$ (2) | | –40 | 105 | °C |
| Storage temperature, $T_{stg}$ | | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage, $V_{IN}$ | 4.5(1) | 17 | V |
| Output voltage, $V_{OUT}$ | 0.6 | 10 | V |
| EN voltage, $V_{EN}$ | 0 | 5.5 | V |
| PGOOD pullup voltage, $V_{PGOOD}$ | | 5.5 | V |
| PGOOD sink current, $I_{PGOOD}$ | | 1 | mA |
| RT/CLK voltage range, $V_{CLK}$ | 0 | 5.5 | V |
| Output current, $I_{OUT}$ | 0 | 6 | A |
| Operating ambient temperature, $T_A$ | –40 | 105 | °C |

(1) For output voltages 0.6 V to < 5.5 V, the recommended minimum $V_{IN}$ is 4.5 V or ($V_{OUT}$ + 1 V), whichever is greater. For output voltages 5.5 V to < 9 V, the recommended minimum $V_{IN}$ is ($V_{OUT}$ + 2 V). For output voltages 9 V to 10 V, the recommended minimum $V_{IN}$ is ($V_{OUT}$ + 3 V).

Copyright © 2018, Texas Instruments Incorporated

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPSM84624 MOL (QFN) 24 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[2] | 22 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter[3] | 2.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter[4] | 13.6 | °C/W |

(1) For more information about thermal metrics, see the *Semiconductor and IC PackageThermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 100 mm × 100 mm, 4-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top board characterization parameter, $\psi_{JT}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and $T_T$ is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and $T_B$ is the temperature of the board 1mm from the device.

## 6.5 Electrical Characteristics

Over –40°C to +105°C ambient temperature, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = $I_{OUT}$max, $f_{sw}$ = 450 kHz (unless otherwise noted); $C_{IN1}$ = 2× 10-µF, 25-V, 1210 ceramic; $C_{IN2}$ = 100-µF, 50-V, electrolytic; $C_{OUT}$ = 4× 47-µF, 10-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **INPUT VOLTAGE ($V_{IN}$)** | | | | | | | |
| $V_{IN}$ | Input voltage | Over $I_{OUT}$ range | | 4.5[1] | | 17 | V |
| UVLO | $V_{IN}$ undervoltage lockout | $V_{IN}$ increasing | | | 4.1 | 4.3 | V |
| | | $V_{IN}$ decreasing | | 3.7 | 3.9 | | V |
| $I_{SHDN}$ | Shutdown supply current | $V_{EN}$ = 0 V | | | 3 | 11 | µA |
| **OUTPUT VOLTAGE ($V_{OUT}$)** | | | | | | | |
| $V_{OUT(ADJ)}$ | Output voltage adjust | Over $I_{OUT}$ range | | 0.6 | | 10 | V |
| $V_{OUT(Ripple)}$ | Output voltage ripple | 20-MHz bandwidth | | | 16 | | mV |
| **FEEDBACK** | | | | | | | |
| $V_{FB}$ | Feedback voltage[2] | $T_A$ = 25°C, $I_{OUT}$ = 0 A | | 0.596 | 0.6 | 0.604 | V |
| | | –40°C ≤ $T_J$ ≤ 125°C, $I_{OUT}$ = 0 A | | 0.595 | 0.6 | 0.605 | V |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 0 A | | | 0.1 | | mV |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C | | | 0.8 | | mV |
| **CURRENT** | | | | | | | |
| $I_{OUT}$ | Output current | Natural convection, $T_A$ = 25°C | | 0 | | 6 | A |
| | Overcurrent threshold | | | | 11 | | A |
| **PERFORMANCE** | | | | | | | |
| η | Efficiency | $V_{IN}$ = 12 V, $I_{OUT}$ = 4 A | $V_{OUT}$ = 5 V, $f_{SW}$ = 1.2 MHz | | 94% | | |
| | | | $V_{OUT}$ = 3.3 V, $f_{SW}$ = 1.0 MHz | | 93% | | |
| | | | $V_{OUT}$ = 1.8 V, $f_{SW}$ = 600 kHz | | 91% | | |
| | | | $V_{OUT}$ = 1.2 V, $f_{SW}$ = 450 kHz | | 87% | | |
| | | | $V_{OUT}$ = 1 V, $f_{SW}$ = 400 kHz | | 86% | | |
| | Transient response voltage deviation | 25% to 75% load step, 2A/µs slew rate, $R_{TT}$ = 4.02 kΩ, $C_{OUT}$ = 200-µF ceramic + 220-µF polymer | | | 41 | | mV |
| | | 25% to 75% load step, 2A/µs slew rate, $R_{TT}$ = 8.87 kΩ, $C_{OUT}$ = 400-µF ceramic | | | 33 | | mV |

(1) For output voltages 0.6 V to < 5.5 V, the recommended minimum $V_{IN}$ is 4.5 V or ($V_{OUT}$ + 1 V), whichever is greater. For output voltages 5.5 V to < 9 V, the recommended minimum $V_{IN}$ is ($V_{OUT}$ + 2 V). For output voltages 9 V to 10 V, the recommended minimum $V_{IN}$ is ($V_{OUT}$ + 3 V).
(2) The overall output voltage tolerance will be affected by the tolerance of the external $R_{FBT}$ and $R_{FBB}$ resistors.


Copyright © 2018, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Over –40°C to +105°C ambient temperature, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = $I_{OUT}$max, $f_{sw}$ = 450 kHz (unless otherwise noted); $C_{IN1}$ = 2× 10-µF, 25-V, 1210 ceramic; $C_{IN2}$ = 100-µF, 50-V, electrolytic; $C_{OUT}$ = 4× 47-µF, 10-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SOFT START** | | | | | | |
| $t_{SS}$ | Internal soft start time | | | 1.25 | | ms |
| $I_{SS}$ | Soft start charge current | | | 5 | | µA |
| **THERMAL** | | | | | | |
| $T_{SHDN}$ | Thermal shutdown | Shutdown temperature | | 170 | | °C |
| | | Hysteresis | | 15 | | °C |
| **ENABLE (EN)** | | | | | | |
| $V_{EN-H}$ | EN rising threshold | | | 1.2 | 1.26 | V |
| $V_{EN-HYS}$ | EN falling threshold | | 1.1 | 1.15 | | V |
| $I_{EN}$ | EN pin sourcing current | $V_{EN}$ = 1.1 V | | 1.2 | | µA |
| | | $V_{EN}$ = 1.3 V | | 3.6 | | µA |
| **POWER GOOD (PGOOD)** | | | | | | |
| $V_{PGOOD}$ | PGOOD thresholds | $V_{OUT}$ rising (fault) | | 108% | | |
| | | $V_{OUT}$ falling (good) | | 106% | | |
| | | $V_{OUT}$ rising (good) | | 91% | | |
| | | $V_{OUT}$ falling (fault) | | 89% | | |
| | Minimum $V_{IN}$ for valid PGOOD | $V_{PGOOD}$ < 0.5 V, $I_{PGOOD}$ = 2 mA | | 0.7 | 1 | V |
| | PGOOD low voltage | 2-mA pullup, $V_{EN}$ = 0 V | | | 0.3 | V |
| **CAPACITANCE** | | | | | | |
| $C_{IN}$ | External input capacitance | Ceramic type | 20(3) | | | µF |
| | | Non-ceramic type | | 100(3) | | µF |
| $C_{OUT}$ | External output capacitance | | min(4) | | 1500(5) | µF |

(3) A minimum of 20-µF ceramic input capacitance is required for proper operation. An additional 100 µF of bulk capacitance is recommended for applications with transient load requirements. See the *Input Capacitor* section for further guidance.
(4) The minimum amount of required output capacitance varies depending on the output voltage (see Standard Component Values Table). A minimum amount of ceramic output capacitance is required. Locate the capacitance close to the device. Adding additional ceramic or non-ceramic capacitance close to the load improves the response of the regulator to load transients.
(5) The maximum output capacitance can be made up of all ceramic type or a combination of ceramic and a single non-ceramic type. See the *Low-ESR Output Capacitors Section* for requirements of non-ceramic output capacitors.

## 6.6 Switching Characteristics

Over operating ambient temperature range (unless otherwise noted)
Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm, and are provided for reference only.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SW** | | | | | | |
| $t_{ON_MIN}$ | Minimum on-time | | | | 140 | ns |
| $t_{OFF_MIN}$ | Minimum off-time | | | | 100 | ns |
| **FREQUENCY (RT) and SYNCHRONIZATION (EN/SYNC)** | | | | | | |
| $f_{SW}$ | Default switching frequency | RT pin = 110 kΩ | 400 | 450 | 500 | kHz |
| | Switching frequency range | | 200 | | 1600 | kHz |
| $V_{CLK-H}$ | Logic high input voltage | | 2 | | | V |
| $V_{CLK-L}$ | Logic low input voltage | | | | 0.8 | V |
| $T_{CLK-MIN}$ | Minimum CLK pulse width | | 35 | | | ns |

Copyright © 2018, Texas Instruments Incorporated

## 6.7 Typical Characteristics ($V_{IN}$ = 12 V)

$T_A$ = 25°C, unless otherwise noted.

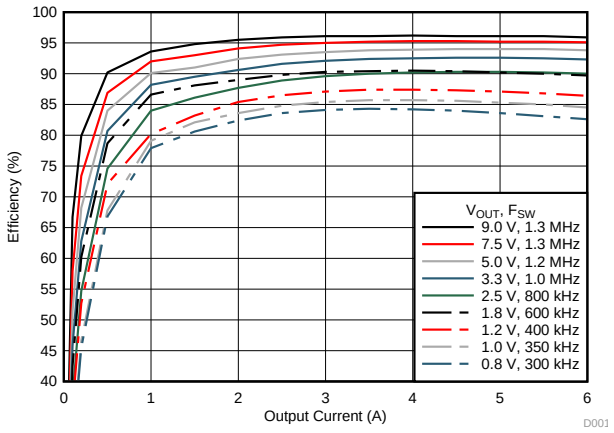



**図 1. Efficiency vs Output Current**

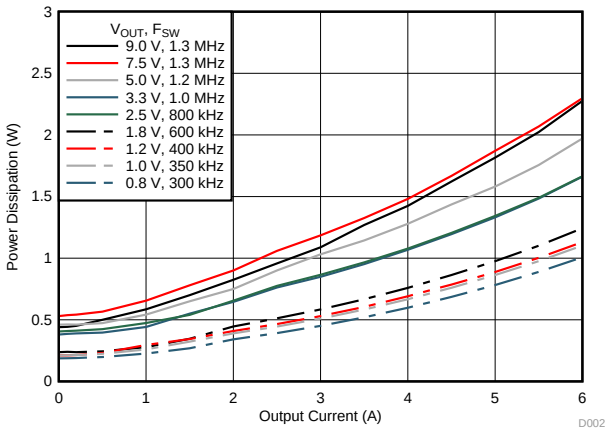
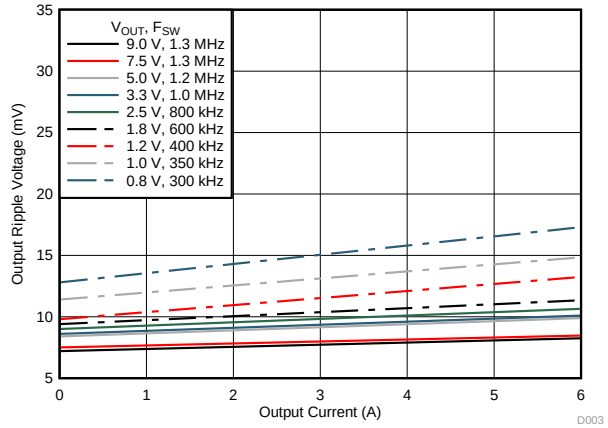
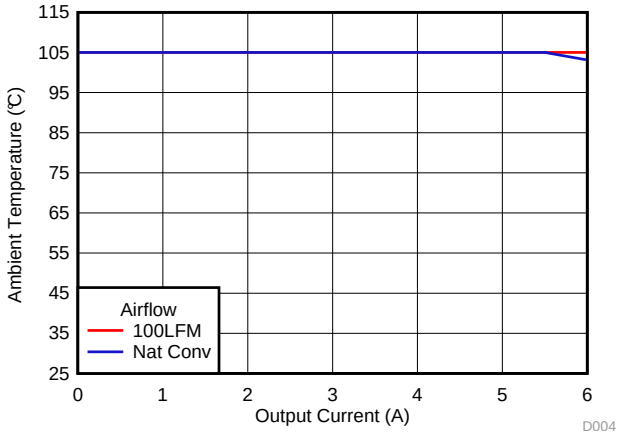



**図 2. Power Dissipation vs Output Current**



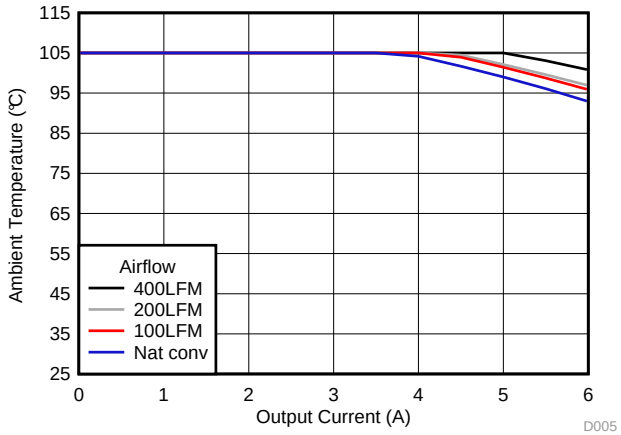

$C_{OUT}$ = 200 µF

**図 3. Ripple Voltage vs Output Current**



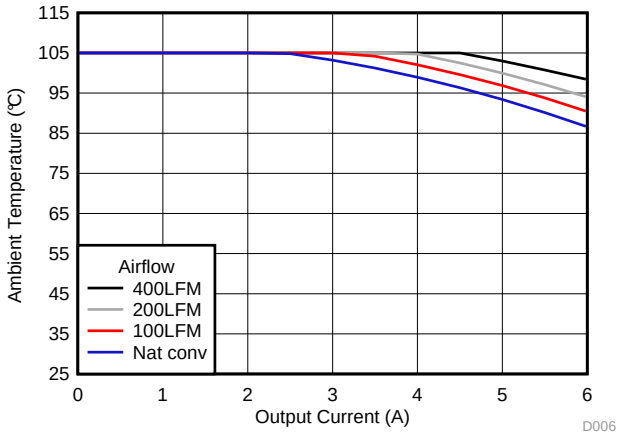

$V_{OUT}$ = 1.2 V $f_{SW}$ = 450 kHz

**図 4. Safe Operating Area**




$V_{OUT}$ = 3.3 V $f_{SW}$ = 1 MHz

**図 5. Safe Operating Area**




$V_{OUT}$ = 5 V $f_{SW}$ = 1.2 MHz

**図 6. Safe Operating Area**


Copyright © 2018, Texas Instruments Incorporated

## 6.8 Typical Characteristics ($V_{IN}$ = 5 V)

$T_A$ = 25°C, unless otherwise noted.

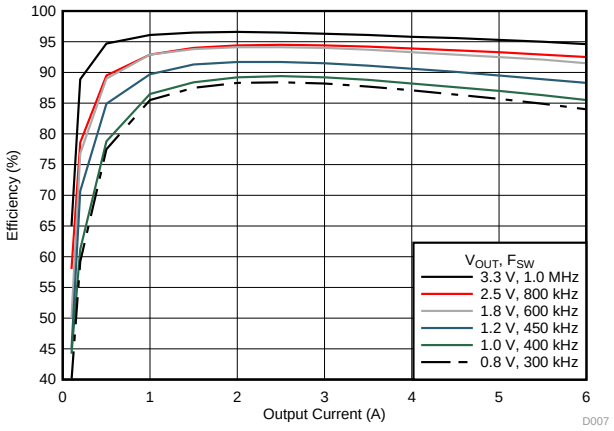



図 7. Efficiency vs Output Current

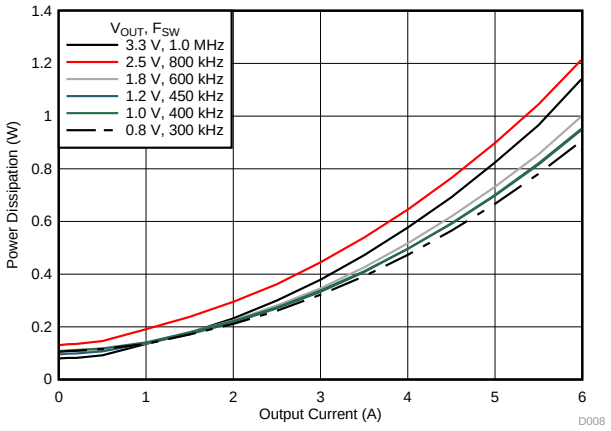
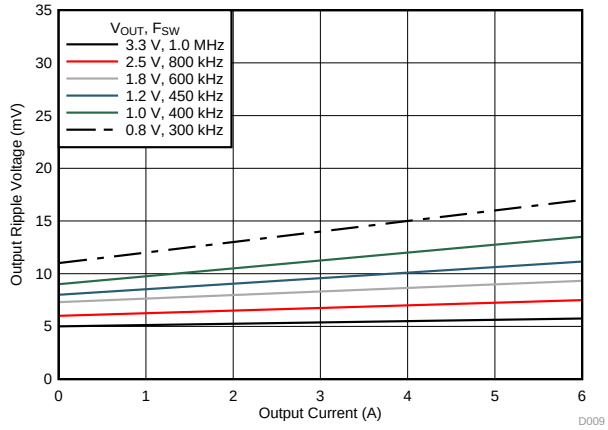
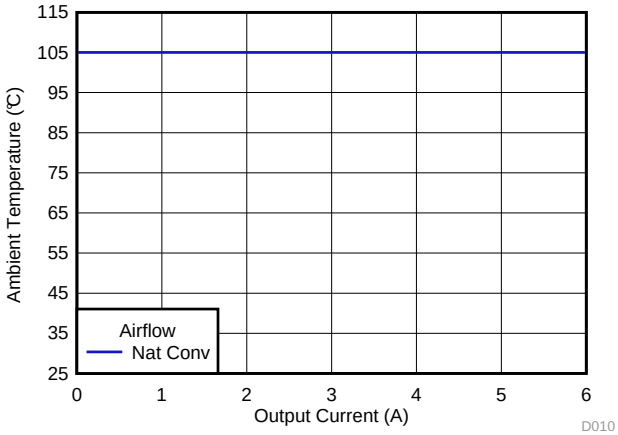



図 8. Power Dissipation vs Output Current



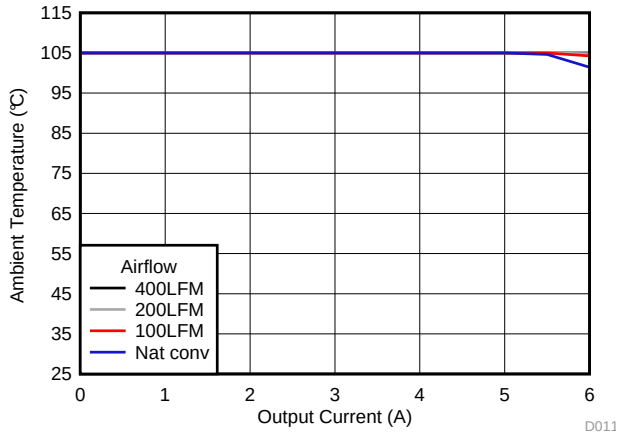

$V_{OUT}$ = 1.2 V $f_{SW}$ = 450 kHz

図 9. Ripple Voltage vs Output Current




$V_{OUT}$ ≤ 1.8 V

図 10. Safe Operating Area




$V_{OUT}$ = 3.3 V $f_{SW}$ = 1 MHz

図 11. Safe Operating Area

Copyright © 2018, Texas Instruments Incorporated

# 7 Detailed Description

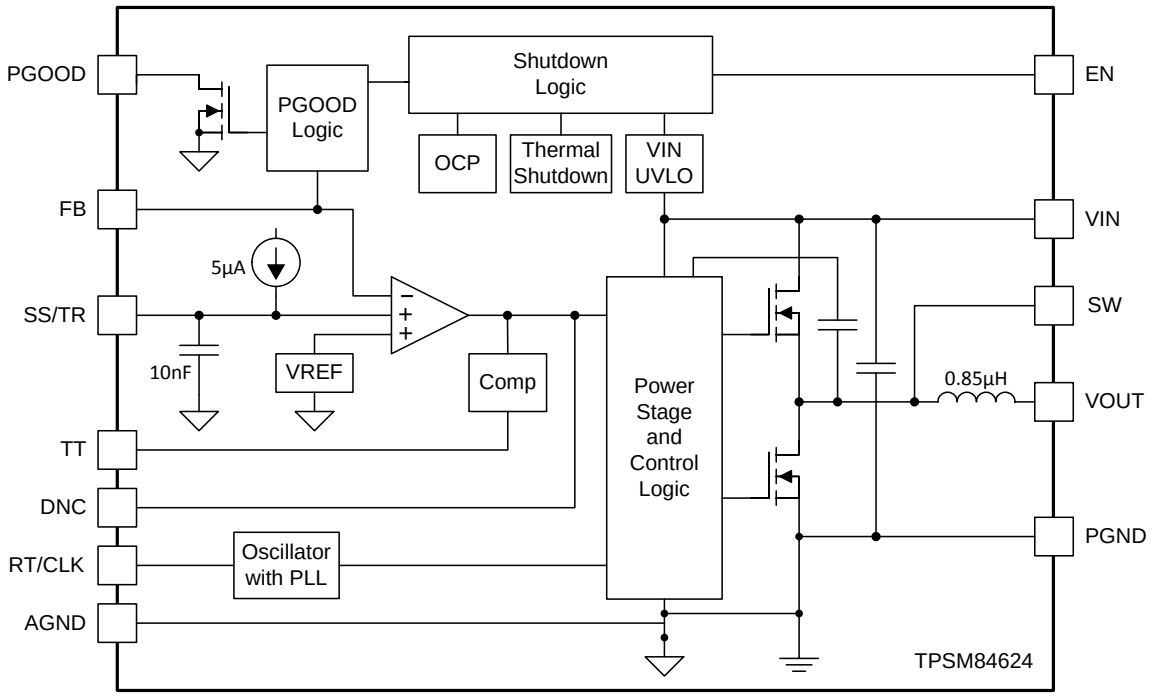
## 7.1 Overview

The TPSM84624 is a full-featured 4.5-V to 17-V input, 6-A, synchronous step-down converter with PWM, MOSFETs, inductor, and control circuitry integrated into a low-profile package. The device integration enables small designs, while still leaving the ability to adjust key parameters to meet specific design requirements. The TPSM84624 provides an output voltage range of 0.6 V to 10 V. An external resistor divider is used to adjust the output voltage to the desired output. The switching frequency is also adjustable by using an external resistor or a synchronization clock to accommodate various input and output voltage conditions and to optimize efficiency.

The TPSM84624 includes the TurboTrans feature which optimizes the transient response of the converter while simultaneously reducing the quantity of external output capacitors required to meet a target voltage deviation specification.

The TPSM84624 has been designed for safe start-up into pre-biased loads. The default start-up is when $V_{IN}$ is typically 4.1 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the internal pullup current of the EN pin allows the device to operate with the EN pin floating. The EN pin can also be pulled low to put the device in standby mode to reduce input quiescent current. The device provides a power-good (PGOOD) signal to indicate when the output voltage is within regulation. Thermal shutdown and current limit features protect the device during an overload condition. A 24-pin QFM package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

## 7.2 Functional Block Diagram




Copyright © 2018, Texas Instruments Incorporated


Copyright © 2018, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 2) programs the output voltage of the TPSM84624. The output voltage adjustment range is from 0.6 V to 10 V. 図 12 shows the feedback resistor connection for setting the output voltage. The recommended value of $R_{FBT}$ is 10 kΩ. The value for $R_{FBB}$ can be calculated using 式 1 or simply selected from the range of values given in 表 1. 表 1 also includes the recommended switching frequency and minimum required output capacitance for each output voltage.

$$R_{FBB} = \frac{6}{(V_{OUT} - 0.6)} \quad (k\Omega) \tag{1}$$

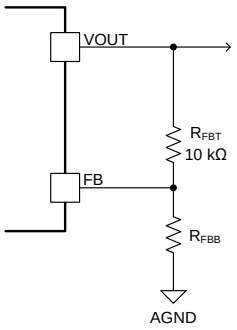



**図 12. Setting the Output Voltage**

**表 1. Standard Component Values**

| $V_{OUT}$ (V) | $R_{FBB}$ (kΩ) | RECOMMENDED $f_{SW}$ (kHz) | $R_{RT}$ (kΩ) | Minimum Required $C_{OUT}$(µF)(1)(2) | |
|---|---|---|---|---|---|
| | | | | CERAMIC | POLYMER(3) |
| 0.6 | open | 250 | 200 | 400 | 220 |
| 0.7 | 60.4 | 250 | 200 | 400 | 220 |
| 0.8 | 30.1 | 300 | 165 | 300 | 220 |
| 0.9 | 20.0 | 350 | 143 | 200 | 220 |
| 1.0 | 15.0 | 400 | 124 | 200 | - |
| 1.1 | 12.1 | 400 | 124 | 200 | - |
| 1.2 | 10.0 | 450 | 110 | 200 | - |
| 1.3 | 8.66 | 500 | 97.6 | 200 | - |
| 1.4 | 7.50 | 500 | 97.6 | 200 | - |
| 1.5 | 6.65 | 550 | 88.7 | 150 | - |
| 1.6 | 6.04 | 550 | 88.7 | 150 | - |
| 1.7 | 5.49 | 600 | 82.5 | 150 | - |
| 1.8 | 4.99 | 600 | 82.5 | 100 | - |
| 1.9 | 4.64 | 650 | 75.0 | 100 | - |
| 2.0 | 4.32 | 700 | 69.8 | 100 | - |
| 2.5 | 3.16 | 800 | 60.4 | 100 | - |
| 3.3 | 2.21 | 1000 | 48.7 | 47 | - |
| 5.0 | 1.37 | 1200 | 40.2 | 47 | - |
| 6.0 | 1.10 | 1200 | 40.2 | 47 | - |
| 7.5 | 0.866 | 1300 | 36.5 | 47 | - |
| 9.0 | 0.715 | 1300 | 36.5 | 22 | - |
| 10 | 0.634 | 1300 | 36.5 | 22 | - |

(1) Additional capacitance above the minimum can be ceramic or polymer type.
(2) Load transients with > 2 A/µs slew rates or load steps exceeding 4 A may require additional capacitance, see *TurboTrans*.
(3) See *Low-ESR Output Capacitors* for details on polymer capacitors.

Copyright © 2018, Texas Instruments Incorporated

### 7.3.2 Switching Frequency (RT)

The switching frequency range of the TPSM84624 is 200 kHz to 1.6 MHz. The switching frequency can easily be set by connecting a resistor ($R_{RT}$) between the RT pin and AGND. Use 式 2 to calculate the $R_{RT}$ value for a desired frequency or simply select from 表 2.

The switching frequency must be selected based on the output voltage setting of the device and the operating input voltage. See 表 2 for the allowable output voltage range for a given switching frequency.

$$R_{RT} = 58650 \times f_{SW}(kHz)^{-1.028} (k\Omega) \quad (2)$$

**表 2. $V_{OUT}$ Range vs Switching Frequency**

| SWITCHING FREQUENCY | $V_{IN}$ = 5 V (±10%) | | $V_{IN}$ = 12 V (±5%) | | $V_{IN}$ = 15 V (±5%) | |
|---|---|---|---|---|---|---|
| | $V_{OUT}$ RANGE (V) | | $V_{OUT}$ RANGE (V) | | $V_{OUT}$ RANGE (V) | |
| | min | max | min | max | min | max |
| 250 kHz | 0.6 | 0.9 | 0.6 | 0.8 | 0.6 | 0.8 |
| 300 kHz | 0.6 | 0.9 | 0.6 | 0.9 | 0.7 | 0.9 |
| 350 kHz | 0.6 | 1.0 | 0.7 | 1.0 | 0.8 | 1.0 |
| 400 kHz | 0.6 | 1.2 | 0.7 | 1.2 | 0.9 | 1.2 |
| 450 kHz | 0.6 | 1.8 | 0.8 | 1.5 | 1.0 | 1.5 |
| 500 kHz | 0.6 | 2.0 | 0.9 | 1.8 | 1.1 | 1.8 |
| 550 kHz | 0.6 | 2.2 | 1.0 | 2.0 | 1.2 | 2.0 |
| 600 kHz | 0.6 | 2.5 | 1.1 | 2.5 | 1.4 | 2.3 |
| 650 kHz | 0.6 | 3.0 | 1.2 | 2.7 | 1.5 | 2.5 |
| 700 kHz | 0.6 | 3.5 | 1.3 | 3.0 | 1.6 | 2.8 |
| 750 kHz | 0.6 | 3.5 | 1.4 | 3.3 | 1.7 | 3.0 |
| 800 kHz | 0.7 | 3.5 | 1.5 | 3.6 | 1.8 | 3.3 |
| 900 kHz | 0.7 | 3.5 | 1.6 | 4.0 | 2.0 | 4.0 |
| 1.0 MHz | 0.9 | 3.5 | 1.8 | 6.0 | 2.2 | 4.8 |
| 1.1 MHz | 1 | 3.5 | 2.0 | 9.0 | 2.5 | 6.0 |
| 1.2 MHz | 1.1 | 3.5 | 2.2 | 9.0 | 2.7 | 8.0 |
| 1.3 MHz | 1.1 | 3.5 | 2.3 | 9.0 | 2.9 | 10 |
| 1.4 MHz | 1.2 | 3.5 | 2.4 | 9.0 | 3.1 | 10 |
| 1.5 MHz | 1.3 | 3.5 | 2.6 | 9.0 | 3.3 | 10 |
| 1.6 MHz | 1.4 | 3.5 | 2.8 | 9.0 | 3.5 | 10 |

### 7.3.3 Synchronization (CLK)

The TPSM84624 switching frequency can also be synchronized to an external clock from 200 kHz to 1.6 MHz. Not all $V_{IN}$, $V_{OUT}$, and $I_{OUT}$ conditions can be set to all of the frequencies in this range due to on-time or off-time limitations. See *表 2* for the allowable operating ranges.

An internal Phase Locked Loop (PLL) has been implemented to allow synchronization and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin (pin 24) with a duty cycle from 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of the RT/CLK pin.

Before the external clock is present the device operates in RT mode and the switching frequency is set by the RT resistor, $R_{RT}$. Select $R_{RT}$ to set the frequency close to the external synchronization frequency. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2 V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock.

During operation, if the external clock is removed, the internal clock frequency begins to drop. After 10 μs without receiving a clock pulse, the device returns to RT mode. Output undershoot can occur while the switching frequency drops and returns to the frequency set by the RT resistor.


Copyright © 2018, Texas Instruments Incorporated

### 7.3.4 Output On/Off Enable (EN)

The EN pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low operating current state. The EN pin has an internal pullup current source allowing the user to float the EN pin for enabling the device.

If an application requires controlling the EN pin, either drive it directly with a logic input or use an open drain/collector device to interface with the pin. Applying a low voltage to the enable control (EN) pin disables the output of the supply, shown in 図 13. When the EN pin voltage exceeds the threshold voltage, the supply executes a soft-start power-up sequence, as shown in 図 14.

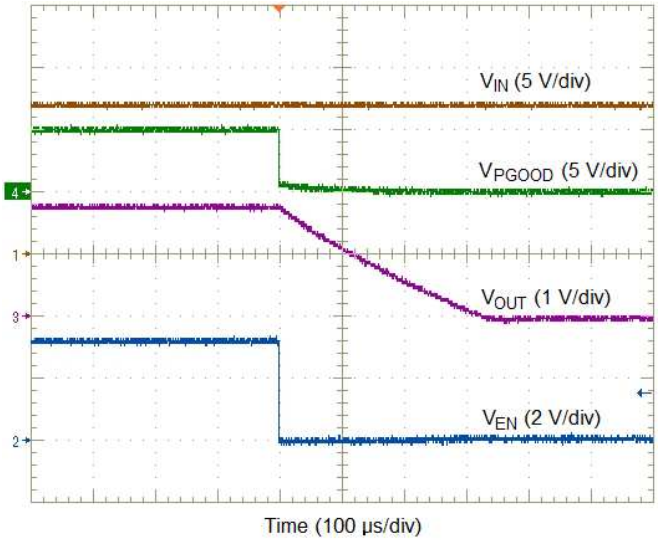



**図 13. Enable Turnoff**

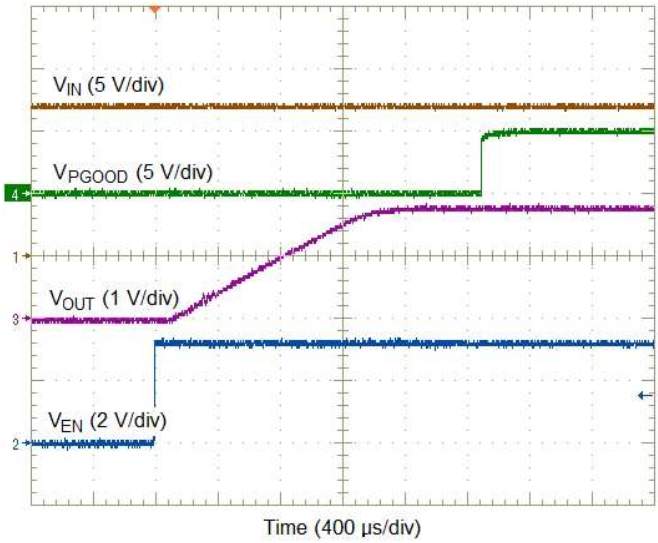



**図 14. Enable Turnon**

### 7.3.5 Input Capacitor Selection

The TPSM84624 requires a minimum input capacitance of 20 µF of ceramic type. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. TI recommends an additional 100 µF of non-ceramic capacitancefor applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate the derating of ceramic capactors, a voltage rating of twice the maximum input voltage is recommended. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 3 A(rms). 表 3 includes a preferred list of capacitors by vendor.

**表 3. Recommended Input Capacitors(1)**

| VENDOR | SERIES | PART NUMBER | CAPACITOR CHARACTERISTICS | | |
|---|---|---|---|---|---|
| | | | WORKING VOLTAGE (V) | CAPACITANCE (2) (µF) | ESR (3) (mΩ) |
| TDK | X7R | C3225X7R1E106K250AC | 25 | 10 | 2 |
| Murata | X7R | GRM32DR71E106KA12L | 25 | 10 | 2 |
| Panasonic | ZA | EEHZA1H101P | 50 | 100 | 28 |
| Panasonic | FC | EEUFC1H101B | 50 | 100 | 162 |

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR @ 100 kHz, 25°C.

Copyright © 2018, Texas Instruments Incorporated

### 7.3.6 Output Capacitor Selection

The minimum required output capacitance of the TPSM84624 is a function of the output voltage and is shown in 表 1. The required capacitance can be comprised of all ceramic capacitors or a combination of ceramic and low-ESR polymer type capacitors. When adding additional capacitors, low-ESR capacitors like the ones recommended in *Low-ESR Output Capacitors* are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See *TurboTrans (TT)* for typical transient response values for several output voltage and capacitance combinations. See 表 4 for recommended output capacitors.

**表 4. Recommended Output Capacitors(1)**

| VENDOR | SERIES | PART NUMBER | CAPACITOR CHARACTERISTICS | | |
|---|---|---|---|---|---|
| | | | WORKING VOLTAGE (V) | CAPACITANCE(2) (µF) | ESR(3) (mΩ) |
| TDK | X7R | C3225X7R1C226K | 16 | 22 | 2 |
| Murata | X7R | GCJ32ER71C226K | 16 | 22 | 2 |
| TDK | X5R | C3225X5R1C226M | 16 | 22 | 2 |
| Murata | X5R | GRM32ER61C226K | 16 | 22 | 2 |
| Murata | X7R | GCM32ER70J476K | 6.3 | 47 | 2 |
| Murata | X7R | GRM32ER71A476K | 10 | 47 | 2 |
| Murata | X5R | GRM32ER61C476K | 16 | 47 | 3 |
| TDK | X5R | C3225X5R0J107M | 6.3 | 100 | 2 |
| Murata | X5R | GRM32ER60J107M | 6.3 | 100 | 2 |
| Murata | X5R | GRM32ER61A107M | 10 | 100 | 2 |
| Panasonic | POSCAP | 4TPE220MF | 4.0 | 220 | 15 |
| Kemet | T520 | T520D227M006ATE015 | 6.3 | 220 | 15 |
| Panasonic | POSCAP | 6TPE330MAA | 6.3 | 330 | 10 |
| Kemet | T520 | T520D337M006ATE010 | 6.3 | 330 | 10 |
| Panasonic | POSCAP | 2R5TPE470M7 | 2.5 | 470 | 7 |
| Kemet | T520 | T520D477M2R5ATE007 | 2.5 | 470 | 7 |

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR @ 100 kHz, 25°C.


Copyright © 2018, Texas Instruments Incorporated

### 7.3.7 TurboTrans (TT)

The TPSM84624 includes the TurboTrans feature which optimizes the transient response of the converter while simultaneously reducing the quantity of external output capacitors required to meet a target voltage deviation specification. A TurboTrans resistor, $R_{TT}$, is required between the TT pin and AGND to properly set the response of the TPSM84624 based on the amount and type of output capacitors. The value of $R_{TT}$ can be calculated using 式 3. In order to calculate the $R_{TT}$ value, a TurboTrans constant, $K_{TT}$, is required. See 表 5 for the $K_{TT}$ value when using only ceramic output capacitors. See 表 6 for the $K_{TT}$ value when using a combination of ceramic and polymer output capacitors. Also, the value of $C_O$ used in 式 3 is the total ***effective*** output capacitance, which takes into account the effects of applied voltage and temperature.

$$R_{TT} = \left[\left(\frac{K_{TT} \times V_{OUT} \times C_{O(eff)}(\mu F)}{50}\right) - 2\right] \ (k\Omega) \tag{3}$$

**表 5. $K_{TT}$ Values (Ceramic Only Output Capacitors)**

| $V_{OUT}$ (V) | 1 - < 1.2 | 1.2 - < 1.5 | 1.5 - < 1.8 | 1.8 - < 2 | 2 - < 2.5 | 2.5 - < 3.3 | 3.3 - < 7.5 | 7.5 - 10 |
|---|---|---|---|---|---|---|---|---|
| $K_{TT}$ | 1 | 1.12 | 1.4 | 1.5 | 1.65 | 1.8 | 2.0 | 2.25 |

**表 6. $K_{TT}$ Values (Ceramic + Polymer Output Capacitors)**

| $V_{OUT}$ (V) | 0.6 - < 0.7 | 0.7 - < 0.9 | 0.9 - < 1 | 1 - < 2.5 | 2.5 - < 3.3 | 3.3 - < 5 | 5 - < 6 | 6 - < 7.5 | 7.5 - 10 |
|---|---|---|---|---|---|---|---|---|---|
| $K_{TT}$ | 0.6 | 0.65 | 0.7 | 0.6 | 0.72 | 0.9 | 1.2 | 1.5 | 1.8 |

#### *7.3.7.1 Low-ESR Output Capacitors*

When selecting non-ceramic output capacitors, the quality of the capacitor is important to maintain stable operation and optimize transient performance. The capacitance rating and the ESR rating are important when selecting these capacitors. Polymer type capacitors with capacitance and ESR in the range shown in 表 7 are required. Capacitors with lower ESR than the minimum listed in 表 7 can be used, however using capacitors with an ESR in the range listed will provide optimal transient performance.

If using a combination of ceramic and polymer type of output capacitance, only a ***single*** polymer capacitor can be used. Depending on the output voltage setting, only capacitors that meet the specifications listed in 表 7 can be used.

**表 7. Allowable Polymer Capacitor**

| $V_{OUT}$ RANGE | CAPACITANCE (µF) | ESR (mΩ) | |
|---|---|---|---|
| | | min | max |
| 0.6 V to < 3.3 V(1) | 220 | 12 | 15 |
| | 270 | 9 | 12 |
| | 330(1) | 7 | 10 |
| 3.3 V to ≤ 10 V | 150 | 15 | 25 |
| | 220 | 12 | 15 |
| | 270 | 9 | 12 |
| | 330 | 7 | 10 |

(1) Applications operating at input voltages > 15 V, output voltages < 3.3V, and temperatures below 0°C, the 330-µF capacitor is not recommended.

Copyright © 2018, Texas Instruments Incorporated

### 7.3.7.2 Transient Response

The TPSM84624 transient response is listed in 表 8 for several common output voltages with different capacitor combinations. The calculated $R_{TT}$ value is included in the table along with the typical voltage deviation for a 1.5 A and 3 A load step. All data was taken at the recommended switching frequency for each output voltage.

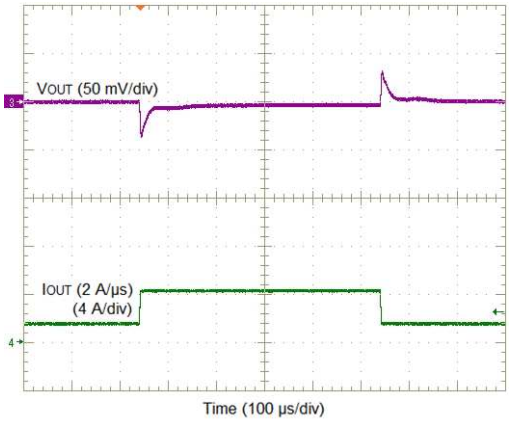
**表 8. Output Voltage Transient Response**

| $V_{IN}$ = 12 V, $C_{IN1}$ = 2x 10 µF Ceramic, $C_{IN2}$ = 100 µF Electrolytic, $T_A$ = 25°C | | | | | |
|---|---|---|---|---|---|
| $V_{OUT}$ (V) | $C_{OUT1}$ Ceramic | $C_{OUT2}$ BULK | $R_{TT}$ (kΩ) | VOLTAGE DEVIATION | |
| | | | | 1.5 A LOAD STEP | 3 A LOAD STEP |
| 0.8[1] | 300 µF | 220 µF | 3.40 | 17 mV (1.8%) | 34 mV (3.4%) |
| | 400 µF | 330 µF | 5.36 | 13 mV (1.4%) | 27 mV (2.3%) |
| 1[1] | 200 µF | - | 2.00 | 23 mV (2.3%) | 45 mV (4.5%) |
| | 200 µF | 220 µF | 3.01 | 17 mV (1.7%) | 34 mV (3.4%) |
| | 400 µF | - | 6.04 | 16 mV (1.6%) | 32 mV (3.2%) |
| | 400 µF | 220 µF | 5.49 | 15 mV (1.5%) | 30 mV (3%) |
| 1.2[1] | 200 µF | - | 3.40 | 26 mV (2.2%) | 52 mV (4.3%) |
| | 200 µF | 220 µF | 4.02 | 20 mV (1.7%) | 41 mV (3.4%) |
| | 400 µF | - | 8.87 | 16 mV (1.4%) | 33 mV (2.7%) |
| | 400 µF | 220 µF | 7.68 | 13 mV (1.1%) | 27 mV (2.2%) |
| 1.8[1] | 100 µF | - | 3.40 | 45 mV (2.5%) | 90 mV (5%) |
| | 300 µF | - | 14.3 | 17 mV (0.9%) | 34 mV (1.9%) |
| | 100 µF | 220 µF | 4.87 | 19 mV (1.1%) | 39 mV (2.2%) |
| 3.3[2] | 100 µF | - | 8.66 | 46 mV (1.4%) | 92 mV (2.8%) |
| | 100 µF | 220 µF | 31.6 | 23 mV (0.7%) | 45 mV (1.4%) |
| | 200 µF | - | 19.1 | 30 mV (0.9%) | 61 mV (1.8%) |
| 5[2] | 100 µF | - | 10.0 | 61 mV (1.2%) | 121 mV (2.4%) |
| | 100 µF | 220 µF | 31.6 | 32 mV (0.5%) | 45 mV (0.9%) |
| | 200 µF | - | 22.1 | 34 mV (0.7%) | 68 mV (1.4%) |
| 7.5[2] | 100 µF | - | 10.5 | 79 mV (1.1%) | 159 mV (2.1%) |
| | 47 µF | 220 µF | 28.0 | 27 mV (0.4%) | 54 mV (0.7%) |

(1) Load step slew rate of 2 A/µs
(2) Load step slew rate of 1 A/µs

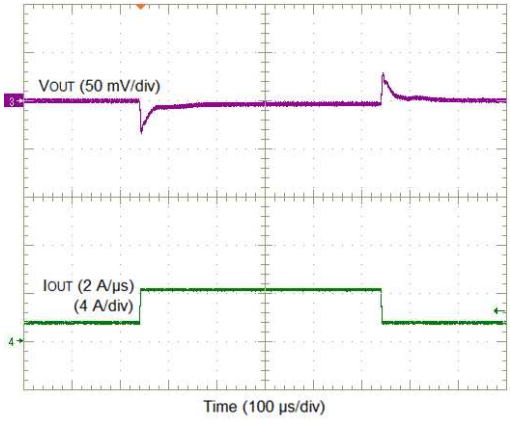

Copyright © 2018, Texas Instruments Incorporated

#### 7.3.7.2.1 Transient Waveforms ($V_{IN}$ = 12 V)



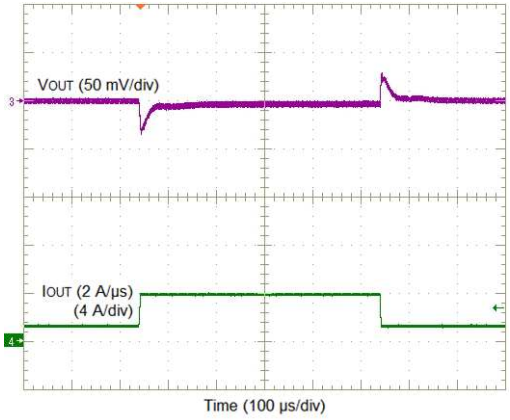

$V_{OUT}$ = 0.8 V $C_{OUT}$ = 300 µF ceramic + 220 µF polymer

**図 15. $V_{OUT}$ = 0.8 V, 3-A Load Step**



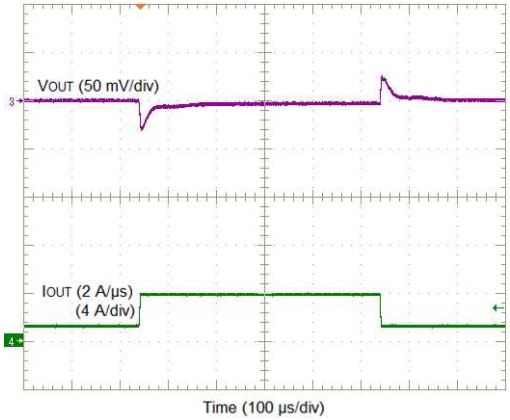

$V_{OUT}$ = 0.8 V $C_{OUT}$ = 300 µF ceramic + 330 µF polymer

**図 16. $V_{OUT}$ = 0.8 V, 3-A Load Step**



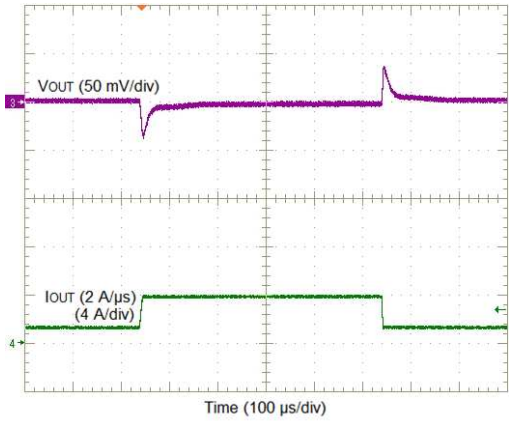

$V_{OUT}$ = 1 V $C_{OUT}$ = 200 µF ceramic + 220 µF polymer

**図 17. $V_{OUT}$ = 1 V, 3-A Load Step**



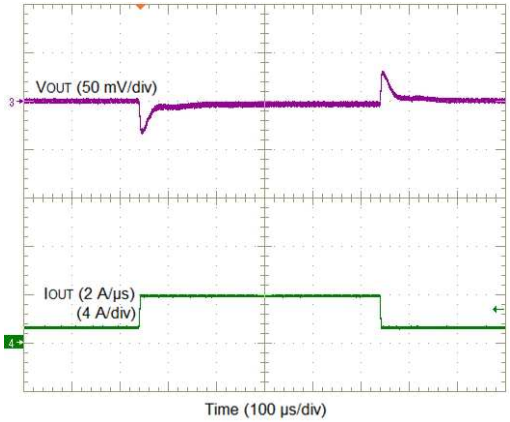

$V_{OUT}$ = 1 V $C_{OUT}$ = 400 µF ceramic + 220 µF polymer

**図 18. $V_{OUT}$ = 1 V, 3-A Load Step**




$V_{OUT}$ = 1.2 V $C_{OUT}$ = 400 µF ceramic

**図 19. $V_{OUT}$ = 1.2 V, 3-A Load Step**




$V_{OUT}$ = 1.2 V $C_{OUT}$ = 400 µF ceramic + 220 µF polymer

**図 20. $V_{OUT}$ = 1.2 V, 3-A Load Step**

Copyright © 2018, Texas Instruments Incorporated

### 7.3.8 Undervoltage Lockout (UVLO)

The TPSM84624 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.1 V (typical) with a typical hysteresis of 200 mV.

Applications may require a higher UVLO threshold to prevent early turnon, for sequencing requirements, or to prevent input current draw at lower input voltages. An external resistor divider can be added to the EN pin to adjust the UVLO threshold higher. The external resistor divider can be configured as shown in 図 21. 表 9 lists standard values for $R_{UVLO1}$ and $R_{UVLO2}$ to adjust the UVLO voltage higher.

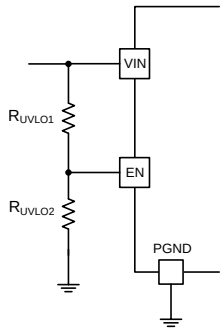



**図 21. Adjustable UVLO**

**表 9. Standard Resistor Values for Adjusting UVLO**

| VIN UVLO (V) | 4.5 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|
| $R_{UVLO1}$ (kΩ) | 68.1 | 68.1 | 68.1 | 68.1 | 68.1 | 68.1 | 68.1 | 68.1 | 68.1 |
| $R_{UVLO2}$ (kΩ) | 24.3 | 21.5 | 16.9 | 14 | 12.1 | 10.5 | 9.31 | 8.45 | 7.50 |
| Hysteresis (mV) | 385 | 400 | 430 | 465 | 500 | 530 | 565 | 600 | 640 |

### 7.3.9 Soft Start (SS/TR)

Leaving SS/TR pin open enables the internal soft-start time interval of approximately 1.25 ms. Adding additional capacitance between the SS pin and AGND increases the soft-start time. Increasing the soft-start time reduces inrush current seen by the input source and reduces the current seen by the device when charging the output capacitors. To avoid the activation of current limit and ensure proper start-up, the SS capacitor may need to be increased when operating near the maximum output capacitance limit.

See 表 10 for several SS capacitor values and timing interval or use 式 4 to calculate the value.

$$t_{SS} = \frac{0.6V \times (C_{SS} + 10nF)}{5\ \mu A} \quad (4)$$

**表 10. Soft-Start Capacitor Values and Soft-Start Time**

| $C_{SS}$ (nF) | open | 10 | 15 | 22 | 47 |
|---|---|---|---|---|---|
| SS Time (ms) | 1.25 | 2.4 | 3 | 3.8 | 6.8 |

During soft-start, the output voltage increases from its starting voltage and rises into regulation. The device is allowed to skip pulses as needed whenever the application conditions exceed the minimum on-time of the device. This behavior is a function of input voltage, output voltage, switching frequency, and load current. During the initial rise of the output voltage, adding an additional non-ceramic output capacitor in parallel with the required ceramic capacitance will improve the output voltage ramp-up.

**注**

When testing soft start performance with an electronic load, the output voltage noise can be exaggerated due to the control loop of the load. Testing with a pure resistive load is a better way to quantify the device performance.


Copyright © 2018, Texas Instruments Incorporated

### 7.3.10 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PGOOD pins. The sequential method is illustrated in 図 22 using two TPSM84624 devices. The PGOOD pin of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation.

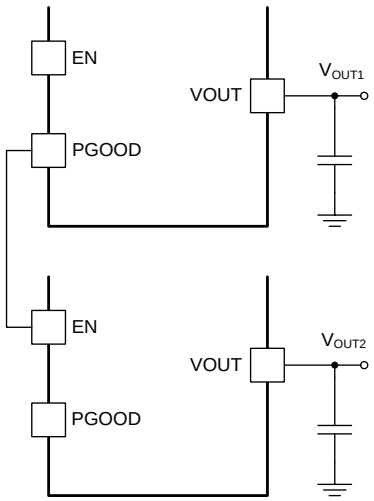



**図 22. Sequencing Schematic**

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in 図 23 to the output of the power supply that needs to be tracked or to another voltage reference source. Use 式 5 and 式 6 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 5)}{0.6} \ (k\Omega) \tag{5}$$

$$R2 = \frac{0.6 \times R1}{(V_{OUT2} - 0.6)} \ (k\Omega) \tag{6}$$

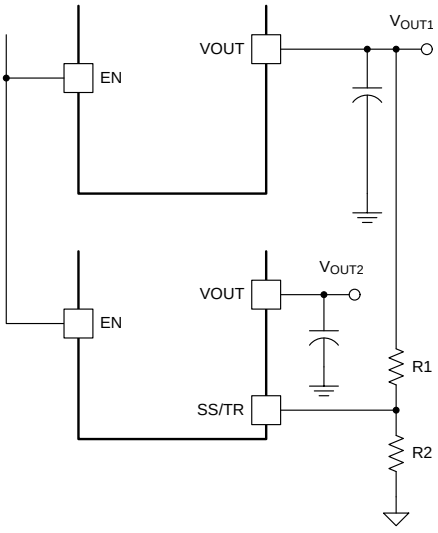



**図 23. Simultaneous Tracking Schematic**

Copyright © 2018, Texas Instruments Incorporated

### 7.3.11 Power Good (PGOOD)

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. Once the output voltage is between 91% and 106% of the setpoint voltage and SS/TR is greater than 0.75 V, the PGOOD pin pulldown is released and the pin floats. TI recommends a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source of 6.5 V or less. The PGOOD pin is pulled low when the output voltage is lower than 89% or greater than 108% of the setpoint voltage.

### 7.3.12 Safe Start-Up Into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased start-up, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than the FB pin voltage and the high-side MOSFET begins to switch.

### 7.3.13 Overcurrent Protection

For protection against load faults, the TPSM84624 is protected from overcurrent conditions by cycle-by-cycle current limiting. In an extended overcurrent condition the device enters hiccup mode to reduce power dissipation. In hiccup mode, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced, which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation.

### 7.3.14 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C typically. The device reinitiates the power up sequence when the junction temperature drops below 155°C typically.

## 7.4 Device Functional Modes

### 7.4.1 Active Mode

The TPSM84624 is in active mode when VIN is above the UVLO threshold and the EN pin voltage is above the EN high threshold. The EN pin has an internal current source to enable the output when the EN pin is left floating. If the EN pin is pulled low the device is put into a low quiescent current state.

### 7.4.2 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPSM84624. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode the device is put into a low quiescent current state. The TPSM84624 also employs undervoltage lockout protection. If $V_{IN}$ is below the UVLO level, the output of the regulator turns off.


Copyright © 2018, Texas Instruments Incorporated

# 8 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPSM84624 is a fixed-frequency, synchronous step-down DC/DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 6 A. The following design procedure can be used to select components for the TPSM84624. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com/webench for more details.

## 8.2 Typical Application

The TPSM84624 requires only a few external components to convert from a wide input voltage supply range to a wide range of output voltages. 図 24 shows a typical TPSM84624 schematic with only the minimum required components.

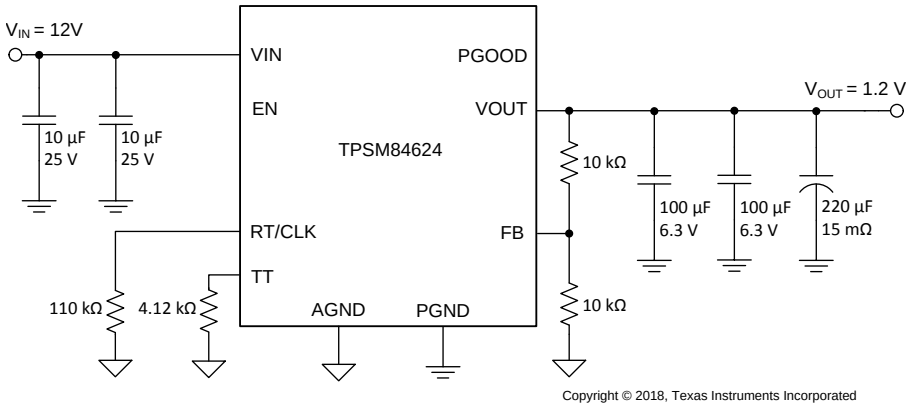



**図 24. TPSM84624 Typical Application**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 11 and follow the design procedures in 表 11.

**表 11. Design Example Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Input voltage $V_{IN}$ | 12 V typical |
| Output voltage $V_{OUT}$ | 1.2 V |
| Output current rating | 6 A |
| Key care-abouts | Small solution size, good transient response |
| Transient response requirements | 3% voltage deviation, 3-A load step, 1-A/µs slew rate |

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM84624 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM84624 device is externally adjustable using a two resistor divider ($R_{FBT}$ and $R_{FBB}$). The recommended value of $R_{FBT}$ is 10 kΩ. Select the value of $R_{FBB}$ from 表 1 or calculate using 式 7:

$$R_{FBB} = \frac{6}{(V_{OUT} - 0.6)} \ (k\Omega) \tag{7}$$

To set the output voltage to 1.2 V, the $R_{FBB}$ value is 10 kΩ.

#### 8.2.2.3 Setting the Switching Frequency

To set the switching frequency of the TPSM84624 a resistor ($R_{RT}$) between the RT/CLK pin and AGND is required. Select the value of $R_{RT}$ from 表 1 or calculate using 式 8:

$$R_{RT} = 58650 \times f_{SW}(kHz)^{-1.028} \ (k\Omega) \tag{8}$$

The recommended switching frequncy for a 1.2 V output is 450 kHz. To set the switching frequency to 450 kHz, the $R_{RT}$ value is 110 kΩ.

#### 8.2.2.4 Input Capacitors

For this design, two 10-µF ceramic capacitors rated for 25 V are used for the input decoupling capacitors.

#### 8.2.2.5 Output Capacitors

The minimum required output capacitance for a 1.2-V output is 200 µF of ceramic capacitance, as listed in 表 1. For this design, two 100-µF ceramic capacitors plus a 220-µF, 15-mΩ polymer capacitor where used to meet the transient requirement spec.

#### 8.2.2.6 TurboTrans Resistor

A TurboTrans resistor ($R_{TT}$) is required between the TT pin and AGND. The value of $R_{TT}$ can be calulated using 式 9. When calculating the $R_{TT}$ value, the total ***effective*** output capacitance which takes into account the effects of applied voltage and temperature.

$$R_{TT} = \left[\left(\frac{K_{TT} \times V_{OUT} \times C_{O(eff)}(\mu F)}{50}\right) - 2\right] \ (k\Omega) \tag{9}$$

The calulated value for $R_{TT}$ for this application is 4.12 kΩ.


Copyright © 2018, Texas Instruments Incorporated

### 8.2.2.7 Application Waveforms

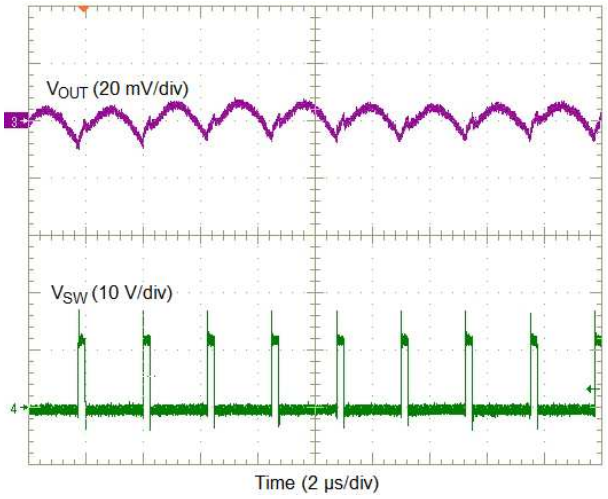



**図 25. Output Ripple and SW Waveforms**

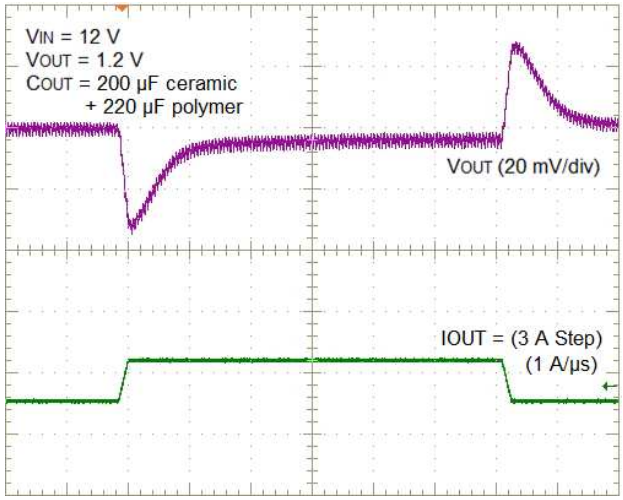



**図 26. Transient Response Waveforms**

## 9 Power Supply Recommendations

The TPSM84624 is designed to operate from an input voltage supply range between 4.5 V and 17 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPSM84624 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the TPSM84624 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Typically, a 47-µF or 100-µF electrolytic capacitor will suffice.

Copyright © 2018, Texas Instruments Incorporated

# 10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

## 10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 27 thru 図 30, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Place $R_{FBB}$, $R_{RT}$, and $C_{SS}$ as close as possible to their respective pins.
- Use multiple vias to connect the power planes (VIN, VOUT, and PGND) to internal layers.

## 10.2 Layout Examples

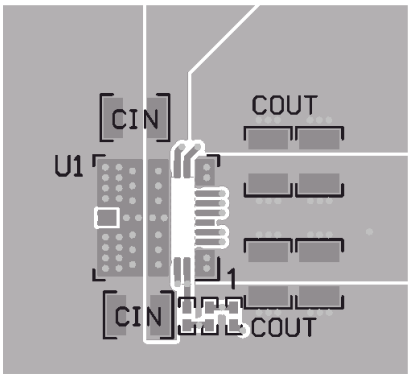



図 27. Typical Top-Layer Layout

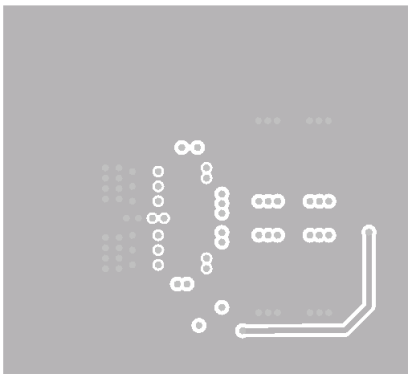


図 28. Typical Layer-2 Layout

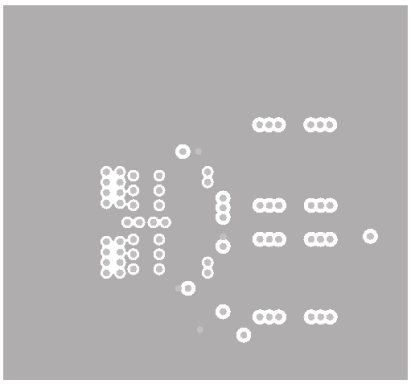


図 29. Typical Layer-3 Layout

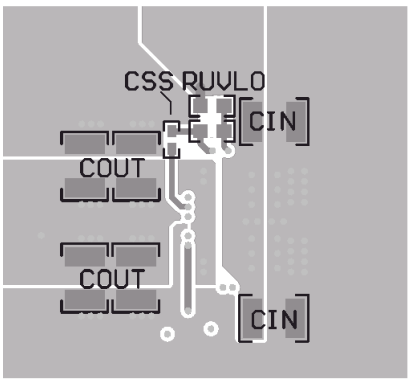



図 30. Typical Bottom-Layer Layout (Bottom View)


Copyright © 2018, Texas Instruments Incorporated

## 10.3 EMI

The TPSM84624 is compliant with EN55011 Class B radiated emissions. 図 31 and 図 32 show typical examples of radiated emissions plots for the TPSM84624. The graphs include the plots of the antenna in the horizontal and vertical positions.

### 10.3.1 EMI Plots

EMI plots were measured using the standard TPSM84624EVM with no input filter.

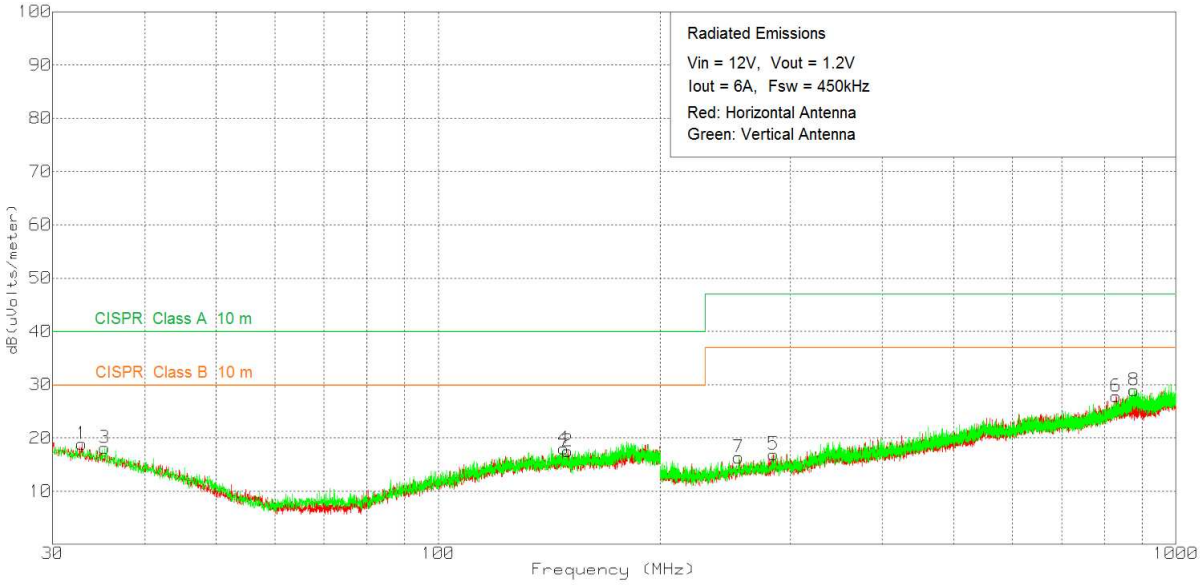



**図 31. Radiated Emissions 12-V Input, 1.2-V Output, 6-A Load (EN55011 Class B)**

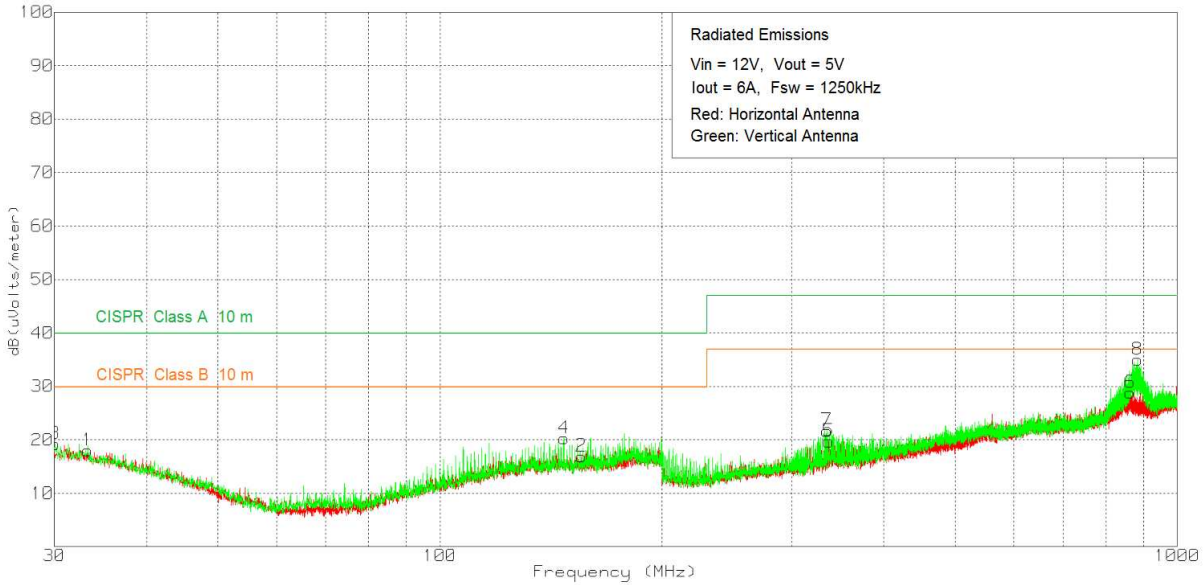



**図 32. Radiated Emissions 12-V Input, 5-V Output, 6-A Load (EN55011 Class B)**

## 10.4 Package Specifications

| TPSM84624 | | VALUE | UNIT |
|---|---|---|---|
| Weight | | 0.90 | grams |
| Flammability | Meets UL 94 V-O | | |
| MTBF Calculated Reliability | Per Bellcore TR-332, 50% stress, $T_A$ = 40°C, ground benign | 73.5 | MHrs |


Copyright © 2018, Texas Instruments Incorporated

# 11 デバイスおよびドキュメントのサポート

## 11.1 デバイス・サポート

### 11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

## 11.2 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPSM84624デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧($V_{IN}$)、出力電圧($V_{OUT}$)、出力電流($I_{OUT}$)の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

## 11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™オンライン・コミュニティ** ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

**設計サポート** ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

## 11.5 商標

TurboTrans, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.6 静電気放電に関する注意事項



これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

Copyright © 2018, Texas Instruments Incorporated

### 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


Copyright © 2018, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPSM84624MOLR | Active | Production | QFM (MOL) \| 24 | 500 \| LARGE T&R | Exempt | NIAU | Level-3-260C-168 HR | -40 to 105 | TPSM84624 |
| TPSM84624MOLR.A | Active | Production | QFM (MOL) \| 24 | 500 \| LARGE T&R | Exempt | NIAU | Level-3-260C-168 HR | -40 to 105 | TPSM84624 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

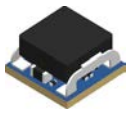
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

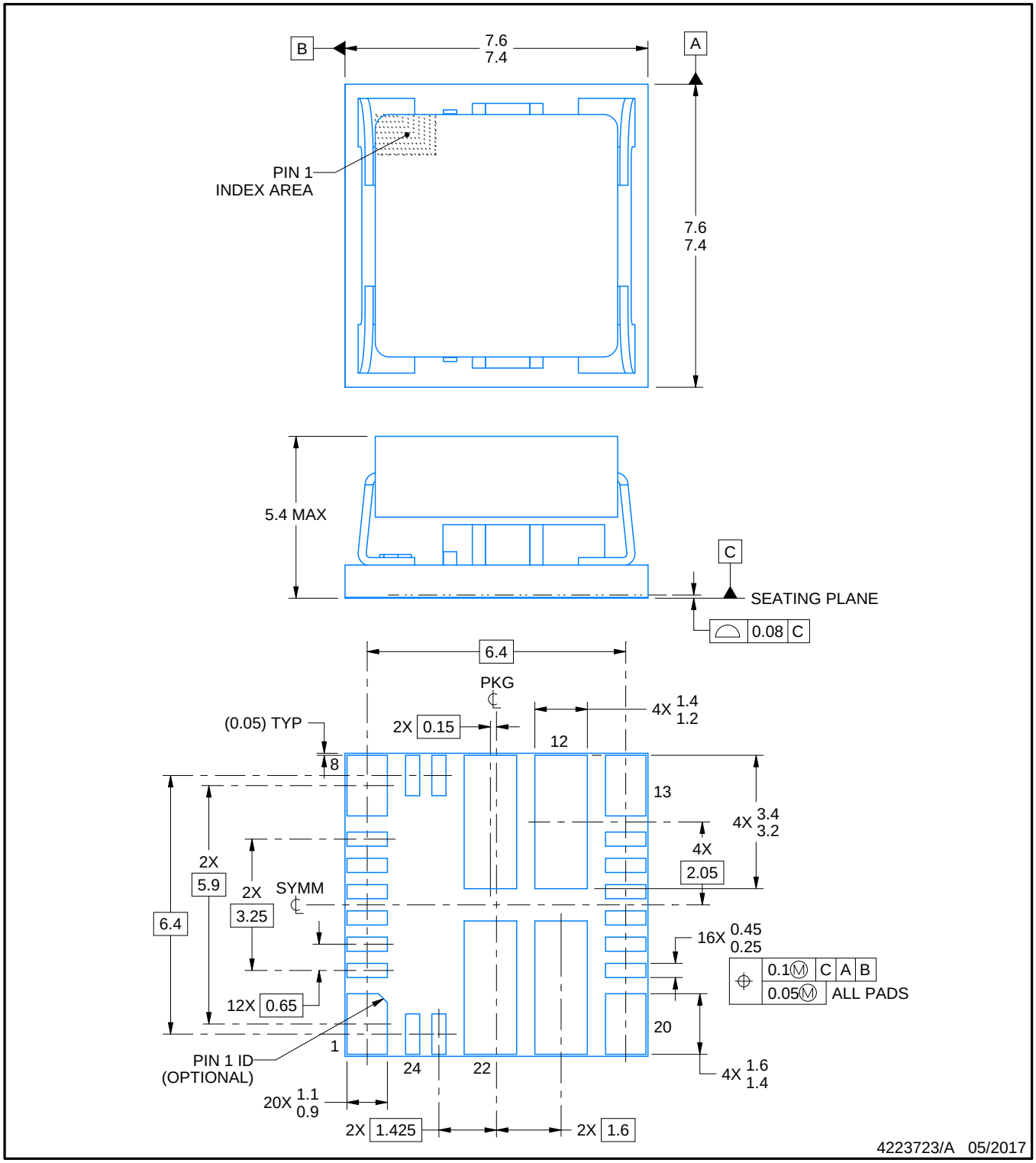
# MOL0024A



# PACKAGE OUTLINE

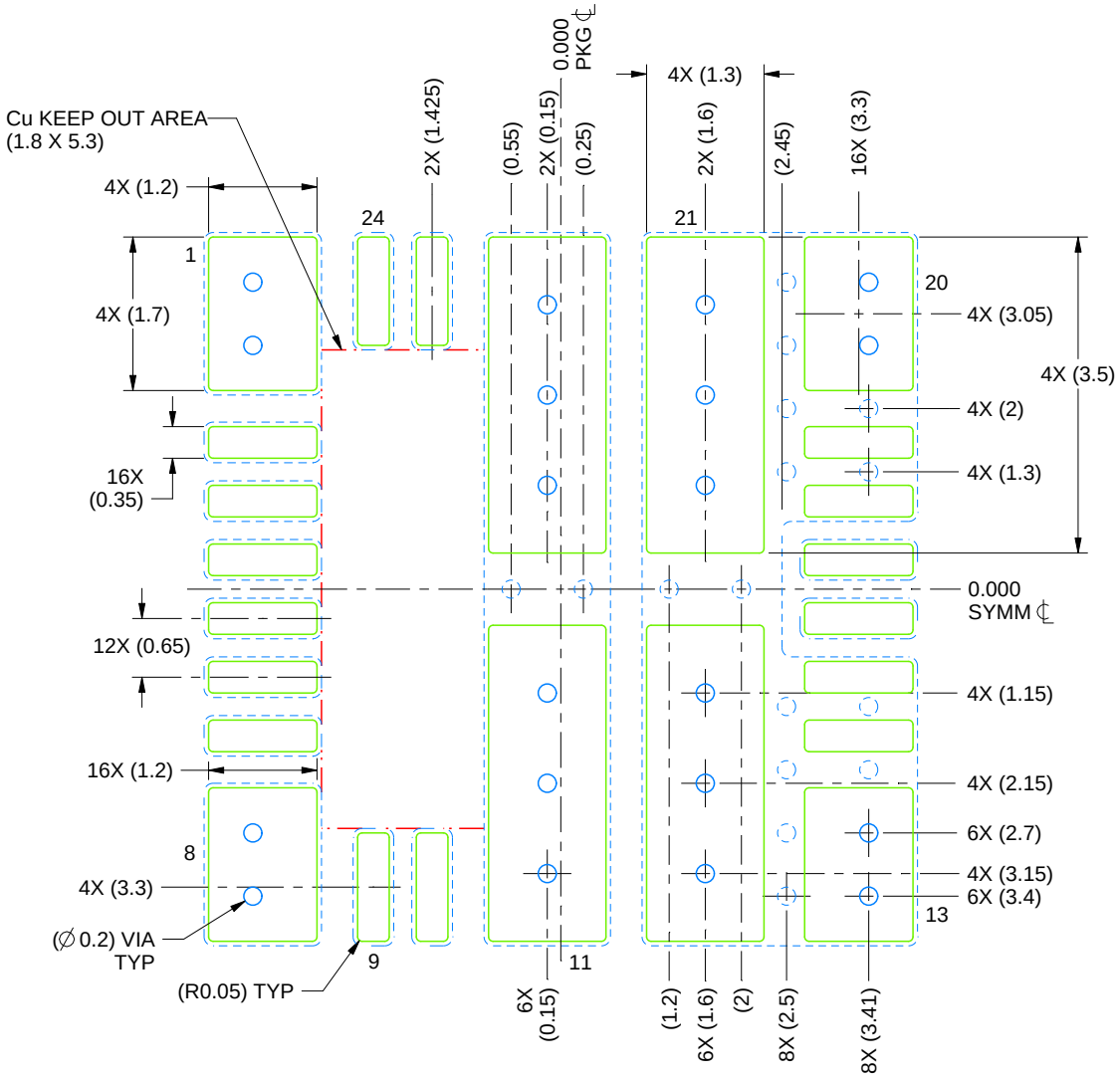
## QFM - 5.4 mm max height

QUAD FLAT MODULE

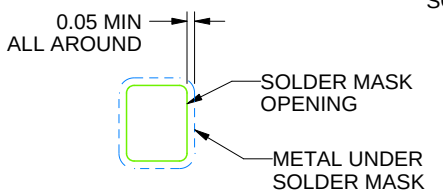



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:12X

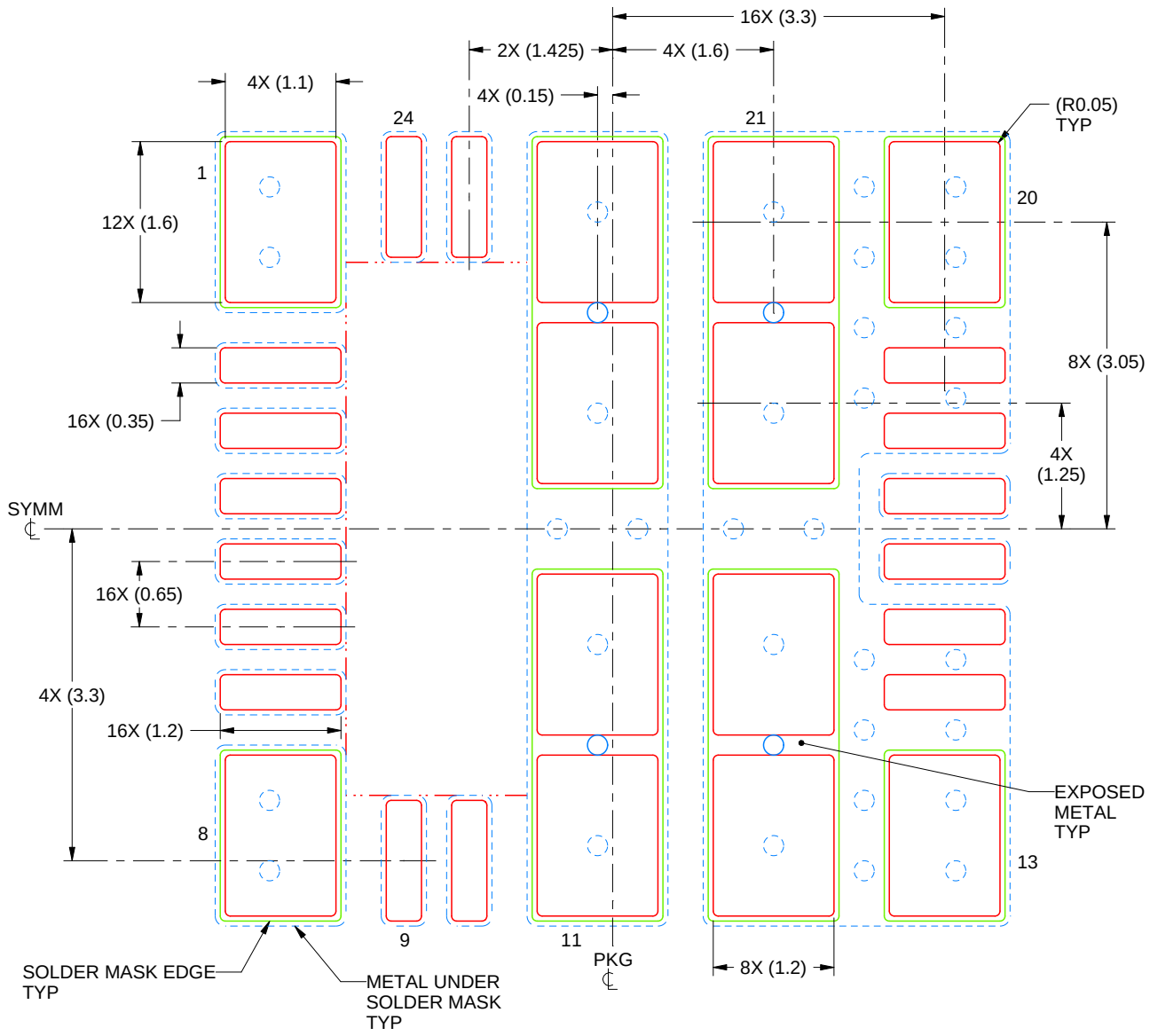



SOLDER MASK DETAIL

4223723/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to the thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 8, 13 & 20: 86%
PADS 11, 12, 21 & 22: 84%
SCALE:15X

4223723/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月