TPSM84A21 8V～14V入力、0.508V～1.35V出力、10A SWIFT™パワー・モジュール

1 特長

- 完全に統合された電源ソリューションで、入力および出力コンデンサを内蔵
- 単一の電圧設定抵抗だけで動作
- 9mm×15mmの占有面積
  - 最大高2.3mm
  - TPSM84A22とピン互換
- 超高速の負荷ステップ応答
- 最高88%の効率
- 1%の出力電圧精度
- スイッチング周波数: 4MHz
- 外部クロックに同期
- パワー・グッド出力
- プリバイアス出力によるスタートアップ
- プログラム可能な低電圧誤動作防止(UVLO)
- 動作時のIC接合部温度範囲: -40℃～+125℃
- 動作時周囲温度範囲: -40℃～+85℃
- EN55022 Class Bの放射規格に準拠

2 アプリケーション

- 電気通信および無線インフラストラクチャ
- 試験/測定機器
- Compact PCI/PCI Express/PXI Express

3 概要

TPSM84A21は使いやすい統合電源ソリューションで、10AのDC/DC同期整流降圧型コンバータのTPS54A20を、パワーMOSFET、シールド付きインダクタ、入力および出力コンデンサ、受動部品とともに、低プロファイルのパッケージに搭載したものです。この総合的な電源ソリューションは、電圧を設定する1つの抵抗だけで動作し、設計においてループ補償や磁性部品の選択が不要になります。

完全に統合された電源ソリューションであるため、標準のアプリケーションは追加の入力または出力コンデンサを必要とせず、出力電圧を設定するための外付けの抵抗1つだけで動作します。高い周波数での動作、非常に高速な過渡応答、正確な電圧レギュレーションにより、TPSM84A21は厳しい規制の仕様を満たすことができます。

PCB占有面積9×15mmで、プリント基板へ簡単にハンダ付けでき、コンパクトで低プロファイルのポイント・オブ・ロード設計が可能です。

製品情報(1)

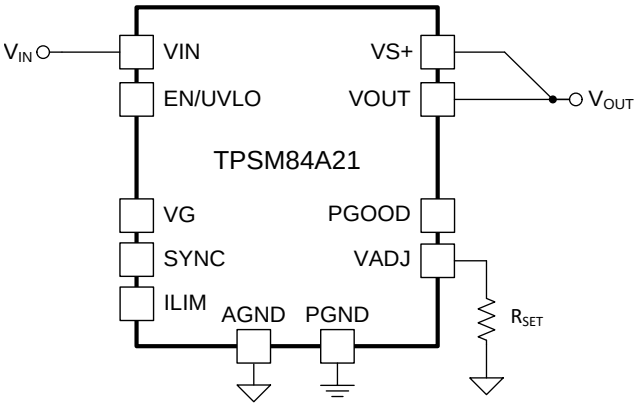
型番	パッケージ	本体サイズ(公称)
TPSM84A21	QFM	9.00mm×15.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイスの比較

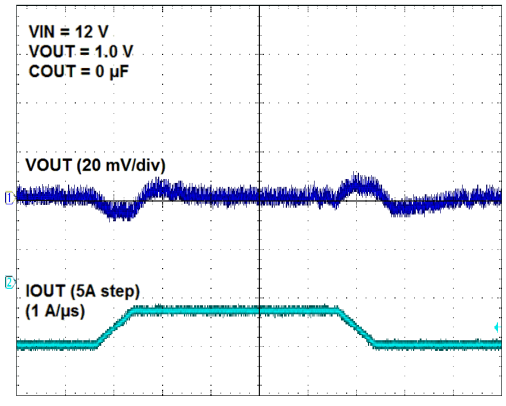
型番	V_{OUT}の可変範囲
TPSM84A21	0.55V～1.35V
TPSM84A22	1.2V～2.05V

概略回路図



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過渡応答



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4 改訂履歴

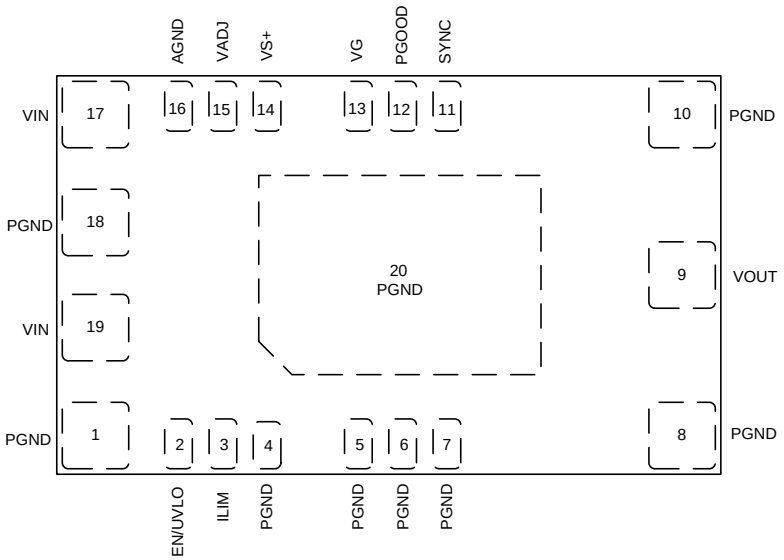
2016年12月 発行のものから更新 **Page**

- 「特長」からMSL 3/245℃ピーク・リフローを削除 ... 1
- Added the *EMI* section ... 21

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5 Pin Configuration and Functions

MOJ Package
20-Pin QFM
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	16	—	Zero voltage reference for analog control circuitry. Connect RSET between this pin and VADJ close to the device. Do not connect this pin to PGND; the connection is made internal to the device.
EN/UVLO	2	I	Enable and UVLO adjust pin. When this pin voltage is low, the device is disabled. Use an open drain, open collector, or a suitable logic gate device to control the enable function. A resistor divider between this pin, PGND, and VIN adjusts the UVLO voltage.
ILIM	3	I	Current limit setting pin. Leave this open for the full current limit threshold of 15 A. Connect a 47 kΩ resistor between this pin and PGND to reduce the current limit threshold to 11.25 A.
PGND	1, 4, 5, 6, 7, 8, 10, 18, 20	—	Power ground of the device. Connect these pins to the power ground plane of the PCB. Thermal vias to internal ground planes should be added beneath pin 20.
PGOOD	12	O	Power good indicator. This pin is an open-drain output and will assert low if the output voltage is greater than ±5% from the programmed value or due to thermal shutdown, under-voltage, or EN shutdown. A pull-up resistor is required. VG can be used as a PGOOD pull-up source.
VS+	14	I	Remote sense connection. This pin must be connected to VOUT at the load or at the device pins. Connect the pin to VOUT at the load for improved regulation.
SYNC	11	I	External clock synchronization pin. An external clock signal can be applied to this pin to synchronize the switching frequency within ±10% of the nominal switching frequency (4 MHz).
VADJ	15	I	Output voltage adjust pin. Connecting a resistor between this pin and AGND sets the output voltage.
VG	13	I	Gate driver supply pin. If this pin is left open, an internal LDO will generate the gate driver supply voltage from the VIN pin. To reduce power consumption and improve efficiency, power this pin with an external 5-V supply. This pin can be used as a PGOOD pull-up source.
VIN	17, 19	I	Input Voltage. These pins supply all of the power to the converter. Connect VIN to a supply voltage between 8 V and 14 V.
VOUT	9	O	Output voltage. Connect any external output capacitors between these pins and PGND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	15	V
	EN/UVLO	–0.3	7	V
	PGOOD, SYNC, VG	–0.3	6	V
	ILIM, VADJ, VS+	–0.3	3	V
	PGND	–0.3	0.3	V
Output voltage	VOUT	–0.3	3	V
Source current	EN/UVLO		100	µA
Sink current	VG		100	mA
	PGOOD		4	mA
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	G
Operating IC junction temperature, T_J(2)		–40	125	°C
Operating ambient temperature, T_A(2)		–40	85	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	8		14	V
V_{OUT}	Output voltage	0.55		1.35	V
V_{VG}	Gate drive voltage	5.0		5.5	V
V_{EN}	EN voltage	0		5.5	V
V_{PGOOD}	PGOOD pull-up voltage	0		5.5	V
V_{SYNC}	SYNC voltage	0		5.5	V
I_{OUT}	Output current	0		10	A
T_J	Operating IC junction temperature (1)	–40		125	°C
T_A	Operating ambient temperature (1)	–40		85	°C

(1) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves, ensures that the maximum junction temperature of any component inside the module is never exceeded.

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6.4 Thermal Information

THERMAL METRIC(1)		TPSM84A21 MOJ (QFM) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	14.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	5.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance, Θ_{JA}, applies to devices soldered directly to a 50 mm x 100 mm double-sided PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces Θ_{JA}.
(3) The junction-to-top board characterization parameter, Θ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and TT is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Over –40°C to +85°C free-air temperature range, VIN = 12 V, V_{OUT} = 1.0 V, I_{OUT} = I_{OUT} max, F_{SW} = 4 MHz, External C_{IN} = 2 × 22 µF 25 V 1210 ceramic plus 1 × 100 µF electrolytic (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
V_{IN}	VIN input voltage range	Over V_{OUT} range	8		14	V
V_{IN_UVLO}	VIN under voltage lock out	V_{IN} increasing		7.65	7.95	V
		V_{IN} decreasing		7.4		V
V_{IN_HYS}	VIN UVLO hysteresis			250		mV
I_{VIN_EN}	VIN standby current	EN = 0 V		47		µA
OUTPUT VOLTAGE (VOUT)						
$V_{OUT(ADJ)}$	Output voltage adjust range	Over I_{OUT} range	0.55		1.35	V
V_{OUT}	Set-point voltage tolerance	V_{OUT} = 1.0 V, T_A = 25°C, I_{OUT} = 0 A	-1.0%		+1.0%(1)	
	Temperature variation	V_{OUT} = 1.0 V, –40°C ≤ T_A ≤ 85°C, I_{OUT} = 0 A		±0.2%(2)		
	Line regulation	V_{OUT} = 1.0 V, over V_{IN} range, I_{OUT} = 0 A, T_A = 25°C		±0.03%		
	Load regulation	V_{OUT} = 1.0 V, over I_{OUT} range, T_A = 25°C		±0.1%		
V_{OUT} Ripple	Output Voltage Ripple	20-MHz Bandwidth, peak-to-peak		8		mV
OUTPUT CURRENT						
I_{OUT}	Output current	See SOA graph for derating over temperature.	0		10	A
	Overcurrent threshold	ILIM = open		15		A
		ILIM = 47 kΩ		11.25		A

(1) The stated limit of the set-point tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(2) Specified by design. Not production tested.

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Electrical Characteristics (continued)

Over –40°C to +85°C free-air temperature range, VIN = 12 V, V_{OUT} = 1.0 V, I_{OUT} = I_{OUT} max, F_{SW} = 4 MHz, External C_{IN} = 2 × 22 µF 25 V 1210 ceramic plus 1 × 100 µF electrolytic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PERFORMANCE							
η	Efficiency(2)	V_{IN} = 12 V, I_{OUT} = 5 A	V_{OUT} = 0.8 V, VG = open		79.8%		
			V_{OUT} = 0.8 V, VG = 5 V		82.5%		
			V_{OUT} = 1.0 V, VG = open		82.6%		
			V_{OUT} = 1.0 V, VG = 5 V		84.9%		
			V_{OUT} = 1.2 V, VG = open		84.5%		
			V_{OUT} = 1.2 V, VG = 5 V		86.5%		
	Transient Response(2)	1 A/µs load step, 25% to 75% IOUT(max), COUT= 0 µF	VOUT over/undershoot		10		mV
			Recovery Time		10		µs
		5 A/µs load step, 25% to 75% IOUT(max), COUT= 0 µF	VOUT over/undershoot		25		mV
			Recovery Time		10		µs
SOFT START							
T_{SS}	Internal soft start time(2)				4.1		ms
INTERNAL REGULATOR (VG)							
V_{VG}	VG pin output voltage			4.4	4.8	5.0	V
ENABLE AND UNDER-VOLTAGE LOCK-OUT (EN/UVLO)							
V_{EN}	EN threshold range			1.17	1.23	1.27	V
I_{EN}	Input current	EN threshold + 50 mV			–4		µA
	Hysteresis current	EN threshold – 50 mV			–1		µA
POWER GOOD (PGOOD)							
V_{PGOOD}	PGOOD Thresholds (2)	V_{VOUT} falling (Fault)			89%		
		V_{VOUT} rising (Good)			95%		
		V_{VOUT} rising (Fault)			109%		
		V_{VOUT} falling (Good)			104%		
	Minimum V_{IN} for valid PGOOD(2)	V_{PGOOD} ≤ 0.5 V at 100 µA			1.2	2.75	V
	PGOOD Low Voltage	I_{PGOOD} = 1.7 mA			0.25	0.3	V
THERMAL SHUTDOWN							
	Thermal shutdown threshold				135		°C
	Thermal shutdown hysteresis				20		°C
CAPACITANCE							
C_{IN}	External Input Capacitance	Ceramic type		0(3)	44		µF
		Non-ceramic type		0(3)	100		µF
C_{OUT}	External Output Capacitance	Ceramic type		0(4)		1000(5)	µF
		Non-ceramic type		0(4)		2200(5)	µF
		Equivalent series resistance (ESR)				35	mΩ

(3) Internal to the device, 66.1 µF (nominal) ceramic input capacitance is present. This device does not require additional input capacitance. If adding additional input capacitance, locate the capacitors close to the device.
(4) Internal to the device, 185 µF (nominal) ceramic output capacitance is present. This device does not require additional output capacitance to operate. Adding additional output capacitance near the load improves the response of the device to load transients.
(5) The maximum output capacitance listed in the table is the maximum amount that has been tested and validated for proper start-up, stability, and transient response. It may be possible to operate with additional output capacitance, however, additional validation is required.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY AND SYNCHRONIZATION (SYNC) (1)						
F_{SW}	Switching frequency	SYNC = open	3.7	4	4.3	MHz
F_{SYNC}	Synchronization frequency range	SYNC Control	3.6		4.4	MHz
V_{SYNC-H}	SYNC high threshold		2.0			V
V_{SYNC-L}	SYNC low threshold				0.8	V
D_{SYNC}	SYNC duty cycle		20%		80%	

(1) Specified by design. Not production tested.

6.7 Package Specifications

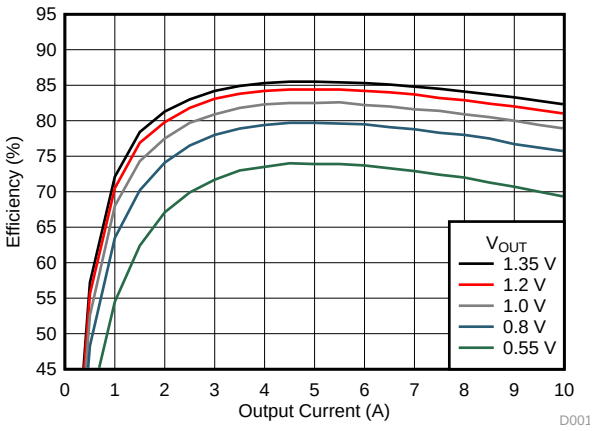
TPSM84A21		VALUE	UNIT
Weight		0.91	grams
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	30.6	MHrs

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6.8 Typical Characteristics

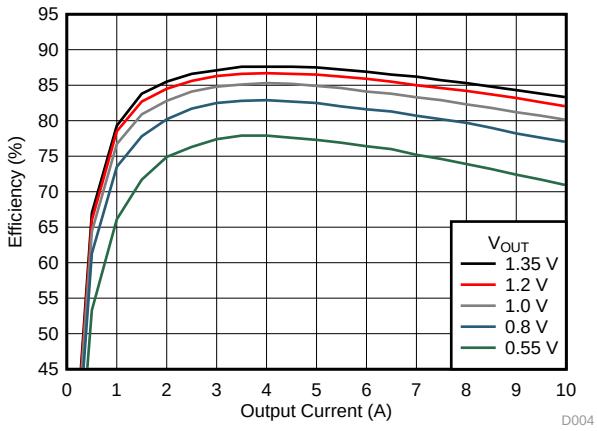
The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to 図 1 through 図 4.

The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 50 mm × 100 mm double-sided PCB with 2 oz. copper. Applies to 図 5 and 図 6.



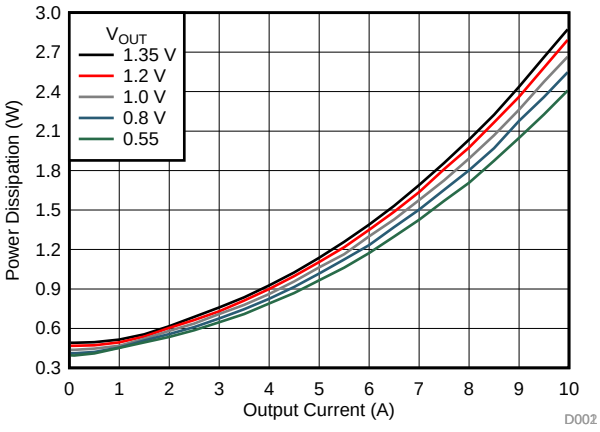
VIN = 12 V VG = open

図 1. Efficiency



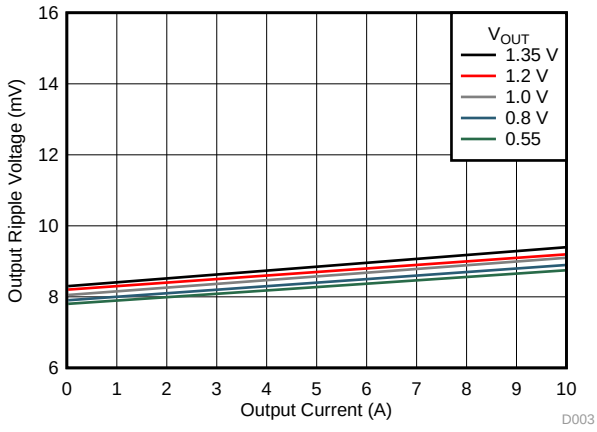
VIN = 12 V VG = 5 V

図 2. Efficiency



VIN = 12 V VG = open

図 3. Power Dissipation

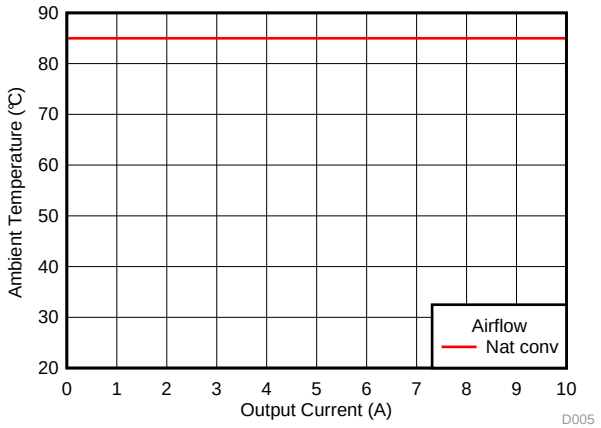


VIN = 12 V

図 4. Output Voltage Ripple

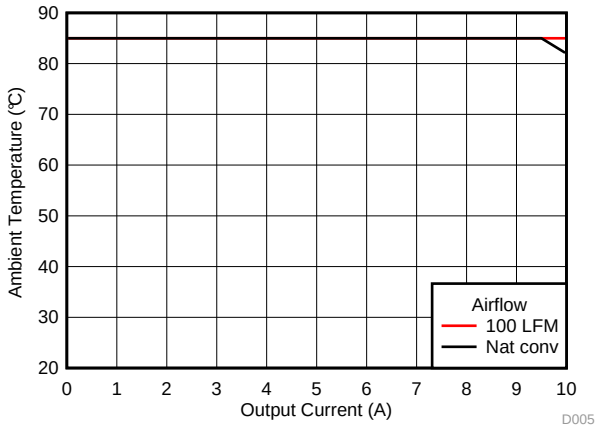
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Typical Characteristics (continued)



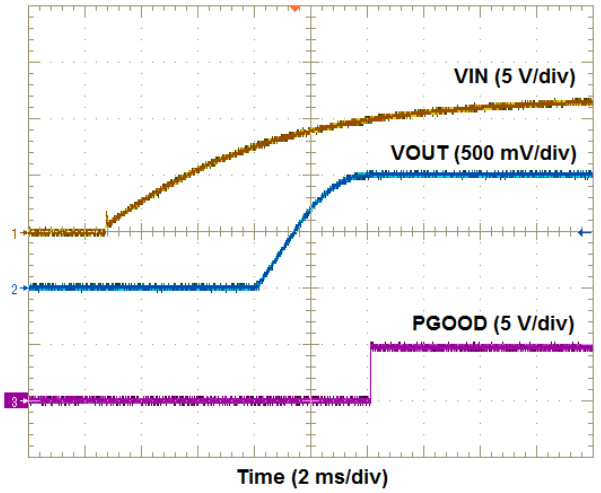
VIN = 12 V VOUT = 0.8 V

図 5. Safe Operating Area



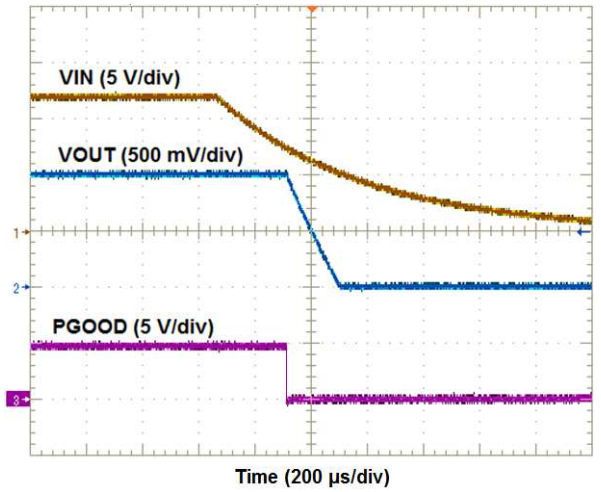
VIN = 12 V VOUT = 1.2 V

図 6. Safe Operating Area



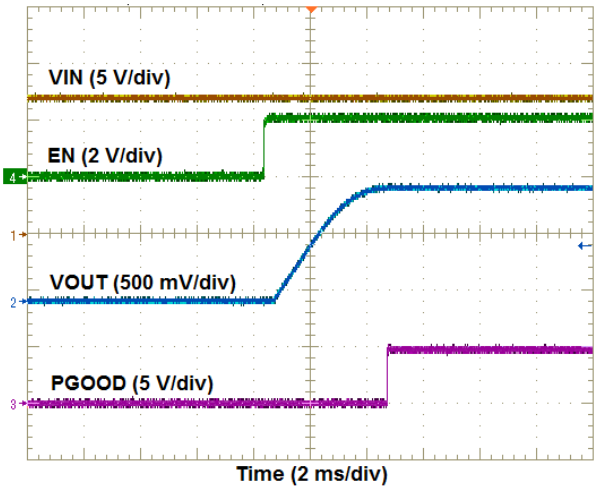
VIN = 12 V VOUT = 1.0 V IOUT = 1 A

図 7. VIN Start-up Waveforms



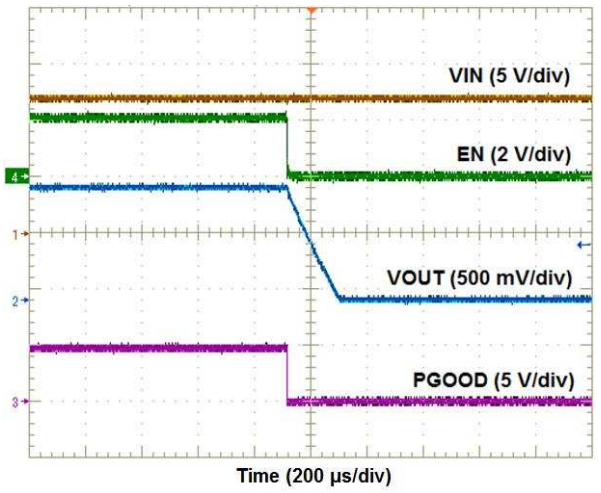
VIN = 12 V VOUT = 1.0 V IOUT = 1 A

図 8. VIN Shut-down Waveforms



VIN = 12 V VOUT = 1.0 V IOUT = 1 A

図 9. EN Start-up Waveforms



VIN = 12 V VOUT = 1.0 V IOUT = 1 A

図 10. EN Shut-down Waveforms

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7 Detailed Description

7.1 Overview

The TPSM84A21 is a 14-V, 10-A, synchronous series capacitor step-down (buck) power module. The TPSM84A21 combines a 10-A DC/DC converter with power MOSFETs, shielded inductors, series capacitor, input and output capacitors, and passives into a low profile, overmolded package. The integrated input and output capacitors allows standard applications to operate with no additional input or output capacitors and only a single resistor to set the output voltage.

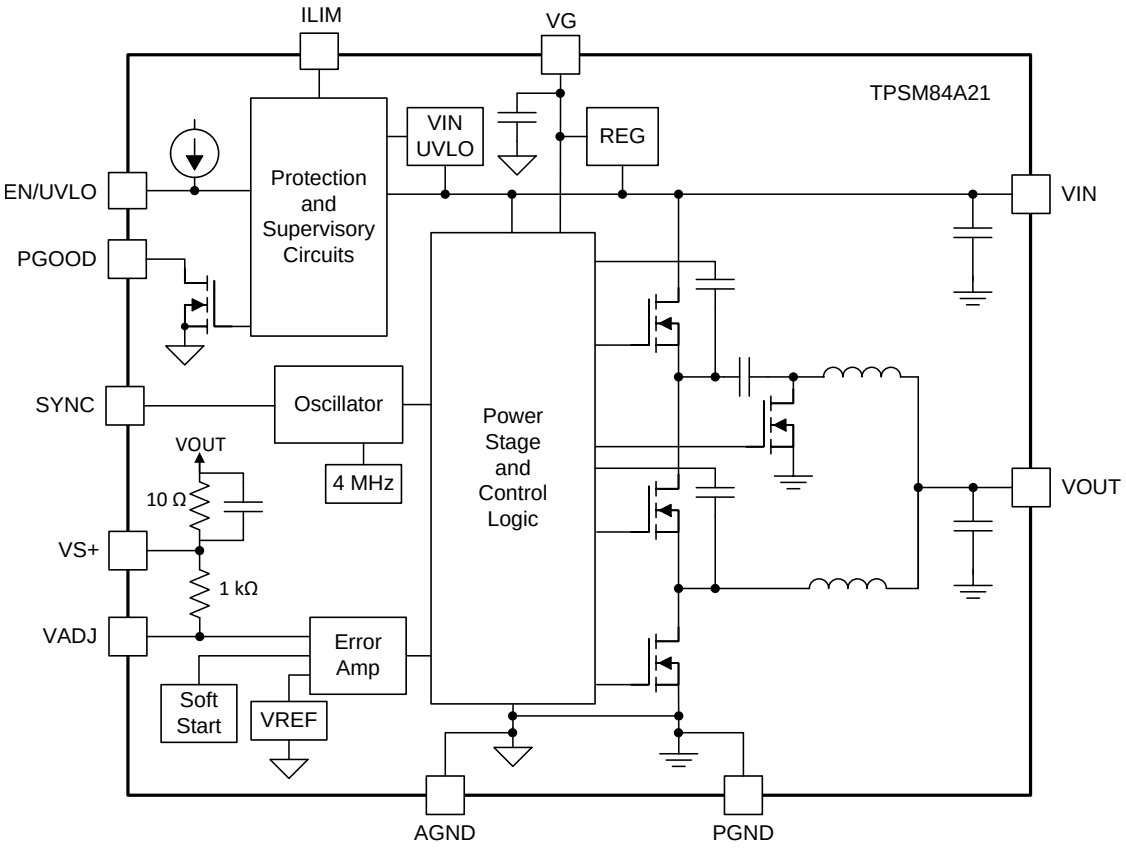
The integrated components allow for high-efficiency, high-density, complete power supply designs with continuous output currents up to 10 A. The TPSM84A21 reduces the external component count by integrating both the input and output capacitors. The TPSM84A21 input voltage range is 8 V to 14 V with an output voltage range of 0.508 V to 1.35 V.

The TPSM84A21 is a two-phase power supply with each phase switching at a fixed 2 MHz frequency, resulting in the internal oscillator frequency of 4 MHz. An external synchronization clock can also be provided via the SYNC pin.

The TPSM84A21 starts up safely into loads with pre-biased outputs (non-zero volts at startup). The device implements an internal input voltage under voltage lockout (UVLO) feature which can be adjusted higher by adding an external resistor divider on the EN/UVLO pin. Electrical ON/OFF control is provided using the enable (EN) feature. The TPSM84A21 is disabled by pulling the EN pin low. When the device is disabled, the supply current is typically less than 50 μA.

The TPSM84A21 has a power good comparator (PGOOD) which monitors the output voltage through the VS+ pin. The PGOOD pin is an open-drain MOSFET which is held low until the output voltage is within ±5% of the set voltage. The PGOOD pin is held low during startup or when a fault occurs.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjusting the Output Voltage (VADJ)

The VADJ pin programs the output voltage of the TPSM84A21. The output voltage adjustment range is from 0.508 V to 1.35 V. The adjustment method requires the addition of R_{SET} connected between VADJ and AGND. If an R_{SET} resistor is not populated, the module will default to 0.508 V. The VS+ pin (pin 14) must be connected to VOUT. TI recommends to make the VS+ connection at the load for the best load regulation performance. The R_{SET} resistor must be connected directly between the VADJ pin (pin 15) and AGND (pin 16).

式 1 can be used to calculate the ideal R_{SET} resistor value for a given output voltage, V_{OUT}. Use 式 2 to calculate the actual V_{OUT} for a given R_{SET} resistor. 表 1 lists the ideal R_{SET} resistor values for a number of common voltages. 表 1 also lists the closest E96 standard resistor values to the ideal R_{SET} values along with the actual output voltage and the set-point error when using the E96 resistor value. For the most accurate output voltage set-point it is best to use the ideal resistor value. The ideal resistor value may not be a standard value and may require two standard value resistors in series or parallel to obtain the desired output voltage.

$$R_{SET} = \frac{1}{\frac{V_{OUT}}{0.508} - 1} \ (k\Omega) \tag{1}$$

$$V_{OUT} = 0.508 * \left(\frac{1}{R_{SET}\,(k\Omega)} + 1 \right) (V) \tag{2}$$

表 1. R_{SET} Resistor Values

			Closest E96 Resistor Value		
V_{OUT} (V)	Ideal R_{SET} (kΩ)		R_{SET} (kΩ)	Actual V_{OUT} (V)	%
0.508	Open		Open	0.508	–
0.55	12.095		12.1	0.549	–0.003
0.60	5.522		5.49	0.601	0.088
0.65	3.578		3.57	0.65	0.046
0.70	2.646		2.67	0.698	–0.248
0.75	2.099		2.10	0.749	–0.013
0.80	1.739		1.74	0.799	–0.006
0.85	1.485		1.50	0.847	–0.392
0.9	1.296		1.30	0.899	–0.137
0.95	1.149		1.15	0.949	–0.027
1.00	1.033		1.02	1.006	0.603
1.05	0.937		0.931	1.053	0.348
1.10	0.858		0.866	1.095	–0.490
1.15	0.791		0.787	1.153	0.303
1.20	0.734		0.732	1.202	0.166
1.25	0.685		0.681	1.254	0.317
1.30	0.641		0.649	1.291	–0.712
1.35	0.603		0.604	1.349	–0.070

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7.3.2 Input and Output Capacitance

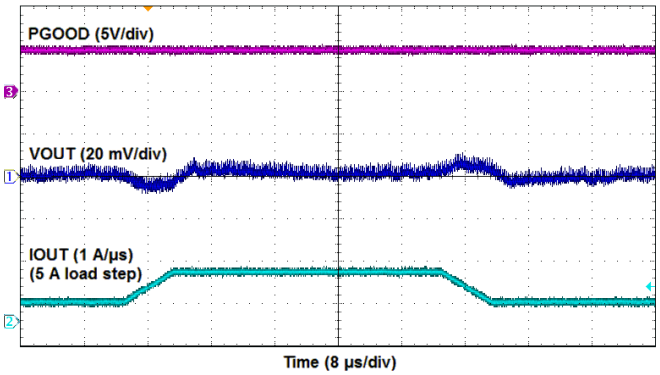
The TPSM84A21 requires no external input or output capacitance to operate. Internal to the TPSM84A21 there is 66.1 µF (nominal) of ceramic input capacitance. Additionally, internal to the TPSM84A21 there is 185 µF (nominal) of ceramic output capacitance.

Applications requiring additional ripple voltage reduction should add ceramic input and output capacitors directly at the VIN and VOUT pins of the device. Applications requiring improved transient response can also benefit by adding additonal ceramic or low-ESR bulk output capacitance. See the Capacitance section of the *Electrical Characteristics* table for more information when adding external input and output capacitors.

7.3.3 Transient Response

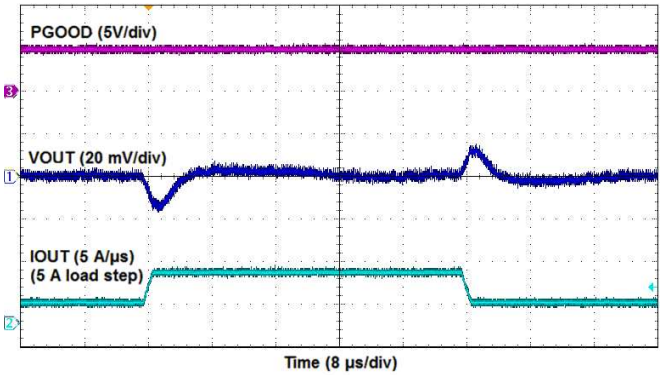
The exceptional transient response of the TPSM84A21 allows many applications to operate with little or no additional output capacitance. 図 11 through 図 14 show typical transient waveforms for the TPSM84A21.

7.3.3.1 Transient Response Waveforms



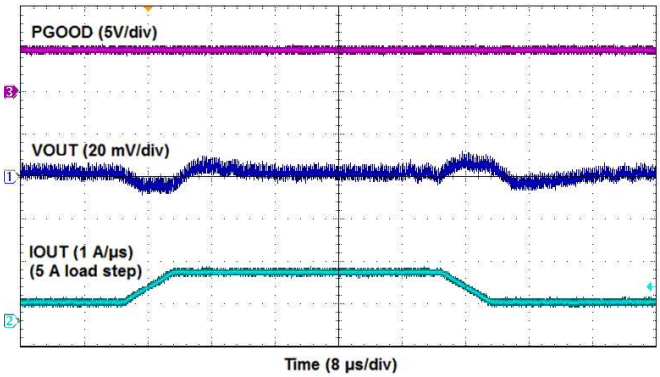
VIN = 12 V VOUT = 0.8 V Load Step = 5 A
COUT = 0 µF Slew Rate = 1 A/µs

図 11. Transient Response



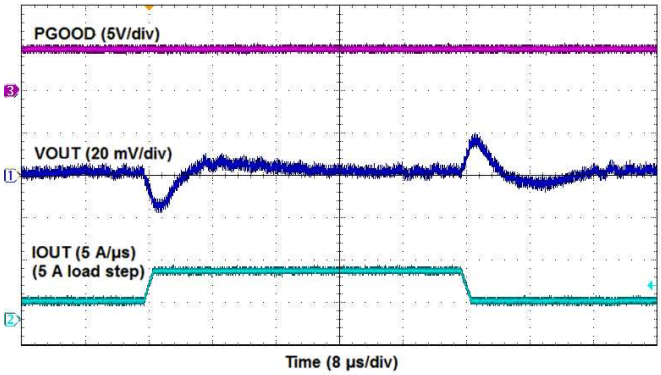
VIN = 12 V VOUT = 0.8 V Load Step = 5 A
COUT = 300 µF Slew Rate = 5 A/µs

図 12. Transient Response



VIN = 12 V VOUT = 1.0 V Load Step = 5 A
COUT = 0 µF Slew Rate = 1 A/µs

図 13. Transient Response



VIN = 12 V VOUT = 1.0 V Load Step = 5 A
COUT = 100 µF Slew Rate = 5 A/µs

図 14. Transient Response

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7.3.4 Oscillator Frequency

The oscillator frequency of this converter is set at 4 MHz. The per phase switching frequency of the converter is half the oscillator frequency, or 2 MHz per phase. The oscillator frequency is fixed internally.

During load transients, the internal control loop will momentarily change the switching frequency in order to meet the output voltage recovery.

7.3.5 External Clock Syncronization

An external clock can be connected to the SYNC pin. The external clock signal overrides the internal oscillator and is used as the system clock. This feature enables the user to synchronize the switching events to a master clock on their board. The internal phase locked loop (PLL) has been implemented to allow synchronization at frequencies between ±10% of the nominal oscillator frequency. This allows the user to easily switch between the internal oscillator mode and the external clock mode while converting power. Before the external clock is present or after it is removed, the device with default to the internal oscillator setting.

To implement the synchronization feature, connect a square wave clock signal to the SYNC pin with a duty cycle between 20% and 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the rising edge of the SYNC pin. The device can be configured for operation in applications where both an internal oscillator mode and an external synchronization clock mode are needed. Before the external clock is present, the switching frequency of the device is set by the internal oscillator. When the external clock is present, the SYNC mode overrides the internal oscillator. The first time the SYNC pin is pulled above the SYNC high threshold (2 V), the device switches from the internal oscillator mode to the SYNC mode and the PLL starts to lock onto the frequency of the external clock. When the external SYNC clock is removed, the converter will transition back to the internal oscillator after 4 internal clock cycles.

7.3.6 Soft Start

The TPSM84A21 has a pre-programmed soft start time of 4.1 ms (typ). The soft start time is the time it takes for the output voltage to rise from zero volts to the voltage set by the R_{SET} resistor. Soft start is an important feature that limits inrush current and reduces the load on the input supply to this device. During soft start, the internal reference voltage is slowly ramped up to the internal reference voltage. This slowly increases the commanded output voltage of the converter and reduces the initial surge in current. During soft start PGOOD remains low, the PLL is not active, and output UVP/OVP faults are disabled.

7.3.7 Power Good (PGOOD)

The Power Good (PGOOD) pin is an open drain output. After startup, when the VADJ pin is typically between 95% and 105% of the internal voltage reference, the PGOOD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source of 5.5 V or less. For convenience, VG can be used as the pull-up voltage. The PGOOD is in a defined state once the VIN input voltage is greater than approximately 1.2 V, but with reduced current sinking capability. The PGOOD achieves full current sinking capability once the VIN input voltage is above the input UVLO. The PGOOD pin is pulled low when the VADJ pin voltage is typically lower than 95% or greater than 105% of the nominal internal reference voltage. The PGOOD pin is also pulled low if a fault is detected, the EN pin is pulled low, or the converter is performing its soft-start power up sequence.

7.3.8 Gate Driver (VG)

A linear regulator internal to the TPSM84A21 generates a 4.8 V internal supply rail on the VG pin. The input of the linear regulator comes from the VIN pin. The VG supply rail is used to power the internal gate drivers and is the input to another regulator that generates the internal supply rails used by the controller. To improve converter efficiency, an external 5 V supply is recommended to be connected to the VG pin, thereby overriding the internal 4.8 V regulator. This external supply must be between 5.0 V and 5.5 V and must be present before applying input voltage to the VIN pin. If not supplying an external voltage to this pin, leave this pin open.

7.3.9 Startup into Pre-biased Outputs

The TPSM84A21 prevents the low-side MOSFETs from discharging a pre-biased output. During pre-biased startup, the low-side MOSFETs do not turn on until after the high-side MOSFETs have started switching. The high-side MOSFETs do not start switching until the internal soft-start reference voltage exceeds the voltage at the VADJ pin.

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7.3.10 Thermal Shutdown

The internal thermal shutdown fault is triggered if the junction temperature exceeds 135°C (typ). This interrupts regulation by making the output high impedance. The device reinitiates the power up sequence when the junction temperature drops below 115°C (typ).

7.3.11 Overcurrent Protection

For protection against load faults, the TPSM84A21 incorporates output overcurrent protection. Applying a load that exceeds the module's overcurrent threshold causes the output to shut down and PGOOD is pulled low. Following shut down, the module attempts to restart after a 32.8-ms hiccup interval counter has expired. This provides a hiccup response to an overcurrent condition. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation.

The TPSM84A21 overcurrent trip point is 15 A (typ) when the ILIM pin is left open. This provides enough margin for brief overshoots in inductor currents during a load transient while at the same time protecting against short circuits or other potentially catastrophic faults on the output. The overcurrent trip point can be reduced to 11.25 A (typ) by placing a 47 kΩ between the ILIM pin and PGND. Programming resistors with up to ±5% variation can be used. The current limit selection is latched in at power up and cannot be changed without cycling input power or the EN pin voltage.

7.3.12 Output Undervoltage/Overvoltage Protection

The device incorporates an output undervoltage/overvoltage protection (UVP/OVP) circuit to prevent damage to the load. This fault can be triggered during large, fast load transients if insufficient output capacitance is used. The UVP/OVP feature compares the VADJ pin voltage to internal thresholds. If the VADJ pin voltage is lower than 90% or greater than 110% of the nominal internal reference voltage, the module is turned off, a fault is triggered, and the PGOOD pin is pulled low. When the fault hiccup interval is complete, the module will attempt to restart.

7.3.13 Enable (EN)

The EN pin provides electrical on and off control of the TPSM84A21. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the module stops switching and enters a low power state. There is no voltage hysteresis in the EN threshold. The rising and falling voltage thresholds occur at the same level. The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device.

If an application requires controlling the EN pin, use an open drain/collector device or a suitable logic gate to interface with the pin. 図 15 shows controlling the EN/UVLO pin using a MOSFET, Q1. Turning Q1 on, disables the device. Using a voltage superviser to control the EN pin allows control of the turn-on and turn-off of the device as opposed to relying on the ramp up or down of the input voltage source.

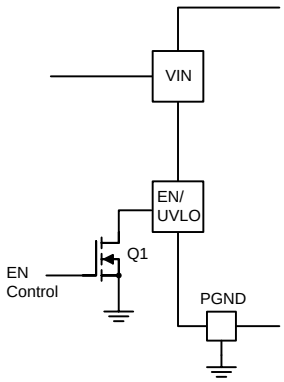


図 15. Enable Control

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7.3.14 Undervoltage Lockout (UVLO)

The TPSM84A21 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 7.65 V(max) with a typical hysteresis of 250 mV.

If an application requires a higher UVLO threshold, the UVLO pin can be configured as shown in 図 16. The value of R_{UVLO1} and R_{UVLO2} can be calculated using 式 3 and 式 4 or selected from 表 2. It is recommended to set the UVLO hysteresis of approximately 500mV in order to avoid repeated chatter during start up or shut down. 表 2 shows recommended R_{UVLO1} and R_{UVLO2} values for various VIN UVLO rising thresholds, with 500 mV of hysteresis.

$$R_{UVLO1} = \frac{V_{IN(RISE)} - V_{IN(FALL)}}{3\ \mu A} \quad (3)$$

$$R_{UVLO2} = \frac{R_{UVLO1} \times 1.23}{V_{IN(FALL)} - 1.23 + (R_{UVLO1} \times 4\ \mu A)} \quad (4)$$

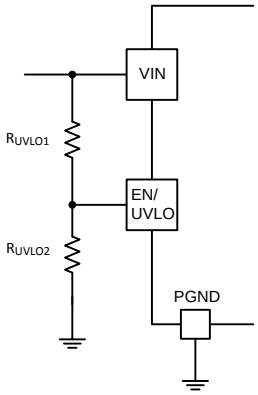


図 16. Adjustable UVLO

表 2. Standard Resistor Values For Adjusting VIN UVLO

VIN UVLO RISING THRESHOLD (V)	8.0	8.5	9.0	9.5	10.0
VIN UVLO FALLING THRESHOLD (V)	7.5	8.0	8.5	9.0	9.5
R_{UVLO1} (kΩ)	169	169	169	169	169
R_{UVLO2} (kΩ)	29.4	27.4	25.5	24.3	22.6

7.4 Device Functional Modes

7.4.1 Active Mode

The TPSM84A21 is in Active Mode when VIN is above the UVLO threshold and the EN/UVLO pin voltage is above the EN high threshold. The simplest way to enable the TPSM84A21 is to leave the EN/UVLO pin floating. This allows self start-up of the TPSM84A21 when the input voltage is above the UVLO threshold.

7.4.2 Light Load Operation

The TPSM84A21 operates in forced continuous conduction mode (FCCM) under light load conditions. When operating in FCCM, the switching frequency remains constant and the high side and low side MOSFETs are turned on and off in a complementary fashion allowing negative inductor current for part of the switching cycle.

7.4.3 Shutdown Mode

The EN/UVLO pin provides electrical ON and OFF control for the TPSM84A21. When the EN/UVLO pin voltage is below the EN threshold, the device is in shutdown mode. In shutdown mode the stand-by current is typically less than 50 μA. The TPSM84A21 also employs under voltage lock out protection. If VIN is below the UVLO level, the output of the regulator turns off.

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8 Application and Implementation

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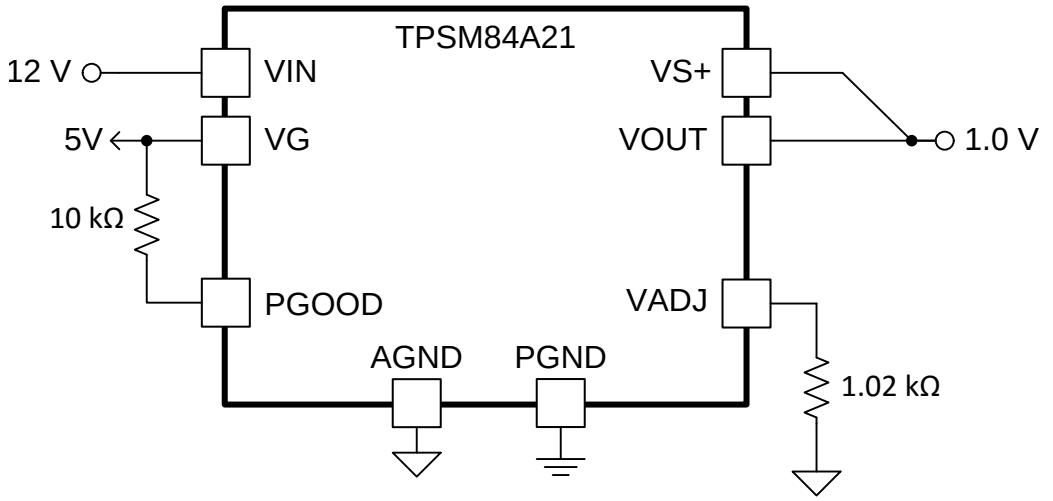
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM84A21 is a synchronous series capacitor step down DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 10 A. The following design procedure can be used to select components for the TPSM84A21. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. Please visit www.ti.com/webench for more details.

8.2 Typical Application

The TPSM84A21 includes both input and output capacitors internal to the device, therefore it only requires a voltage setting resistor and possibly a pull-up resistor on the PGOOD pin in most applications. 図 17 shows a typical TPSM84A21 schematic with only the minimum required components.



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図 17. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 3 and follow the design procedures below.

表 3. Design Parameters

DESIGN PARAMETER	VALUE
Input Voltage V_{IN}	12 V typical
Output Voltage V_{OUT}	1.0 V
Output Current Rating	10 A
Key care-abouts	Tight transient response, small footprint, high efficiency, PGOOD signal
Transient Response Requirements	±2% voltage deviation, 5 A load step, 5 A/µs slew rate

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8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage of the TPSM84A21 is externally adjustable using a single resistor (R_{SET}). Select the value of R_{SET} from or calculate using 式 5:

$$R_{set} = \frac{1}{\frac{V_{out}}{0.508} - 1} (k\Omega) \quad (5)$$

To set the output voltage to 1.0 V, the calculated value for R_{SET} is 1.03 kΩ. The closest E96 value is 1.02 kΩ.

8.2.2.2 Input and Output Capacitance

The TPS84A21 requires no external input or output capacitance to operate. Input and output capacitors can be added to improve ripple or transient response. In this design example, in order to meet the ±2% voltage deviation for a 5-A, 5-A/µs load step, 100 µF of output capacitance is required.

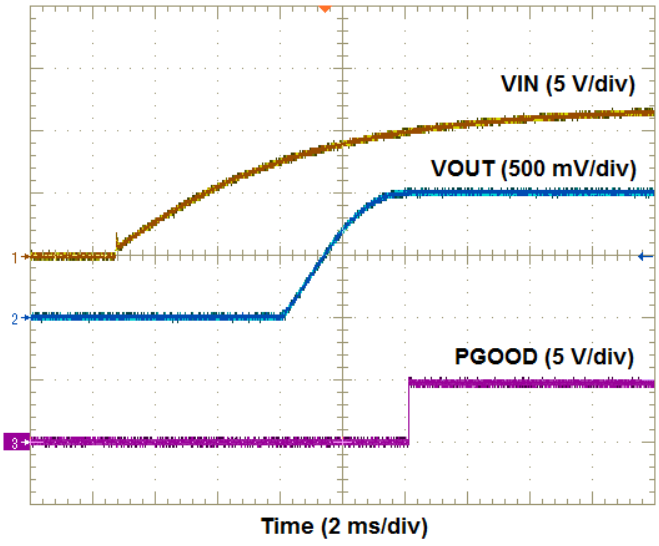
8.2.2.3 Power Good (PGOOD)

Applications requiring voltage rail sequencing can benefit from the PGOOD signal present with the TPSM84A21. The PGOOD pin is an open drain output. When the output voltage is typically between 95% and 105% of the set point, the PGOOD pin pull-down is released and the pin floats, requiring an external pull-up resistor for a high signal. A 10-kΩ pull-up resistor is placed between the PGOOD pin and an external 5V rail.

8.2.2.4 External VG Voltage

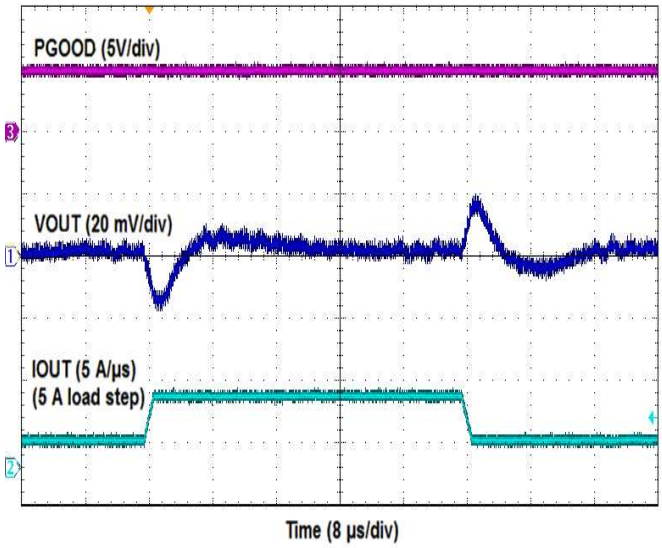
The VG supply rail is used to power the internal gate drivers and other internal supply rails used by the controller. For best efficiency, supply an external 5 V to the VG pin, thereby overriding the internal 4.8 V regulator. Expect a 2-3% efficiency improvement by driving the VG pin with an external 5V.

8.2.3 Application Curves



VIN = 12 V VOUT = 1.0 V

図 18. Start-up Waveforms



VIN = 12 V VOUT = 1.0 V Load Step = 5 A
COUT = 100 µF Slew Rate = 1 A/µs

図 19. Application Transient Response

9 Power Supply Recommendations

The TPSM84A21 is designed to operate from an input voltage supply range between 8 V and 14 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the TPSM84A21, additional bulk capacitance may be required at the input pins. A typical recommended amount of bulk input capacitance is 47 μF - 100 μF.

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10 Layout

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 図 20 and 図 22 show typical, top-side PCB layouts. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- When adding input and output ceramic capacitors, place them close to the device pins to minimize high frequency noise.
- Locate any additional output capacitors between the ceramic capacitors and the load.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Place R_{SET} as close as possible to the VADJ pin.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Examples

The layout shown in 図 20 shows the minimum solution size with only a single voltage setting resistor (R1) as the only additional required component. 図 21 shows a typical internal PCB layer with a trace connecting the VS+ pin to VOUT near the load.

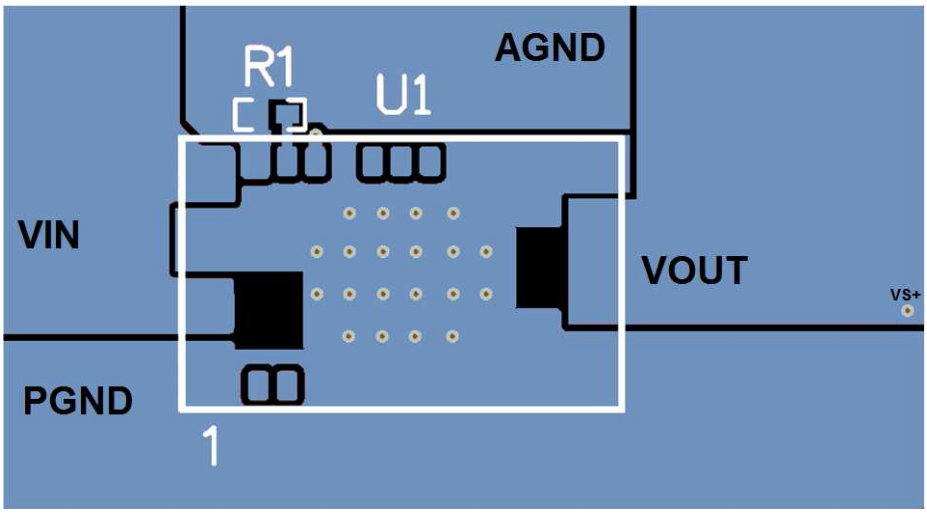


図 20. Minimum Component Layout

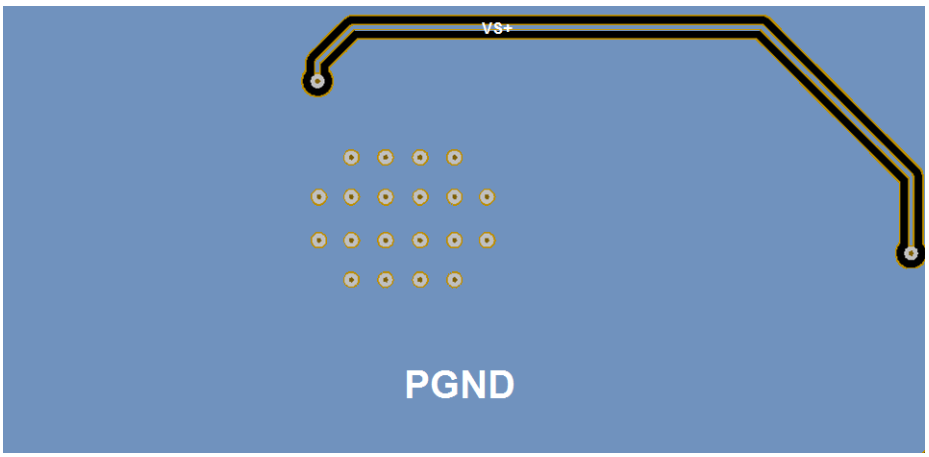


図 21. VS+ Trace on Internal Layer

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Layout Examples (continued)

図 22 shows a layout with the placement of additional ceramic input capacitors (C1, C3) and ceramic output capacitors (C2, C4) for designs that require additional ripple reduction or improved transient response. 図 23 shows a typical internal PCB layer with a trace connecting the VS+ pin to VOUT near the load

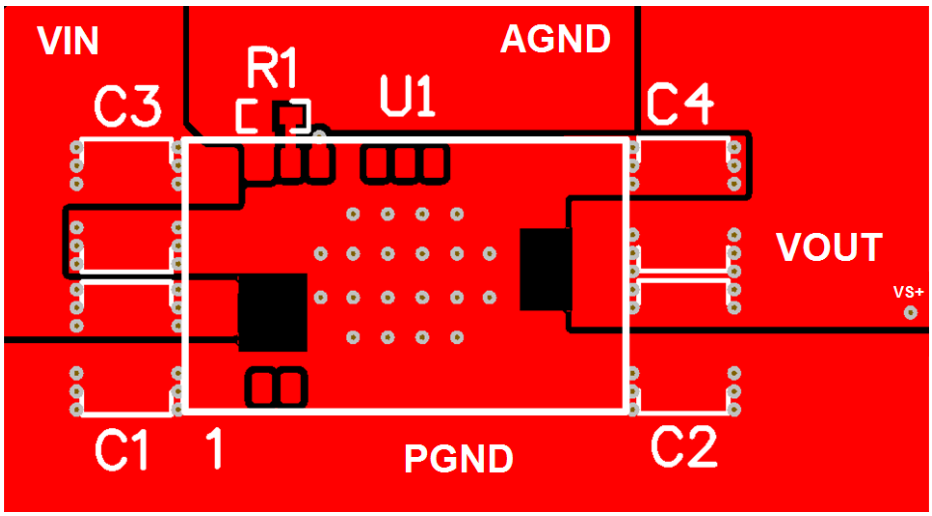


図 22. Layout with Optional CIN and COUT

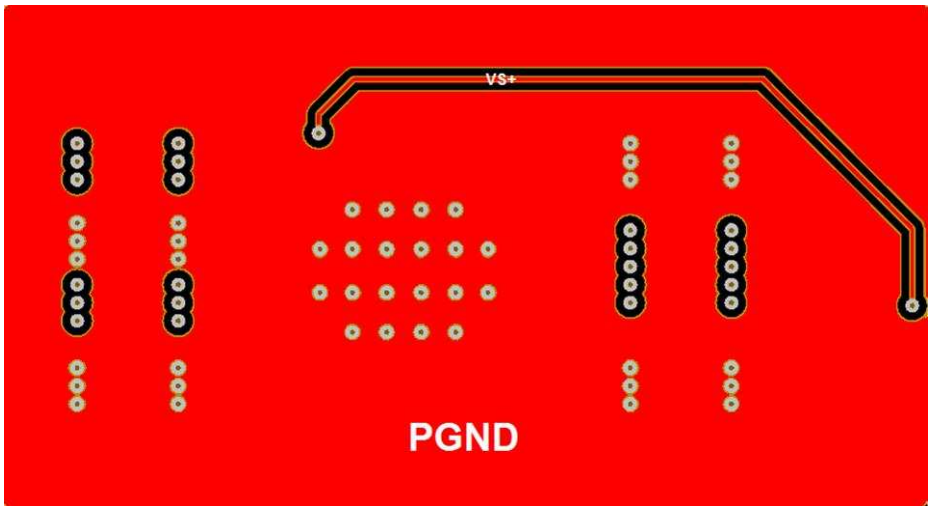


図 23. VS+ Trace on Internal Layer

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10.3 EMI

The TPSM84A21 is compliant with EN55022 Class B radiated emissions. 図 24 to 図 27 show typical examples of radiated emissions plots for the TPSM84A21. Graphs included show plots of the antenna in the horizontal and vertical positions.

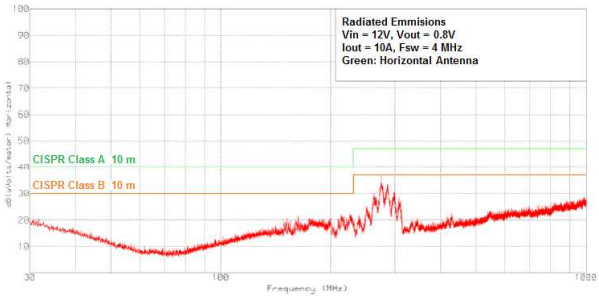


図 24. Radiated Emissions 12-V Input, 0.8-V Output, 10-A Load, Horizontal Antenna

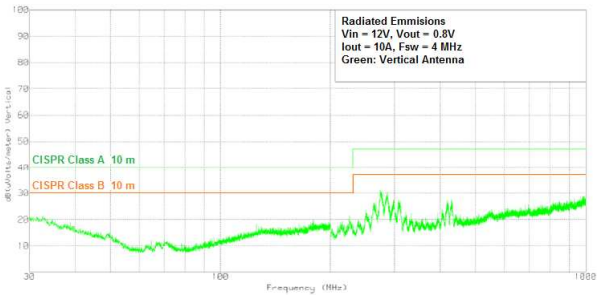


図 25. Radiated Emissions 12-V Input, 0.8-V Output, 10-A Load, Vertical Antenna

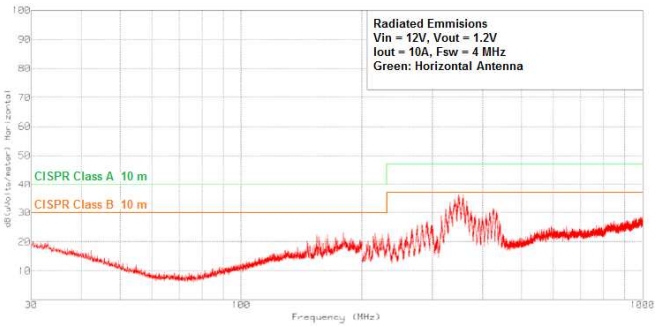


図 26. Radiated Emissions 12-V Input, 1.2-V Output, 10-A Load, Horizontal Antenna

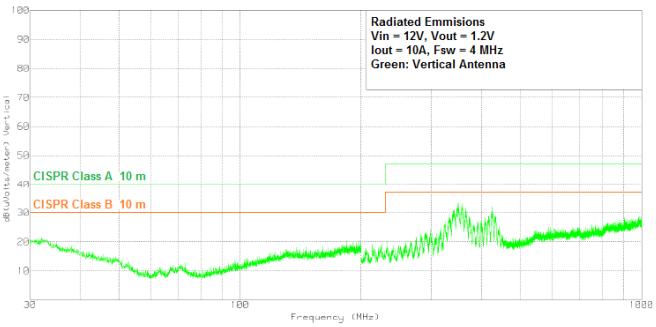


図 27. Radiated Emissions 12-V Input, 1.2-V Output, 10-A Load, Vertical Antenna

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください：

- 『TPSM84A22 8V～14V入力、1.2V～2.05V出力、10A SWIFT™電源モジュール』、SLVSDF8
- 『TPS54A20 8V～14V入力、10A、最高10MHzの SWIFT™降圧型コンバータ』、SLVSCQ8

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

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11.5 静電気放電に関する注意事項



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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM84A21MOJR	Active	Production	QFM (MOJ) | 20	500 | LARGE T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	TPSM84A21
TPSM84A21MOJR.A	Active	Production	QFM (MOJ) | 20	500 | LARGE T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	TPSM84A21
TPSM84A21MOJT	Active	Production	QFM (MOJ) | 20	250 | SMALL T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	TPSM84A21
TPSM84A21MOJT.A	Active	Production	QFM (MOJ) | 20	250 | SMALL T&R	In-Work	NIAU	Level-3-260C-168 HR	-40 to 85	TPSM84A21

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

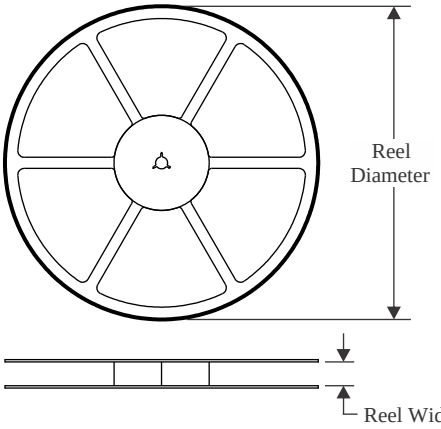
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

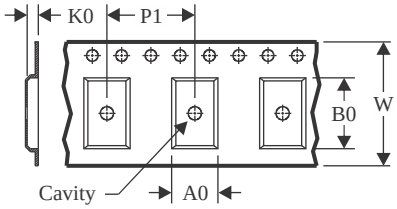
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

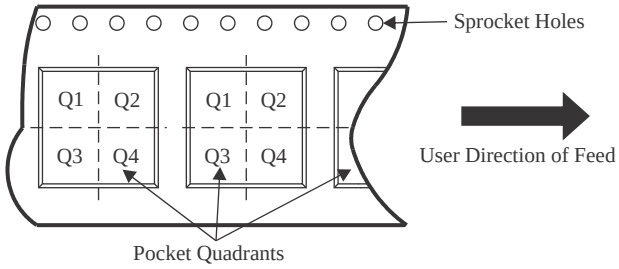


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

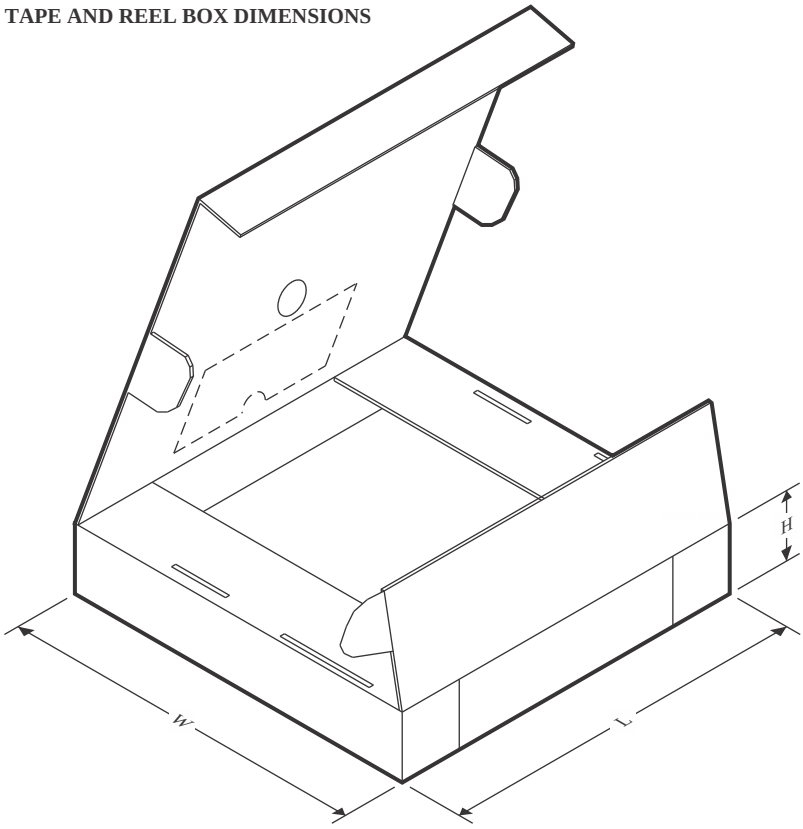
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM84A21MOJR	QFM	MOJ	20	500	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1
TPSM84A21MOJT	QFM	MOJ	20	250	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

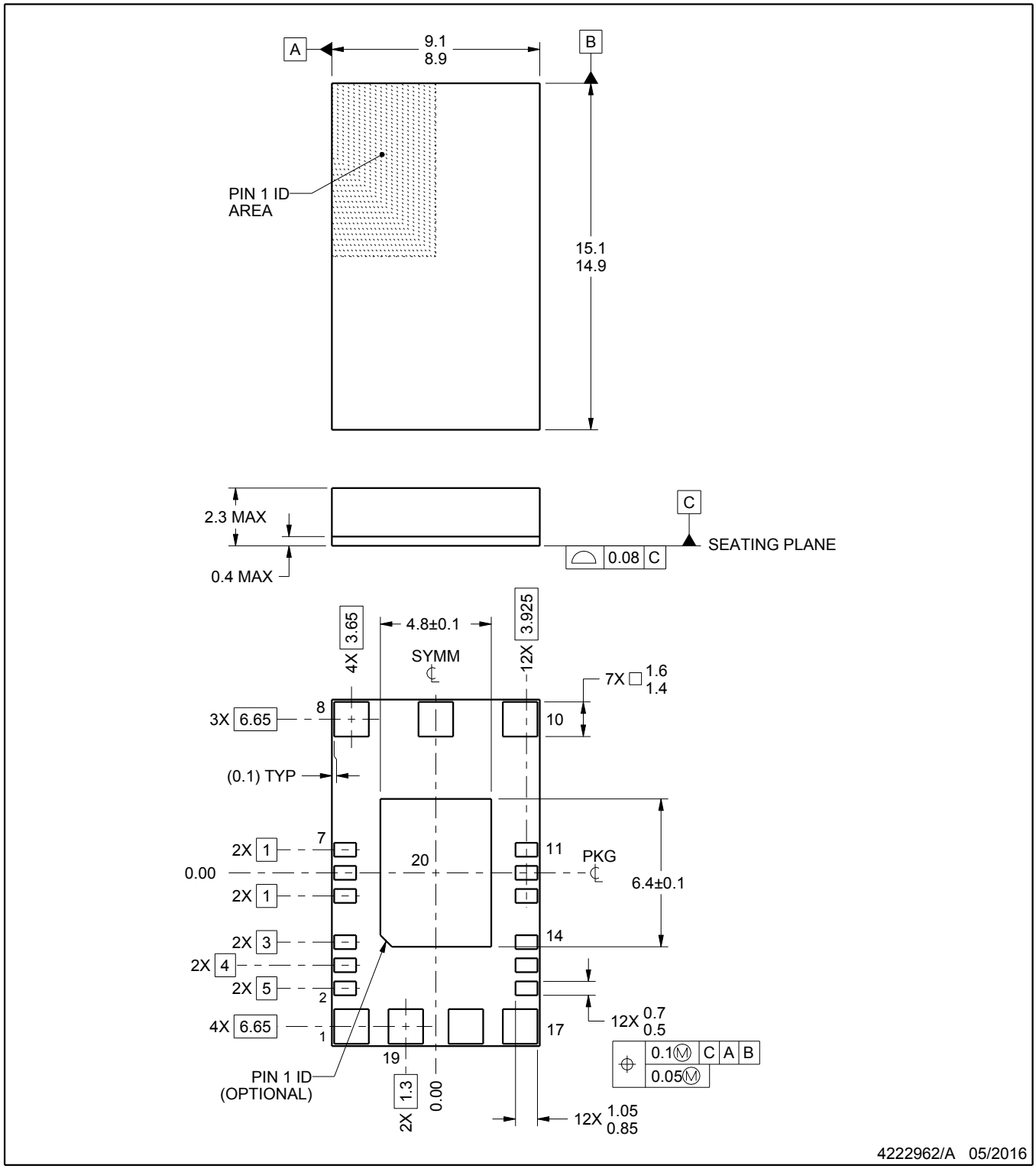
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM84A21MOJR	QFM	MOJ	20	500	383.0	353.0	58.0
TPSM84A21MOJT	QFM	MOJ	20	250	383.0	353.0	58.0

PACKAGE OUTLINE

MOJ0020A

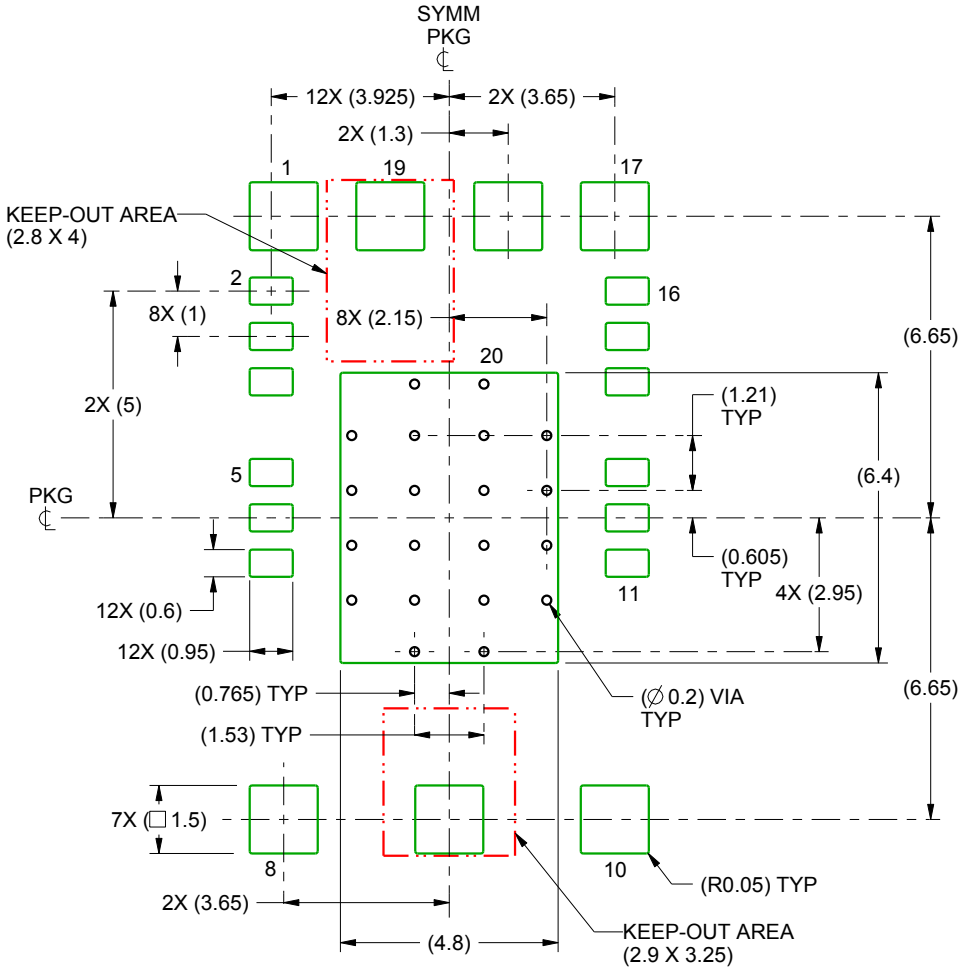
QFM - 2.3 mm max height

QUAD FLAT MODULE

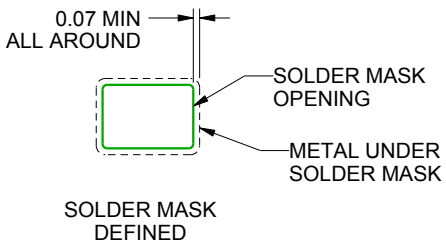


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:6X

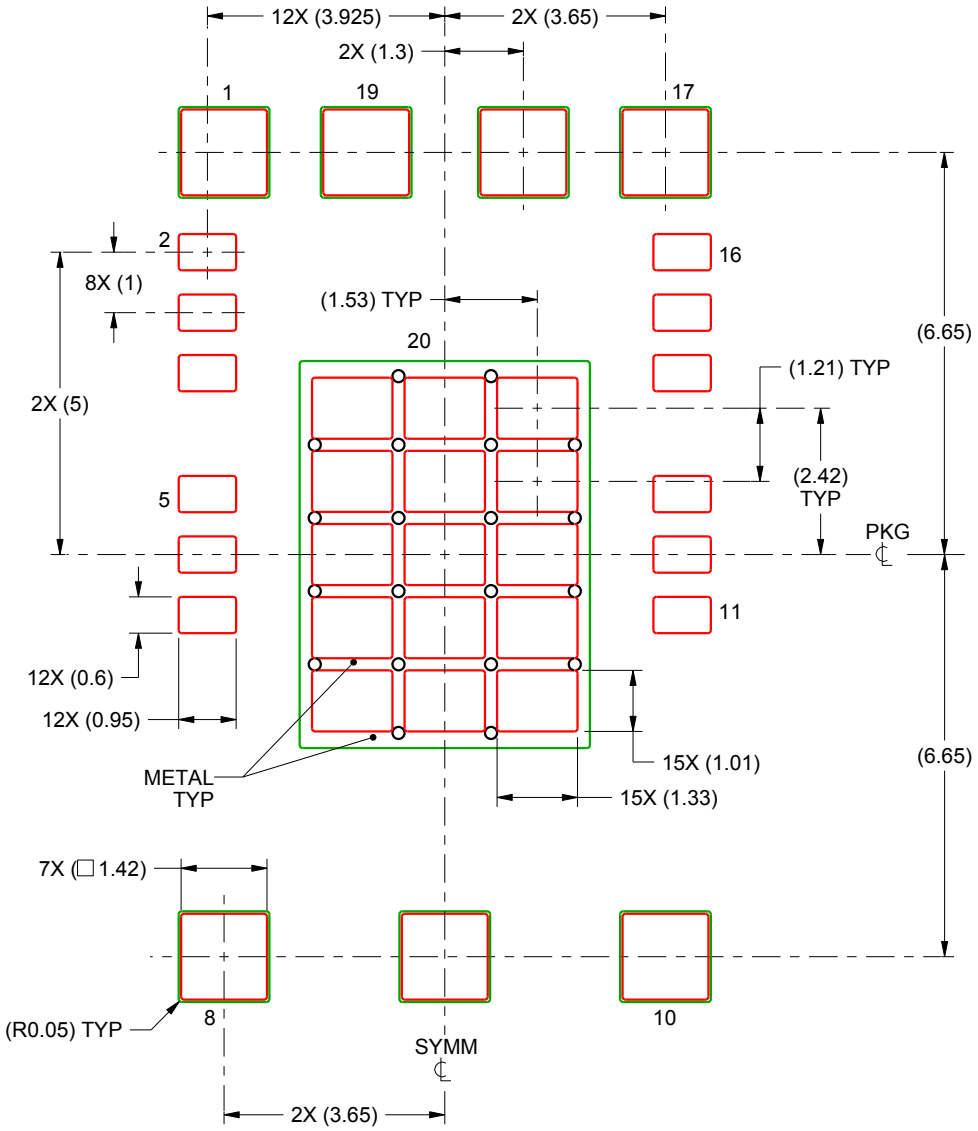


SOLDER MASK
DEFINED

4222962/A 05/2016

NOTES: (continued)

3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 8-10 & 17-19: 90%
PAD 20: 65.6 %
SCALE:8X

4222962/A 05/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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