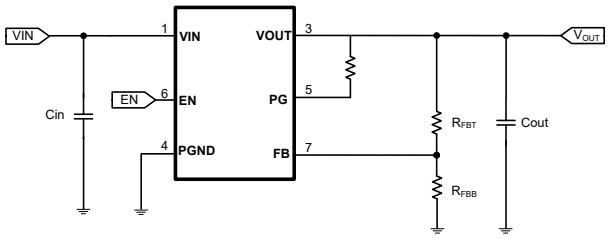
TPSM86325x 3V～17V 入力、3A、同期整流降圧モジュール、QFN パッケージ

1 特長

- 多様なアプリケーションに適した構成
  - 入力電圧範囲:3V ～ 17V
  - TPSM863252 の出力電圧範囲:0.6V～10V
  - TPSM863257 の出力電圧範囲:0.6V～5.5V
  - TPSM863253 の固定 3.3V 出力電圧
  - 0.6V の基準電圧
  - 25℃で ±1% の基準電圧精度
  - -40℃～125℃で ±1.5% の基準電圧精度
  - 55mΩ と 24mΩ の各 MOSFET を内蔵
  - 100μA 低静止時電流
  - 1.2MHz のスイッチング周波数
  - 最大 95% の高デューティ サイクル動作
  - 高精度の EN スレッショルド電圧
  - 1.6ms (標準値) の固定ソフト スタート時間
- 使いやすく小さい設計サイズ
  - TPSM863252 Eco モード、TPSM863257 および TPSM863253 FCCM モード (軽負荷時)
  - 高速過渡 D-CAP3™ 制御モード
  - ブートストラップ コンデンサおよびインダクタを内蔵することでレイアウトを容易化
  - プリバイアス付き出力電圧でのスタートアップに対応
  - ラッチなしの OV、OT、UVLO 保護
  - サイクル単位の OC および NOC 保護
  - 動作時接合部温度:-40℃～125℃
  - 3.3mm × 4mm × 2mm の QFN パッケージ
- WEBENCH® Power Designer により、TPSM863252 を使用するカスタム設計を作成
- WEBENCH® Power Designer により、TPSM863253 を使用するカスタム設計を作成
- WEBENCH® Power Designer により、TPSM863257 を使用するカスタム設計を作成



概略回路図

2 アプリケーション

- 商用ネットワークとサーバーの電源
- AC/DC アダプタ / 電源
- ファクトリ オートメーションおよび制御
- 試験 / 測定機器

3 概要

TPSM86325x はシンプルで使いやすい、高効率、高電力密度の同期整流降圧モジュールで、入力電圧範囲は 3V～17V で、最大 3A の連続電流に対応しています。

TPSM86325x は、過渡応答を高速化するため、かつ外部補償を行わなくても低 ESR 出力コンデンサが使えるように、D-CAP3 制御モードを採用しています。このデバイスは、最大 95% のデューティ サイクルでの動作をサポートできます。

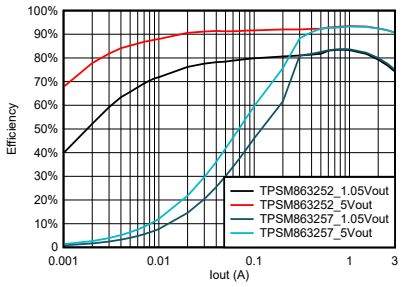
TPSM863252 は Eco モードで動作することで、軽負荷時も高い効率を維持します。TPSM863257 は FCCM モードで動作することで、すべての負荷条件で同じ周波数と小さい出力リップルを維持します。TPSM863253 は FCCM モードの 3.3V 固定出力電圧部品です。内部モジュールには TPS863253 分圧抵抗とフィードフォワード コンデンサが内蔵されています。このデバイスは、OVP、OCP、UVLO、OTP、UVP (ヒカップ機能付き) による完全な保護機能を備えています。

このデバイスは、QFN パッケージで供給されます。接合部温度の仕様は -40℃～125℃です。

製品情報

部品番号(3)	モード	出力電圧	パッケージ (1)	パッケージ サイズ (2)
TPSM863252	ECO	0.6V～10V	RDX (QFN-FCMOD、7)	4.00mm × 3.30mm
TPSM863257	FCCM	0.6V～5.5V		
TPSM863253	FCCM	3.3V		

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 「ファミリ デバイス」の表を参照してください。



TPSM86325x の効率 (V_{IN} = 12V)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Family Devices

PART NUMBER	CURRENT (A)	OUTPUT VOLTAGE (V)	MODE
TPSM863252	0 to 3	0.6 to 10	Eco
TPSM863253	0 to 3	3.3	FCCM
TPSM863257	0 to 3	0.6 to 6	FCCM
TPSM861252	0 to 1	0.6 to 10	Eco
TPSM861253	0 to 1	3.3	FCCM
TPSM861257	0 to 1	0.6 to 6	FCCM

5 Pin Configuration and Functions

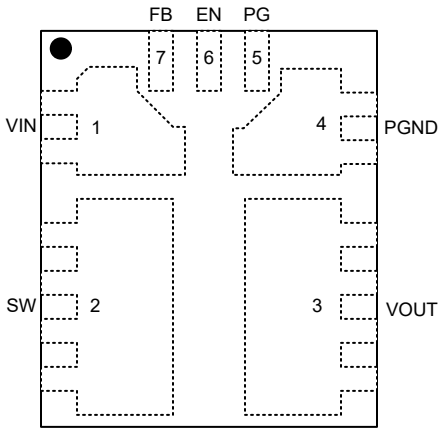

図 5-1. TPSM863252, TPSM863257 RDX Package, 7-Pin QFN-FCMOD (Top View)

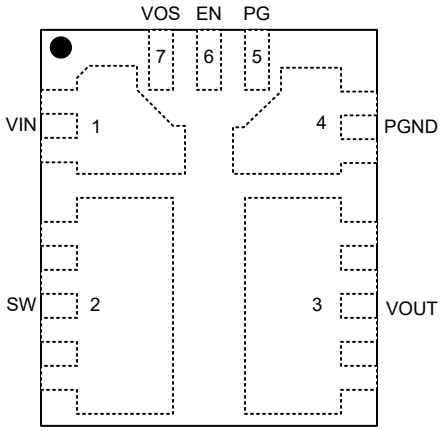

図 5-2. TPSM863253 RDX Package, 7-Pin QFN-FCMOD (Top View)

表 5-1. Pin Functions

Pin		Type[1]	Description
Name	NO.		
VIN	1	P	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
SW	2	NC	Switch pin of the power stage. Do not connect, leave floating.
VOUT	3	P	Output connection. Connect recommended output capacitance from VOUT to PGND.
PGND	4	G	Power ground connection
PG	5	A	Power-good open drain output. PG pin can be floating.
EN	6	A	Enable pin of buck converter. Drive EN high to turn on the converter; drive EN low to turn off the converter. Internal pulldown to GND by a resistor.
FB	7	A	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and ground.
VOS	7	A	TPSM863253: Converter feedback input. Connect to Vout directly.

(1) A = Analog, P = Power, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	18	V
Input voltage	FB, EN, PG	–0.3	6	V
GND	GND	–0.3	0.3	V
Output voltage	VOUT(TPSM863252)	–0.3	11	V
Output voltage	VOUT(TPSM863257)	–0.3	6	V
Mechanical shock	Mil-STD-883D, Method 2002.3, 1ms, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000Hz		20	G
Operating junction temperature range, TJ		–40	150	°C
Storage temperature, Tstg	Storage temperature, Tstg	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	± 2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	± 500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	3		17	V
Input voltage	FB, EN, PG	–0.1		5.5	V
GND	GND	–0.1		0.1	V
Output voltage	VOUT(TPSM863252)	–0.1		10	V
Output voltage	VOUT(TPSM863253)		3.3		V
Output voltage	VOUT(TPSM863257)	–0.1		5.5	V
Output current	IO	0		3	A
T_J	Operating junction temperature	–40		125	°C
Tstg	Storage temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPSM86325x RDX 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.3	°C/W
$R_{\theta JA_effective}$	Junction-to-ambient thermal resistance on EVM board	40[2]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) This RθJA_effective is tested on TPSM863252EVM board (4 layer board, copper thickness of top and bottom layer are 2oz, and copper thickness of internal GND is 1oz) at Vin = 12V, Vout = 5V, Iout = 3A , TA = 25ºC.

6.5 Electrical Characteristics

Over operating T_J = –40ºC – 125ºC, V_{VIN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range	VIN	3		17	V
I_{VIN}	VIN supply current	No load, V_{EN} = 5V, non-switching, PSM version		100		µA
		No load, V_{EN} = 5V, non-switching, FCCM version		370		µA
I_{INSDN}	VIN shutdown current	No load, V_{EN} = 0V		2		µA
UVLO						
UVLO	VIN undervoltage lockout	Wake up VIN voltage	2.8	2.9	3.0	V
UVLO	VIN undervoltage lockout	Shut down VIN voltage	2.6	2.7	2.8	V
UVLO	VIN undervoltage lockout	Hysteresis VIN voltage		200		mV
FEEDBACK VOLTAGE						
VFB	FB voltage	T_J = 25°C	594	600	606	mV
VFB	FB voltage	T_J = –40°C to 125°C	591	600	609	mV
VOUT	TPSM863253 output voltage	T_J = 0°C to 65°C	3.27	3.3	3.33	V
VOUT	TPSM863253 output voltage	T_J = –40°C to 125°C	3.25	3.3	3.35	V
MOSFET						
$R_{DS(ON)HI}$	High-side MOSFET Rds(on)	T_J = 25°C, V_{VIN} ≥ 5V		55		mΩ
		T_J = 25°C, V_{VIN} = 3V [1]		68		mΩ
$R_{DS(ON)LO}$	Low-side MOSFET Rds(on)	T_J = 25°C,V_{VIN} ≥ 5V		24		mΩ
		T_J = 25°C, V_{VIN} = 3V		30		mΩ
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	T_J = 25°C, V_{VOUT} = 3.3V		1.2		MHz
$T_{OFF(MIN)}$ [1]	Minimum off-time	V_{FB} = 0.5V		110		ns
$T_{ON(MIN)}$	Minimum on-time			60		ns
CURRENT LIMIT						
I_{OCL_LS}	Over current threshold	Valley current set point	3.1	4.1	5.1	A

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6.5 Electrical Characteristics (続き)

Over operating T_J = –40ºC – 125ºC, V_{VIN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{NOCL}	Negative over current threshold	Valley current set point	1.5	2.0	2.5	A
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN threshold high-level		1.15	1.20	1.25	V
$V_{EN(OFF)}$	EN threshold low-level		0.90	1.00	1.10	V
V_{ENHYS}	EN hystersis			200		mV
REN1	EN pulldown resistor			2		MΩ
OUTPUT DISCHARGE and SOFT START						
t_{SS}	Internal soft-start time			1.6		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold		110	115	120	%
t_{OVPDLY}	OVP prop deglitch			24		us
V_{UVP}	UVP trip threshold		55	60	65	%
t_{UVPDLY}	UVP prop deglitch			220		us
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect		14		ms
PGOOD						
TPGDLY	PG start-up delay	PG from low to high		1		ms
TPGDLY	PG start-up delay	PG from high to low		28		us
VPGTH	PG threshold	VFB falling (fault)	80	85	90	%
VPGTH	PG threshold	VFB rising (good)	85	90	95	%
VPGTH	PG threshold	VFB rising (fault)	110	115	120	%
VPGTH	PG threshold	VFB falling (good)	105	110	115	%
VPG_L	PG sink current capability	IOL = 4mA			0.4	V
IPGLK	PG leak current	VPGOOD = 5.5V			1	uA
THERMAL PROTECTION						
T_{OTP} (1)	OTP trip threshold			155		°C
T_{OTPHSY} (1)	OTP hysteresis			20		°C

(1) Specified by design

6.6 Typical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12V (unless otherwise noted)

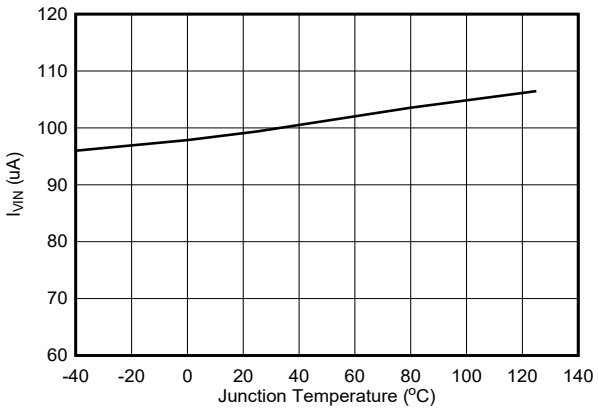

図 6-1. TPSM863252 Quiescent Current

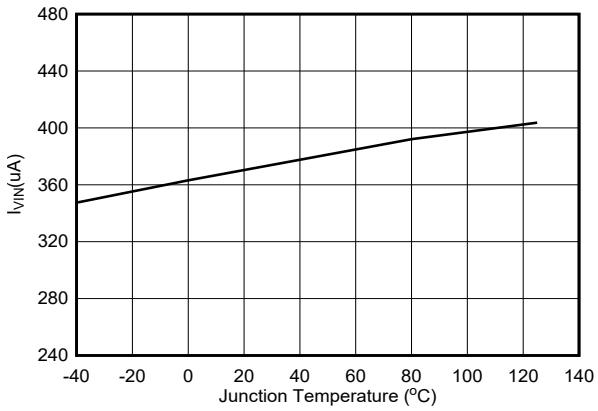

図 6-2. TPSM863257 Quiescent Current

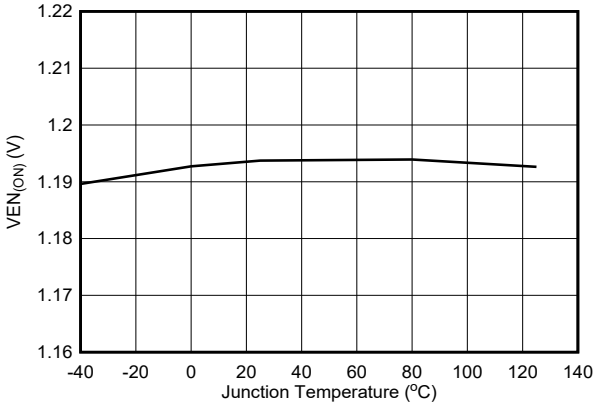

図 6-3. Enable On Threshold Voltage

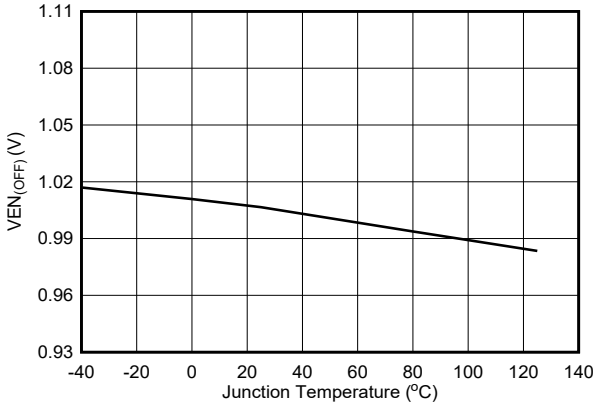

図 6-4. Enable Off Threshold Voltage

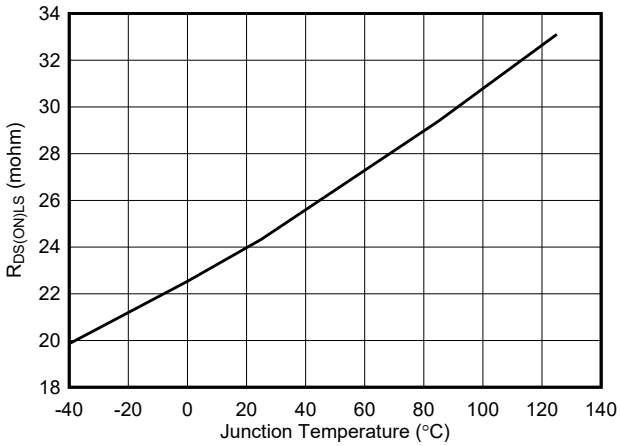

図 6-5. Low-Side $R_{DS(ON)}$

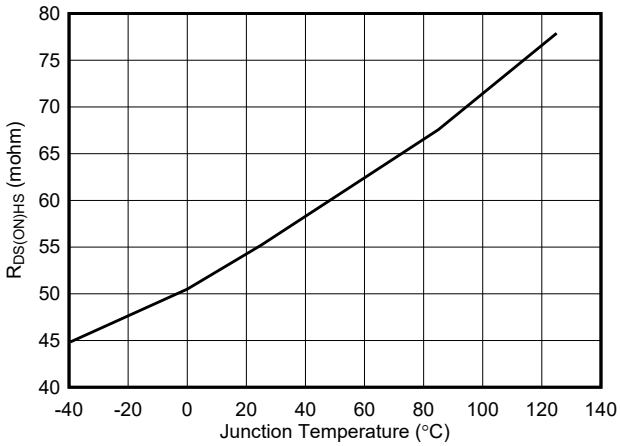

図 6-6. High-Side $R_{DS(ON)}$

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6.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V (unless otherwise noted)

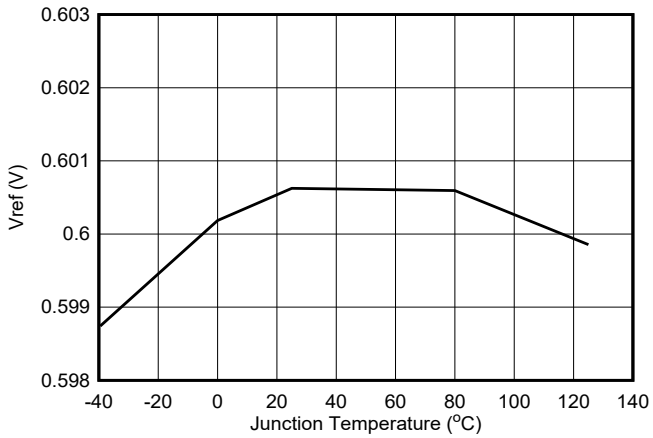

図 6-7. VREF Voltage

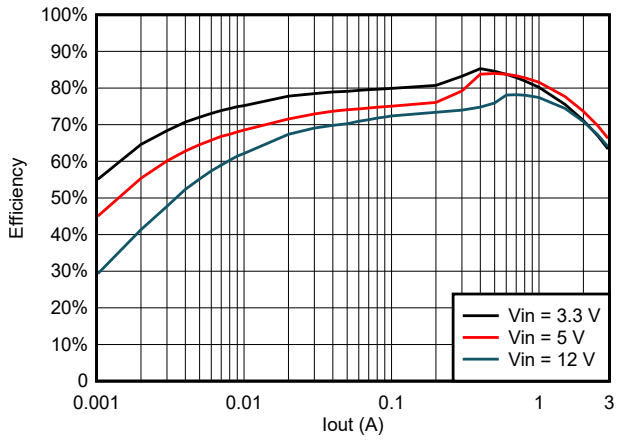

図 6-8. TPSM863252 Efficiency at 0.6V_{OUT}

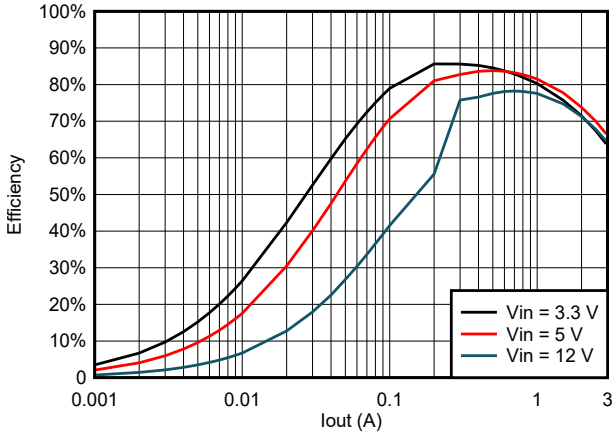

図 6-9. TPSM863257 Efficiency at 0.6V_{OUT}

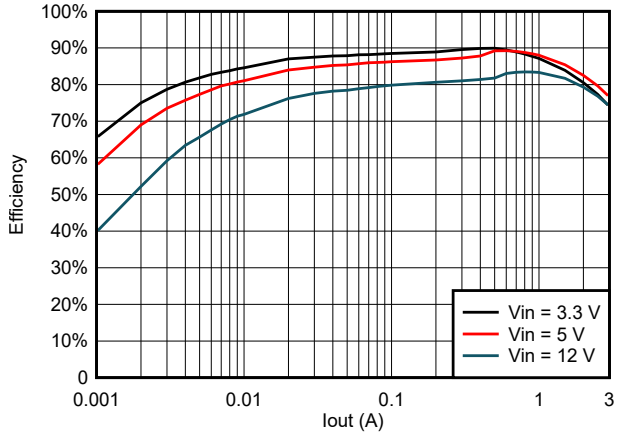

図 6-10. TPSM863252 Efficiency at 1.05V_{OUT}

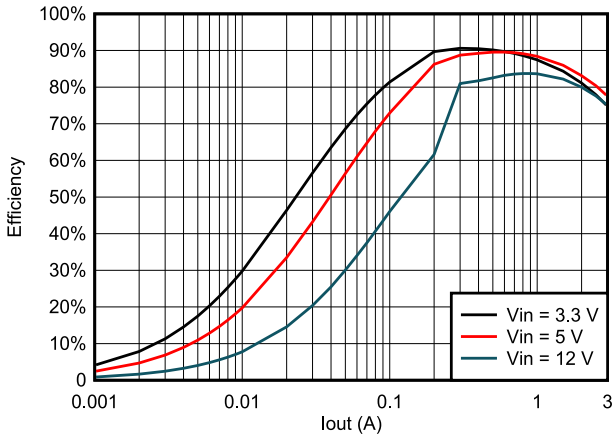

図 6-11. TPSM863257 Efficiency at 1.05V_{OUT}

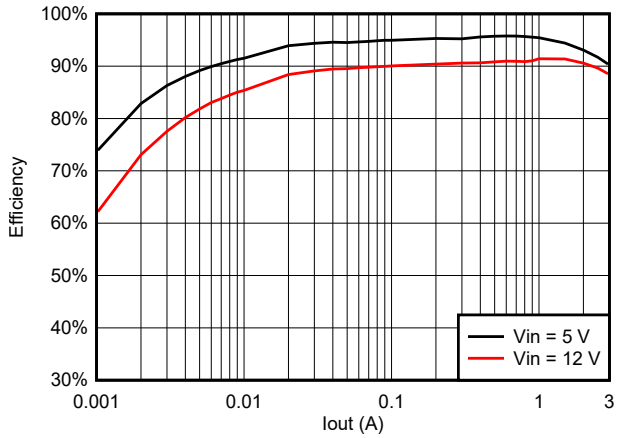

図 6-12. TPSM863252 Efficiency at 3.3V_{OUT}

6.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V (unless otherwise noted)

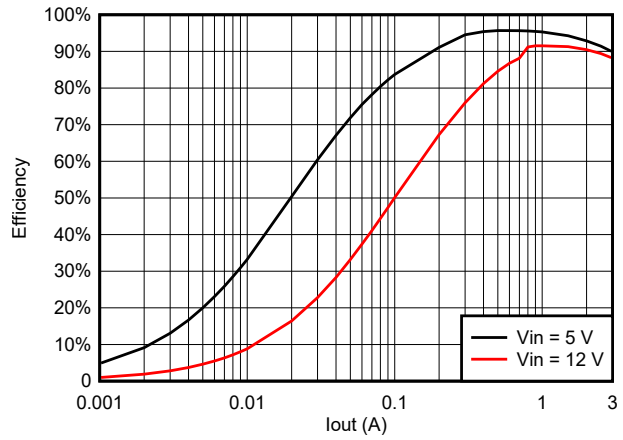

図 6-13. TPSM863257 Efficiency at 3.3V_{OUT}

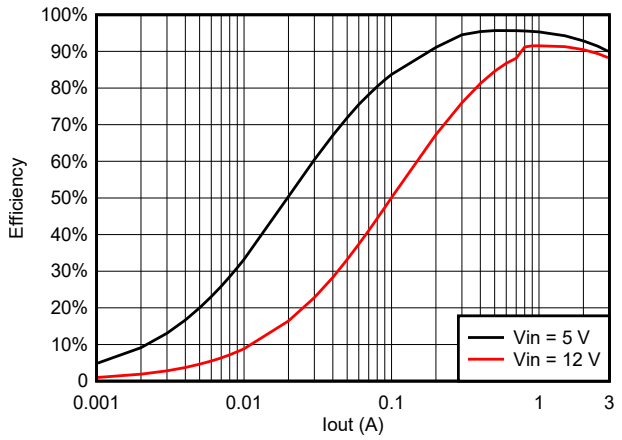

図 6-14. TPSM863253 Efficiency at 3.3V_{OUT}

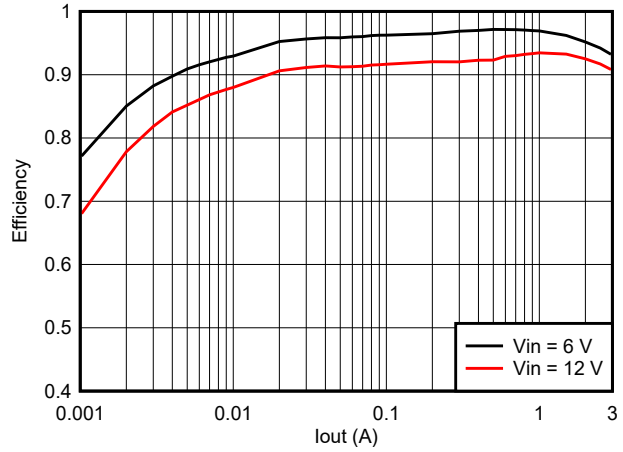

図 6-15. TPSM863252 Efficiency at 5V_{OUT}

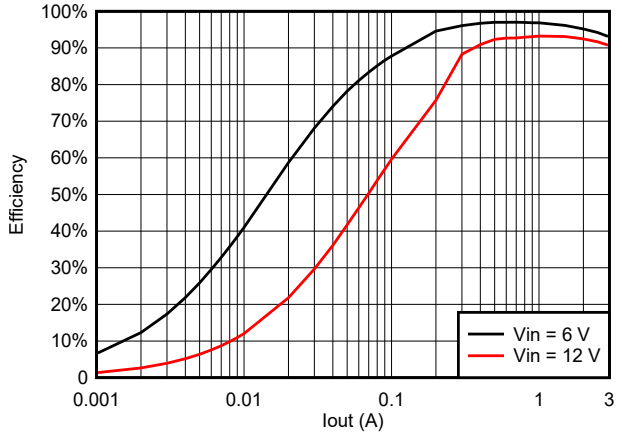

図 6-16. TPSM863257 Efficiency at 5V_{OUT}

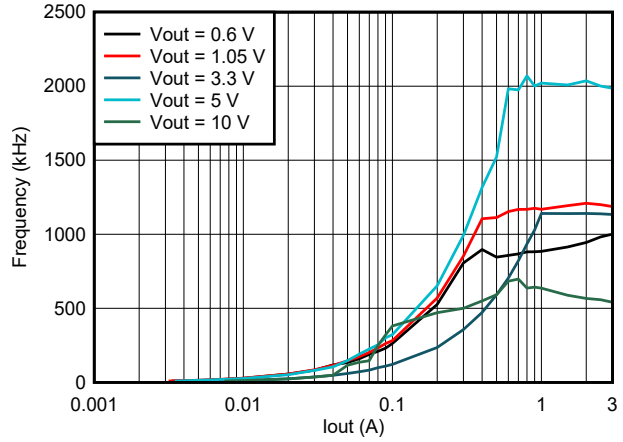

図 6-17. TPSM863252 Frequency vs Loading at 12V Input Voltage

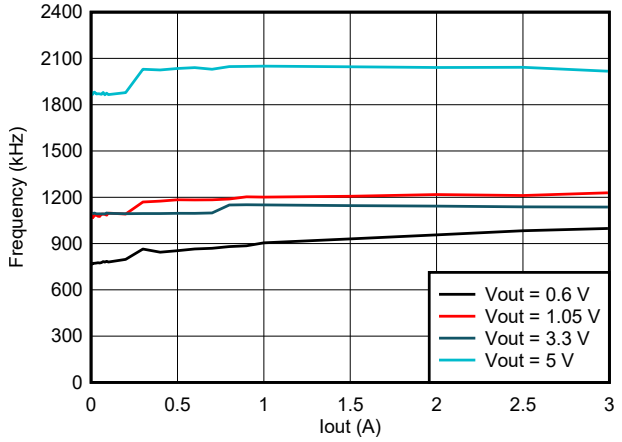

図 6-18. TPSM863257 Frequency vs Loading at 12V Input Voltage

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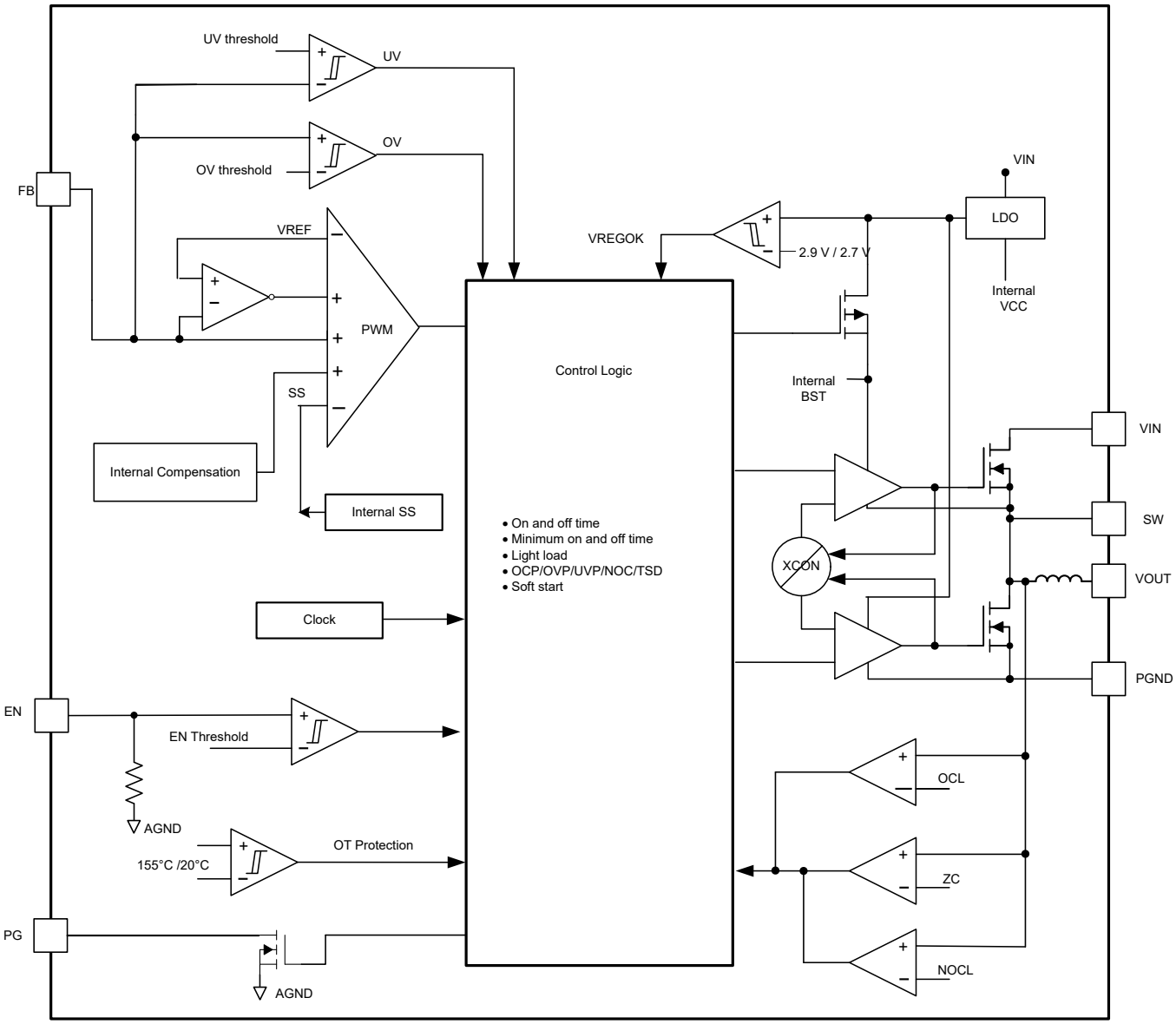
7 Detailed Description

7.1 Overview

The TPSM86325x is a 3A, integrated, FET, synchronous buck module that operates from 3V to 17V input voltage and TPSM863252 output voltage range is 0.6V to 10V. TPSM863257 output voltage range is 0.6V to 5.5V. TPSM863253 is fixed 3.3V output voltage version. The device employs a D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 control mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation mode at lighter load condition.

The Eco-mode version allows the TPSM863252 to maintain high efficiency at light load. The FCCM version allows the TPSM863253 and TPSM863257 to maintain a fixed switching frequency and lower voltage output ripple. The TPSM86325x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The device is stable even with virtually no ripple at the output. The TPSM86325x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

7.3.2 Eco-mode Control

The TPSM863252 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer time. This event makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use the below equation to calculate the transition point to the light load operation $I_{OUT(LL)}$ current. The typical inductance is 1uH.

$$I_{out(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Prebiased Soft Start

The TPSM86325x has an internal fixed 1.6ms soft-start time. The EN default status is low. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes higher than the feedback voltage, V_{FB}. This scheme makes sure that the converter ramps up smoothly into the regulation point.

7.3.4 Overvoltage Protection

The TPSM86325x has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, the OVP is triggered with a 24µs deglitch time. Both the high-side MOSFET and the low-side MOSFET drivers are turned off. When the overvoltage condition is removed, the device returns to switching.

7.3.5 Frequency

TPSM86325x default frequency is about 1.2MHz. When output voltage is higher than 3.6V and the ration of output voltage to input voltage < 0.62 (the hysteresis is 0.04), the frequency changes to 2MHz to decrease output voltage ripple. The following table shows a summary.

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表 7-1. TPSM86325x Frequency at CCM

Conditions	Conditions	Frequency
Output voltage < 3.6V		1.2MHz
Output voltage ≥ 3.6V	Duty ≥ 0.62	1.2MHz
	Duty < 0.62	2MHz

7.3.6 Large Duty Operation

The TPSM86325x can support large duty operations up to 95% by smoothly dropping down the switching frequency. When V_{IN} / V_{OUT} < 1.6 and V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make t_{ON} extended to implement the large duty operation and keep output voltage. The minimum switching frequency is limited to approximately 600kHz.

7.3.7 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the off state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- On time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT}. If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects this action and the device shuts down after the UVP delay time and restarts after the hiccup wait time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPSM863257 is a FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When the NOC condition is removed, the device returns to normal switching.

7.3.8 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is a non-latch protection.

7.3.9 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This protection is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Eco-mode Operation

The TPSM863252 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes a longer time. This event makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

7.4.2 FCCM Mode Operation

The TPSM863253 and TPSM863257 operate in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency is maintained at an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical buck DC/DC converter that is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3A. The following design procedure can be used to select component values for TPSM86325x. Alternately, the WEBENCH Power Designer software can be used to generate a complete design. The WEBENCH Power Designer software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in 図 8-1 is developed to meet the requirements in 表 8-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

図 8-1 shows the 12V input, 1.05V output converter schematic.

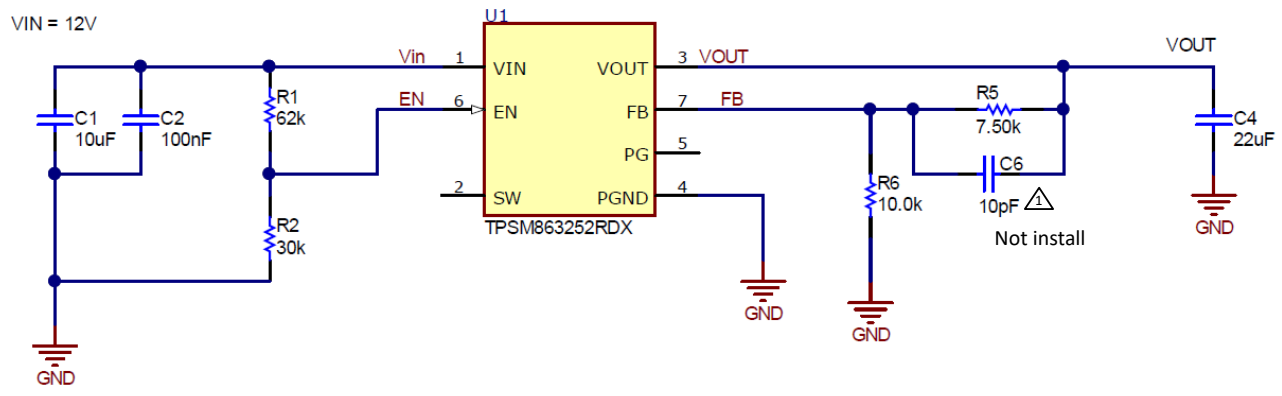

図 8-1. Schematic

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

Parameter		Conditions	MIN	TYP	MAX	Unit
V_{OUT}	Output voltage			1.05		V
I_{OUT}	Output current			3		A
ΔV_{OUT}	Transient response	0.3A – 2.7A load step, 1A/µs slew rate		±3% × V_{OUT}		V
V_{IN}	Input voltage		4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		20		mV
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPSM863252 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPSM863253 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPSM863257 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Start by using 式 2 to calculate V_{OUT}.

To improve efficiency at very light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. Use a 10kΩ resistor for R_6 to start the design.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_5}{R_6}\right) \tag{2}$$

8.2.2.3 Output Filter Selection

TPSM86325x integrates a 1uH inductor. TI suggests to use below output cap to make the loop stable. TI suggests CFF range to use 10pF to 100pF.

表 8-2. Recommended Component Values

Output Voltage (V)	R5 (kΩ)	R6 (kΩ)	Minimum C_{OUT} (µF)	Typical C_{OUT} (µF)	Maximum C_{OUT} (µF)	CFF (pF)
0.8	3.3	10.0	22	44	100	—
1.05	7.5	10.0	10	22	88	—
2.5	95.0	30.0	10	22	88	22
3.3	135.0	30.0	22	44	100	22
5	220.0	30.0	22	44	100	22
10	470.0	30.0	22	44	100	10

The capacitor value and ESR determines the amount of output voltage ripple. The TPSM86325x are intended for use with ceramic or other low-ESR capacitors. Use 式 3 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times f_{SW}} \tag{3}$$

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For this design, one MuRata GRM21BR61A226ME44L, 22µF output capacitor are used. The typical ESR is 2mΩ each.

8.2.2.4 Input Capacitor Selection

The TPSM86325x requires an input decoupling capacitor, and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10µF for the decoupling capacitor. TI recommends an additional 0.1µF capacitor from the VIN pin to ground to provide high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.2.5 Enable Circuit

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold, the device starts switching, and when the EN pin voltage falls below the turn-off threshold, thr IC stops switching. The default status is low. There is a 2MΩ internal pulldown resistor in the EN pin.

EN can be controlled by a typical divider resistor circuit from Vin or by a voltage of lower than 5.5V.

Because there is a 2MΩ internal pulldown resistor in the EN pin, TPSM86325x also supports to only connect a top resistor from VIN pin to EN pin. EN voltage is got by the divide net of top resistor and 2MΩ. EN voltage cannot be allowed to be over 6V.

8.2.3 Application Curves

The following data is tested with V_{IN} = 12V, V_{OUT} = 1.05V, T_A = 25°C, unless otherwise specified.

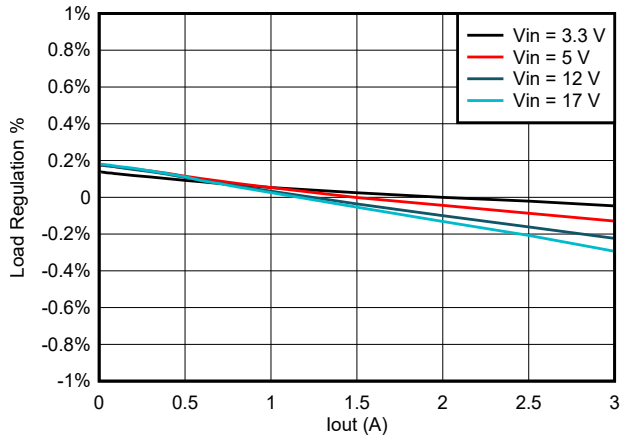

図 8-2. TPSM863252 Load Regulation vs Loading

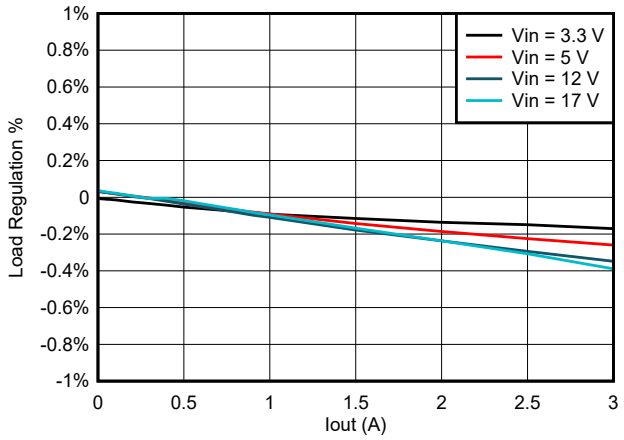

図 8-3. TPSM863257 Load Regulation vs Loading

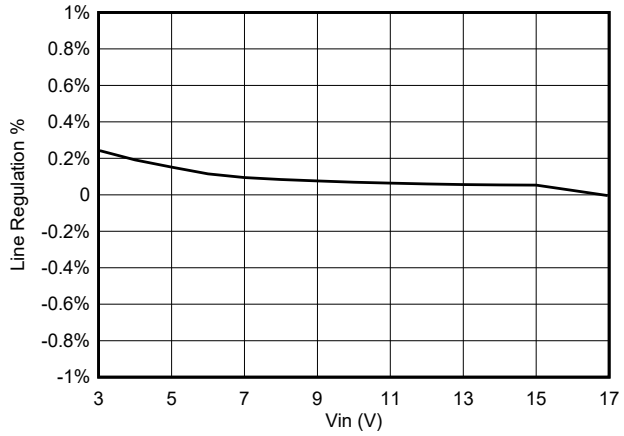

図 8-4. TPSM863252 Line Regulation vs V_{IN} at 3A Loading

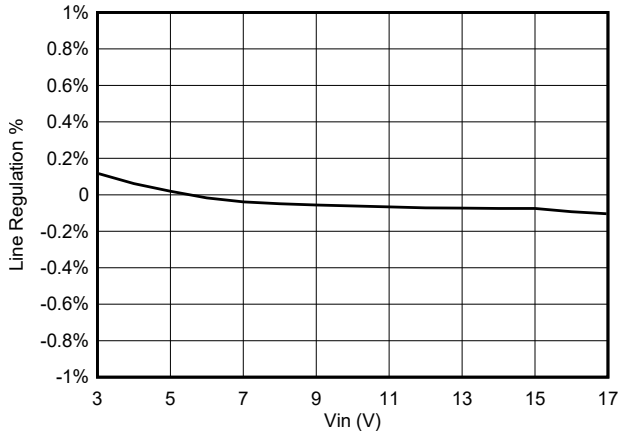

図 8-5. TPSM863257 Line Regulation vs V_{IN} at 3A Loading

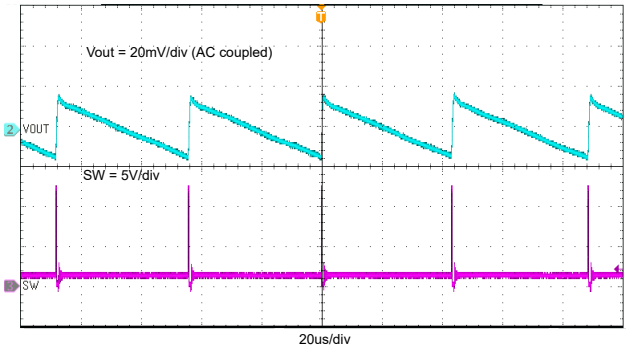

図 8-6. TPSM863252 Output Voltage Ripple With 0.01A Loading

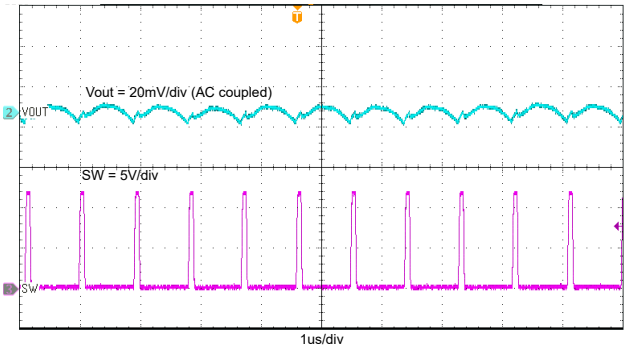

図 8-7. TPSM863257 Output Voltage Ripple With 0.01A Loading

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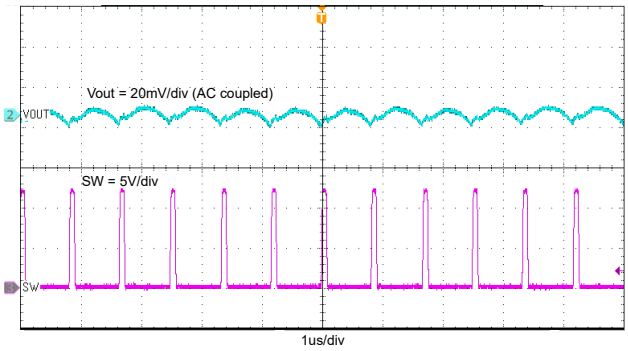

図 8-8. TPSM86325x Output Voltage Ripple With 3A Loading

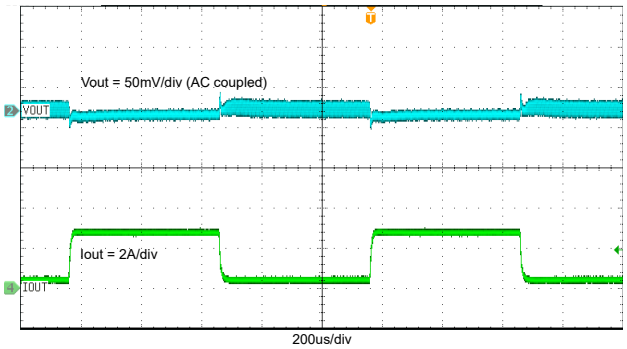

図 8-9. TPSM863252 Transient Response With 0.3A to 2.7A

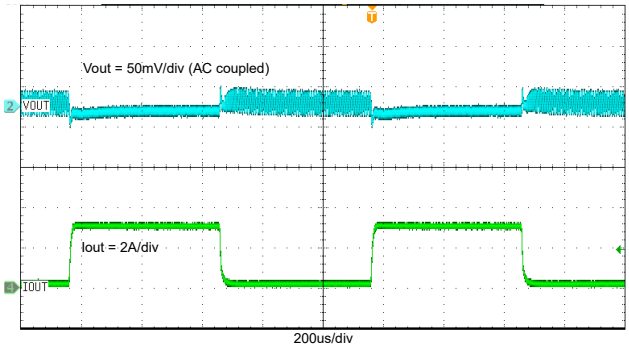

図 8-10. TPSM863252 Transient Response With 0.1A to 3A

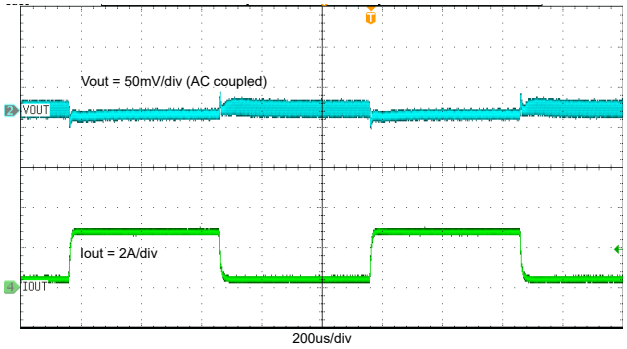

図 8-11. TPSM863257 Transient Response With 0.3A to 2.7A

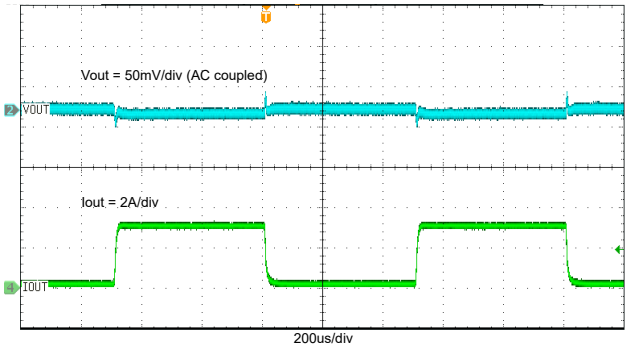

図 8-12. TPSM863257 Transient Response With 0.1A to 3A

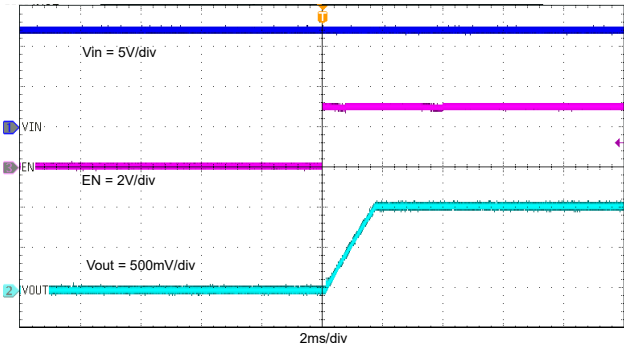

図 8-13. Start-Up Through EN, I_{OUT} = 3A

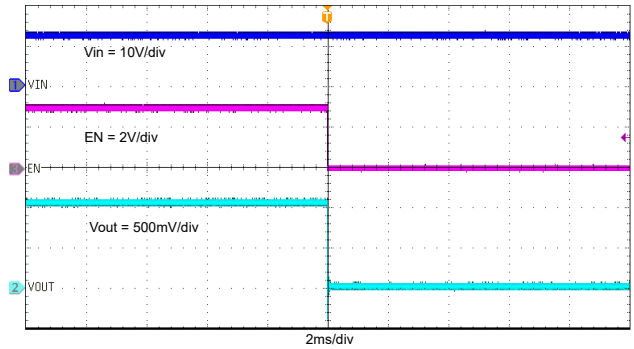

図 8-14. Shutdown Through EN, I_{OUT} = 3A

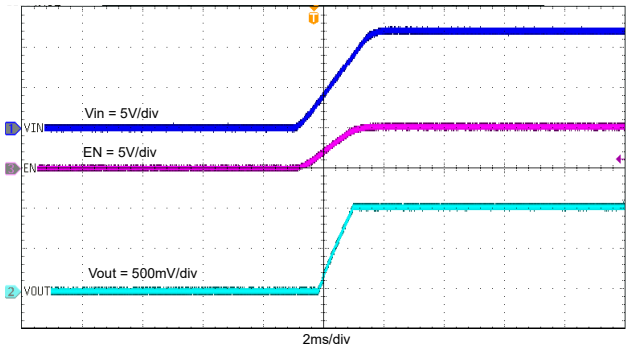

図 8-15. Start-Up with V_{IN} Rising, I_{OUT} = 3A

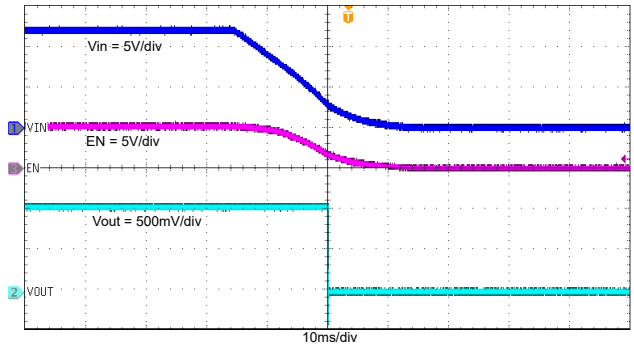

図 8-16. Shutdown with V_{IN} Falling, I_{OUT} = 3A

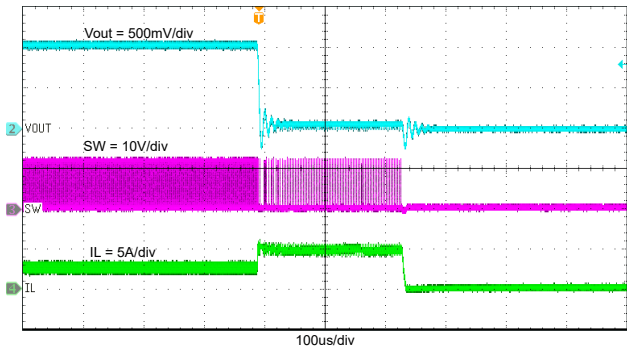

図 8-17. TPSM863252 Normal Operation to Output Hard Short

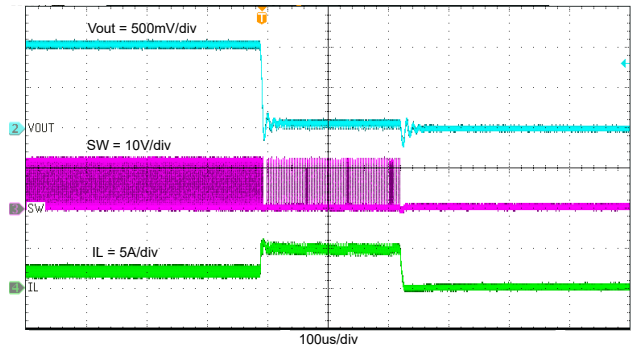

図 8-18. TPSM863257 Normal Operation to Output Hard Short

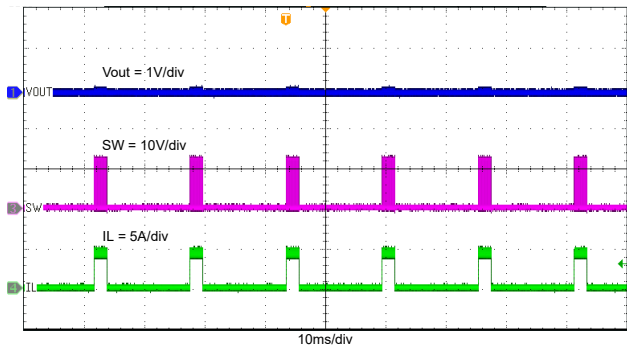

図 8-19. Output Hard Short Hiccup

8.3 Power Supply Recommendations

The TPSM86325x are designed to operate from input supply voltages in the range of 3V to 17V. Buck converters require the input voltage be higher than the output voltage for proper operation.

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8.4 Layout

8.4.1 Layout Guidelines

- Make sure the VIN and GND traces are as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Connect a separate VOUT path to the upper feedback resistor.
- Place a voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
- Make sure the trace of the FB node is as small as possible to avoid noise coupling.
- Make sure the GND trace between the output capacitor and the GND pin are as wide as possible to minimize the trace impedance.

8.4.2 Layout Example

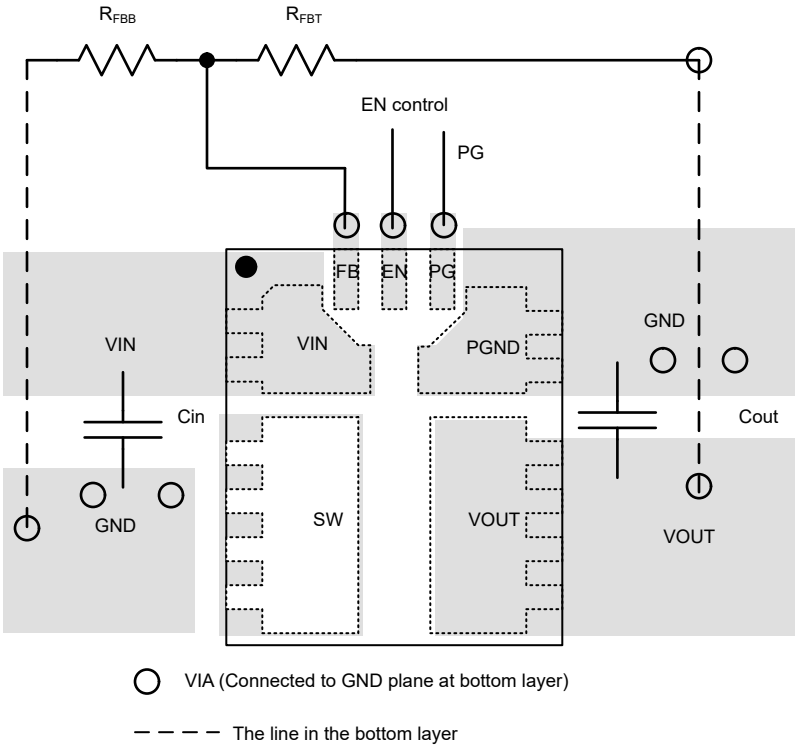

図 8-20. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPSM863252 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPSM863253 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPSM863257 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2023) to Revision C (January 2024) **Page**

- TPSM863253 のステータスを「事前情報」から「量産データ」に変更。「TPSM863253 の固定 3.3V 出力電圧」を追加。TPSM863253 モードの説明を追加。ドキュメント全体にわたって WEBENCH のリンクを追加 1
- 「概要」に TPSM863253 の情報を追加 1
- Updated the *Family Devices* table 3
- Added TPSM863253 efficiency figure. 8
- Added TPSM863253 mode introduction. 14

Changes from Revision A (June 2023) to Revision B (September 2023) **Page**

- ドキュメントに TPSM863253 を追加 1

Changes from Revision * (March 2023) to Revision A (June 2023) **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM863252RDXR	Active	Production	QFN-FCMOD (RDX) | 7	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	863252
TPSM863252RDXR.A	Active	Production	QFN-FCMOD (RDX) | 7	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	863252
TPSM863253RDXR	Active	Production	QFN-FCMOD (RDX) | 7	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	863253
TPSM863253RDXR.A	Active	Production	QFN-FCMOD (RDX) | 7	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	863253
TPSM863257RDXR	Active	Production	QFN-FCMOD (RDX) | 7	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	863257
TPSM863257RDXR.A	Active	Production	QFN-FCMOD (RDX) | 7	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	863257

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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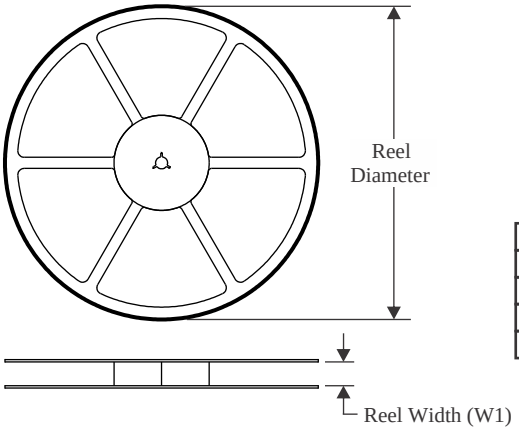
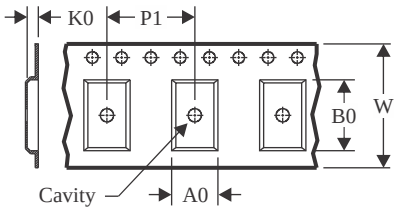
TAPE AND REEL INFORMATION

REEL DIMENSIONS

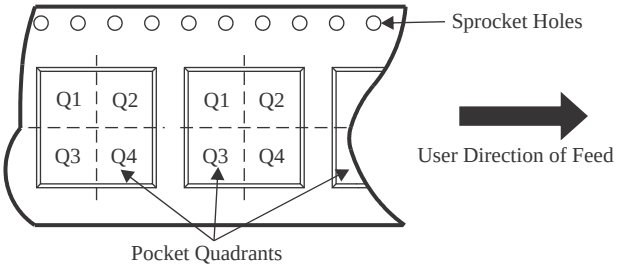


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

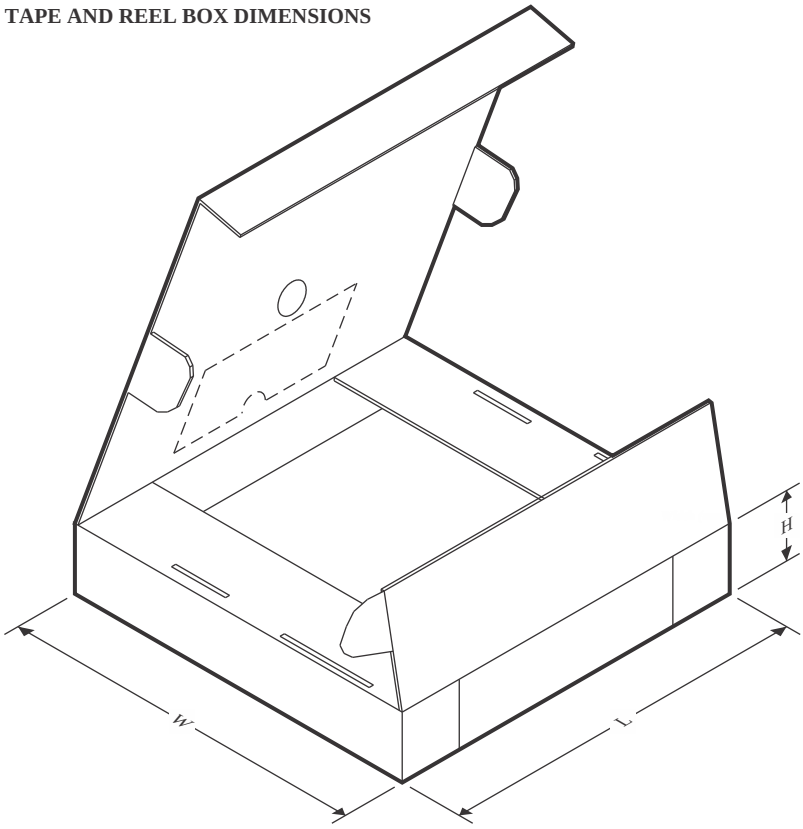
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

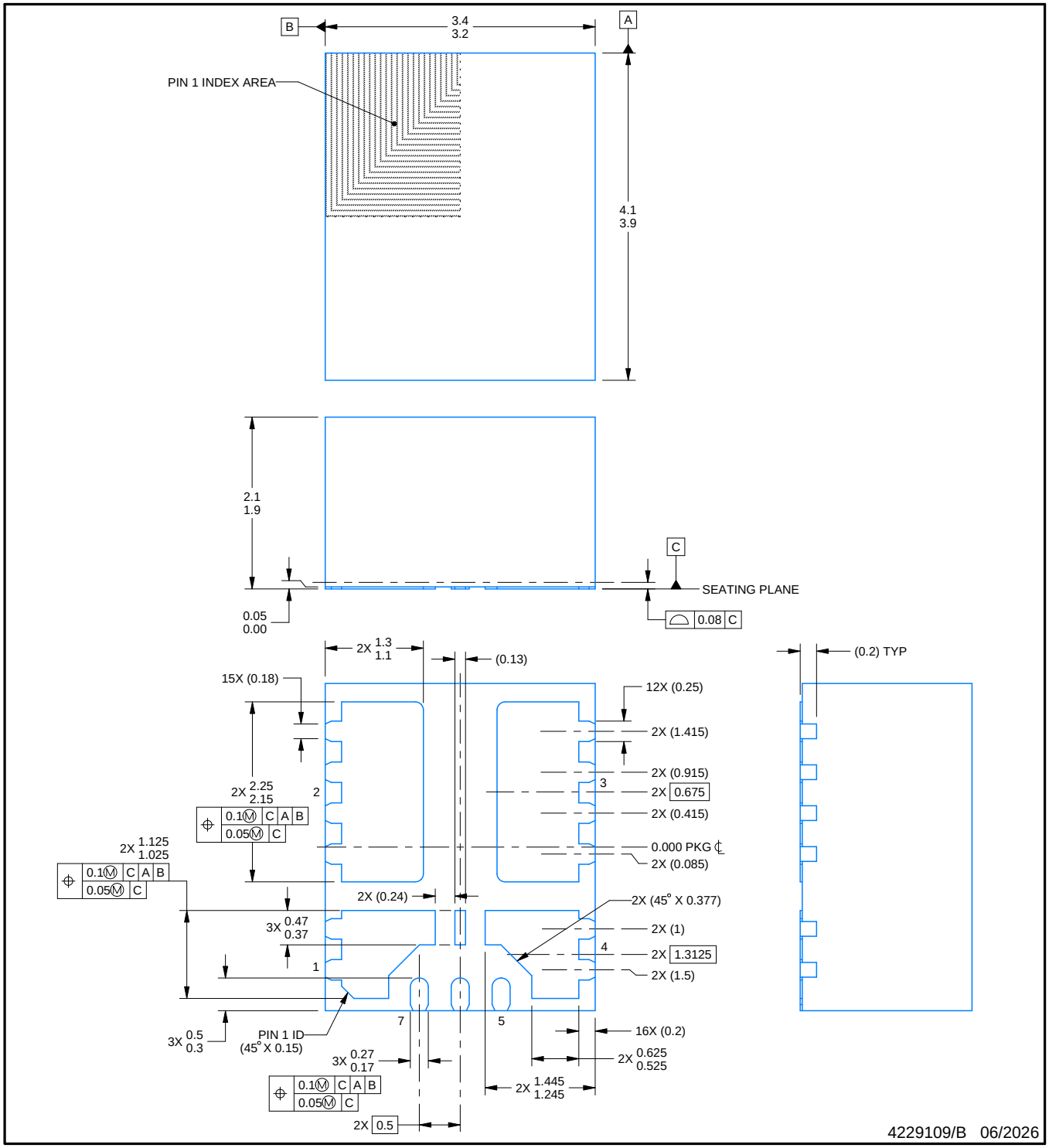
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM863252RDXR	QFN-FCMOD	RDX	7	3000	330.0	17.6	3.6	4.3	2.25	8.0	12.0	Q1
TPSM863253RDXR	QFN-FCMOD	RDX	7	3000	330.0	12.4	3.6	4.3	2.3	8.0	12.0	Q1
TPSM863257RDXR	QFN-FCMOD	RDX	7	3000	330.0	17.6	3.6	4.3	2.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



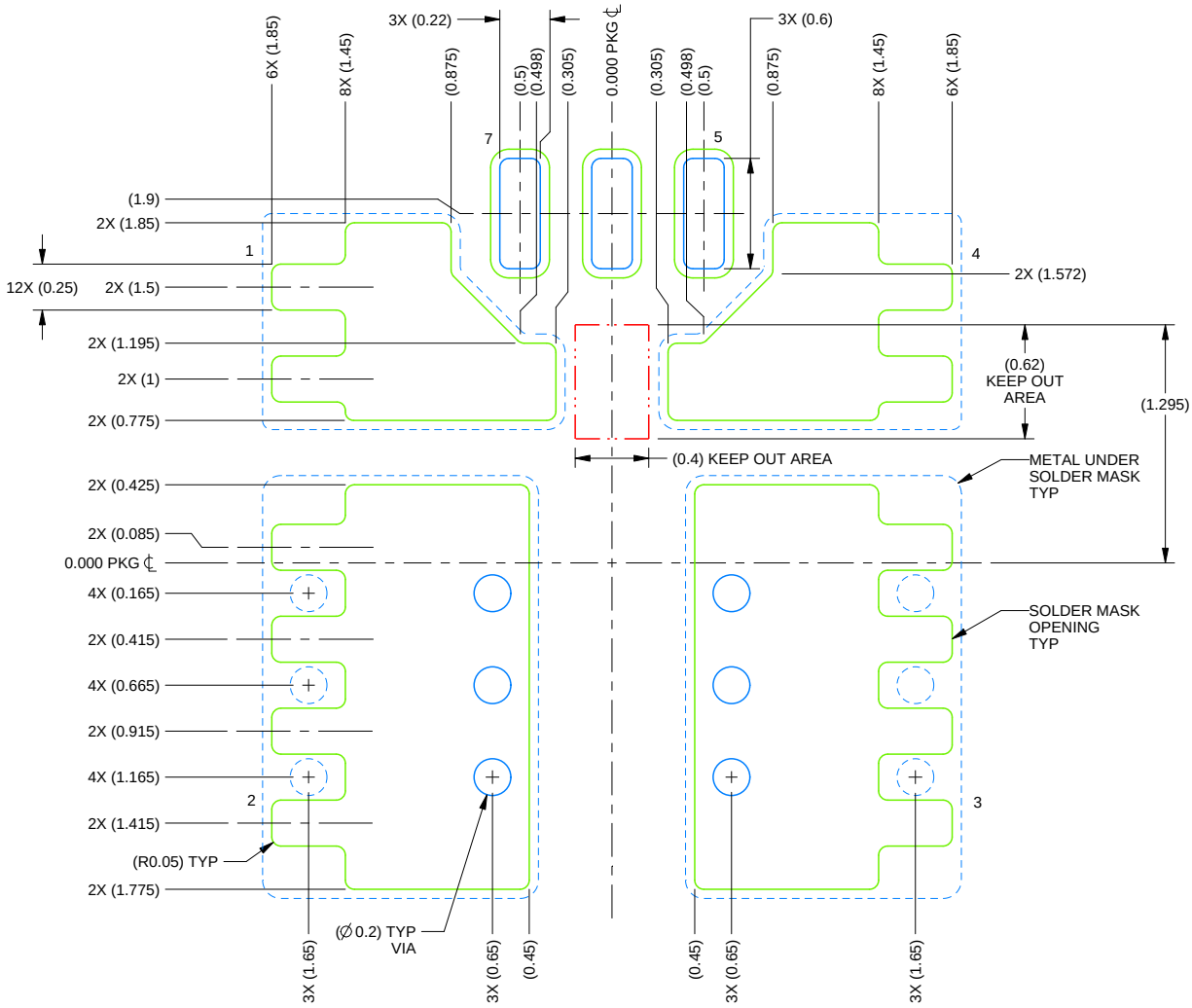
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM863252RDXR	QFN-FCMOD	RDX	7	3000	336.0	336.0	48.0
TPSM863253RDXR	QFN-FCMOD	RDX	7	3000	367.0	367.0	38.0
TPSM863257RDXR	QFN-FCMOD	RDX	7	3000	336.0	336.0	48.0

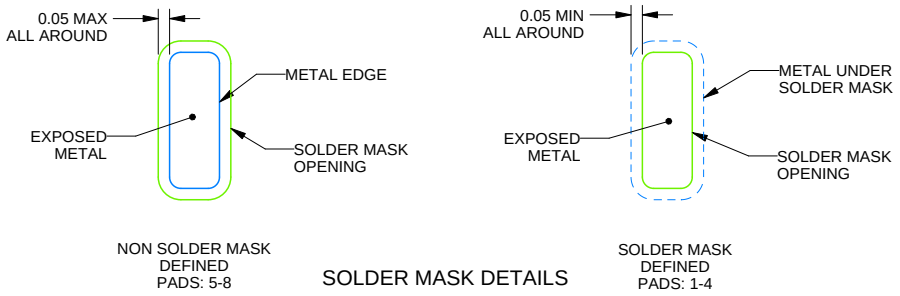


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 25X



SOLDER MASK DETAILS

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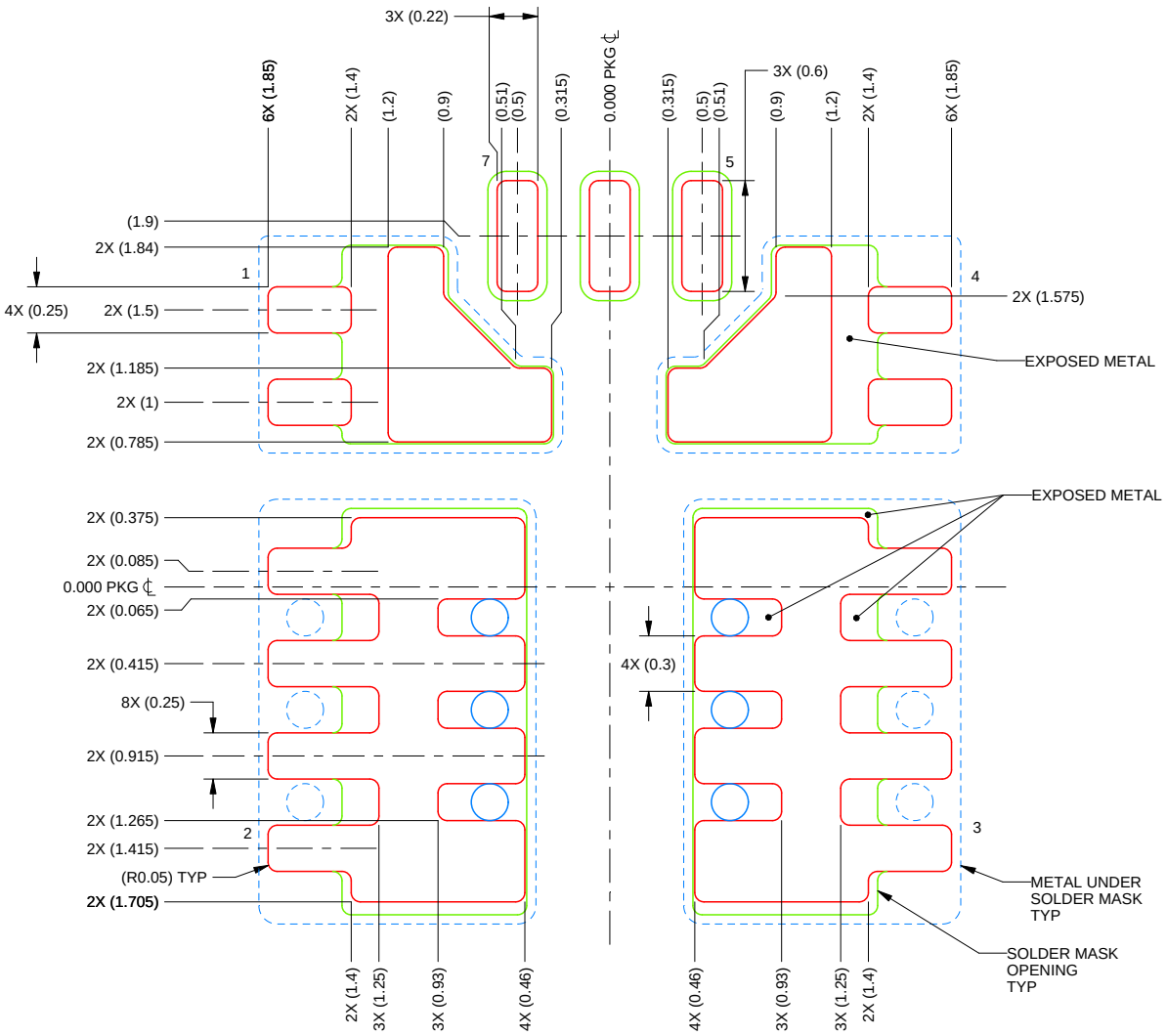
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS: 1, 2, 3 & 4: 75%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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