TRS3221E ±15kV IEC ESD 保護機能搭載、小型パッケージの 3V～5.5V シングル チャネル RS-232 ライン ドライバ / レシーバ

1 特長

- RS-232 ピンの ESD 保護
  - ±15kV 人体モデル (HBM)
  - ±8kV (IEC 61000-4-2、接触放電)
  - ±15kV (IEC 61000-4-2、エアギャップ放電)
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V～5.5V の V_{CC} 電源で動作
- 最大 250kbit/s で動作
- 1 つのドライバと 1 つのレシーバ
- ニア チップスケール パッケージ、16 ピン VQFN (RGT、TSSOP パッケージより 82% 小型)
- 小さいスタンバイ電流:1µA (標準値)
- 外付けコンデンサ:4 × 0.1µF
- 3.3V 電源で 5V ロジック入力を許容
- 代替の高速ピン互換デバイス (1Mbit/s)
  - TRSF3221E
- 自動パワー ダウン機能により、ドライバを自動的にディセーブルすることで電力を節約

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリ駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

3 概要

TRS3221E は、1 つの V_{CC} 電源で動作するシングル ドライバ / シングル レシーバ RS-232 ソリューションです。RS-232 ピンは、IEC G1000-4-2 ESD 保護に対応しています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート コネクタの間の電気的インターフェイスとして機能します。チャージ ポンプと 4 つの小さな外付けコンデンサにより、3V～5.5V の単一電源で動作できます。本デバイスは最大 250kbit/s のデータ信号速度、最大 30V/µs のドライバ出力スルーレートで動作します。

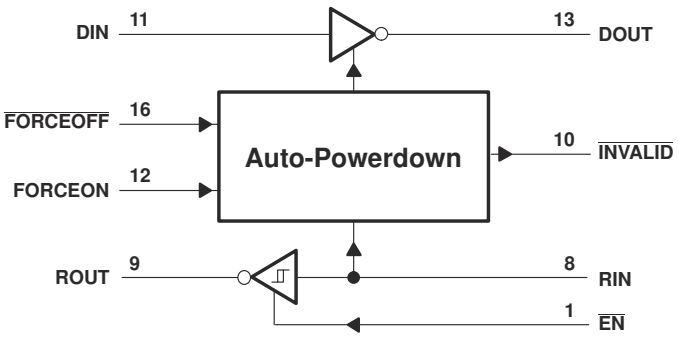
シリアル ポートが使われていない際のパワー マネージメントを柔軟に制御できます。FORCEON が LOW かつ $\overline{\text{FORCEOFF}}$ が HIGH の場合、自動パワー ダウン機能が動作します。この動作モード中、デバイスがレシーバ入力で有効な RS-232 信号を検出しない場合、ドライバ出力はディスエーブルになります。$\overline{\text{FORCEOFF}}$ を LOW に設定しかつ $\overline{\text{EN}}$ を HIGH に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1µA に減少します。シリアル ポートを切り離した場合、またはペリフェラル ドライバをオフにした場合、自動パワー ダウン状態になります。FORCEON と $\overline{\text{FORCEOFF}}$ を HIGH にすると、自動パワー ダウンを無効にできます。

自動パワー ダウンが有効な場合、レシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。$\overline{\text{INVALID}}$ 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知します。$\overline{\text{INVALID}}$ は、レシーバの入力電圧が 2.7V を上回っている、または −2.7V を下回っている、あるいは −0.3V と 0.3V の間にあった期間が 30µs 未満である場合、HIGH (有効データ) になります。$\overline{\text{INVALID}}$ は、レシーバの入力電圧が 30µs を超えて −0.3V と 0.3V の間にある場合、LOW (無効データ) になります。レシーバの入力レベルについては、図 6-5 を参照してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TRS3221E	SSOP (DB) (16)	6.2 mm × 5.3mm
	TSSOP (PW) (16)	5mm × 4.4mm
	VQFN (RGT) (16)	3 mm × 3mm
	SOT-23-THN (DYY) (16)	4.2mm × 2mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

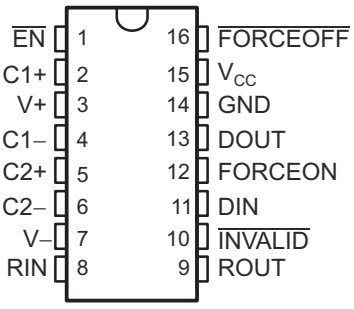

図 4-1. 16-Pin SSOP (DB) or TSSOP (PW) Packages, Top View

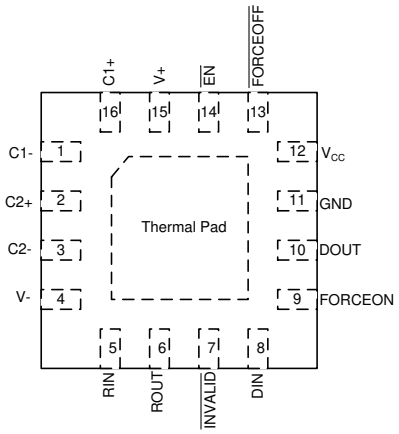

図 4-2. 16-pin VQFN (RGT) Package, Top View

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DB or PW	RGT		
C1+	2	16	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2+	5	2	—	
C1–	4	1	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2–	6	3	—	
DIN	11	8	I	Driver input
DOUT	13	10	O	RS-232 driver output
$\overline{EN}$	1	14	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
$\overline{FORCEOFF}$	16	13	I	Automatic power-down control input
FORCEON	12	9	I	Automatic power-down control input
GND	14	11	GND	Ground
$\overline{INVALID}$	10	7	O	Invalid output pin. Output is low when all RIN inputs are unpowered.
RIN	8	5	I	RS-232 receiver input
ROUT	9	6	O	Receiver output
V_{CC}	15	12	—	3V to 5.5V supply voltage
V+	3	15	O	5.5V supply generated by the charge pump
V–	7	4	O	–5.5V supply generated by the charge pump
Thermal Pad	None	Thermal Pad	-	Exposed thermal pad. Can be connected to GND or left floating.

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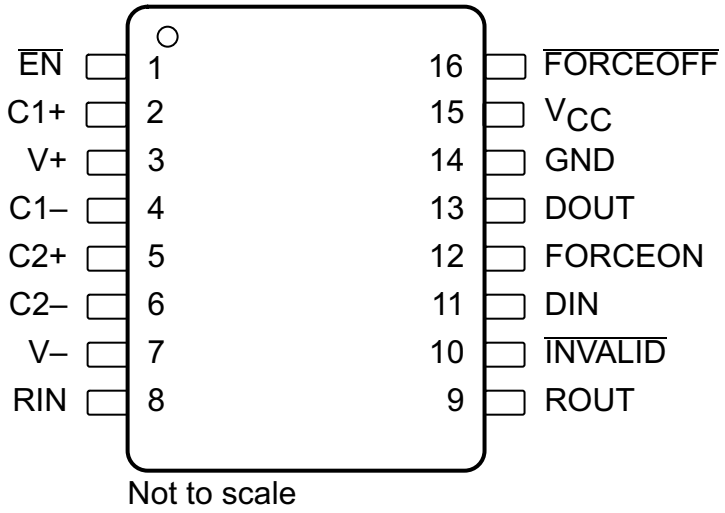

図 4-3. DYY Package
16-Pin SOT-23-THN
(Top View)

表 4-2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
C2+	5		
C1–	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2–	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
$\overline{EN}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
$\overline{FORCEOFF}$	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
$\overline{INVALID}$	10	O	Invalid output pin. Output low when RIN input is unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V_{CC}	15	—	3V to 5.5V supply voltage
V+	3	O	5.5V supply generated by the charge pump
V–	7	O	–5.5V supply generated by the charge pump

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	–0.3	6	V
		RIN	–25	25	
V_O	Output voltage range	DOUT	–13.2	13.2	V
		ROUT, $\overline{\text{INVALID}}$	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except RIN and DOUT	±3000	V
			RIN and DOUT pins (RS232 ports)	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings, IEC Specifications

NAME	TEST CONDITIONS	VALUE	UNIT
R_{IN}, D_{OUT} (2)	IEC 61000-4-2 Contact Discharge (1) (2)	±8000	V
	IEC 61000-4-2 Air-Gap Discharge (1) (2)	±15000	

(1) A minimum of 1-µF capacitor is required between VCC and GND to meet the specified IEC ESD level
(2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

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5.4 Recommended Operating Conditions

See 図 8-1, and note (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	TRS3221EC		0		70	°C
		TRS3221EI		–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.5 Thermal Information

THERMAL METRIC(1)		TRS3221E				UNIT
		DB (SSOP)	PW (TSSOP)	RGT (VQFN)	DYY (SOT-23-THN)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	110.9	52.1	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	41.7	60.6	56.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	57.2	26.8	51.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	4.2	2.5	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.8	56.6	26.8	50.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	12.0	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER			TEST CONDITIONS(2)		MIN	TYP(1)	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				±0.01	±1	µA
I_{CC}	Supply current	Auto-powerdown disabled	V_{CC} = 3.3 V or 5 V, T_A = 25°C	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off		No load, $\overline{FORCEOFF}$ at GND		1	10	µA
		Auto-powerdown enabled		No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

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5.7 Driver Section Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER		TEST CONDITIONS(3)			MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND		5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}		–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}				±0.01	±1	μA
I_{IL}	Low-level input current	V_I = GND				±0.01	±1	μA
I_{OS}	Short-circuit output current(2)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V			±35	±60	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12 V,	V_{CC} = 3 V to 3.6 V			±25	μA
			V_O = ±10 V,	V_{CC} = 4.5 V to 5.5 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

5.8 Driver Section Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER		TEST CONDITIONS(3)			MIN	TYP(1)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF,	R_L = 3 kΩ, See 図 6-1	RGT package	250	500		kbit/s
				DB or PW package	150	250		
$t_{sk(p)}$	Pulse skew(2)	C_L = 1000 pF,	R_L = 3 kΩ 図 6-2	RGT package		50		ns
		C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See 図 6-2	DB or PW package		100		
SR(tr)	Slew rate, transition region (see 図 6-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF		6		30	V/μs
			C_L = 150 pF to 2500 pF		4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

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5.9 Receiver Section Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.5		V
I_{off}	Output leakage current	$\overline{EN}$ = V_{CC}		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.10 Receiver Section Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-1)

PARAMETER		TEST CONDITIONS(3)		TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 6-3	RGT package	100	ns
			DB or PW package	150	
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See 図 6-3	RGT package	125	ns
			DB or PW package	150	
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 6-4		200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See 図 6-4		200	ns
$t_{sk(p)}$	Pulse skew(2)	See 図 6-3	RGT package	25	ns
			DB or PW package	50	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

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5.11 Auto-Powerdown Section Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 6-5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T–(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for I $\overline{NVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = –1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

5.12 Auto-Powerdown Section Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 6-5)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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5.13 Typical Characteristics

V_{CC} = 3.3 V and T_A = 25 °C unless specified otherwise.

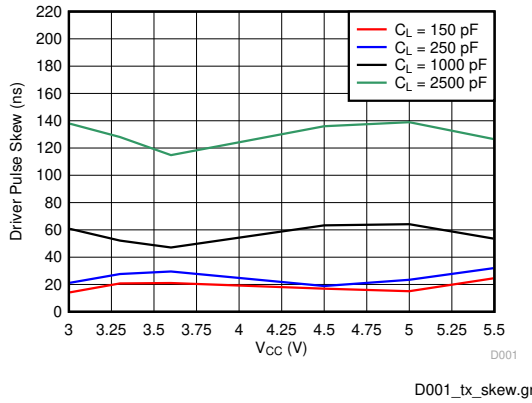

図 5-1. Driver Pulse Skew vs Load Capacitance and Supply Voltage at T_A = 25 °C (RGT Package)

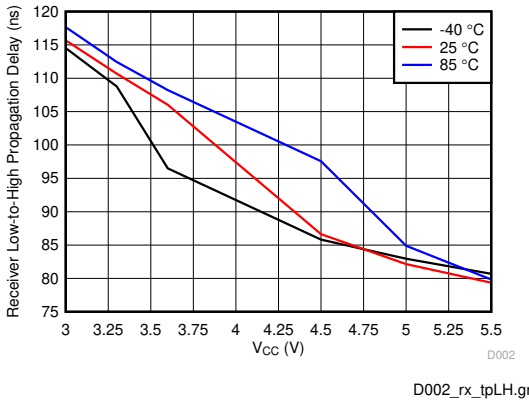

図 5-2. Receiver Path Low-to-High Propagation Delay vs T_A and Supply Voltage (RGT Package)

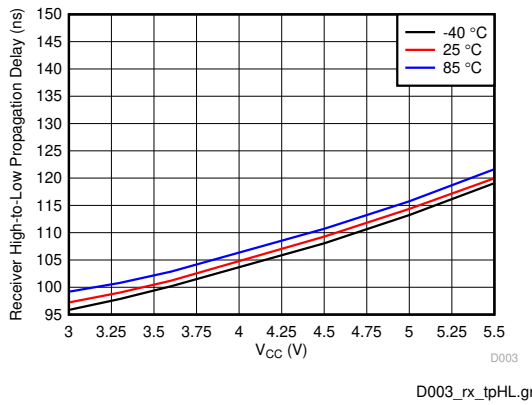

図 5-3. Receiver Path High-to-Low Propagation Delay vs T_A and Supply Voltage (RGT Package)

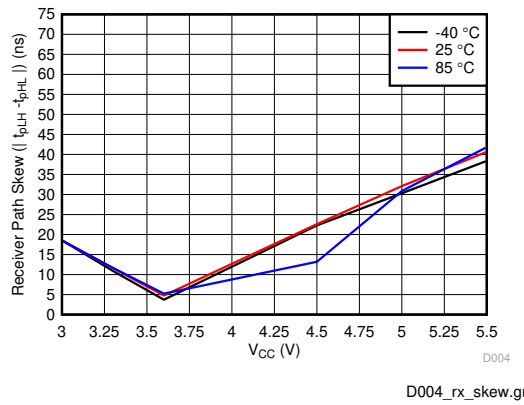

図 5-4. Receiver Pulse Skew ($|t_{pLH} - t_{pHL}|$) vs T_A and Supply Voltage (RGT Package)

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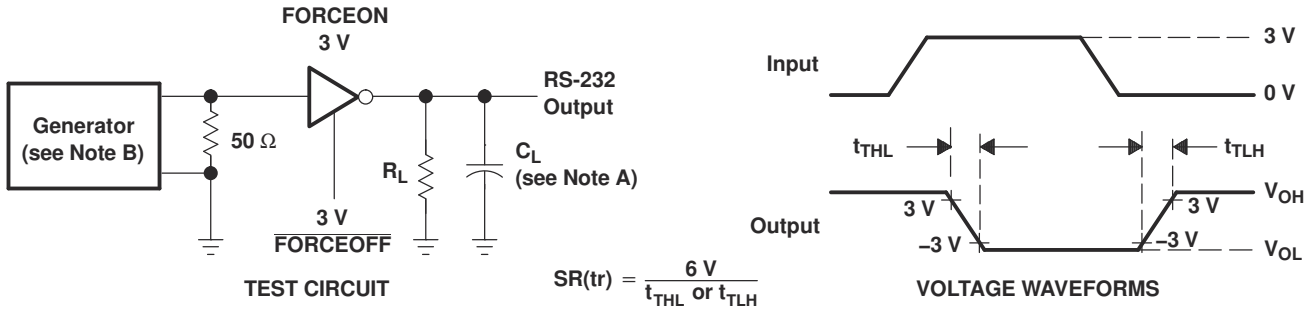
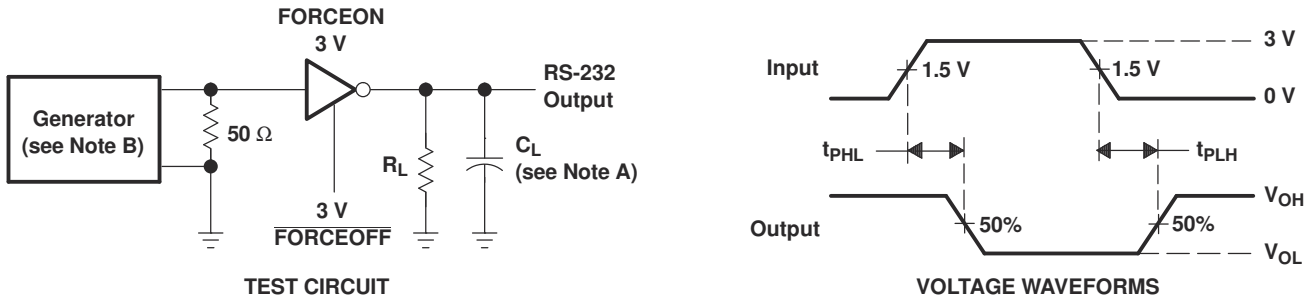
6 Parameter Measurement Information



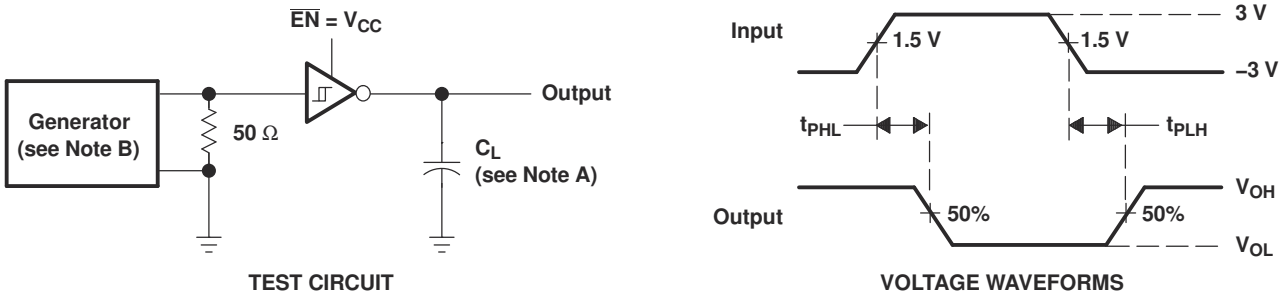
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-3. Receiver Propagation Delay Times

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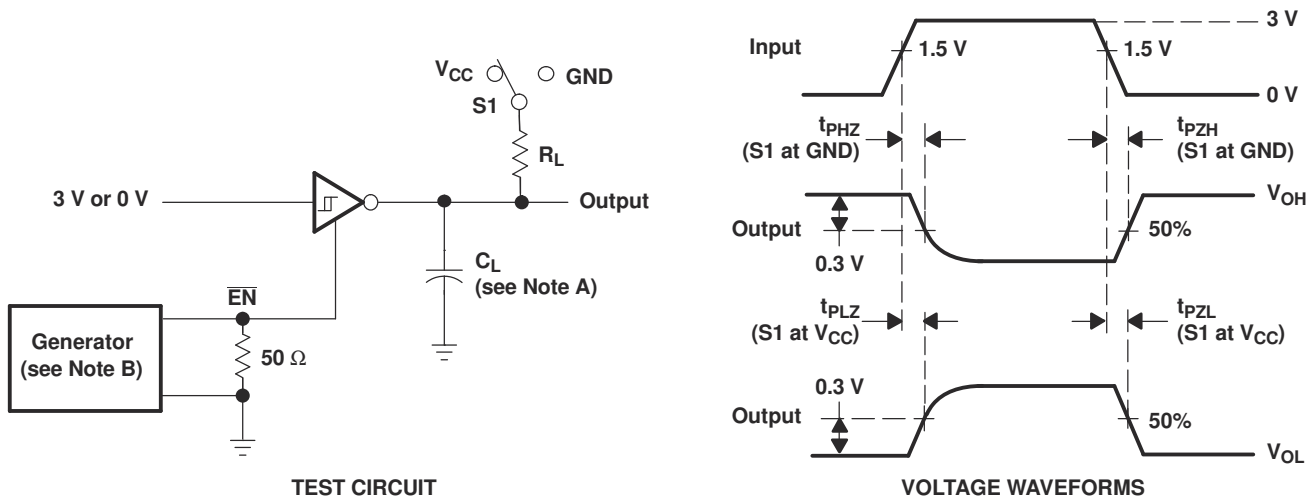

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

図 6-4. Receiver Enable and Disable Times

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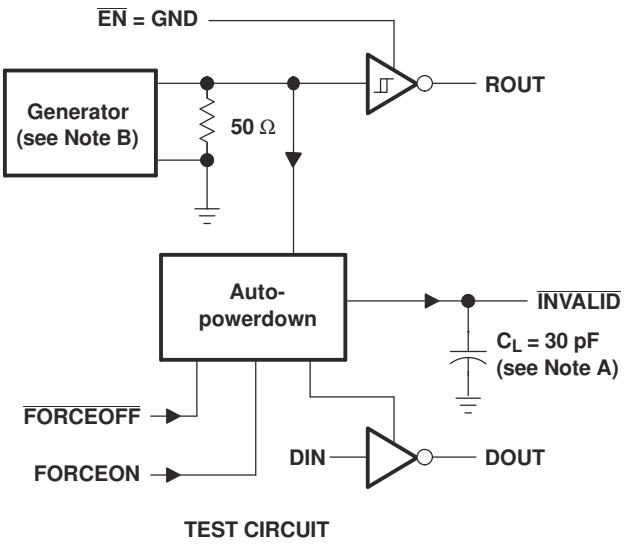
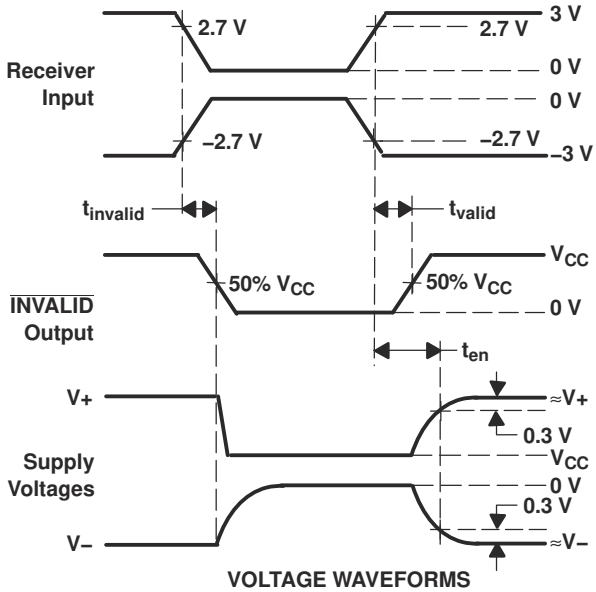
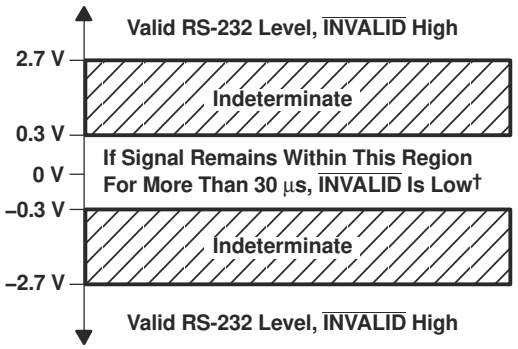


TEST CIRCUIT



VOLTAGE WAVEFORMS



† Auto-powerdown disables drivers and reduces supply current to 1 µA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

図 6-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

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7 Detailed Description

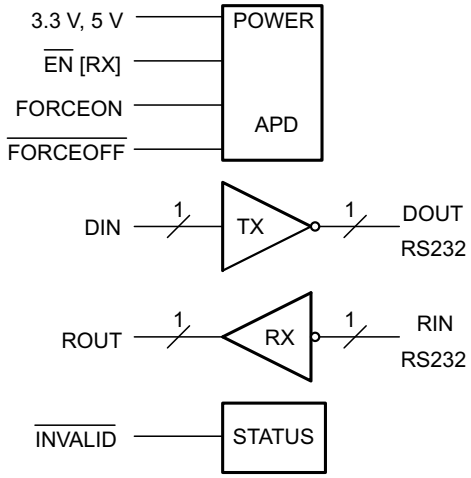
7.1 Overview

The TRS3221E device is a one-driver and one-receiver RS-232 interface device. The RS-232 input and output are protected up to ±15kV using the Human-Body Model. The charge pump requires only four small 0.1µF capacitors for operation from a 3.3V supply. The TRS3221E device is capable of running at data rates up to 250kbps while maintaining RS-232-compliant output levels.

Automatic power down can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With automatic power down plus enabled, the device activates automatically when a valid signal is applied to any receiver input. The device can automatically power down the driver to save power when the RIN input is unpowered.

$\overline{\text{INVALID}}$ is high (valid data) if receiver input voltage is greater than 2.7V or less than –2.7V, or has been between –0.3V and 0.3V for less than 30µs. $\overline{\text{INVALID}}$ is low (invalid data) if receiver input voltages are between –0.3V and 0.3V for more than 30µs. Refer to 図 6-5 for receiver input levels.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors. The automatic power-down feature for the driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. The receiver is controlled by the $\overline{\text{EN}}$ input (see 表 7-1 and 表 7-2).

When the device is unpowered, it can be safely connected to an active remote RS232 device.

7.3.2 RS232 Driver

One driver interfaces standard logic level to RS232 levels. DIN input must be valid high or low.

7.3.3 RS232 Receiver

One receiver interfaces RS232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

7.3.4 RS232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30 µs. The $\overline{\text{INVALID}}$ output goes high when the receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{cc} is powered regardless of FORCEON and $\overline{\text{FORCEOFF}}$ inputs (see 表 7-3).

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7.4 Device Functional Modes

表 7-1. Driver

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with automatic power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by automatic power-down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, Yes = |RIN| > 2.7 V, No = |RIN| < 0.3 V

表 7-2. Receiver

INPUTS(1)			OUTPUT	RECEIVER STATUS
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	ROUT	
X	H	X	Z	Output off
L	L	X	H	Normal operation
H	L	X	L	
Open	L	No	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 7-3. $\overline{\text{INVALID}}$

INPUTS(1)				OUTPUT
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{EN}}$	$\overline{\text{INVALID}}$
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

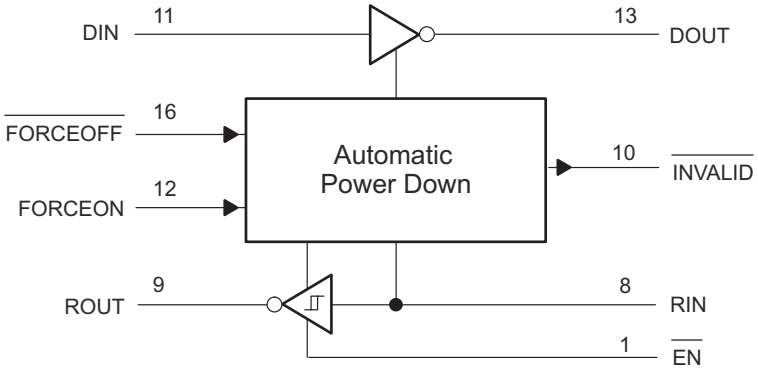

図 7-1. Logic Diagram

8 Application Information Disclaimer

注

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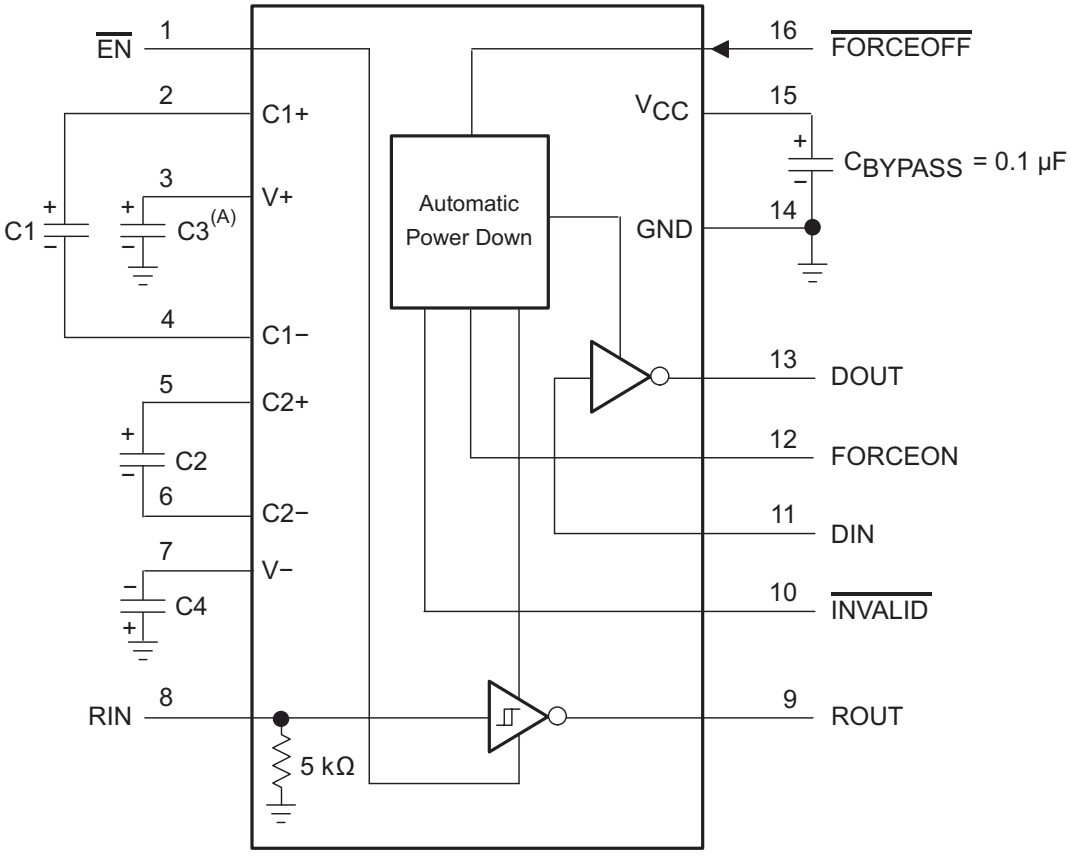
8.1 Application Information

The TRS3221E device is designed to convert single-ended signals into RS232-compatible signals, and RS232-compatible signals into single-ended signals.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector

8.2 Typical Application



A. C3 can be connected to V_{CC} or GND.
B. Resistor values shown are nominal.
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.
D. See 表 8-1 for capacitor values.

図 8-1. Typical Operating Circuit and Capacitor Values

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8.3 Design Requirements

- Recommended V_{CC} is 3.3V or 5V
  - 3V to 5.5V is also possible
  - Maximum recommended bit rate is 250kbps
  - Use capacitors as shown in 図 8-1 and 表 8-1

表 8-1. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3V ± 0.3V	0.1µF	0.1µF
5V ± 0.5V	0.047µF	0.33µF
3V to 5.5V	0.1µF	0.47µF

8.4 Detailed Design Procedure

For proper operation, add capacitors as shown in 図 8-1 and 表 8-1.

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on V_{CC} level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC}. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

8.5 Application Curve

V_{CC} of 3.3V and 250kbps alternative bit data stream

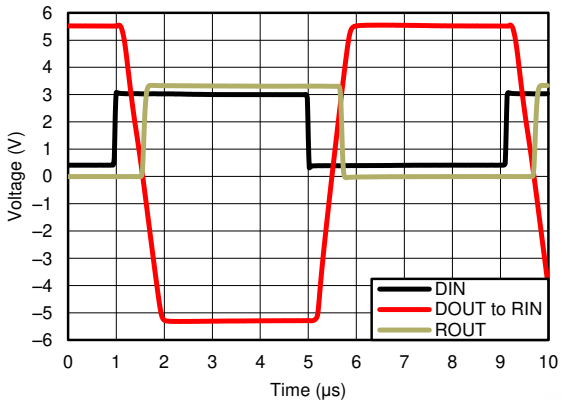

図 8-2. 250kbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3V

Power Supply Recommendations

V_{CC} must be between 3V and 5.5V. Charge pump capacitors must be chosen using 表 8-1.

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8.6 Layout

8.6.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

8.6.2 Layout Example

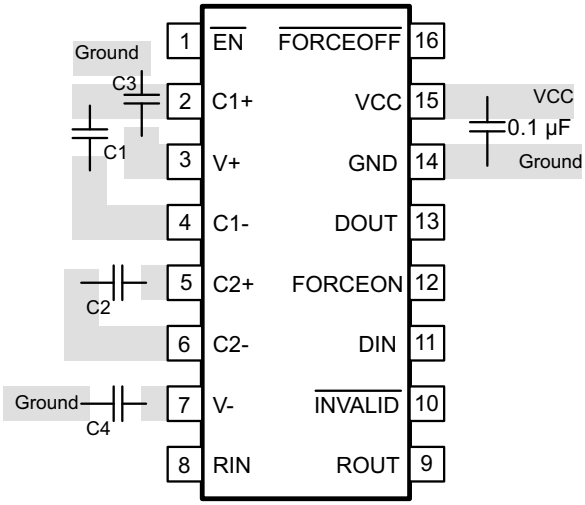

図 8-3. Layout Diagram

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2021) to Revision C (December 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更	1
• データシートに SOT-23-THN (DYY) パッケージを追加	1
• Added Note 2 to the *ESD Ratings, IEC Specifications*	5

Changes from Revision A (December 2020) to Revision B (July 2021)	Page
• *「アプリケーション」*の一覧を変更	1
• Changed the table note for the *ESD Ratings, IEC Specifications* to make it applicable to all packages	5
• Changed the thermal information for PW and DB packages	6

Changes from Revision * (June 2007) to Revision A (December 2020)	Page
• 「ESD 定格」、「IEC 仕様」表、「熱に関する情報」表、「代表的特性」セクション、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

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- 「注文情報」表を削除。 1
- Added the RGT (VQFN-16) package pinout 3
- Added data rate and $t_{sk(p)}$ rows for the RGT package in *Driver Section Switching Characteristics* table 7
- Added t_{pLH}, t_{pHL}, $t_{sk(p)}$ rows for the RGT package in *Reciever Section Switching Characteristics* table 8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3221ECDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS21EC
TRS3221ECDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS21EC
TRS3221ECPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	RS21EC
TRS3221ECPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS21EC
TRS3221ECPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EC
TRS3221ECPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EC
TRS3221EIDB	Obsolete	Production	SSOP (DB) | 16	-	-	Call TI	Call TI	-40 to 85	RS21EI
TRS3221EIDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIDYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIDYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI
TRS3221EIRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3221
TRS3221EIRGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3221

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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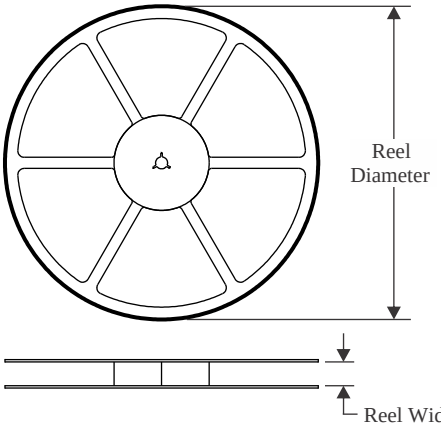
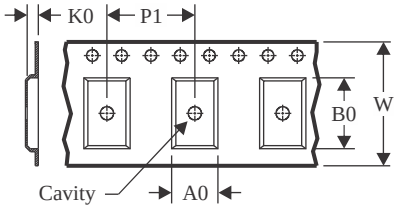
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

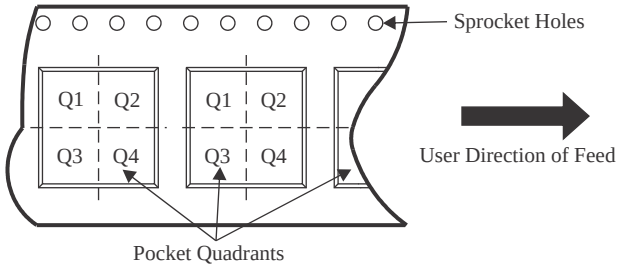


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

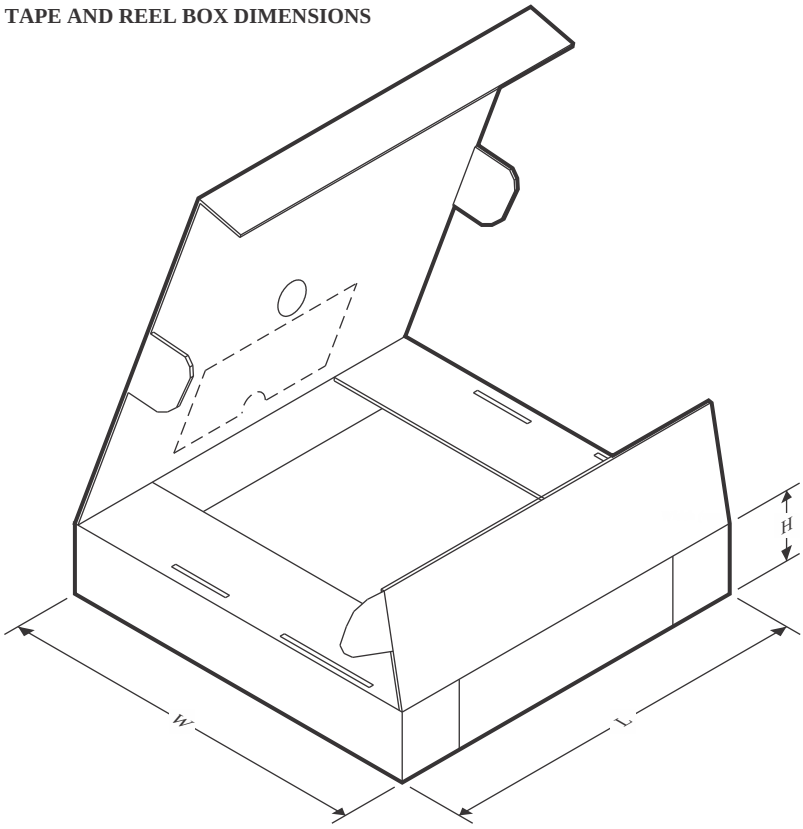
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
TRS3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3221EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TRS3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
TRS3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

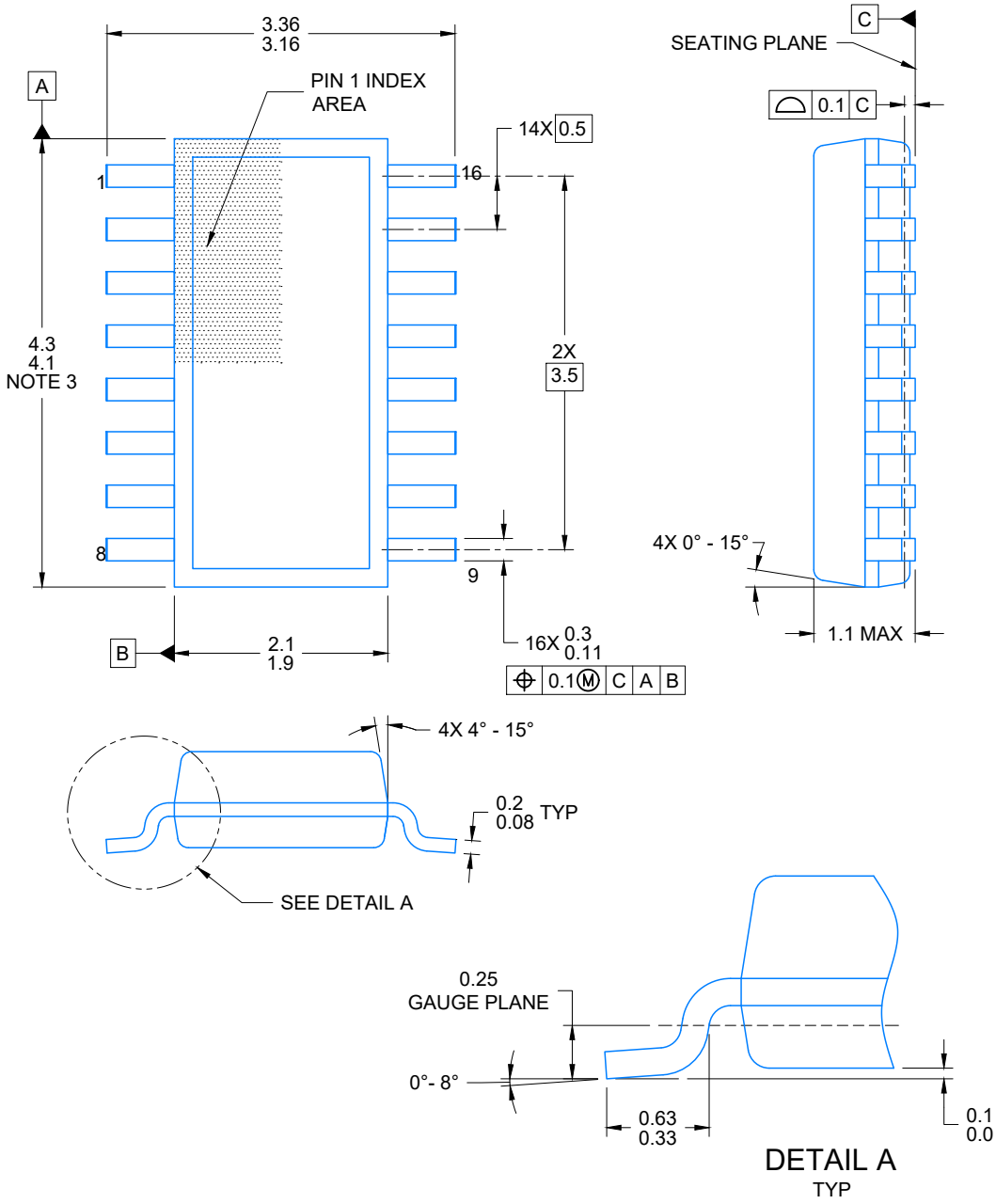
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3221ECDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRS3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3221ECPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TRS3221ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3221EIDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRS3221EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TRS3221EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TRS3221EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3221EIPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
TRS3221EIRGTR	VQFN	RGT	16	3000	360.0	360.0	36.0

PACKAGE OUTLINE

DYY0016A

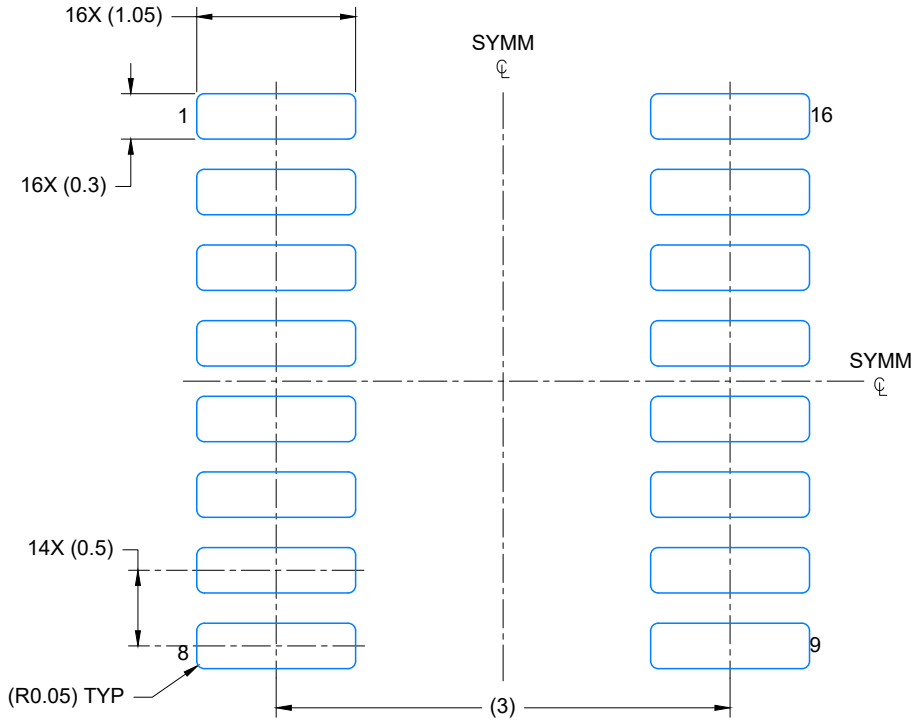
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

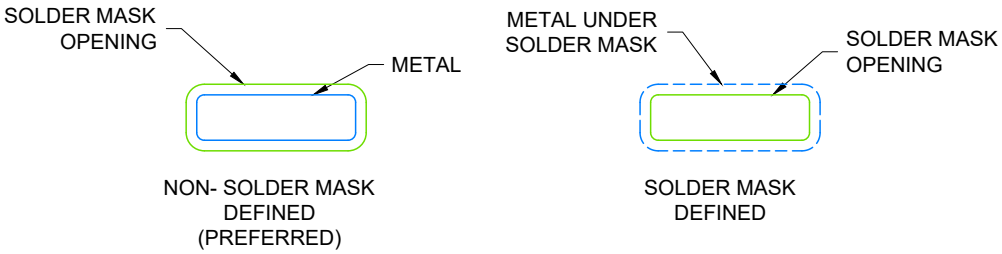


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

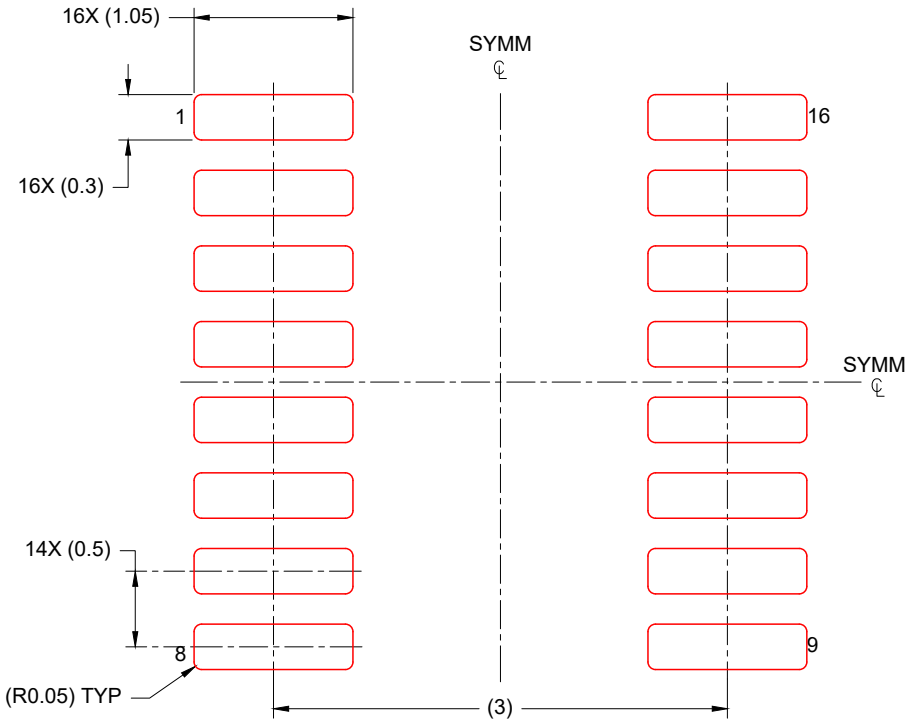
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

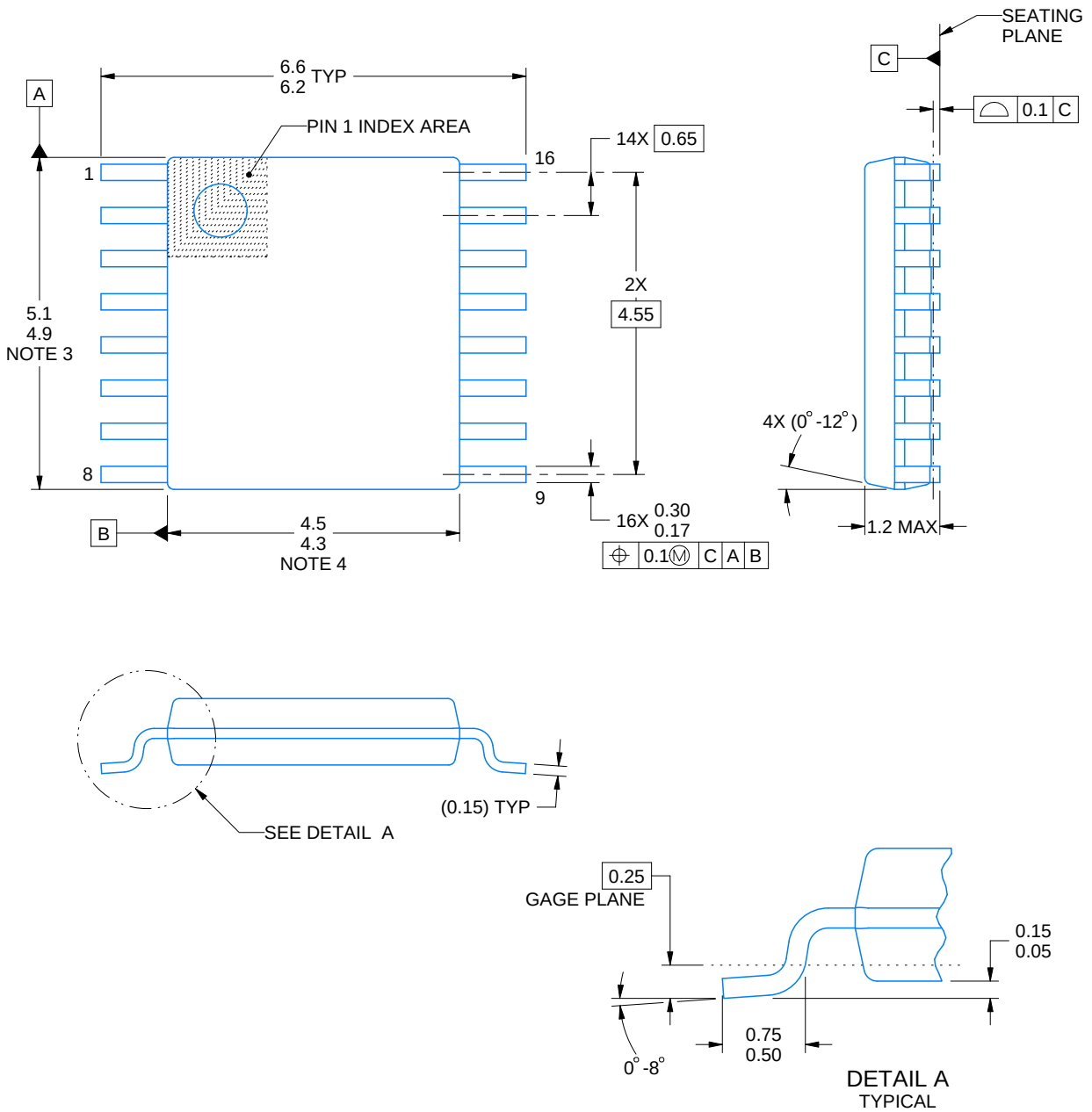
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

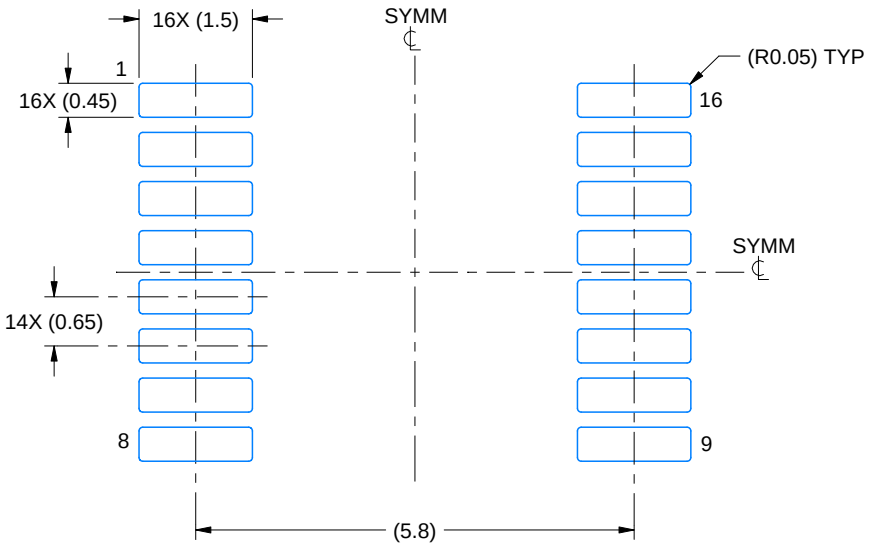
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

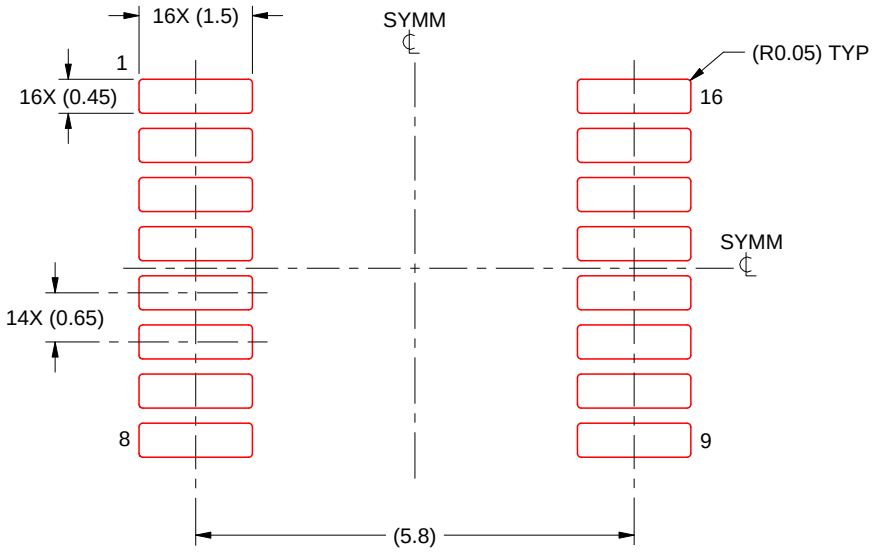


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

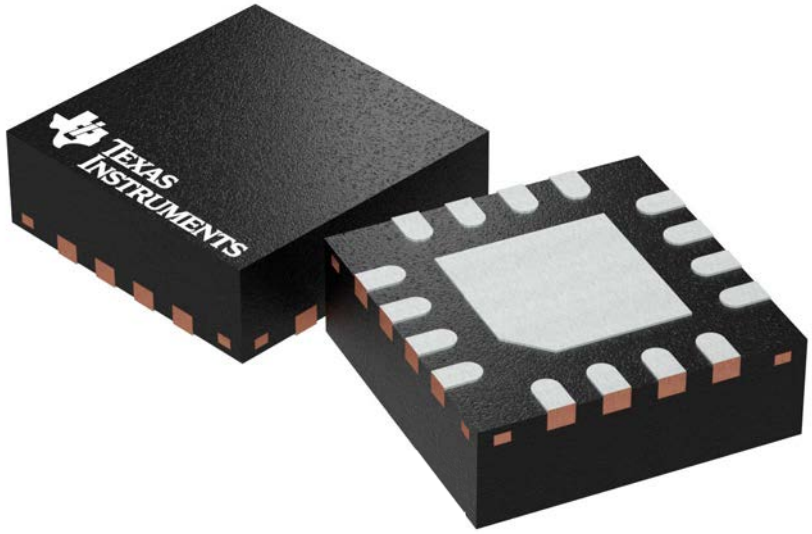
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



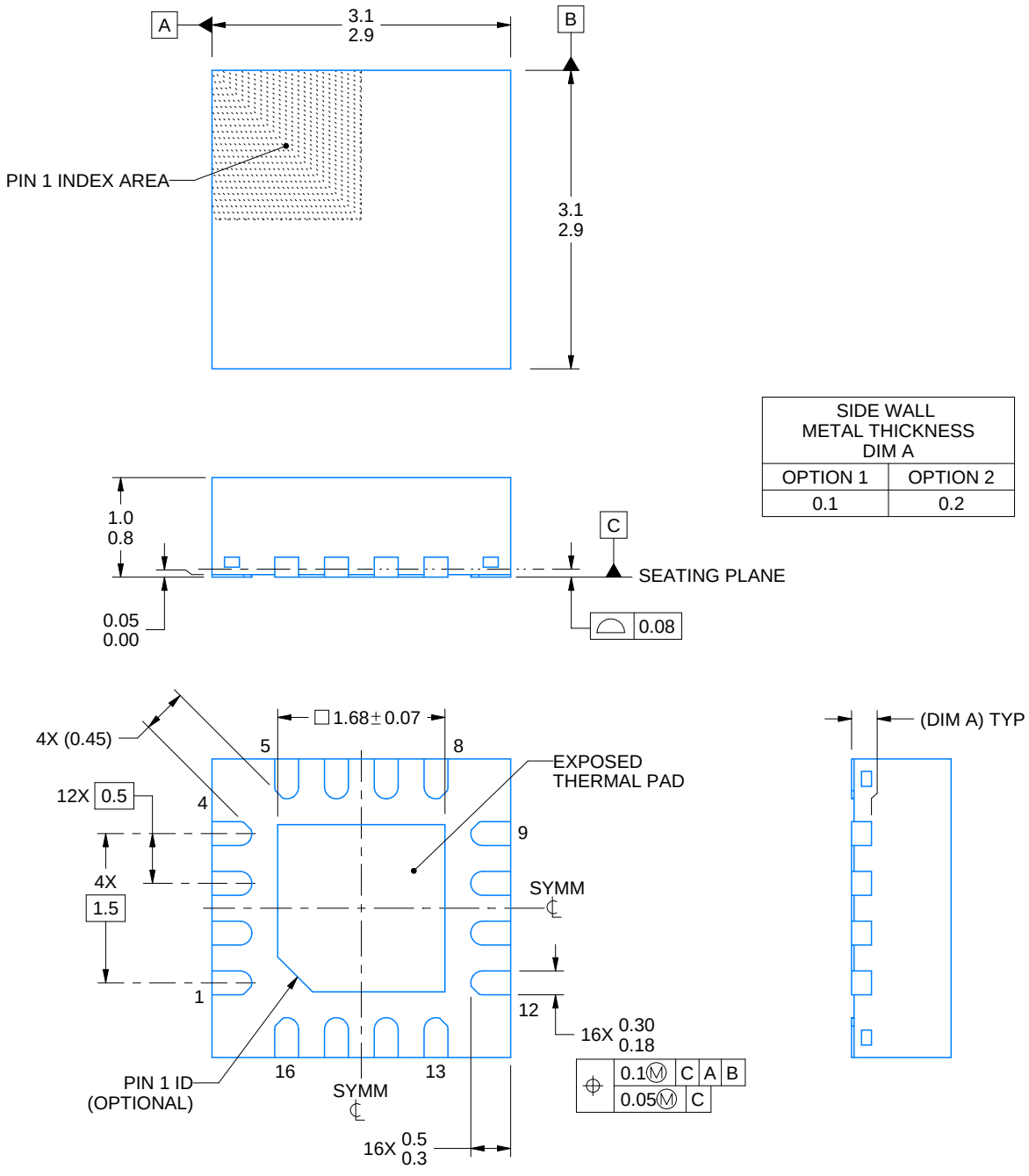
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

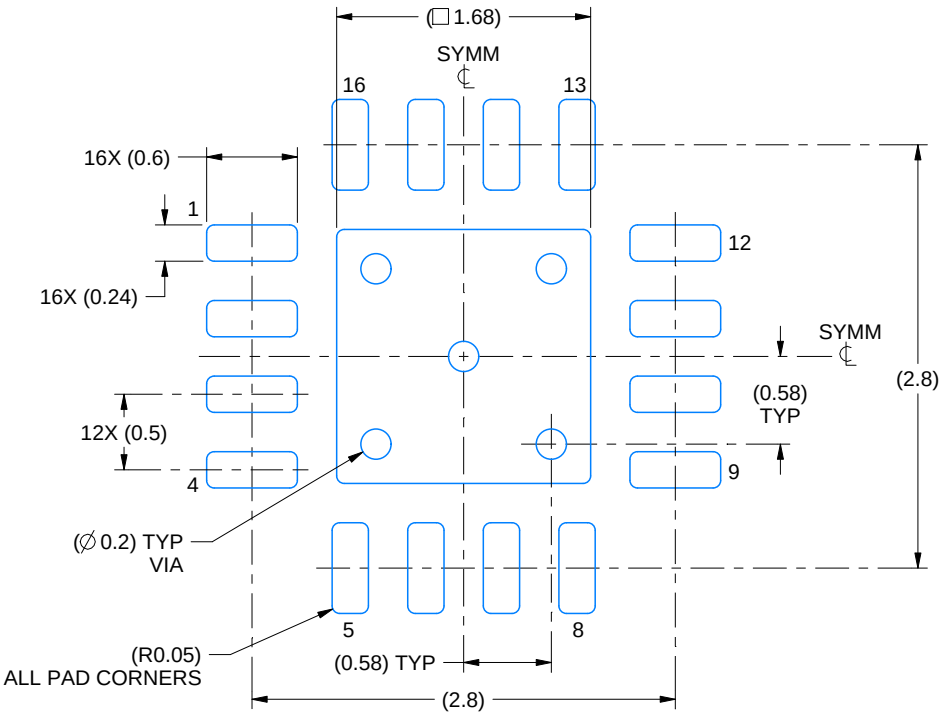
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

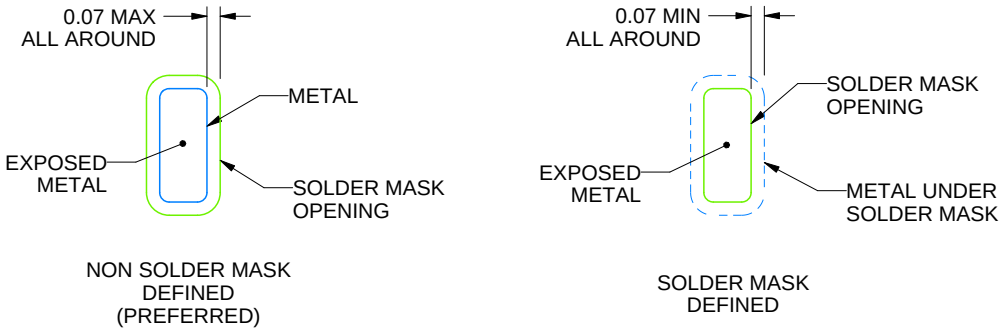


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

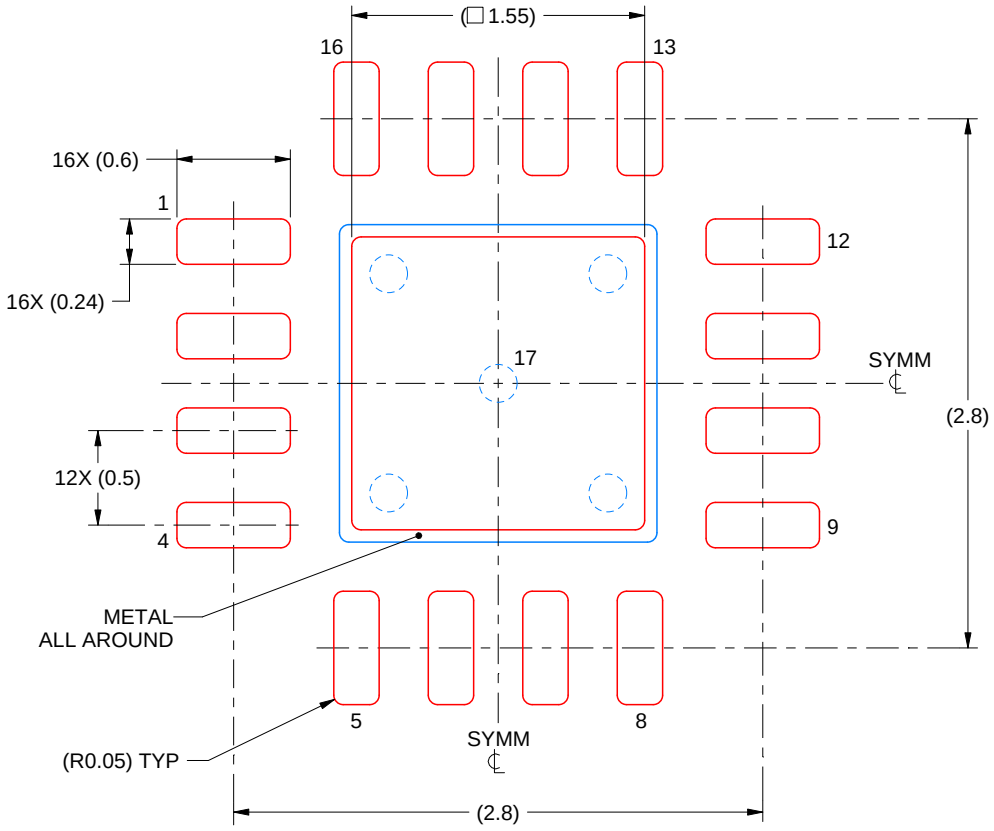


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

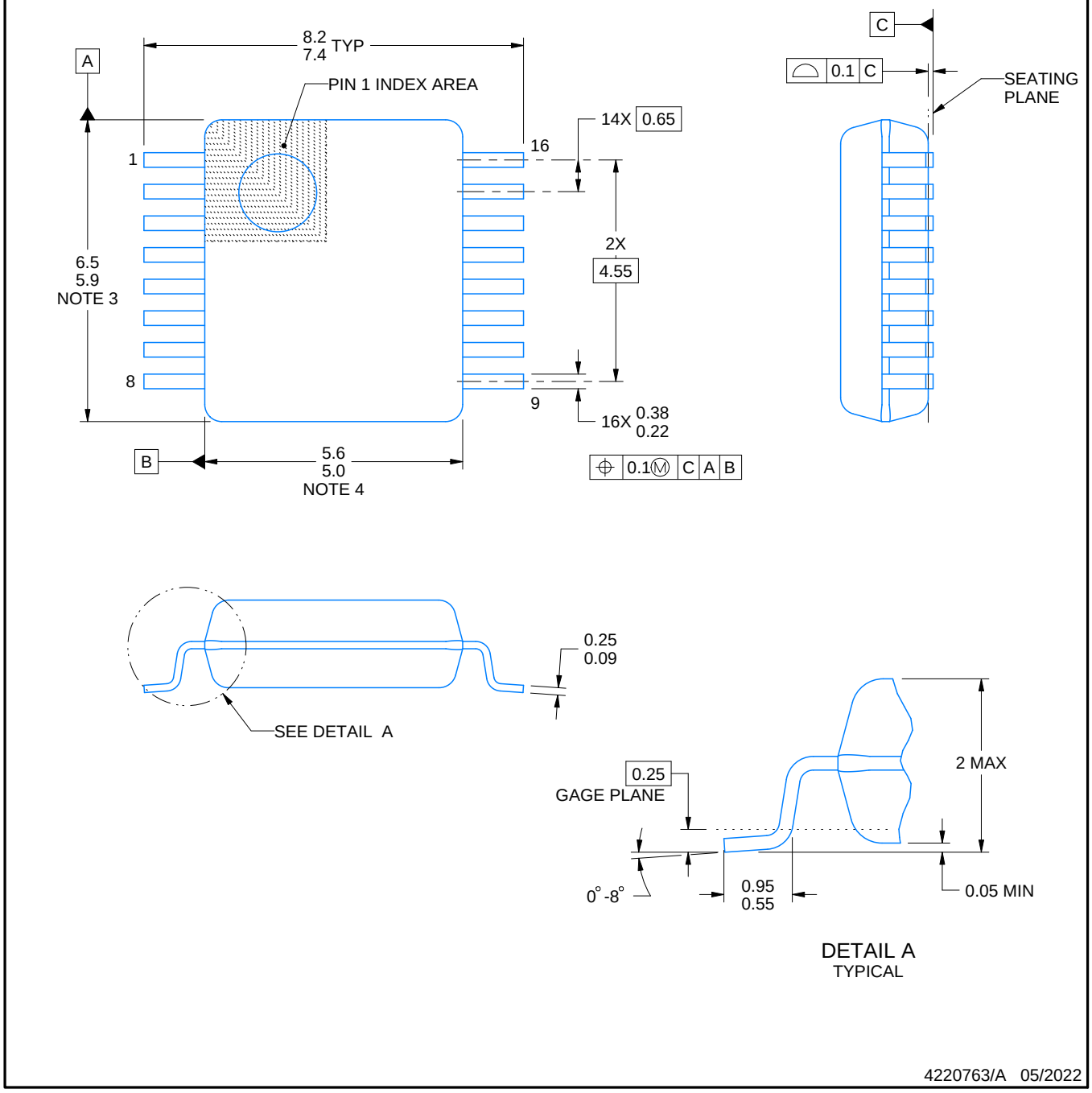
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DB0016A

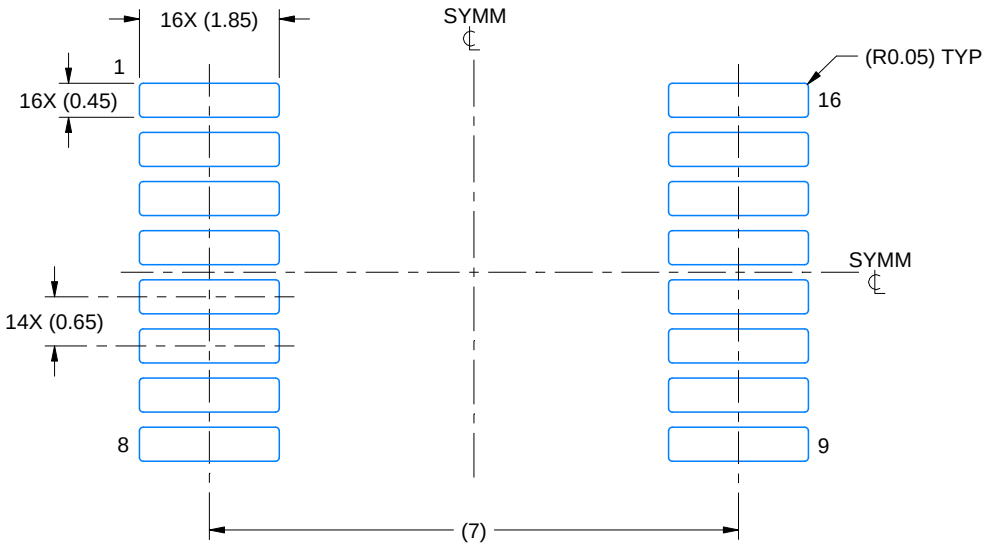
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

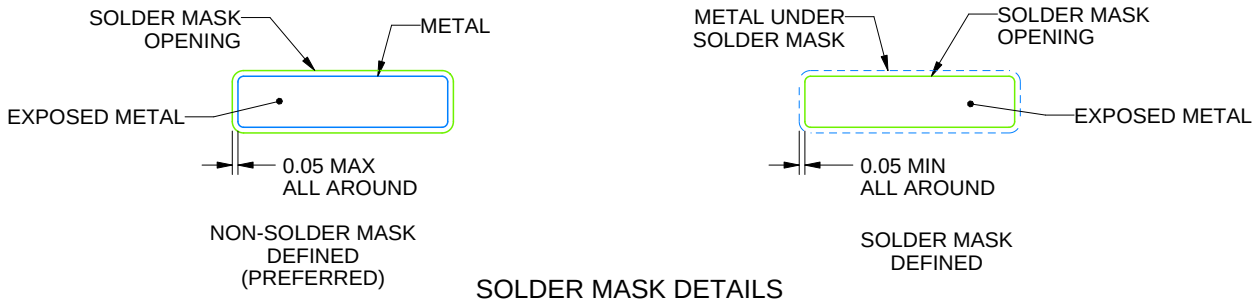


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

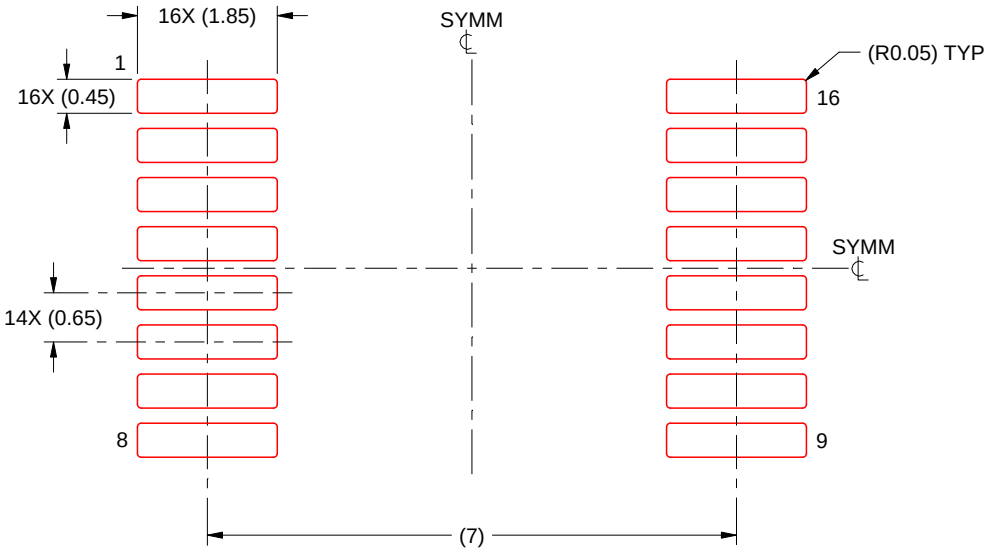


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月