

## TRS3243E $\pm 15\text{kV}$ IEC ESD 保護機能搭載、 3V~5.5V マルチチャネル RS-232 ライン・ドライバ/レシーバ

### 1 特長

- IBM™ PC/AT™ シリアル・ポート用のシングルチップおよび単一電源インターフェイス
- RS-232 バス・ピン用 ESD 保護機能
  - $\pm 15\text{kV}$  人体モデル (HBM)
  - $\pm 8\text{kV}$  IEC 61000-4-2、接触放電
  - $\pm 15\text{kV}$  IEC 61000-4-2、気中放電
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V~5.5V の  $V_{CC}$  電源で動作
- 常時アクティブの非反転レシーバ出力 (ROUT2B)
- 最大 500kbit/s のデータ・レートでの送信に対応
- 小さいスタンバイ電流: 1 $\mu\text{A}$  (標準値)
- 外付けコンデンサ:  $4 \times 0.1\mu\text{F}$
- 3.3V 電源で 5V ロジック入力を許容
- 業界標準の '3243E デバイスと交換可能
- シリアルマウス駆動可能
- 有効な RS-232 信号が検出されない場合、自動パワー・ダウン機能によりドライバ出力をディスエーブル
- プラスチック・スモール・アウトライン (DW)、シュリンク・スモール・アウトライン (DB)、シン・シュリンク・スモール・アウトライン (PW) パッケージを選択可能

### 2 アプリケーション

- バッテリ駆動システム
- パーソナル・エレクトロニクス
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

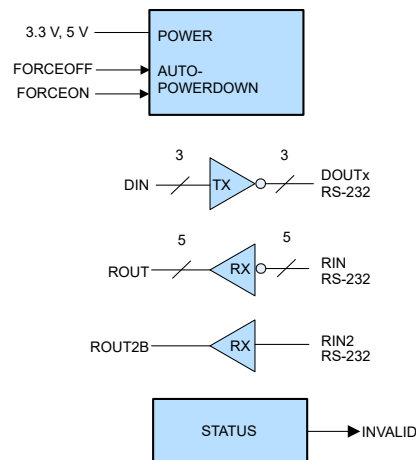
### 3 概要

TRS3243E デバイスは、3 つのライン・ドライバ、5 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、シリアル・ポート接続ピンには、 $\pm 15\text{kV}$  ESD (HBM および IEC61000-4-2、気中放電) および  $\pm 8\text{kV}$  ESD (IEC61000-4-2、接触放電) の保護を備えています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート・コネクタの間の電氣的インターフェイスとして機能します。このドライバとレシーバの組み合わせは、IBM PC/AT で使用される標準的なシリアル・ポートまたはその互換シリアル・ポートの要件を満たしています。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。さらに、本デバイスには常時アクティブな非反転出力 (ROUT2B) があり、リング・インジケータを使用するアプリケーションが、デバイスの電源がオフのときにもデータを送信できるようになっています。本デバイスは最大 250kbit/s のデータ信号速度、最大 30V/ $\mu\text{s}$  のドライバ出力スルーレートで動作します。

#### パッケージ情報

| 部品番号     | パッケージ (1)  | 本体サイズ (公称)              |
|----------|------------|-------------------------|
| TRS3243E | SSOP (DB)  | 10.20mm $\times$ 5.30mm |
|          | SOIC (DW)  | 17.90mm $\times$ 7.50mm |
|          | TSSOP (PW) | 9.70mm $\times$ 4.40mm  |
|          | VQFN (RHB) | 5.00mm $\times$ 5.00mm  |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision D (October 2022) to Revision E (December 2022)                                                                                                                                                                                         | Page |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <ul style="list-style-type: none"> <li>Changed 表 9-1 to match revision C of the data sheet. <math>V_{CC}</math> column: 3 V <math>\pm</math> 5.5 V to: 3 V to 5.5 V and C1 column value: 0.47 <math>\mu</math>F to: 0.047 <math>\mu</math>F .....</li> </ul> | 15   |

| Changes from Revision C (September 2011) to Revision D (October 2022)                                                                                                                                                                                                                                                                                                                                                                                                                     | Page                  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| <ul style="list-style-type: none"> <li>「注文情報」表を削除 .....</li> <li>「製品情報」表、「ピン構成および機能」セクション、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 .....</li> <li>先頭ページの画像をブロック図から概略回路図に変更.....</li> <li>Added the <i>ESD Ratings - IEC Specifications</i> table.....</li> <li>Changed the <math>I_{CC}</math> Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the <i>Electrical Characteristics</i> .....</li> </ul> | 1<br>1<br>1<br>6<br>8 |

| Changes from Revision B (July 2009) to Revision C (September 2011)                                                                                                                                                                                                                           | Page           |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| <ul style="list-style-type: none"> <li>Deleted "VALID RIN RS-232 LEVEL" from INPUTS.....</li> <li>Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs.....</li> <li>Added table "ROUT2B and INVALID Outputs" defining truth for ROUT2B and INVALID outputs. ....</li> </ul> | 14<br>14<br>14 |

## 5 Pin Configuration and Functions

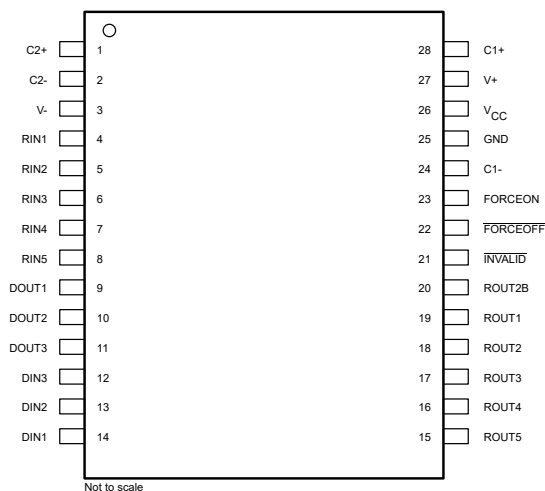
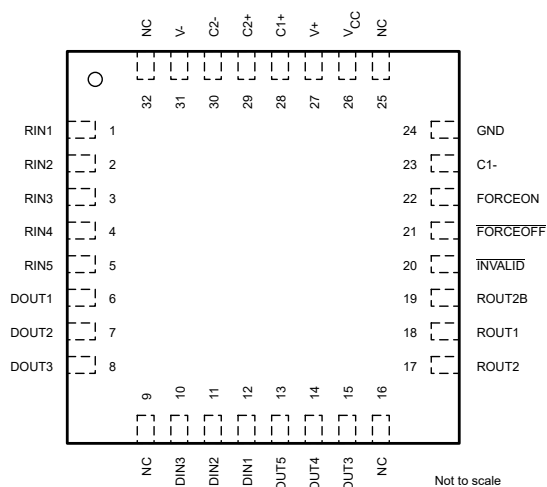


图 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP)  
(Top View)

表 5-1. Pin Functions

| PIN |                 | TYPE | DESCRIPTION                                                    |
|-----|-----------------|------|----------------------------------------------------------------|
| NO. | NAME            |      |                                                                |
| 1   | C2+             | —    | Positive terminal of the voltage-doubler charge-pump capacitor |
| 2   | C2-             | —    | Negative terminal of the voltage-doubler charge-pump capacitor |
| 3   | V-              | —    | Negative charge pump output voltage                            |
| 4   | RIN1            | I    | RS-232 receiver inputs                                         |
| 5   | RIN2            |      |                                                                |
| 6   | RIN3            |      |                                                                |
| 7   | RIN4            |      |                                                                |
| 8   | RIN5            |      |                                                                |
| 9   | DOUT1           | O    | RS-232 driver outputs                                          |
| 10  | DOUT2           |      |                                                                |
| 11  | DOUT3           |      |                                                                |
| 12  | DIN3            | I    | Driver inputs                                                  |
| 13  | DIN2            |      |                                                                |
| 14  | DIN1            |      |                                                                |
| 15  | ROUT5           | O    | Receiver outputs                                               |
| 16  | ROUT4           |      |                                                                |
| 17  | ROUT3           |      |                                                                |
| 18  | ROUT2           |      |                                                                |
| 19  | ROUT1           |      |                                                                |
| 20  | ROUT2B          | —    | Always-active noninverting receiver output;                    |
| 21  | INVALID         | O    | Invalid Output Pin                                             |
| 22  | FORCEOFF        | I    | Auto Powerdown Control input (Refer to Truth Table)            |
| 23  | FORCEON         | I    | Auto Powerdown Control input (Refer to Truth Table)            |
| 24  | C1-             | —    | Negative terminal of the voltage-doubler charge-pump capacitor |
| 25  | GND             | —    | Ground                                                         |
| 26  | V <sub>CC</sub> | —    | 3-V to 5.5-V supply voltage                                    |
| 27  | V+              | —    | Positive charge pump output voltage                            |
| 28  | C1+             | —    | Positive terminal of the voltage-doubler charge-pump capacitor |



**图 5-2. RHB Package, 32 Pin (VQFN)  
(Top View)**

**表 5-2. Pin Functions**

| PIN |                 | TYPE | DESCRIPTION                                                    |
|-----|-----------------|------|----------------------------------------------------------------|
| NO. | NAME            |      |                                                                |
| 1   | RIN1            | I    | RS-232 receiver inputs                                         |
| 2   | RIN2            |      |                                                                |
| 3   | RIN3            |      |                                                                |
| 4   | RIN4            |      |                                                                |
| 5   | RIN5            |      |                                                                |
| 6   | DOUT1           | O    | RS-232 driver outputs                                          |
| 7   | DOUT2           |      |                                                                |
| 8   | DOUT3           |      |                                                                |
| 9   | NC              | —    | Not connected internally                                       |
| 10  | DIN3            | I    | Driver inputs                                                  |
| 11  | DIN2            |      |                                                                |
| 12  | DIN1            |      |                                                                |
| 13  | ROUT5           | O    | Receiver outputs                                               |
| 14  | ROUT4           |      |                                                                |
| 15  | ROUT3           |      |                                                                |
| 16  | NC              | —    | Not connected internally                                       |
| 17  | ROUT2           | O    | Receiver outputs                                               |
| 18  | ROUT1           |      |                                                                |
| 19  | ROUT2B          | O    | Always-active noninverting receiver output                     |
| 20  | INVALID         | O    | Invalid Output Pin                                             |
| 21  | FORCEOFF        | I    | Auto Powerdown Control input (Refer to Truth Table)            |
| 22  | FORCEON         | I    | Auto Powerdown Control input (Refer to Truth Table)            |
| 23  | C1-             | —    | Negative terminal of the voltage-doubler charge-pump capacitor |
| 24  | GND             | —    | Ground                                                         |
| 25  | NC              | —    | Not connected internally                                       |
| 26  | V <sub>CC</sub> | —    | 3-V to 5.5-V supply voltage                                    |
| 27  | V+              | —    | Positive charge pump output voltage                            |

**表 5-2. Pin Functions (continued)**

| PIN |      | TYPE | DESCRIPTION                                                    |
|-----|------|------|----------------------------------------------------------------|
| NO. | NAME |      |                                                                |
| 28  | C1+  | —    | Positive terminal of the voltage-doubler charge-pump capacitor |
| 29  | C2+  | —    |                                                                |
| 30  | C2-  | —    | Negative terminal of the voltage-doubler charge-pump capacitor |
| 31  | V-   | —    | Negative charge pump output voltage                            |
| 32  | NC   | —    | Not connected internally                                       |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                 |                             | MIN   | MAX                   | UNIT |
|------------------|-------------------------------------------------|-----------------------------|-------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                   |                             | −0.3  | 6                     | V    |
| V+               | Positive output supply voltage <sup>(2)</sup>   |                             | −0.3  | 7                     | V    |
| V−               | Negative output supply voltage <sup>(2)</sup>   |                             | 0.3   | −7                    | V    |
| V+ − V−          | Output supply voltage difference <sup>(2)</sup> |                             |       | 13                    | V    |
| V <sub>I</sub>   | Input voltage                                   | Driver ( FORCEOFF, FORCEON) | −0.3  | 6                     | V    |
|                  |                                                 | Receiver                    | −25   | 25                    |      |
| V <sub>O</sub>   | Output voltage                                  | Driver                      | −13.2 | 13.2                  | V    |
|                  |                                                 | Receiver ( INVALID)         | −0.3  | V <sub>CC</sub> + 0.3 |      |
| T <sub>stg</sub> | Storage temperature                             |                             | −65   | 150                   | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

|                         |                         |                                                                                       | VALUE   | UNIT |
|-------------------------|-------------------------|---------------------------------------------------------------------------------------|---------|------|
| <b>Driver Section</b>   |                         |                                                                                       |         |      |
| V <sub>(ESD)</sub>      | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> Driver output pins  | ±15,000 | V    |
| <b>Receiver Section</b> |                         |                                                                                       |         |      |
| V <sub>(ESD)</sub>      | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> Receiver input pins | ±15,000 | V    |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - IEC Specifications

|                    |                         |                                                |                     | VALUE | UNIT |
|--------------------|-------------------------|------------------------------------------------|---------------------|-------|------|
| Driver Section     |                         |                                                |                     |       |      |
| V <sub>(ESD)</sub> | Electrostatic discharge | IEC61000-4-2, Air-Gap Discharge <sup>(1)</sup> | Driver outputs pins | ±15   | kV   |
|                    |                         | IEC61000-4-2, Contact Discharge <sup>(1)</sup> |                     | ±8    |      |
| Receiver Section   |                         |                                                |                     |       |      |
| V <sub>(ESD)</sub> | Electrostatic discharge | IEC61000-4-2, Air-Gap Discharge <sup>(1)</sup> | Receiver input pins | ±15   | kV   |
|                    |                         | IEC61000-4-2, Contact Discharge <sup>(1)</sup> |                     | ±8    |      |

- (1) For the DB, PW and RHB package only: A minimum of 1-μF capacitor between V<sub>CC</sub> and GND is required to meet the specified IEC 61000-4-2 rating

## 6.4 Recommended Operating Conditions

See [Figure 9-1](#) <sup>(1)</sup>

|                |                                             |                         | MIN                     | NOM | MAX | UNIT |
|----------------|---------------------------------------------|-------------------------|-------------------------|-----|-----|------|
| Supply voltage |                                             | $V_{CC} = 3.3\text{ V}$ | 3                       | 3.3 | 3.6 | V    |
|                |                                             | $V_{CC} = 5\text{ V}$   | 4.5                     | 5   | 5.5 |      |
| $V_{IH}$       | Driver and control high-level input voltage | DIN, FORCEOFF, FORCEON  | $V_{CC} = 3.3\text{ V}$ |     | 2   | V    |
|                |                                             |                         | $V_{CC} = 5\text{ V}$   |     | 2.4 |      |
| $V_{IL}$       | Driver and control low-level input voltage  | DIN, FORCEOFF, FORCEON  |                         |     | 0.8 | V    |
| $V_I$          | Driver and control input voltage            | DIN, FORCEOFF, FORCEON  | 0                       |     | 5.5 | V    |
| $V_I$          | Receiver input voltage                      |                         | –25                     |     | 25  | V    |
| $T_A$          | Operating free-air temperature              | TRS3243EC               | 0                       |     | 70  | °C   |
|                |                                             | TRS3243EI               | –40                     |     | 85  |      |

(1) Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

## 6.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | VQFN (RHB) | TSSOP (PW) | SOIC (DW) | DB (SSOP) | UNIT |
|-------------------------------|----------------------------------------------|------------|------------|-----------|-----------|------|
|                               |                                              | 32 PINS    | 28 PINS    | 28 PINS   | 28 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 34.1       | 70.3       | 59.0      | 76.1      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 25.9       | 21.0       | 28.8      | 35.8      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 14.6       | 29.2       | 30.3      | 37.4      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 0.5        | 1.3        | 7.8       | 7.4       | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 14.6       | 28.8       | 30.0      | 37.0      | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 5.1        | N/A        | N/A       | N/A       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))<sup>(2)</sup>

| PARAMETER               |                                                                |                                                                                             | TEST CONDITIONS                                                                                                    |                              | MIN | TYP <sup>(1)</sup>    | MAX                   | UNIT |    |
|-------------------------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|------------------------------|-----|-----------------------|-----------------------|------|----|
| I <sub>I</sub>          | Input leakage current                                          | FORCEOFF, FORCEON                                                                           |                                                                                                                    |                              |     | ±0.01                 | ±1                    | μA   |    |
| I <sub>CC</sub>         | Supply current<br>(T <sub>A</sub> = 25°C)                      | Auto-powerdown disabled                                                                     | No load,<br>FORCEOFF and FORCEON at V <sub>CC</sub><br>For DB, PW and RHB package                                  |                              |     | 0.3                   | 1.2                   | mA   |    |
|                         |                                                                | Auto-powerdown disabled                                                                     | No load,<br>FORCEOFF and FORCEON at V <sub>CC</sub><br>For DW package                                              |                              |     | 0.3                   | 1                     | mA   |    |
|                         |                                                                | Powered off                                                                                 | No load, FORCEOFF at GND                                                                                           |                              |     | 1                     | 10                    | μA   |    |
|                         |                                                                | Auto-powerdown enabled                                                                      | No load, FORCEOFF at V <sub>CC</sub> .<br>FORCEON at GND,<br>All RIN are open or grounded,<br>All DIN are grounded |                              |     | 1                     | 10                    |      |    |
| DRIVER SECTION          |                                                                |                                                                                             |                                                                                                                    |                              |     |                       |                       |      |    |
| V <sub>OH</sub>         | High-level output voltage                                      | All DOUT at R <sub>L</sub> = 3 kΩ to GND                                                    |                                                                                                                    |                              |     | 5                     | 5.4                   | V    |    |
| V <sub>OL</sub>         | Low-level output voltage                                       | All DOUT at R <sub>L</sub> = 3 kΩ to GND                                                    |                                                                                                                    |                              |     | –5                    | –5.4                  | V    |    |
| V <sub>O</sub>          | Output voltage<br>(mouse driveability)                         | DIN1 = DIN2 = GND, DIN3 = V <sub>CC</sub> , 3-kΩ to GND at DOUT3,<br>DOUT1 = DOUT2 = 2.5 mA |                                                                                                                    |                              |     | ±5                    |                       | V    |    |
| I <sub>IH</sub>         | High-level input current                                       | V <sub>I</sub> = V <sub>CC</sub>                                                            |                                                                                                                    |                              |     | ±0.01                 | ±1                    | μA   |    |
| I <sub>IL</sub>         | Low-level input current                                        | V <sub>I</sub> at GND                                                                       |                                                                                                                    |                              |     | ±0.01                 | ±1                    | μA   |    |
| V <sub>hys</sub>        | Input hysteresis                                               |                                                                                             |                                                                                                                    |                              |     |                       | ±1                    | V    |    |
| I <sub>OS</sub>         | Short-circuit output current <sup>(3)</sup>                    | V <sub>CC</sub> = 3.6 V,                                                                    | V <sub>O</sub> = 0 V                                                                                               |                              |     |                       | ±60                   | mA   |    |
|                         |                                                                | V <sub>CC</sub> = 5.5 V,                                                                    | V <sub>O</sub> = 0 V                                                                                               |                              |     |                       |                       |      |    |
| r <sub>O</sub>          | Output resistance                                              | V <sub>CC</sub> , V+, and V– = 0 V,                                                         |                                                                                                                    | V <sub>O</sub> = ±2 V        |     | 300                   | 10M                   | Ω    |    |
| I <sub>off</sub>        | Output leakage current                                         | FORCEOFF = GND,                                                                             | V <sub>O</sub> = ±12 V,                                                                                            | V <sub>CC</sub> = 0 to 5.5 V |     |                       | ±25                   | μA   |    |
| RECEIVER SECTION        |                                                                |                                                                                             |                                                                                                                    |                              |     |                       |                       |      |    |
| V <sub>OH</sub>         | High-level output voltage                                      | I <sub>OH</sub> = –1 mA                                                                     |                                                                                                                    |                              |     | V <sub>CC</sub> – 0.6 | V <sub>CC</sub> – 0.1 | V    |    |
| V <sub>OL</sub>         | Low-level output voltage                                       | I <sub>OH</sub> = 1.6 mA                                                                    |                                                                                                                    |                              |     |                       | 0.4                   | V    |    |
| V <sub>IT+</sub>        | Positive-going input threshold voltage                         | V <sub>CC</sub> = 3.3 V                                                                     |                                                                                                                    |                              |     | 1.6                   | 2.4                   | V    |    |
|                         |                                                                | V <sub>CC</sub> = 5 V                                                                       |                                                                                                                    |                              |     | 1.9                   | 2.4                   |      |    |
| V <sub>IT–</sub>        | Negative-going input threshold voltage                         | V <sub>CC</sub> = 3.3 V                                                                     |                                                                                                                    |                              |     | 0.6                   | 1.1                   | V    |    |
|                         |                                                                | V <sub>CC</sub> = 5 V                                                                       |                                                                                                                    |                              |     | 0.8                   | 1.4                   |      |    |
| V <sub>hys</sub>        | Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )        |                                                                                             |                                                                                                                    |                              |     |                       | 0.5                   | V    |    |
| I <sub>off</sub>        | Output leakage current (except ROUT2B)                         | FORCEOFF = 0 V                                                                              |                                                                                                                    |                              |     |                       | ±0.05                 | ±10  | μA |
| r <sub>i</sub>          | Input resistance                                               | V <sub>I</sub> = ±3 V or ±25 V                                                              |                                                                                                                    |                              |     | 3                     | 5                     | 7    | kΩ |
| AUTO-POWERDOWN SECTION  |                                                                |                                                                                             |                                                                                                                    |                              |     |                       |                       |      |    |
| V <sub>IT+(valid)</sub> | Receiver input threshold for INVALID high-level output voltage | FORCEON = GND, FORCEOFF = V <sub>CC</sub>                                                   |                                                                                                                    |                              |     |                       | 2.7                   | V    |    |
| V <sub>IT–(valid)</sub> | Receiver input threshold for INVALID high-level output voltage | FORCEON = GND, FORCEOFF = V <sub>CC</sub>                                                   |                                                                                                                    |                              |     | –2.7                  |                       | V    |    |
| V <sub>T(invalid)</sub> | Receiver input threshold for INVALID low-level output voltage  | FORCEON = GND, FORCEOFF = V <sub>CC</sub>                                                   |                                                                                                                    |                              |     | –0.3                  | 0.3                   | V    |    |
| V <sub>OH</sub>         | INVALID high-level output voltage                              | I <sub>OH</sub> = -1 mA, FORCEON = GND, FORCEOFF = V <sub>CC</sub>                          |                                                                                                                    |                              |     | V <sub>CC</sub> – 0.6 |                       | V    |    |
| V <sub>OL</sub>         | INVALID low-level output voltage                               | I <sub>OL</sub> = 1.6 mA, FORCEON = GND, FORCEOFF = V <sub>CC</sub>                         |                                                                                                                    |                              |     |                       | 0.4                   | V    |    |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

(2) Test conditions are C1–C4 = 0.1 μF at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047 μF, C2–C4 = 0.33 μF at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

## 6.7 Switching Characteristics

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#)) <sup>(2)</sup>

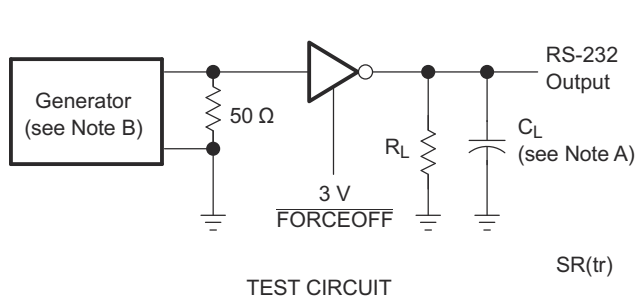
| PARAMETER              |                                                      | TEST CONDITIONS                                                                |                                             | MIN | TYP <sup>(1)</sup> | MAX | UNIT   |
|------------------------|------------------------------------------------------|--------------------------------------------------------------------------------|---------------------------------------------|-----|--------------------|-----|--------|
| DRIVER SECTION         |                                                      |                                                                                |                                             |     |                    |     |        |
|                        | Maximum data rate                                    | C <sub>L</sub> = 1000 pF,<br>One DOUT switching,                               | R <sub>L</sub> = 3 kΩ<br>See Figure 1       | 250 | 500                |     | kbit/s |
| t <sub>sk(p)</sub>     | Pulse skew <sup>(3)</sup>                            | C <sub>L</sub> = 150 pF to 2500 pF,                                            | R <sub>L</sub> = 3 kΩ to 7 kΩ, See Figure 2 |     | 100                |     | ns     |
| SR(tr)                 | Slew rate, transition region<br>(see Figure 1)       | V <sub>CC</sub> = 3.3 V,<br>R <sub>L</sub> = 3 kΩ to 7 kΩ,<br>PRR = 250 kbit/s | C <sub>L</sub> = 150 pF to 1000 pF          | 6   |                    | 30  | V/μs   |
|                        |                                                      |                                                                                | C <sub>L</sub> = 150 pF to 2500 pF          | 4   |                    | 30  |        |
| RECEIVER SECTION       |                                                      |                                                                                |                                             |     |                    |     |        |
| t <sub>PLH</sub>       | Propagation delay time, low-<br>to high-level output | C <sub>L</sub> = 150 pF, See <a href="#">Figure 7-2</a>                        |                                             |     | 150                |     | ns     |
| t <sub>PHL</sub>       | Propagation delay time, high-<br>to low-level output |                                                                                |                                             |     | 150                |     | ns     |
| t <sub>en</sub>        | Output enable time                                   | C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 7-3</a> |                                             |     | 200                |     | ns     |
| t <sub>dis</sub>       | Output disable time                                  |                                                                                |                                             |     | 200                |     | ns     |
| t <sub>sk(p)</sub>     | Pulse skew <sup>(3)</sup>                            | See <a href="#">Figure 7-2</a>                                                 |                                             |     | 50                 |     | ns     |
| AUTO-POWERDOWN SECTION |                                                      |                                                                                |                                             |     |                    |     |        |
| t <sub>valid</sub>     | Propagation delay time, low-<br>to high-level output | V <sub>CC</sub> = 5 V                                                          |                                             |     | 1                  |     | μs     |
| t <sub>invalid</sub>   | Propagation delay time, high-<br>to low-level output | V <sub>CC</sub> = 5 V                                                          |                                             |     | 30                 |     | μs     |
| t <sub>en</sub>        | Supply enable time                                   | V <sub>CC</sub> = 5 V                                                          |                                             |     | 100                |     | μs     |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

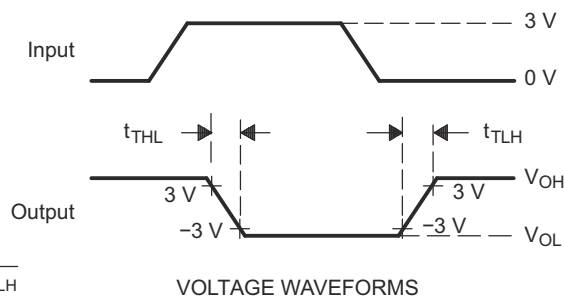
(2) Test conditions are  $C1-C4 = 0.1\text{ }\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} + 0.3\text{ V}$ ;  $C1 = 0.047\text{ }\mu\text{F}$ ,  $C2-C4 = 0.33\text{ }\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

## 7 Parameter Measurement Information



$$SR(tr) = \frac{6 V}{t_{THL} \text{ or } t_{TLH}}$$

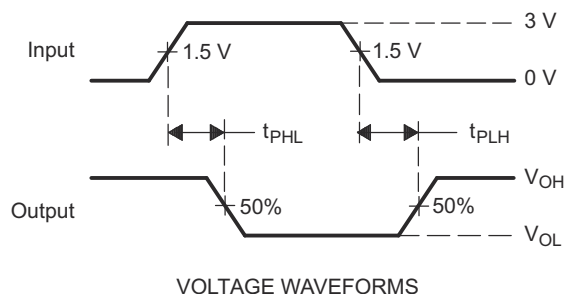
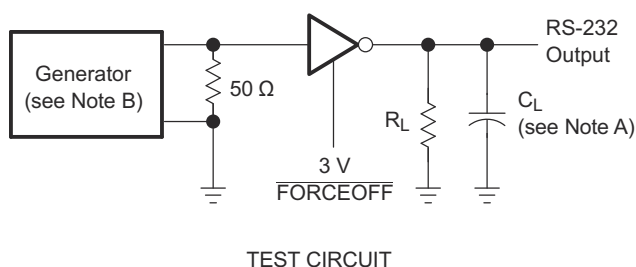


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A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

### 7-1. Driver Slew Rate

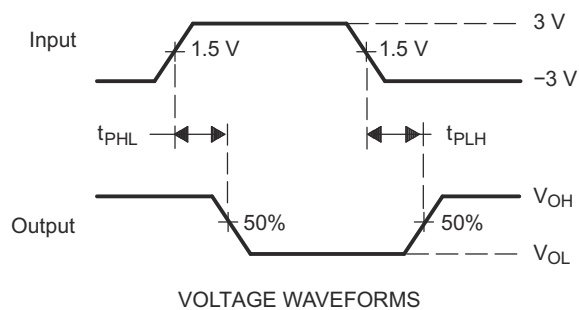
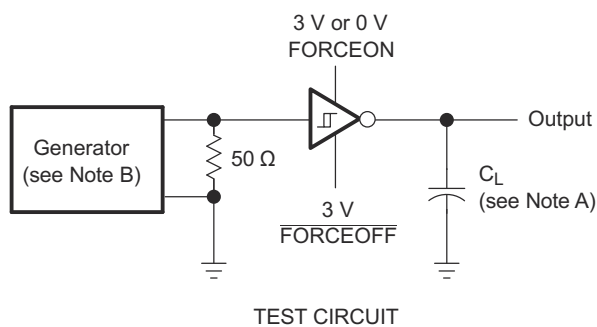


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A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

### 7-2. Driver Pulse Skew

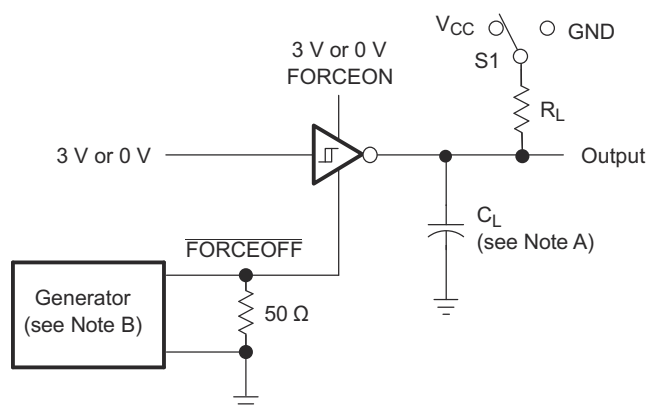


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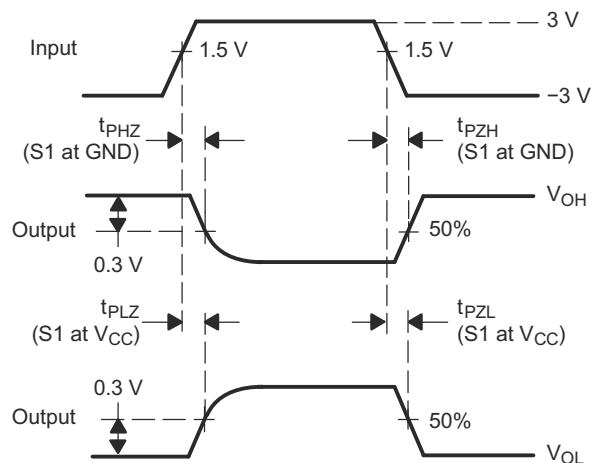
A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

### 7-3. Receiver Propagation Delay Times



TEST CIRCUIT

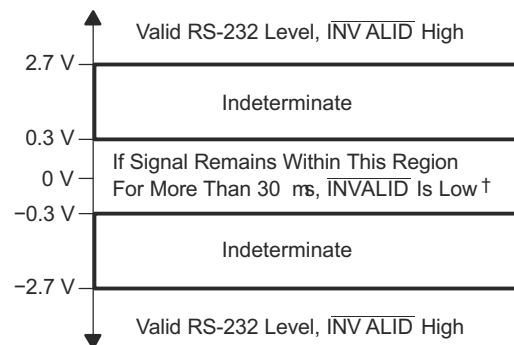
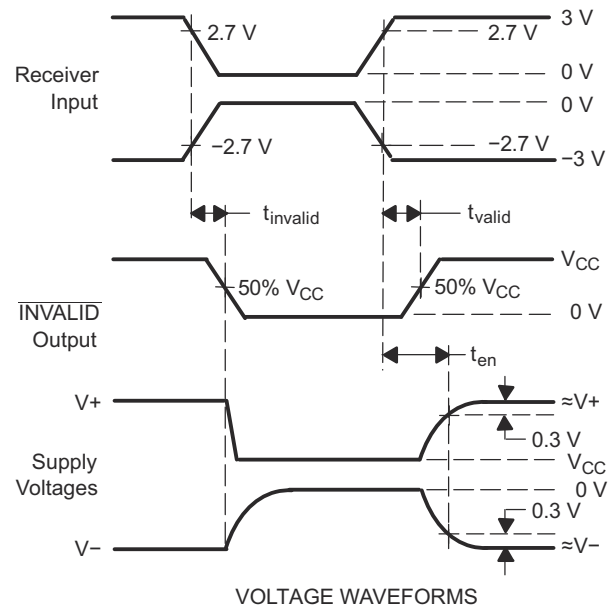
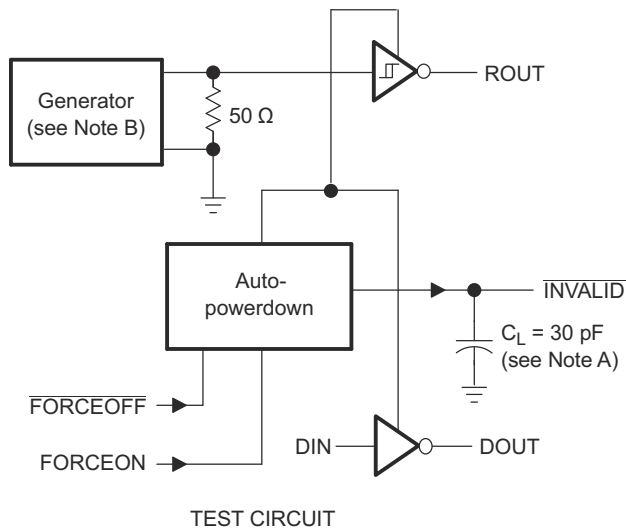


VOLTAGE WAVEFORMS

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- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .
- C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

#### 7-4. Receiver Enable And Disable Times



$^\dagger$  Auto-powerdown disables drivers and reduces supply current to 1 mA.

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A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

## 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times And Supply Enabling Time

## 8 Detailed Description

### 8.1 Overview

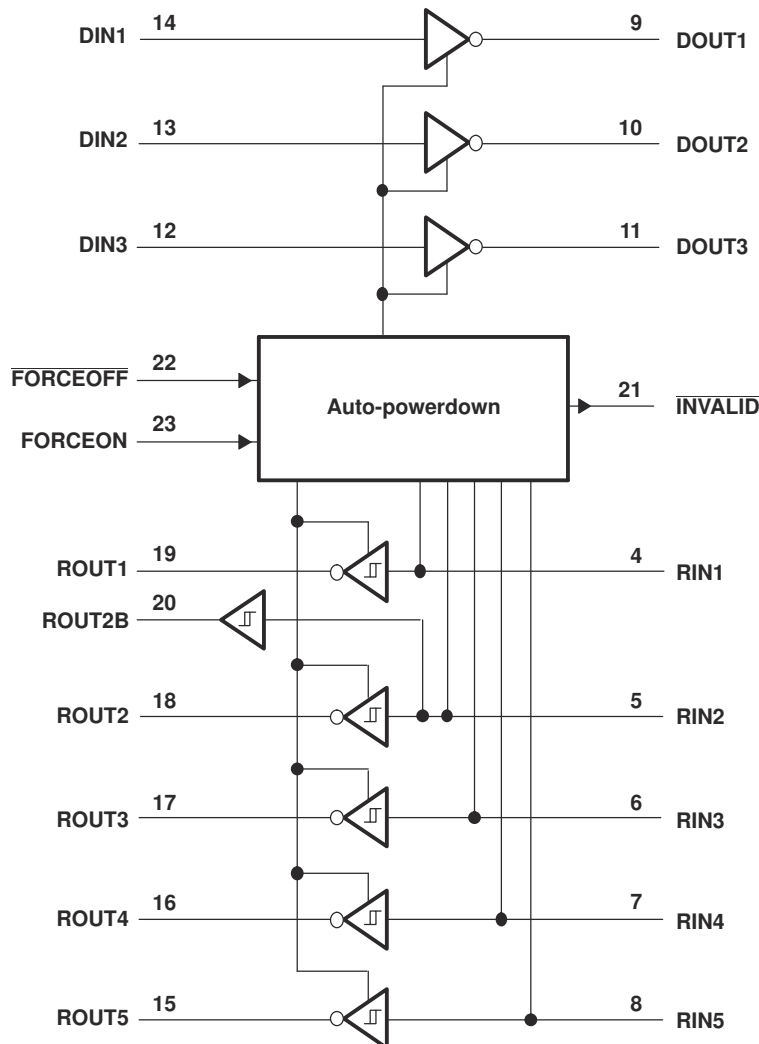
Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when **FORCEON** is low and **FORCEOFF** is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If **FORCEOFF** is set low, both drivers and receivers (except **ROUT2B**) are shut off, and the supply current is reduced to 1  $\mu$ A.

Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when **FORCEON** and **FORCEOFF** are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The **INVALID** output is used to notify the user if an RS-232 signal is present at any receiver input. **INVALID** is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30  $\mu$ s. **INVALID** is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30  $\mu$ s. Refer to [Figure 7-5](#) for receiver input levels.

The TRS3243E is characterized for operation from 0°C to 70°C. The TRS3243EI is characterized for operation from -40°C to +85°C.

### 8.2 Functional Block Diagram



Logic Diagram (Positive Logic)

## 8.3 Device Functional Modes

表 8-1 through 表 8-3 show the device functional modes.

表 8-1. Each Driver

| INPUTS <sup>(1)</sup> |         |          |                           | OUTPUT | DRIVER STATUS                                    |
|-----------------------|---------|----------|---------------------------|--------|--------------------------------------------------|
| DIN                   | FORCEON | FORCEOFF | VALID RIN<br>RS-232 LEVEL | DOUT   |                                                  |
| X                     | X       | L        | X                         | Z      | Powered off                                      |
| L                     | H       | H        | X                         | H      | Normal operation with<br>auto-powerdown disabled |
| H                     | H       | H        | X                         | L      |                                                  |
| L                     | L       | H        | Yes                       | H      | Normal operation with<br>auto-powerdown enabled  |
| H                     | L       | H        | Yes                       | L      |                                                  |
| X                     | L       | H        | No                        | Z      | Powered off by auto-powerdown<br>feature         |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 8-2. Each Receiver

| INPUTS <sup>(1)</sup> |         |          | OUTPUT | RECEIVER STATUS                                          |
|-----------------------|---------|----------|--------|----------------------------------------------------------|
| RIN                   | FORCEON | FORCEOFF | ROUT   |                                                          |
| X                     | X       | L        | Z      | Powered off                                              |
| L                     | X       | H        | H      | Normal operation with<br>auto-powerdown disabled/enabled |
| H                     | X       | H        | L      |                                                          |
| Open                  | X       | H        | H      |                                                          |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 8-3. ROUT2B And Outputs  $\overline{\text{INVALID}}$

| INPUTS <sup>(1)</sup>     |      |         |          | OUTPUTS                     |        | OUTPUT STATUS |
|---------------------------|------|---------|----------|-----------------------------|--------|---------------|
| VALID RIN<br>RS-232 LEVEL | RIN2 | FORCEON | FORCEOFF | $\overline{\text{INVALID}}$ | ROUT2B |               |
| Yes                       | L    | X       | X        | H                           | L      | Always active |
| Yes                       | H    | X       | X        | H                           | H      |               |
| Yes                       | Open | X       | X        | H                           | L      |               |
| No                        | Open | X       | X        | L                           | L      |               |

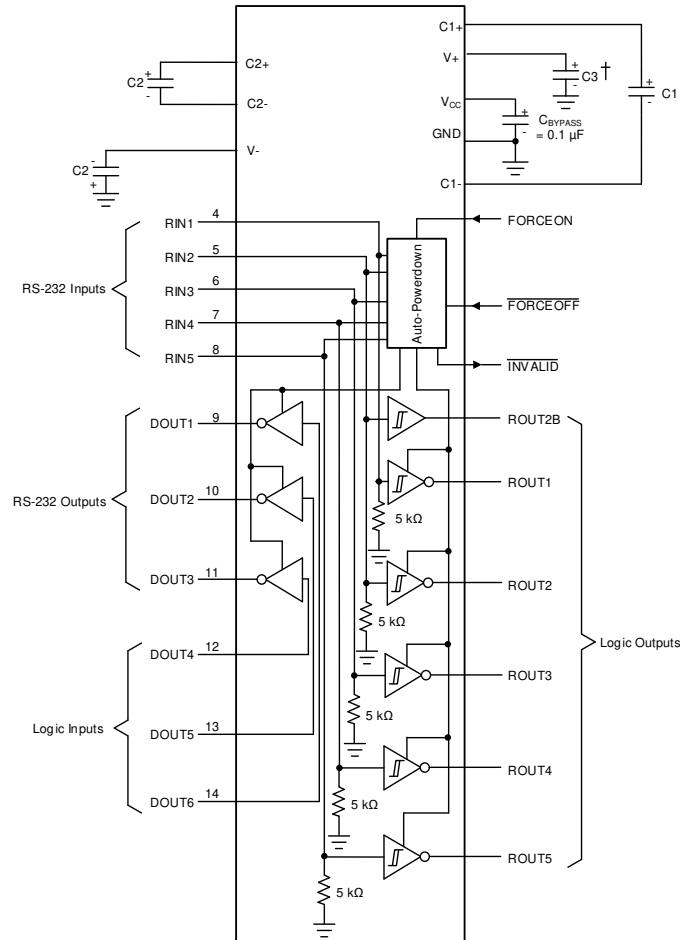
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Typical Application



- A. C3 can be connected to  $V_{CC}$  or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If using polarized tantalum or electrolytic capacitors, connect them as shown.

図 9-1. Typical Operating Circuit and Capacitor Values

表 9-1.  $V_{CC}$  vs Capacitor Values

| $V_{CC}$          | C1            | C2, C3, and C4 |
|-------------------|---------------|----------------|
| 3.3 V $\pm$ 0.3 V | 0.1 $\mu$ F   | 0.1 $\mu$ F    |
| 5 V $\pm$ 0.5 V   | 0.047 $\mu$ F | 0.33 $\mu$ F   |
| 3 V to 5.5 V      | 0.1 $\mu$ F   | 0.47 $\mu$ F   |

## 9.1.1 Detailed Design Procedure

### 9.1.1.1 ESD Protection

TI TRS3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$ -kV in all states: normal operation, shutdown, and powered down. The TRS3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The TRS3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

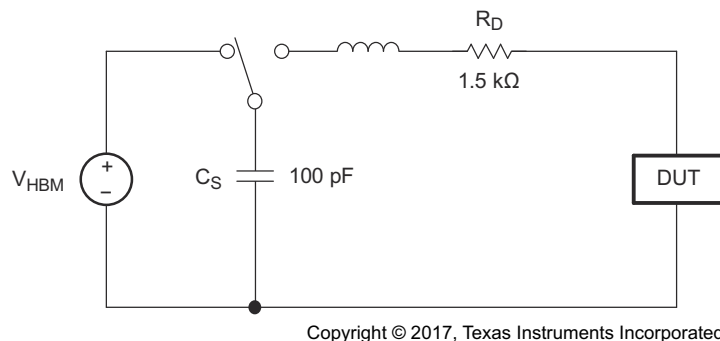
- $\pm 15$ -kV Human-Body Model (HBM)
- $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- $\pm 8$ -kV IEC61000-4-2, Contact Discharge

### 9.1.1.2 ESD Test Conditions

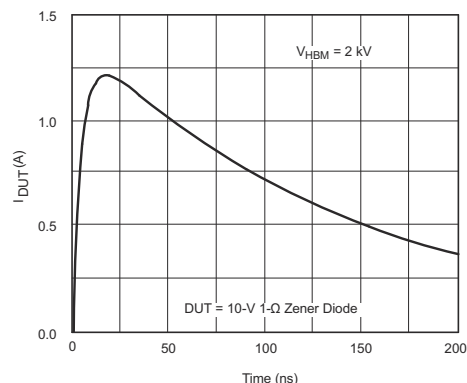
ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

### 9.1.1.3 Human-Body Model (HBM)

The HBM of ESD testing is shown in [Figure 9-2](#), while [Figure 9-3](#) shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k $\Omega$  resistor.



**Figure 9-2. HBM ESD Test Circuit**

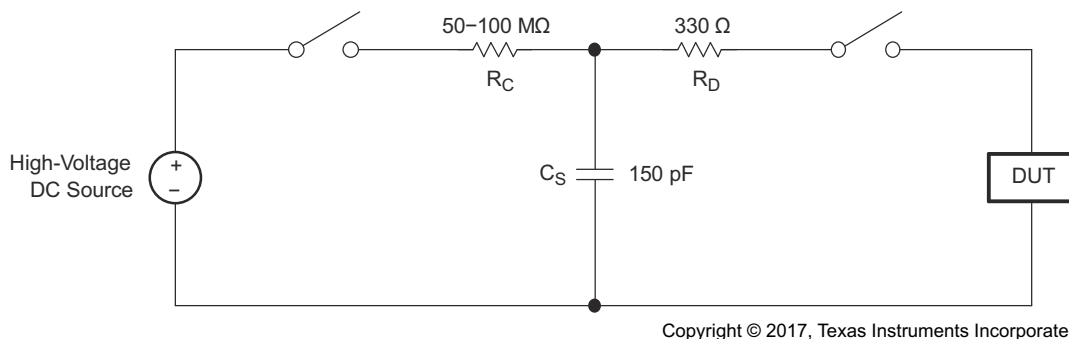


**Figure 9-3. Typical HBM Current Waveform**

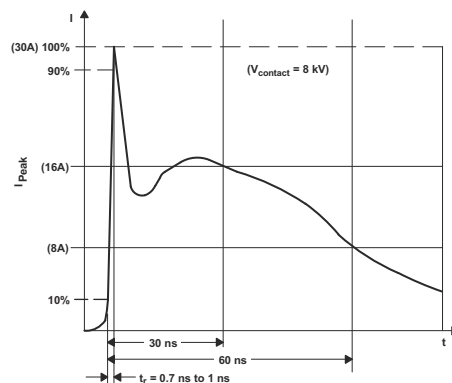
#### 9.1.1.4 IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The TRS3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

Figure 9-4 shows the IEC61000-4-2 model, and Figure 9-5 shows the current waveform for the corresponding  $\pm 8$ -kV contact-discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding  $\pm 15$ -kV (Level 4) air-gap discharge test involves approaching the DUT with an already energized probe.



**Figure 9-4. Simplified IEC61000-4-2 ESD Test Circuit**



**Figure 9-5. Typical Current Waveform Of IEC61000-4-2 ESD Generator**

## 10 Device and Documentation Support

### 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](https://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

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### 10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.5 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TRS3243ECDB</a>   | Obsolete      | Production           | SSOP (DB)   28  | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | TRS3243EC           |
| <a href="#">TRS3243ECDBR</a>  | Active        | Production           | SSOP (DB)   28  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TRS3243EC           |
| TRS3243ECDBR.A                | Active        | Production           | SSOP (DB)   28  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TRS3243EC           |
| <a href="#">TRS3243ECDW</a>   | Obsolete      | Production           | SOIC (DW)   28  | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | TRS3243EC           |
| <a href="#">TRS3243ECDWR</a>  | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TRS3243EC           |
| TRS3243ECDWR.A                | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TRS3243EC           |
| <a href="#">TRS3243ECPW</a>   | Obsolete      | Production           | TSSOP (PW)   28 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | RS43EC              |
| <a href="#">TRS3243ECPWR</a>  | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | RS43EC              |
| TRS3243ECPWR.A                | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | RS43EC              |
| <a href="#">TRS3243ECRHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | RS43EC              |
| TRS3243ECRHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | RS43EC              |
| <a href="#">TRS3243EIDBR</a>  | Active        | Production           | SSOP (DB)   28  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TRS3243EI           |
| TRS3243EIDBR.A                | Active        | Production           | SSOP (DB)   28  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TRS3243EI           |
| TRS3243EIDBRG4                | Active        | Production           | SSOP (DB)   28  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TRS3243EI           |
| TRS3243EIDBRG4.A              | Active        | Production           | SSOP (DB)   28  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TRS3243EI           |
| <a href="#">TRS3243EIDW</a>   | Obsolete      | Production           | SOIC (DW)   28  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | TRS3243EI           |
| <a href="#">TRS3243EIDWR</a>  | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TRS3243EI           |
| TRS3243EIDWR.A                | Active        | Production           | SOIC (DW)   28  | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TRS3243EI           |
| <a href="#">TRS3243EIPWR</a>  | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | RS43EI              |
| TRS3243EIPWR.A                | Active        | Production           | TSSOP (PW)   28 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | RS43EI              |
| <a href="#">TRS3243EIRHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | RS43EI              |
| TRS3243EIRHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | RS43EI              |
| TRS3243EIRHBRG4               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | RS43EI              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

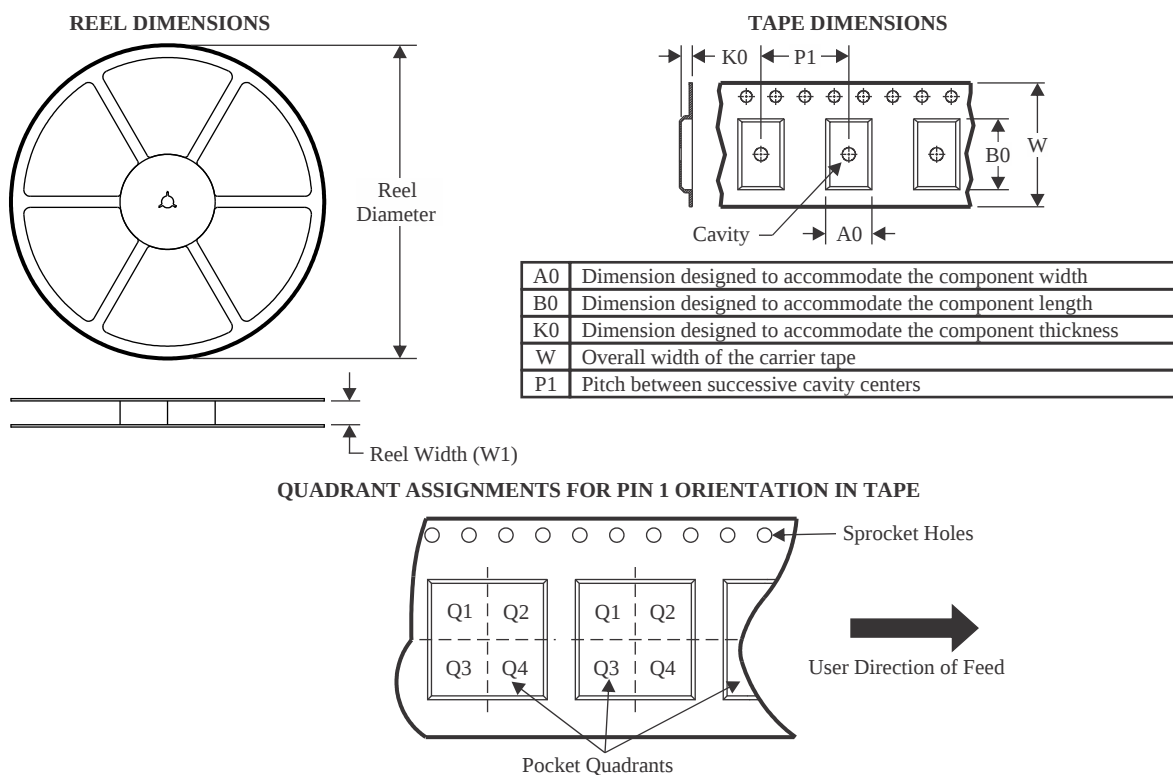
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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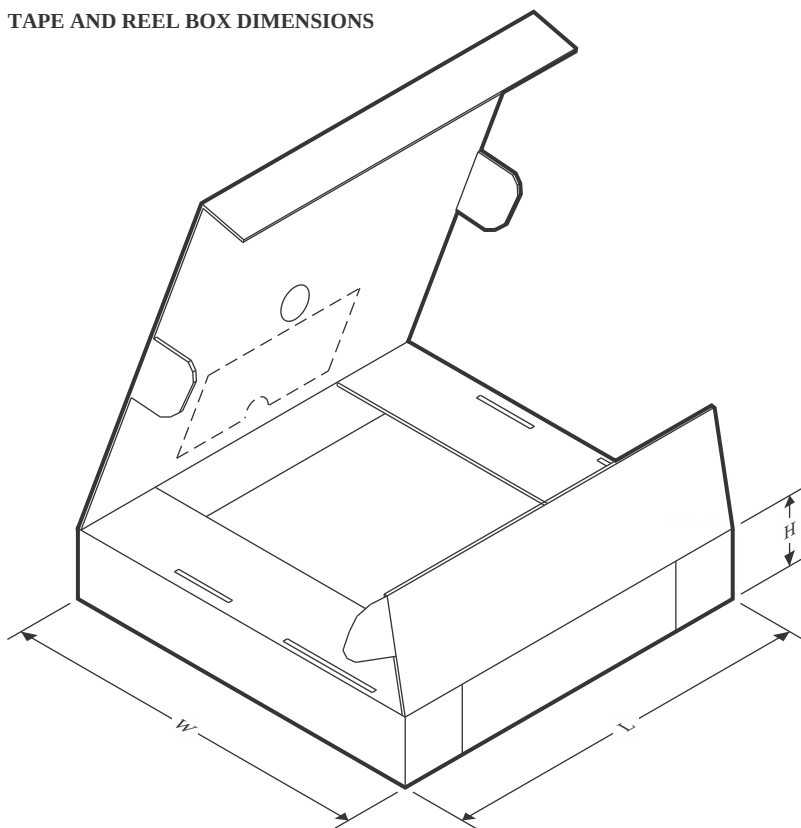
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRS3243ECDBR   | SSOP         | DB              | 28   | 2000 | 330.0              | 16.4               | 8.45    | 10.55   | 2.5     | 12.0    | 16.2   | Q1            |
| TRS3243ECDWR   | SOIC         | DW              | 28   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |
| TRS3243ECPWR   | TSSOP        | PW              | 28   | 2000 | 330.0              | 16.4               | 6.75    | 10.1    | 1.8     | 12.0    | 16.0   | Q1            |
| TRS3243ECRHBR  | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TRS3243EIDBR   | SSOP         | DB              | 28   | 2000 | 330.0              | 16.4               | 8.45    | 10.55   | 2.5     | 12.0    | 16.2   | Q1            |
| TRS3243EIDBRG4 | SSOP         | DB              | 28   | 2000 | 330.0              | 16.4               | 8.45    | 10.55   | 2.5     | 12.0    | 16.2   | Q1            |
| TRS3243EIDWR   | SOIC         | DW              | 28   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |
| TRS3243EIPWR   | TSSOP        | PW              | 28   | 2000 | 330.0              | 16.4               | 6.75    | 10.1    | 1.8     | 12.0    | 16.0   | Q1            |
| TRS3243EIRHBR  | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

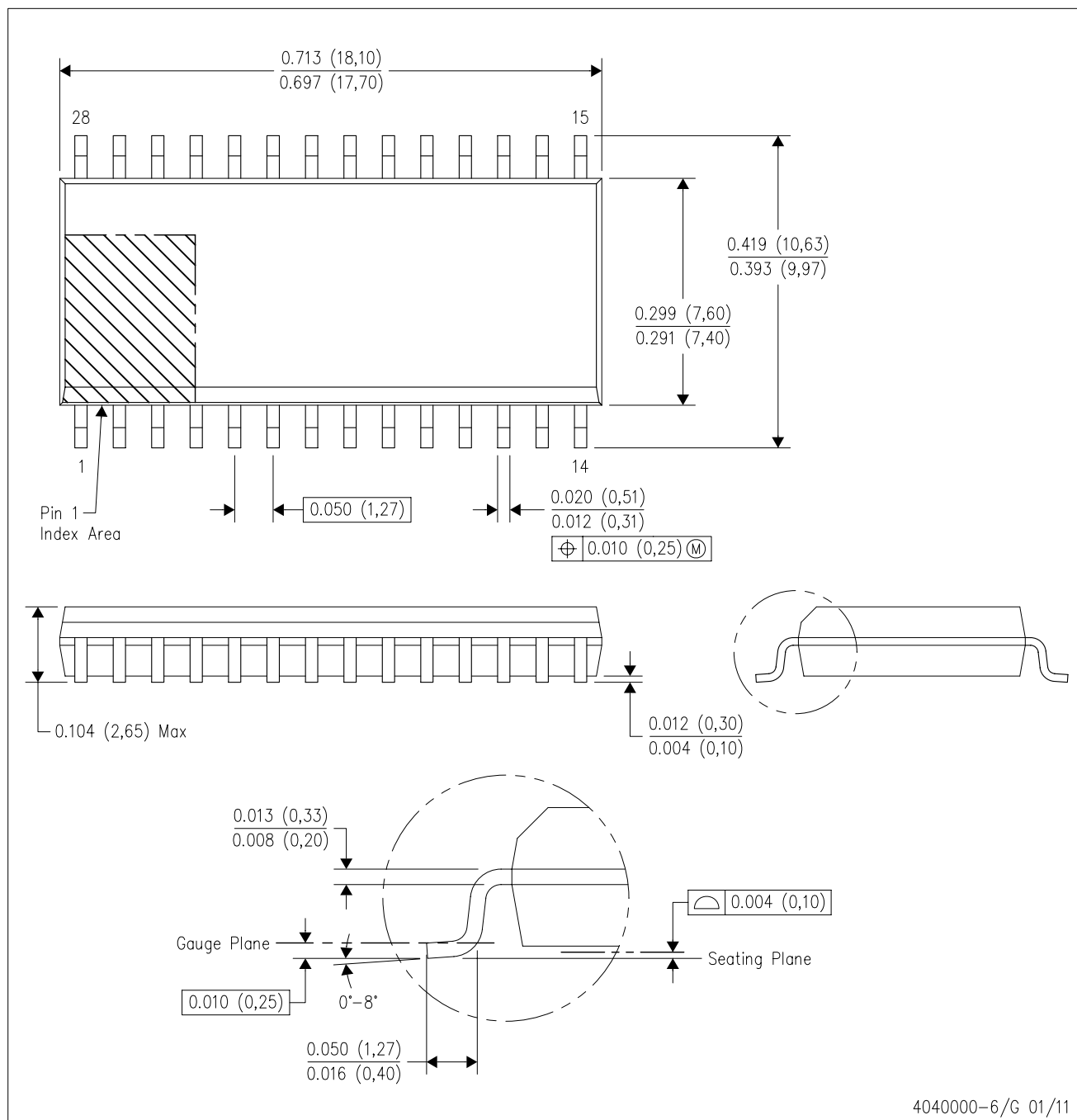


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRS3243ECDDBR  | SSOP         | DB              | 28   | 2000 | 353.0       | 353.0      | 32.0        |
| TRS3243ECDWR   | SOIC         | DW              | 28   | 1000 | 350.0       | 350.0      | 66.0        |
| TRS3243ECPWR   | TSSOP        | PW              | 28   | 2000 | 353.0       | 353.0      | 32.0        |
| TRS3243ECRHBR  | VQFN         | RHB             | 32   | 3000 | 360.0       | 360.0      | 36.0        |
| TRS3243EIDBR   | SSOP         | DB              | 28   | 2000 | 353.0       | 353.0      | 32.0        |
| TRS3243EIDBRG4 | SSOP         | DB              | 28   | 2000 | 353.0       | 353.0      | 32.0        |
| TRS3243EIDWR   | SOIC         | DW              | 28   | 1000 | 350.0       | 350.0      | 66.0        |
| TRS3243EIPWR   | TSSOP        | PW              | 28   | 2000 | 353.0       | 353.0      | 32.0        |
| TRS3243EIRHBR  | VQFN         | RHB             | 32   | 3000 | 360.0       | 360.0      | 36.0        |

DW (R-PDSO-G28)

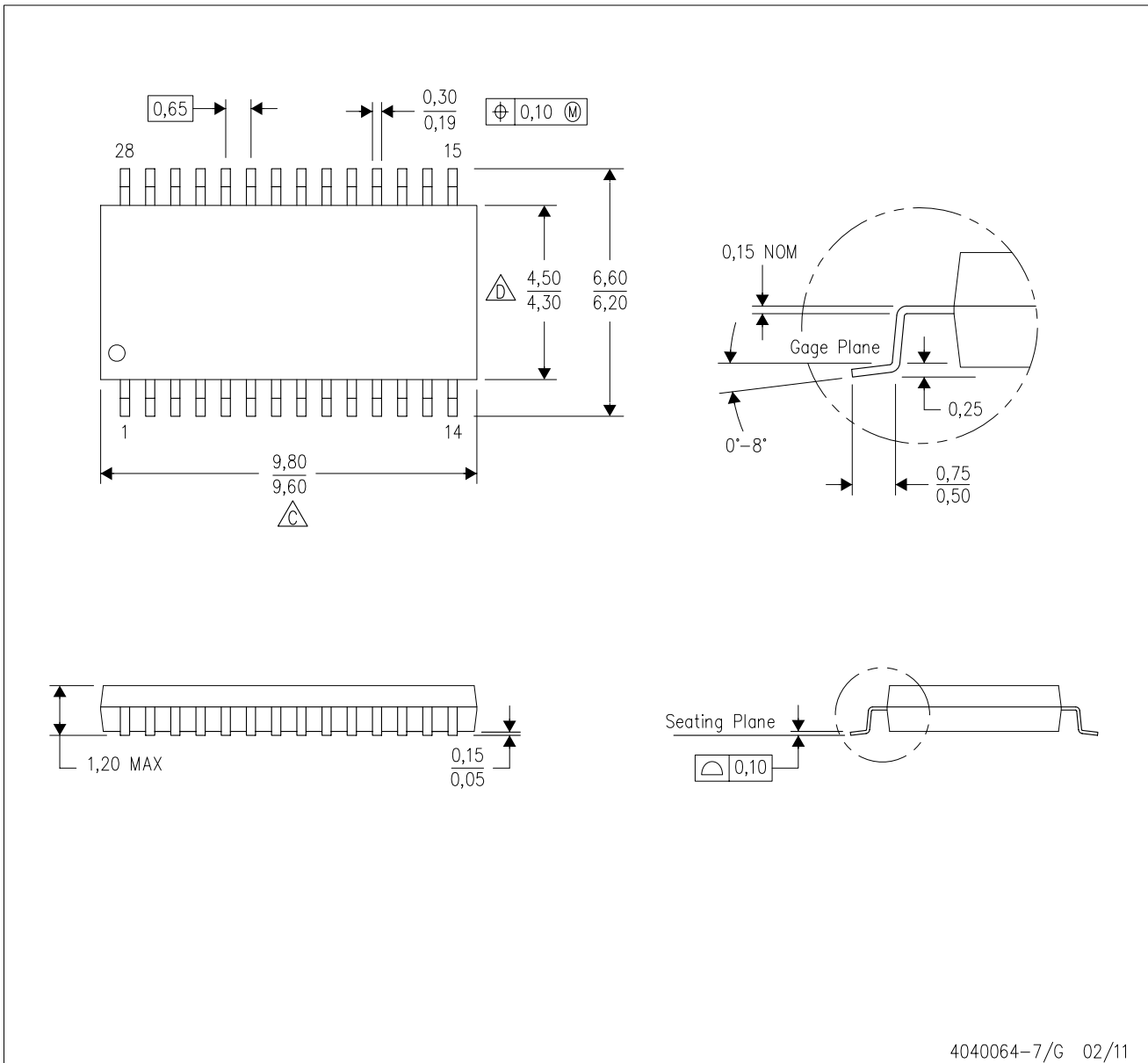
PLASTIC SMALL OUTLINE



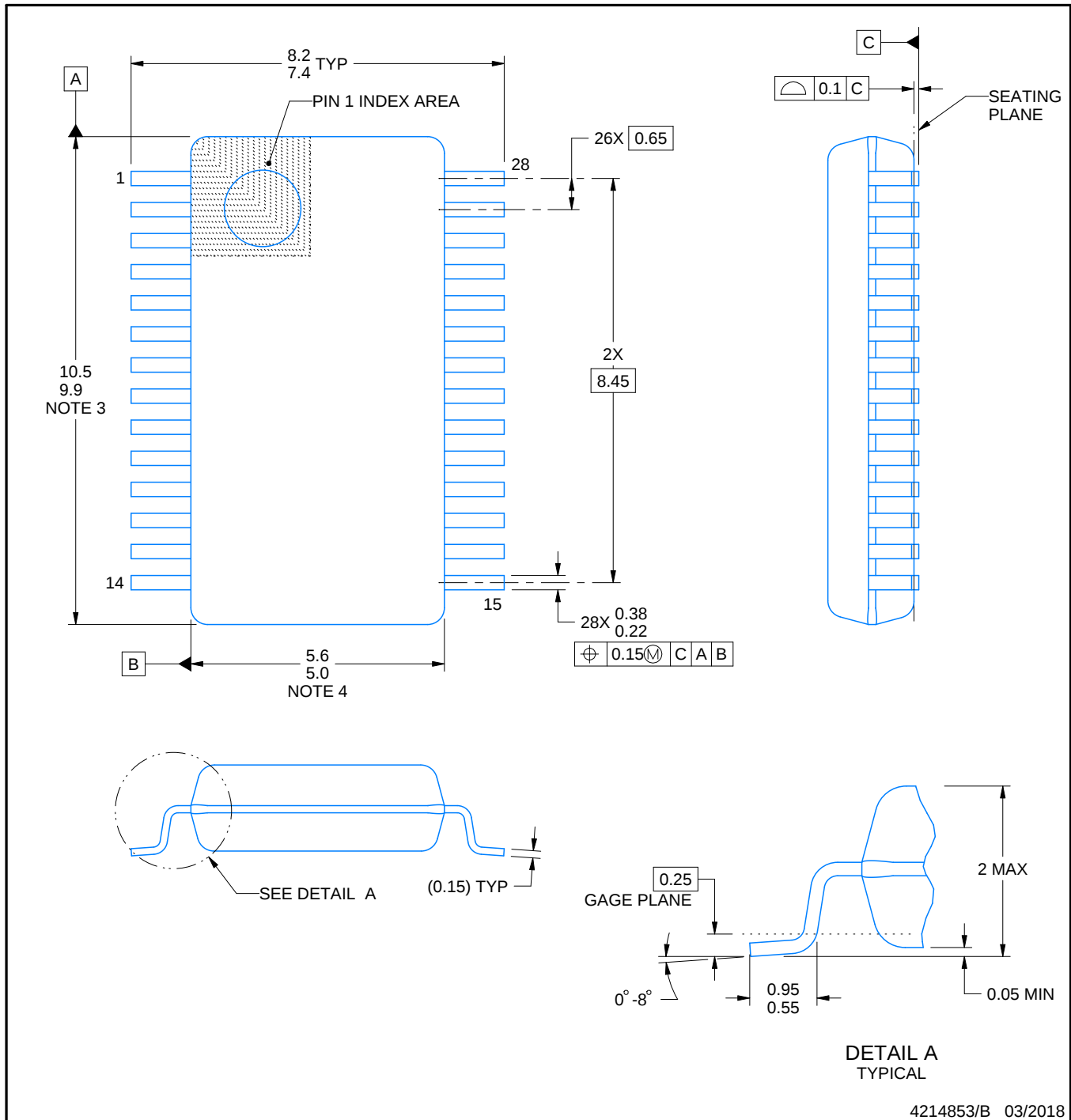
- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AE.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



4214853/B 03/2018

## NOTES:

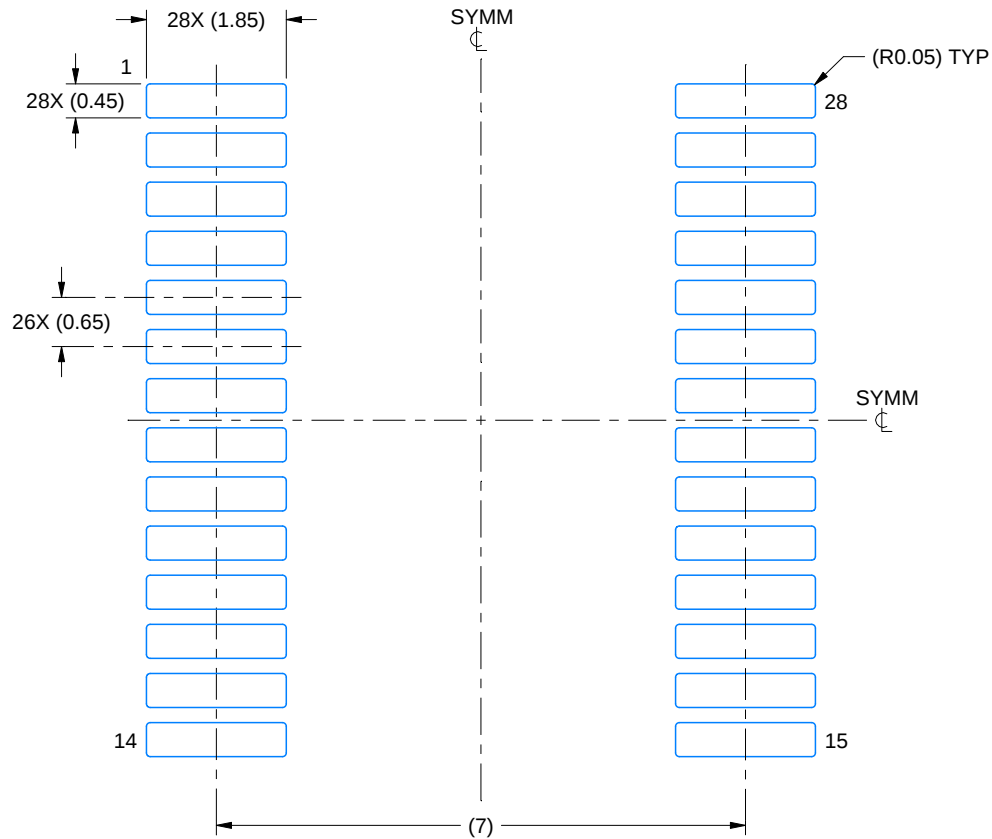
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

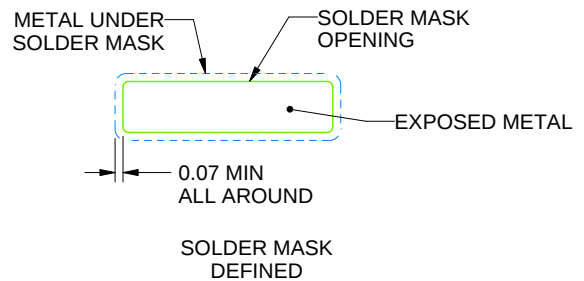
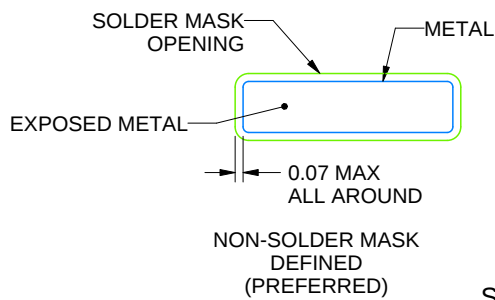
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

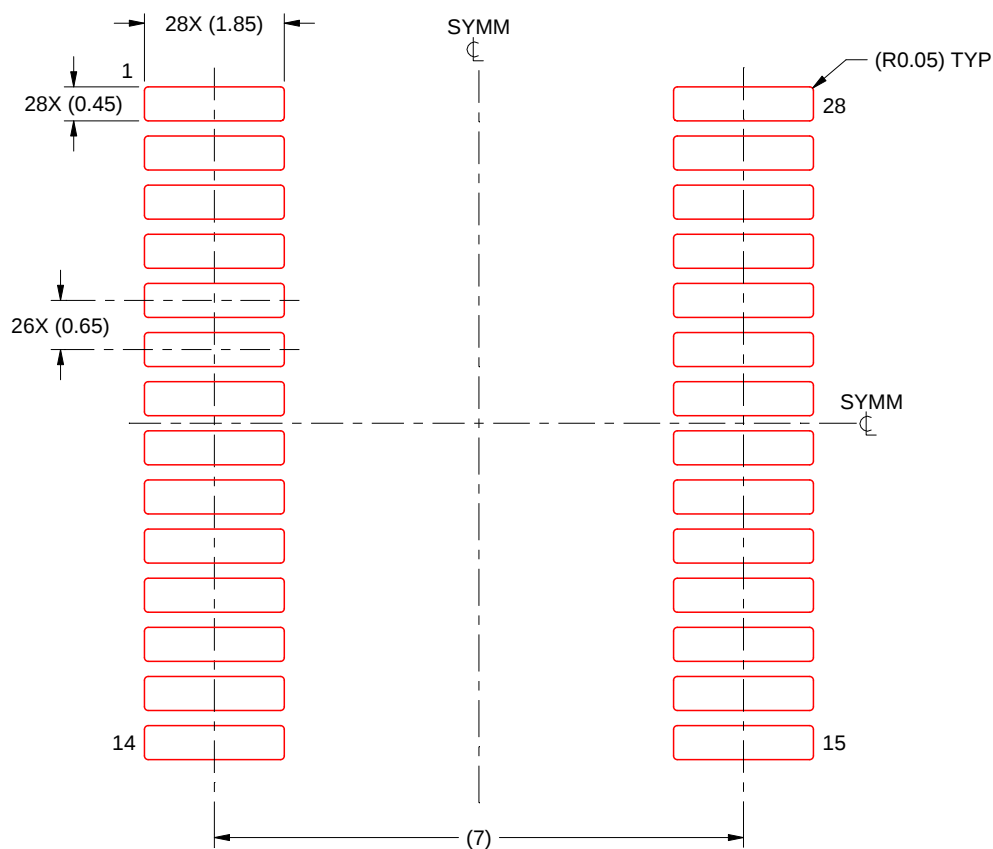
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

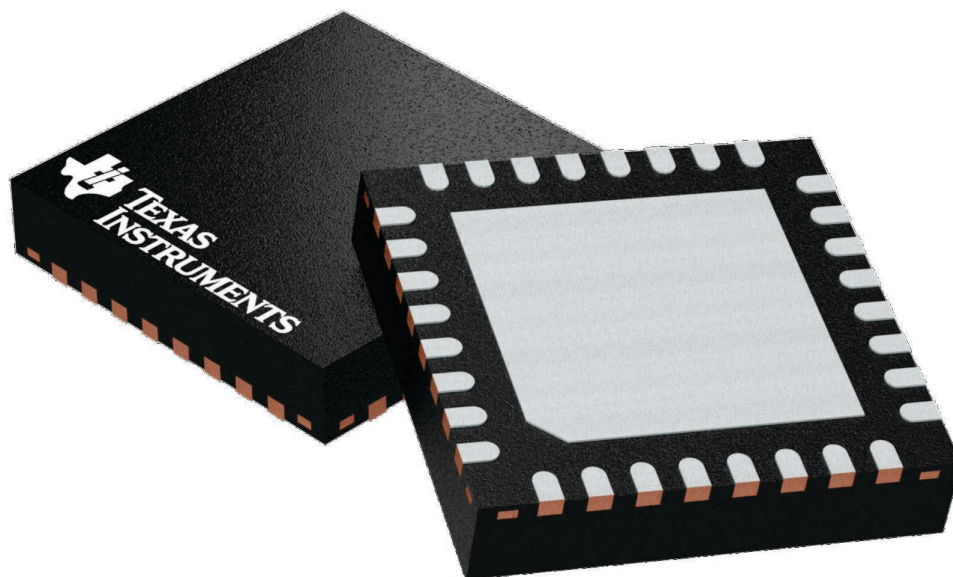
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



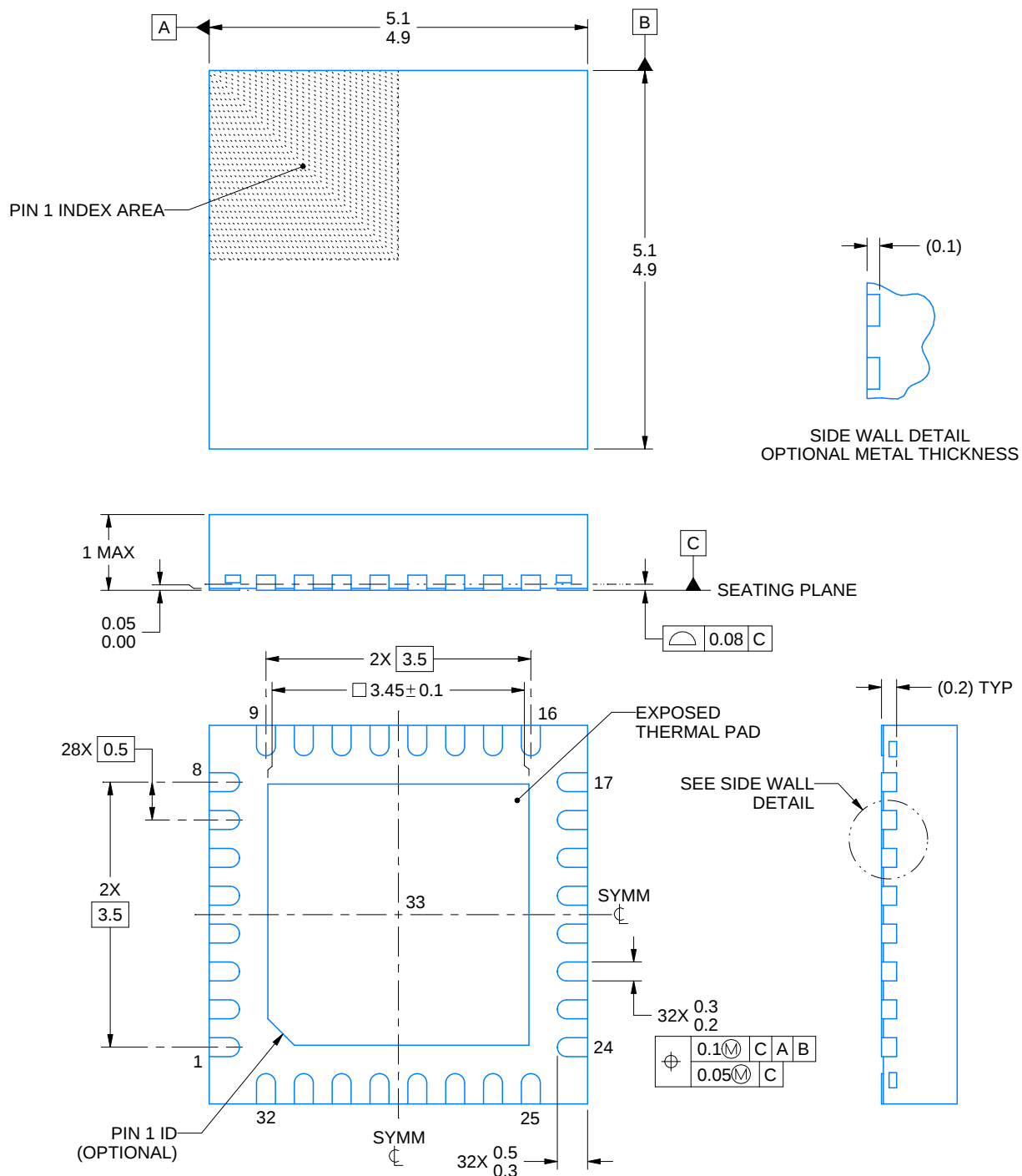
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223442/B 08/2019

NOTES:

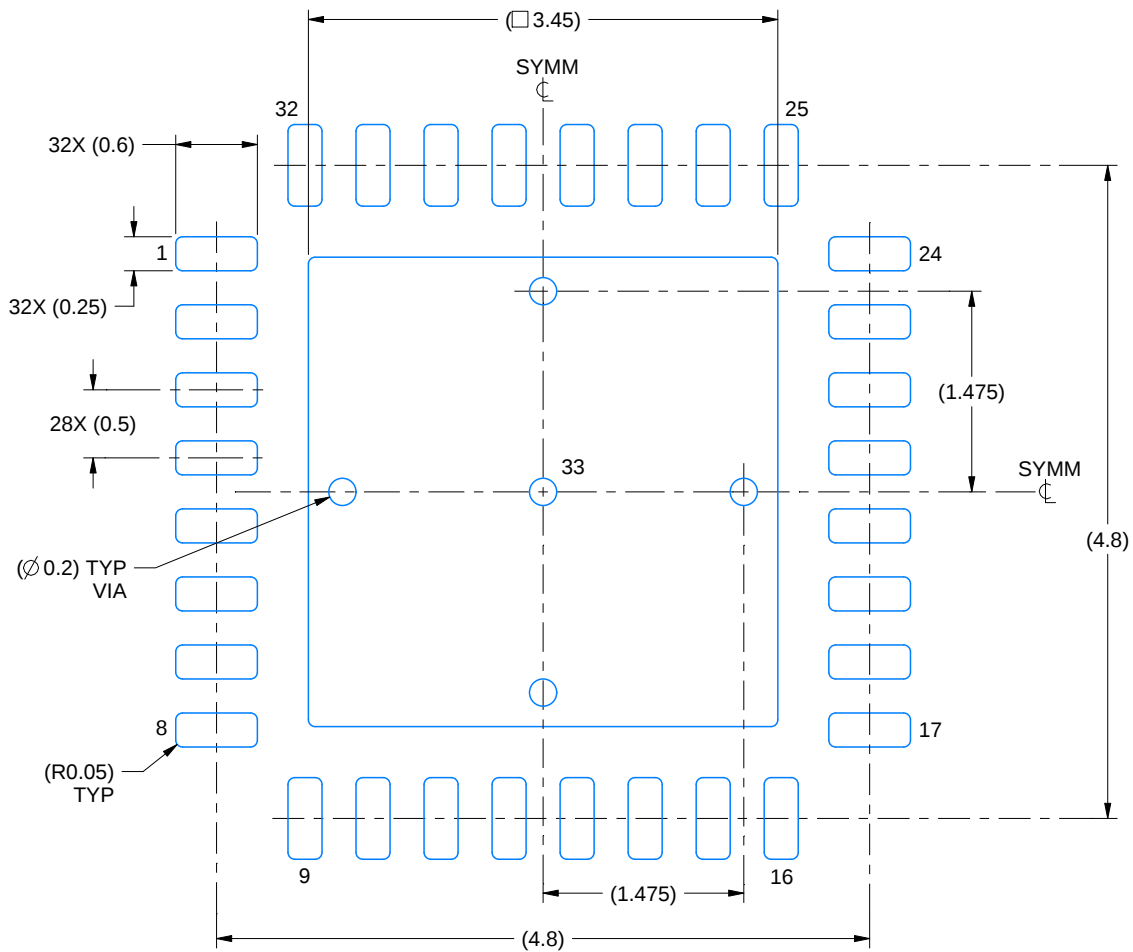
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

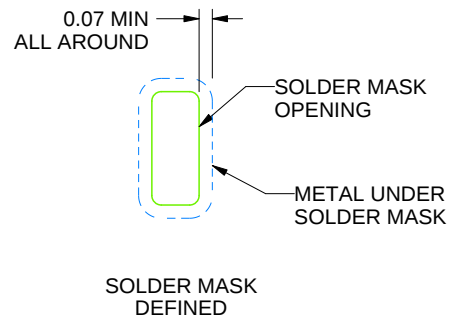
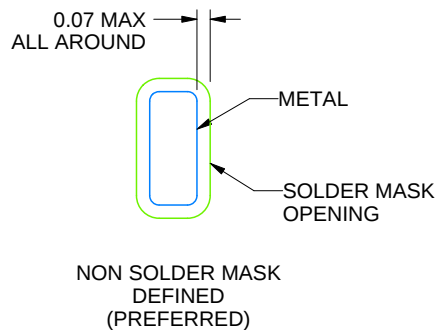
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

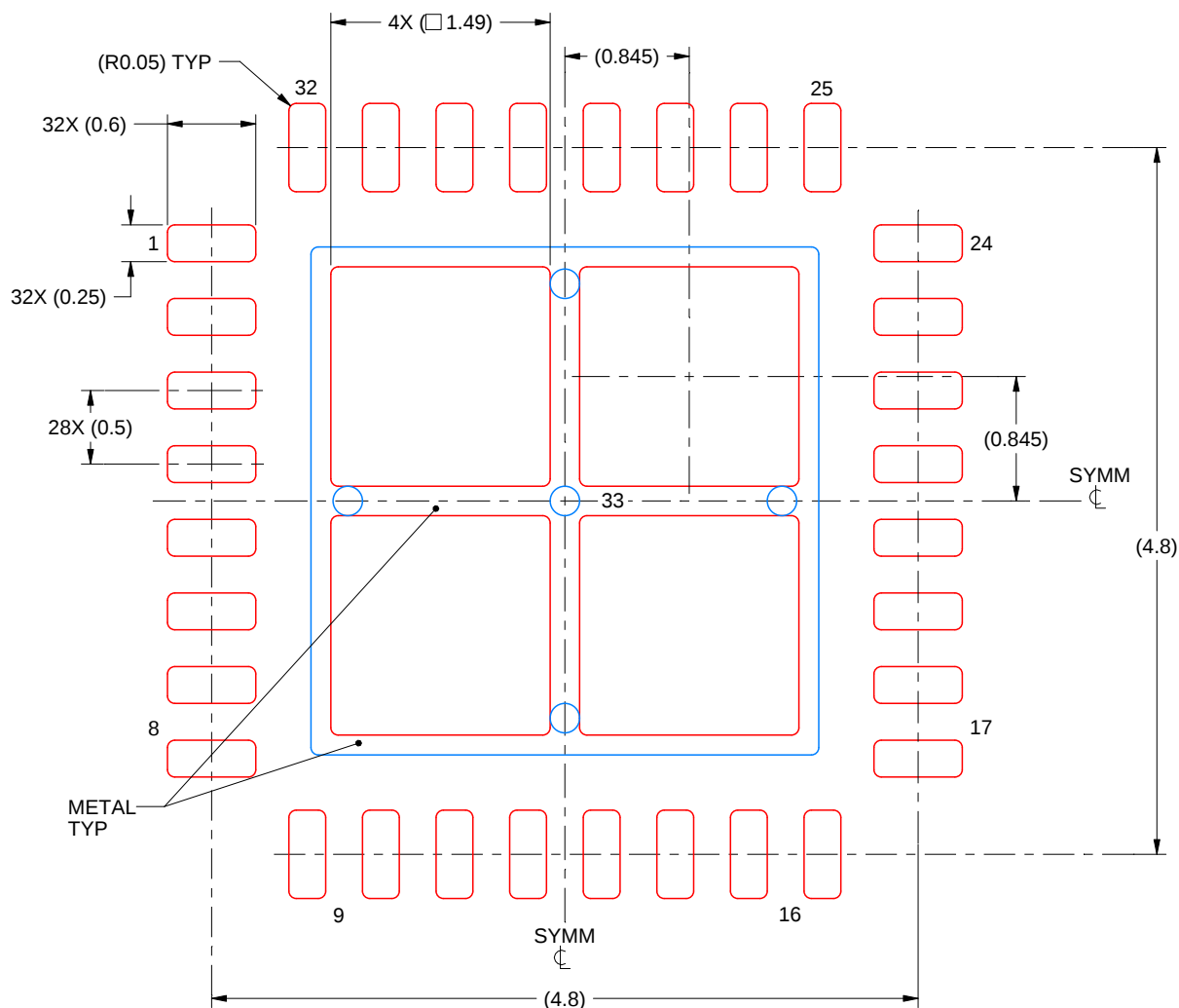
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**RHB0032E**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月