TRSF3232E ±15kV IEC ESD 保護機能搭載、小型パッケージの 3V～5.5V 2 チャネル RS-232 1Mbit/s ライン ドライバ / レシーバ

1 特長

- 3V～5.5V の V_{CC} 電源で動作
- 最大 1Mbit/s で動作
- 低い消費電流:300µA (標準値)
- 外付けコンデンサ:4 × 0.1µF
- 3.3V 電源で 5V ロジック入力を許容
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- RS-232 ピンの ESD 保護
  - ±15kV 人体モデル (HBM)
  - ±15kV IEC 61000-4-2 気中放電
  - ±8kV IEC 61000-4-2 接触放電
- ニア チップ スケール QFN (3mm x 3mm) パッケージで提供 (SOIC-16 より 85% 小型)

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリ駆動システム
- PDA
- ノートブック PC
- パームトップ PC
- ハンドヘルド機器

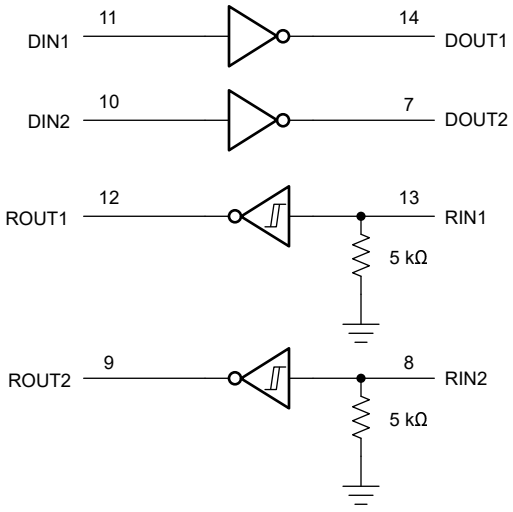
3 概要

TRSF3232E は 2 つのライン ドライバ、2 つのライン レシーバ、1 つのデュアル チャージ ポンプ回路で構成されており、ピン間 (シリアル ポート接続ピン、GND を含む) に ±15kV の ESD 保護機能を備えています。このデバイスは、非同期通信コントローラとシリアルポート コネクタの間の電気的インターフェイスとして機能します。チャージ ポンプと 4 つの小さな外付けコンデンサにより、3V～5.5V の単一電源で動作できます。TRSF3232E は最大 1Mbit/s のデータ信号速度、14V/µs～150V/µs のドライバ出力スルーレートで動作します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TRSF3232E	D (SOIC)	9.9 mm × 6mm
	DB (SSOP)	6.2 mm × 7.8mm
	DW (SOIC)	10.3 mm × 10.3mm
	PW (TSSOP)	5 mm × 6.4mm
	RGT (VQFN)	3 mm × 3mm
	SOT-23-THN (DYY) (16)	4.2mm × 2mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



論理図 (正論理)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

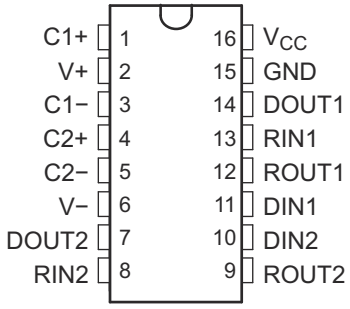


図 4-1. D, DB, DW, PW or DYY Package 16-Pin SSOP, TSSOP, or SOT-23-THN (Top View)

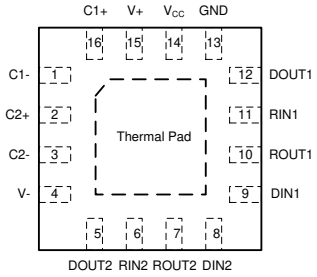


図 4-2. RGT, VQFN Package (Top View)

表 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	D, DB, DW, PW or DYY	RGT		
C1+	1	16	-	Positive lead of C1 capacitor
V+	2	15	O	Positive charge pump output for storage capacitor only
C1-	3	1	-	Negative lead of C1 capacitor
C2+	4	2	-	Positive lead of C2 capacitor
C2-	5	3	-	Negative lead of C2 capacitor
V-	6	4	O	Negative charge pump output for storage capacitor only
DOUT2	7	5	O	RS232 line data output (to remote RS232 system)
RIN2	8	6	I	RS232 line data input (from remote RS232 system)
ROUT2	9	7	O	Logic data output (to UART)
DIN2	10	8	I	Logic data input (from UART)
DIN1	11	9	I	Logic data input (from UART)
ROUT1	12	10	O	Logic data output (to UART)
RIN1	13	11	I	RS232 line data input (from remote RS232 system)
DOUT1	14	12	O	RS232 line data output (to remote RS232 system)
GRD	15	13	-	Ground
V_{CC}	16	14	-	Supply Voltage, Connect to external 3-V to 5.5-V power supply
Thermal Pad	-	Thermal Pad	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) see note (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive-output supply voltage range(2)		–0.3	7	V
V–	Negative-output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Drivers	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1].	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

5.3 ESD Protection, Driver

PIN NAME	TEST CONDITIONS	TYP	UNIT
DOUT1, DOUT2(2)	Human-body model (HBM)	±15	kV
	IEC 61000-4-2 Air-Gap Discharge(1)	±15	
	IEC 61000-4-2 Contact Discharge(1)	±8	

(1) For RGT, D and PW packages only: A minimum of 1-µF capacitor is needed between V_{CC} and GND to meet the specified IEC ESD level .
(2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 ESD Protection, Receiver

PIN NAME	TEST CONDITIONS	TYP	UNIT
RIN1, RIN2(2)	HBM	±15	kV
	IEC 61000-4-2 Air-Gap Discharge (1)	±15	
	IEC 61000-4-2 Contact Discharge (1)	±8	

(1) For RGT, D and PW packages only:A minimum of 1-µF capacitor is needed between V_{CC} and GND to meet the specified IEC ESD level.
(2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

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5.5 Recommended Operating Conditions

See note (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver low-level input voltage		DIN			0.8	V
V_I	Driver input voltage		DIN	0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature		TRSF3232EI	–40		85	°C
			TRSF3232EC	0		70	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see 図 8-1).

5.6 Thermal Information

THERMAL METRIC(1)		TRSF3232E						UNIT
		PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)	RGT (VQFN)	DYY (SOT-23-THN)	
		16 Pins	16 Pins	16 Pins	16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.2	85.9	57	46	48.8	106.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (bottom) thermal resistance	39.0	43.1	33.5	36.2	55.8	47.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	44.5	37.1	43.8	23.2	44.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	10.1	7.5	4.2	1.7	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	44.1	37.1	42.9	23.2	43.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	9.0	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.7 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load,	V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see 図 8-1).
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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5.8 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.5		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	μA
I_{OS} (3)	Short-circuit output current	V_{CC} = 3.6 V, V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V, V_O = 0 V	RGT package only		±35	±60	
			D, DB, DW, PW packages		±35	±90	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V (see 図 8-1).
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

5.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V (see 図 8-1).
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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5.10 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
	Maximum data rate (see 図 6-1)	R_L = 3 kΩ, One DOUT switching	C_L = 250 pF,V_{CC} = 3 V to 4.5 V	1000			kbit/s
			C_L = 1000 pF,V_{CC} = 3.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew[3]	C_L = 1000 pF, R_L = 3 kΩ, V_{cc}= 5 V (see 図 6-2)	RGT package only		70		ns
		C_L = 150 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ (see 図 6-2)	D, DB, DW, PW packages		300		
SR(tr)	Slew rate, transition region (see 図 6-1)	R_L = 3 kΩ to 7 kΩ, C_L = 150 pF to 1000 pF, V_{CC} = 3.3 V		14		150	V/µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see 図 8-1).
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.11 Switching Characteristics, Reveiver

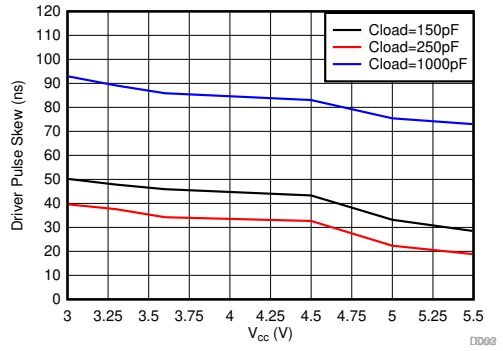
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF	RGT package		85		ns
			D, DB, DW, PW packages		300		
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF	RGT package		110		ns
			D, DB, DW, PW packages		300		
$t_{sk(p)}$	Pulse skew[3]	RGT package			25		ns
		D, DB, DW, PW packages			300		

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V (see 図 8-1).
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

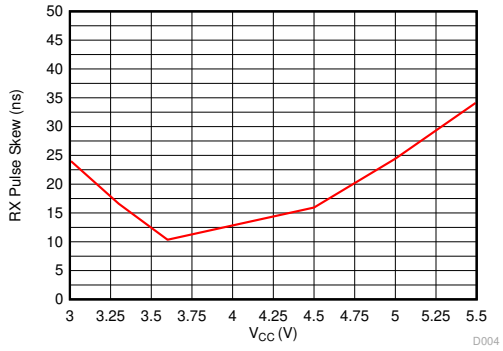
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5.12 Typical Characteristics



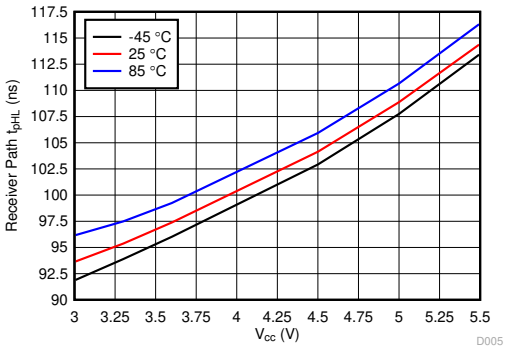
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図 5-1. Driver pulse skew at T_A = 25°C (RGT package)



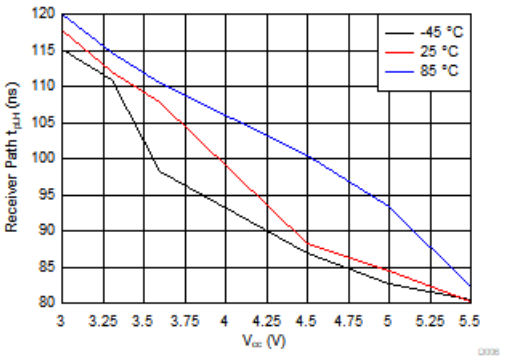
D004_SLLS825.grf

図 5-2. Receiver path skew at T_A = 25°C (t_{pHL}-t_{pLH}) (RGT package)



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図 5-3. Receiver path high-to-low propagation delay, C_L = 150pF (RGT package)

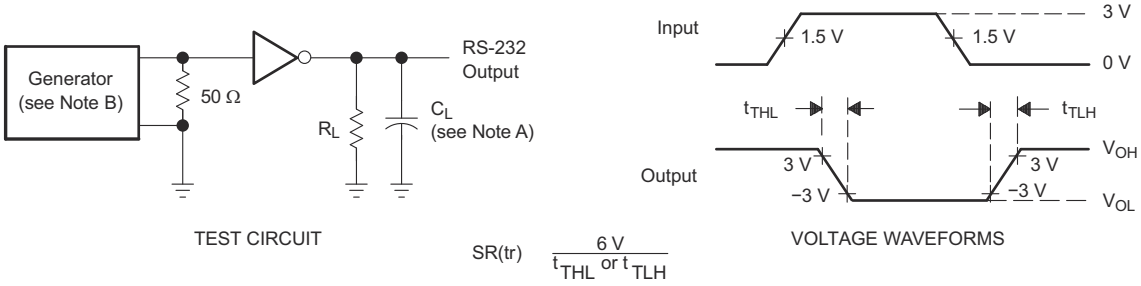


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図 5-4. Receiver path low-to-high propagation delay, C_L = 150pF (RGT package)

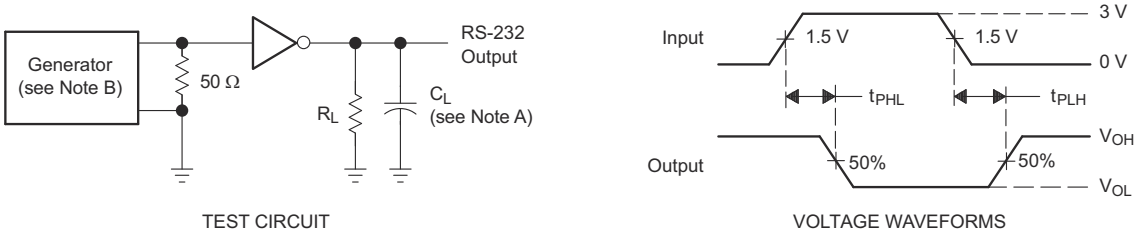
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6 Parameter Measurement Information



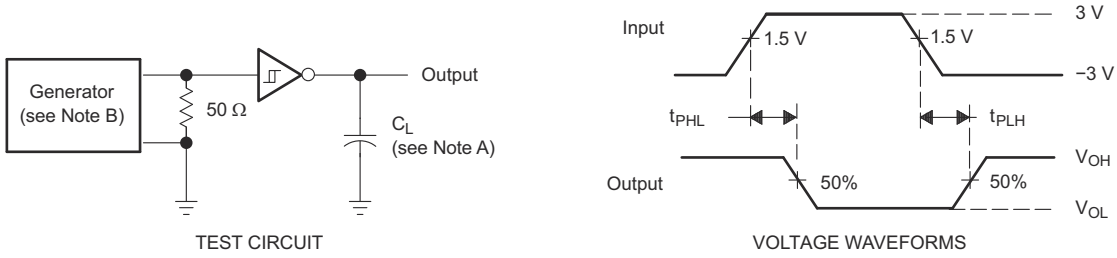
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

図 6-1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

図 6-2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

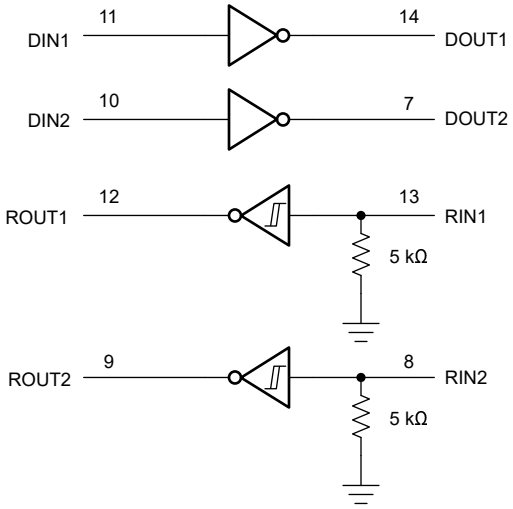
図 6-3. Receiver Propagation Delay Times

7 Detailed Description

7.1 Overview

The TRSF3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15kV IEC ESD protection between serial-port connection terminals and GND. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3V to 5.5V supply. The device operates at data signaling rates up to 1Mbps and a maximum of 150V/µs driver output slew rate. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

7.3.2 RS232 Driver

Two drivers interface the standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

7.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

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7.4 Device Functional Modes

表 7-1. Each Driver

INPUT DIN(1)	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 7-2. Each Receiver

INPUT RIN(1)	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

7.4.1 V_{CC} Powered by 3V to 5.5V

The device is in normal operation.

7.4.2 V_{CC} Unpowered, V_{CC} = 0V

When the TRS3232 device is unpowered, it can be safely connected to an active remote RS232 device.

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8 Application and Implementation

注

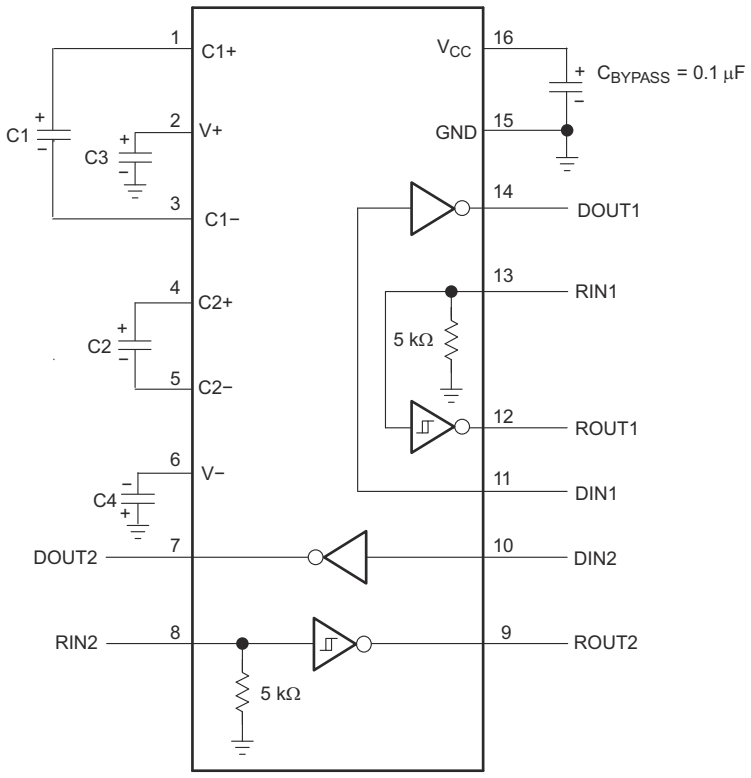
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8.1 Application Information

The TRSF3232E device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa. This device can be used in any application where an RS232 line driver or receiver is required.

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.

8.2 Typical Application



A. C3 can be connected to V_{CC} or GND.

図 8-1. Typical Operating Circuit and Capacitor Values

表 8-1. VCC vs Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3V ± 0.3V	0.1µF	0.1µF
5V ± 0.5V	0.047µF	0.33µF
3V to 5.5V	0.1µF	0.47µF

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8.2.1 Design Requirements

- Recommended V_{CC} is 3.3V or 5V
  - 3V to 5.5V is also possible
- Maximum recommended bit rate is 250kbites

8.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels. Select capacitor values based on VCC level for best performance.

8.2.3 Application Performance Plots

VCC must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using 表 8-1

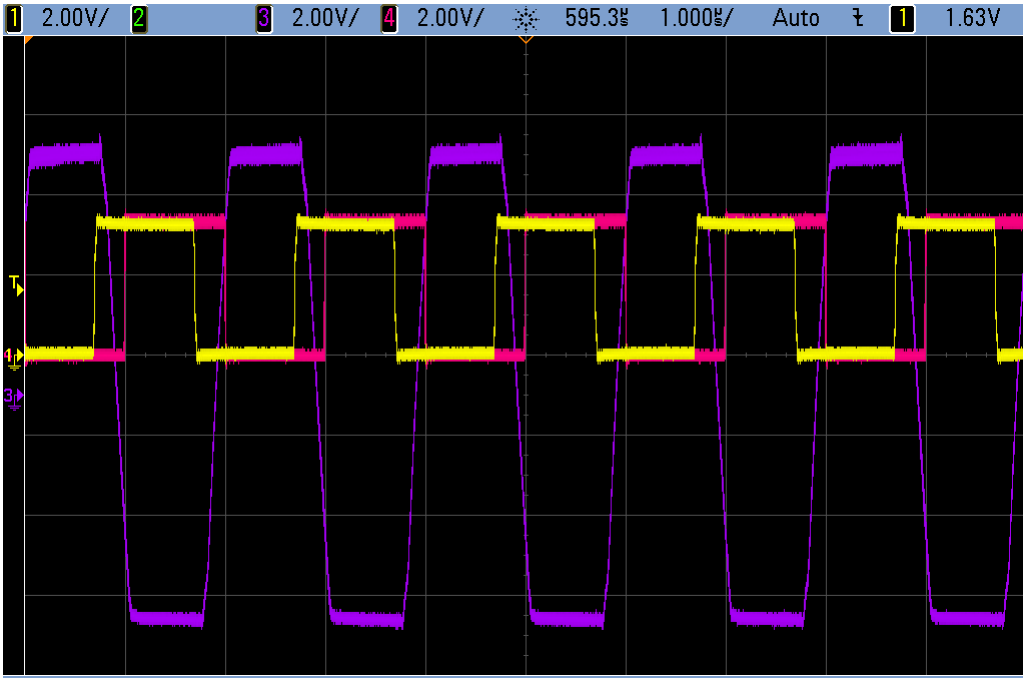


図 8-2. 1Mbps timing waveform from driver input to receiver output loopback. DOUT to RIN trace is in purple, DIN trace is in yellow and ROUT trace is in pink

8.3 Power Supply Recommendations

The supply voltage, V_{CC}, should be between 3V and 5.5V. Select the charge-pump capacitors using 表 8-1.

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

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8.4.2 Layout Example

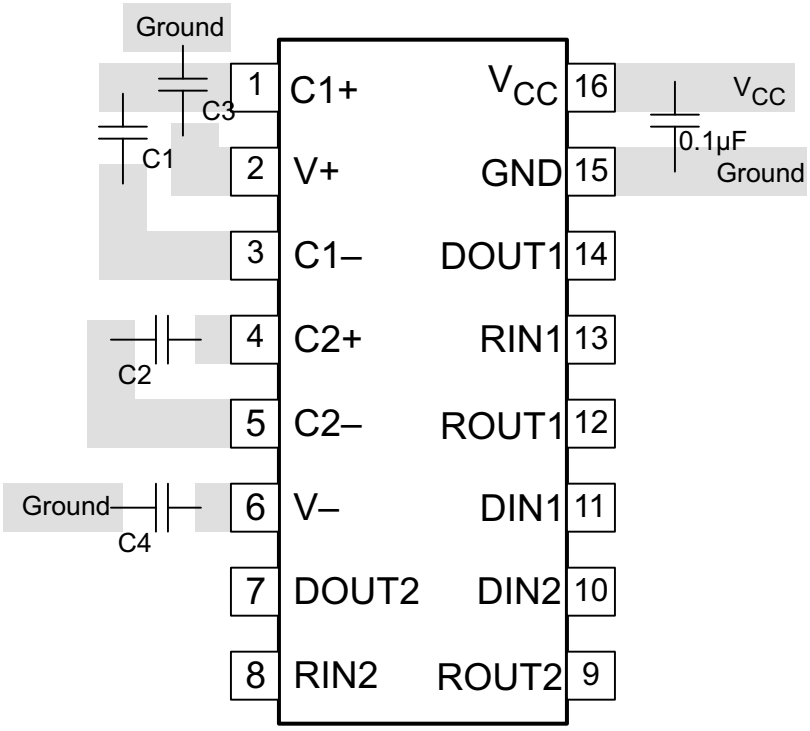


図 8-3. Layout Diagram

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2021) to Revision C (December 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更	1
• データシートに SOT-23-THN (DYY) パッケージを追加	1
• Added Note 2 to the *ESD Protection, Driver*	4
• Added Note 2 to the *ESD Protection, Receiver*	4

Changes from Revision A (December 2020) to Revision B (June 2021)	Page
• 以下の「アプリケーション」を追加。産業用 PC、有線ネットワーク、データ・センターおよびエンタープライズ・コンピューティング	1
• Changed the table note in the *ESD Protection, Driver* table to make it applicable to D and PW packages	4
• Changed the table note in the *ESD Protection, Reciever* table to make it applicable to D and PW packages	4
• Changed the thermal parameter values for D and PW packages in the *Thermal Information* table	5

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Changes from Revision * (August 2007) to Revision A (December 2020) **Page**

- 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- Added Note to the *ESD Protection, Driver* 4
- Added Note to the *ESD Protection, Receiver* 4
- Added $t_{sk(p)}$ row for RGT package in the *Switching Characteristics, Driver* 7
- Added t_{PLH} and t_{PHL} rows for RGT package in the *Switching Characteristics, Reveiver* 7
- Added $t_{sk(p)}$ row for RGT package in the *Switching Characteristics, Reveiver* 7

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、指定のデバイスに使用できる最新のデータです。このデータは、予告なく、このドキュメントを改訂せずに変更される場合があります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRSF3232ECDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT32EC
TRSF3232ECDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT32EC
TRSF3232ECDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRSF3232EC
TRSF3232ECDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRSF3232EC
TRSF3232ECDWR	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	TRSF3232EC
TRSF3232ECPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	RT32EC
TRSF3232ECPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT32EC
TRSF3232EID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	TRSF3232EI
TRSF3232EIDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3232EI
TRSF3232EIDYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIDYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT32EI
TRSF3232EIRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	F3232
TRSF3232EIRGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	F3232

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

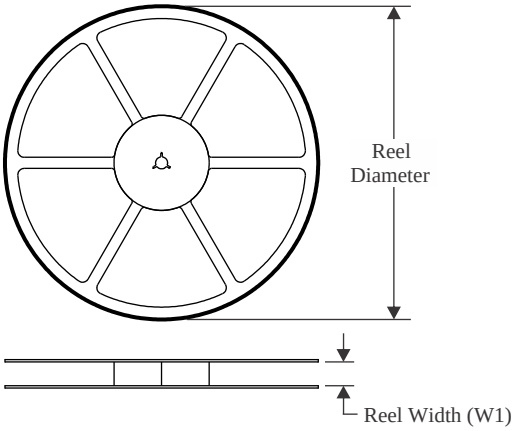
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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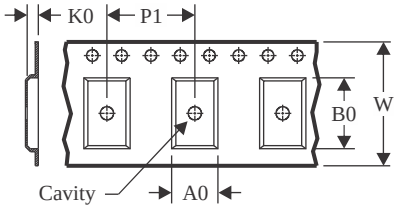
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

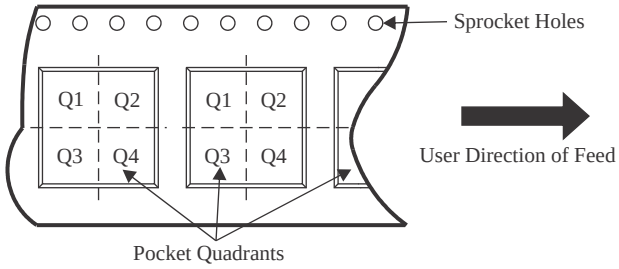


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

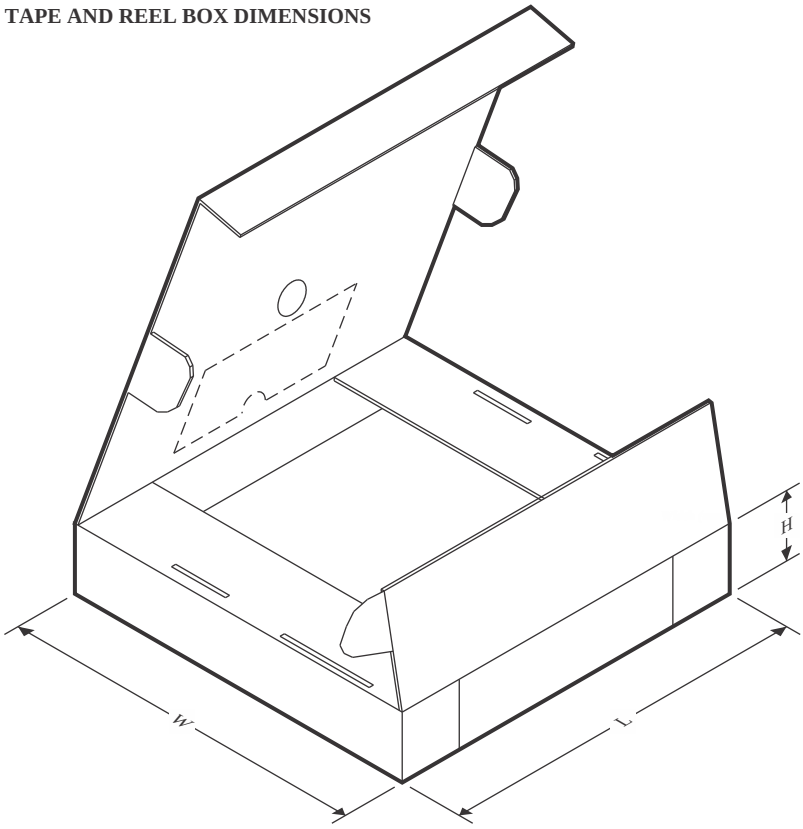
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRSF3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
TRSF3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRSF3232EIDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRSF3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRSF3232EIDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TRSF3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3232EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3232EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

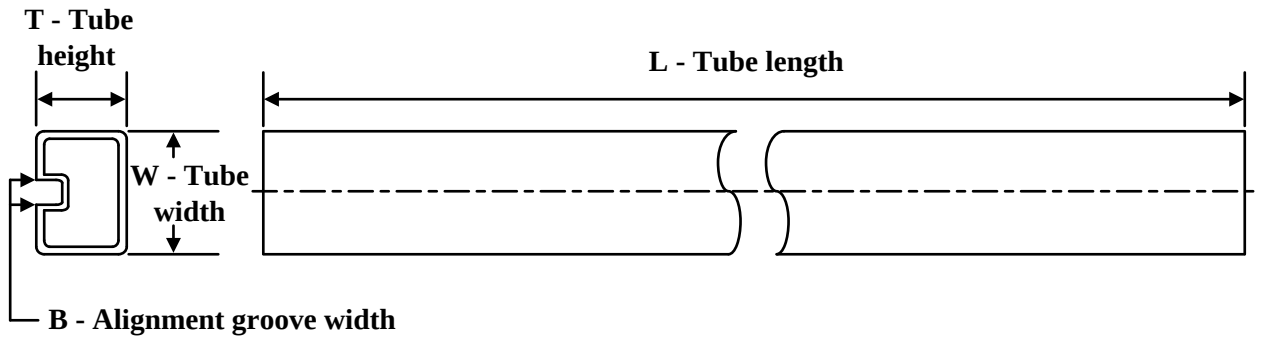
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3232ECDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRSF3232ECDR	SOIC	D	16	2500	353.0	353.0	32.0
TRSF3232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRSF3232ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3232EIDBR	SSOP	DB	16	2000	353.0	353.0	32.0
TRSF3232EIDR	SOIC	D	16	2500	353.0	353.0	32.0
TRSF3232EIDRG4	SOIC	D	16	2500	353.0	353.0	32.0
TRSF3232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRSF3232EIDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TRSF3232EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3232EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TRSF3232EIPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
TRSF3232EIRGTR	VQFN	RGT	16	3000	360.0	360.0	36.0

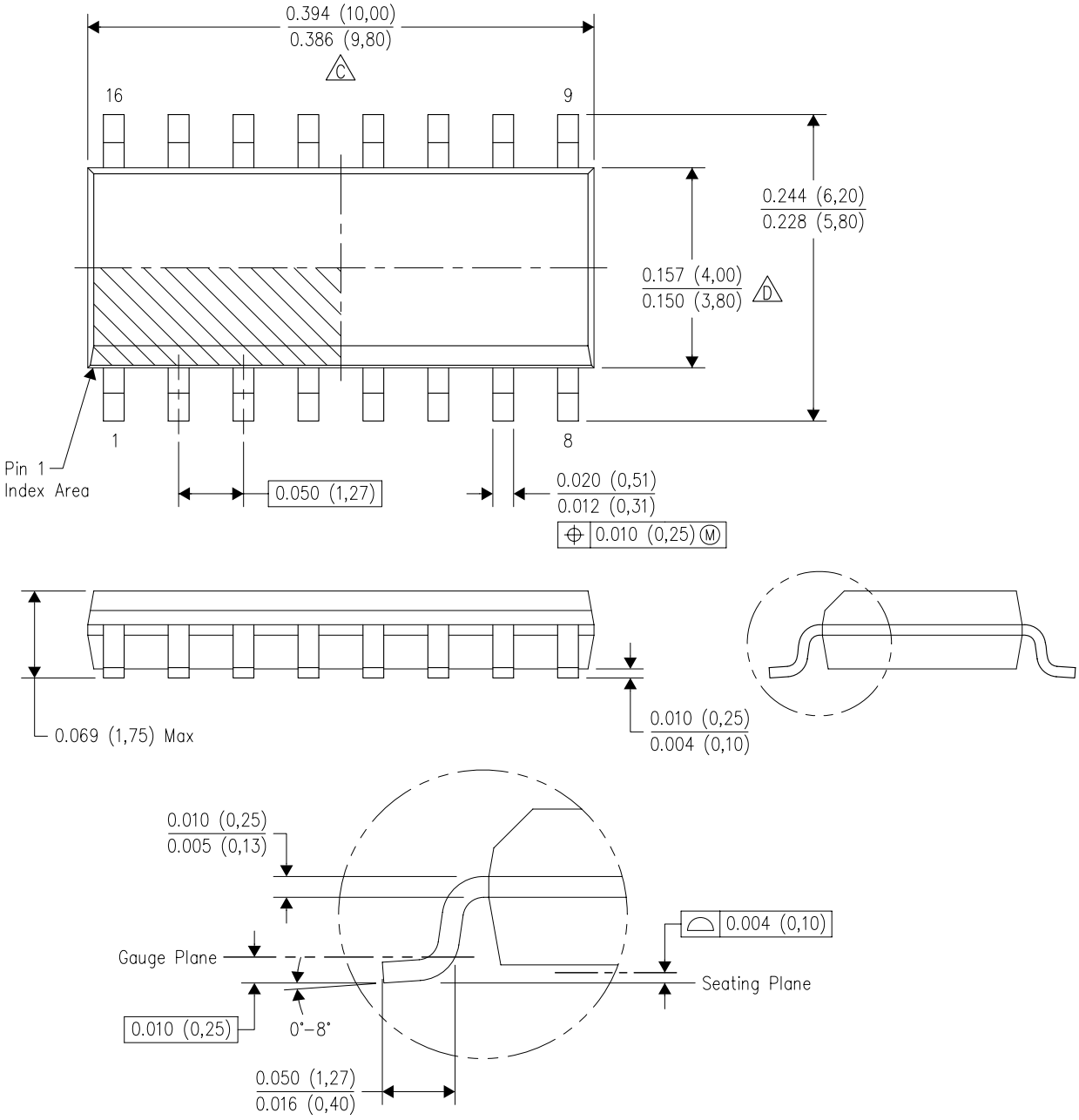
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TRSF3232EIDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TRSF3232EIDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



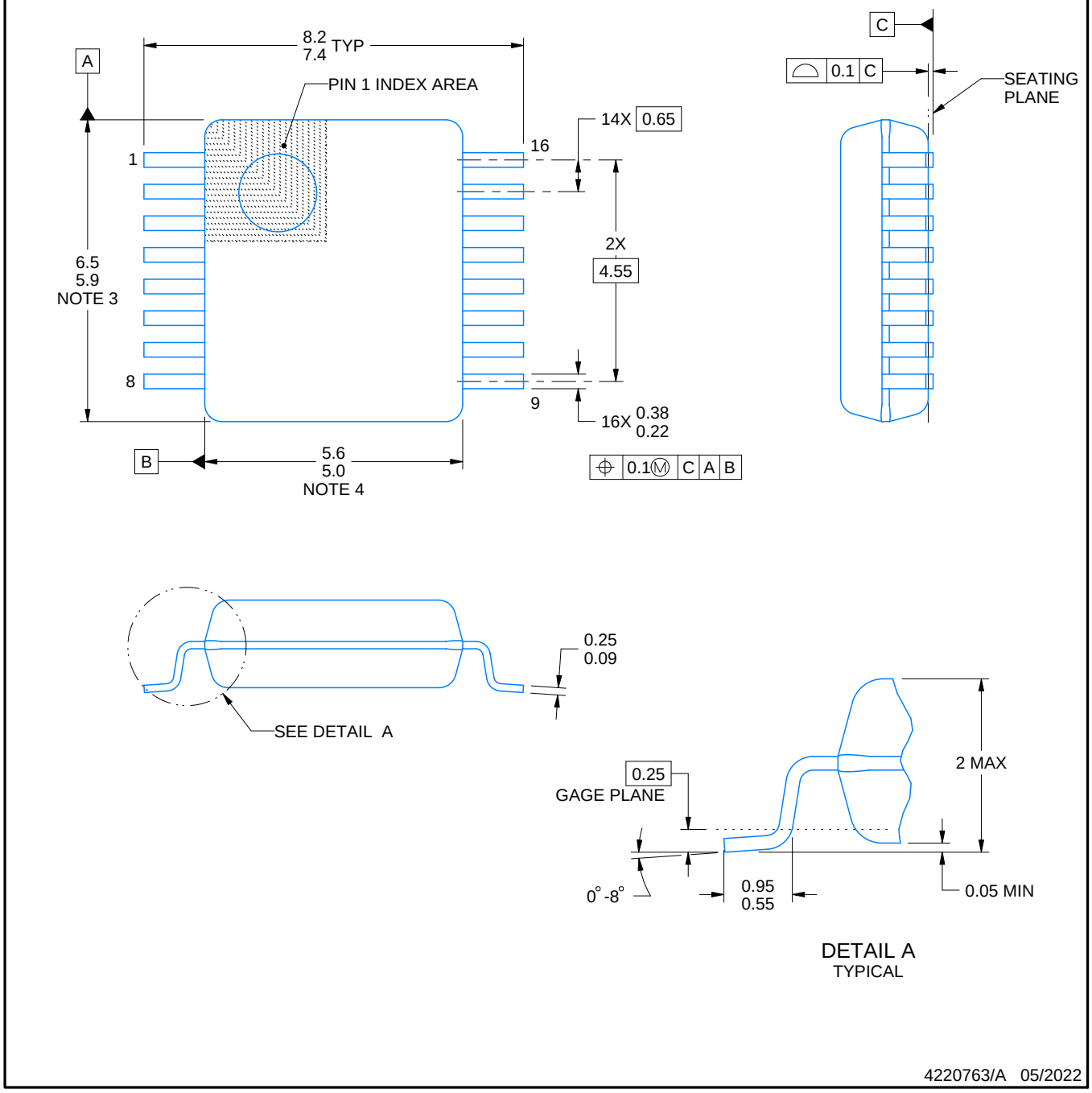
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

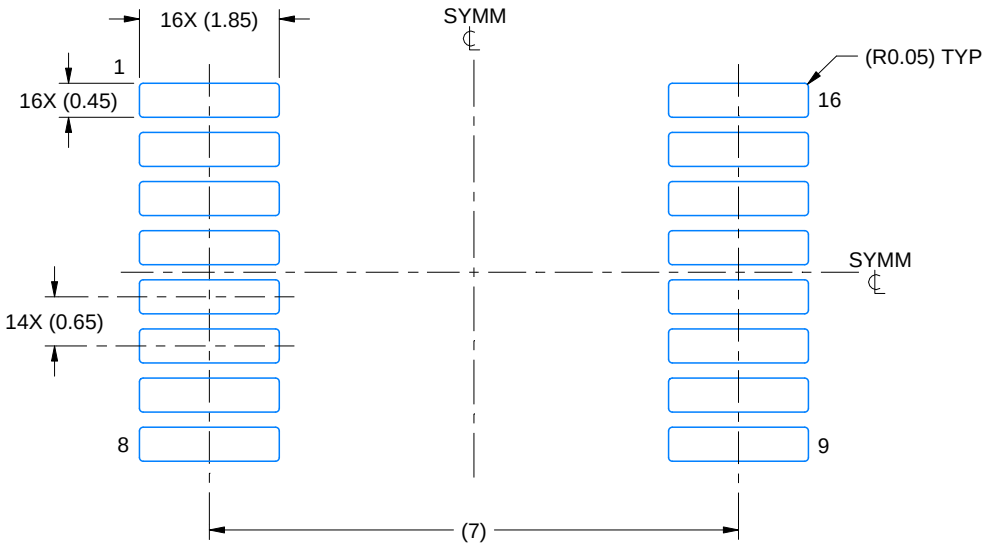
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

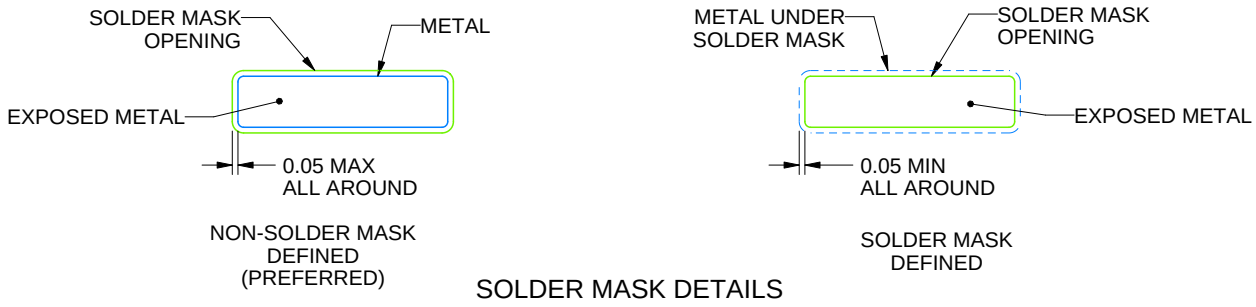


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

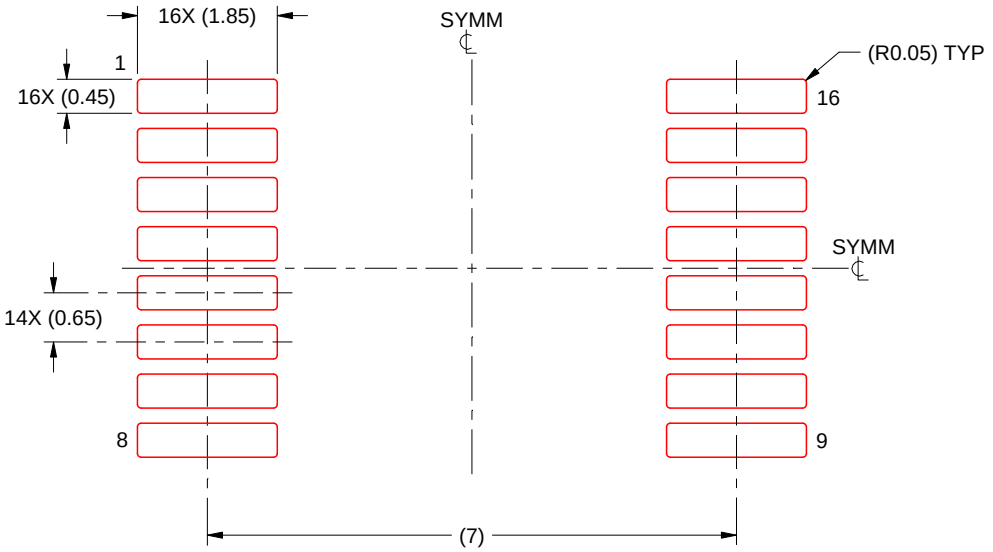


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

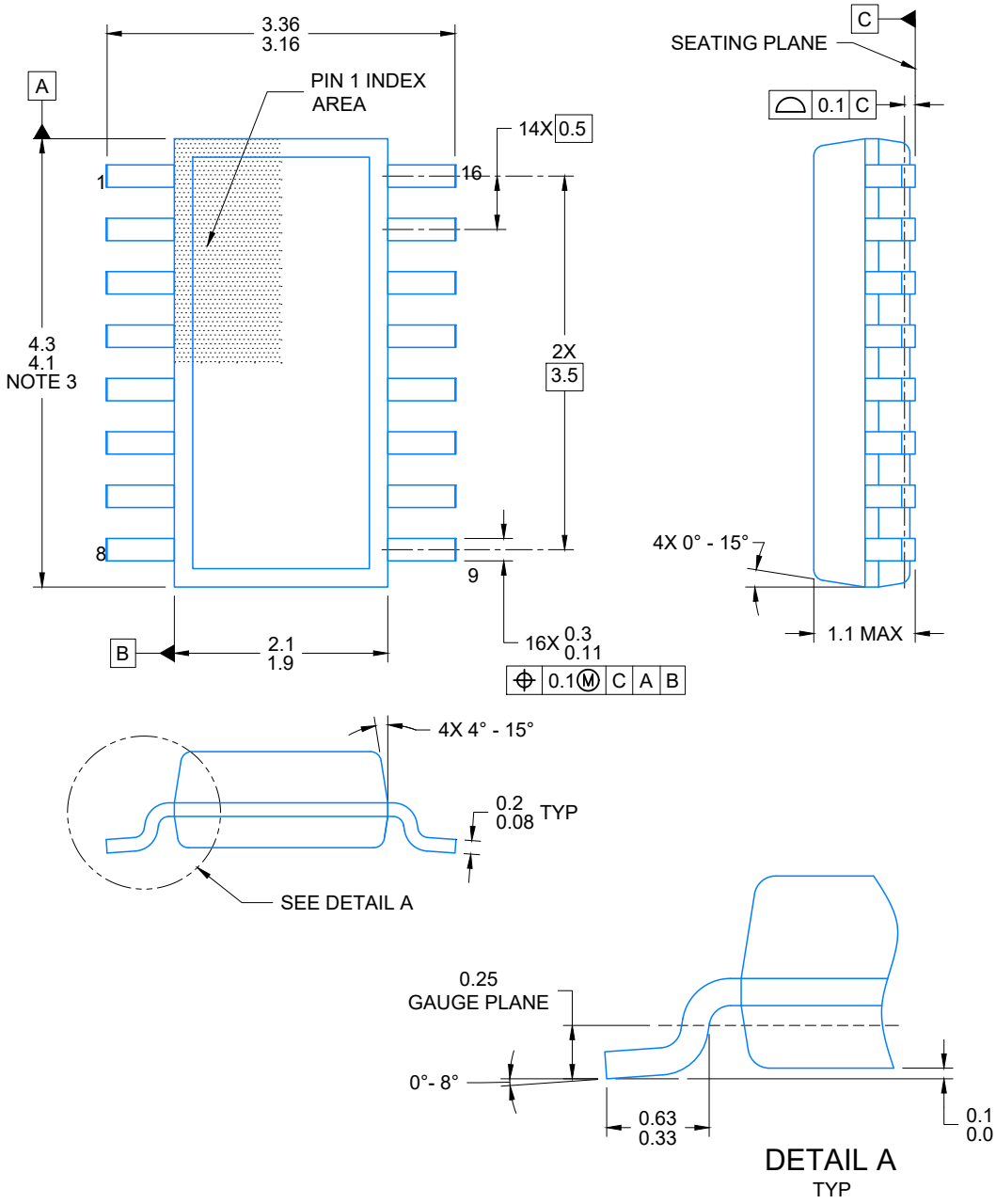
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0016A

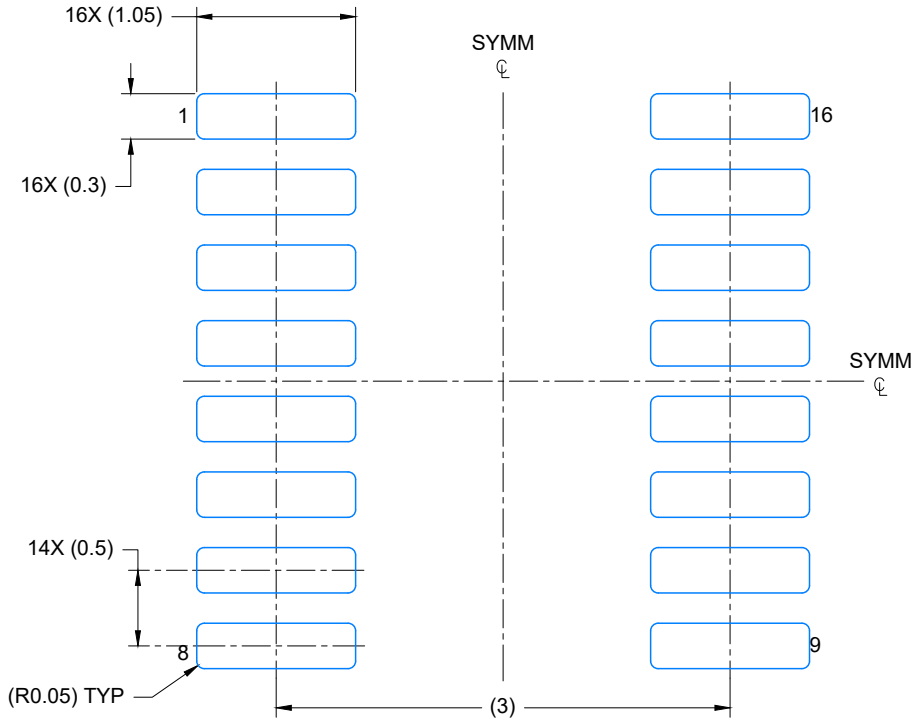
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

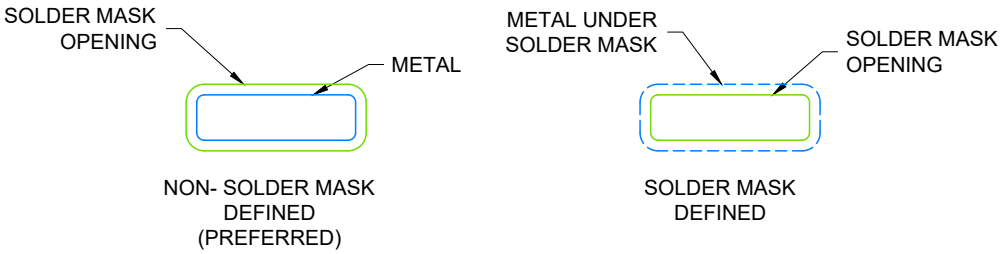


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

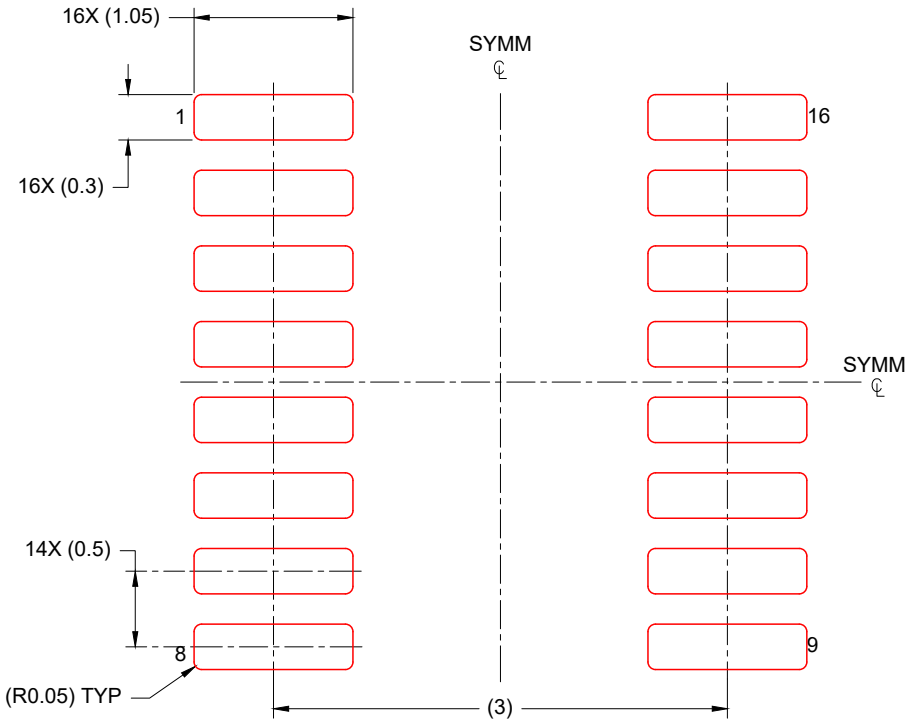
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

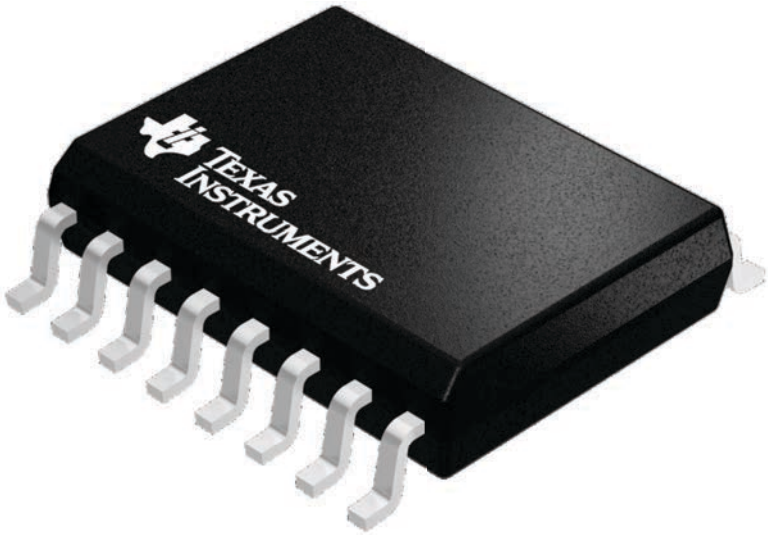
DW 16

SOIC - 2.65 mm max height

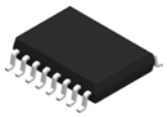
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

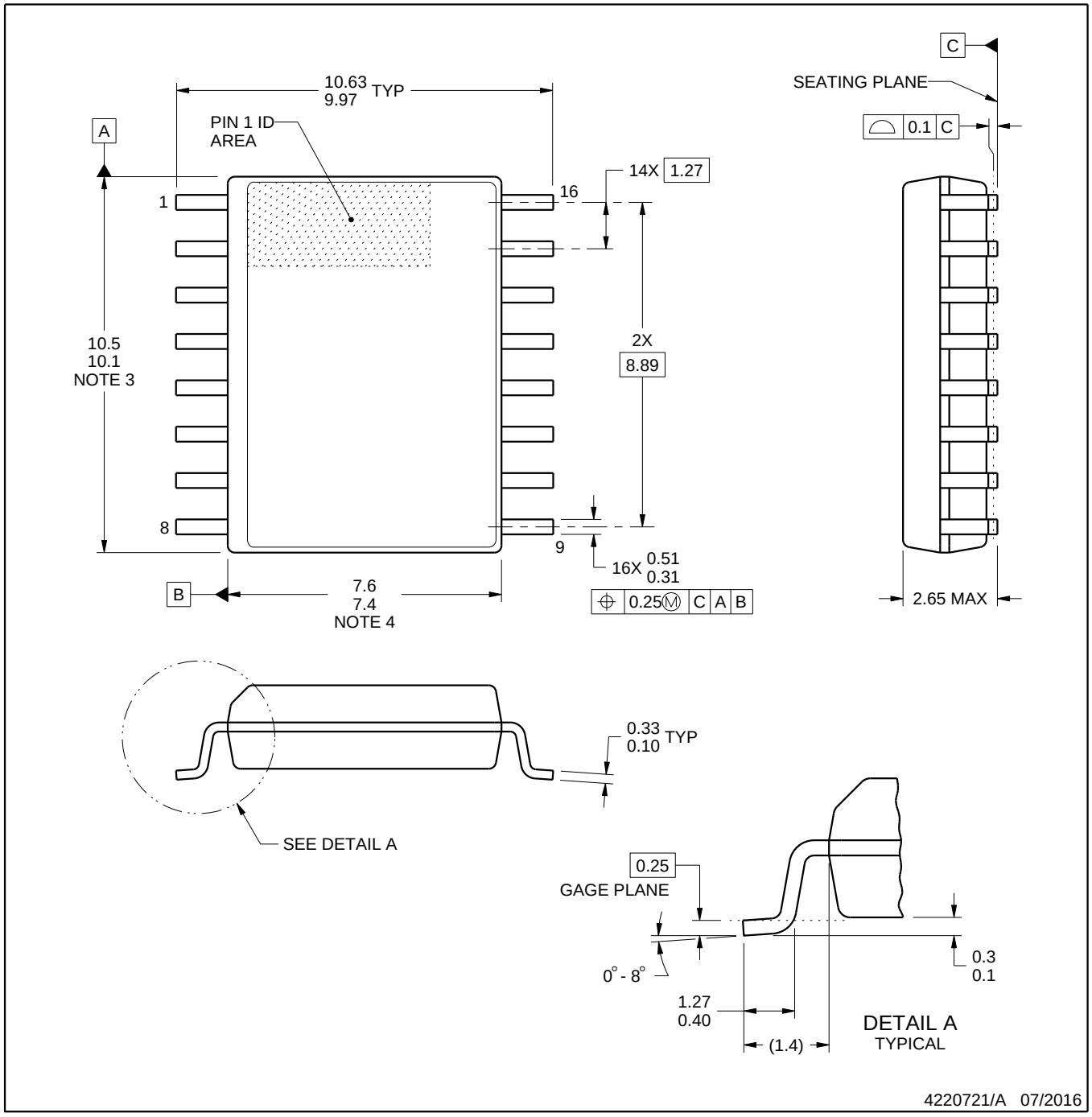


PACKAGE OUTLINE

DW0016A

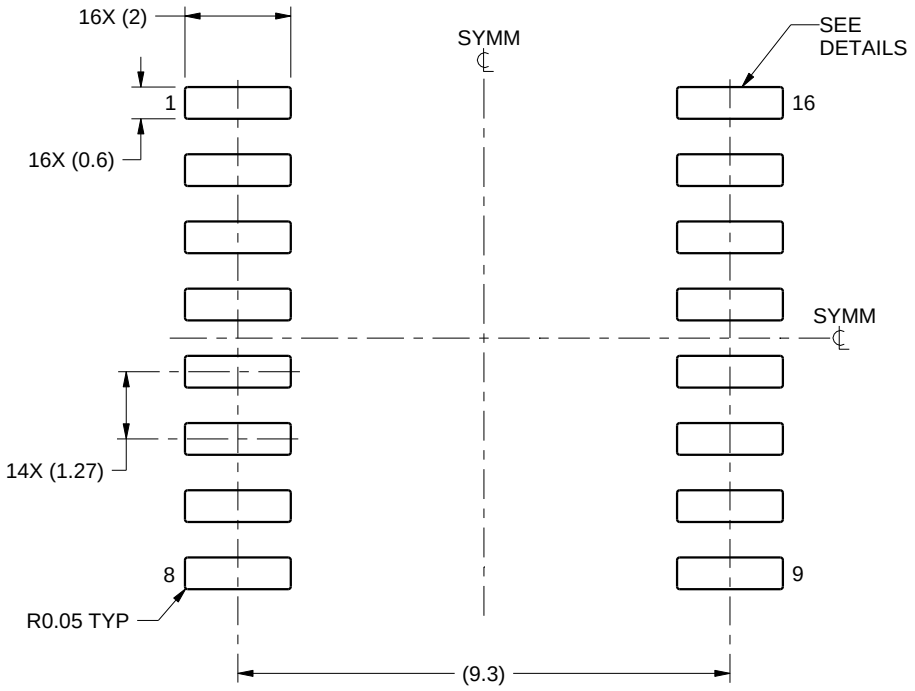
SOIC - 2.65 mm max height

SOIC

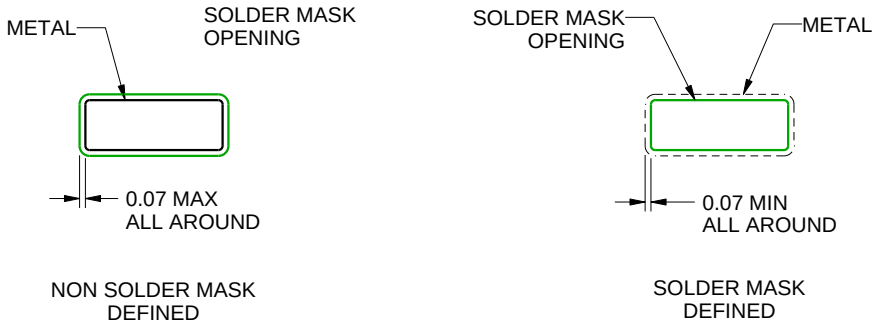


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

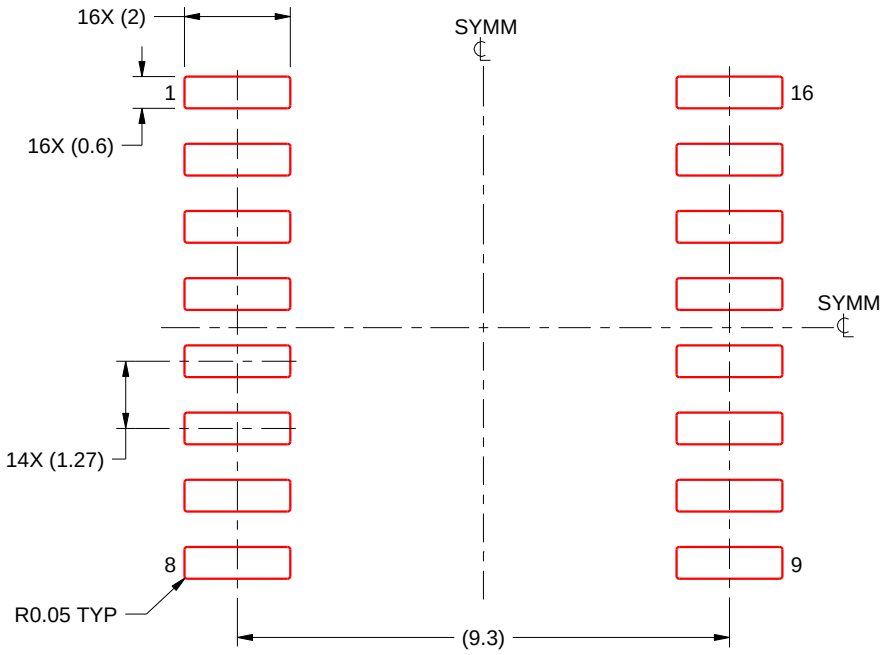


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

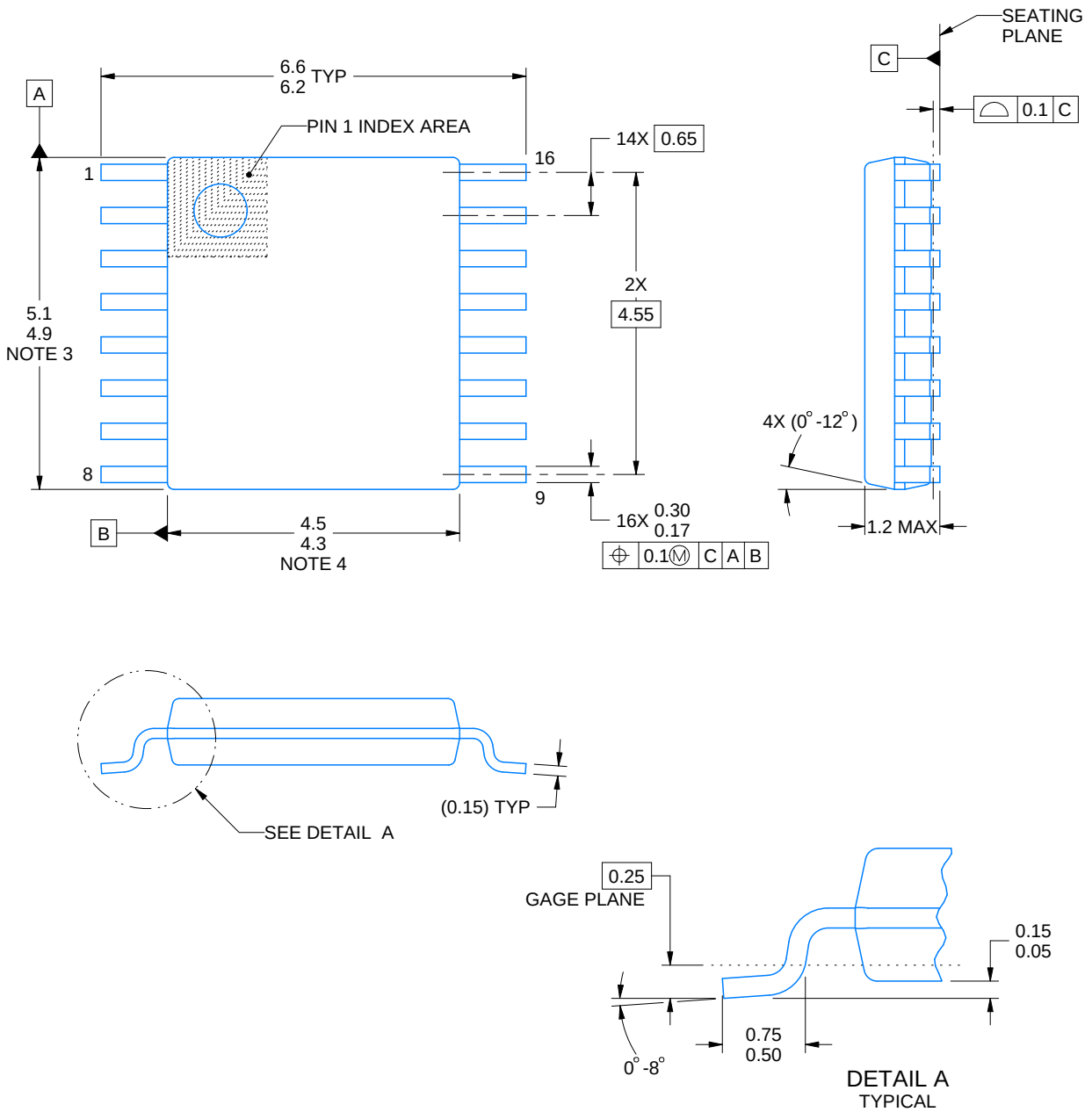
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

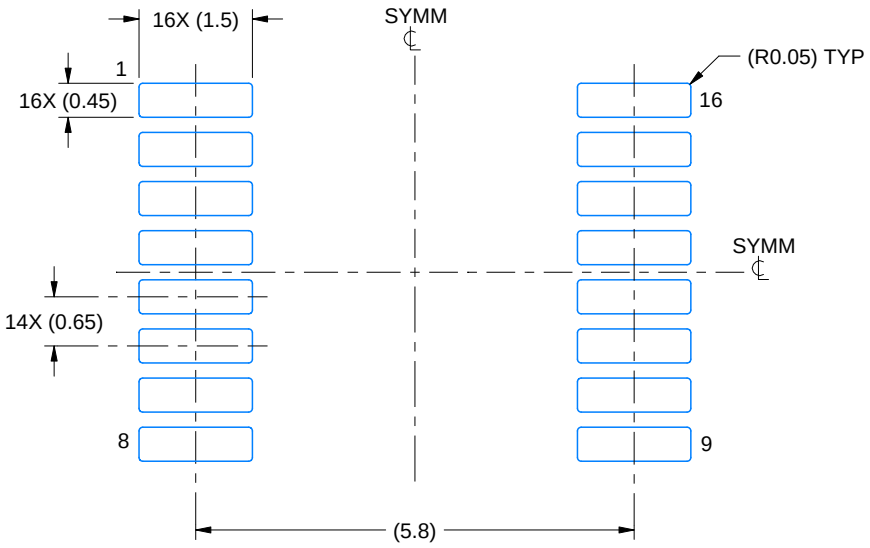
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

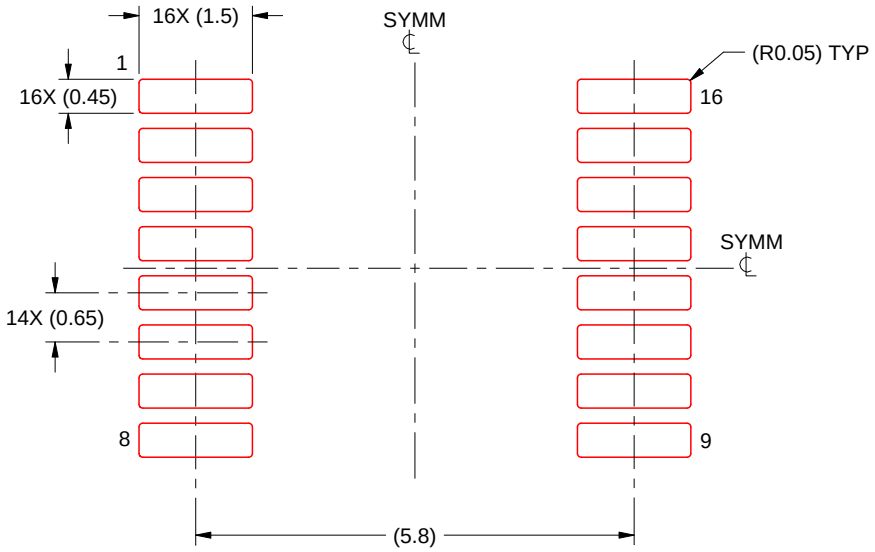


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

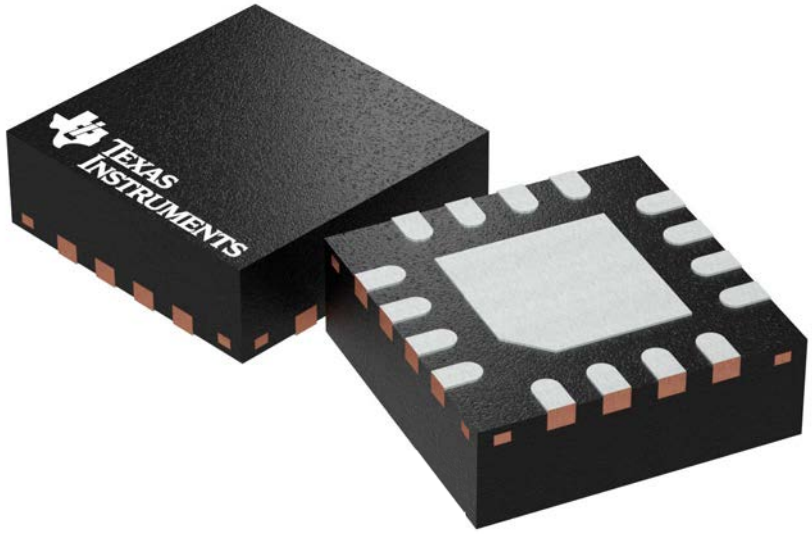
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



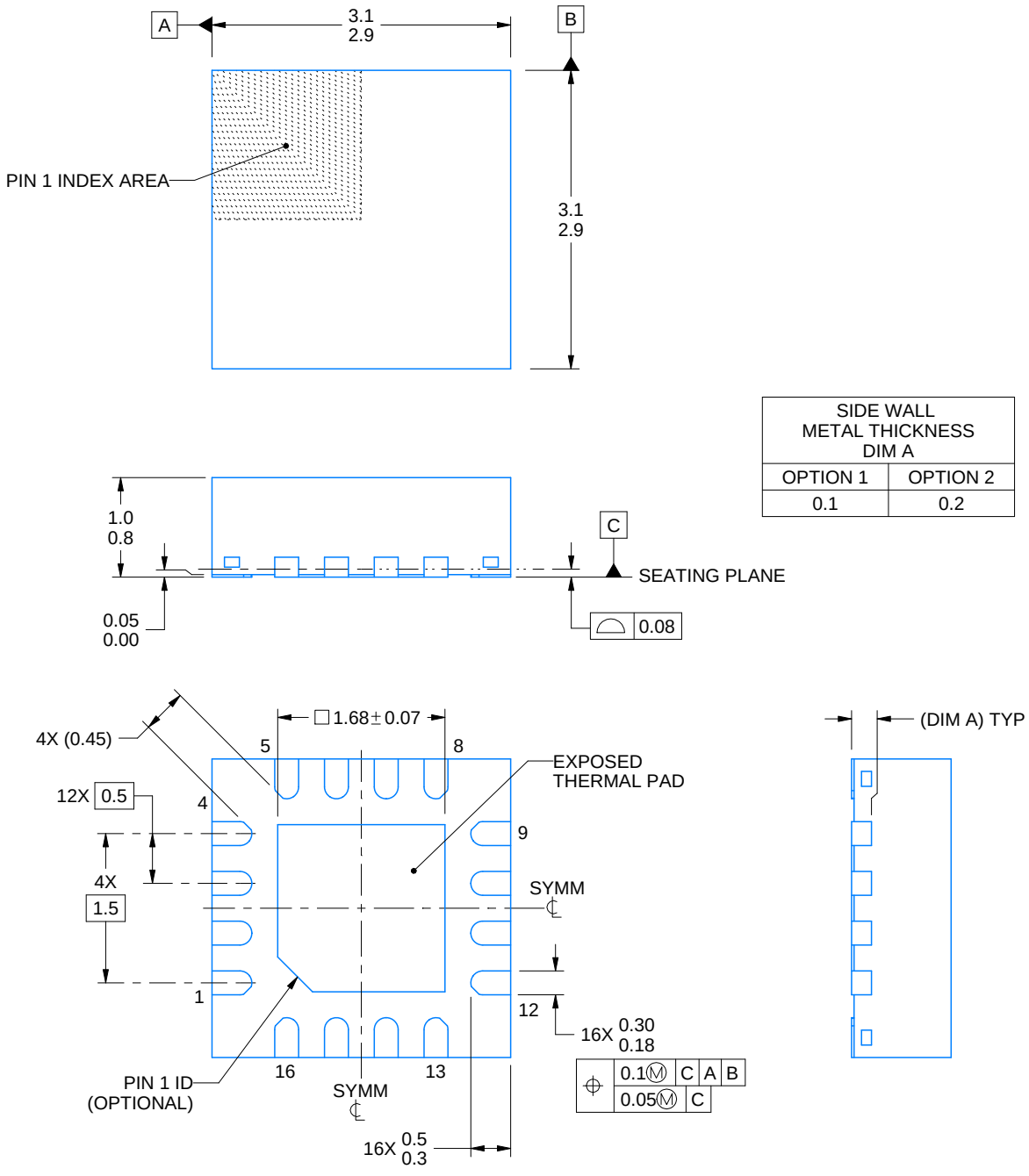
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

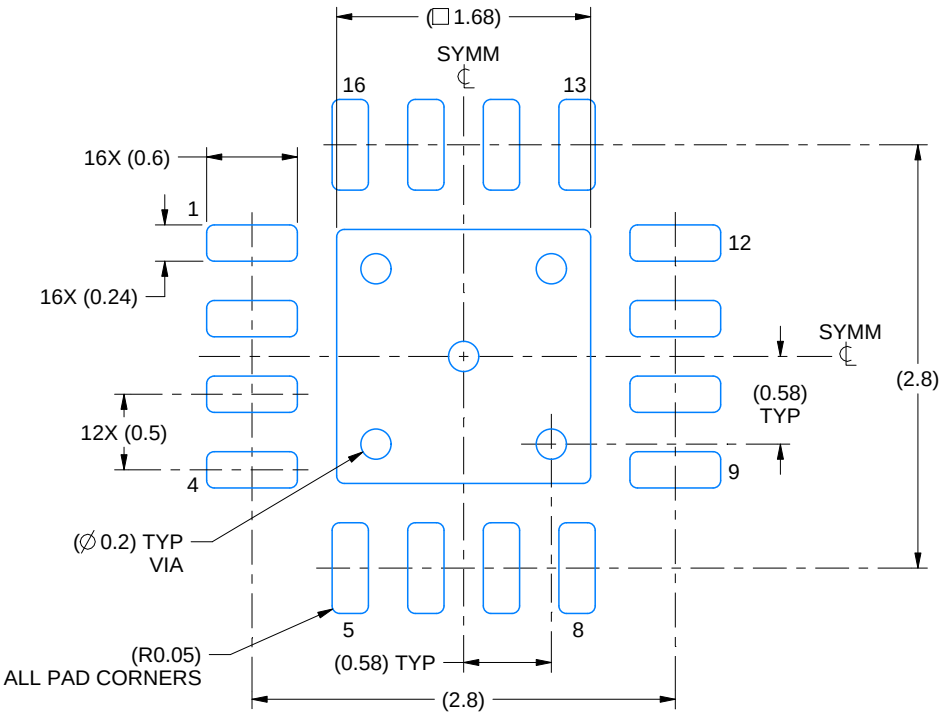
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

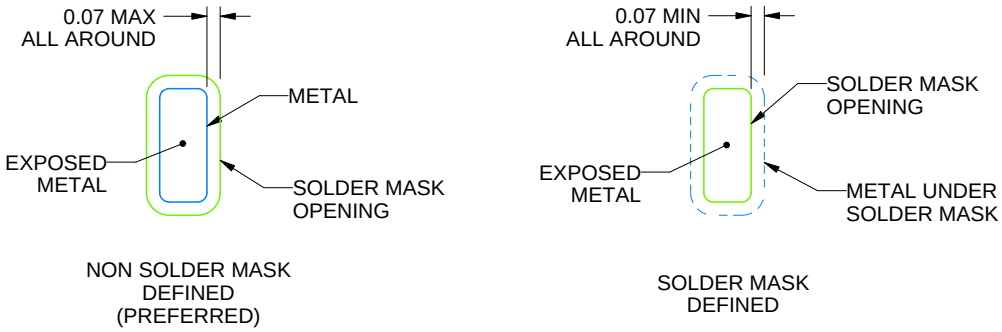


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

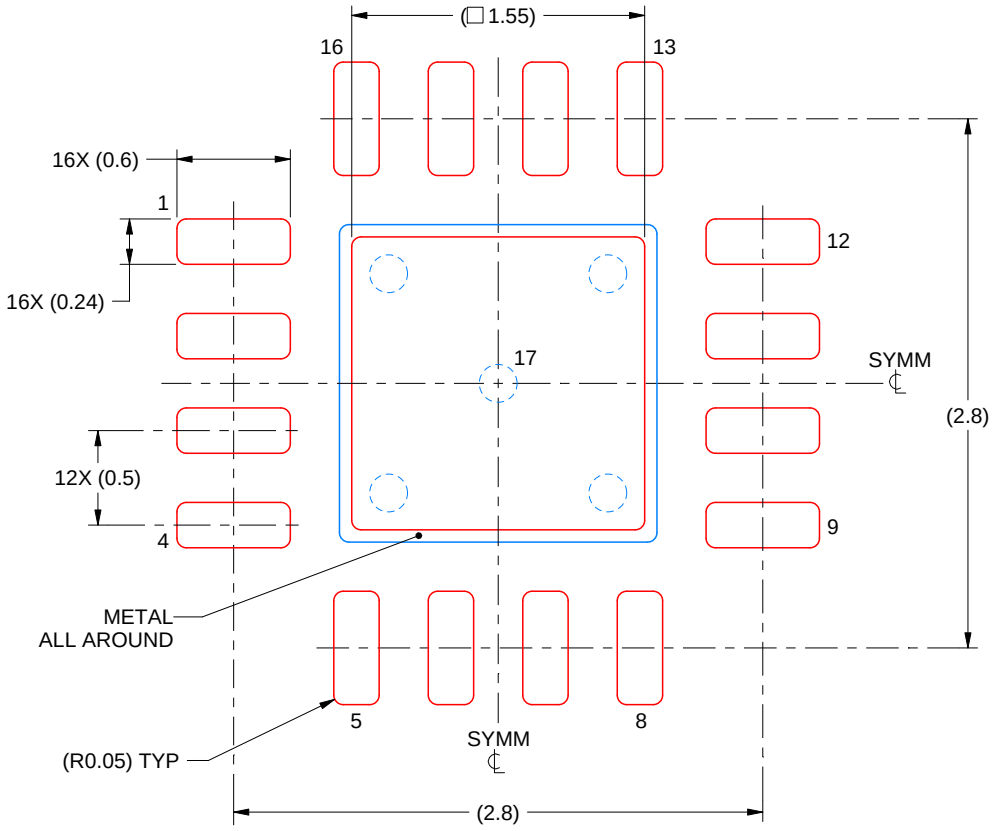


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月