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シングル5Ω SP3Tアナログ・スイッチ 5V/3.3V 3:1マルチプレクサ/デマルチプレクサ

1 特長

- Break-Before-Makeスイッチングを規定
- 低いオン抵抗
- 高帯域幅
- 制御入力は5.5V許容
- 低い電荷注入
- 非常に優れたオン抵抗マッチング
- 低い全高調波歪(THD)
- 1.65V～5.5Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESD 22に準拠しテスト済み
  - 人体モデルで2000V (A114-B、クラスII)
  - 荷電デバイス・モデルで1000V (C101)

2 アプリケーション

- 携帯電話
- 携帯情報端末
- ポータブル機器

3 概要

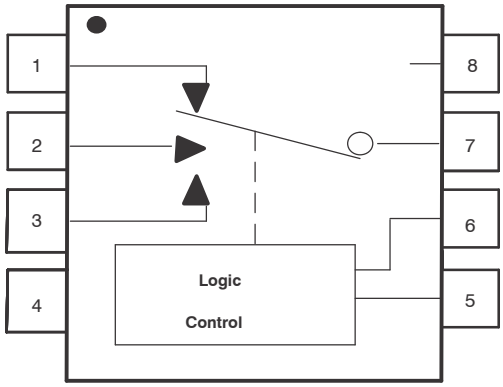
TS5A3357は1チャネルの高性能3:1アナログ・スイッチで、1.65V～5.5Vで動作するよう設計されています。オン抵抗が低く、入力/出力容量が低いことで、信号歪みが小さくなっています。Break-Before-Make機能により、信号をポートから他のポートへ最小の信号歪みで転送できます。また、このデバイスは電荷注入が小さいため、高性能のオーディオおよびデータ収集システムに適しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS5A3357	VSSOP (8)	2.3mm×2mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ロジック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (December 2007) から Revision B に変更 **Page**

- 「*製品情報*」表、「*ESD定格*」表、「*推奨動作条件*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

5 Device Comparison Table

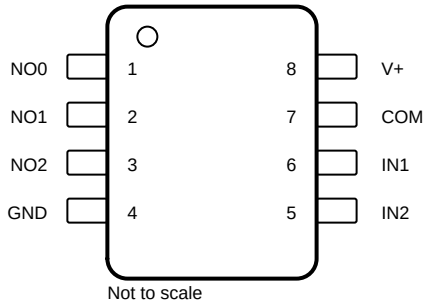
Table 1. Summary of Characteristics(1)

Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (r_{on})	5 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	6.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	6.5 ns/3.7 ns
Break-before-make time (t_{BBM})	0.5 ns
Charge injection (Q_C)	3.4 pC
Bandwidth (BW)	334 MHz
OFF isolation (O_{ISO})	–82 dB at 10 MHz
Crosstalk (X_{TALK})	–62 dB at 10 MHz
Total harmonic distortion (THD)	0.05%
Leakage current ($I_{COM(OFF)}$)	±1 μA

(1) V_+ = 5 V, T_A = 25°C

6 Pin Configuration and Functions

DCU Package
VSSOP 8 Pin
Top View



Not to scale

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NO0	1	Normally open
NO1	2	Normally open
NO2	3	Normally open
GND	4	Digital ground
IN2	5	Digital control to connect COM to NO
IN1	6	Digital control to connect COM to NO
COM	7	Common
V+	8	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_+	Supply voltage range(2)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(2) (3) (4)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	–100	100	mA
V_I	Digital input voltage range(2) (3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range	1.65	5.5	V
V_{NO} V_{COM}	Analog voltage range	0	V_+	
V_I	Digital input voltage range	0	5.5	

7.4 Thermal Information

THERMAL METRIC(1)		TS5A3357 DCU (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –30 mA,	Switch ON, See Figure 13	Full	4.5 V			15	Ω
ON-state resistance	r_{on}	V_{NO} = 0, I_{COM} = 30 mA	Switch ON, See Figure 13	25°C	4.5 V		5	7	Ω
				Full				7	
		V_{NO} = 2.4 V, I_{COM} = –30 mA		25°C			6	12	
				Full				12	
		V_{NO} = 4.5 V, I_{COM} = –30 mA		25°C			7	15	
				Full				15	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 3.15 V, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	5 V		6.5		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	0	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 14	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V			0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 5-V Supply(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	5 V	1.5		6.5	ns
				Full	4.5 V to 5.5 V	1.5		7	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	5 V	0.8		3.7	ns
				Full	4.5 V to 5.5 V	0.8		7	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	5 V	0.5			ns
				Full	4.5 V to 5.5 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	5 V		3.4		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	5 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	4.5 V to 5.5 V		334		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	4.5 V to 5.5 V		–82		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	4.5 V to 5.5 V		–62		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	μA
				Full				10	

7.6 Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	Full	3 V			25	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 24 mA	Switch ON, See Figure 13	25°C	3 V		6.5	9	Ω
				Full				9	
		V_{NO} = 3 V, I_{COM} = –24 mA		25°C			9	20	
				Full				20	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3.3 V		13.5		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–1		0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply[1] (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	3.3 V	2		9.5	ns
				Full	3 V to 3.6 V	2		11	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	3.3 V	1.3		5.1	ns
				Full	3 V to 3.6 V	1.5		5.5	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	3.3 V	0.5			ns
				Full	3 V to 3.6 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	3.3 V		1.75		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3 V to 3.6 V		327		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3 V to 3.6 V		–82		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	3 V to 3.6 V		–62		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	μA
				Full				10	

7.7 Electrical Characteristics for 2.5-V Supply[1]

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	Full	2.3 V			50	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 8 mA	Switch ON, See Figure 13	25°C	2.3 V		8	12	Ω
				Full				12	
		V_{NO} = 2.3 V, I_{COM} = –8 mA		25°C			11	30	
				Full				30	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.3		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.5 V		39		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		V_+ × 0.75		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.25	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V			0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply(1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	2.5 V		3	15	ns
				Full	2.3 V to 2.7 V		3	16.5	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	2.5 V		2	7.2	ns
				Full	2.3 V to 2.7 V		2	7.8	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	2.5 V	0.5			ns
				Full	2.3 V to 2.7 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	2.5 V		1.15		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	2.5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	2.5 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.3 V to 2.7 V		320		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.3 V to 2.7 V		–81		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	2.3 V to 2.7 V		–61		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	µA
				Full				10	

7.8 Electrical Characteristics for 1.8-V Supply[1]

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –4 mA,	Switch ON, See Figure 13	Full	1.65 V			150	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 4 mA	Switch ON, See Figure 13	25°C	1.65 V		10	20	Ω
				Full				20	
		V_{NO} = 1.8 V, I_{COM} = –4 mA		25°C			17	50	
				Full				50	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.3		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.8 V		140		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		$V_+ \times 0.75$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.25$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V			0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	1.8 V	5		32	ns
				Full	1.65 V to 1.95 V	5		34	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	1.8 V	3		14	ns
				Full	1.65 V to 1.95 V	3		14.5	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	1.8 V	0.5			ns
				Full	1.65 V to 1.95 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	1.8 V		0.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	1.8 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	1.8 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	1.8 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	1.8 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	1.65 V to 1.95 V		341		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	1.65 V to 1.95 V		–81		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	1.65 V to 1.95 V		–61		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	µA
				Full				10	

7.9 Typical Characteristics

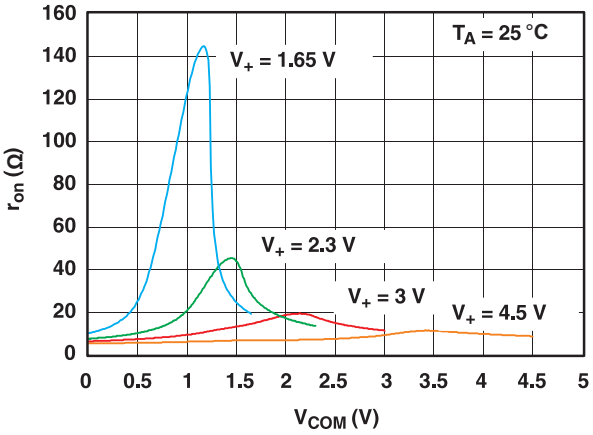


Figure 1. r_{on} vs V_{COM}

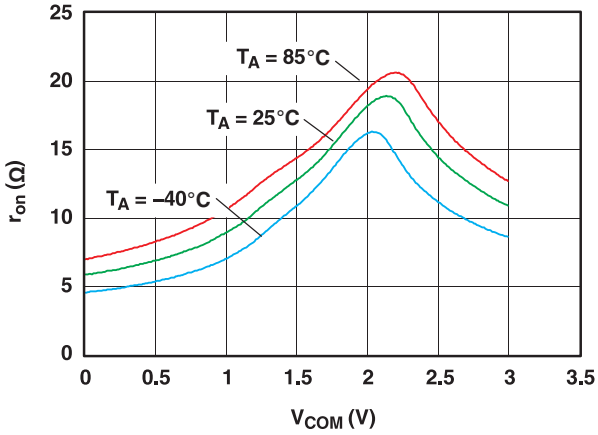


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

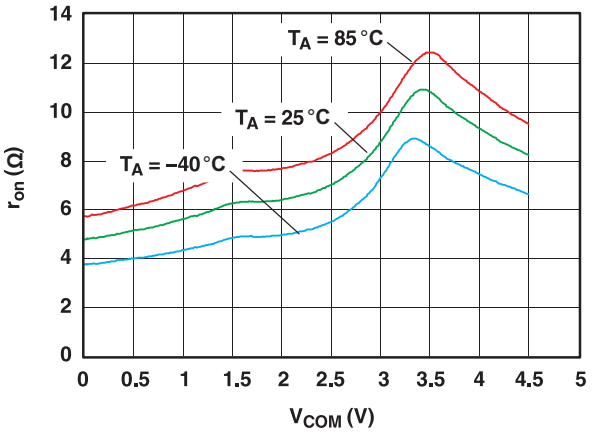


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

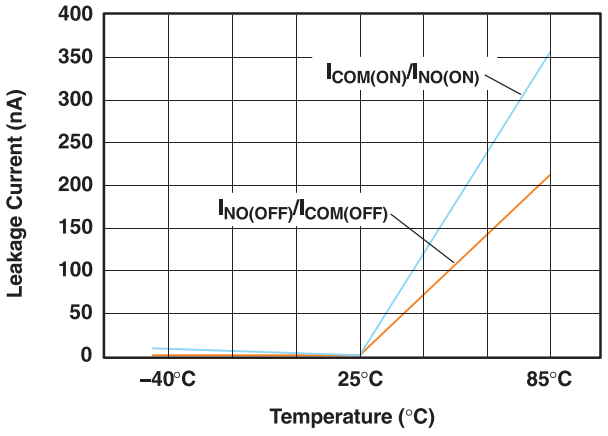


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

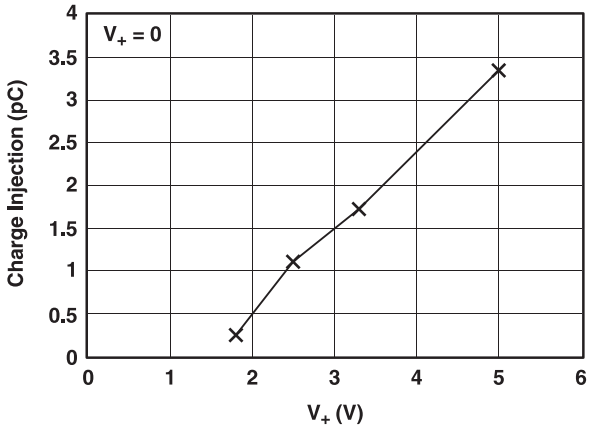


Figure 5. Charge Injection (Q_C) vs V_{COM}

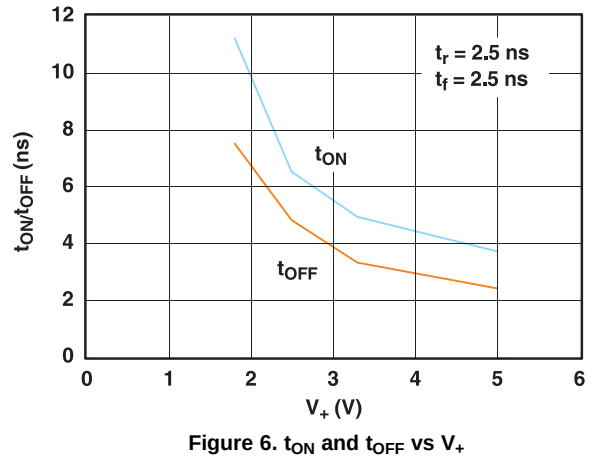


Figure 6. t_{ON} and t_{OFF} vs V_+

Typical Characteristics (continued)

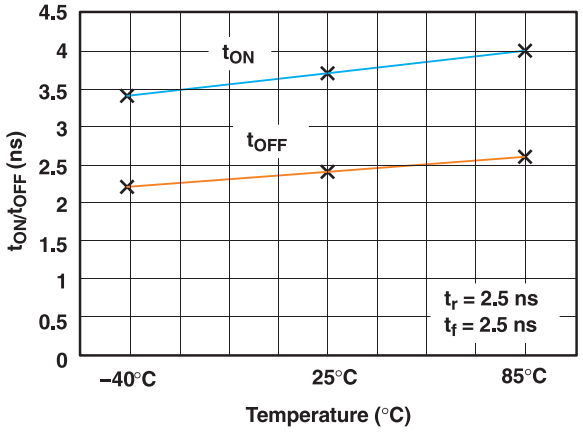


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

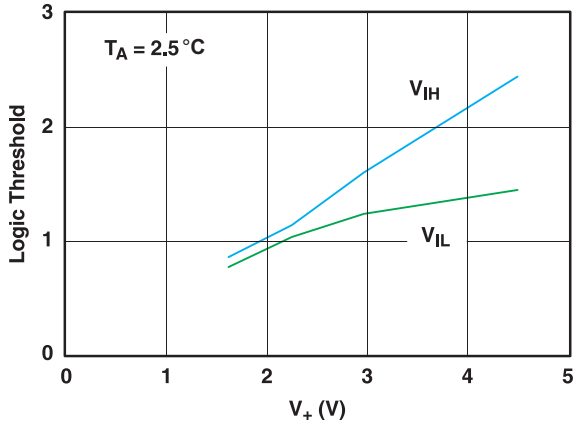


Figure 8. Logic-Level Threshold vs V_+

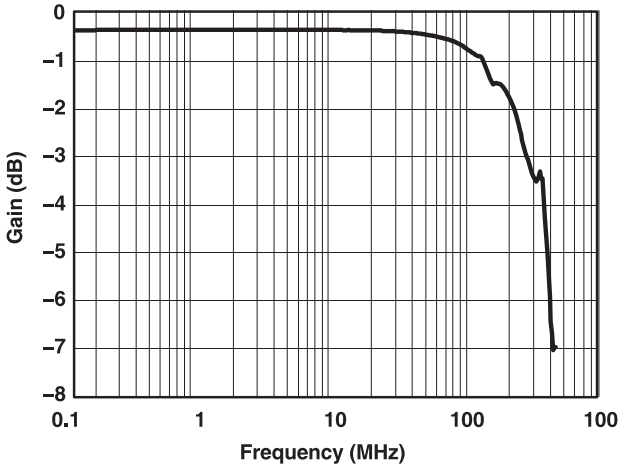


Figure 9. Frequency Response (V_+ = 3 V)

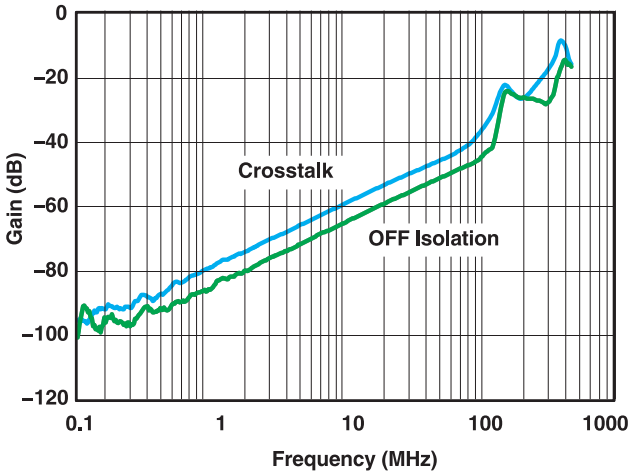


Figure 10. OFF Isolation and Crosstalk vs Frequency (V_+ = 3 V)

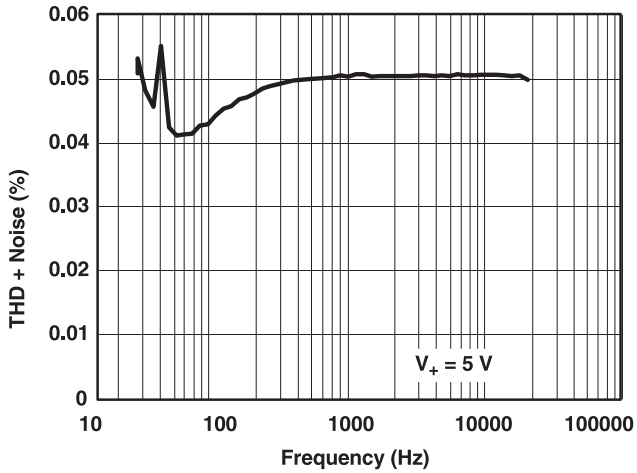


Figure 11. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

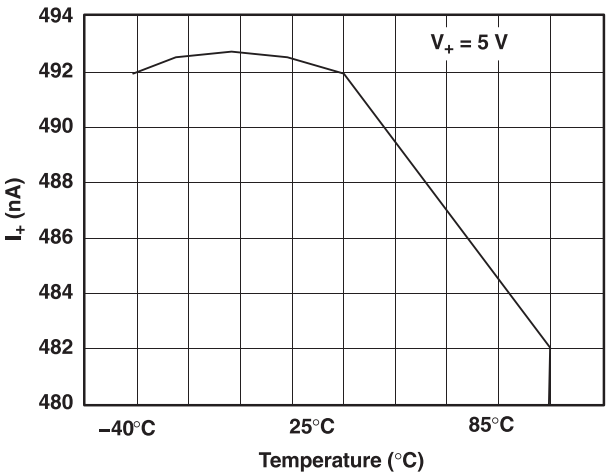


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

8 Parameter Measurement Information

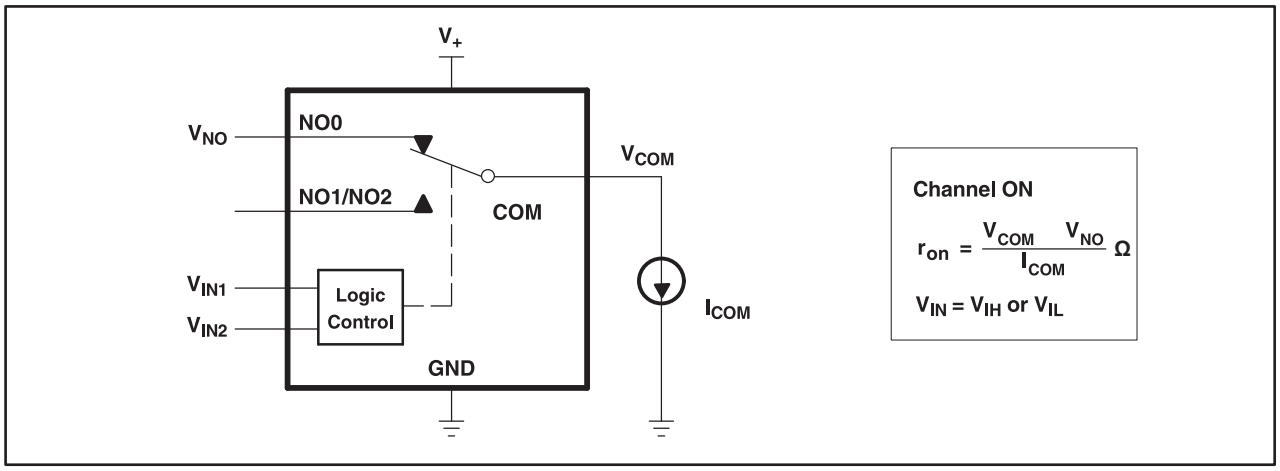


Figure 13. ON-State Resistance (r_{on})

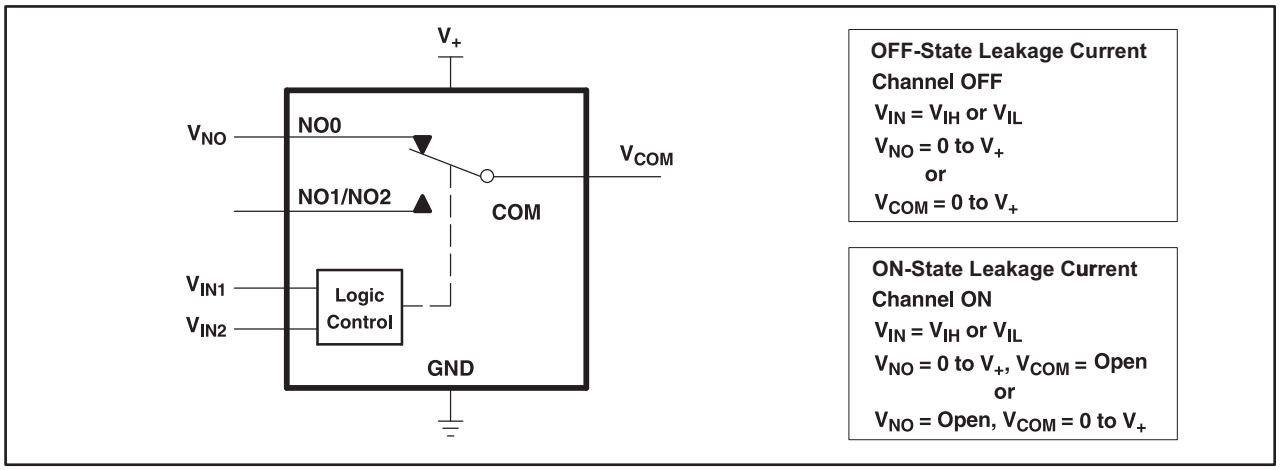


Figure 14. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{COM(OFF)}$, $I_{NO(ON)}$, $I_{NO(OFF)}$)

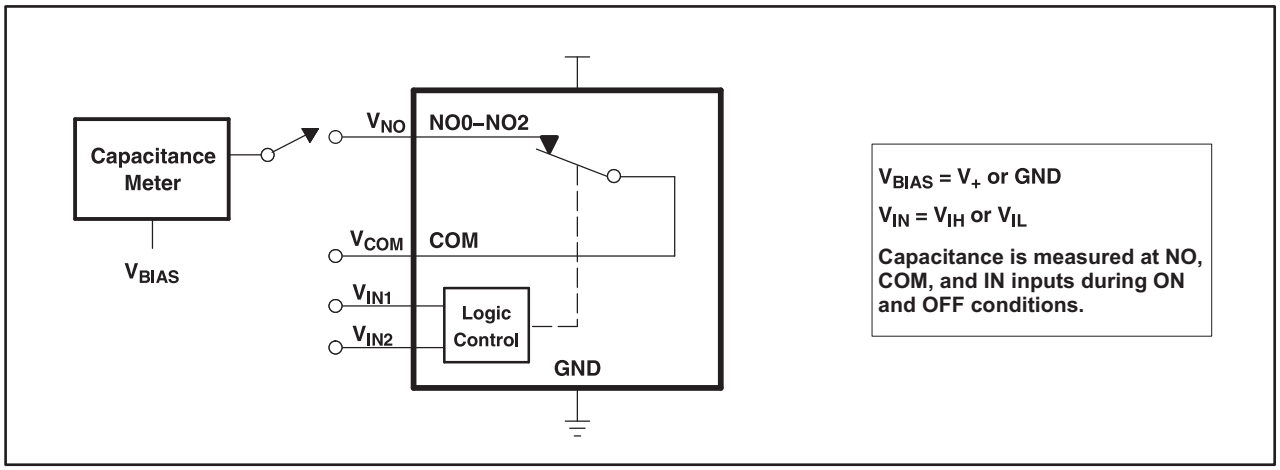
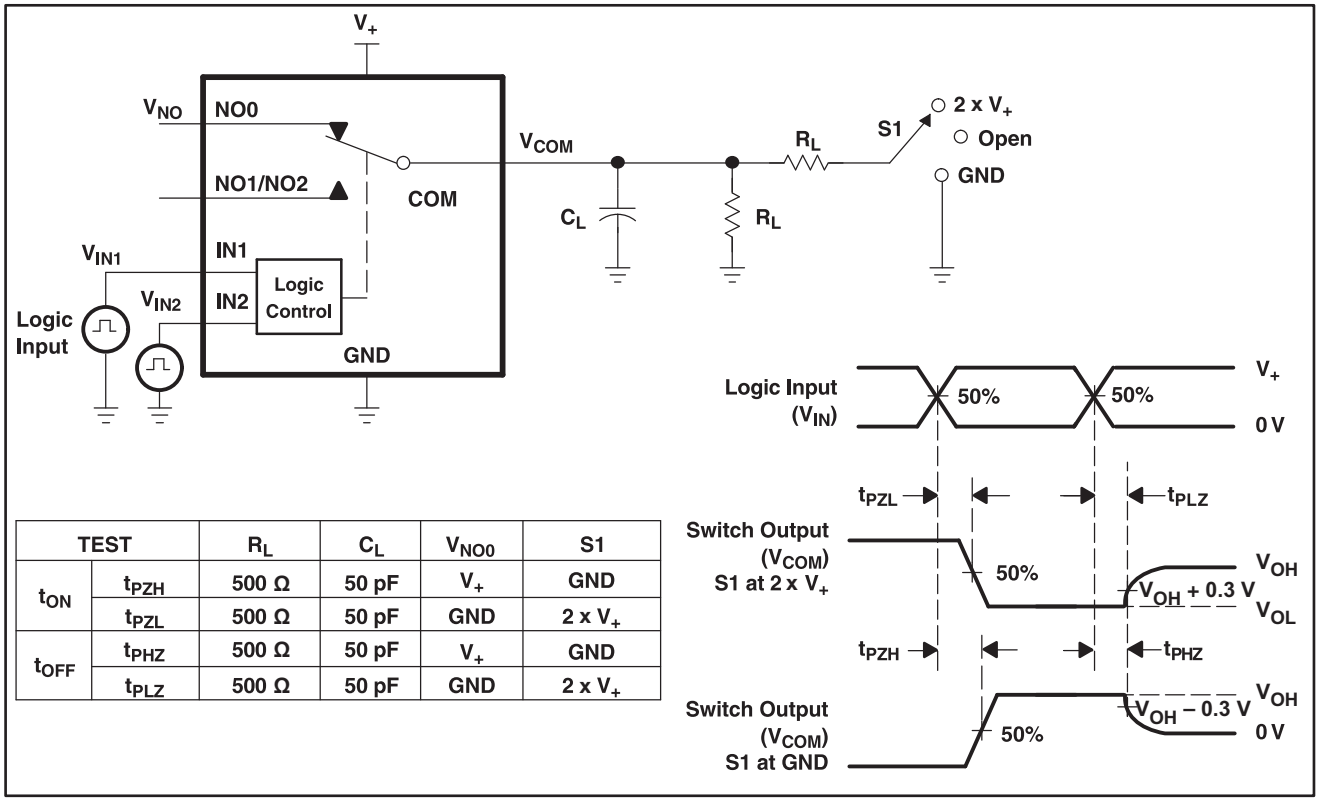


Figure 15. Capacitance (C_I, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{COM(OFF)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)

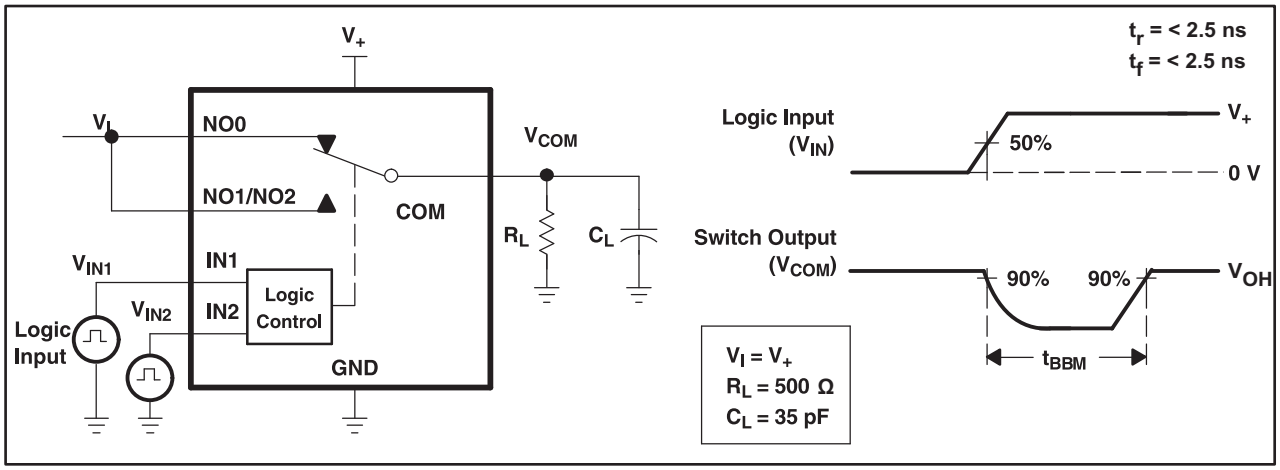


TEST		R_L	C_L	V_{NO0}	S1
t_{ON}	t_{PZH}	500 Ω	50 pF	V_+	GND
	t_{PZL}	500 Ω	50 pF	GND	2 x V_+
t_{OFF}	t_{PHZ}	500 Ω	50 pF	V_+	GND
	t_{PLZ}	500 Ω	50 pF	GND	2 x V_+

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 16. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 17. Break-Before-Make Time (t_{BBM})

Parameter Measurement Information (continued)

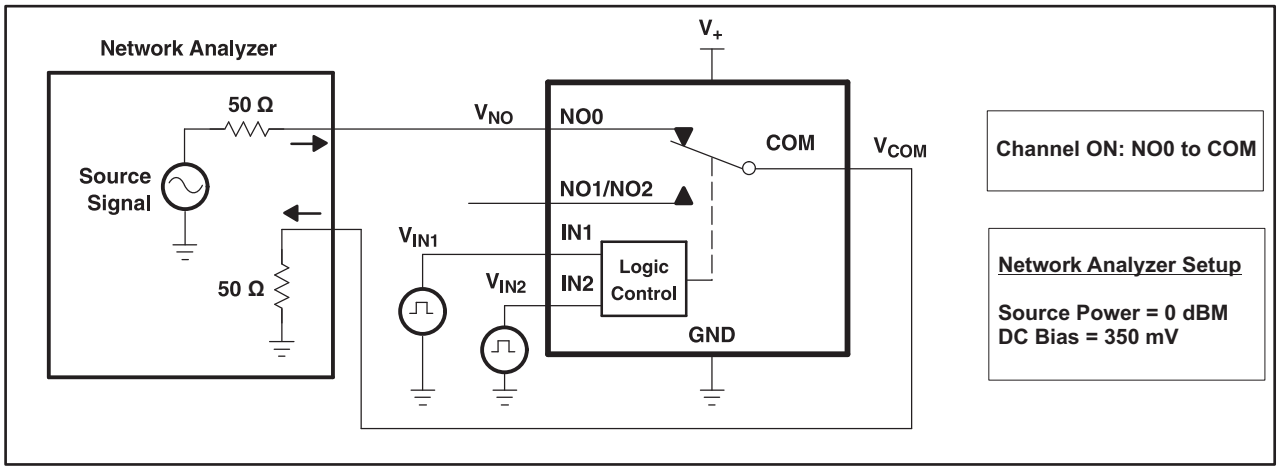


Figure 18. Bandwidth (BW)

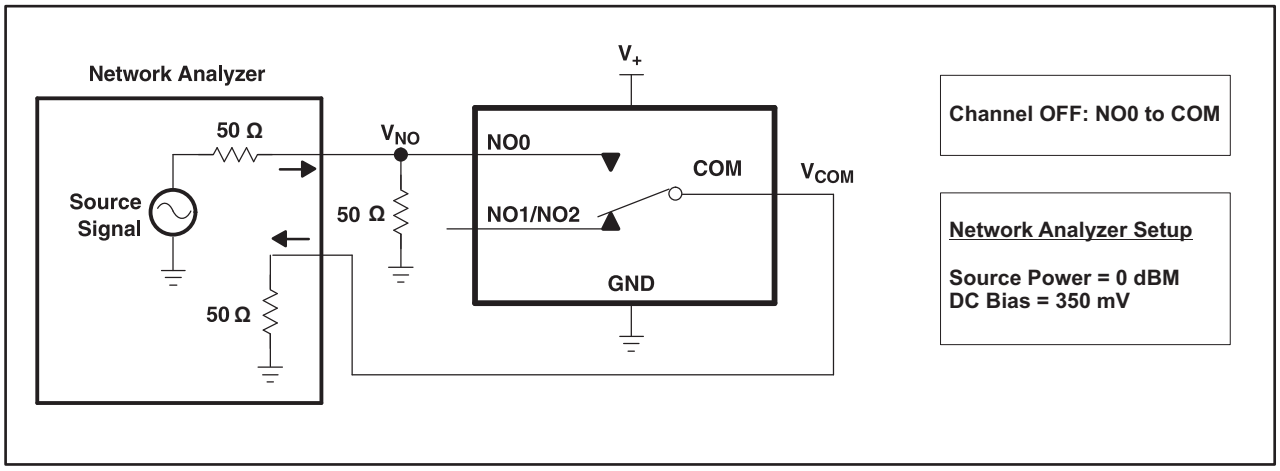


Figure 19. OFF Isolation (O_{ISO})

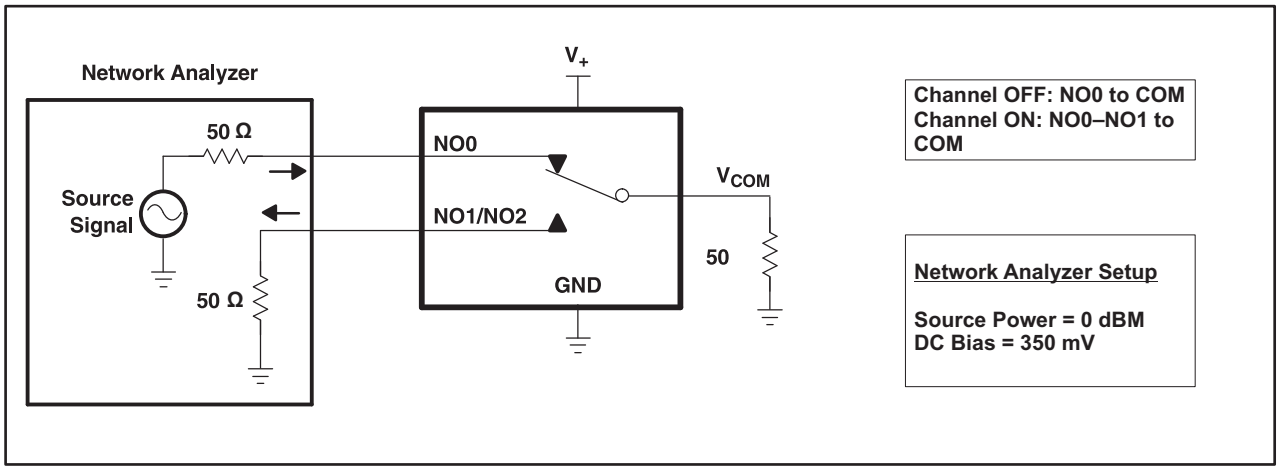
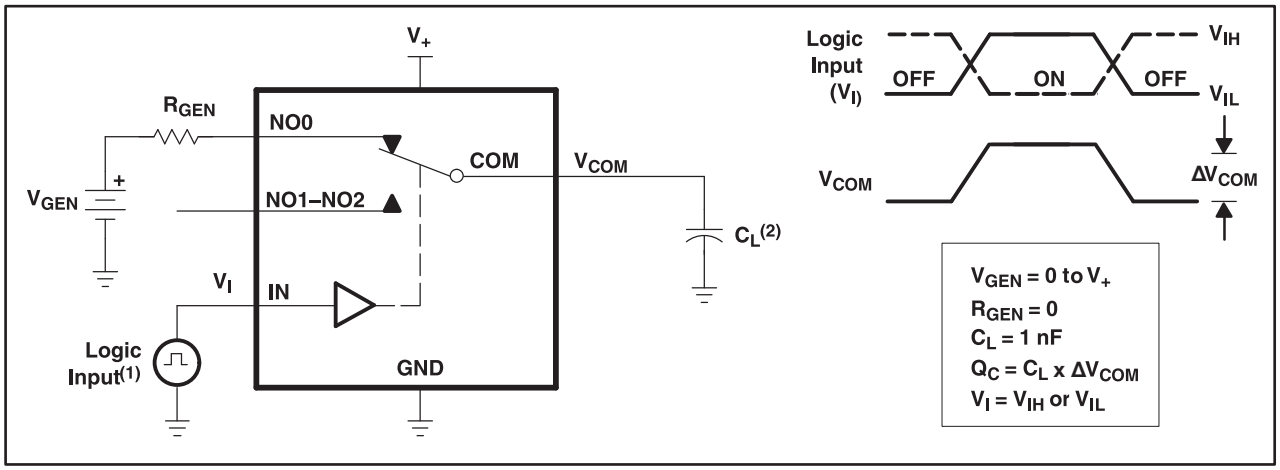


Figure 20. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

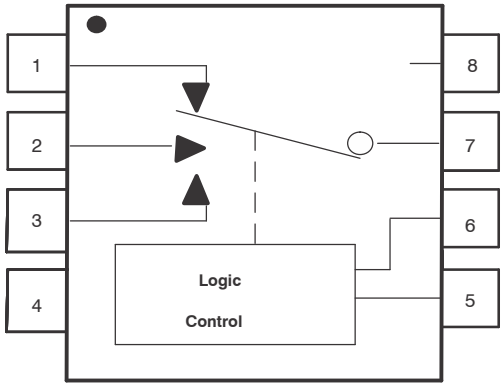
Figure 21. Charge Injection (Q_C)

9 Detailed Description

9.1 Overview

The TS5A3357 is a bidirectional, single-channel, 3:1 analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3357 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3357 device also has a specified break-before-make feature.

9.2 Functional Block Diagram



9.3 Feature Description

Break-before-make

Break-before-make is a safety feature that prevents two inputs from connecting when the TS5A3357 is switching. The TS5A3357 COM pin first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the break and the make is known as a break-before-make delay t_{BBM}.

9.4 Device Functional Modes

The digital control pins IN1 and IN2 determine the state of the connection between the COM and NO pins based on the truth table below.

Table 2. Function Table

IN1	IN2	COM TO NO0	COM TO NO1	COM TO NO2
L	L	OFF	OFF	OFF
H	L	ON	OFF	OFF
L	H	OFF	ON	OFF
H	H	OFF	OFF	ON

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.2 Typical Application

The TS5A3357 switch is bidirectional, so the NO and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 3 different signal paths.

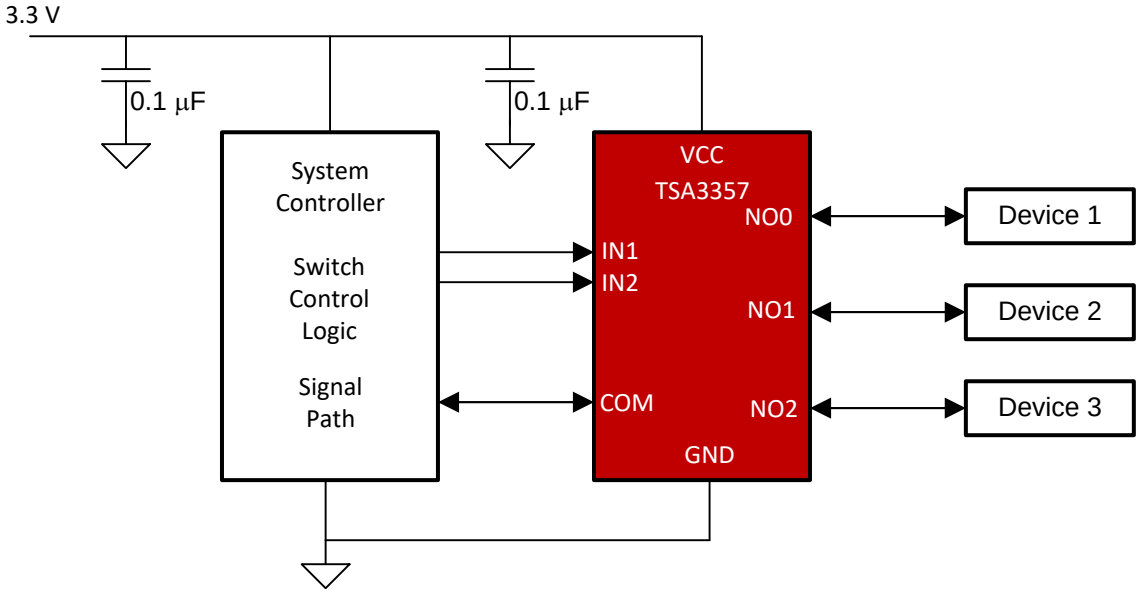


Figure 22. Typical Application Schematic

10.2.1 Design Requirements

The TS5A3357 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

10.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3357 input and output signal swing through NO and COM are dependent on the supply voltage V_+. For example, if the desired signal level to pass through the switch is 5 V, VCC must be greater than or equal to 5 V. V_+ = 3.3 V would not be valid for passing a 5-V signal since the Analog signal voltage cannot exceed the supply.

Typical Application (continued)

10.2.3 Application Curves

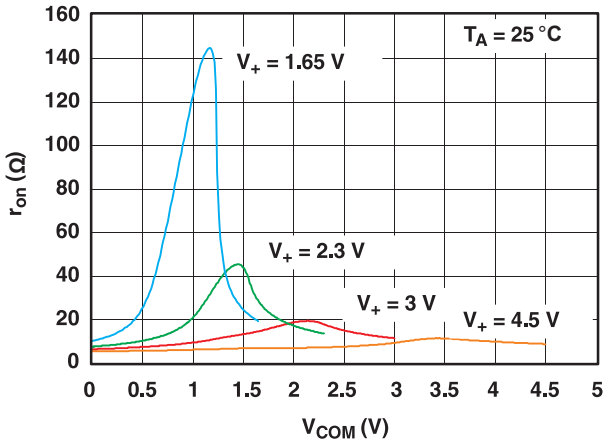


Figure 23. r_{on} vs V_{COM}

11 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_+ on first, followed by NO or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

12 Layout

12.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device. Bypass capacitors should be used on power supplies. Short trace lengths should be used to avoid excessive loading.

12.2 Layout Example

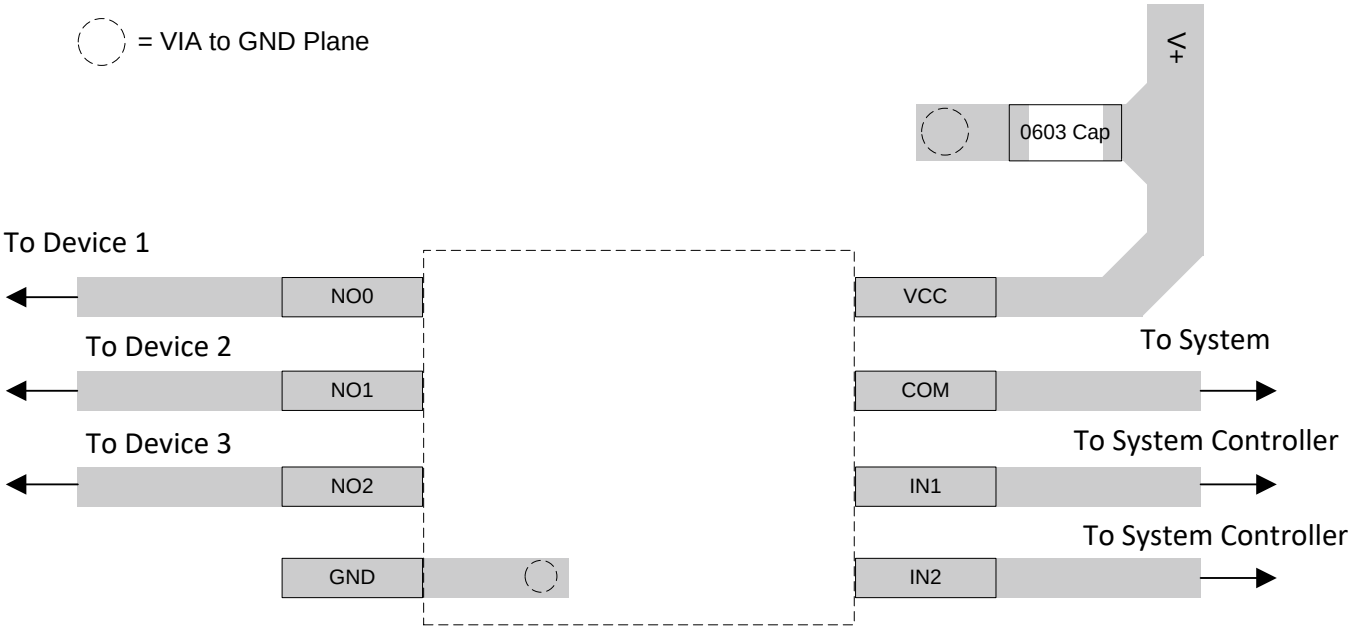


Figure 24. Example Layout

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.2 ドキュメントのサポート

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.5 商標

E2E is a trademark of Texas Instruments.

13.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3357DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JA9Q, JA9R)
TS5A3357DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JA9Q, JA9R)
TS5A3357DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA9R
TS5A3357DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA9R
TS5A3357DCUT	Obsolete	Production	VSSOP (DCU) | 8	-	-	Call TI	Call TI	-40 to 85	(JA9Q, JA9R)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TS5A3357 :

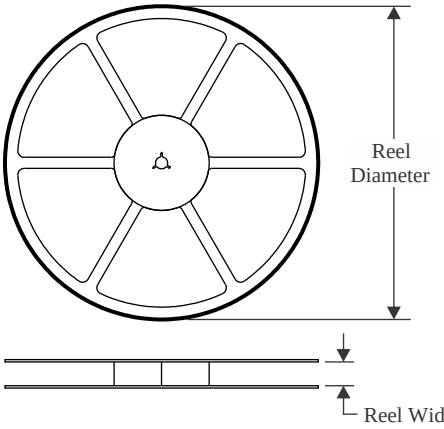
- Automotive : TS5A3357-Q1

NOTE: Qualified Version Definitions:

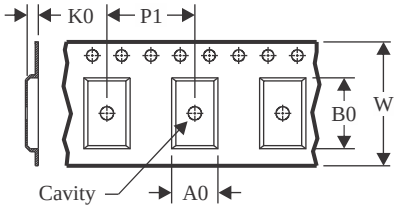
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

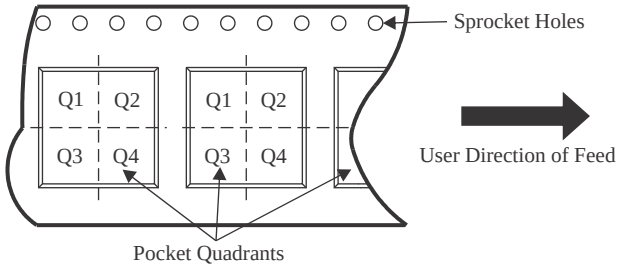


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

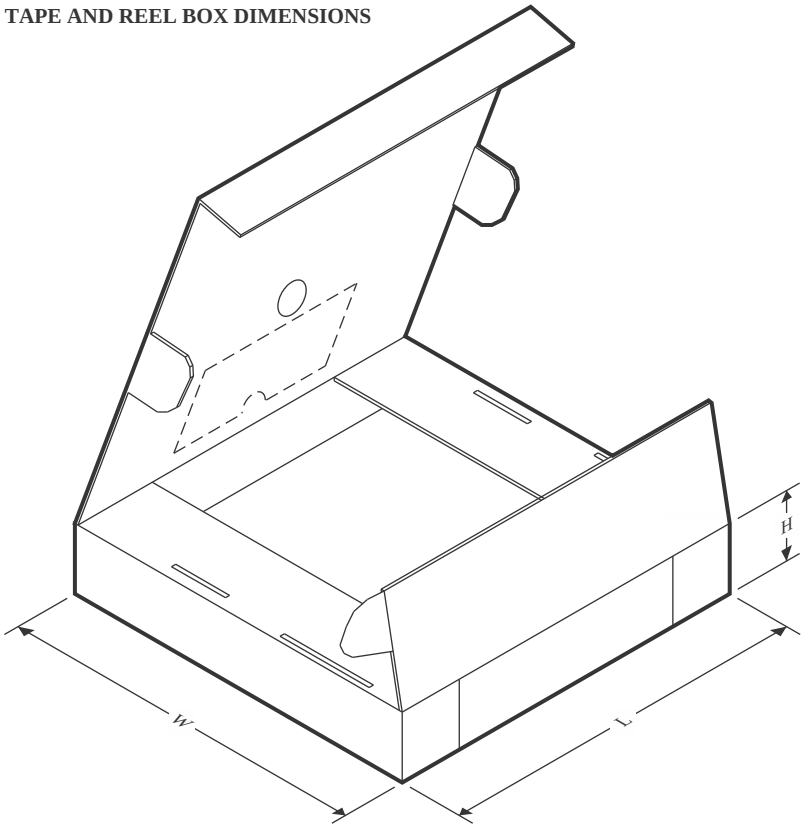
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3357DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3357DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

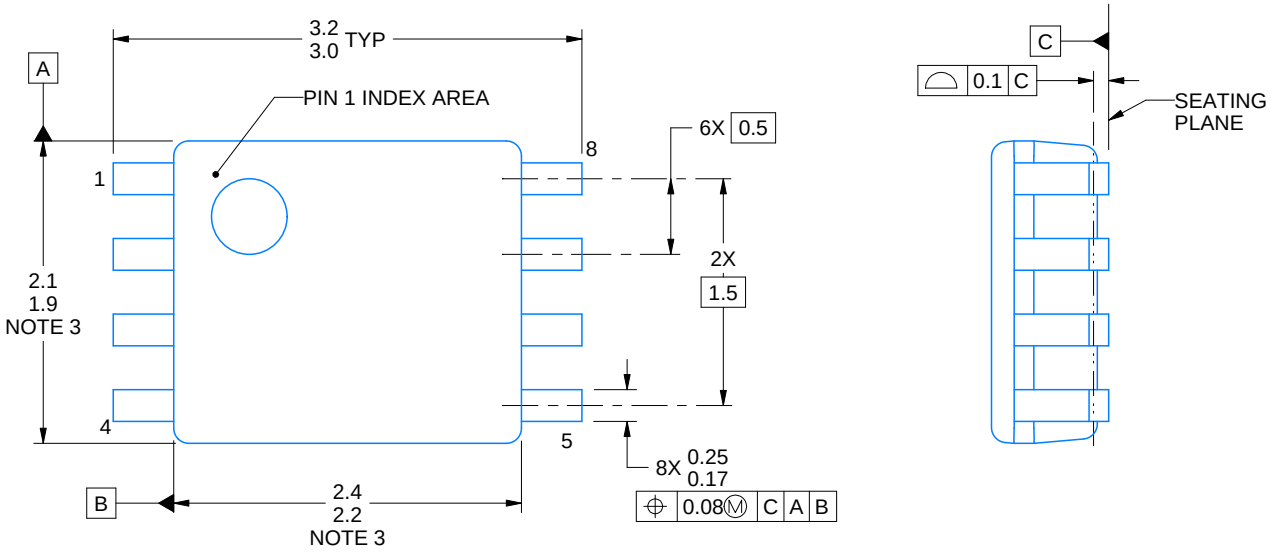
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3357DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
TS5A3357DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0

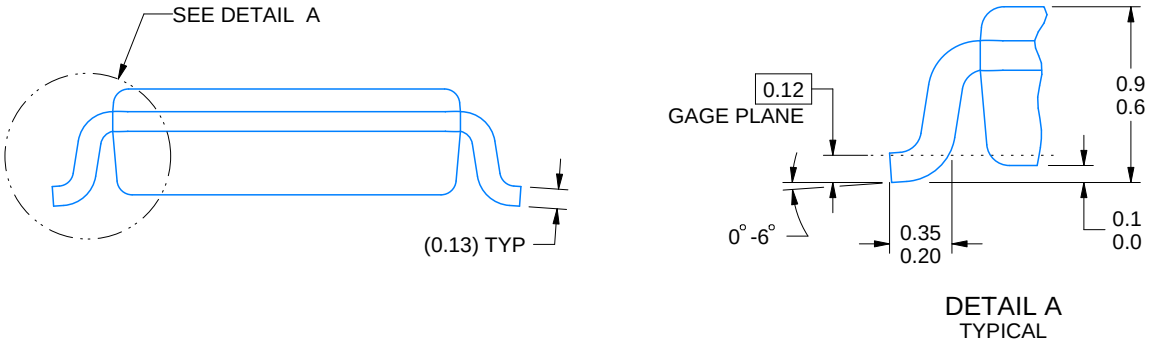
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE





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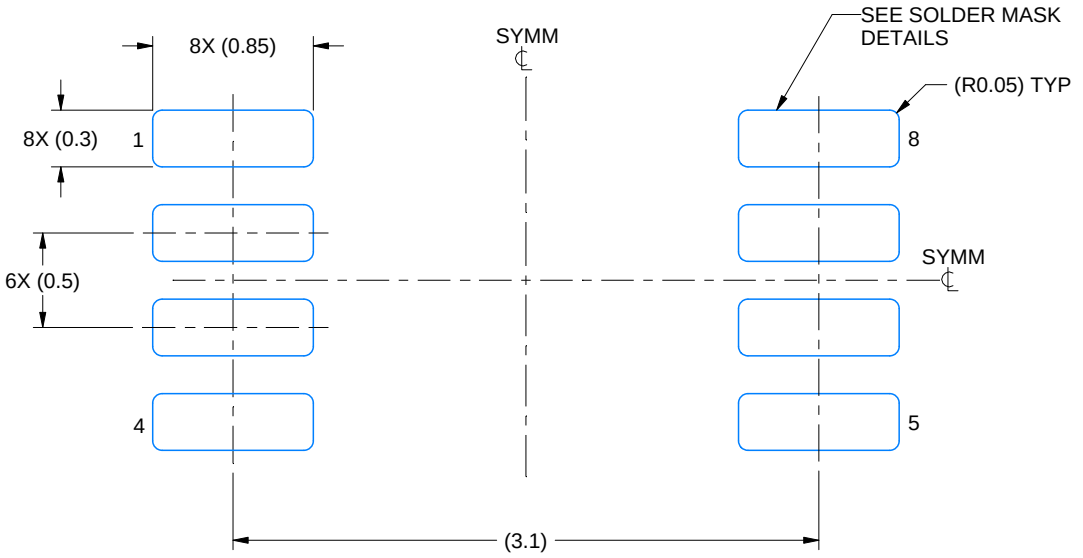
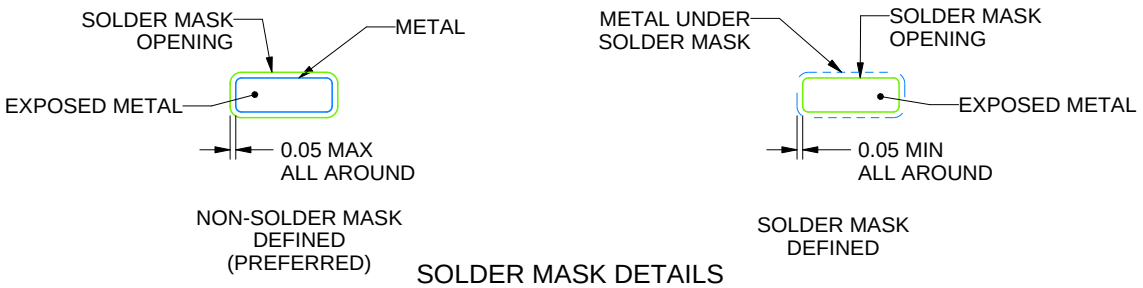
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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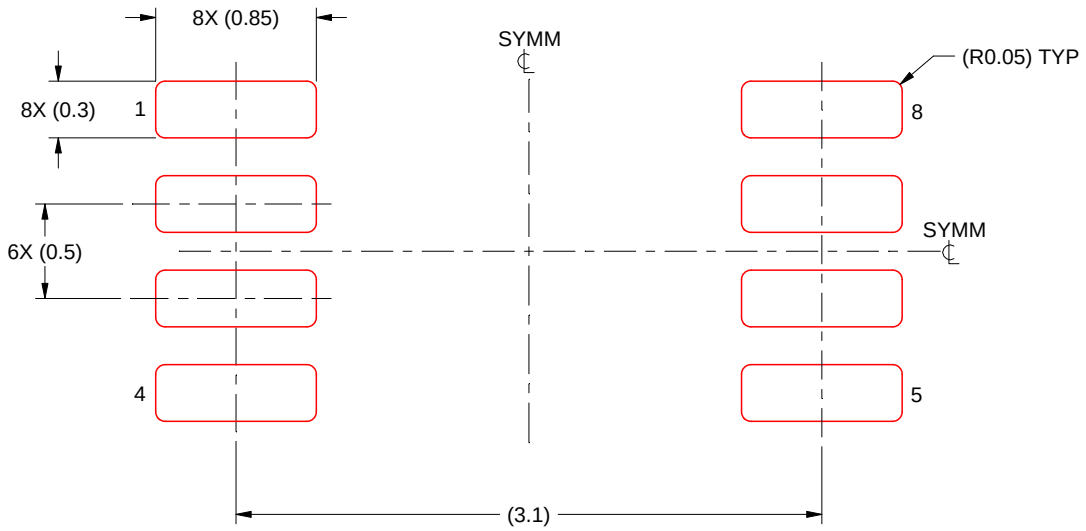
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月