TSB41BA3F-EP IEEE 1394b、3 ポート ケーブル・トランシーバ / アービタ

1 特長

- 新機能 (ベータ・モードで動作しているポート用):スクランブラ同期損失の検出、高速パワーオン再接続、同期損失時の高速再トレーニング、高速トーン・デバウンス、高速接続 (スキップ・トーン・デバウンスおよび速度ネゴシエーション) セクション 13.2.3 を参照
- 1394-1995、IEEE 1394a-2000、IEEE 1394b-2002 の規定を s100、s100b、s200、s200b、S400 および s400b の信号速度で完全にサポート (b は IEEE 1394b 信号を示す) セクション 13.1 を参照
- 完全な下位互換性のある、400Mbps のバイリンガル 1394b および 100/200/400Mbps の 1394a-2000 準拠の 3 つを提供
- 1394a-2000 の完全なサポートは、接続デバウンス、アービトレーション・ショート・リセット、マルチスピード・コンカチネーション、アービトレーション・アクセラレーション、フライバイ・コンカチネーション、ポートのディセーブル / サスペンド / レジューム、レガシー DV デバイスとの互換性のための拡張レジューム信号を含む
- Firewire™、DTVLink、SB1394、DishWire、IEEE std 1394 の i.LINK™ 実装と完全に相互運用可能
- ケーブル / トランシーバのハードウェア速度とポート・モードは、端子状態により選択可能
- ポートをベータ専用、400Mbps 専用、200Mbps 専用、100Mbps 専用に設定することで、CAT5 ケーブル・トランシーバへの接続をサポート
- ポートをベータ専用、200Mbps 専用、100Mbps 専用に設定することで、s200 プラスチック光ファイバ・トランシーバへの接続をサポート
- ベータ・モードのすべてのポートの光信号検出入力により、光トランシーバとの接続が可能
- ポート 1 と 2 を強制的に 1394a 専用モードにすることで、1394a コネクタの使用をサポート
- PHY-LINK インターフェイスは、1394a-2000 モード (49.152MHz で 2/4/8 ビット) または 1394b モード (98.304MHz で 8 ビット) から選択可能
- レジスタ・ビットにより、ソフトウェア・デバイス・リセット、競合ビット、電力クラス・ビット、リンク・アクティブ制御ビット、1394A-2000 機能をソフトウェアで制御可能
- 各ポートの個別バイアス (tpbias)
- ケーブル・ポートは、リモート・ノードにアクティブな接続をするための回線状態を監視
- ケーブル電源の有無を監視
- 1394a-2000 準拠の同相ノイズ・フィルタを入力バイアス検出回路に搭載し、クロストーク・ノイズを除去
- バッテリ駆動アプリケーションでエネルギーを節約するパワーダウン機能
- 低コストの 49.152MHz 水晶振動子は、100/200/400Mbps でデータを送受信し、49.152MHz および 98.304MHz でリンク層コントローラ・クロックを提供
- 3.3V 電源を使用してリンク層コントローラと相互運用可能
- 1.8V、3.3V、5V 電源を使用して他の 1394 物理層 (PHY) と相互運用可能
- フェイルセーフ回路は、デバイスへの突然の電力損失を感知してポートをディスエーブルにして、TSB41BA3F-EP が接続されているデバイスの tpbias をロードしないようにし、ポートから電源プレーンへ戻るリークをブロックする
- 防衛、航空宇宙、医療アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 長い製品ライフ・サイクル
  - 製品変更通知期間の延長
  - 製品のトレーサビリティ

2 アプリケーション

- 航空 / 防衛
- ファクトリ・オートメーションおよび制御
- 医療用

3 概要

TSB41BA3F-EP は、ケーブル・ベースの IEEE 1394 ネットワークに 3 ポート・ノードを実装するために必要なデジタルおよびアナログ・トランシーバ機能を提供します。各ケーブル・ポートには 2 つの差動ライン・トランシーバが組み込まれています。トランシーバには、接続ステータスの決定、初期化とアービトレーション、パケットの送受信のために、必要に応じて回線状態を監視する回路が含まれています。TSB41BA3F-EP は、TSB82AF15-EP、TSB12LV21、TSB12LV26、TSB12LV32、TSB42AA4、TSB42AB4、TSB12LV01B、TSB12LV01C、または TSB82AA2 などのリンク・レイヤ・コントローラ (LLC) とインターフェイスします。また、ケーブル・ポートを介して、TSB43AB2 などの統合型 1394 Link + PHY レイヤに接続することもできます。

表 3-1. 製品情報 セクション 15

部品番号	パッケージ	本体サイズ
TSB41BA3F-EP	80 ピン PFP	12.00mm × 12.00mm

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 1
2 アプリケーション 1
3 概要 1
4 Revision History 2
5 Terminal Configuration and Functions 3
Terminal Functions 3
6 Specifications 11
6.1 Absolute Maximum Ratings 11
6.2 ESD Ratings 11
6.3 Recommended Operating Conditions 12
6.4 Thermal Information 12
6.5 Electrical Characteristics - Driver 13
6.6 Electrical Characteristics - Receiver 13
6.7 Electrical Characteristics - Device 13
6.8 Switching Characteristics 13
7 Operating Life Deration 15
8 Parameter Measurement Information 16
9 Overview 17
10 Functional Block Diagram 21
11 Principles Of Operation (1394b Interface) 22
11.1 LLC Service Request 23
11.2 Status Transfer 26
11.3 Receive 28
11.4 Transmit 29
12 Principles Of Operation (1394a-2000 Interface) 33
12.1 LLC Service Request 34
12.2 Status Transfer 37
12.3 Receive 38
12.4 Transmit 39
12.5 Interface Reset and Disable 42
13 Applications, Implementation, and Layout 46
13.1 Known exceptions to functional specification (errata) 46
13.2 Application Information 46
14 Device and Documentation Support 66
14.1 Tools and Software 66
14.2 Device Nomenclature 66
14.3 Documentation Support 67
14.4 サポート・リソース 68
14.5 Trademarks 68
14.6 静電気放電に関する注意事項 68
14.7 用語集 68
15 Mechanical, Packaging, and Orderable Information 69
15.1 Packaging Information 69
15.2 Mechanical Data 70

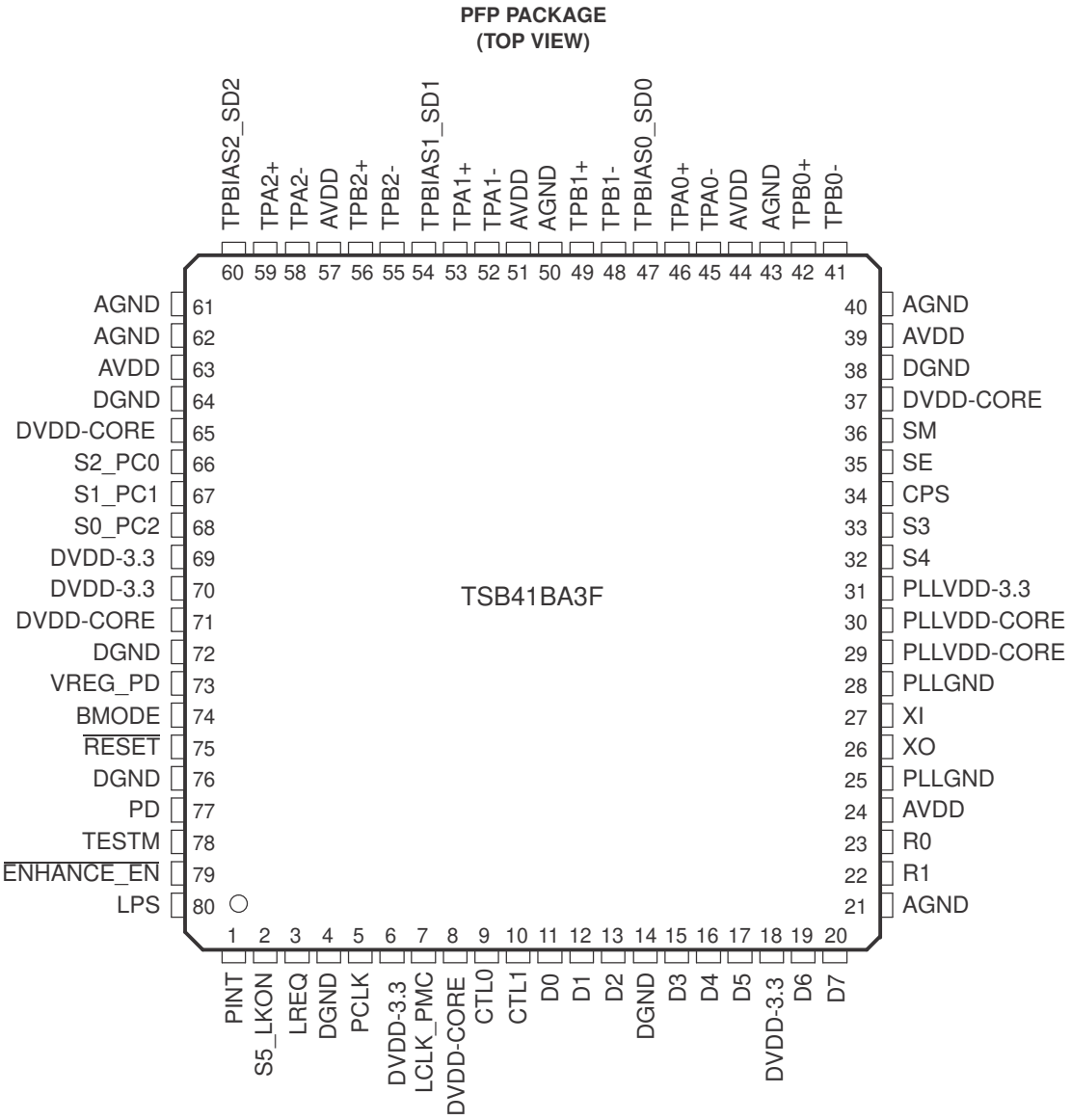
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2020	*	Initial Release

Copyright © 2023 Texas Instruments Incorporated

5 Terminal Configuration and Functions



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	PFP NO.		
AGND	Supply	21, 40, 43, 50, 61, 62	–	Analog circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
AVDD	Supply	24, 39, 44, 51, 57, 63	–	Analog circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. Lower frequency 10-µF filtering capacitors are also recommended. These supply terminals are separated from the PLLVDD-CORE, PLLVDD-3.3, DVDD-CORE, and DVDD-3.3 terminals internal to the device to provide noise isolation. The PLLVDD-3.3, AVDD, and DVDD-3.3 terminals must be tied together with a low dc impedance connection on the circuit board.

Copyright © 2023 Texas Instruments Incorporated

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	PFP NO.		
BMODE	CMOS	74	I	Beta-mode input. This terminal determines the PHY-link interface connection protocol. When logic-high (asserted), the PHY-link interface complies with the 1394b-2002 B PHY-link interface. When logic-low (deasserted), the PHY-link interface complies with the legacy 1394a-2000 standard. When using an LLC such as the 1394b-2002 TSB82AF15-EP, this terminal must be pulled high. When using an LLC such as the 1394a-2000 TSB12LV26, this terminal must be tied low. 注 NOTE: The PHY-link interface cannot be changed between the different protocols during operation.
CPS	CMOS	34	I	Cable-power status input. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This transition from cable power sensed to cable power not sensed can be used to generate an interrupt to the LLC.
CTL0 CTL1	CMOS	9 10	I/O	Control I/Os. These bidirectional signals control communication between the TSB41BA3F-EP and the LLC. Bus holders are built into these terminals.
D0–D7	CMOS	11, 12, 13, 15, 16, 17, 19, 20	I/O	Data I/Os. These are bidirectional data signals between the TSB82BA3 and the LLC. Bus holders are built into these terminals. If power management control (PMC) is selected using LCLK_PMC, then some of these terminals can be used for PMC. See the LCLK_PMC terminal description for more information.
DGND	Supply	4, 14, 38, 64, 72, 76		Digital circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
DVDD-CORE	Supply	8, 37, 65, 71	–	Digital core circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. An additional 1-µF capacitor is required for voltage regulation. These supply terminals are separated from the DVDD-3.3, PLLVDD-CORE, PLLVDD-3.3, and AVDD terminals internal to the device to provide noise isolation.
DVDD-3.3	Supply	6, 18, 69, 70	–	Digital 3.3-V circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. Lower-frequency 10-µF filtering capacitors are also recommended. The DVDD-3.3 terminals must be tied together at a low-impedance point on the circuit board. These supply terminals are separated from the PLLVDD-CORE, PLLVDD-3.3, DVDD-CORE, and AVDD terminals internal to the device to provide noise isolation. The PLLVDD-3.3, AVDD, and DVDD-3.3 terminals must be tied together with a low dc impedance connection on the circuit board.

Copyright © 2023 Texas Instruments Incorporated

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	PFP NO.		
LCLK_PMC	CMOS	7	I	Link clock. Link-provided 98.304-MHz clock signal to synchronize data transfers from link to the PHY. On hardware reset, this terminal is sampled to determine the power management control (PMC) mode. **LCLK_PMC** / **LPS** / **BMODE** / **Mode** H / L / H / No LLC (PMC mode) n/c[1] / lps / L / Legacy LLC LCLK_PMC[2] / lps / H / Beta LLC In PMC mode, because no LLC is attached, the data lines (D7–D0) are available to indicate power states. In PMC mode, the following signals are output: • D0—port 0 cable-power disable (see Note) • D1—port 1 cable-power disable (port in sleep or disabled) • D2—port 2 cable-power disable (port in sleep or disabled) • D6—All ports cable-power disable (all ports in sleep/disable) logical AND of bits D0–D2 • D3–D5 and D7 are reserved for future use. 注 NOTE: The cable-power disable is asserted when the port is either: • Hard-disabled (both the disabled and hard-disabled bits are set) • Sleep-disabled (both the disabled and sleep_enable bits are set) • Disconnected • Asleep • Connected in DS mode, but nonactive (that is, suspended or disabled) Otherwise, the cable-power disable output is deasserted (that is, cable power is enabled) when the port is dc-connected or active. A bus holder is built into this terminal.
LPS	CMOS	80	I	Link power status input. This terminal monitors the active/power status of the link-layer controller (LLC) and controls the state of the PHY-LLC interface. This terminal must be connected to either the V_{DD} supplying the LLC through an approximately 1-kΩ resistor or to a pulsed output which is active when the LLC is powered. A pulsed signal must be used when an isolation barrier exists between the LLC and PHY (see 図 13-7). The LPS input is considered inactive if it is sampled low by the PHY for more than an LPS_RESET time (~2.6 µs), and is considered active otherwise (that is, asserted steady high or an oscillating signal with a low time less than 2.6 µs). The LPS input must be high for at least 22 ns to be observed as high by the PHY. When the TSB41BA3F-EP detects that the LPS input is inactive, it places the PHY-LLC interface into a low-power reset state. In the reset state, the CTL (CTL0 and CTL1) and D (D0 to D7) outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than an LPS_DISABLE time (~26 µs), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The LLC state that is communicated in the self-ID packet is considered active only if both the LPS input is active and the LCtrl register bit is set to 1. The LLC state that is communicated in the self-ID packet is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	CMOS	3	I	LLC request input. The LLC uses this input to initiate a service request to the TSB41BA3F-EP. A bus holder is built into this terminal.

[1] Internal pulldown on LCLK_PMC
[2] LCLK_PMC from LLC normally low during reset

Copyright © 2023 Texas Instruments Incorporated

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	PFP NO.		
PCLK	CMOS	5	O	PHY clock. Provides a 98.304-MHz clock signal, synchronized with data transfers, to the LLC when the PHY-link interface is operating in the 1394b mode (BMODE asserted). PCLK output provides a 49.152-MHz clock signal, synchronized with data transfers, to the LLC when the PHY-link interface is in legacy 1394a-2000 (BMODE input deasserted).
PD	CMOS	77	I	Power-down input. A high on this terminal turns off all internal circuitry. Asserting the PD input high also activates an internal pulldown on the $\overline{\text{RESET}}$ terminal to force a reset of the internal control logic.
PINT	CMOS	1	O	PHY interrupt. The PHY uses this output to serially transfer status and interrupt information to the link when PHY-link interface is in the 1394b mode. A bus holder is built into this terminal.
PLLGND	Supply	25, 28	–	PLL circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
PLLVDD-CORE	Supply	29, 30	–	PLL core circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. An additional 1-µF capacitor is required for voltage regulation. The PLLVDD-CORE terminals must be separate from the DVDD-CORE terminals. These supply terminals are separated from the DVDD-CORE, DVDD-3.3, PLLVDD-3.3, and AVDD-3.3 terminals internal to the device to provide noise isolation.
PLLVDD-3.3	Supply	31	–	PLL 3.3-V circuit power terminal. A combination of high-frequency decoupling capacitors near the terminal are suggested, such as paralleled 0.1 µF and 0.001 µF. Lower frequency 10-µF filtering capacitors are also recommended. This supply terminal is separated from the DVDD-CORE, DVDD-3.3, PLLVDD-CORE, and AVDD-3.3 terminals internal to the device to provide noise isolation. The DVDD-3.3 terminals must be tied together at a low-impedance point on the circuit board. The PLLVDD-3.3, AVDD-3.3, and DVDD-3.3 terminals must be tied together with a low dc impedance connection.
$\overline{\text{RESET}}$	CMOS	75	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pullup resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation (see *power-up reset* in the *Application Information* section). The $\overline{\text{RESET}}$ terminal also incorporates an internal pulldown which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and can also be driven by an open-drain-type driver.
R0 R1	Bias	23 22	–	Current setting resistor terminals. These terminals are connected to a precision external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1% is required to meet the IEEE Std 1394-1995 output voltage limits.
SE	CMOS	35	I	Test control input. This input is used in the manufacturing test of the TSB41BA3F-EP. For normal use, this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
$\overline{\text{ENHANCE_EN}}$	CMOS	79	I	Enhancement Enable Formerly SLPEN Automotive sleep mode enable input. At power-on reset, FPR, FRT and FTD register values are set by $\overline{\text{ENHANCE_EN}}$. - When $\overline{\text{ENHANCE_EN}}$ is low FPR, FRT and FTD enhancements are enabled. - When $\overline{\text{ENHANCE_EN}}$ is high FPR, FRT and FTD enhancements are disabled. See セクション 13.2.3.**NOTE:** SLPEN has not been used in most applications. In most applications pin 79 SLPEN was tied to ground (low). If the TSB41BA3F-EP device is used as a drop-in replacement where pin 79 $\overline{\text{ENHANCE_EN}}$ is low, all three enhancements will be enabled without any hardware or software changes. If automotive sleep mode is required, then it would be required to use revision D or enable sleep mode through software programming of page 0 registers.
SM	CMOS	36	I	Test control input. This input is used in the manufacturing test of the TSB41BA3F-EP. For normal use this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
S2_PC0 S1_PC1 S0_PC2	CMOS	66 67 68	I	Port mode selection terminals 2-0 and power-class programming. On hardware reset, this terminal when used with the other five selection terminals allows the user to select the speed and mode of the ports. See 表 5-1. Depending on the selection, these inputs can set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high through a 1-kΩ resistor or by tying directly to ground through a 1-kΩ resistor. Bus holders are built into these terminals.

Copyright © 2023 Texas Instruments Incorporated

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	PFP NO.		
S3	CMOS	33	I	Port mode selection terminal 3. On hardware reset, this terminal when used with the other five selection terminals allows the user to select the speed and mode of the ports. See 表 5-1. Programming is done by tying the terminals high through a 1-kΩ or smaller resistor or by tying directly to ground through a 1-kΩ or smaller resistor. A bus holder is built into this terminal.
S4	CMOS	32	I	Port mode selection terminal 4. On hardware reset, this terminal when used with the other five selection terminals allows the user to select the speed and mode of the ports. See 表 5-1. Programming is done by tying the terminals high through a 1-kΩ or smaller resistor or by tying directly to ground through a 1-kΩ or smaller resistor. A bus holder is built into this terminal.
S5_LKON	CMOS	2	I/O	Port mode selection terminal 5 and link-on output. This terminal can be connected to the link-on input terminal of the LLC through a 1-kΩ resistor if the link-on input is available on the link layer. On hardware reset this terminal, when used with the other Port Speed/Mode Selection terminals, allows the user to select whether ports act like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal 1394b bilingual mode or high through a 1-kΩ or less resistor to enable 1394b bilingual mode or high through a 1-kΩ or less resistor to enable 1394a-2000-only mode. A bus holder is built into this terminal. See 表 5-1. A bus holder is built into this terminal. After hardware reset, this terminal is the link-on output, which notifies the LLC or other power-up logic to power up and become active. The link-on output is a square wave signal with a period of approximately 163 ns (8 PCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high-impedance. The link-on output is activated if the LLC is inactive (the LPS input inactive or the LCtrl bit cleared) and when one of the following occurs: 1. The PHY receives a link-on PHY packet addressed to this node. 2. The PEI (port-event interrupt) register bit is 1. 3. Any of the CTOI (configuration-timeout interrupt), CPSI (cable-power-status interrupt), or STOI (state-time-out interrupt) register bits is 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. 4. The PHY is power-cycled and the power class is 0 through 4. Once activated, the link-on output is active until the LLC becomes active (both the LPS input active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus-reset occurs unless the link-on output is otherwise active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet). In the case of power-cycling the PHY, the LKON signal must stop after 167 µs if the preceding conditions have not been met. 注 NOTE: If an interrupt condition exists which otherwise would cause the link-on output to be activated if the LLC were inactive, then the link-on output is activated when the LLC subsequently becomes inactive.
TESTM	CMOS	78	I	Test control input. This input is used in the manufacturing test of the TSB41BA3F-EP. For normal use this terminal must be pulled high through a 1-kΩ resistor to V_{DD}.
TPA0– TPA0+ TPB0– TPB0+	Cable	45 46 41 42	I/O	Port-0 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.

Copyright © 2023 Texas Instruments Incorporated

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	PFP NO.		
TPA1– TPA1+ TPB1– TPB1+	Cable	52 53 48 49	I/O	Port-1 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPA2– TPA2+ TPB2– TPB2+	Cable	58 59 55 56	I/O	Port-2 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPBIAS0_SD0 TPBIAS1_SD1 TPBIAS2_SD2	Cable In	47 54 60	I/O	Twisted-pair bias output and signal detect input. This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection in 1394a-2000 mode. Each of these terminals, except for an unused port, must be decoupled with a 1-µF capacitor to ground. For the unused port, this terminal can be left unconnected. When a port is configured as a Beta-mode port (B1, B2, B4) this terminal becomes an input and must be high when a valid signal is present. For optical transceivers, the signal detect of the transceiver must be connected to this terminal. The input is an LVCMOS level input.
VREG_PD	CMOS	73	I	Voltage regulator power-down input. When asserted logic-high through a 1kΩ resistor, this terminal powers down the internal 3.3-V-to-1.8-V regulator. For single-supply (3.3-V only) operation, this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND. (If there is high system noise or ground bounce expected, smaller resistor will offer more immunity)
XI XO	Crystal	27 26	I O	Crystal oscillator inputs. These terminals connect to a 49.152-MHz parallel-resonant fundamental-mode crystal. The optimum values for the external shunt capacitors depend on the specifications of the crystal used (see the *crystal selection* section in the *TSB41AB3 IEEE 1394a-2000 Three-Port Cable Transceiver/Arbiter* data sheet, SLLS418. XI is a 1.8-V CMOS input.

Copyright © 2023 Texas Instruments Incorporated

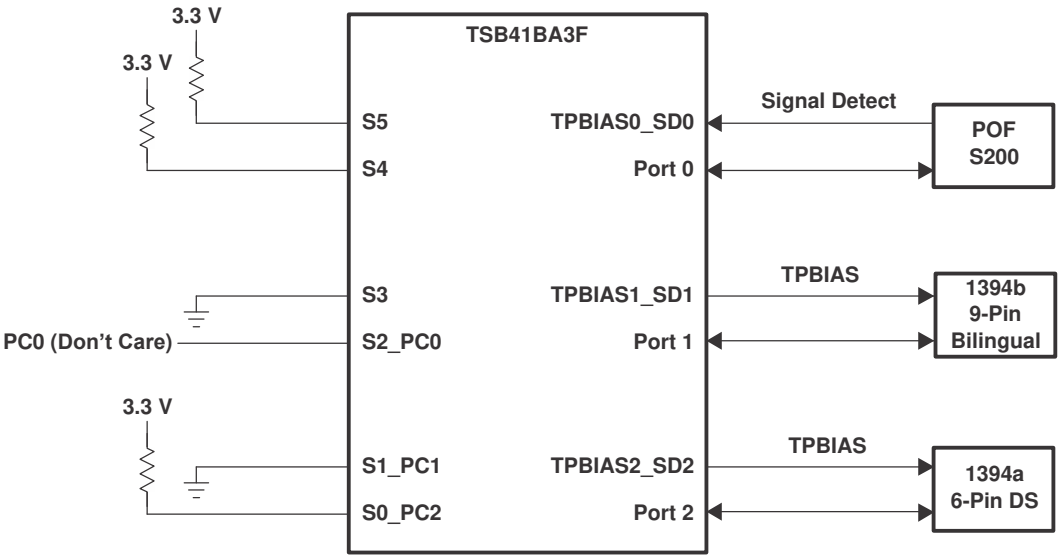
表 5-1. Port Speed/Mode Selection

MODE NO.	INPUT SELECTION						RESULTING PORT, POWER CLASS, AND SELF-ID							
	S5_ LKON	S4	S3	S2_ PC0	S1_ PC1	S0_ PC2	PORT(1)						POWER CLASS	SELF-ID
							2		1		0			
1	0	0	0	PC0	PC1	PC2	Bi	T	Bi	T	Bi	T	PC = (PC0, PC1, PC2)	1394b
2	0	0	1	PC0	PC1	PC2	DS	T	Bi	T	Bi	T	PC = (PC0, PC1, PC2)	1394b
3	0	1	0	PC0	PC1	PC2	DS	T	DS	T	Bi	T	PC = (PC0, PC1, PC2)	1394b
4	0	1	1	0	0	0	B1	S	B1	S	B1	S	PC = 000	1394b
5	0	1	1	0	0	1	B2	S	B2	S	B2	S	PC = 000	1394b
6	0	1	1	0	1	0	B4	S	B4	S	B4	S	PC = 000	1394b
7	0	1	1	0	1	1	B2	S	Bi	T	B4	S	PC = 100	1394b
8	0	1	1	1	0	0	B1	S	DS	T	DS	T	PC = 100	1394a S100 (2)
9	0	1	1	1	0	1	DS	T	DS	T	B2	S	PC = 100	1394b
10	0	1	1	1	1	0	DS	T	DS	T	B4	S	PC = 100	1394b
11	0	1	1	1	1	1	B2	S	DS	T	B4	S	PC = 100	1394b
12	1	0	0	PC0	0	0	B1	S	Bi	T	B1	S	PC = PC0,0,0 (100 or 000)	1394b
13	1	0	0	PC0	0	1	B2	S	Bi	T	B2	S	PC = PC0,0,0 (100 or 000)	1394b
14	1	0	0	PC0	1	0	B4	S	Bi	T	B4	S	PC = PC0,0,0 (100 or 000)	1394b
15	1	0	0	PC0	1	1	B1	S	Bi	T	B2	S	PC = PC0,0,0 (100 or 000)	1394b
16	1	0	1	PC0	0	0	Bi	T	Bi	T	B1	S	PC = PC0,0,0 (100 or 000)	1394b
17	1	0	1	PC0	0	1	Bi	T	Bi	T	B2	S	PC = PC0,0,0 (100 or 000)	1394b
18	1	0	1	PC0	1	0	Bi	T	Bi	T	B4	S	PC = PC0,0,0 (100 or 000)	1394b
19	1	0	1	PC0	1	1	B1	S	Bi	T	B4	S	PC = PC0,0,0 (100 or 000)	1394b
20	1	1	0	PC0	0	0	DS	T	Bi	T	B1	S	PC = PC0,0,0 (100 or 000)	1394b
21	1	1	0	PC0	0	1	DS	T	Bi	T	B2	S	PC = PC0,0,0 (100 or 000)	1394b
22	1	1	0	PC0	1	0	DS	T	Bi	T	B4	S	PC = PC0,0,0 (100 or 000)	1394b
23	1	1	0	PC0	1	1	B1	S	DS	T	B2	S	PC = PC0,0,0 (100 or 000)	1394b
24	1	1	1	PC0	0	0	B1	S	DS	T	B1	S	PC = PC0,0,0 (100 or 000)	1394b
25	1	1	1	PC0	0	1	B2	S	DS	T	B2	S	PC = PC0,0,0 (100 or 000)	1394b
26	1	1	1	PC0	1	0	B4	S	DS	T	B4	S	PC = PC0,0,0 (100 or 000)	1394b
27	1	1	1	PC0	1	1	B1	S	DS	T	B4	S	PC = PC0,0,0 (100 or 000)	1394b

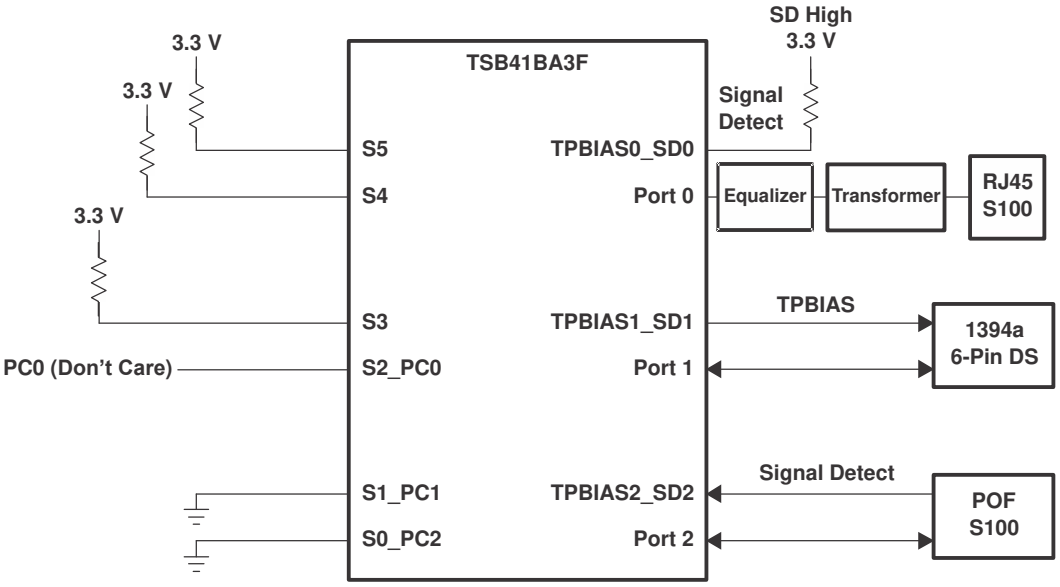
(1) LEGEND:
Bi = 1394b-2002 bilingual (S400b only Beta operating speed and data strobe: S400, S200, and S100 operating speeds)
DS = 1394a-2000, data strobe-only, S400, S200, and S100 operating speeds
B1 = 1394b-2002 Beta-only, S100b operating speed
B2 = 1394b-2002 Beta-only, S200b and S100b operating speeds
B4 = 1394b-2002 Beta-only, S400b, S200b, and S100b operating speeds
S = TPBIAS#_SD# terminal is in signal detect input mode
T = TPBIAS#_SD# terminal is in TPBIAS output mode

(2) Mode 8 must only be used to do an S100 home network translation. It must not be used as a nominal end equation mode.

Copyright © 2023 Texas Instruments Incorporated



Mode 21, Port/Speed Mode (1, 1, 0, PC0, 0, 1)



Mode 24, Port/Speed Mode (1, 1, 1, PC0, 0, 0)

Copyright © 2023 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD18}	Supply voltage range(1)	DVDD-CORE, PLLVDD-CORE	–0.3	2.1	V
V_{DD33}	Supply voltage range(1)	DVDD-3.3,PLLVDD-3.3, AVDD	–0.3	4	V
V_{I33}	Input voltage range(1)	Sx, Sx_PCx, VREG_PD, PD, LPS, LREQ, LCLK, CTLx, Dx, CPS. SLPEN, RESET, BMODE, TESTM, SDx	–0.5	V_{DD33} + 0.5	V
V_{O33}	Output voltage range at any output(1)	PINT, PCLK, CTLx, Dx, LKON,	–0.5	V_{DD33} + 0.5	V
V_A	Analog I/O voltage range(1)	TPAx. TPBx	–0.5	V_{DD33}	V
V_R	Reference voltage range(1)	only R1 (R0 is internal ground reference)	–0.5	2.1	V
V_X	Clock input voltage range(1)	XI, XO	–0.5	V_{DD18}	V
T_J	Absolute maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

(1) All voltage values, except differential I/O bus voltages, are with respect to network ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2023 Texas Instruments Incorporated

6.3 Recommended Operating Conditions

		MIN	TYP(1)	MAX	UNIT
Supply voltage, 3.3 V_{DD33}	Source power node	3	3.3	3.6	V
	Nonsource power node	3(2)	3.3	3.6	
Supply voltage, 1.8 V_{DD18}	Core voltage	1.75	1.85	2	V
High-level input voltage, V_{IH}	LREQ, CTL0, CTL1, D0–D7, LCLK_PMC	0.7 V_{DD33}			V
	S5_LKON, S4, S3, S2_PC0, S1_PC1, S0_PC2, SLPEN, PD, BMODE, TPBIAS0_SD0, TPBIAS1_SD1, TPBIAS2_SD2	0.7 V_{DD33}			
	$\overline{\text{RESET}}$	0.6 V_{DD33}			
Low-level input voltage, V_{IL}	LREQ, CTL0, CTL1, D0–D7, LCLK_PMC			0.25 V_{DD33}	V
	S5_LKON, S4, S3, S2_PC0, S1_PC1, S0_PC2, SLPEN, PD, BMODE, TPBIAS0_SD0, TPBIAS1_SD1, TPBIAS2_SD2			0.2 V_{DD33}	
	$\overline{\text{RESET}}$			0.3 V_{DD33}	
Output current, $I_{OL/OH}$	CTL0, CTL1, D0–D7, S5_LKON, PINT, PCLK	–4		4	mA
Output current, I_O	TPBIAS outputs	–5.6		1.3	mA
T_A	Operating temperature (free-air)	-40		110	°C
T_J	Operating junction temperature	-40		125	°C
1394b Differential input voltage, V_{ID}	Cable inputs, during data reception	200		800	mV
1394a Differential input voltage, V_{ID}	Cable inputs, during data reception	118		260	mV
	Cable inputs, during arbitration	168		265	
1394a Common-mode input voltage, V_{IC}	TPB cable inputs, source power node	0.4706		2.515	V
	TPB cable inputs, nonsource power node	0.4706		2.015(2)	
Power-up reset time, t_{pu}	$\overline{\text{RESET}}$ input	2(3)			ms
1394a receive input jitter	TPA, TPB cable inputs, S100 operation			±1.08	ns
	TPA, TPB cable inputs, S200 operation			±0.5	
	TPA, TPB cable inputs, S400 operation			±0.315	
1394a receive input skew	Between TPA and TPB cable inputs, S100 operation			±0.8	ns
	Between TPA and TPB cable inputs, S200 operation			±0.55	
	Between TPA and TPB cable inputs, S400 operation			±0.5	

(1) All typical values are at V_{DD} = 3.3 V and T_A = 25°C.
(2) For a node that does not source power, see Section 4.2.2.2 in IEEE 1394a-2000.
(3) Time after valid clock received at PHY XI input terminal.

6.4 Thermal Information

THERMAL METRIC(1)		HTQFP (PFP)	UNIT
		80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

Copyright © 2023 Texas Instruments Incorporated

6.5 Electrical Characteristics - Driver

over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OD}	1394a differential output voltage	56 Ω, See 図 8-1	172		265	mV
V_{OD}	1394b differential output voltage		300	700	800	mV
I_{DIFF}	Driver difference current, TPA+, TPA–, TPB+, TPB–	Drivers enabled, speed signaling off	–1.05(1)		1.05(1)	mA
I_{SP200}	Common-mode speed signaling current, TPB+, TPB–	S200 speed signaling enabled	–4.84(2)		–2.53(2)	mA
I_{SP400}	Common-mode speed signaling current, TPB+, TPB–	S400 speed signaling enabled	–12.4(2)		–8.1(2)	mA
V_{OFF}	Off-state differential voltage	Drivers disabled, See 図 8-1			20	mV

(1) Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
(2) Limits defined as absolute limit of each TPB+ and TPB– driver currents.

6.6 Electrical Characteristics - Receiver

over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30		30	mV
V_{TH-CB}	Cable bias detect threshold, TPBx cable inputs	Drivers disabled	0.6		1	V
$V_{TH}+$	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
$V_{TH}–$	Negative arbitration comparator threshold voltage	Drivers disabled	–168		–89	mV
$V_{TH-SP200}$	Speed signal threshold	TPBIAS–TPA common-mode voltage, drivers disabled	49		131	mV
$V_{TH-SP400}$	Speed signal threshold		314		396	mV

6.7 Electrical Characteristics - Device

over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current 3.3 V_{DD33}	See (1)		110	150	mA
V_{TH}	Power status threshold, CPS input(2)	400-kΩ resistor(2)	4.7		7.5	V
V_{OH}	High-level output voltage, CTL0, CTL1, D0–D7, PCLK, S5_LKON outputs	V_{DD33} = 3 to 3.6 V, I_{OH} = –4 mA	0.85 V_{DD33}			V
V_{OL}	Low-level output voltage, CTL0, CTL1, D0–D7, PCLK, S5_LKON outputs	I_{OL} = 4 mA			0.22 V_{DD33}	V
I_{OZ}	Off-state output current, CTL0, CTL1, D0–D7, S5_LKON I/Os	V_O = V_{DD33} or 0 V			±20	μA
I_{IRST}	Pullup current, $\overline{RESET}$ input	V_I = 1.5 V or 0 V	–90		–20	μA
V_O	TPBIAS output voltage	At rated I_O current	1.665		2.015	V

(1) Repeat max packet (one port receiving maximum size isochronous packet–4096 bytes, sent on every isochronous interval, data value of 0x00FF 00FFh; two ports repeating; all ports with S400 Beta-mode connection), $V_{DD3.3}$ = 3.3 V, internal regulator, T_A = 25°C
(2) Measured at cable-power side of resistor

6.8 Switching Characteristics

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
t_r	TP differential rise time, transmit	1394a-2000	10% to 90%, At 1394 connector	0.3		0.8	ns
		1394b-2002 S400B		80		800	ps

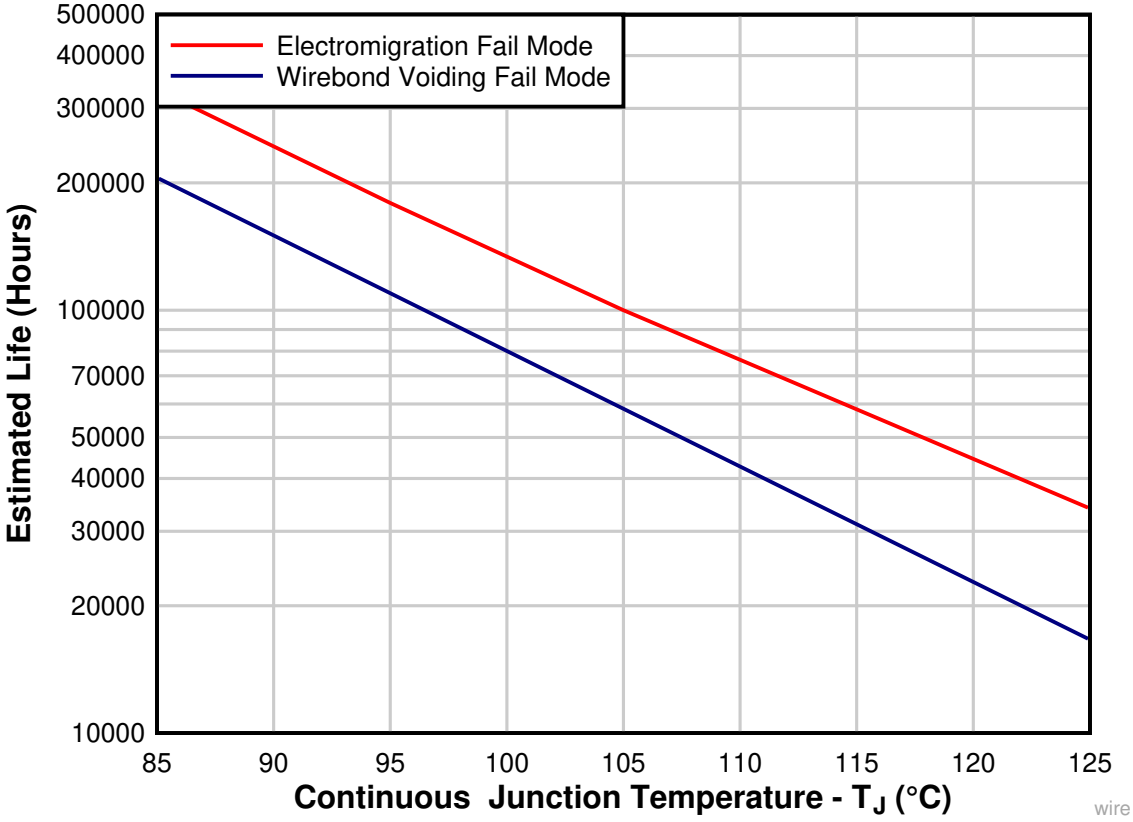
Copyright © 2023 Texas Instruments Incorporated

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
t_f	TP differential fall time, transmit	1394a-2000	90% to 10%, At 1394 connector	0.3		0.8	ns
		1394b-2002 S400B		80		800	ps
t_{su}	Setup time, CTL0, CTL1, D0–D7, LREQ to PCLK	1394a-2000	50% to 50%, See 図 8-2	2.5			ns
t_h	Hold time, CTL0, CTL1, D0–D7, LREQ after PCLK	1394a-2000	50% to 50%, See 図 8-2	0			ns
t_{su}	Setup time, CTL0, CTL1, D0–D7, LREQ to LCLK_PMC	1394b	50% to 50%, See 図 8-2	2.5			ns
t_h	Hold time, CTL0, CTL1, D0–D7, LREQ after LCLK_PMC	1394b	50% to 50%, See 図 8-3	0			ns
t_d	Delay time, PCLK to CTL0, CTL1, D0–D7, PINT	1394a-2000 and 1394b-2002	50% to 50%, See 図 8-3	0.5	1.6		ns

Copyright © 2023 Texas Instruments Incorporated

7 Operating Life Deration

The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.



A. Silicon operating life design goal is 100000 power-on hours (POH) at 105°C junction temperature (does not include package interconnect life).

B. The predicted operating lifetime versus junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

図 7-1. TSB41BA3F-EP Operating Life Derating Chart

Copyright © 2023 Texas Instruments Incorporated

8 Parameter Measurement Information

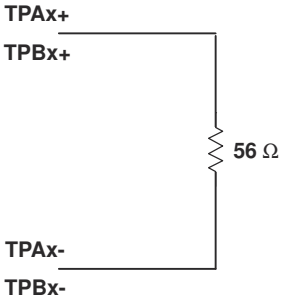


図 8-1. Test Load Diagram

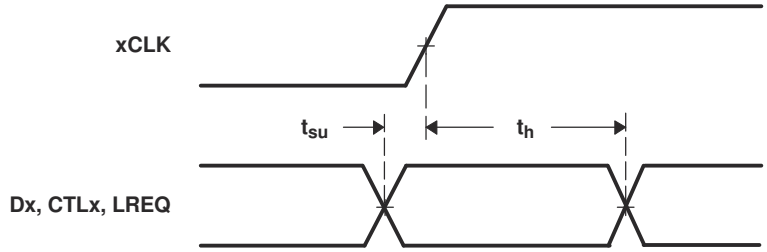


図 8-2. Dx, CTLx, LREQ Input Setup and Hold Time Waveforms

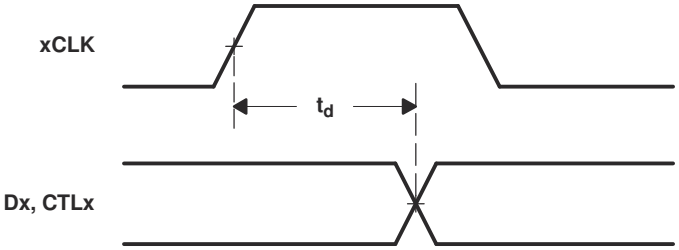


図 8-3. Dx and CTLx Output Delay Relative to xCLK Waveforms

Copyright © 2023 Texas Instruments Incorporated

9 Overview

The TSB41BA3F-EP is powered by a single 3.3-V supply. The core voltage supply is supplied by an internal voltage regulator to the PLLVDD-CORE and DVDD-CORE terminals. To protect the phase-locked loop (PLL) from noise, the PLLVDD-CORE terminals must be separately decoupled from the DVDD-CORE terminals. The PLLVDD-CORE terminals are decoupled with 1-µF and smaller decoupling capacitors and the DVDD-CORE terminals are separately decoupled with 1-µF and smaller decoupling capacitors. The separation between DVDD-CORE and PLLVDD-CORE must be implemented by separate power supply rails or planes.

The TSB41BA3F-EP can be powered by dual supplies, a 3.3-V supply for I/O and a core voltage supply. The core voltage supply is supplied to the PLLVDD-CORE and DVDD-CORE terminals to the requirements in the *recommended operating conditions* section of this data sheet. The PLLVDD-CORE terminals must be separated from the DVDD-CORE terminals, the PLLVDD-CORE terminals are decoupled with 1-µF and smaller decoupling capacitors and the DVDD-CORE terminals separately decoupled with 1-µF and smaller decoupling capacitors. The separation between DVDD-CORE and PLLVDD-CORE can be implemented by separate power supply rails, or by a single power supply rail, where the DVDD-CORE and PLLVDD-CORE are separated by a filter network to keep noise from the PLLVDD-CORE supply.

The TSB41BA3F-EP requires an external 49.152-MHz crystal to generate a reference clock. The external clock drives an internal PLL, which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. A 49.152-MHz clock signal is supplied by the PHY to the associated LLC for synchronization of the two devices and is used for resynchronization of the received data when operating the PHY-link interface in compliance with the IEEE 1394a-2000 standard. A 98.304-MHz clock signal is supplied by the PHY to the associated LLC for synchronization of the two devices when operating the PHY-link interface in compliance with the IEEE 1394b-2002 standard. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

Data bits to be transmitted through the cable ports are received from the LLC on 2, 4, or 8 parallel paths (depending on the requested transmission speed and PHY-link interface mode of operation). They are latched internally, combined serially, encoded, and transmitted at 98.304, 122.78, 196.608, 245.76, 393.216, or 491.52 Mbps (referred to as S100, S100B, S200, S200B, S400, or S400B speed, respectively) as the outbound information stream.

The PHY-link interface can follow either the IEEE 1394a-2000 protocol or the IEEE 1394b-2002 protocol. When using a 1394a-2000 LLC such as the TSB12LV26, the BMODE terminal must be deasserted. The PHY-link interface then operates in accordance with the legacy 1394a-2000 standard. When using a 1394b LLC such as the TSB82AF15-EP, the BMODE terminal must be asserted. The PHY-link interface then conforms to the 1394b-2002 standard.

The cable interface can follow either the IEEE 1394a-2000 protocol or the 1394b protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When any of the three ports is connected to a 1394a-2000-compliant device, the cable interface on that port operates in the 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to a 1394b-compliant node, the cable interface on that port operates per the 1394b-2002 standard at S100B, S200B, or S400B speed. The TSB41BA3F-EP automatically determines the correct cable interface connection method for the bilingual ports.

注

The BMODE terminal does not select the cable interface mode of operation. The BMODE terminal selects the PHY-link interface mode of operation and affects the arbitration modes on the cable. When the BMODE terminal is deasserted, the PHY-link interface is placed in 1394a-2000 mode and BOSS arbitration is disabled. When the BMODE terminal is asserted, the PHY-link interface is placed in 1394b-2002 mode and BOSS arbitration is enabled.

During packet reception, the serial data bits are split into 2-, 4-, or 8-bit parallel streams (depending on the indicated receive speed and the PHY-link interface mode of operation), resynchronized to the local system clock,

Copyright © 2023 Texas Instruments Incorporated

and sent to the associated LLC. The received data is also transmitted (repeated) on the other connected and active cable ports.

Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to a 1394a-2000-compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during 1394a-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to a 1394a-2000-compliant node, the TSB41BA3F-EP provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB41BA3F-EP are designed to work with external 112-Ω termination resistor networks in order to match the 110-Ω cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected ~56-Ω resistors. The midpoint of the pair of resistors that is connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 270 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

When the power supply of the TSB41BA3F-EP is off while the twisted-pair cables are connected, the TSB41BA3F-EP transmitter and receiver circuitry present a high-impedance signal to the cable that does not load the device at the other end of the cable.

When the TSB41BA3F-EP is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the preferred method is for the port to be forced to the 1394a-only mode (data-strobe-only mode, DS), then the TPB+ and TPB– terminals can be tied together and then pulled to ground; or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS#_SD# terminal can be left unconnected.

If the port is left in bilingual (Bi) mode, then the TPB+ and TPB– terminals can be left unconnected or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS#_SD# terminal can be left unconnected.

If the port is left in a forced 1394b Beta-only (B1, B2, or B4) mode, then the TPB+ and TPB– terminals can be left unconnected or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS#_SD# terminal must be pulled to ground through a 1.2-kΩ or smaller resistor.

To operate a port as a 1394b bilingual port, the speed/mode selections terminals (S5_LKON, S4, S3, S2_PC0, S1_PC1, and S0_PC2) need to be pulled to V_{CC} or ground through a 1-kΩ resistor. The port must be operated in the 1394b bilingual mode whenever a 1394b bilingual or a 1394b Beta-only connector is connected to the port. To operate the port as a 1394a-only port, the speed/mode selection terminals must be configured correctly to force 1394a-2000-only operation on that port. The only time the port must be forced to the data-strobe-only mode is if the port is connected to a 1394a connector (either 6-pin, which is recommended, or 4-pin). This mode is provided to ensure that 1394b signaling is never sent across a 1394a cable.

Copyright © 2023 Texas Instruments Incorporated

注

A bilingual port can only connect to a 1394b-only port that operates at S400b. It cannot establish a connection to a S200b or S100b port. A port that has been forced to S400b (B4) can connect to a 1394b-only port at S400b (B4) or S200b (B2) or S100b (B1). A port that has been forced to S200b can connect to a 1394b-only port at S200b or S100b. A port that has been forced to S100b can only connect to a 1394b-only port at S100b.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal must be connected to V_{DD} through a 1-kΩ resistor. The SE and SM terminals must be tied to ground through a 1-kΩ resistor.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. In some speed/mode selections the S2_PC0, S1_PC1, and S0_PC2 terminals indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable); see 表 5-1. The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the TSB41BA3F-EP, this bit can only be set by a write to the PHY register set. If a node is a contender for IRM or BM, then the node software must set this bit in the PHY register set.

The LPS (link power status) terminal works with the S5_LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used with the LCtrl bit (see 表 13-1 and 表 13-2 in the APPLICATION INFORMATION section) to indicate the active/power status of the LLC. The LPS signal also resets, disables, and initializes the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

注

The TSB41BA3F-EP does not have a cable-not-active (CNA) terminal. To achieve a similar function, the individual PHY ports can be set up to issue interrupts whenever the port changes state. If the LPS terminal is low, then this generates a link-on (LKON) output clock. See register bits PIE, PEI, and WDIE along with the individual interrupt bits.

The LPS input is considered inactive if it remains low for more than the LPS_RESET time (see the LPS terminal definition) and is considered active otherwise. When the TSB41BA3F-EP detects that the LPS input is inactive, the PHY-LLC interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS_DISABLE time (see the LPS terminal definition), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The TSB41BA3F-EP continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY initializes the interface and returns to normal operation. The PHY-LLC interface is also held in the disabled state during hardware reset. When the LPS terminal is returned to an active state after being sensed as having entered the LPS_DISABLE time, the TSB41BA3F-EP issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY LLC now being accessible).

The PHY uses the S5_LKON terminal to notify the LLC to power up and become active. When activated, the output S5_LKON signal is a square wave. The PHY activates the S5_LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as previously described, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the S5_LKON output when the LLC becomes active (both LPS sensed as active and the LCtrl bit set to 1). The PHY also deasserts the S5_LKON output when a bus reset occurs, unless a PHY interrupt condition exists which would otherwise cause S5_LKON to be active. If the PHY is power-cycled and the power class is 0 through 4, then the PHY asserts S5_LKON for approximately 167 µs or until both the LPS is active and the LCtrl bit is 1.

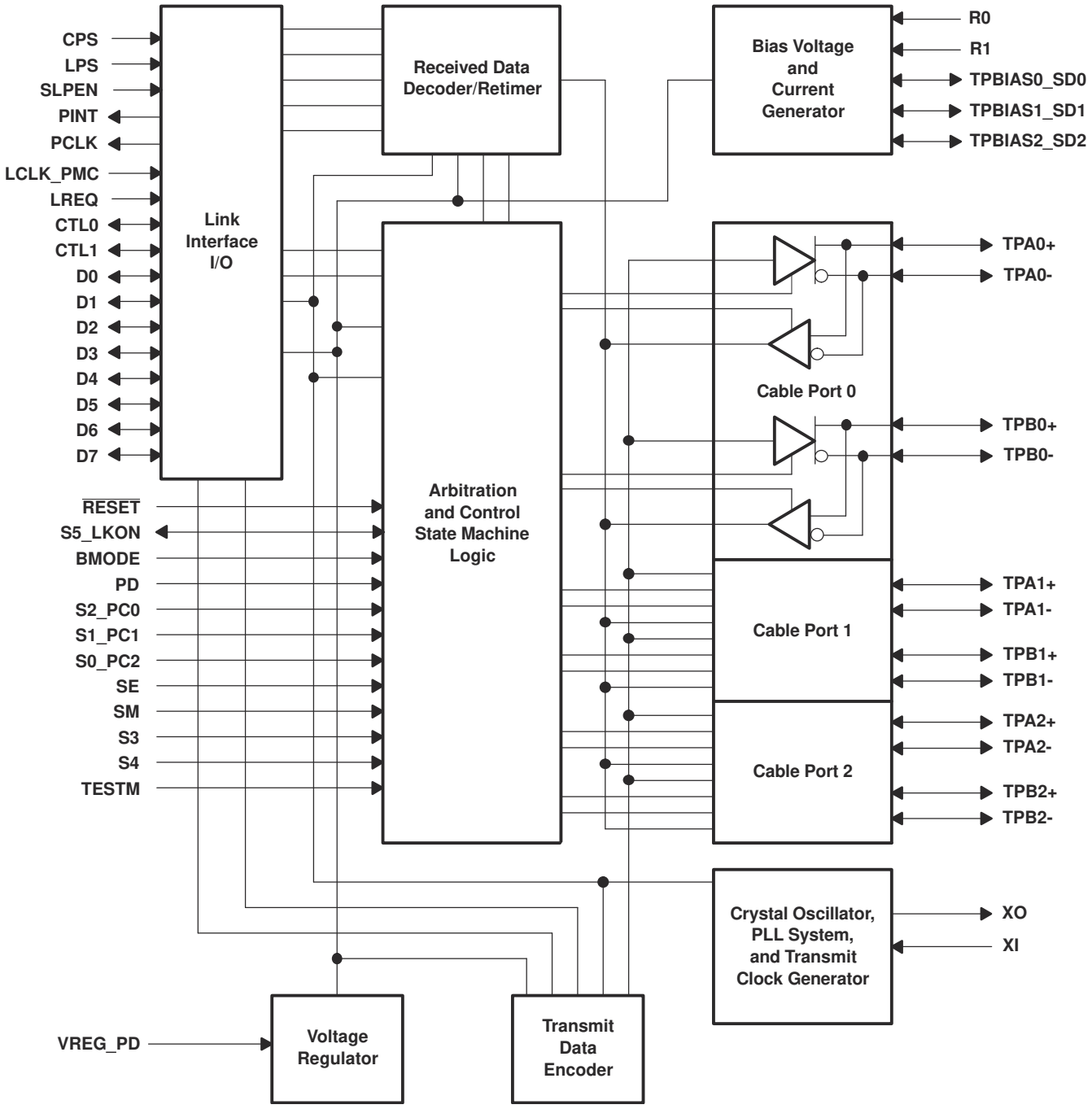
Copyright © 2023 Texas Instruments Incorporated

注

Revision F of the TSB41BA3 contains feature enhancements that may impact ability to be drop in replacement with revision D or prior. See セクション 13.2.3 for further details.

Copyright © 2023 Texas Instruments Incorporated

10 Functional Block Diagram



11 Principles Of Operation (1394b Interface)

The TSB41BA3F-EP is designed to operate with an LLC such as the Texas Instruments TSB82AF15-EP when the BMODE terminal is tied high. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface. This interface is formally specified in the IEEE 1394b-2002 standard.

The interface to the LLC consists of the PCLK, LCLK_PMC, CTL0–CTL1, D0–D7, LREQ, PINT, LPS, and S5_LKON terminals on the TSB41BA3F-EP, as shown in 図 11-1.

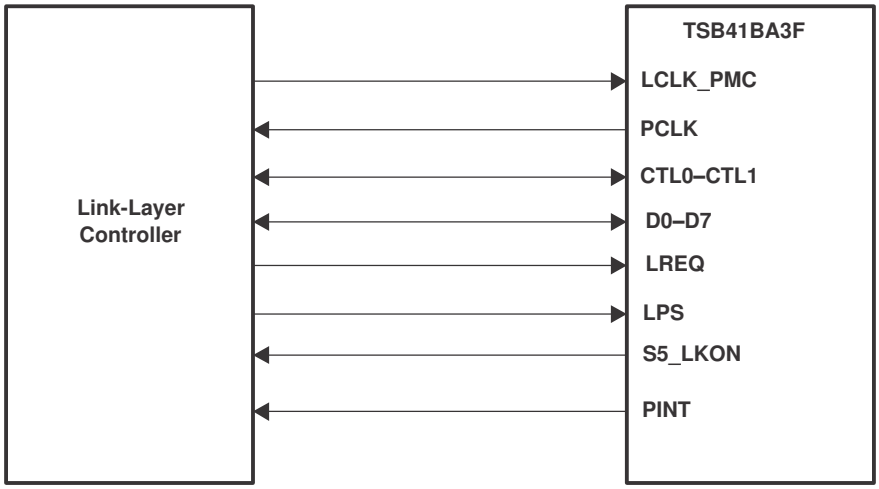


図 11-1. PHY-LLC Interface

The LCLK_PMC terminal provides a clock signal to the PHY. The LLC derives this clock from the PCLK signal and is phase-locked to the PCLK signal. All LLC to PHY transfers are synchronous to LCLK_PMC.

The PCLK terminal provides a 98.304-MHz interface system clock. All control, data, and PHY interrupt signals are synchronized to the rising edge of PCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB41BA3F-EP and LLC.

The D0–D7 terminals form a bidirectional data bus, which transfers status information, control information, or packet data between the devices. The TSB41BA3F-EP supports S400B, S200B, and S100B data transfers over the D0–D7 data bus. In S400B, S200B, and S100B operation, all Dn terminals are used.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY in order to request access to the serial bus for packet transmission, read or write PHY registers, or control arbitration acceleration. All data on LREQ is synchronous to LCLK_PMC.

The LPS and S5_LKON terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC, and can be used to reset the PHY-LLC interface or to disable PCLK. The S5_LKON terminal sends a wake-up notification to the LLC and indicates an interrupt to the LLC when either LPS is inactive or the PHY register L bit is 0.

The PINT terminal is used by the PHY for the serial transfer of status, interrupt, and other information to the LLC.

The TSB41BA3F-EP normally controls the CTL0–CTL1 and D0–D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

Four operations can occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register or to request the PHY to gain control of the serial bus in order to transmit a packet.

Copyright © 2023 Texas Instruments Incorporated

The PHY can initiate a status transfer either autonomously or in response to a register read request from the LLC.

The PHY initiates a receive operation whenever a packet is received from the serial bus.

The PHY initiates a transmit operation after winning control of the serial bus following a bus request by the LLC. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

表 11-1 and 表 11-2 show the encoding of the CTL0–CTL1 bus.

表 11-1. CTL Encoding When PHY Has Control of the Bus

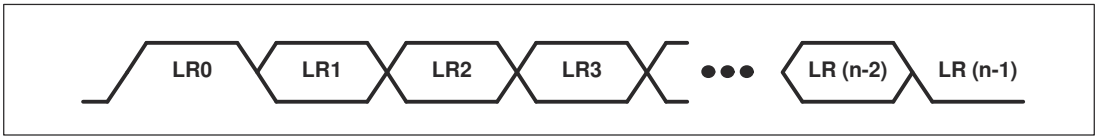
CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC.
1	0	Receive	An incoming packet is being sent from the PHY to the LLC.
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet.

表 11-2. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Transmit	An outgoing packet is being sent from the LLC to the PHY.
1	0	Reserved	Reserved
1	1	Holation	The LLC is holding the bus while data is being prepared for transmission, or the LLC is sending a request to arbitrate for access to the bus, or the LLC is identifying the end of a subaction gap to the PHY.

11.1 LLC Service Request

To request access to the bus, to read or write a PHY register, or to send a link notification to PHY, the LLC sends a serial bit stream on the LREQ terminal as shown in 図 11-2.



Each cell represents one clock sample period, and n is the number of bits in the request stream.

図 11-2. LREQ Request Stream

The length of the stream varies depending on the type of request as shown in 表 11-3.

表 11-3. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	11
Read register request	10
Write register request	18
Link notification request	6
PHY-link interface reset request	6

Regardless of the type of request, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream. The second through fifth bits of the request stream indicate the type of the request. In the following descriptions, bit LR1 is the most significant and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Copyright © 2023 Texas Instruments Incorporated

表 11-4 shows the encoding for the request type.

表 11-4. Request Type Encoding

LR1–LR4	NAME	DESCRIPTION
0000	Reserved	Reserved
0001	Immed_Req	Immediate request. On detection of idle, the PHY arbitrates for the bus.
0010	Next_Even	Next even request. The PHY arbitrates for the bus to send an asynchronous packet in the even fairness interval phase.
0011	Next_Odd	Next odd request. The PHY arbitrates for the bus to send an asynchronous packet in the odd fairness interval phase.
0100	Current	Current request. The PHY arbitrates for the bus to send an asynchronous packet in the current fairness interval.
0101	Reserved	Reserved
0110	Isoch_Req_Even	Isochronous even request. The PHY arbitrates for the bus to send an isochronous packet in the even isochronous period.
0111	Isoch_Req_Odd	Isochronous odd request. The PHY arbitrates for the bus to send an isochronous packet in the odd isochronous period.
1000	Cyc_Start_Req	Cycle start request. The PHY arbitrates for the bus to send a cycle start packet.
1001	Reserved	Reserved
1010	Reg_Read	Register read request. The PHY returns the specified register contents through a status transfer.
1011	Reg_Write	Register write request. Write to the specified register in the PHY.
1100	Isoch_Phase_Even	Isochronous phase even notification. The link reports to the PHY that: 1) A cycle start packet has been received. 2) The link has set the isochronous phase to even.
1101	Isoch_Phase_Odd	Isochronous phase odd notification. The link reports to the PHY that: 1) A cycle start packet has been received. 2) The link has set the isochronous phase to odd.
1110	Cycle_Start_Due	Cycle start due notification. The link reports to the PHY that a cycle start packet is due for reception.
1111	Reserved	Reserved

For a bus request, the length of the LREQ bit stream is 11 bits as shown in 表 11-5.

表 11-5. Bus Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	Indicates the type of bus request. See 表 11-4.
5	Request format	Indicates the packet format to be used for packet transmission. See 表 11-6.
6–9	Request speed	Indicates the speed at which the link sends the data to the PHY. See 表 11-7 for the encoding of this field.
10	Stop bit	Indicates the end of the transfer (always 0). If bit 6 is 0, then this bit can be omitted.

表 11-6 shows the 1-bit request format field used in bus requests.

表 11-6. Bus Request Format Encoding

LR5	DATA RATE
0	Link does not request either Beta or legacy packet format for bus transmission
1	Link requests Beta packet format for bus transmission

表 11-7 shows the 4-bit request speed field used in bus requests.

Copyright © 2023 Texas Instruments Incorporated

表 11-7. Bus Request Speed Encoding

LR6–LR9	DATA RATE
0000	S100
0001	Reserved
0010	S200
0011	Reserved
0100	S400
0101	Reserved
0110	S800
All Others	Invalid

注

The TSB41BA3F-EP accepts a bus request with an invalid speed code and processes the bus request normally. However, during packet transmission for such a request, the TSB41BA3F-EP ignores any data presented by the LLC and transmits a null packet.

For a read register request, the length of the LREQ bit stream is 10 bits as shown in 表 11-8.

表 11-8. Read Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	A 1010 indicates this is a read register request.
5–8	Address	Identifies the address of the PHY register to be read
9	Stop bit	Indicates the end of the transfer (always 0)

For a write register request, the length of the LREQ bit stream is 18 bits as shown in 表 11-9.

表 11-9. Write Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	A 1011 indicates this is a write register request.
5–8	Address	Identifies the address of the PHY register to be written
9–16	Data	Gives the data that is to be written to the specified register address
17	Stop bit	Indicates the end of the transfer (always 0)

For a link notification request, the length of the LREQ bit stream is 6 bits as shown in 表 11-10.

表 11-10. Link Notification Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	A 1100, 1101, or 1110 indicates this is a link notification request
5	Stop bit	Indicates the end of the transfer (always 0)

For fair or priority access, the LLC sends a bus request at least one clock after the PHY-LLC interface becomes idle. The PHY queues all bus requests and can queue one request of each type. If the LLC issues a different request of the same type, then the new request overwrites any nonserviced request of that type. On the receipt (CTL terminals are asserted to the receive state, 10b) of a packet, queued requests are not cleared by the PHY.

Copyright © 2023 Texas Instruments Incorporated

The cycle master node uses a cycle start request (Cyc_Start_Req) to send a cycle start message. After receiving or transmitting a cycle start message, the LLC can issue an isochronous bus request (IsoReq). The PHY clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC must issue an immediate bus request (Immed_Req) during the reception of the packet addressed to it. This is required in order to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the received packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and releases the interface immediately; the LLC must not use this grant to send another type of packet. After the interface is released the LLC can proceed with another request.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a PHY status transfer. A write or read register request can be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

11.2 Status Transfer

A status transfer is initiated by the PHY when status information is to be transferred to the LLC. Two types of status transfers can occur: bus status transfer and PHY status transfer. Bus status transfers send the following status information: bus reset indications, subaction and arbitration reset gap indications, cycle start indications, and PHY interface reset indications. PHY status transfers send the following information: PHY interrupt indications, unsolicited and solicited PHY register data, bus initialization indications, and PHY-link interface error indications. The PHY uses a different mechanism to send the bus status transfer and the PHY status transfer.

Bus status transfers use the CTL0−CTL1 and D0−D7 terminals to transfer status information. Bus status transfers can occur during idle periods on the PHY-link interface or during packet reception. When the status transfer occurs, a single PCLK cycle of status information is sent to the LLC. The information is sent such that each individual Dn terminal conveys a different bus status transfer event. During any bus status transfer, only one status bit is set. If the PHY-link interface is inactive, then the status information is not sent. When a bus reset on the serial bus occurs, the PHY sends a bus reset indication (via the CTLn and Dn terminals), cancels all packet transfer requests, sets asynchronous and isochronous phases to even, forwards self-ID packets to the link, and sends an unsolicited PHY register 0 status transfer (via the PINT terminal) to the LLC. In the case of a PHY interface reset operation, the PHY-link interface is reset on the following PCLK cycle.

表 11-11 shows the definition of the bits during the bus status transfer and 図 11-3 shows the timing.

表 11-11. Status Bits

STATUS BIT	DESCRIPTION
D0	Bus reset
D1	Arbitration reset gap—odd
D2	Arbitration reset gap—even
D3	Cycle start—odd
D4	Cycle start—even
D5	Subaction gap
D6	PHY interface reset
D7	Reserved

Copyright © 2023 Texas Instruments Incorporated

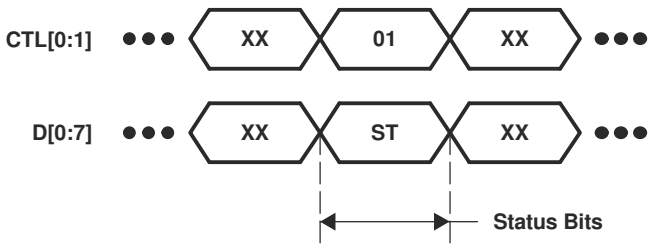
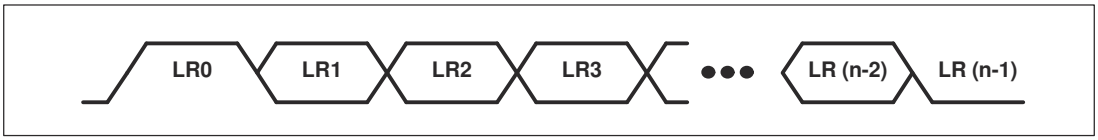


図 11-3. Bus Status Transfer Timing

PHY status transfers use the PINT terminal to send status information serially to the LLC as shown in 図 11-4. PHY status transfers (see 表 11-12) can occur at any time during normal operation. The PHY uses the PHY_INTERRUPT PHY status transfer when required to interrupt the LLC due to a configuration time-out, a cable-power failure, a port interrupt, or an arbitration time-out. When transferring PHY register contents, the PHY uses either the solicited or the unsolicited register read status transfer. The unsolicited register 0 contents are passed to the LLC only during initialization of the serial bus. After any PHY-link interface initialization, the PHY sends a PHY status transfer indicating whether or not a bus reset occurred during the inactive period of the PHY-link interface. If the PHY receives an illegal request from the LLC, then the PHY issues an INTERFACE_ERROR PHY status transfer.



Each cell represents one clock sample period, and n is the number of bits in the request stream.

図 11-4. PINT (PHY Interrupt) Stream

表 11-12. PHY Status Transfer Encoding

PI[1:3]	NAME	DESCRIPTION	NUMBER OF BITS
000	NOP	No status indication	5
001	PHY_INTERRUPT	Interrupt indication: configuration time-out, cable-power failure, port event interrupt, or arbitration state machine time-out	5
010	PHY_REGISTER_SOL	Solicited PHY register read	17
011	PHY_REGISTER_UNSOL	Unsolicited PHY register read	17
100	PH_RESTORE_NO_RESET	PHY-link interface initialized; no bus resets occurred.	5
101	PH_RESTORE_RESET	PHY-link interface initialized; a bus reset occurred.	5
110	INTERFACE_ERROR	PHY received illegal request.	5
111	Reserved	Reserved	Reserved

Most PHY status transfers are 5 bits long. The transfer consists of a start bit (always 1), followed by a request type (see 表 11-12), and lastly followed by a stop bit (always 0). The only exception is when the transfer of a register contents occurs. Solicited and unsolicited PHY register read transfers are 17 bits long and include the additional information of the register address and the data contents of the register (see 表 11-13).

表 11-13. Register Read (Solicited and Unsolicited) PHY Status Transfer Encoding

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	A 010 or a 011 indicates a solicited or unsolicited register contents transfer.
4–7	Address	Identifies the address of the PHY register whose contents are being transferred
8–15	Data	The contents of the register specified in bits 4 through 7
16	Stop bit	Indicates the end of the transfer (always 0)

Copyright © 2023 Texas Instruments Incorporated

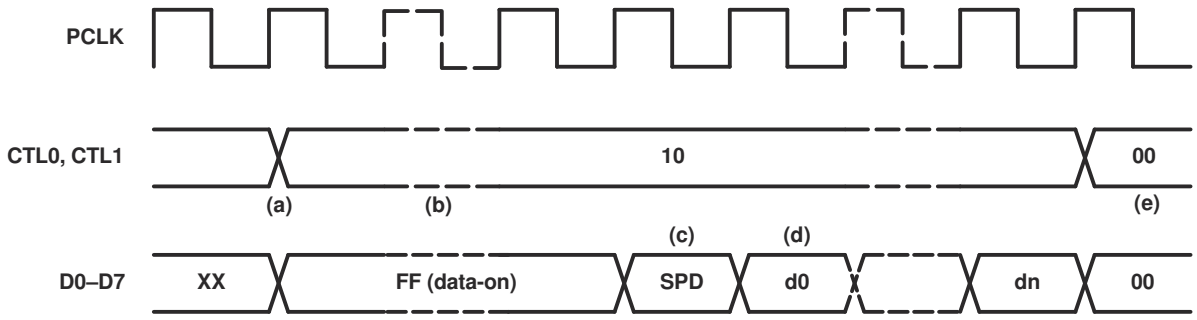
11.3 Receive

When the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL terminals and a logic 1 on each of the D terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in 表 11-14) on the D terminals, followed by packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

The PHY can optionally send status information to the LLC at anytime during the data-on indication. Only bus status transfer information can be sent during a data-on indication. The PHY holds the CTL terminals in the status state for 1 PCLK cycle and modifies the D terminals to the correct status state. Note that the status transfer during the data-on indication does not need to be preceded or followed by a data-on indication.

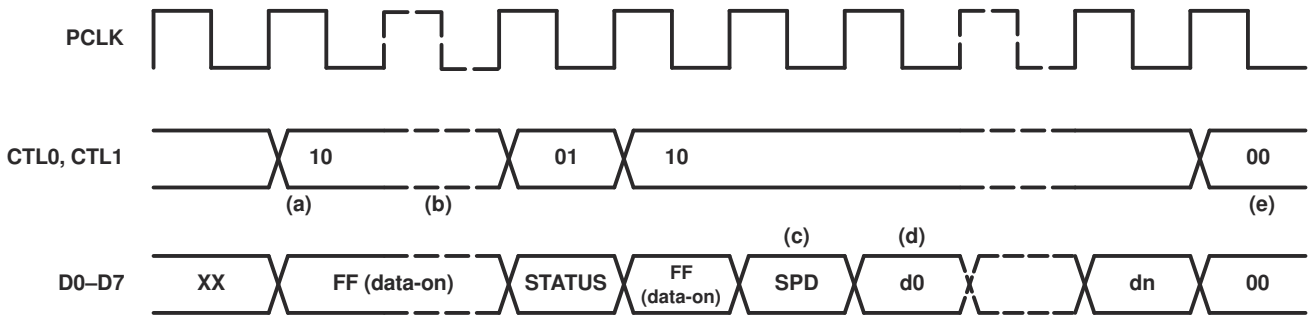
It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY asserts receive on the CTL terminals with the data-on indication (all 1s) on the D terminals, followed by idle on the CTL terminals, without any speed code or data being transferred. In all cases, in normal operation, the TSB41BA3F-EP sends at least one data-on indication before sending the speed code or terminating the receive operation.

The TSB41BA3F-EP also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet it transferred to the LLC just as any other received self-ID packet.



A. SPD = speed code, see 表 11-14. d0–dn = packet data.

図 11-5. Normal Packet Reception Timing



A. SPD = speed code, see 表 11-14. d0–dn = packet data. STATUS = status bits, see 表 11-11.

図 11-6. Normal Packet Reception Timing With Optional Bus Status Transfer

The sequence of events for a normal packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status

Copyright © 2023 Texas Instruments Incorporated

transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.

2. Data-on indication. The PHY can assert the data-on indication code on the D lines for one or more cycles preceding the speed code. The PHY can optionally send a bus status transfer during the data-on indication for one PCLK cycle. During this cycle, the PHY asserts status (01b) on the CTL lines while sending status information on the D lines.
3. Speed code. The PHY indicates the speed of the received packet by asserting a speed code on the D lines for one cycle immediately preceding packet data. The link decodes the speed code on the first receive cycle for which the D lines are not the data-on code. If the speed code is invalid or indicates a speed higher than that which the link is capable of handling, then the link must ignore the subsequent data.
4. Receive data. Following the data-on indication (if any) and the speed code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.
5. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

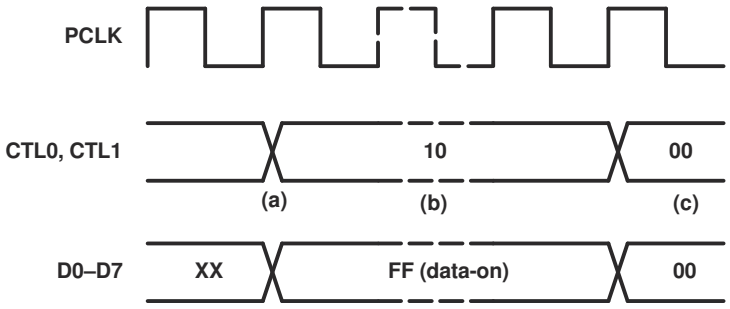


図 11-7. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.
2. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.
3. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

表 11-14. Receive Speed Codes and Format

D0–D7(1)	DATA RATE AND FORMAT
0000 0000	S100 legacy
0000 0001	S100 Beta
0000 0100	S200 legacy
0000 0101	S200 Beta
0000 1000	S400 legacy
0000 1001	S400 Beta
0000 1101	S800 Beta
1111 1111	Data-on indication
All others	Reserved

(1) Y = Output as 1 by PHY, ignored by LLC.
X = Output as 0 by PHY, ignored by LLC.

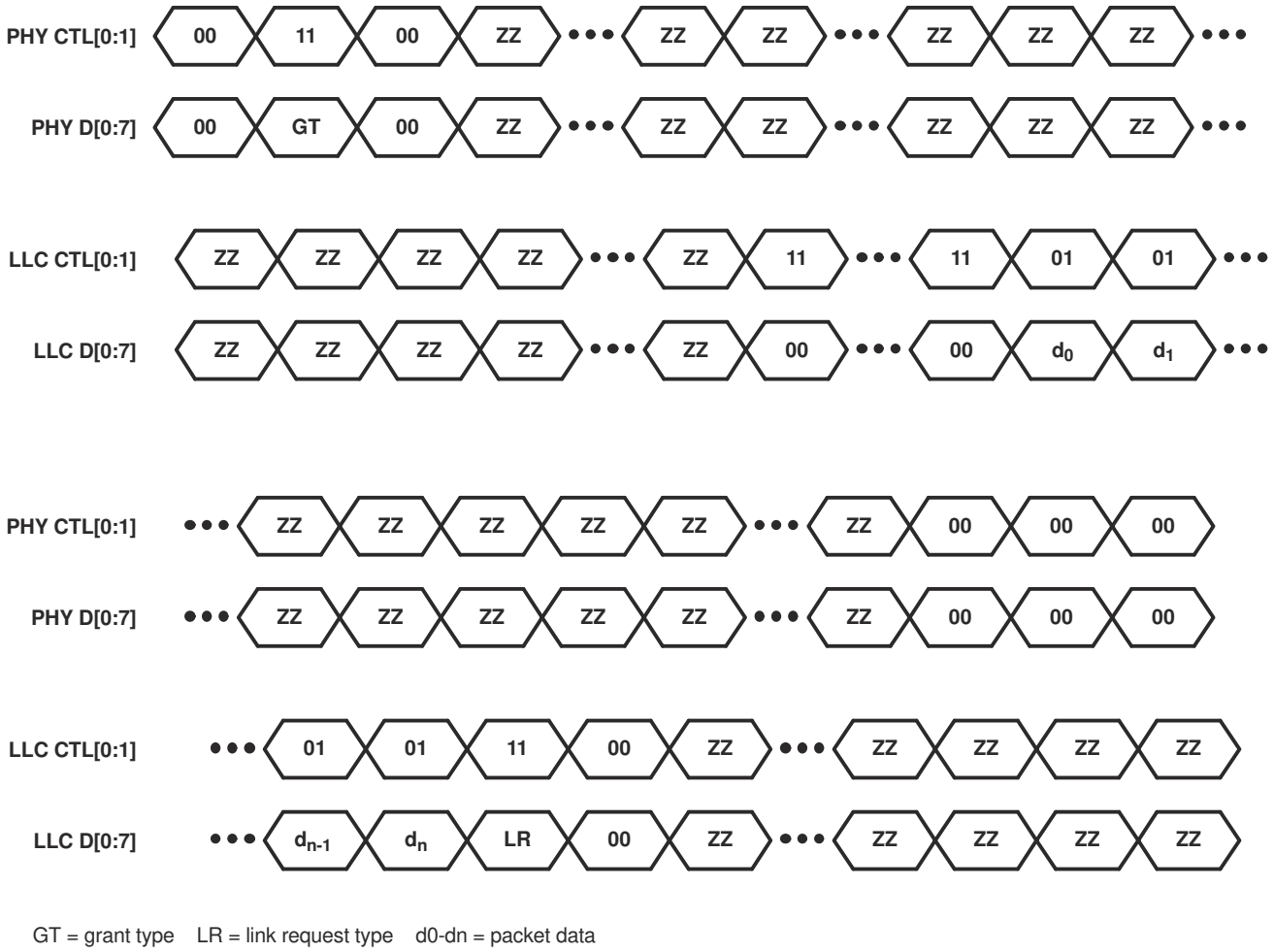
11.4 Transmit

When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, then the PHY-LLC interface bus is granted to the LLC by asserting

Copyright © 2023 Texas Instruments Incorporated

the grant state (11b) on the CTL terminals and the grant type on the D terminals for one PCLK cycle, followed by idle for one clock cycle. The LLC then takes control of the bus by asserting either idle (00b), hold (11b), or transmit (01b) on the CTL terminals. If the PHY does not detect a hold or transmit state within eight PCLK cycles, then the PHY takes control of the PHY-link interface. The hold state is used by the LLC to retain control of the bus while it prepares data for transmission. The LLC can assert hold for zero or more clock cycles (that is, the LLC need not assert hold before transmit). During the hold state, the LLC is expected to drive the D lines to 0. The PHY asserts data-prefix on the serial bus during this time.

When the LLC is ready to send data, the LLC asserts transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either hold or idle on the CTL terminals for one clock cycle. If the hold is asserted, then the hold is immediately followed by one clock cycle of idle. The link then releases the PHY-link interface by putting the CTL and D terminals in a high-impedance state. The PHY then regains control of the PHY-link interface.



GT = grant type LR = link request type d0-dn = packet data

図 11-8. Transmit Packet Timing With Optional Link Request

The hold state asserted at the end of packet transmission allows the LLC to make an additional link request for packet transmission and/or to notify the PHY that the packet marks the end of a subaction. The link requests allowed after packet transmission are listed in 表 11-15 (note that the link request types allowed during this period are a subset of all of the allowed types of link requests—see 表 11-4). The associated speed codes and packet format are listed in 表 11-15 and 表 11-16, respectively. If the LLC requests to send an additional packet, then the PHY does not necessarily have to grant the request. If the LLC is notifying the PHY of the end of a subaction, then the LLC sets D4 during the hold state at the end of packet transmission.

Copyright © 2023 Texas Instruments Incorporated

表 11-15. Link Request Type Encoding During Packet Transmission

D1–D3	Request Type
000	No request
001	Isoch_Req_Odd
010	Isoch_Req_Even
011	Current
100	Next_Even
101	Next_Odd
110	Cyc_Start_Req
111	Reserved

表 11-16. Link Request Speed Code Encoding During Packet Transmission

D5–D6	DATA RATE
00	S100
01	S200
10	S400
11	S800

表 11-17. Link Request Format Encoding During Packet Transmission

D0	FORMAT
0	Link does not request either Beta or legacy packet format for bus transmission.
1	Link requests Beta packet format for bus transmission.

表 11-18. Subaction End Notification Encoding During Packet Transmission

D4	DESCRIPTION
0	Transmitted packet does not represent end of a subaction.
1	Transmitted packet marks the end of a subaction.

The PHY indicates to the link during the GRANT cycle which type of grant is being issued. This indication includes the grant type as well as the grant speed. The link uses the bus grant for transmitting the granted packet type. The link transmits a granted packet type only if its request type exactly matches the granted speed and the granted format.

表 11-19. Format Type During Grant Cycle

D0 VALUE DURING GRANT CYCLE	FORMAT
0	Unspecified
1	Beta format

Copyright © 2023 Texas Instruments Incorporated

表 11-20. Grant Type Values During Grant Cycle

[D1–D3] VALUE DURING GRANT CYCLE	REQUEST TYPE
000	Reserved
001	Reserved
010	Isochronous grant
011	Reserved
100	Reserved
101	Asynchronous grant
110	Cycle start grant
111	Immediate grant

表 11-21. Speed Type Values During Grant Cycle

[D5–D6] VALUE DURING GRANT CYCLE	SPEED TYPE
00	S100
01	S200
10	S400
11	S800

Copyright © 2023 Texas Instruments Incorporated

12 Principles Of Operation (1394a-2000 Interface)

The TSB41BA3F-EP is designed to operate with an LLC such as the Texas Instruments TSB12LV21B, TSB12LV26, TSB12LV32, TSB42AA4, or TSB12LV01B when the BMODE terminal is tied low. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface. This interface is formally defined in IEEE 1394a-2000, Section 5A.

The interface to the LLC consists of the PCLK, CTL0–CTL1, D0–D7, LREQ, LPS, and S5_LKON terminals on the TSB41BA3F-EP, as shown in 図 12-1.

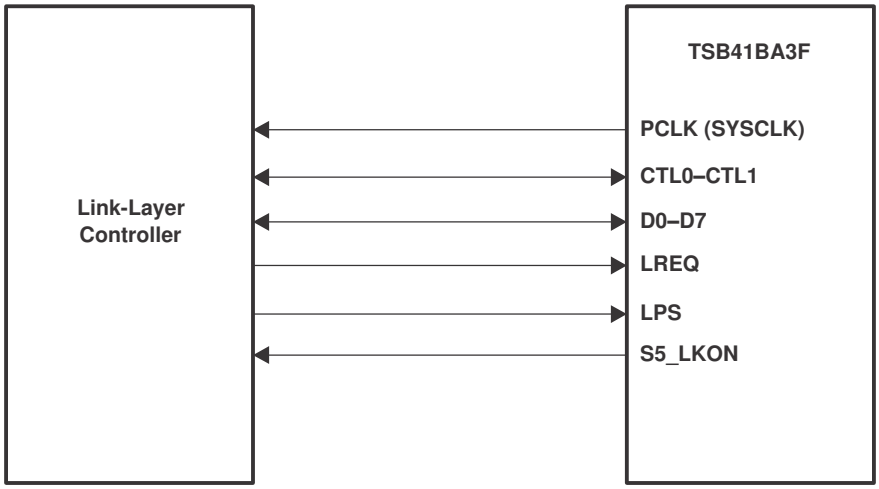


図 12-1. PHY-LLC Interface

The PCLK terminal provides a 49.152-MHz interface system clock. All control and data signals are synchronized to and sampled on the rising edge of PCLK. This terminal serves the same function as the SYSCLK terminal of 1394a-2000-compliant PHY devices.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB41BA3F-EP and LLC.

The D0–D7 terminals form a bidirectional data bus, which transfers status information, control information, or packet data between the devices. The TSB41BA3F-EP supports S100, S200, and S400 data transfers over the D0–D7 data bus. In S100 operation, only the D0 and D1 terminals are used; in S200 operation, only the D0–D3 terminals are used; and in S400 operation, all D0 – D7 terminals are used for data transfer. When the TSB41BA3F-EP is in control of the D0–D7 bus, unused Dn terminals are driven low during S100 and S200 operations. When the LLC is in control of the D0–D7 bus, unused Dn terminals are ignored by the TSB41BA3F-EP.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY in order to request access to the serial bus for packet transmission, read or write PHY registers, or control arbitration acceleration.

The LPS and S5_LKON terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC and can be used to reset the PHY-LLC interface or to disable PCLK. The S5_LKON terminal sends a wake-up notification to the LLC or external circuitry and indicates an interrupt to the LLC when either LPS is inactive or the PHY register L bit is 0.

The TSB41BA3F-EP normally controls the CTL0–CTL1 and D0–D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY.

Four operations can occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a service request to read or write a PHY register, to request the PHY to gain control of the serial bus in order to transmit a packet, or to control arbitration acceleration.

Copyright © 2023 Texas Instruments Incorporated

The PHY can initiate a status transfer either autonomously or in response to a register read request from the LLC.

The PHY initiates a receive operation whenever a packet is received from the serial bus.

The PHY initiates a transmit operation after winning control of the serial bus following a bus request by the LLC. The transmit operation is initiated when the PHY grants control of the interface to the LLC.

表 12-1 and 表 12-2 show the encoding of the CTL0–CTL1 bus.

表 12-1. CTL Encoding When PHY Has Control of the Bus

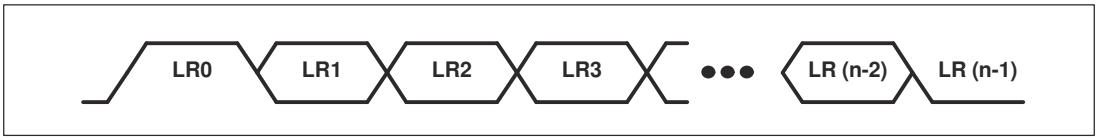
CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC.
1	0	Receive	An incoming packet is being sent from the PHY to the LLC.
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet.

表 12-2. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission or indicating that another packet is to be transmitted (concatenated) without arbitrating.
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY.
1	1	Reserved	None

12.1 LLC Service Request

To request access to the bus, to read or write a PHY register, or to control arbitration acceleration, the LLC sends a serial bit stream on the LREQ terminal as shown in 図 12-2.



Each cell represents one clock sample period, and n is the number of bits in the request stream.

図 12-2. LREQ Request Stream

The length of the stream varies depending on the type of request as shown in 表 12-3.

表 12-3. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	7 or 8
Read register request	9
Write register request	17
Acceleration control request	6

Regardless of the type of request, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. The second through fourth bits of the request stream indicate the type of the request. In the following descriptions, bit 0 is the most significant and is transmitted first in the request bit stream. The LREQ terminal is normally low.

Copyright © 2023 Texas Instruments Incorporated

表 12-4 shows the encoding for the request type.

表 12-4. Request Type Encoding

LR1–LR3	NAME	DESCRIPTION
000	ImmReq	Immediate bus request. On detection of idle, the PHY takes control of the bus immediately without arbitration.
001	IsoReq	Isochronous bus request. On detection of idle, the PHY arbitrates for the bus without waiting for a subaction gap.
010	PriReq	Priority bus request. The PHY arbitrates for the bus after a subaction gap, ignores the fair protocol.
011	FairReq	Fair bus request. The PHY arbitrates for the bus after a subaction gap, follows the fair protocol.
100	RdReg	The PHY returns the specified register contents through a status transfer.
101	WrReg	Write to the specified register
110	AccelCtl	Enable or disable asynchronous arbitration acceleration
111	Reserved	Reserved

For a bus request, the length of the LREQ bit stream is 7 or 8 bits as shown in 表 12-5.

表 12-5. Bus Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	Indicates the type of bus request. See 表 12-4.
4–6	Request speed	Indicates the speed at which the PHY sends the data for this request. See 表 12-6 for the encoding of this field.
7	Stop bit	Indicates the end of the transfer (always 0). If bit 6 is 0, then this bit can be omitted.

表 12-6 shows the 3-bit request speed field used in bus requests.

表 12-6. Bus Request Speed Encoding

LR4–LR6	DATA RATE
000	S100
010	S200
100	S400
All Others	Invalid

注

The TSB41BA3F-EP accepts a bus request with an invalid speed code and processes the bus request normally. However, during packet transmission for such a request, the TSB41BA3F-EP ignores any data presented by the LLC and transmits a null packet.

For a read register request, the length of the LREQ bit stream is 9 bits as shown in 表 12-7.

表 12-7. Read Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	A 100 indicates this is a read register request.
4–7	Address	Identifies the address of the PHY register to be read
8	Stop bit	Indicates the end of the transfer (always 0)

For a write register request, the length of the LREQ bit stream is 17 bits as shown in 表 12-8.

Copyright © 2023 Texas Instruments Incorporated

表 12-8. Write Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	A 101 indicates this is a write register request.
4–7	Address	Identifies the address of the PHY register to be written to
8–15	Data	Gives the data that is to be written to the specified register address
16	Stop bit	Indicates the end of the transfer (always 0)

For an acceleration control request, the length of the LREQ data stream is 6 bits as shown in 表 12-9.

表 12-9. Acceleration Control Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	A 110 indicates this is an acceleration control request.
4	Control	Asynchronous period arbitration acceleration is enabled if 1 and disabled if 0
5	Stop bIt	Indicates the end of the transfer (always 0)

For fair or priority access, the LLC sends the bus request (FairReq or PriReq) at least one clock after the PHY-LLC interface becomes idle. If the CTL terminals are asserted to the receive state (10b) by the PHY, then any pending fair or priority request is lost (cleared). Additionally, the PHY ignores any fair or priority requests if the receive state is asserted while the LLC is sending the request. The LLC can then reissue the request one clock after the next interface idle.

The cycle master node uses a priority bus request (PriReq) to send a cycle start message. After receiving or transmitting a cycle start message, the LLC can issue an isochronous bus request (IsoReq). The PHY clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC must issue an immediate bus request (ImmReq) during the reception of the packet addressed to it. This is required in order to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the receive packet ends, the PHY immediately grants control of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC does not transmit an acknowledge, but instead cancels the transmit operation and releases the interface immediately; the LLC must not use this grant to send another type of packet. After the interface is released, the LLC can proceed with another request.

The LLC can make only one bus request at a time. Once the LLC issues any request for bus access (ImmReq, IsoReq, FairReq, or PriReq), it cannot issue another bus request until the PHY indicates that the bus request was lost (bus arbitration lost and another packet received), or won (bus arbitration won and the LLC granted control). The PHY ignores new bus requests while a previous bus request is pending. All bus requests are cleared on a bus reset.

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the LLC at the next opportunity through a status transfer. If a received packet interrupts the status transfer, then the PHY continues to attempt the transfer of the requested register until it is successful. A write or read register request can be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the LLC. A bus reset does not clear a pending read register request.

The TSB41BA3F-EP includes several arbitration acceleration enhancements, which allow the PHY to improve bus performance and throughput by reducing the number and length of interpacket gaps. These enhancements include autonomous (fly-by) isochronous packet concatenation, autonomous fair and priority packet concatenation onto acknowledge packets, and accelerated fair and priority request arbitration following acknowledge packets. The enhancements are enabled when the EAA bit in PHY register 5 is set.

Copyright © 2023 Texas Instruments Incorporated

The arbitration acceleration enhancements can interfere with the ability of the cycle master node to transmit the cycle start message under certain circumstances. The acceleration control request is therefore provided to allow the LLC temporarily to enable or disable the arbitration acceleration enhancements of the TSB41BA3F-EP during the asynchronous period. The LLC typically disables the enhancements when its internal cycle counter rolls over, indicating that a cycle-start message is imminent, and then re-enables the enhancements when it receives a cycle-start message. The acceleration control request can be made at any time and is immediately serviced by the PHY. Additionally, a bus reset or isochronous bus request causes the enhancements to be re-enabled, if the EAA bit is set.

12.2 Status Transfer

A status transfer is initiated by the PHY when there is status information to be transferred to the LLC. The PHY waits until the interface is idle before starting the transfer. The transfer is initiated by the PHY asserting status(01b) on the CTL terminals, along with the first two bits of status information on the D[0:1] terminals. The PHY maintains CTL = Status for the duration of the status transfer. The PHY might prematurely end a status transfer by asserting something other than *status* on the CTL terminals. This occurs if a packet is received before the status transfer completes. The PHY continues to attempt to complete the transfer until all status information has been successfully transmitted. At least one idle cycle occurs between consecutive status transfers.

The PHY normally sends just the first 4 bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The PHY sends an entire 16-bit status packet to the LLC after a read register request, or when the PHY has pertinent information to send to the LLC or transaction layers. The only defined condition where the PHY automatically sends a register to the LLC is after self-ID, where the PHY sends the physical-ID register that contains the new node address. All status transfers are either 4 or 16 bits unless interrupted by a received packet. The status flags are considered to have been successfully transmitted to the LLC immediately on being sent, even if a received packet subsequently interrupts the status transfer. Register contents are considered to have been successfully transmitted only when all 8 bits of the register have been sent. A status transfer is retried after being interrupted only if any status flags remain to be sent, or if a register transfer has not yet completed.

表 12-10 shows the definition of the bits in the status transfer, and 図 12-3 shows the timing.

表 12-10. Status Bits

BIT(s)	NAME	DESCRIPTION
0	Arbitration reset gap	Indicates that the PHY has detected that the bus has been idle for an arbitration reset gap time (as defined in the IEEE 1394a-2000 standard). This bit is used by the LLC in the busy/retry state machine.
1	Subaction gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time (as defined in the IEEE 1394a-2000 standard). This bit is used by the LLC to detect the completion of an isochronous cycle.
2	Bus reset	Indicates that the PHY has entered the bus reset state
3	Interrupt	Indicates that a PHY interrupt event has occurred. An interrupt event might be a configuration time-out, a cable-power voltage falling too low, a state time-out, or a port status change.
4–7	Address	This field holds the address of the PHY register whose contents are being transferred to the LLC.
8–15	Data	This field holds the register contents.

Copyright © 2023 Texas Instruments Incorporated

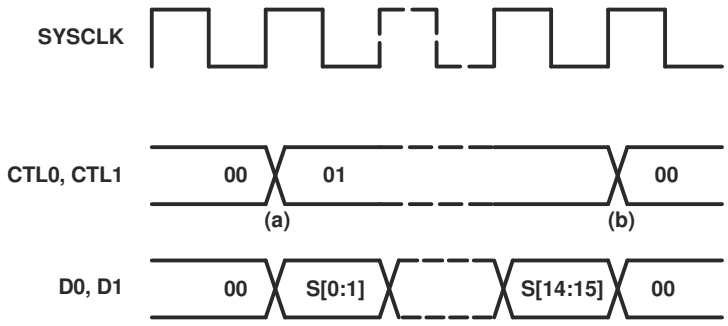


図 12-3. Status Transfer Timing

The sequence of events for a status transfer is as follows:

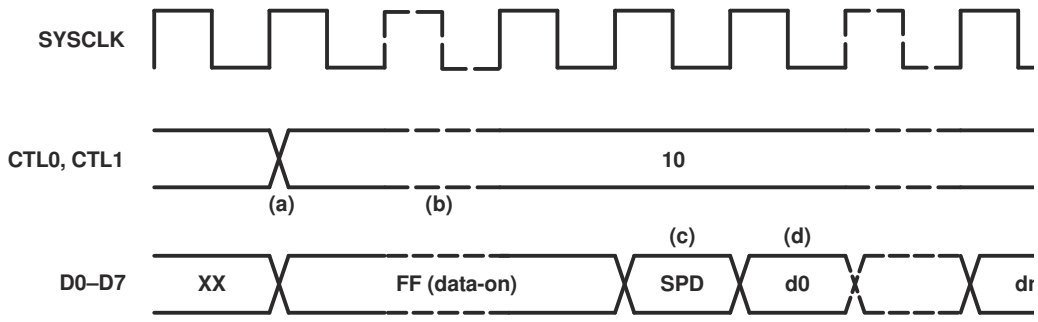
1. Status transfer initiated. The PHY indicates a status transfer by asserting status on the CTL lines along with the status data on the D0 and D1 lines (only 2 bits of status are transferred per cycle). Normally (unless interrupted by a receive operation), a status transfer is either 2 or 8 cycles long. A 2-cycle (4-bit) transfer occurs when only status information is to be sent. An 8-cycle (16-bit) transfer occurs when register data is to be sent in addition to any status information.
2. Status transfer terminated. The PHY normally terminates a status transfer by asserting idle on the CTL lines. The PHY can also interrupt a status transfer at any cycle by asserting receive on the CTL lines to begin a receive operation. The PHY asserts at least one idle cycle between consecutive status transfers.

12.3 Receive

Whenever the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL terminals and a logic 1 on each of the D bus terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in 表 12-11) on the D terminals, followed by packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting idle on the CTL terminals. All received packets are transferred to the LLC. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY, or whenever the LLC immediately releases the bus without transmitting any data. In this case, the PHY asserts receive on the CTL terminals with the data-on indication (all 1s) on the D bus terminals, followed by Idle on the CTL terminals, without any speed code or data being transferred. In all cases, in normal operation, the TSB41BA3F-EP sends at least one data-on indication before sending the speed code or terminating the receive operation.

The TSB41BA3F-EP also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet is transferred to the LLC just as any other received self-ID packet.



A. SPD = Speed code, see 表 12-11. d0–dn = Packet data

図 12-4. Normal Packet Reception Timing

Copyright © 2023 Texas Instruments Incorporated

The sequence of events for a normal packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.
2. Data-on indication. The PHY can assert the data-on indication code on the D lines for one or more cycles preceding the speed code.
3. Speed code. The PHY indicates the speed of the received packet by asserting a speed code on the D lines for one cycle immediately preceding packet data. The link decodes the speed code on the first receive cycle for which the D lines are not the data-on code. If the speed code is invalid or indicates a speed higher that which the link is capable of handling, then the link must ignore the subsequent data.
4. Receive data. Following the data-on indication (if any) and the speed code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.
5. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

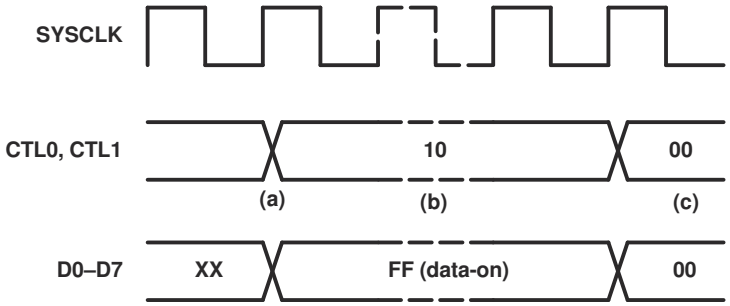


図 12-5. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation can interrupt a status transfer operation that is in progress so that the CTL lines can change from status to receive without an intervening idle.
2. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.
3. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY asserts at least one idle cycle following a receive operation.

表 12-11. Receive Speed Codes

D0–D7(1)	DATA RATE
00XX XXXX	S100
0100 XXXX	S200
0101 0000	S400
11YY YYYY	data-on indication

(1) X = Output as 0 by PHY, ignored by LLC.
Y = Output as 1 by PHY, ignored by LLC.

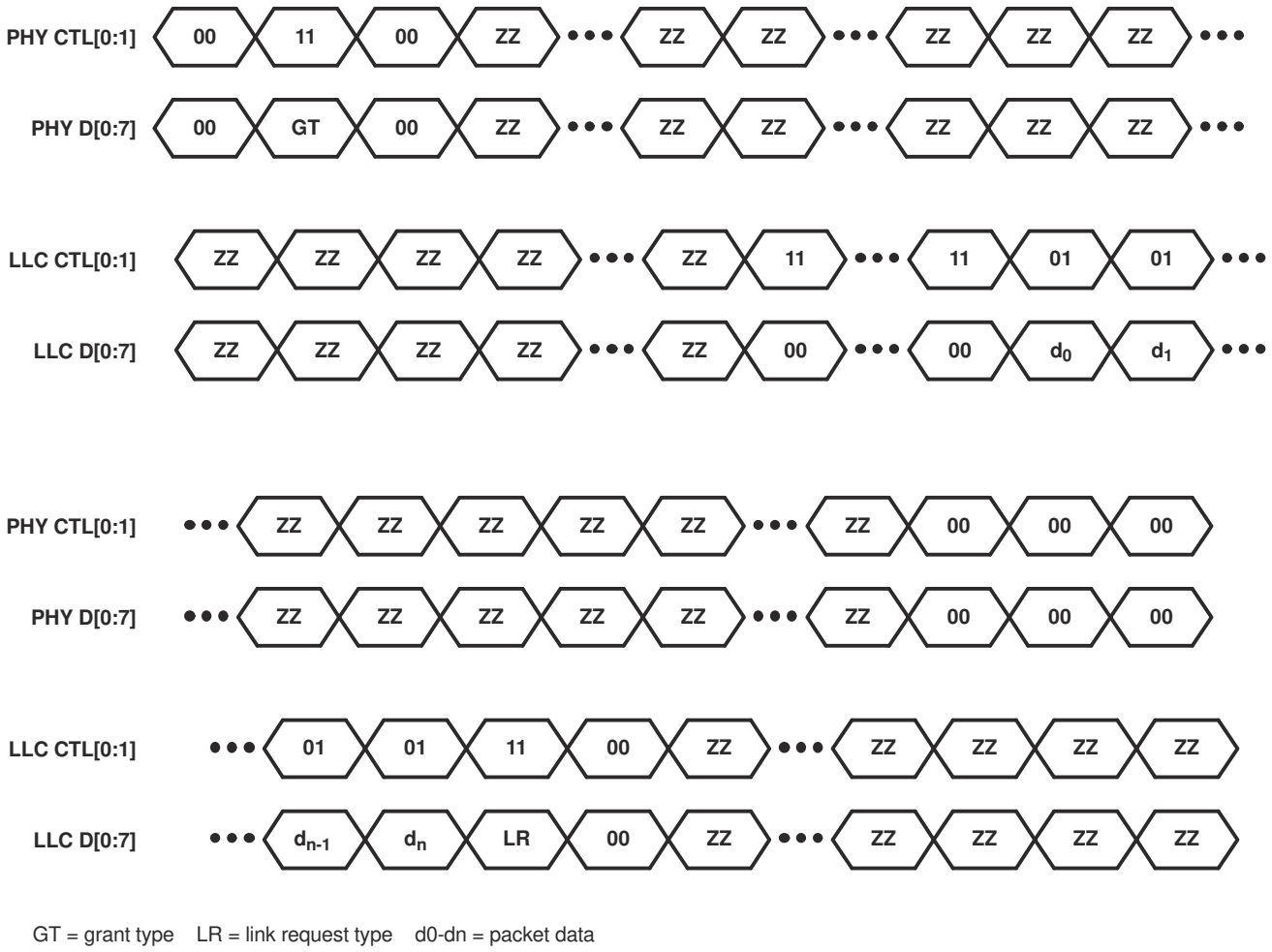
12.4 Transmit

When the LLC issues a bus request through the LREQ terminal, the PHY arbitrates to gain control of the bus. If the PHY wins arbitration for the serial bus, then the PHY-LLC interface bus is granted to the LLC by asserting the grant state (11b) on the CTL terminals and the grant type on the D terminals for one PCLK cycle, followed by idle for one clock cycle. The LLC then takes control of the bus by asserting either idle (00b), hold (11b), or transmit (01b) on the CTL terminals. If the PHY does not detect a hold or transmit state within eight PCLK cycles, then the PHY takes control of the PHY-link interface. The hold state is used by the LLC to retain control

Copyright © 2023 Texas Instruments Incorporated

of the bus while it prepares data for transmission. The LLC can assert hold for zero or more clock cycles (that is, the LLC need not assert hold before transmit). During the hold state, the LLC is expected to drive the D lines to 0. The PHY asserts data-prefix on the serial bus during this time.

When the LLC is ready to send data, the LLC asserts transmit on the CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The LLC then asserts either hold or idle on the CTL terminals for one clock cycle. If the hold is asserted, then the hold is immediately followed by one clock cycle of idle. The link then releases the PHY-link interface by putting the CTL and D terminals in a high-impedance state. The PHY then regains control of the PHY-link interface.



GT = grant type LR = link request type d0-dn = packet data

図 12-6. Transmit Packet Timing With Optional Link Request

The hold state asserted at the end of packet transmission allows the LLC to make an additional link request for packet transmission and/or to notify the PHY that the packet marks the end of a subaction. The link requests allowed after packet transmission are listed in 表 12-12 (note that the link request types allowed during this period are a subset of all of the allowed types of link requests—see 表 11-4). The associated speed codes and packet format are listed in 表 12-12 and 表 12-13, respectively. If the LLC requests to send an additional packet, then the PHY does not necessarily have to grant the request. If the LLC is notifying the PHY of the end of a subaction, then the LLC sets D4 during the hold state at the end of packet transmission.

Copyright © 2023 Texas Instruments Incorporated

表 12-12. Link Request Type Encoding During Packet Transmission

D1–D3	Request Type
000	No request
001	Isoch_Req_Odd
010	Isoch_Req_Even
011	Current
100	Next_Even
101	Next_Odd
110	Cyc_Start_Req
111	Reserved

表 12-13. Link Request Speed Code Encoding During Packet Transmission

D5–D6	DATA RATE
00	S100
01	S200
10	S400
11	S800

表 12-14. Link Request Format Encoding During Packet Transmission

D0	FORMAT
0	Link does not request either Beta or legacy packet format for bus transmission.
1	Link requests Beta packet format for bus transmission.

表 12-15. Subaction End Notification Encoding During Packet Transmission

D4	DESCRIPTION
0	Transmitted packet does not represent end of a subaction.
1	Transmitted packet marks the end of a subaction.

The PHY indicates to the link during the GRANT cycle which type of grant is being issued. This indication includes the grant type as well as the grant speed. The link uses the bus grant for transmitting the granted packet type. The link transmits a granted packet type only if its request type exactly matches the granted speed and the granted format.

表 12-16. Format Type During Grant Cycle

D0 VALUE DURING GRANT CYCLE	FORMAT
0	Unspecified
1	Beta format

Copyright © 2023 Texas Instruments Incorporated

表 12-17. Grant Type Values During Grant Cycle

[D1–D3] VALUE DURING GRANT CYCLE	REQUEST TYPE
000	Reserved
001	Reserved
010	Isochronous grant
011	Reserved
100	Reserved
101	Asynchronous grant
110	Cycle start grant
111	Immediate grant

表 12-18. Speed Type Values During Grant Cycle

[D5–D6] VALUE DURING GRANT CYCLE	SPEED TYPE
00	S100
01	S200
10	S400
11	S800

12.5 Interface Reset and Disable

The LLC controls the state of the PHY-LLC interface using the LPS signal. The interface can be placed into a reset state, a disabled state, or be made to initialize and then return to normal operation. When the interface is not operational (whether reset, disabled, or in the process of initialization), the PHY cancels any outstanding bus request or register read request, and ignores any requests made via the LREQ line. Additionally, any status information generated by the PHY is not queued and does not cause a status transfer on restoration of the interface to normal operation.

The LPS signal can be either a level signal or a pulsed signal, depending on whether the PHY-LLC interface is a direct connection or is made across an isolation barrier. When an isolation barrier exists between the PHY and LLC, the LPS signal must be pulsed. In a direct connection, the LPS signal can be either a pulsed or a level signal. Timing parameters for the LPS signal are given in 表 12-19.

Copyright © 2023 Texas Instruments Incorporated

表 12-19. LPS Timing Parameters

SYMBOL	DESCRIPTION		MIN	MAX	UNIT
t_{LPSL}	LPS low time (when pulsed)(2)		0.09	2.6	µs
t_{LPSH}	LPS high time (when pulsed)(2)		0.021	2.6	µs
t_{LPS_DUTY}	LPS duty cycle (when pulsed)(3)		20%	60%	
t_{LPS_RESET}	Time for PHY to recognize LPS deasserted and reset the interface		2.6	2.68	µs
$t_{LPS_DISABLE}$	Time for PHY to recognize LPS deasserted and disable the interface		26.03	26.11	µs
$t_{RESTORE}$	Time to permit optional isolation circuits to restore during an interface reset		15	23(1)	µs
$t_{CLK_ACTIVATE}$	Time for PCLK to be activated from reassertion of LPS	PHY not in low-power state		60	ns
		PHY in low-power state	5.3	7.3	ms

(1) The maximum value for $t_{RESTORE}$ does not apply when the PHY-LLC interface is disabled, in which case an indefinite time can elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface, it is necessary that the LLC ensure that LPS is deasserted for less than $t_{LPS_DISABLE}$.
(2) The specified t_{LPSL} and t_{LPSH} times are worst-case values appropriate for operation with the TSB41BA3F-EP. These values are broader than those specified for the same parameters in the 1394a-2000 Supplement (that is, an implementation of LPS that meets the requirements of 1394a-2000 operates correctly with the TSB41BA3F-EP).
(3) A pulsed LPS signal must have a duty cycle (ratio of t_{LPSH} to cycle period) in the specified range to ensure proper operation when using an isolation barrier on the LPS signal (for example, as shown in 図 13-7).

The LLC requests that the interface be reset by deasserting the LPS signal and terminating all bus and request activity. When the PHY observes that LPS has been deasserted for t_{LPS_RESET}, it resets the interface. When the interface is in the reset state, the PHY sets its CTL and D outputs in the logic 0 state and ignores any activity on the LREQ signal. 図 12-7 shows the timing for interface reset.

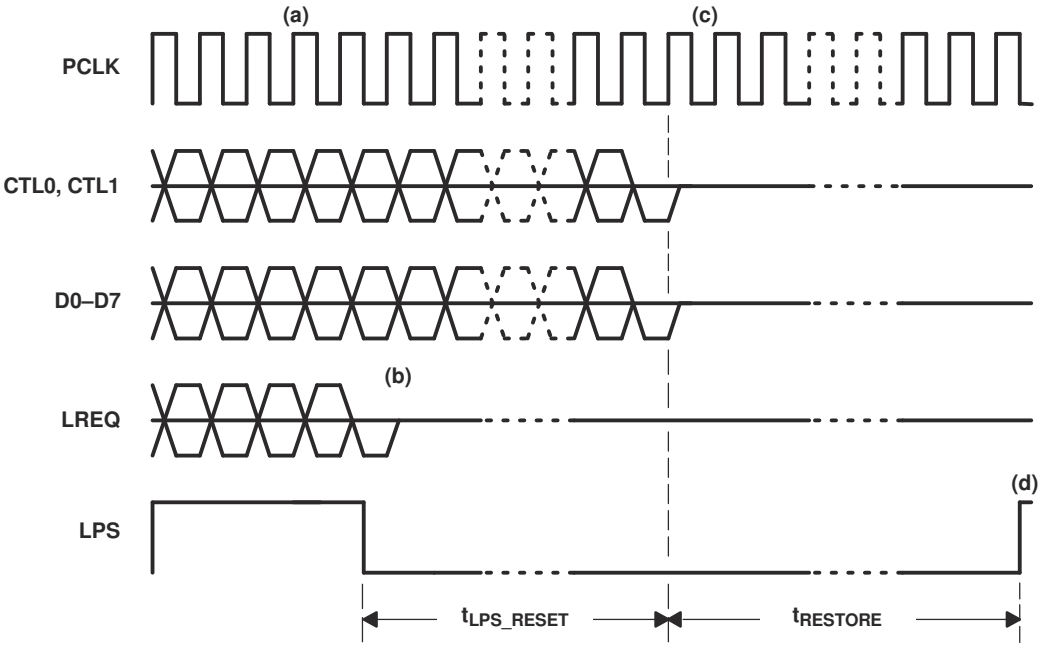


図 12-7. Interface Reset

The sequence of events for resetting the PHY-LLC interface is as follows:

1. Normal operation. Interface is operating normally, with LPS asserted, PCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line. In 図 12-7, the LPS signal is shown as a nonpulsed level signal. However, it is permissible to use a pulsed signal for LPS in a direct connection between the PHY and LLC; a pulsed signal is required when using an isolation barrier.
2. LPS deasserted. The LLC deasserts the LPS signal and, within 1 µs, terminates any request or interface bus activity, places its CTL and D outputs into the high-impedance state, and drives its LREQ output low.

Copyright © 2023 Texas Instruments Incorporated

3. Interface reset. After t_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.
4. Interface restored. After the minimum $t_{RESTORE}$ time, the LLC can again assert LPS active. When LPS is asserted, the interface is initialized as described in the following paragraph.

If the LLC continues to keep the LPS signal deasserted, it then requests that the interface be disabled. The PHY disables the interface when it observes that LPS has been deasserted for $t_{LPS_DISABLE}$. When the interface is disabled, the PHY sets its CTL and D outputs as previously stated for interface reset, but also stops PCLK activity. The interface is also placed into the disabled condition on a hardware reset of the PHY. 図 12-8 shows the timing for the interface disable.

When the interface is disabled, the PHY enters a low-power state if none of its ports are active.

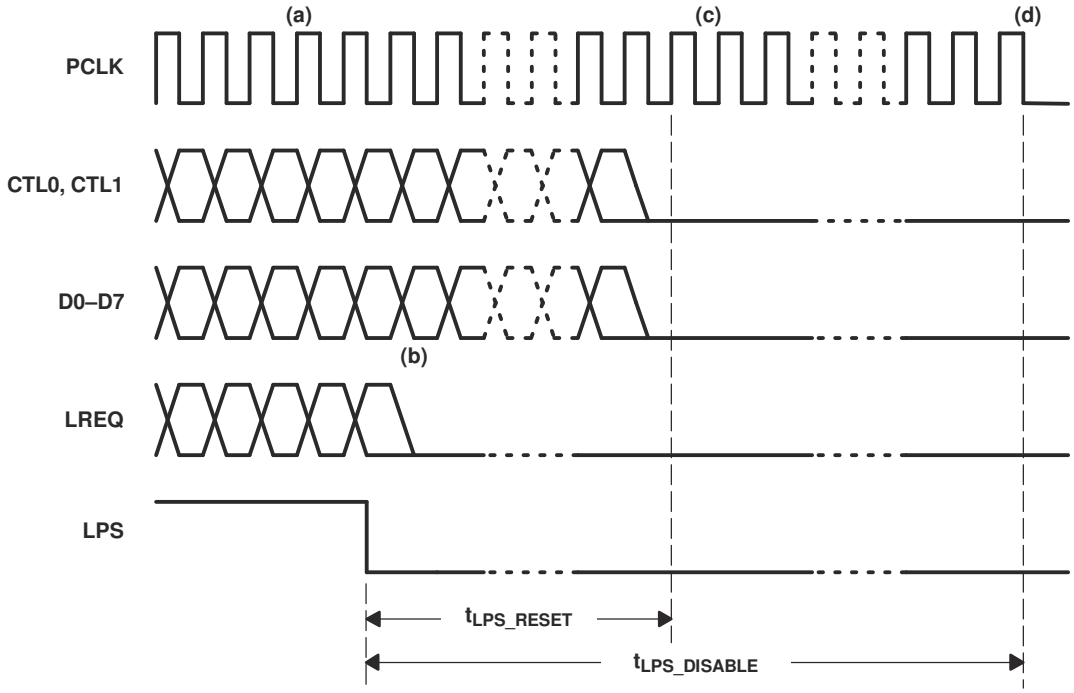


図 12-8. Interface Disable

The sequence of events for disabling the PHY-LLC is as follows:

1. Normal operation. Interface is operating normally, with LPS active, PCLK active, status and packet data reception and transmission via the CTL and D lines, and request activity via the LREQ line.
2. LPS deasserted. The LLC deasserts the LPS signal and, within 1 µs, terminates any request or interface bus activity, places its CTL and D outputs into a high-impedance state, and drives its LREQ output low.
3. Interface reset. After t_{LPS_RESET} time, the PHY determines that LPS is inactive, terminates any interface bus activity, and drives its CTL and D outputs low. The PHY-LLC interface is now in the reset state.
4. Interface disabled. If the LPS signal remains inactive for $t_{LPS_DISABLE}$ time, then the PHY terminates PCLK activity by driving the PCLK output low. The PHY-LLC interface is now in the disabled state.

Copyright © 2023 Texas Instruments Incorporated

After the interface has been reset, or reset and then disabled, the interface is initialized and restored to normal operation when LPS is reasserted by the LLC. 図 12-9 shows the timing for interface initialization.

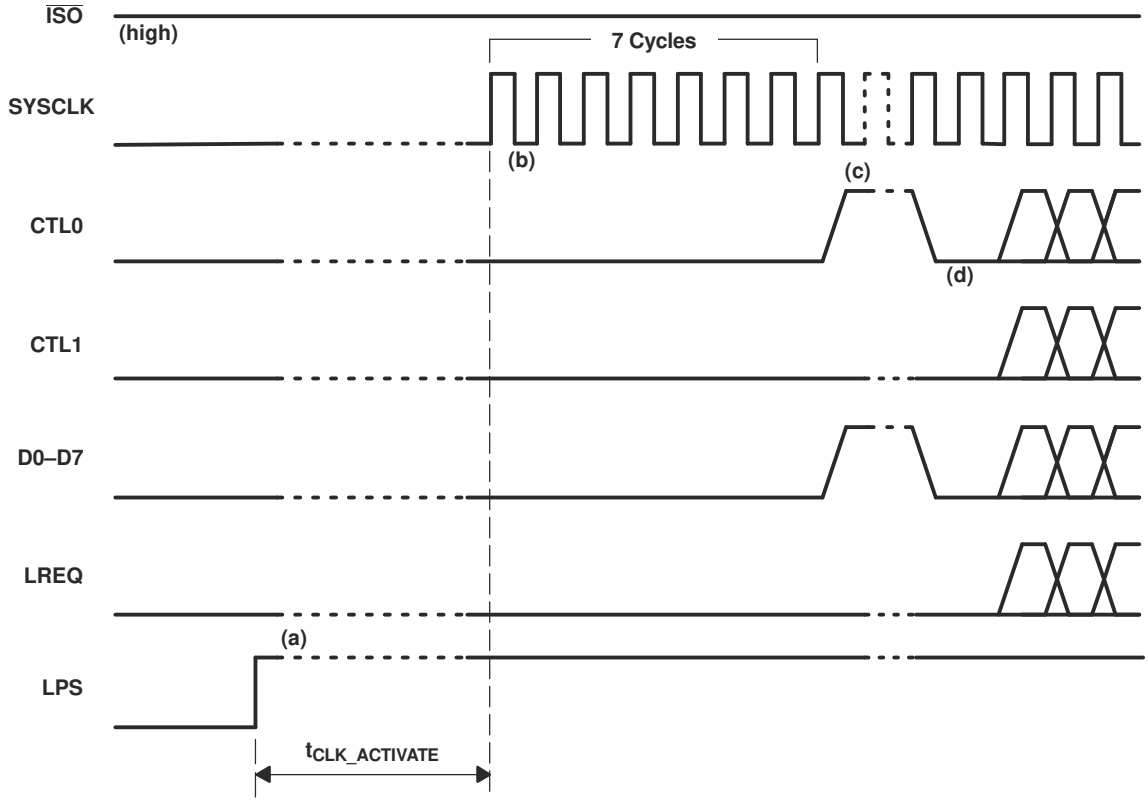


図 12-9. Interface Initialization

The sequence of events for initialization of the PHY-LLC is as follows:

1. LPS reasserted. After the interface has been in the reset or disabled state for at least the minimum $t_{RESTORE}$ time, the LLC causes the interface to be initialized and restored to normal operation by reasserting the LPS signal. (In 図 12-9, the interface is shown in the disabled state with PCLK inactive. However, the interface initialization sequence described here is also executed if the interface is merely reset but not yet disabled.)
2. PCLK activated. If the interface is disabled, then the PHY reactivates its PCLK output when it detects that LPS has been reasserted. If the PHY has entered a low-power state, then it takes between 5.3 ms and 7.3 ms for PCLK to be restored; if the PHY is not in a low-power state, then the PCLK is restored within 60 ns. The PCLK output is a 50% duty cycle square wave with a frequency of 49.152 MHz ±100 ppm (period of 20.345 ns). During the first 7 cycles of PCLK, the PHY continues to drive the CTL and D terminals low. The LLC is also required to drive its CTL and D outputs low for one of the first 6 cycles of PCLK but otherwise to place its CTL and D outputs in the high-impedance state. The LLC continues to drive its LREQ output low during this time.
3. Receive indicated. On the eighth PCLK cycle following reassertion of LPS, the PHY asserts the receive state on the CTL lines and the data-on indication (all 1s) on the D lines for one or more cycles.
4. Initialization complete. The PHY asserts the idle state on the CTL lines and logic 0 on the D lines. This indicates that the PHY-LLC interface initialization is complete and normal operation can commence. The PHY now accepts requests from the LLC via the LREQ line.

Copyright © 2023 Texas Instruments Incorporated

13 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1 Known exceptions to functional specification (errata).

13.1.1 Errata # 1:Restore from Leaf Node (Nephew)

13.1.1.1 Detailed Description

When a TSB41BA3F (and previous versions) port is a Nephew (in Standby) and the attached link layer controller issues a bus request to send a packet or arbitrated short bus reset, it causes a MAX_ARB_STATE_TIMEOUT which results in a bus reset. In the Nephew, the bus reset results in an incorrect two node self-ID map in the Nephew. The Nephew proxy/creates an extra self-ID packet. The connection between the Nephew and Uncle is Restored and the correct PHY Configuration packets are transferred from the Uncle to the Nephew.

注

When the Uncle restores the connection the Restore process is correct.

13.1.1.2 Background

IEEE-1394 Standard specifies, when a node’s port is put into Standby it becomes the Nephew and the attached PHY port is the Uncle. No bus reset is generated by the Standby action and high-level software in the Nephew should see the same topology both before and after the Standby. The Standard also defines, the Nephew shall restore the connection to the Uncle when a Remote Command packet with an extended command of Restore is received by the Nephew or the Nephew’s node requests the 1394 bus to send a packet. No bus reset shall be generated by the bus request or restore action. After the restore, it is expected high-level software may request a bus reset.

13.1.1.3 Workaround Proposal

The standard’s defined Restore process can be done without a bus reset. When the TSB41BA3 is the Nephew and it initiates a Restore with a bus request, a bus reset is required to update the Self-ID list with current topology information.

13.1.1.4 Corrective Action

None for current device.

13.2 Application Information

Obtain reference schematics, reference layouts, debug documents, and software recommendations for the TSB41BA3F-EP from the Texas Instruments website or your local Texas Instruments representative.

13.2.1 Interoperability with earlier revisions of TSB41BA3

In a Beta Only topology, all nodes implement both Beta mode PHY and Link Layers, with more than one TSB41BA3F and one or more TSB41BA3, TSB41BA3A, TSB41BA3B PHYs acting as repeaters, not a leaf, could cause a time out error followed by a bus reset. Note: If one or more non-Beta mode nodes (Alpha PHY or Beta PHY with Alpha Link Layer) are present in the bus topology, this issue will not occur

Work Around: When implementing a Beta Only node, Beta mode PHY and Link Layer, only use the TSB41BA3D or TSB41BA3F PHYs.

Copyright © 2023 Texas Instruments Incorporated

13.2.2 Internal Register Configuration

The TSB41BA3F-EP has 16 accessible internal registers. The configuration of the registers at addresses 0h through 7h (the base registers) is fixed, whereas the configuration of the registers at addresses 8h through Fh (the paged registers) depends on which of eight pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h. Note that while this register set is compatible with 1394a-2000 register sets, some fields have been redefined, and this register set contains additional fields.

表 13-1 shows the configuration of the base registers, and 表 13-2 gives the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

表 13-1. Base Register Configuration

Address	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Num_Ports (0011b)				
0011	PHY_Speed (111b)			SREN	Delay (1011b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	WDIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Max Legacy SPD			BLINK	Bridge		Rsvd	
0111	Page_Select			Rsvd	Port_Select			

表 13-2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus reset until the self-ID has completed as indicated by an unsolicited register 0 status transfer from the PHY to the LLC.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable-power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus reset. The RHB bit is reset to 0 by a hardware reset and is unaffected by a bus reset. If two nodes on a single bus have their root holdoff bit set, then the result is not defined. To prevent two nodes from having their root-holdoff bit set, this bit must only be written using a PHY configuration packet.
IBR	1	Rd/Wr	Initiate bus reset. This bit instructs the PHY to initiate a long (166-µs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is reset to 0 after a hardware reset or a bus reset. Care must be exercised when writing to this bit to not change the other bits in this register. It is recommended that whenever possible a bus reset be initiated using the ISBR bit and not the IBR bit.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet). **It is strongly recommended that this field only be changed using PHY configuration packets.**
Extended	3	Rd	Extended register definition. For the TSB41BA3F-EP, this field is 111b, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For the TSB41BA3F-EP, this field is 3.
PHY_Speed	3	Rd	PHY speed capability. This field is no longer used. For the TSB41BA3F-EP PHY, this field is 111b. Speeds for 1394b PHYs must be checked on a port-by-port basis.

Copyright © 2023 Texas Instruments Incorporated

表 13-2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
SREN	1	Rd/Wr	Standby/restore enable. This bit when set to 1 enables the port to go into the standby reduced power state when commanded by a Standby PHY command packet. This enable works for all ports of the local device. Note the 1394b standard only allows leaf (one port connected) nodes to be placed into standby mode.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst-case repeater data delay of the PHY, expressed as 144+(delay × 20) ns. For the TSB41BA3F-EP, this field is Fh. The worst-case repeater delay for S100B is 361 ns.
LCtrl	1	Rd/Wr	Link-active status control. This bit controls the indicated active status of the LLC reported in the self-ID packet. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC bit in the node self-ID packet is set active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software-controllable means to indicate the LLC self-ID active status in lieu of using the LPS input terminal. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus reset. 注 NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information continue to be presented on the interface, and any requests indicated on the LREQ input are processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to 0 on hardware reset. After hardware reset, this bit can only be set via a software register write. This bit is unaffected by a bus reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst-case difference between the fastest and slowest repeater data delay, expressed as (jitter+1) × 20 ns. For the TSB41BA3F-EP, this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the S5–S0 input terminals on a hardware reset and is unaffected by a bus reset. See 表 5-1 and 表 13-9.
WDIE	1	Rd/Wr	Watchdog interrupt enable. This bit, if set to 1, enables the port event interrupt (PIE) bit to be set whenever resume operations begin on any port, or when any of the CTOI, CPSI, or STOI interrupt bits are set and the link interface is nonoperational. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the PHY to initiate a short (1.3 µs) arbitrated bus reset at the next opportunity. This bit is reset to 0 by a bus reset. It is recommended that short bus reset is the only reset type initiated by software. IEC 61883-6 requires that a node initiate short bus resets to minimize any disturbance to an audio stream. 注 NOTE: Legacy IEEE Std 1394-1995-compliant PHYs are not capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.

Copyright © 2023 Texas Instruments Incorporated

表 13-2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start and might indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the CTOI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the S5_LKON output to notify the LLC to service the interrupt. 注 NOTE: If the network is configured in a loop, then only those nodes which are part of the loop generate a configuration time-out interrupt. All other nodes instead time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus reset. This bit is only set when the bus topology includes 1394a nodes; otherwise, 1394b loop healing prevents loops from being formed in the topology.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low, indicating that cable power might be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit. If the CPSI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the S5_LKON output to notify the LLC to service the interrupt.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the STOI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the S5_LKON output to notify the LLC to service the interrupt.
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (WDIE) bit is set, then the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in 1394b mode. 注 NOTE: The use of accelerated arbitration is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. The EAA bit is set only if the attached LLC is 1394a-2000-compliant. If the LLC is not 1394a-2000 or 1394b-2002-compliant, then the use of the arbitration acceleration enhancements can interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multispeed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in 1394a-2000. This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in 1394b mode. 注 NOTE: The use of multispeed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multispeed concatenation requires that the attached LLC be 1394a-2000 or 1394b-2002-compliant.
Max Legacy SPD	3	Rd	Maximum legacy-path speed. This field holds the maximum speed capability of any legacy node (1394a-2000 or 1394-1995-compliant) as indicated in the self-ID packets received during bus initialization. Encoding is the same as for the PHY_SPEED field (but limited to S400 maximum).
BLINK	1	Rd	Beta-mode link. This bit indicates that a Beta-mode-capable link is attached to the PHY. This bit is set by the BMODE input terminal on the TSB41BA3F-EP.

Copyright © 2023 Texas Instruments Incorporated

表 13-2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Bridge	2	Rd/Wr	This field controls the value of the bridge (brdg) field in self-ID packet. The power reset value is 0. Details for when to set these bits are specified in the IEEE 1394.1 bridging specification.
Page_Select	3	Rd/Wr	Page_Select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by a hardware reset and is unaffected by bus reset.
Port_Select	4	Rd/Wr	Port_Select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus reset.

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. 表 13-3 shows the configuration of the port status page registers, and 表 13-4 gives the corresponding field descriptions. If the selected port is unimplemented, then all registers in the port status page are read as 0.

表 13-3. Page 0 (Port Status) Register Configuration

Address	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Astat			Bstat		Ch	Con	RxOK	Dis
1001	Negotiated_speed			PIE	Fault	Standby_fault	Disscrm	B_Only
1010	DC_connected	Max_port_speed			LPP	Cable_speed		
1011	Connection_unreliable	Reserved			Beta_mode	Reserved		
1100	Port_error							
1101	Reserved			Sleep_Flag	Sleep_enable	Loop_disable	In_standby	Hard_disable
1110	Reserved							
1111	Reserved		EASOD	ELSSD	FRT	FTD	Reserved	FPR

表 13-4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Astat	2	Rd	TPA line state. This field indicates the instantaneous TPA line state of the selected port, encoded as follows: **Code** **Arb Value** 11 Z 01 1 10 0 00 invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the Astat field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. 注 NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but this does not mean that the port is necessarily active. For 1394b-coupled connections, the Con bit is set when a port detects connection tones from the peer PHY and operating-speed negotiation is completed.

Copyright © 2023 Texas Instruments Incorporated

表 13-4. Page 0 (Port Status) Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
RxOK	1	Rd	Receive OK. In 1394a-2000 mode this bit indicates the reception of a debounced TPBias signal. In Beta mode, this bit indicates the reception of a continuous electrically valid signal. NOTE: RxOK is set to false during the time that only connection *tones* are detected in Beta mode.
Dis	1	Rd/Wr	Port disabled control. If this bit is 1, then the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset. When this bit is set, the port cannot become active; however, the port still tones, but does not establish an active connection.
Negotiated_speed	3	Rd	Indicates the maximum speed negotiated between this PHY port and its immediately connected port. The encoding is as for Max_port_speed. It is set during connection when in Beta mode or to a value established during self-ID when in 1394a-2000 mode.
PIE	1	Rd/Wr	Port-event-interrupt enable. When this bit is 1, a port event on the selected port sets the port-event-interrupt (PEI) bit and notifies the link. This bit is reset to 0 by a hardware reset and is unaffected by bus reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume fault or suspend fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
Standby_fault	1	Rd/Wr	This bit is set to 1 if an error is detected during a standby operation and cleared on exit from the standby state. A write of 1 to this bit or receipt of the appropriate remote command packet clears it to 0. When this bit is cleared, standby errors are cleared.
Disscrm	1	Rd/Wr	Disable scrambler. If this bit is set to 1, then the data sent during packet transmission is not scrambled.
B_Only	1	Rd	Beta-mode operation only. For the TSB41BA3F-EP, this bit is set to 0 for all ports when all ports are programmed as bilingual or a combination of bilingual and data-strobe (1394a) only. If a port has been programmed to be Beta-only at a selected speed (for example B1 is Beta-only S100), then this bit is set to 1.
DC_connected	1	Rd	If this bit is set to 1, the port has detected a dc connection to the peer port by means of a 1394a-style connect-detect circuit.
Max_port_speed	3	Rd/Wr	Max_port_speed The maximum speed at which a port is allowed to operate in Beta mode. The encoding is: 000 = S100 001 = S200 010 = S400 011 = S800 100 = S1600 101 = S3200 110 = reserved 111 = reserved An attempt to write to the register with a value greater than the hardware capability of the port results in the maximum value that the port is capable of being stored in the register. The port uses this register only when a new connection is established in the Beta mode or when a port is programmed as a Beta-only port. When a port is programmed as a bilingual port, it is fixed at S400 for the Beta speed and is not updated by a write to this register. The power reset value is the maximum speed capable of the port. Software can modify this value to force a port to train at a lower-than-maximum speed (when in a Beta-only mode), but no lower than the minimum speed.
LPP (Local_plug_present)	1	Rd	This flag is set permanently to 1.
Cable_speed	3	Rd	This variable is set to the maximum speed that the port is capable of in Beta mode. The encoding is the same as for Max_port_speed.
Connection_unreliable	1	Rd/Wr	If this bit is set to 1, then a Beta-mode speed negotiation has failed or synchronization has failed. A write of 1 to this field resets the value to 0.

Copyright © 2023 Texas Instruments Incorporated

表 13-4. Page 0 (Port Status) Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Beta_mode	1	Rd	Operating in Beta mode. If this bit is 1, the port is operating in Beta mode; it is equal to 0 otherwise (that is, when operating in 1394a-2000 mode, or when disconnected). If Con is 1, RxOK is 1, and Beta_mode is 0, then the port is active and operating in the 1394a-2000 mode.
Port_error	8	Rd/Wr	Incremented whenever the port receives an invalid codeword, unless the value is already 255. Cleared when read (including being read by means of a remote access packet). Intended for use by a single bus-wide diagnostic program.
Sleep_Flag	1	Rd	This bit is set to 1 if the port is in the sleep state. The transition to the sleep state occurs only if the port has been enabled for the sleep mode.
Sleep_enable	1	Rd/Wr	This bit is set to 1 if the port has been enabled for sleep mode. If the SLPEN terminal is sampled high during reset, then this bit is set high for all ports. If sampled low, then it is 0. Software can individually enable or disasble sleep mode for a port by writing to this bit. Sleep mode operation is described in the IDB-1394 specification. In PMC mode when no link is present, the sleep state of each port can be monitored on the data lines as described in the Terminal Functions table entry for LCLK_PMC.
Loop_disable	1	Rd	This bit is set to 1 if the port has been placed in the loop-disable state as part of the loop-free build process (the PHYs at either end of the connection are active, but if the connection itself were activated, then a loop would exist). Cleared on bus reset and on disconnection.
In_standby	1	Rd	This bit is set to 1 if the port is in standby power-management state.
Hard_disable	1	Rd/Wr	No effect unless the port is disabled. If this bit is set to 1, the port does not maintain connectivity status on an ac connection when disabled. The values of the Con and RxOK bits are forced to 0. This flag can be used to force renegotiation of the speed of a connection. It can also be used to place the device into a lower-power state because when hard-disabled, a port no longer tones to maintain 1394b ac-connectivity status.
EASOD	1	Rd/Wr	Enhancement auto-shut-off disable (EASOD). This bit is set to EASOD = 0 at power-up reset. EASOD set to 1 when the Automatic Enhancement Shut-Off Counter (AESOC) reaches 15. This bit can be set or cleared with a local link PHY register write.
ELSSD	1	Rd/Wr	Enable loss-of-scrambler-sync detection. This bit is set ELSSD = 1 at power-up reset. This bit can be set or cleared with a local link PHY register write.
FRT	1	Rd/Wr	Fast Retrain Enable (FRT). When FRT = 1 Fast Retrain enhancement is enabled. When FRT = 0 Fast Retrain enhancement is disabled. At powerup/ PHY reset, this bit will be set true unless a hardware programming signal set the default to false. See セクション 13.2.3 for details.
FTD	1	Rd/Wr	Fast Connection Tone Debounce Enable (FTD). This bit, if set, enables the port to bypass the tone debounce step and go directly to speednegotiation during the Beta connection process. At power-up/ PHY reset, this bit will be set true unless a hardware programming signal set the default to false. See セクション 13.2.3 for details. **NOTE**: FTD should only be enabled when it is known that no connection debounce is needed, i.e., in a fixed topology.
FPR	1	Rd/Wr	Fast Power-On Re-Connect (FPR) Enable. When FPR = 1 Fast Power-On Re-Connect enhancement is enabled. When FPR = 0 Fast Power-On Re- Connect is disabled. At power-up/ PHY reset, this bit will be set true unless a hardware programming signal set the default to false. See セクション 13.2.3 for details.

The vendor identification page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select fieldin base register 7. 表 13-5 shows the configuration of the vendor identification page, and 表 13-6 shows the corresponding field descriptions.

Copyright © 2023 Texas Instruments Incorporated

表 13-5. Page 1 (Vendor Id) Register Configuration

Address	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID0							
1011	Vendor_ID1							
1100	Vendor_ID2							
1101	Product_ID0							
1110	Product_ID1							
1111	Product_ID2							

表 13-6. Page 1 (Vendor Id) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB41BA3F-EP, this field is 02h, indicating compliance with the 1394b-2002 specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB41BA3F-EP, this field is 08_00_28h (Texas Instruments) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the TSB41BA3F-EP, this field is 83_40_07h (the MSB is at register address 1101b).

The vendor-dependent page provides access to the special control features of the TSB41BA3F-EP, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select fieldin base register 7. 表 13-7 shows the configuration of the vendor-dependent page and 表 13-8 shows the corresponding field descriptions.

表 13-7. Page 7 (Vendor-Dependent) Register Configuration

Address	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Reserved		MAX_INVALID_EXT		Reserved		Reserved	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	SWR	Reserved for test						
1111	Reserved for test							

表 13-8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
MAX_INVALID_EXT	2	Rd/Wr	The count limit used in the loss-of-sync logic is: 4*MAX_INVALID_EXT + 3. At Power On Reset the MAX_INVALID_EXT field is set to ‘b10 (2) when enhancements are enabled and to 0 otherwise. (I.e., the invalid count limit is increased to 11 when enhancements are enabled at Power On Reset).
SWR	1	Rd/Wr	Software hard reset. Writing a 1 to this bit forces a hard reset of the PHY (same effect as momentarily asserting the $\overline{\text{RESET}}$ terminal low). This bit is always read as a 0.

13.2.3 Feature Enhancements to revision F

Several new features have been added to the IEEE-1394-2008 standard implementation to increase the robustness of IEEE-1394 Beta connections.

Copyright © 2023 Texas Instruments Incorporated

13.2.3.1 Detect Loss of Descrambler Synchronization

If for some reason the descrambler loses synchronization with the incoming scrambled 8b10b symbols, the receiving PHY will not detect them as invalid characters and will not increment invalidCount. This causes it to miss-interpret the incoming symbols and could result in the generation of multiple bus resets in a short period of time. This situation can not be resolved until the descrambler is re-synchronized with the incoming scrambled 8b10b symbols which only occurs during training. This enhancement to the IEEE-1394-2008 Standard has the PHY detect the loss of descrambler synchronization. When loss of descrambler synchronization is detected, the port is forced to exit the P2:Active state. This forces the port to retrain the descrambler with the incoming scrambled symbols. The ELSSD register bit enables and disable this enhancement. ELSSD bit is enabled by default upon reset.

13.2.3.1.1 Detect Loss of Descrambler Synchronization Advantages and Uses

This enhancement, along with the Fast-Retrain enhancement, minimizes the impact of the loss of descrambler synchronization from many bus resets and approximately 500 milliseconds of connection loss to two bus resets and as little as 200 microseconds of connection loss.

13.2.3.2 Fast Retrain

In revision D and prior, If for some reason (physical disconnect or intermediate signal degradation) the port connection between IEEE-1394 Beta ports lose synchronization, the PHY will transition the port connection from P2:Active state to P0:Disconnected and a minimum reconnect time of approximately 500 milliseconds is required. IEEE-1394-2008 section 13.3.2.1.2 Resynchronization procedure touches on resynchronization when a port determines synchronization has been lost, however it doesn't fully define it. This enhancement to the IEEE-1394-2008 Standard fully defines the resynchronization procedure, Fast-Retrain. The Fast-Retrain process has the potential to speed up the loss of connection time from approximately 500 milliseconds to a few hundred microseconds. The Fast-Retrain enhancement allows an IEEE-1394 Beta connection to attempt to retrain a connection that has lost synchronization by attempting to immediately train the connection at the previously connected data rate.

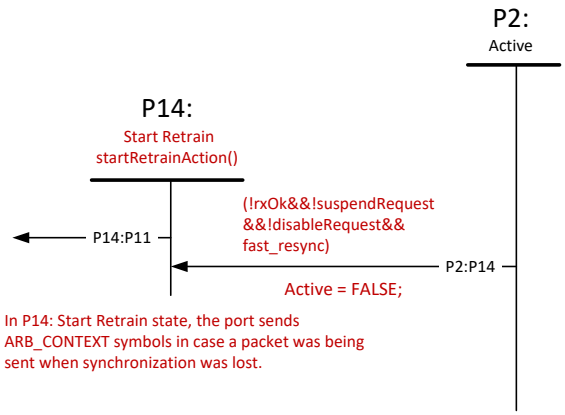


図 13-1. Fast-Retrain Port Connection State Machine Changes

P2:P14

If Fast-Retrain is enabled (fast_resync = 1) and the port detects a loss of synchronization (!rxOk && ! suspendRequest && !disableRequest && fast_resync) the port transitions from the P2:Active to the P14: Start Retrain state.

P14: Start Retrain

In the P14: Start Retrain state 2 to 16 ARB_CONTEXT characters are sent before transitioning to the P11:Untested state. The transmission of ARB_CONTEXT characters are sent in case the port was transmitting a packet when the loss of synchronization occurred.

P14:P11

Copyright © 2023 Texas Instruments Incorporated

Upon entry into the P11:Untested state the port immediately starts the training process at the previously connected data rate. For this reason, the tone based speed negotiation is not required and transmission of 8b10b symbols can begin immediately. After this point the normal Untested state process is followed.

If the retrain process doesn't complete after DISCONNECTED_TONE_INTERVAL (42.66 to 48 milliseconds) the ports will force disconnect and transition through the P12:Loop Disabled state to P0:Disconnected.

13.2.3.2.1 Fast-Retrain Advantages and Uses

This enhancement minimizes the impact of an intermediate signal degradation causing a loss of synchronization from two bus resets and approximately 500 milliseconds of connection loss to two bus resets and as little as 200 microseconds of connection loss. While the benefits of Fast-Retrain are obvious, if the intermediate signal degradation causes the port to lose synchronization often there is a potential to create multiple bus resets in a short period of time. Multiple bus resets would adversely affect the operation of the rest of the IEEE-1394 bus.

To limit the effects of multiple bus resets in a short period of time, the Fast-Retrain enhancement implements automatic enhancement shut off. The automatic enhancement shut-off is triggered when the Automatic Enhancement Shut-Off Counter (AESOC) reaches 15. This counter is incremented whenever the port transitions from the P11:Untested state to the P2:Active state, and is decremented every 5.33 milliseconds if non-zero. Therefore, if the port re-connects at an average rate of more than once every 5.33 milliseconds the automatic enhancements shut-off will be triggered, and the Fast-Retrain, Fast Power-On Re-connect, and Fast Connection enhancements for that port are all disabled. If the Enhancement Auto-Shut-Off Disable bit is set to 1, this automatic shut-off feature is disabled.

When EASOD is set true, the Fast-Retrain, Fast Power-On and Fast Connection Debounce for that port are all disabled.

13.2.3.2.2 Fast-Retrain Backward Compatibility

Fast-Retrain maintains backward compatibility with IEEE-1394-2008 and IEEE-1394b-2002 implementations. In the case of a temporary loss of signal, when a non-Fast-Retrain PHY port exits the P2:Active state because of a loss of synchronization it will transition through the P3:Suspend Initiator and P5:Suspended states to P0:Disconnected. The Fast-Retrain port will fail to retrain and will transition to P12:Loop Disabled state from the P11:Untested state. However, as the non-Fast-Retrain port doesn't transmit a tone for approximately 84 milliseconds after the loss of synchronization, the Fast-Retrain port will not detect a connection and will then transition to the P0:Disconnected state. In the case of physical disconnect the Fast-Retrain port will end up in the P0:Disconnected state waiting for a new connection.

13.2.3.3 Fast Power-On Re-connect

In environments where connections are mostly static, where connections mostly consist of nodes being powered on and not plugged in, it can be advantageous to shorten the connection time from over 500 milliseconds to hundreds of microseconds. The Fast Power-On Re-connect enhancement enables this quick connection behavior while maintaining backward compatibility. Fast Power-On Re-Connect was designed to facilitate faster reconnection when one device and/or PHY is power cycled/reset for some reason and comes back online. IMPORTANT NOTE: Because the Fast Power-On Re-Connect process doesn't conduct speed negotiation it can only attempt to connect at the maximum connection port speed (maxPortSpeed). Connecting two Fast Power-On Re-Connect capable PHYs with different maxPortSpeeds will result in both PHY's ports entering the P12:Loop Disabled state with connectionUnreliable set to 1.

Copyright © 2023 Texas Instruments Incorporated

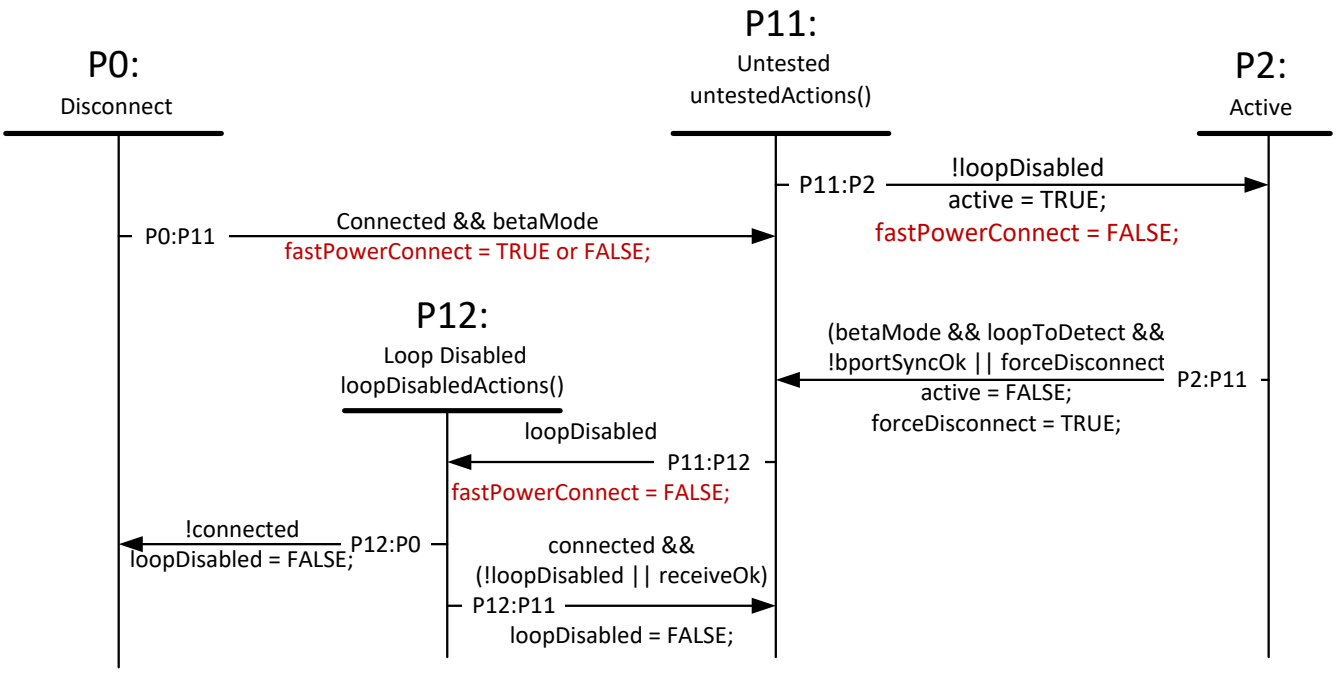


図 13-2. Fast Power-On Re-Connect Port Connection State Machine Changes

Copyright © 2023 Texas Instruments Incorporated

P0: Disconnect

When a Fast Power-On Re-Connect enabled port is in the P0: Disconnect state for at least 1.66 milliseconds and then it detects a continuous tone for 1.66 milliseconds (this is not a IEEE-1394-2008 666usec tone but rather a betaMode (betaMode = TRUE) Fast Power-On Re-Connect tone (connected = TRUE)) the port will transition from P0:Disconnected to P11:Untested state and set fastPowerConnect = TRUE. If the transition from P0:Disconnected to P11:Untested occurs because of a non-continuous tone, the port will set fastPowerConnect = FALSE. The continuous tone indicates that the attached PHY also supports Fast Power-On Re-Connect and is in the P11:Untested state and is transmitting 8b10b Training symbols in an attempt to synchronize.

P0:P11

fastPowerConnect = TRUE if continuous tone or FALSE is not continuous tone.

P11: Untested with fastPowerConnect = TRUE

Much like the transition from P14: Start Retrain, the port immediately starts Training. However, the data rate is determined by the maxPortSpeed. If the Retrain process doesn't complete after 42.67 milliseconds the ports will force disconnect and transition through the P12:Loop Disabled state to P0:Disconnected.

13.2.3.3.1 Fast Power-On Re-Connect Advantages and Uses

Fast Power-On Re-Connect was designed to facilitate faster reconnect of a connection when one device and/or PHY is power cycled/reset for some reason and comes back online.

This mechanism assumes that the port was previously Beta connected and in the P2:Active state when the device and/or PHY was reset/power cycled. If the connected peer port supports Fast Retrain it will lose symbol synchronization and will go to the P11: Untested state in an attempt to re-establish synchronization. It will attempt to Retrain for a DISCONNECTED_TONE_INTERVAL (42.66 to 48 milliseconds). If device and/or PHY comes back online while the peer is still in the P11:Untested state (sending continuous tones), the Fast Power-On Re-Connect port will transition directly to P11:Untested and start the Training process at maxPortSpeed. This should reduce the total reconnect time from approximately 500 milliseconds to approximately 5 milliseconds.

13.2.3.3.2 Fast Power-On Re-Connect Backward Compatibility

When a Fast Power-On Re-Connect device and/or PHY is connected to an IEEE-1394-2008 Beta PHY and it is power cycled/reset the IEEE-1394-2008 Beta PHY port will go to the P0:Disconnected state and send non-continuous tones (666 microsecond tones).

When the Fast Power-On Re-Connect capable device and/or PHY comes back online, it doesn't see continuous tones therefore after the appropriate number of connection tones are observed it sets fastPowerConnect = FALSE and transitions to P11:Untested state.

13.2.3.4 Fast Connection Tone Debounce

In environments where connections are mostly static where, connections mostly consist of nodes being powered on and not plugged in, it can be advantageous to shorten the connection time from over 500 milliseconds to less than 100 milliseconds. The Fast Connection Tone Debounce enhancement enables this quick connection behavior while maintaining backward compatibility.

P0: Disconnected

When Fast Connection Tone Debounce is enabled the port immediately starts transmitting connection tones while listen for connection tones. Once a valid connection tone (not continuous tone) is received, connected is set TRUE, fastPowerConnect is set FALSE and the state transitions from P0:Disconnected to P11:Untested to start speed negotiation.

P0:P11

fastPowerConnect = FALSE;

Copyright © 2023 Texas Instruments Incorporated

P11: Untested

The port then sends both connection and speed negotiation tones while listening for both connection and speed negotiation tones, it doesn't wait 10 connection intervals before it sends or listens for speed negotiation tones. Once the speed is successfully negotiated it follows the IEEE-1394-2008 P11:Untested state training and loop free build process.

注

NOTE: Fast Connection Tone Debounce reduces the connection debounce time from 426 milliseconds to approximately 42.6 milliseconds. Therefore, it should only be enabled when it is known that no connection debounce is needed, i.e., in a fixed topology.

13.2.3.5 Programmable invalidCount

When a port is in the P2:Active state if the invalidCount exceeds the value of 0x3 the port has lost synchronization and it shall exit the P2:Active state. The intent of the value of 0x3 is unclear but it is thought that a higher value may increase the invalid signal tolerance and may reduce the number of disconnects due to loss of synchronization. With the Fast Retrain feature, the value in making the invalidCount programmable has diminished. A programmable invalidCount register has been created with a default of 0x3 when this enhancement is disabled, and 0xB when this enhancement is enabled. See for details.

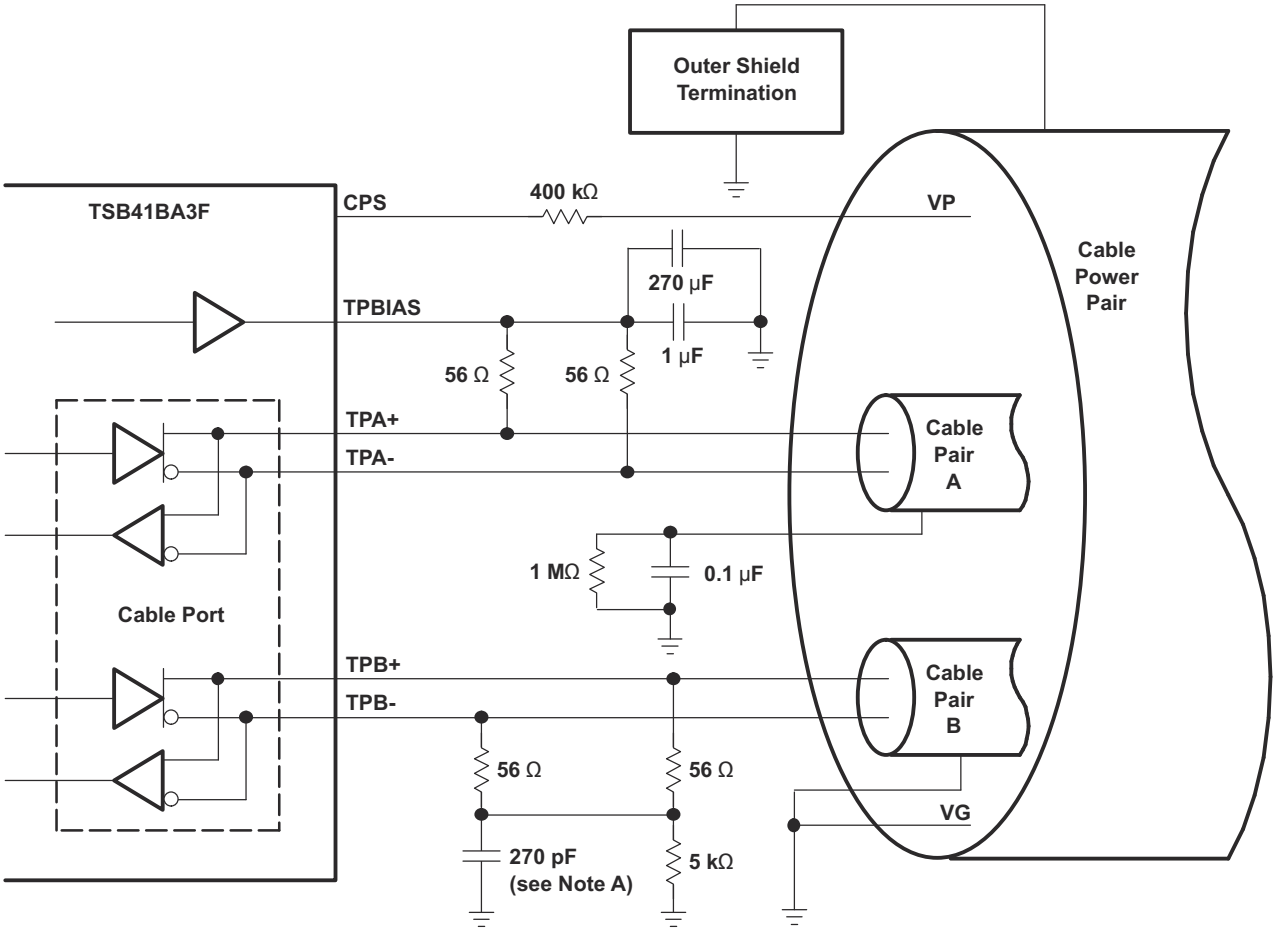
13.2.4 Power-Class Programming

The S2_PC0, S1_PC1, and S0_PC2 terminals can be used in some port speed/mode selections to set the default value of the power-class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Descriptions of the various power-classes are given in 表 13-9. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

表 13-9. Power-Class Descriptions

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node can be powered from the bus and is using up to 3 W; no additional power is needed to enable the link. The node can also provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Reserved for future standardization.
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.

Copyright © 2023 Texas Instruments Incorporated



A. The IEEE Std 1394-1995 calls for a 250-pF capacitor, which is a nonstandard component value. A 270-pF capacitor is recommended.

図 13-3. Typical TP Cable Connections

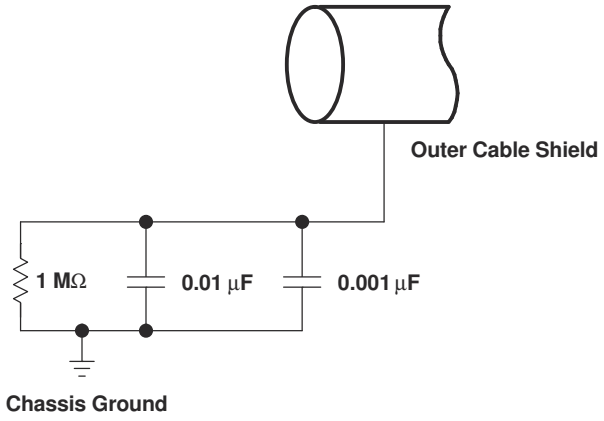


図 13-4. Typical DC-Isolated Outer Shield Termination

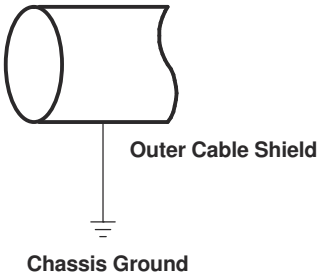


図 13-5. Non-DC-Isolated Outer Shield Termination

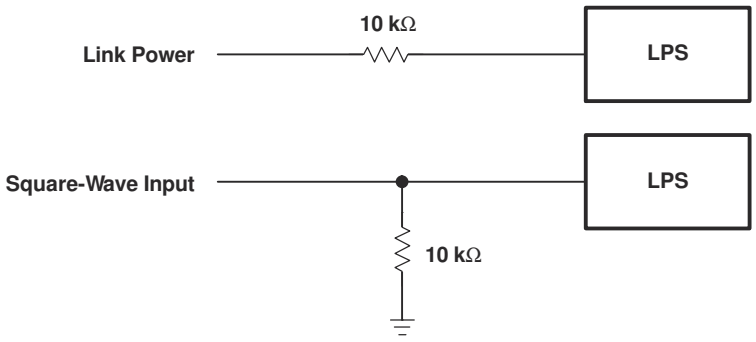


図 13-6. Nonisolated Connection Variations For LPS

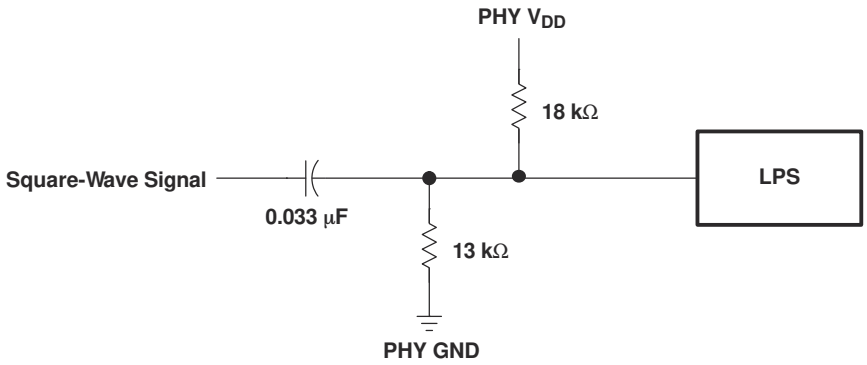


図 13-7. Isolated Circuit Connection For LPS

13.2.5 Using The TSB41BA3F-EP With A 1394-1995 Or 1394a-2000 Link Layer

The TSB41BA3F-EP implements the PHY-LLC interface specified in the 1394b Supplement. This interface is based on the interface described in Section 17 of IEEE 1394b-2002. When using an LLC that is compliant with the IEEE 1394b-2002 interface, the BMODE input must be tied high.

The TSB41BA3F-EP also functions with an LLC that is compliant with the older 1394 standards. This interface is compatible with both the older Annex J interface specified in the IEEE Std 1394-1995 (with the exception of the Annex J isolation interfacing method) and the PHY-LLC interface specified in 1394a-2000. When using an LLC that is not compliant with the IEEE 1394b-2002 interface, the BMODE input must be tied low.

When the BMODE input is tied low, the TSB41BA3F-EP implements the PHY-LLC interface specified in the 1394a-2000 Supplement. This interface is based on the interface described in informative Annex J of IEEE Std 1394-1995, which is the interface used in the oldest Texas Instruments PHY devices. The PHY-LLC interface specified in 1394a-2000 is compatible with the older Annex J. However, the TSB41BA3F-EP does not support the Annex J isolation interfacing method. When implementing the 1394a-2000 interface, certain signals are not used:

Copyright © 2023 Texas Instruments Incorporated

- The PINT output (terminal 1) can be left open.
- The LCLK_PMC input (terminal 7) must be tied directly to ground or through a pulldown resistor of ~1 kΩ or less, unless the PMC mode is desired (see LCLK_PMC terminal description).

All other signals are connected to their counterparts on the 1394a link-layer controller. The PCLK output corresponds to the SCLK input signal on most LLCs.

The 1394a-2000 Supplement includes enhancements to the Annex J interface that should be comprehended when using the TSB41BA3F-EP with a 1394-1995 LLC device.

- A new LLC service request was added which allows the LLC to temporarily enable and disable asynchronous arbitration accelerations. If the LLC does not implement this new service request, then the arbitration enhancements must not be enabled (see the EAA bit in PHY register 5).
- The capability to perform multispeed concatenation (the concatenation of packets of differing speeds) was added in order to improve bus efficiency (primarily during isochronous transmission). If the LLC does not support multispeed concatenation, then multispeed concatenation must not be enabled in the PHY (see the EMC bit in PHY register 5).
- In order to accommodate the higher transmission speeds expected in future revisions of the standard, 1394a-2000 extended the speed code in bus requests from 2 bits to 3 bits, increasing the length of the bus request from 7 bits to 8 bits. The new speed codes were carefully selected so that new 1394a-2000 PHY and LLC devices would be compatible, for speeds from S100 to S400, with legacy PHY and LLC devices that use the 2-bit speed codes. The TSB41BA3F-EP correctly interprets both 7-bit bus requests (with 2-bit speed code) and 8-bit bus requests (with 3-bit speed codes). Moreover, if a 7-bit bus request is immediately followed by another request (for example, a register read or write request), then the TSB41BA3F-EP correctly interprets both requests. Although the TSB41BA3F-EP correctly interprets 8-bit bus requests, a request with a speed code exceeding S400 while in 1394a-2000 PHY-link interface mode results in the TSB41BA3F-EP transmitting a null packet (data prefix followed by data end, with no data in the packet).

13.2.6 Power-Up Reset

To ensure proper operation of the TSB41BA3F-EP, the $\overline{\text{RESET}}$ terminal must be asserted low for a minimum of 2 ms from the time that PHY power reaches the minimum required supply voltage and the input clock to the PHY is valid. When using a passive capacitor on the $\overline{\text{RESET}}$ terminal to generate a power-on-reset signal, the minimum reset time is ensured if the value of the capacitor satisfies the following equation (the value must be no smaller than approximately 0.1 µF):

C_{min} = 0.0077 × T + 0.085 + (external_oscillator_start-up_time × 0.05)

Where C_{min} is the minimum capacitance on the $\overline{\text{RESET}}$ terminal in µF, T is the V_{DD} ramp time, 10%–90%, in ms, external_oscillator_start-up_time is the time in ms from application of power to the external oscillator until the oscillator outputs a valid clock. If a crystal is used rather than an oscillator, then the external_oscillator_start-up_time can be set to 0.

For example with a 2-ms power ramp time and a 2-ms oscillator start-up time:

C_{min} = 0.0077 × 2 + 0.085 + (2 × 0.05) = 0.2 µF

It is appropriate to select the nearest standard value capacitor that exceeds this value, for example 0.22 µF.

Or with a 2-ms power ramp time and a 49.152-MHz fundamental crystal:

C_{min} = 0.0077 × 2 + 0.085 + (0 × 0.05) = 0.1 µF

13.2.7 Crystal Selection

The TSB41BA3F-EP and other Texas Instruments PHY devices are designed to use an external 49.152-MHz crystal connected between the XI and XO terminals to provide the reference for an internal oscillator circuit. This oscillator in turn drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S400 media data rates.

A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE Std 1394. Adjacent PHYs can therefore have a difference of up to 200 ppm from each other in their internal clocks, and PHYs must

Copyright © 2023 Texas Instruments Incorporated

be able to compensate for this difference over the maximum packet length. Larger clock variations can cause resynchronization overflows or underflows, resulting in corrupted packet data or even PHY lockup.

For the TSB41BA3F-EP, the PCLK output can be used to measure the frequency accuracy and stability of the internal oscillator and PLL from which it is derived. When operating the PHY-LLC interface with a non-1394b LLC, the frequency of the PCLK output must be within ±100 ppm of the nominal frequency of 49.152 MHz. When operating the PHY-LLC interface with a 1394b LLC, the frequency of the PCLK output must be within ±100 ppm of the nominal frequency of 98.304 MHz.

The following are some typical specifications for crystals used with the physical layers from Texas Instruments in order to achieve the required frequency accuracy and stability:

- Crystal mode of operation: Fundamental
- Frequency tolerance at 25°C: Total frequency variation for the complete circuit is ±100 ppm. A crystal with ±30 ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A crystal with ±30 ppm frequency stability is recommended for adequate margin.

注

The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability can be made as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal can be specified at 50 ppm, and the temperature tolerance can be specified at 30 ppm to give a total of 80 ppm possible variation due to the oscillator alone. Aging also contributes to the frequency variation.

- Load capacitance: For parallel resonant mode crystal circuits, the frequency of oscillation depends on the load capacitance specified for the crystal. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also board layout and circuit. It might be necessary to select discrete load capacitors iteratively until the PCLK output is within specification. It is recommended that load capacitors with a maximum of ±5% tolerance be used.

As an example, for the OHCI + 41LV03 evaluation module (EVM), which uses a crystal specified for 12-pF loading, load capacitors (C9 and C10 in 図 13-8) of 16 pF each were appropriate for the layout of that particular board. The load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY terminals (C_{PHY}), and the loading of the board itself (C_{BD}). The value of C_{PHY} is typically about 1 pF and C_{BD} is typically 0.8 pF per centimeter of board etch; a typical board can have 3 pF to 6 pF or more. The load capacitors C9 and C10 combine as capacitors in series so that the total load capacitance is:

$$C_L = \frac{C9 \times C10}{C9 + C10} + C_{PHY} + C_{BD}$$

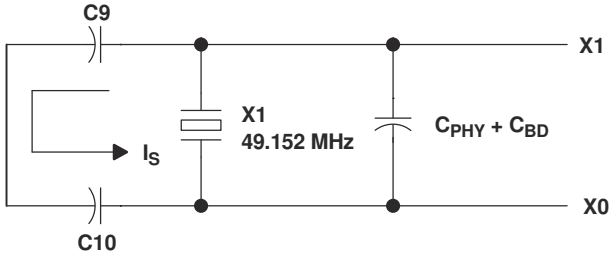


図 13-8. Load Capacitance for the TSB41BA3F-EP PHY

Copyright © 2023 Texas Instruments Incorporated

注

The layout of the crystal portion of the PHY circuit is important for obtaining the correct frequency, minimizing noise introduced into the PHY's phase-locked loop, and minimizing any emissions from the circuit. The crystal and two load capacitors must be considered as a unit during layout. The crystal and load capacitors must be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Varying the size of the capacitors can help in this. Minimizing the loop area minimizes the effect of the resonant current (I_S) that flows in this resonant circuit. This layout unit (crystal and load capacitors) must then be placed as close as possible to the PHY XI and XO terminals to minimize trace lengths.

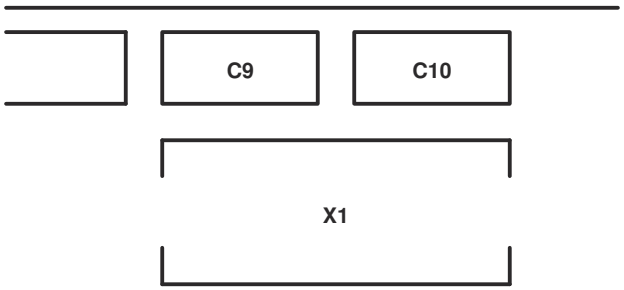


図 13-9. Recommended Crystal And Capacitor Layout

It is strongly recommended that part of the verification process for the design be to measure the frequency of the PCLK output of the PHY. This should be done using a frequency counter with an accuracy of six digits or better. If the PCLK frequency is more than the crystal's tolerance from 49.152 MHz or 98.304 MHz, then the load capacitance of the crystal can be varied to improve frequency accuracy. If the frequency is too high, add more load capacitance; if the frequency is too low, decrease the load capacitance. Typically, changes must be done to both load capacitors (C9 and C10 in 図 13-9) at the same time, and both must be of the same value. Additional design details and requirements can be provided by the crystal vendor.

13.2.8 Bus Reset

It is recommended, that whenever the user has a choice, the user should initiate a bus reset by writing to the initiate-short-bus-reset (ISBR) bit (bit 1, PHY register 0101b). Care must be taken to not change the value of any of the other writeable bits in this register when the ISBR bit is written to.

In the TSB41BA3F-EP, the initiate-bus-reset (IBR) bit can be set to 1 in order to initiate a bus reset and initialization sequence; however, it is recommended to use the ISBR bit instead. The IBR bit is located in PHY register 1 along with the root-holdoff bit (RHB) and gap-count register. As required by the 1394b Supplement, this configuration maintains compatibility with older Texas Instruments PHY designs which were based on either the suggested register set defined in Annex J of IEEE Std 1394-1995 or the 1394a-2000 Supplement. Therefore, whenever the IBR bit is written, the RHB and gap-count register are also necessarily written.

It is recommended that the RHB and gap-count register only be updated by PHY configuration packets. The TSB41BA3F-EP is 1394a- and 1394b-compliant, and therefore, both the reception and transmission of PHY configuration packets cause the RHB and gap-count register to be loaded, unlike older IEEE Std 1394-1995-compliant PHYs which decode only received PHY configuration packets.

The gap-count register is set to the maximum value of 63 after two consecutive bus resets without an intervening write to the gap-count register, either by a write to PHY register 1 or by a PHY configuration packet. This mechanism allows a PHY configuration packet to be transmitted and then a bus reset to be initiated so as to verify that all nodes on the bus have updated their RHBs and gap-count register values, without having the gap-count register set back to 63 by the bus reset. The subsequent connection of a new node to the bus, which initiates a bus reset, then causes the gap-count register of each node to be set to 63. Note, however, that if a subsequent bus reset is instead initiated by a write to register 1 to set the IBR bit, then all other nodes on the

Copyright © 2023 Texas Instruments Incorporated

bus have their gap-count register values set to 63, while this node's gap-count register remains set to the value just loaded by the write to PHY register 1.

Therefore, in order to maintain consistent gap-count registers throughout the bus, the following rules apply to the use of the IBR bit, RHB, and gap-count register in PHY register 1:

- Following the transmission of a PHY configuration packet, a bus reset must be initiated in order to verify that all nodes have correctly updated their RHBs and gap-count register values, and to ensure that a subsequent new connection to the bus causes the gap-count register to be set to 63 on all nodes in the bus. If this bus reset is initiated by setting the IBR bit to 1, then the RHB and gap-count register must also be loaded with the correct values consistent with the just-transmitted PHY configuration packet. In the TSB41BA3F-EP, the RHB and gap-count register have been updated to their correct values on the transmission of the PHY configuration packet and so these values can first be read from register 1 and then rewritten.
- Other than to initiate the bus reset, which must follow the transmission of a PHY configuration packet, whenever the IBR bit is set to 1 in order to initiate a bus reset, the gap-count register value must also be set to 63 so as to be consistent with other nodes on the bus, and the RHB must be maintained with its current value.
- The PHY register 1 must not be written to except to set the IBR bit. The RHB and gap-count register must not be written without also setting the IBR bit to 1.
- To avoid these problems, all bus resets initiated by software must be initiated by writing the ISBR bit (bit 1 PHY register 0101b). Care must be taken to not change the value of any of the other writeable bits in this register when the ISBR bit is written to. Also, the only means to change the gap count of any node must be by means of the PHY configuration packet, which changes all nodes to the same gap count.

13.2.9 Designing With Powerpad™ Devices

The TSB41BA3F-EP is housed in a high-performance, thermally enhanced, 80-terminal PFP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the thermal pad, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) might be required to prevent any inadvertent shorting by the exposed thermal pad of connection etches or vias under the package. The recommended option, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained In the following paragraphs. Although the actual size of the exposed die pad can vary, the maximum size required for the keepout area for the 80-terminal PFP PowerPAD package is 10 mm × 10 mm. The actual thermal pad size for the TSB41BA3F-EP is 6 mm × 6 mm.

It is required that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size, depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land might or might not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the Texas Instruments *PowerPAD™ Thermally Enhanced Package* application report (SLMA002) available via the Texas Instruments Web pages at URL http://www.ti.com.

Copyright © 2023 Texas Instruments Incorporated

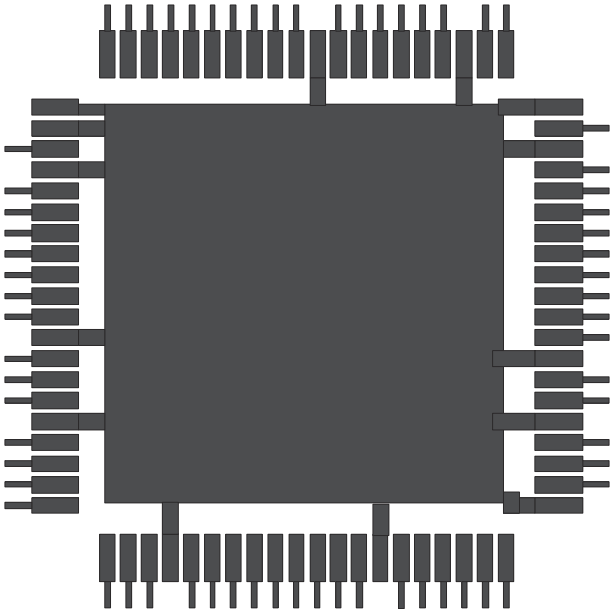


図 13-10. Example of a Thermal Land for the TSB41BA3F-EP PHY

For the TSB41BA3F-EP, this thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size ought to be as large as possible without shorting the device signal terminals. The thermal land can be soldered to the exposed thermal pad using standard reflow soldering techniques.

Although the thermal land can be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane for the device. More information can be obtained from the Texas Instruments application report *PHY Layout* (SLLA020).

Copyright © 2023 Texas Instruments Incorporated

14 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

14.1 Tools and Software

Design Kits and Evaluation Modules

Concise Description	Description

TI Designs and Reference Designs

Concise Description	Description

Software

Concise Description	Description

Development Tools

Concise Description	Description

Models

Concise Description	Description

14.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

Copyright © 2023 Texas Instruments Incorporated

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *your package*), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *your device speed range*). 図 14-1 provides a legend for reading the complete device name for any *your device* device.

For orderable part numbers of *your device* devices in the *your package* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *Silicon Errata*.

図 14-1. Device Nomenclature

14.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral is listed below.

Errata

Concise Description	Description

Application Reports

Concise Description	Description

User's Guides

Concise Description	Description

Selection and Solution Guides

Concise Description	Description

White Papers

Concise Description	Description

More Literature

Copyright © 2023 Texas Instruments Incorporated

Concise Description	Description

14.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により、現状のまま提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

14.5 Trademarks

Firewire™ is a trademark of Apple Computer, Inc.
i.LINK™ is a trademark of Sony Kabushiki Kaisha TA Sony Corporation.
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

14.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

14.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

Copyright © 2023 Texas Instruments Incorporated

15 Mechanical, Packaging, and Orderable Information

15.1 Packaging Information

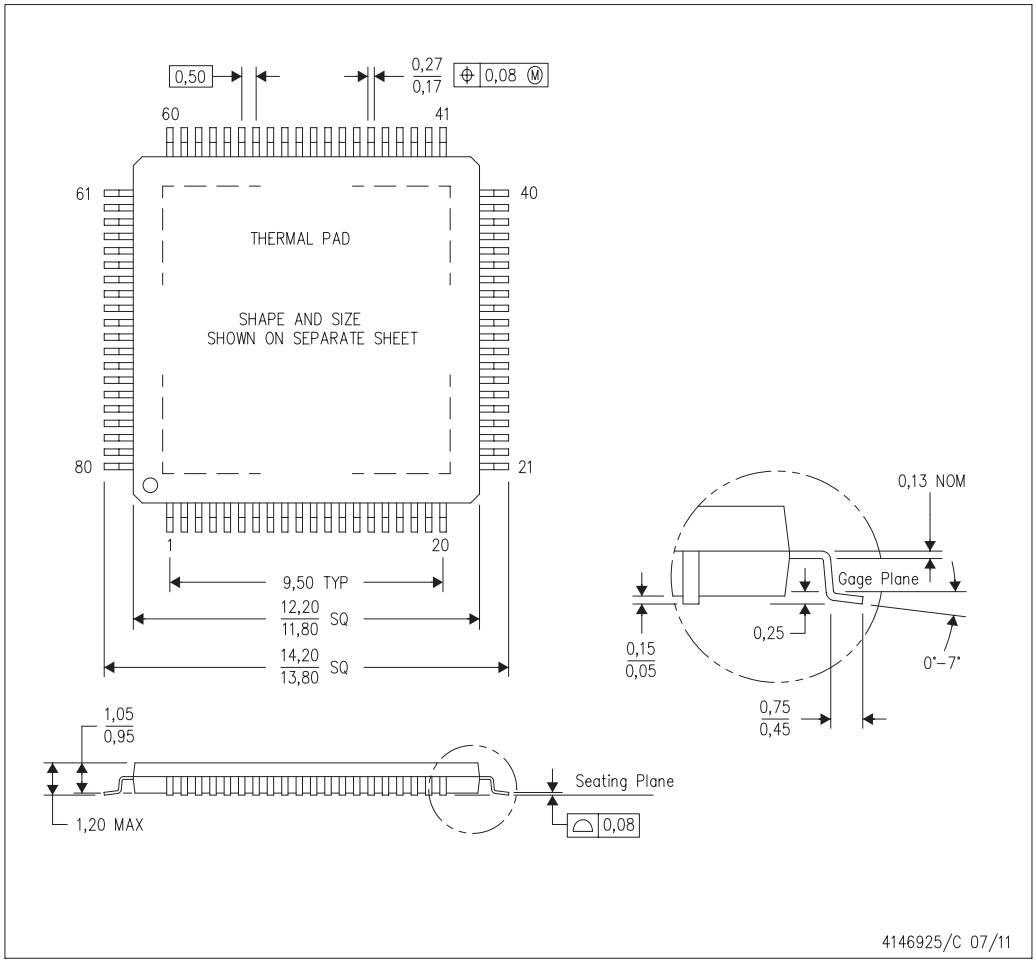
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

15.2 Mechanical Data

MECHANICAL DATA

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD Is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
www.ti.com

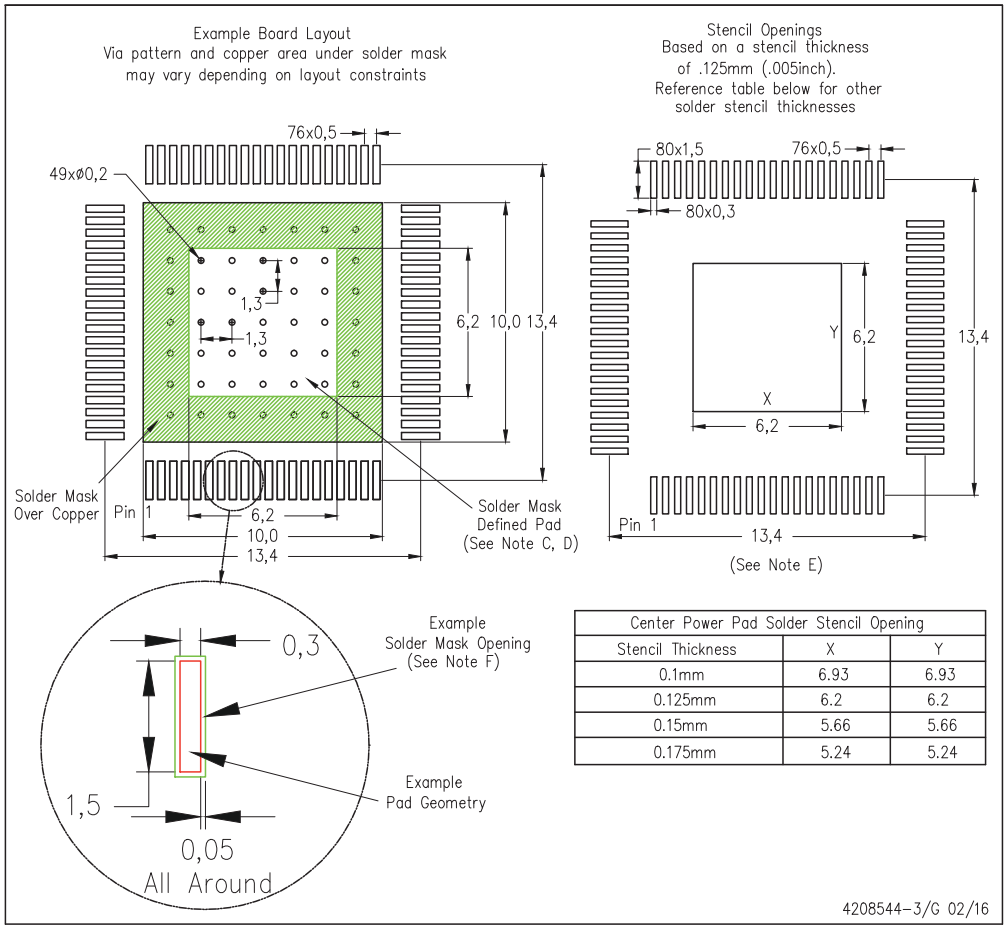
THERMAL PAD MECHANICAL DATA

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

Copyright © 2023 Texas Instruments Incorporated

LAND PATTERN DATA

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSB41BA3FTPFPEP	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 110	TSB41B3FEP
TSB41BA3FTPFPEP.A	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 110	TSB41B3FEP
V62/03670-04XE	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 110	TSB41B3FEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

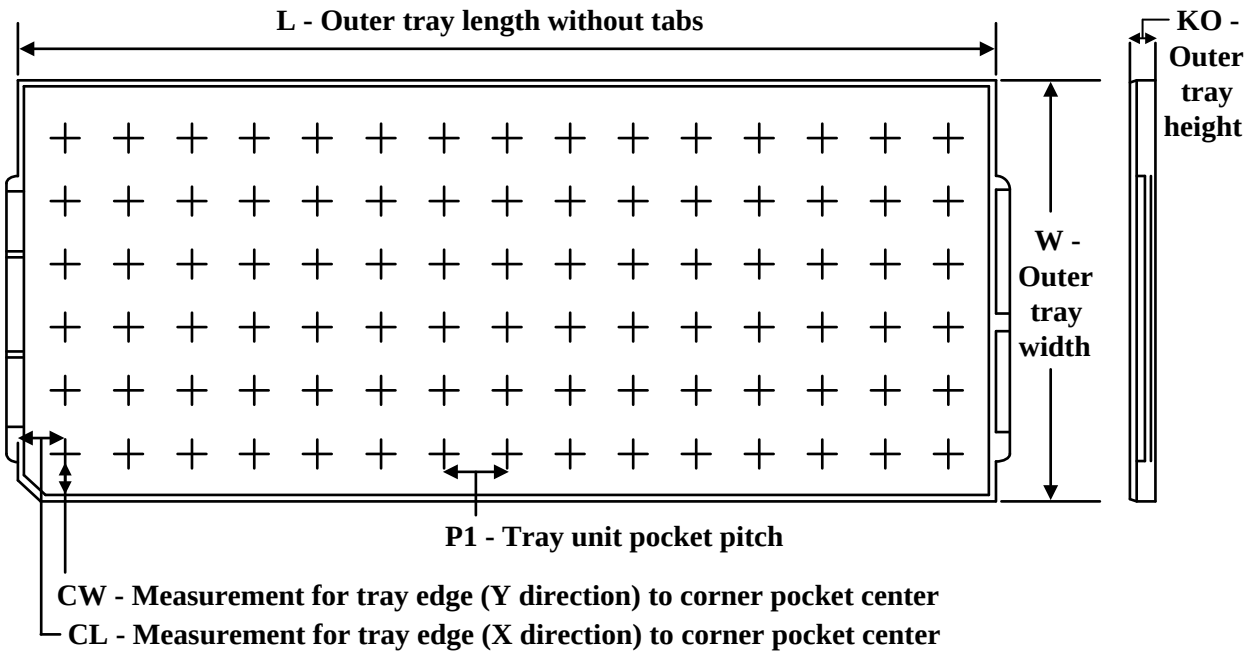
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY

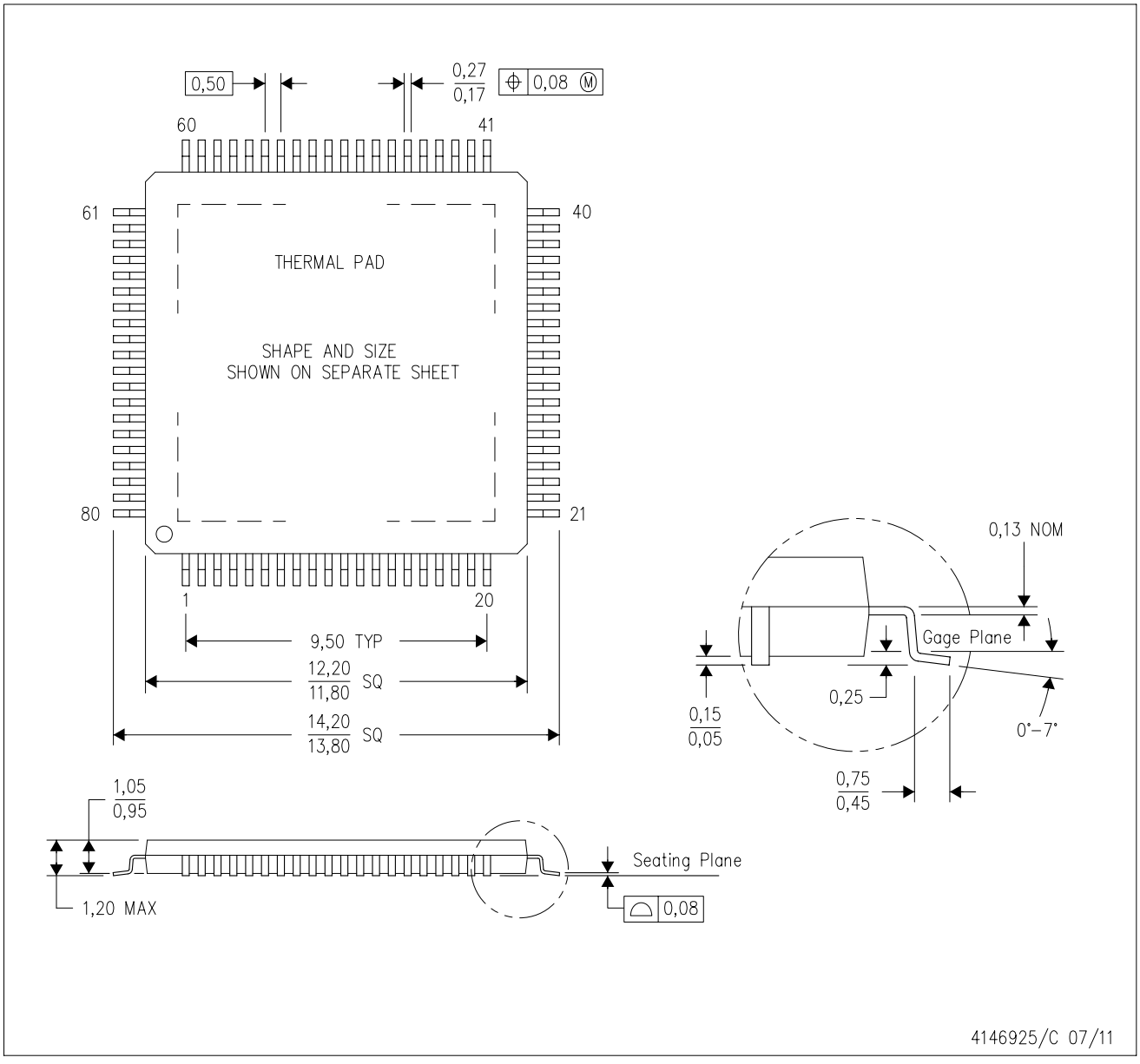


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSB41BA3FTPFPEP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TSB41BA3FTPFPEP.A	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
V62/03670-04XE	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

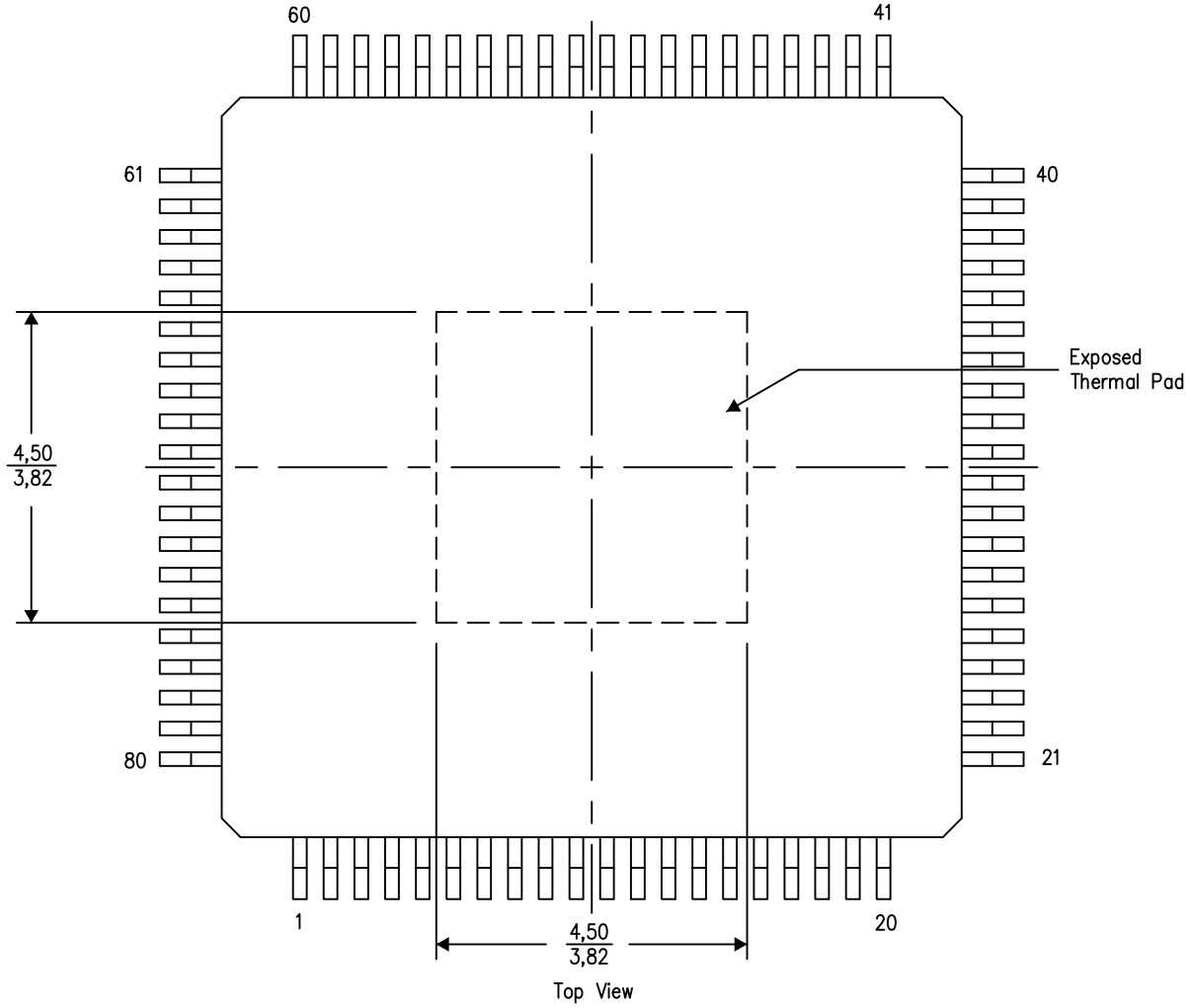
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



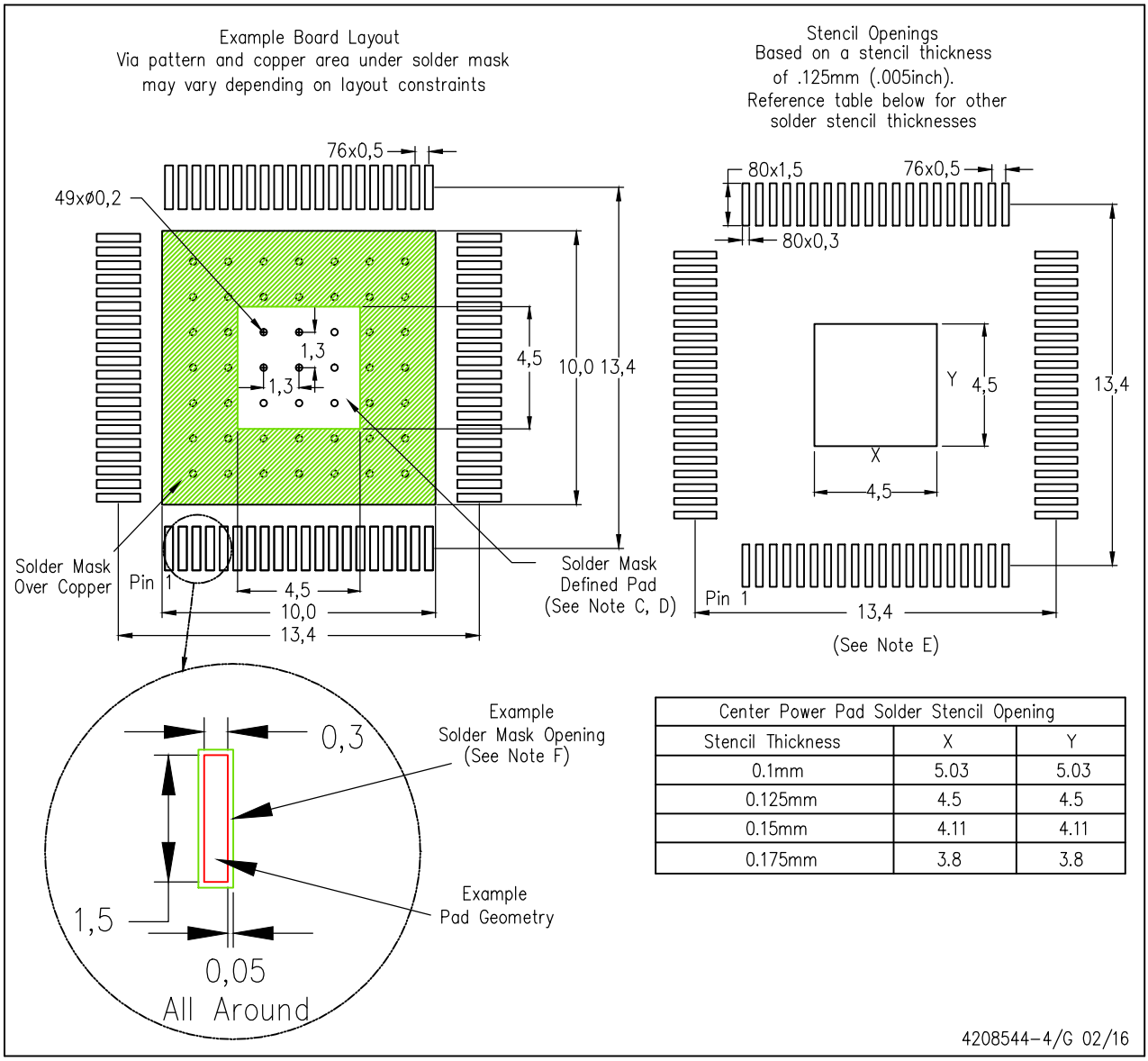
Exposed Thermal Pad Dimensions

4206327–15/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.03	5.03
0.125mm	4.5	4.5
0.15mm	4.11	4.11
0.175mm	3.8	3.8

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月