TUSB4020BI-Q1 車載用 2 ポートの USB 2.0 ハブ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 3：-40ºC～85ºC T_A
- 2 ポート USB 2.0 ハブ
- USB 2.0 ハブ機能：
  - マルチ トランザクション トランスレータ (MTT) ハブ：2 つのトランザクション トランスレータ
  - トランザクション トランスレータごとに 4 つの非同期エンドポイント バッファ
- Type C 互換
- バッテリ充電の規格
  - CDP モード (上流ポート接続時)
  - DCP モード (上流ポート未接続時)
  - DCP モードは中国電気通信業界標準 YD/T 1591-2009 に準拠
  - D+/D- デバイダ モード
- ポート単位または一括制御のパワー スイッチングおよび過電流通知入力
- OTP ROM、シリアル EEPROM、または I^2C/SMBus ターゲット インターフェイスで次のカスタム構成に対応：
  - VID および PID
  - ポートのカスタマイズ
  - メーカーおよび製品文字列 (OTP ROM は除く)
  - シリアル番号 (OTP ROM は除く)
- 端子選択か、EEPROM または I^2C/SMBus ターゲット インターフェイスを使用したアプリケーション機能選択
- 128 ビットの UUID (Universally Unique Identifier) を提供
- USB 2.0 上流ポート経由でオンボードおよびイン システムの OTP/EEPROM プログラミングをサポート
- 単一クロック入力、24MHz の水晶振動子または発振器
- 特別なドライバ要件なし、USB スタックをサポートする任意のオペレーティング システムでシームレスに動作
- 48 ピン HTQFP パッケージ (PHP)

2 アプリケーション

- 車載用
- コンピュータ システム
- ドッキング・ステーション
- モニタ
- セットトップ ボックス

3 概要

TUSB4020BI-Q1 は、2 ポートの USB 2.0 ハブです。上流ポートでハイ スピード / フル スピード USB 接続を、2 つの下流ポートでハイ スピード、フル スピード、ロー スピード USB 接続を提供します。上流のポートが、ハイ スピードおよびフル スピード / ロー スピードの接続をサポートする電気的環境に接続されている場合、下流のポートでハイ スピードおよびフル スピード/ロー スピード USB 接続が有効になります。上流のポートが、フル スピード / ロー スピード接続のみをサポートする電気的環境に接続されている場合、下流のポートでハイ スピード接続が無効になります。

TUSB4020BI-Q1 には、ポートごと、または一括の電力スイッチングと過電流保護が搭載されています。

ポート パワー個別制御のハブは、各下流ポートへの給電を USB ホストのリクエストに応じてオン/オフします。また、ポート パワー個別制御のハブが過電流イベントを検出した場合には、影響を受ける下流ポートへの電力だけがオフになります。

一括制御のハブは、いずれかのポートで電力が必要になると、すべての下流ポートへの給電をオンにします。下流ポートへの給電は、すべてのポートが給電を停止できる状態にならない限り、オフになりません。また、一括制御のハブが過電流イベントを検出すると、すべての下流ポートへの給電がオフになります。

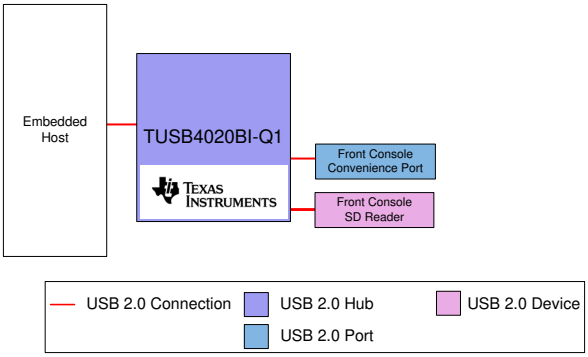
TUSB4020BI-Q1 は、バッテリ充電のサポートなどいくつかの機能について端子ストラップ構成を提供しており、OTP ROM、I^2C EEPROM、または PID、VID、およびカスタム ポートと PHY 構成用の I^2C/SMBus ターゲット インターフェイスにより、カスタマイズを行えます。また、I^2C EEPROM または I^2C/SMBus ターゲット インターフェイスを使用する場合、カスタム ストリングをサポートします。

このデバイスは 48 ピンの HTQFP パッケージで供給され、産業用温度範囲の -40℃～85℃で動作するよう設計されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TUSB4020BI-Q1	PHP (HTQFP、48)	9mm × 9mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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4 Pin Configuration and Functions

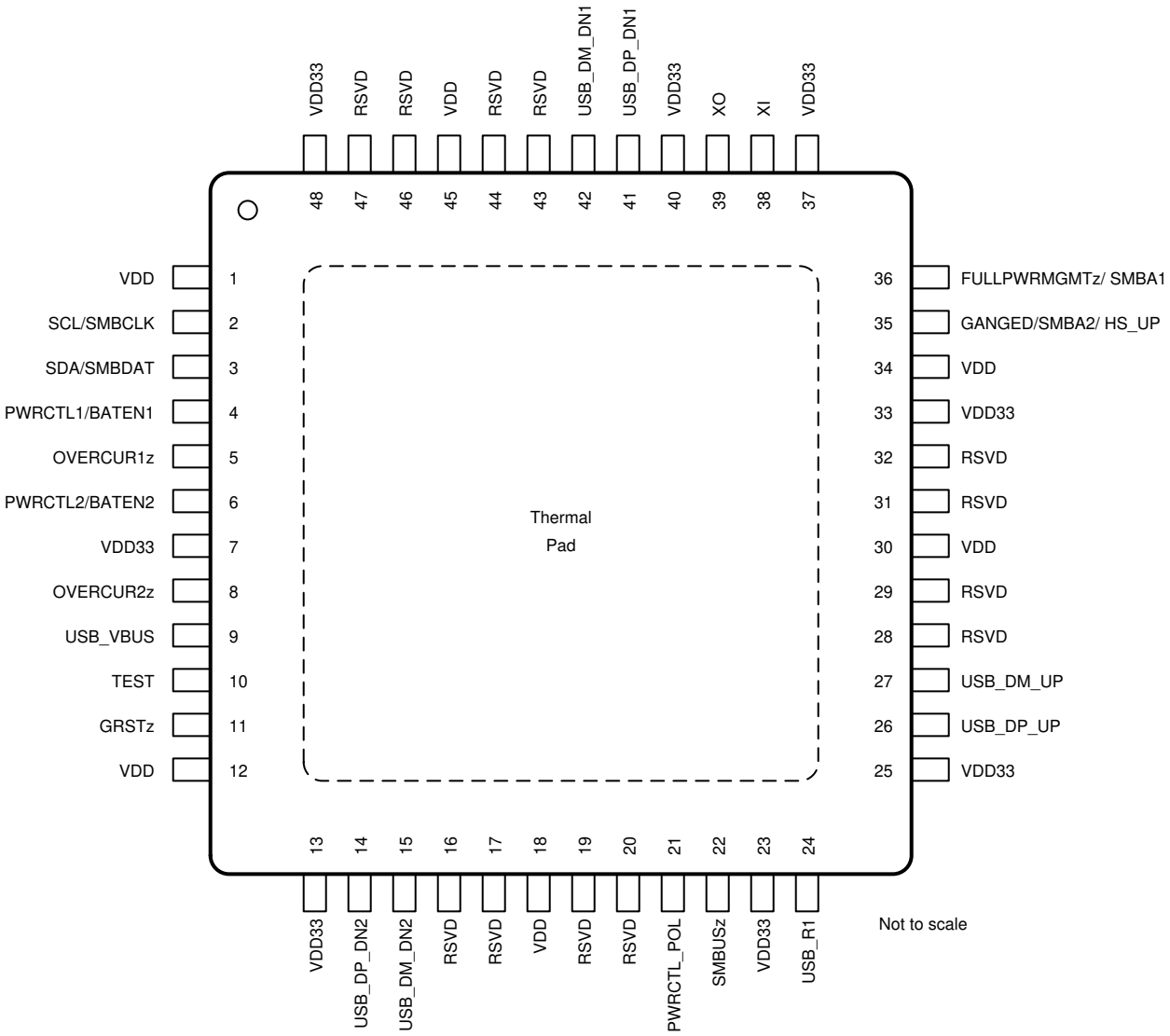


図 4-1. PHP Package, 48-Pin HTQFP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLOCK AND RESET SIGNALS			
GRSTz	11	I PU	Global power reset. This reset brings all of the TUSB4020BI-Q1 internal registers back to the default state. When GRSTz is asserted, the device is completely nonfunctional.
XI	38	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input can alternately be driven by the output of an external oscillator.
XO	39	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin can be left unconnected.
USB UPSTREAM SIGNALS			
USB_DP_UP	26	I/O	USB high-speed differential transceiver (positive)
USB_DM_UP	27	I/O	USB high-speed differential transceiver (negative)
USB_R1	24	I	Precision resistor reference. Connect a 9.53kΩ ±1% resistor between USB_R1 and GND.

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
USB_VBUS	9	I	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9kΩ ±1% resistor and to ground through a 10kΩ ±1% resistor from the signal to ground.
USB DOWNSTREAM SIGNALS			
USB_DP_DN1	41	I/O	USB high-speed differential transceiver (positive) downstream port 1.
USB_DM_DN1	42	I/O	USB high-speed differential transceiver (negative) downstream port 1.
PWRCTL1/BATEN1	4	I/O PD	USB port 1 power-on control for downstream power or battery charging enable. The terminal is used for control of the downstream power switch for Port 1. In addition, the value of the terminal is sampled at the deassertion of reset to determine the value of the battery charging support for Port 1 as indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR1z	5	I PU	USB DS port 1 overcurrent detection input. This terminal is used to connect the overcurrent output of the downstream port power switch for port 1. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred If power management is enabled, review the power switch to determine the required external circuitry. In ganged mode, either OVERCUR1z or OVERCUR2z can be used. In ganged mode, the overcurrent is reported as a hub event instead of a port event.
USB_DP_DN2	14	I/O	USB high-speed differential transceiver (positive) downstream port 2.
USB_DM_DN2	15	I/O	USB high-speed differential transceiver (negative) downstream port 2.
PWRCTL2/BATEN2	6	I/O PD	Power-on control /battery charging enable for downstream port 2. This terminal is used for control of the downstream power switch for port 2. The value of the terminal is sampled at the deassertion of reset to determine the value of the battery charging support for port 2 as indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR2z	8	I PU	Overcurrent detection for downstream port 2. This terminal is used to connect the over current output of the downstream port power switch for port 2. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred If power management is enabled, review the power switch to determine the required external circuitry. In ganged mode either OVERCUR1z or OVERCUR2z can be used. In ganged mode the overcurrent is reported as a hub event instead of a port event.
I^2C/SMBUS SIGNALS			
SCL/SMBCLK	2	I/O PD	I^2C clock/SMBus clock. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial clock interface for an I^2C EEPROM. When SMBUSz = 0, this terminal acts as the serial clock interface for an SMBus host. This pin must be pulled up to use the OTP ROM. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	3	I/O PD	I^2C data/SMBus data. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial data interface for an I^2C EEPROM. When SMBUSz = 0, this terminal acts as the serial data interface for an SMBus host. This pin must be pulled up to use the OTP ROM. Can be left unconnected if external interface not implemented.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
TEST AND MISCELLANEOUS SIGNALS			
SMBUSz	22	I PU	SMBUS mode. The value of the terminal is sampled at the deassertion of reset to enable I^2C or SMBus mode. 0 = SMBus mode selected 1 = I^2C mode selected After reset, this signal is driven low by the TUSB4020BI-Q1. Due to this behavior, TI recommends to not tie directly to supply but instead pull up or pull down using external resistor.
PWRCTL_POL	21	I/O PD	Power control polarity. The value of the terminal is sampled at the deassertion of reset to set the polarity of PWRCTL[2:1]. 0 = PWRCTL polarity is active high. 1 = PWRCTL polarity is active low. After reset, this signal is driven low by the TUSB4020BI-Q1. Due to this behavior, TI recommends to not tie directly to supply but instead pull up or pull down using external resistor.
GANGED/SMBA2/ HS_UP	35	I PU	Ganged operation enable/SMBus address bit 2/ high-speed status for upstream port The value of the terminal is sampled at the deassertion of reset to set the power switch and over current detection mode as follows: 0 = Individual power control supported when power switching is enabled. 1 = Power control gangs supported when power switching is enabled. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus target address bit 2. SMBus target address bit 3 is always 1 for the TUSB4020BI-Q1. After reset, this signal indicates the high-speed USB connection status of the upstream port. A value of 1 indicates the upstream port is connected to a high-speed USB capable port. Note: individual power control must be enabled for battery charging applications.
FULLPWRMGMTz/ SMBA1	36	I, PU	Full power management enable/ SMBus Address bit 1. The value of the terminal is sampled at the deassertion of reset to set the power switch control follows: 0 = Power switching supported 1 = Power switching not supported Full power management is the ability to control power to the downstream ports of the TUSB4020BI-Q1 using PWRCTL[2:1]/BATEN[2:1]. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus target address bit 1. SMBus target address bit 3 is always 1 for the TUSB4020BI-Q1. Can be left unconnected if full power management and SMBus are not implemented. After reset, this signal is driven low by the TUSB4020BI-Q1. Due to this behavior, TI recommends to not tie directly to supply but instead pull up or pull down using external resistor. Note: power switching must be supported for battery charging applications.
RSVD	16, 17, 19, 20, 28, 29, 31, 32, 43, 44, 46, 47	I/O	Reserved. These pins are for internal use only and must be left unconnected on PCB.
TEST	10	I PD	TEST mode enable. When this terminal is asserted high at reset enables test mode. This terminal is reserved for factory use. TI recommends to pull down this terminal to ground.
POWER AND GROUND SIGNALS			
VDD	1, 12, 18, 30, 34, 45	PWR	1.1V power rail
VDD33	7, 13, 23, 25, 33, 37, 40, 48	PWR	3.3V power rail
GND	PAD	—	Ground

(1) I = input, O = output, I/O = input/output, PU = internal pullup resistor, PD = internal pulldown resistor, and PWR = power signal

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	V_{DD} Steady-state supply voltage	–0.3	1.4	V
	V_{DD33} Steady-state supply voltage	–0.3	3.8	V
Voltage	USB_VBUS pin	–0.3	1.4	V
	XI and XO pins	–0.4	2.45	V
	All other pins	–0.3	3.8	V
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) per AEC Q100-002(1)		±4000	V
		Charged device model (CDM) per AEQ Q100-011	Corner pins	±1000	
			Other pins	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD(1)	1.1V supply voltage	0.99	1.1	1.26	V
VDD33	3.3V supply voltage	3	3.3	3.6	V
USB_VBUS	Voltage at USB_VBUS pin	0		1.155	V
XI, XO	Voltage at XI and XO pin	–0.35		1.98	V
T_A	Operating free-air temperature range	–40	25	85	°C
T_J	Operating junction temperature range	–40	25	105	°C

(1) A 1.05V, 1.1V, or 1.2V supply can be used as long as minimum and maximum supply conditions are met.

5.4 Thermal Information

THERMAL METRIC(1)		TUSB4020BI-Q1 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta\ JA}$	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{\theta\ JC(top)}$	Junction-to-case (top) thermal resistance	16.1	°C/W
$R_{\theta\ JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.9	°C/W
$R_{\theta\ JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 3.3V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage(1)	VDD33		2		VDD33	V
V_{IL}	Low-level input voltage(1)	VDD33		0		0.8	V
V_I	Input voltage			0		VDD33	V
V_O	Output voltage(2)			0		VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0		25	ns
V_{hys}	Input hysteresis(3)					0.13 × VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = –4mA	2.4			V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4mA			0.4	V
I_{OZ}	High-impedance, output current(2)	VDD33	V_I = 0 to VDD33			±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	VDD33	V_I = 0 to VDD33			±225	µA
I_I	Input current(5)	VDD33	V_I = 0 to VDD33			±15	µA

(1) Applies to external inputs and bidirectional buffers
(2) Applies to external outputs and bidirectional buffers
(3) Applies to GRSTz
(4) Applies to pins with internal pullups/pulldowns
(5) Applies to external input buffers

5.6 Hub Input Supply Current

typical values measured at T_A = 25°C

PARAMETER	VDD33	VDD11	UNIT
	3.3V	1.1V	
LOW-POWER MODES			
Power-on (after reset)	5	39	mA
Disconnect from host	5	39	mA
Suspend	5	39	mA
ACTIVE MODES (US STATE / DS STATE)			
2.0 host / 1 HS device active	48	71	mA
2.0 host / 2 HS devices active	60	80	mA

5.7 Power-Up Timing Requirements

		MIN	NOM	MAX	UNIT
t_{d1}	VDD33 stable before VDD stable(1)	see (2)			ms
t_{d2}	VDD and VDD33 stable before deassertion of GRSTz	3			ms
t_{su_io}	Setup for MISC inputs(3) sampled at the deassertion of GRSTz	0.1			µs
t_{hd_io}	Hold for MISC inputs(3) sampled at the deassertion of GRSTz.	0.1			µs
t_{VDD33_RAMP}	VDD33 supply ramp requirements	0.2		100	ms
t_{VDD_RAMP}	VDD supply ramp requirements	0.2		100	ms

(1) An active reset is required if the VDD33 supply is stable before the VDD11 supply. This active Reset shall meet the 3ms power-up delay counting from both power supplies being stable to the deassertion of GRSTz.
(2) There is no power-on relationship between VDD33 and VDD unless GRSTz is only connected to a capacitor to GND. Then VDD must be stable minimum of 10 µs before the VDD33.
(3) MISC pins sampled at deassertion of GRSTz: FULLPWRMGMTz, GANGED, PWRCTL_POL, SMBUSz, BATEN[4:1], and AUTOENz.

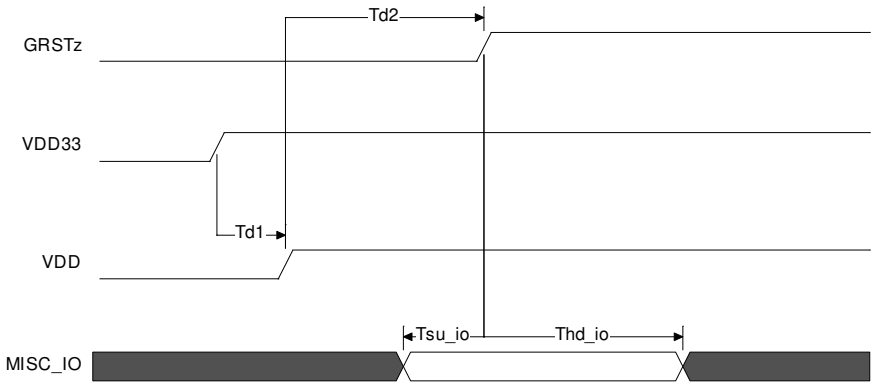


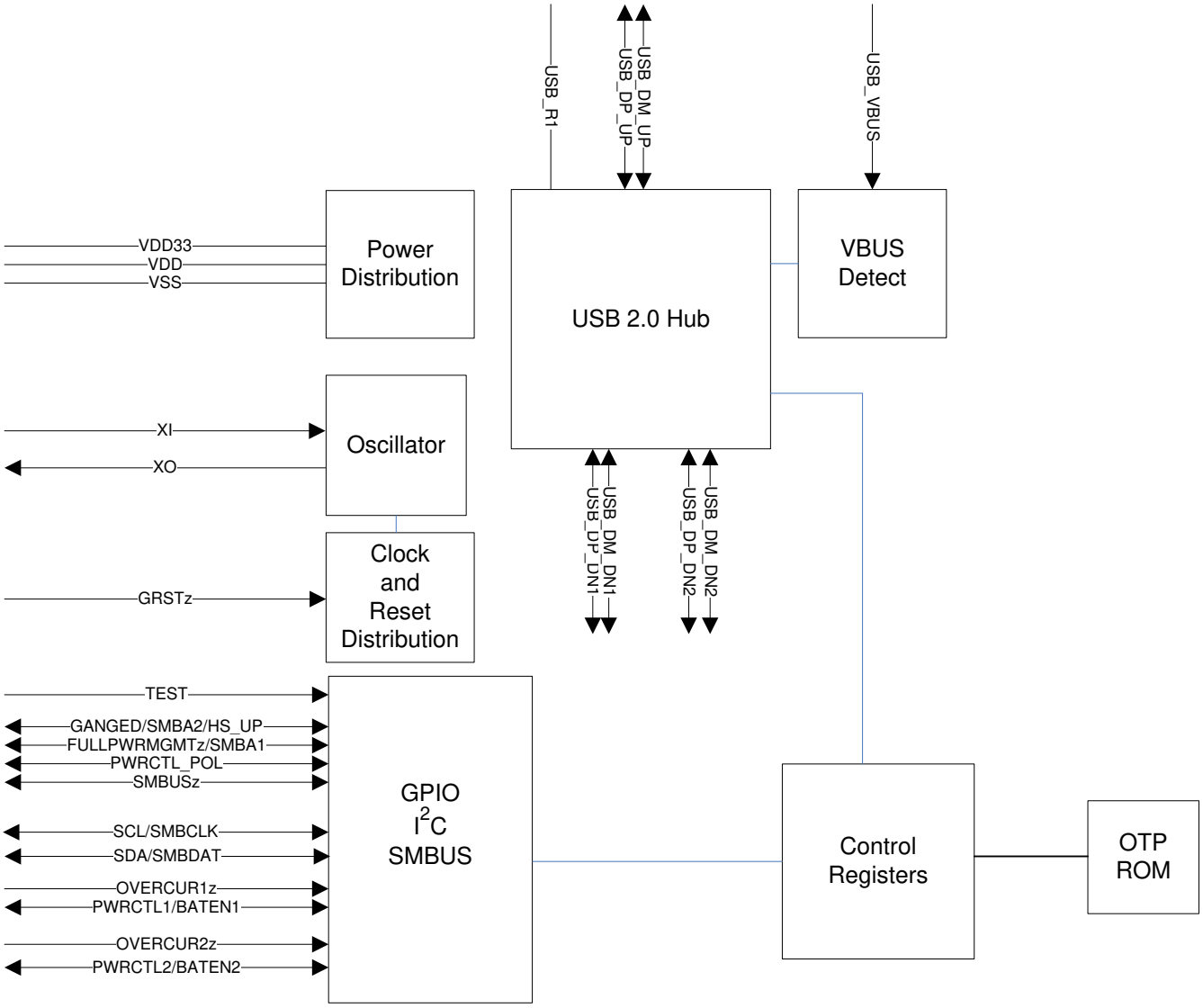
図 5-1. Power-Up Timing Requirements

6 Detailed Description

6.1 Overview

The TUSB4020BI-Q1 is a two-port USB 2.0 hub, which provides USB high-speed/full-speed connections on the upstream port and USB high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that supports high-speed and full-speed/low-speed connections, USB high-speed and full-speed/low-speed connectivity is enabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, USB high-speed connectivity are disabled on the downstream ports.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Battery Charging Features

The TUSB4020BI-Q1 provides support for battery charging. Battery charging support can be enabled on a per port basis through the REG_6h(batEn[1:0]).

Battery charging support includes both charging downstream port (CDP) and dedicated charging port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

In addition to standard DCP mode, the TUSB4020BI-Q1 provides a mode (AUTOMODE) which automatically provides support for DCP devices and devices that support custom charging indication. AUTOMODE is disabled by default. When in AUTOMODE, the port automatically switches between a divider mode and the DCP mode depending on the portable device connected. The divider mode places a fixed DC voltage on the ports DP and DM signals which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 5 W. The divider mode can be configured to report a high-current setting (up to 10 W) through REG_Ah(HiCurAcpModeEn). When AUTOMODE is enabled through REG_Ah(autoModeEnz), the CDP mode is not functional. CDP mode can not be used when AUTOMODE is enabled.

The battery charging mode for each port depends on the state of Reg_6h(batEn[n]), the status of the VBUS input, and the state of REG_Ah(autoModeEnz) upstream port, as identified in 表 6-1. Battery charging can also be enabled through the PWRCTL1/BATEN1 and PWRCTL2/BATEN2 pins.

表 6-1. TUSB4020BI-Q1 Battery Charging Modes

batEn[n]	VBUS	autoModeEnz	BC Mode Port x (x = n + 1)
0	Do not care	Do not care	Do not care
1	<4V	0	Automode(3) (4)
		1	DCP(1) (2)
	>4V	1	CDP(1)

(1) USB device is USB Battery Charging Specification Revision 1.2 Compliant
(2) USB device is Chinese Telecommunications Industry Standard YD/T 1591-2009
(3) Auto-mode automatically selects divider-mode or DCP mode.
(4) Divider mode can be configured for high-current mode through register or OTP settings.

6.3.2 USB Power Management

The TUSB4020BI-Q1 can be configured for power switched applications using either per-port or ganged power-enable controls and overcurrent status inputs.

Power switch support is enabled by REG_5h(fullPwrMgmtz) and the per-port or ganged mode is configured by REG_5h(ganged). The power switch can also be enabled through the FULLPWRMGMTz pin. Also ganged or individual control can be controlled by the GANGED pin.

The TUSB4020BI-Q1 supports both active-high and active-low power-enable controls. The PWRCTL[2:1] polarity is configured by REG_Ah(pwrctlPol). The polarity can also be configured by the PWRCTL_POL pin.

6.3.3 Clock Generation

The TUSB4020BI-Q1 accepts a crystal input to drive an internal oscillator or an external clock source. Keep the XI and XO traces as short as possible and away from any switching leads to minimize noise coupling.

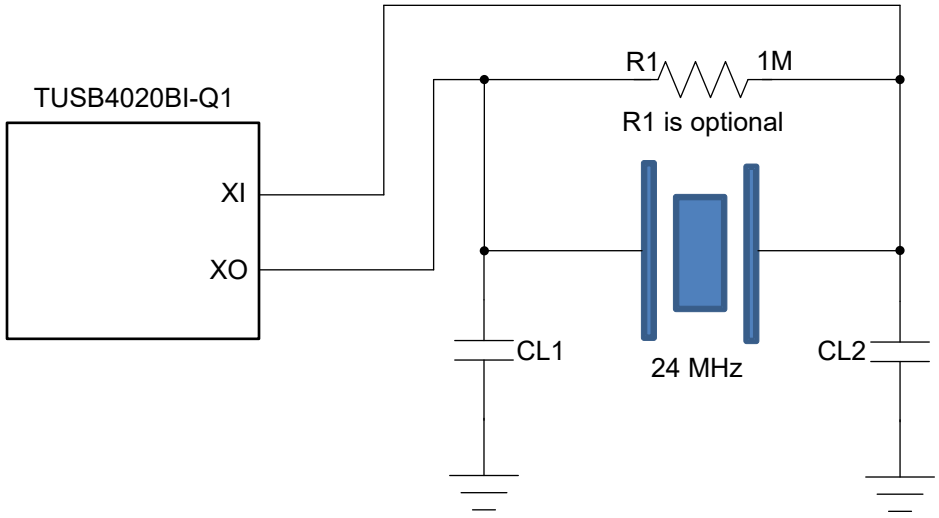


図 6-1. TUSB4020BI-Q1 Clock

6.3.4 Power-Up and Reset

The TUSB4020BI-Q1 does not have specific power sequencing requirements with respect to the VDD or VDD33 power rails. The VDD or VDD33 power rails can be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered-up must be limited to 100 hours over the projected lifetime of the device.
- Bus contention while VDD33 is powered-down can violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. A supply bus is powered down when the supply is below that range, either stable or in transition.

A minimum reset duration of 3ms is required, which is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

6.4 Device Functional Modes

6.4.1 External Configuration Interface

The TUSB4020BI-Q1 supports a serial interface for configuration register access. The device can be configured by an attached I^2C EEPROM or accessed as a target by a SMBus-capable host controller. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT terminals are pulled up to 3.3V at the deassertion of reset. The mode, I^2C controller, or SMBus target is determined by the state of SMBUSz terminal at reset.

6.5 Programming

6.5.1 One-Time Programmable (OTP) Configuration

The TUSB4020BI-Q1 allows device configuration through OTP non-volatile memory (OTP). The programming of the OTP is supported using vendor-defined USB device requests. For details using the OTP features, contact a TI representative.

表 6-2 provides a list features which can be configured using the OTP. The bit field section in 表 6-2 shows which features can be controlled by OTP ROM. The bits not listed in the table are not accessible by the OTP ROM.

表 6-2. OTP Configurable Features

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_01h	[7:0]	Vendor ID LSB
REG_02h	[7:0]	Vendor ID MSB
REG_03h	[7:0]	Product ID LSB
REG_04h	[7:0]	Product ID MSB
REG_07h	[0]	Port removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[1:0], that is: 1 = Not removable 0 = Removable
REG_07h	[1]	Port removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[1:0], that is: 1 = Not removable 0 = Removable
REG_0Ah	[1]	Automode enable
REG_0Ah	[4]	High-current divider mode enable.
REG_F2h	[3:1]	USB power switch power-on delay.

6.5.2 I^2C EEPROM Operation

The TUSB4020BI-Q1 supports a single-controller, standard mode (100kbps) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB4020BI-Q1 reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0.

If the value of the EEPROM contents at byte 00h equals 55h, the TUSB4020BI-Q1 loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB4020BI-Q1 exits the I^2C mode and continues execution with the default values in the configuration registers. The hub does not connect on the upstream port until the configuration is completed. If the TUSB4020BI-Q1 detects an unprogrammed EEPROM (value other than 55h), the device enters programming mode and a programming endpoint within the hub is enabled.

Note, the bytes located above offset Ah are optional. The requirement for data in those addresses depends on the options configured in the Device Configuration, Phy Custom Configuration, and Device Configuration 2 registers.

For details on I^2C operation, refer to the UM10204 I^2C-bus Specification and User Manual.

6.5.3 SMBus Target Operation

When the SMBus interface mode is enabled, the TUSB4020BI-Q1 supports read block and write block protocols as a target-only SMBus device.

The TUSB4020BI-Q1 target address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP terminal at reset
- y is the state of FULLPWRMGMTz/SMBA1 terminal at reset
- z is the read/write bit; 1 = read access, 0 = write access.

If the TUSB4020BI-Q1 is addressed by a host using an unsupported protocol, the device does not respond. The TUSB4020BI-Q1 waits indefinitely for configuration by the SMBus host and does not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements, refer to the System Management Bus Specification.

6.6 Register Maps

6.6.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be overwritten when the TUSB4020BI-Q1 is in I^2C or SMBus mode.

表 6-3. TUSB4020BI-Q1 Register Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	No
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved	Yes, program to 00h
0Ah	Device Configuration Register 2	Yes
0Bh to 0Fh	Reserved	
10h to 1Fh	UUID Byte [15:0]	No
20h to 21h	LangID Byte [1:0]	Yes, if customStrings is set
22h	Serial Number String Length	Yes, if customSerNum is set
23h	Manufacturer String Length	Yes, if customStrings is set
24h	Product String Length	Yes, if customStrings is set
25h to 2Fh	Reserved	Yes
30h to 4Fh	Serial Number String Byte [31:0]	Yes, if customSerNum is set
50h to 8Fh	Manufacturer String Byte [63:0]	Yes, if customStrings is set
90h to CFh	Product String Byte [63:0]	Yes, if customStrings is set
D0 to DFh	Reserved	No
F0h	Additional Feature Configuration Register	Yes
F1h	Reserved	Yes
F2h	Charging Port Control Register	Yes
F3 to F7h	Reserved	No
F8h	Device Status and Command Register	No
F9 to FFh	Reserved	No

6.6.1.1 ROM Signature Register (offset = 0h) [reset = 0h]

図 6-2. Register Offset 0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-4. ROM Signature Register

Bit	Field	Type	Reset	Description
7:0	romSignature	R/W	0h	ROM Signature Register. This register is used by the TUSB4020BI-Q1 in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB4020BI-Q1 aborts the EEPROM load and executes with the register defaults.

6.6.1.2 Vendor ID LSB Register (offset = 1h) [reset = 51h]

図 6-3. Register Offset 51h

7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-5. Vendor ID LSB Register

Bit	Field	Type	Reset	Description
7:0	vendorIdLsb	R/W	51h	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value can be overwritten to indicate a customer vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.

6.6.1.3 Vendor ID MSB Register (offset = 2h) [reset = 4h]

図 6-4. Register Offset 2h

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-6. Vendor ID MSB Register

Bit	Field	Type	Reset	Description
7:0	vendorIdMsb	R/W	4h	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value can be overwritten to indicate a customer vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.

6.6.1.4 Product ID LSB Register (offset = 3h) [reset = 25h]

図 6-5. Register Offset 3h

7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-7. Product ID LSB Register

Bit	Field	Type	Reset	Description
7:0	productIdLsb	R/W	25h	Product ID LSB. Least significant byte of the product ID assigned by TI. The default value of this register is 25h representing the LSB of the product ID assigned by TI. The value reported in the USB 2.0 device descriptor is the value of this register bit wise XORed with 00000010b. The value can be overwritten to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.

6.6.1.5 Product ID MSB Register (offset = 4h) [reset = 80h]

図 6-6. Register Offset 4h

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-8. Bit Descriptions – Product ID MSB Register

Bit	Field	Type	Reset	Description
7:0	productIdLsb	R/W	80h	Product ID MSB. Most significant byte of the product ID assigned by TI; the default value of this register is 80h representing the MSB of the product ID assigned by TI. The value can be overwritten to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register reflects the OTP ROM value.

6.6.1.6 Device Configuration Register (offset = 5h) [reset = 1Xh]

図 6-7. Register Offset 5h

7	6	5	4	3	2	1	0
0	0	0	1	X	X	0	0
R/W	R/W	R/W	R	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-9. Device Configuration Register

Bit	Field	Type	Reset	Description
7	customStrings	R/W	1Xh	Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers. 0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only. 1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers can be loaded by EEPROM or written by SMBus. The default value of this bit is 0.
6	customSernum	R/W	1Xh	Custom serial number enable. This bit controls the ability to write to the serial number registers. 0 = The Serial Number String Length and Serial Number String registers are read only. 1 = The Serial Number String Length and Serial Number String registers can be loaded by EEPROM or written by SMBus. The default value of this bit is 0.
5	RSVD	R/W	1Xh	Reserved. This bit is reserved.
4	RSVD	R	1Xh	Reserved. This bit is reserved and returns 1 when read.
3	ganged	R/W	1Xh	Ganged. This bit is loaded at the deassertion of reset with the value of the GANGED/SMBA2/HS_UP terminal. 0 = When fullPwrMgmtz = 0, each port is individually power switched and enabled by the PWRCTL[2:1]/BATEN[2:1] terminals 1 = When fullPwrMgmtz = 0, the power switch control for all ports is ganged and enabled by the PWRCTL1/BATEN1 terminal When the TUSB4020BI-Q1 is in I^2C mode, the TUSB4020BI-Q1 loads this bit from the contents of the EEPROM. When the TUSB4020BI-Q1 is in SMBUS mode, the value can be overwritten by an SMBus host.
2	fullPwrMgmtz	R/W	1Xh	Full Power Management. This bit is loaded at the deassertion of reset with the value of the FULLPWRMGMTz/SMBA1 terminal. 0 = Port power switching and over-current status reporting is enabled 1 = Port power switching and over-current status reporting is disabled When the TUSB4020BI-Q1 is in I^2C mode, the TUSB4020BI-Q1 loads this bit from the contents of the EEPROM. When the TUSB4020BI-Q1 is in SMBUS mode, the value can be overwritten by an SMBus host.
1	RSVD	R/W	1Xh	Reserved. This bit is reserved and must not be altered from the default.
0	RSVD	R	1Xh	Reserved. This field is reserved and returns 0 when read.

6.6.1.7 Battery Charging Support Register (offset = 6h) [reset = 0Xh]

図 6-8. Register Offset 6h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	X	X
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-10. Battery Charging Support Register

Bit	Field	Type	Reset	Description
7:2	RSVD	R	0Xh	Reserved. Read only, returns 0 when read.
1:0	batEn[1:0]	R/W	0Xh	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. 0 = The port is not enabled for battery charging support features 1 = The port is enabled for battery charging support features Each bit corresponds directly to a downstream port, that is batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2. The default value for these bits are loaded at the deassertion of reset with the value of PWRCTL/BATEN[1:0]. When in I2C/SMBus mode the bits in this field can be overwritten by EEPROM contents or by an SMBus host.

6.6.1.8 Device Removable Configuration Register (offset = 7h) [reset = 0Xh]

図 6-9. Register Offset 7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	X	X
R/W	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-11. Device Removable Configuration Register

Bit	Field	Type	Reset	Description
7	customRmbl	R/W	0Xh	Custom removable status. When this field is a 1, the TUSB4020BI-Q1 uses rmbl bits in this register to identify removable status for the ports.
6:2	RSVD	R	0Xh	Reserved. Read only, returns 0 when read. Bits 3:2 are RW. The bits are reserved and return 0 when read.
1:0	rmbl[1:0]	R/W	0Xh	Removable. The bits in this field indicate whether a device attached to downstream ports 2 through 1 are removable or permanently attached. 0 = The device attached to the port is not removable 1 = The device attached to the port is removable Each bit corresponds directly to a downstream port n + 1, that is rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, and so forth. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this filed reflects the inverted values of the OTP ROM non_rmb[1:0] field.

6.6.1.9 Port Used Configuration Register (offset = 8h) [reset = 0h]

図 6-10. Register Offset 8h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-12. Port Used Configuration Register

Bit	Field	Type	Reset	Description
7:0	RSVD	R	0h	Reserved. Read only.

6.6.1.10 PHY Custom Configuration Register (offset = 9h) [reset = 0h]

図 6-11. Register Offset 9h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R/W	R	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-13. PHY Custom Configuration Register

Bit	Field	Type	Reset	Description
7:6	RSVD	R	0h	Reserved. Read only, returns 0 when read.
5	RSVD	R/W	0h	Reserved. This bit is reserved and must not be altered from the default.
4:2	RSVD	R	0h	Reserved. Read only, returns 0 when read.
1:0	RSVD	R/W	0h	Reserved. This field is reserved and must not be altered from the default.

6.6.1.11 Device Configuration Register 2 (offset = Ah)

図 6-12. Register Offset Ah

7	6	5	4	3	2	1	0
0	0	X	0	0	0	0	0
R	RW	RW	RW	RW	RW	RW	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-14. Bit Descriptions – Device Configuration Register 2

Bit	Field Name	Access	Reset	Description
7	RSVD	RO		Reserved. Read only, returns 0 when read.
6	customBCfeatures	RW		Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls. 0 = The HiCurAcpModeEn and AutoModeEnz bits are read only and the values are loaded from the OTP ROM. 1 = The HiCurAcpModeEn and AutoModeEnz bits are read/write and can be loaded by EEPROM or written by SMBus. from this register. This bit can be written simultaneously with HiCurAcpModeEn and AutoModeEnz.
5	pwrctlPol	RW		Power enable polarity. This bit is loaded at the deassertion of reset with the inverse value of the PWRCTL_POL terminal. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high When the TUSB4020BI-Q1 is in I^2C mode, the TUSB4020BI-Q1 loads this bit from the contents of the EEPROM. When the TUSB4020BI-Q1 is in SMBUS mode, the value can be overwritten by an SMBus host.
4	HiCurAcpModeEn	RO/RW		High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. 0 = High current divider mode disabled 1 = High current divider mode enabled This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit.
3	RSVD	RW		Reserved
2	dsportEcrEn	RW		DSPort ECR enable. This bit enables full implementation of the DSPORT ECR (April 2013). 0 = DSPort ECR (April 2013) is enabled with the exception of changes related to the CCS bit is set upon entering U0, and changes related to avoiding or reporting compliance mode entry. 1 = The full DSport ECR (April 2013) is enabled.
1	autoModeEnz	RO/RW		Automatic Mode Enable. This bit is loaded from the OTP ROM. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions: 0 = Automatic mode battery charging features are enabled. Only battery charging DCP and custom BC (divider mode) is enabled. 1 = Automatic mode is disabled; only battery charging DCP and CDP mode is supported. Note: when the upstream port is connected, battery charging CDP mode is supported on all ports when this field is one. This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM AutoModeEnz bit.
0	RSVD	RO		Reserved. Read only, returns 0 when read.

6.6.1.12 UUID Registers (offset = 10h to 1Fh)

図 6-13. Register Offset 10h to 1Fh

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-15. Bit Descriptions – UUID Byte N Register

Bit	Field Name	Access	Reset	Description
7:0	uuidByte[n]	RO		UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

6.6.1.13 Language ID LSB Register (offset = 20h)

図 6-14. Register Offset 20h

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-16. Bit Descriptions – Language ID LSB Register

Bit	Field Name	Access	Reset	Description
7:0	langIdLsb	RW		Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB4020BI-Q1 only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host.

6.6.1.14 Language ID MSB Register (offset = 21h)

図 6-15. Register Offset 21h

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-17. Bit Descriptions – Language ID MSB Register

Bit	Field Name	Access	Reset	Description
7:0	langIdMsb	RO/RW		Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB4020BI-Q1 only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host.

6.6.1.15 Serial Number String Length Register (offset = 22h)

図 6-16. Register Offset 22h

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-18. Bit Descriptions – Serial Number String Length Register

Bit	Field Name	Access	Reset	Description
7:6	RSVD	RO		Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RO/RW		Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24-byte serial number string is supported. The maximum string length is 32 bytes. When customSernum is 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

6.6.1.16 Manufacturer String Length Register (offset = 23h)

図 6-17. Register Offset 23h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-19. Bit Descriptions – Manufacturer String Length Register

Bit	Field Name	Access	Reset	Description
7	RSVD	RO		Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RO/RW		Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

6.6.1.17 Product String Length Register (offset = 24h)

図 6-18. Register Offset 24h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-20. Bit Descriptions – Product String Length Register

Bit	Field Name	Access	Reset	Description
7	RSVD	RO		Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RO/RW		Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field can be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers.

6.6.1.18 Serial Number Registers (offset = 30h to 4Fh)

図 6-19. Register Offset 30h to 4Fh

7	6	5	4	3	2	1	0
X	X	x	x	x	x	x	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-21. Bit Descriptions – Serial Number Registers

Bit	Field Name	Access	Reset	Description
7:0	serialNumber[n]	RO/RW		Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is set by TI. When customSernum is 1, these registers can be overwritten by EEPROM contents or by an SMBus host.

6.6.1.19 Manufacturer String Registers (offset = 50h to 8Fh)

図 6-20. Register Offset 50h to 8Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-22. Bit Descriptions – Manufacturer String Registers

Bit	Field Name	Access	Reset	Description
7:0	mfgStringByte[n]	RO/RW		Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

6.6.1.20 Product String Registers (offset = 90h to CFh)

図 6-21. Register Offset 90h to CFh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-23. Bit Descriptions – Product String Byte N Register

Bit	Field Name	Access	Reset	Description
7:0	prodStringByte[n]	RW		Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

6.6.1.21 Additional Feature Configuration Register (offset = F0h)

図 6-22. Register Offset F0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-24. Bit Descriptions – Additional Feature Configuration Register

Bit	Field Name	Access	Reset	Description
7:1	RSVD	RO		Reserved. Read only, returns 0 when read.
0	RSVD	RW		Reserved This bit is loaded at the deassertion of reset with the value of the SCL/SMBCLK terminal.

6.6.1.22 Charging Port Control Register (offset = F2h)

図 6-23. Register Offset F2h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-25. Bit Descriptions – Charging Port Control Register

Bit	Field Name	Access	Reset	Description
7:4	RSVD	RO		Reserved. Read only, returns 0 when read.
3:1	pwronTime	RW		Power-On Delay Time. When dsportEcrEn is set, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from custom charging mode to Dedicated Charging Port Mode. The nominal timing is defined as follows: TPWRON_EN = (pwronTime + 1) × 200ms (1) These registers can be overwritten by EEPROM contents or by an SMBus host.
0	RSVD	RW		Reserved. This bit is reserved and must not be altered from the default.

6.6.1.23 Device Status and Command Register (offset = F8h)

図 6-24. Register Offset F8h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RSU	RCU

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

表 6-26. Bit Descriptions – Device Status and Command Register

Bit	Field Name	Access	Reset	Description
7:2	RSVD	R		Reserved. Read only, returns 0 when read.
1	smbusRst	RSU		SMBus interface reset. This bit loads the registers back to the GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	RCU		Configuration active. This bit indicates that configuration of the TUSB4020BI-Q1 is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB4020BI-Q1 does not connect on the upstream port while this bit is 1. When in the SMBus mode, this bit must be cleared by the SMBus host to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

7 Application and Implementation

注

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7.1 Application Information

The TUSB4020BI-Q1 is a two-port USB 2.0 hub, which provides USB high-speed/full-speed connections on the upstream port and USB high-speed, full-speed, or low-speed connections on the downstream port. The TUSB4020BI-Q1 can be used in any application that needs additional USB compliant ports. For example, a specific notebook can only have two downstream USB ports. By using the TUSB4020BI-Q1, the notebook can increase the downstream port count to three.

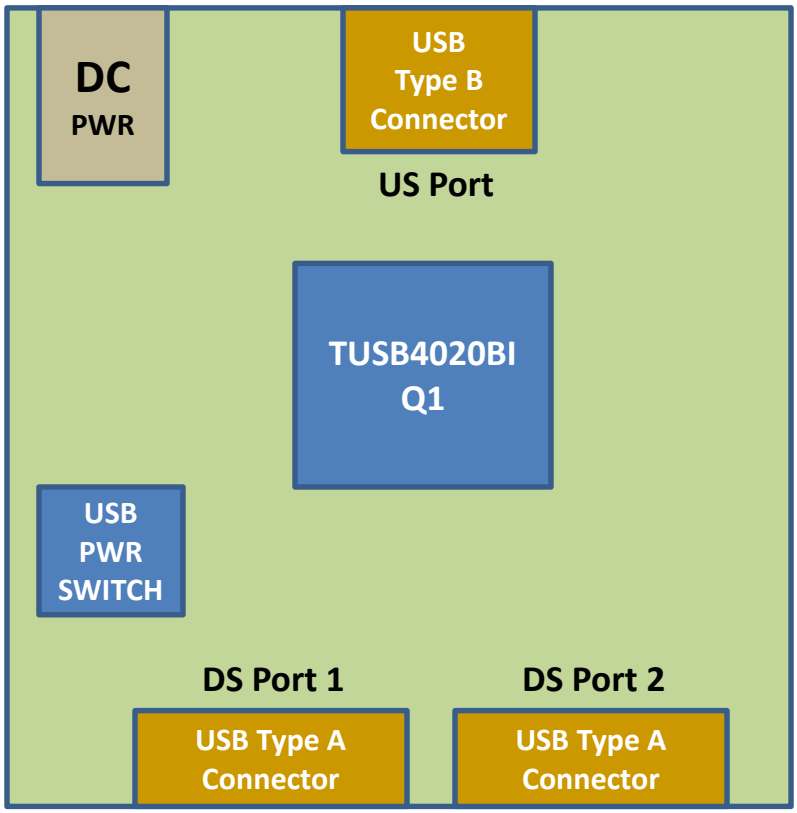

図 7-1. Discrete USB Hub Product

7.1.1 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12pF to 24pF and frequency stability rating of ±100PPM or better. To ensure proper start-up oscillation condition, TI recommends a maximum crystal equivalent series resistance (ESR) of 50Ω. Use a parallel load capacitor if a crystal source is used. The exact load capacitance value used depends on the crystal vendor. Refer to application note *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* for details on how to determine the load capacitance value.

7.1.2 Input Clock Requirements

When using an external clock source such as an oscillator, make sure the reference clock has a ±100PPM or better frequency stability and has less than 50ps absolute peak-to-peak jitter. Tie XI to the 1.8V clock source and leave the XO pin floating.

7.2 Typical Applications

A common application for the TUSB4020BI-Q1 is as a self-powered standalone USB hub product. The product is powered by an external 5V DC power adapter. In this application using a USB cable, TUSB4020BI-Q1 device's upstream port is plugged into a USB host controller. The downstream ports of the TUSB4020BI-Q1 are exposed to users for connecting USB hard drives, camera, flash drive, and so forth.

7.2.1 Upstream Port Implementation

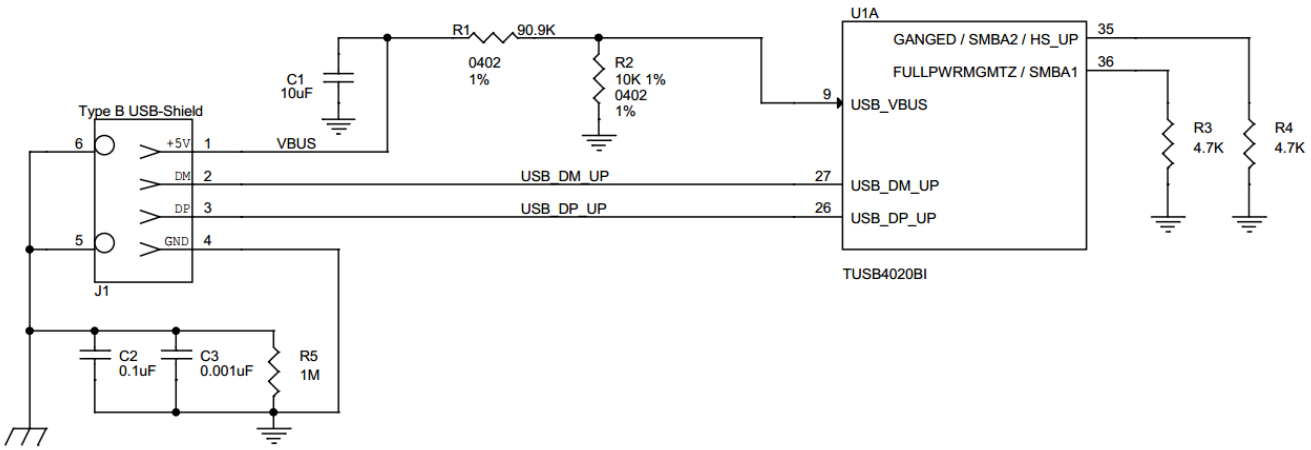

図 7-2. Upstream Port Implementation Schematic

7.2.1.1 Design Requirements

表 7-1. Input Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD supply	1.1V
VDD33 supply	3.3V
Upstream port USB support (HS, FS)	HS, FS
Downstream port 1 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 2 USB support (HS, FS, LS)	HS, FS, LS
Number of removable downstream ports	2
Number of non-removable downstream ports	0
Full power management of downstream ports	Yes (FULLPWRMGMTZ = 0)
Individual control of downstream port power switch	Yes (GANGED = 0)
Power switch enable polarity	Active high (PWRCTL_POL = 0)
Battery charge support for downstream port 1	Yes
Battery charge support for downstream port 2	Yes
I^2C EEPROM support	No
24MHz clock source	Crystal

7.2.1.2 Detailed Design Procedure

The upstream of the TUSB4020BI-Q1 is connected to a USB2 type B connector. This particular example has GANGED terminal and FULLPWRMGMTZ terminal pulled low, which results in individual power support each downstream port. The VBUS signal from the USB2 type B connector is fed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements.

7.2.1.3 Application Curves

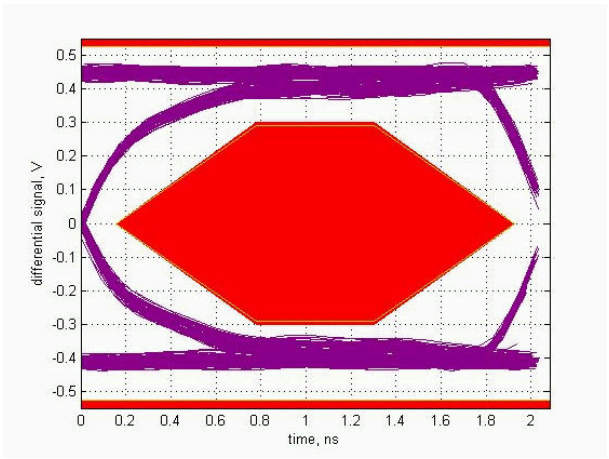

図 7-3. HighSpeed TX Eye for Downstream Port 1

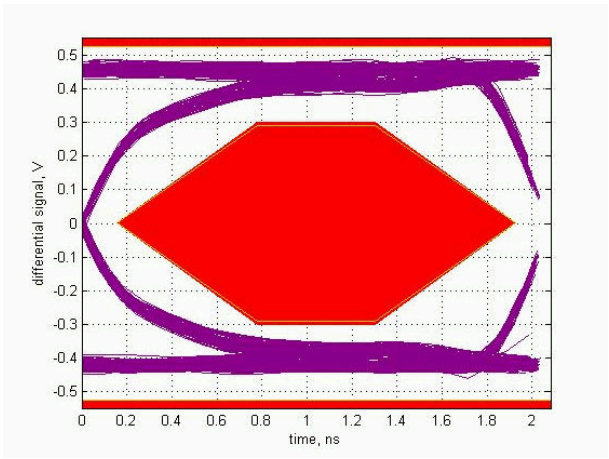

図 7-4. HighSpeed TX Eye for Downstream Port 2

7.2.2 Downstream Port 1 Implementation

The downstream port 1 of the TUSB4020BI-Q1 is connected to a USB2 type A connector. With BATEN1 terminal pulled up, battery charge support is enabled for port 1. If battery charge support is not needed, then uninstall the pullup resistor on BATEN1. The PWRCTL_POL is pulled-down, which results in active-high power enable (PWRCTL1 and PWRCTL2) for a USB VBUS power switch.

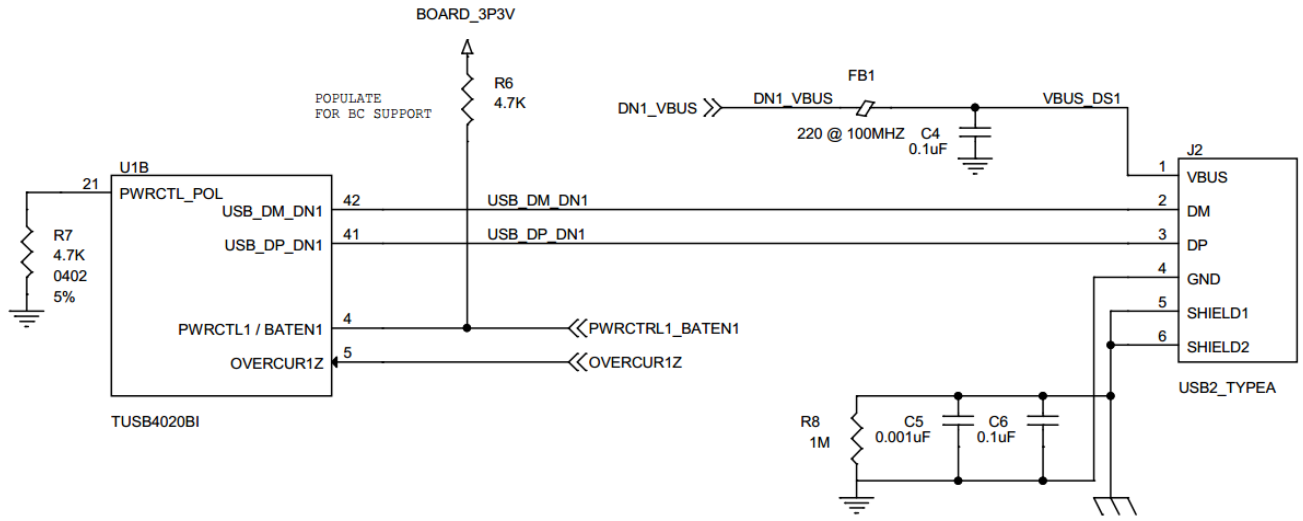

図 7-5. Downstream Port 1 Implementation Schematic

7.2.3 Downstream Port 2 Implementation

The downstream port 2 of the TUSB4020BI-Q1 is connected to a USB2 type A connector. With BATEN2 terminal pulled up, battery charge support is enabled for port 2. If battery charge support is not needed, then uninstall the pullup resistor on BATEN2.

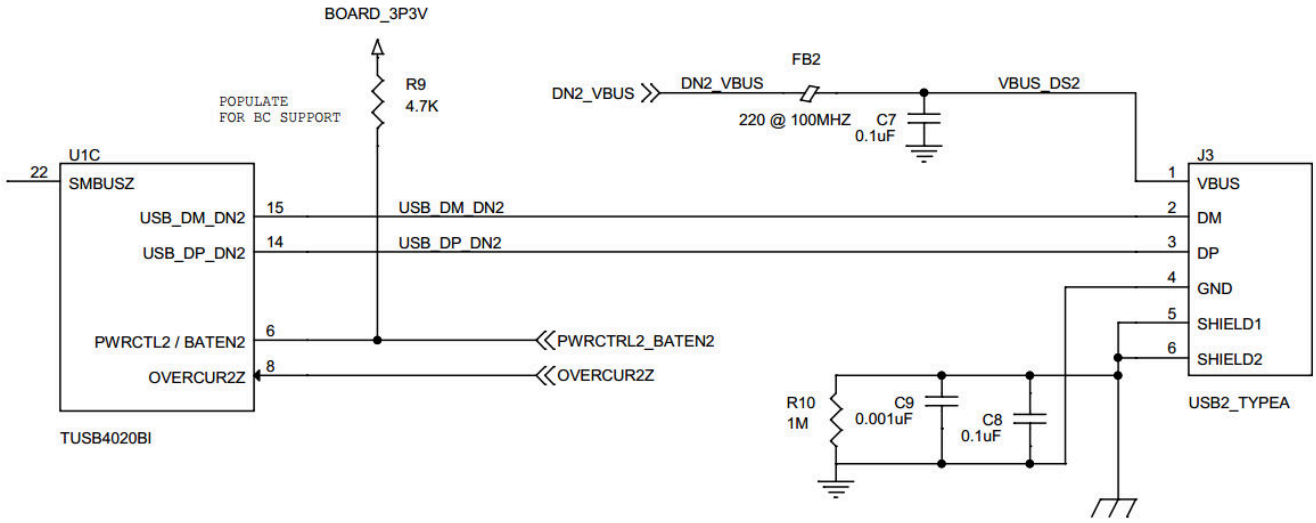

図 7-6. Downstream Port 2 Implementation Schematic

7.2.4 VBUS Power Switch Implementation

This particular example uses the TI TPS2561 dual-channel precision adjustable current-limited power switch. For details on this power switch or other power switches available from TI, refer to www.ti.com.

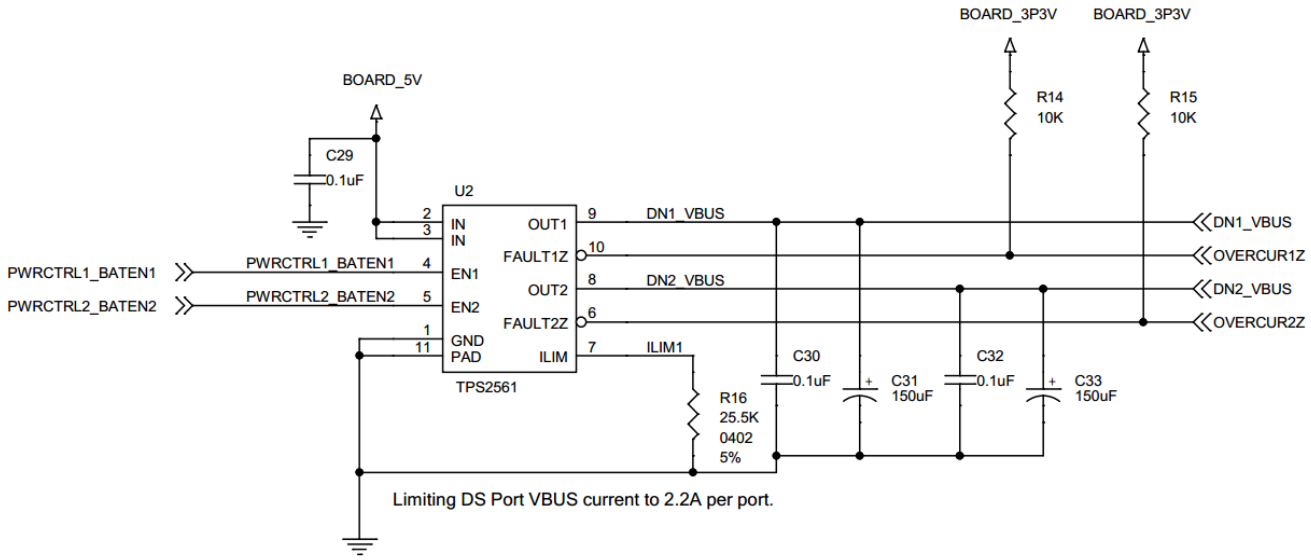

図 7-7. Power Switch Implementation Schematic

7.2.5 Clock, Reset, and Miscellaneous

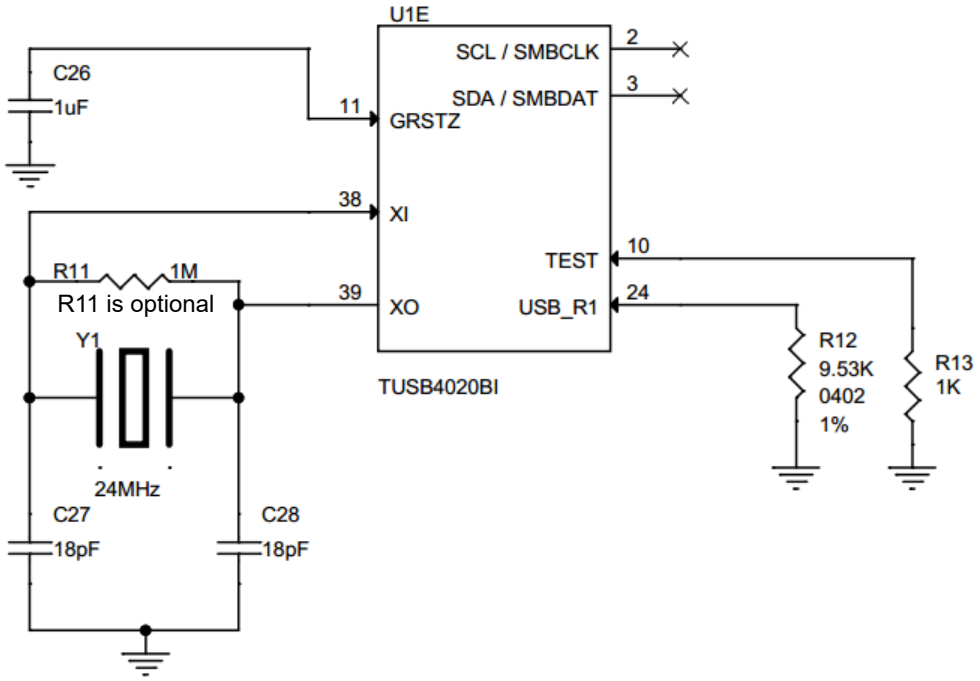

図 7-8. Clock, Reset, and Miscellaneous Schematic

7.2.6 Power Implementation

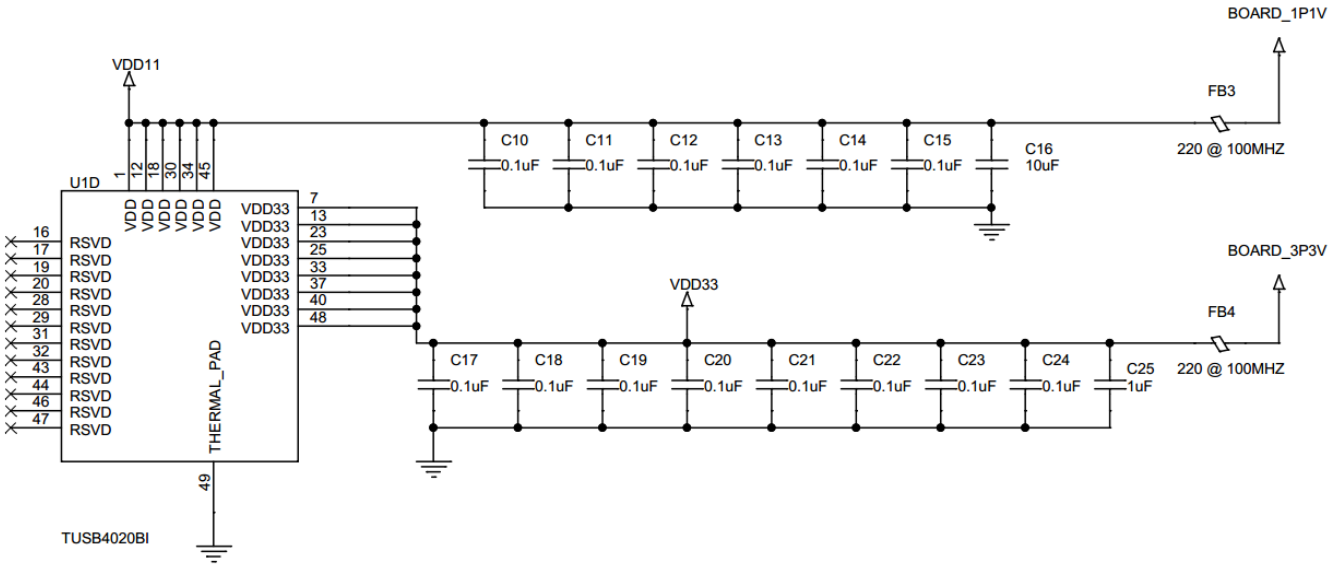

図 7-9. Power Implementation Schematic

8 Power Supply Recommendations

8.1 Power Supply

Implement V_{DD} and V_{DD33} as a single power plane.

- The V_{DD} terminals of the TUSB4020BI-Q1 supply 1.1V (nominal) power to the core of the TUSB4020BI-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the core voltage regulator can need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05Ω) can be selected.
- The V_{DD33} terminals of the TUSB4020BI-Q1 supply 3.3V power rail to the I/O of the TUSB4020BI-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10µF capacitor or 1µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. Place the smaller decoupling capacitors as close to the TUSB4020BI-Q1 power pins as possible with an optimal grouping of two of differing values per pin.

8.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5V and at least 500mA per port. Downstream port power switches can be controlled by the TUSB4020BI-Q1 signals. It is possible to leave the downstream port power always enabled.
- Each downstream port's VBUS requires a large bulk low-ESR capacitor of 22µF or larger to limit in-rush current.
- TI recommends ferrite beads on the VBUS pins of the downstream USB port connections for both ESD and EMI reasons. A 0.1µF capacitor on the USB connector side of the ferrite provides a low-impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

8.3 Ground

TI recommends to use only one board ground plane in the design. This provides the best image plane for signal traces running above the plane. Connect the thermal pad of the TUSB4020BI-Q1 and any of the voltage regulators to this plane with vias. An earth or chassis ground is only implemented near the USB port connectors on a different plane for EMI and ESD purposes.

9 Layout

9.1 Layout Guidelines

9.1.1 Placement

1. Place a 9.53kΩ ±1% resistor connected to terminal USB_R1 as close as possible to the TUSB4020BI-Q1.
2. Place a 0.1µF capacitor as close as possible on each V_{DD} and V_{DD33} power pin.
3. Place the ESD and EMI protection devices (if used) as close as possible to the USB connector.
4. If a crystal is used, place the crystal as close as possible to the TUSB4020BI-Q1 device's XI and XO terminals.
5. Place voltage regulators as far away as possible from the TUSB4020BI-Q1, crystal, and differential pairs.
6. In general, place the large bulk capacitors associated with each power as close as close as possible to the voltage regulators.

9.1.2 Package Specific

1. The TUSB4020BI-Q1 package has a 0.5mm pin pitch.
2. The TUSB4020BI-Q1 package has a 3.6mm × 3.6mm thermal pad. This thermal pad must be connected to ground through a system of vias.
3. Make sure that all vias under the device, except for those connected to thermal pad, are solder masked to avoid potential issues with thermal pad layouts.

9.1.3 Differential Pairs

This section describes the layout recommendations for all of the TUSB4020BI-Q1 differential pairs: USB_DP_XX, USB_DM_XX.

- Must be designed with a differential impedance of 90 Ω ±10%.
- To minimize crosstalk, TI recommends to keep high-speed signals away from each other. Separate each pair by at least 5× the signal trace width. Separating with ground as depicted in the layout example also helps minimize crosstalk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points causes impedance discontinuity, and therefore, negatively impacts signal performance. If test points are used, place the test points in series and symmetrically. The test points must not be placed in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. Keep the use of bends in differential traces to a minimum. When bends are used, make sure the number of left and right bends are as equal as possible and that the angle of the bend is ≥135°. Take this action to minimize any length mismatch caused by the bends, and therefore, minimize the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. Eight inches is the maximum recommended trace length for USB 2.0 differential-pair signals. Longer trace lengths require very careful routing to assure proper signal integrity.
- Match the etch lengths of the differential pair traces (that is DP and DM). Make sure the USB 2.0 differential pairs do not exceed 50mil relative trace length difference.
- Minimize the use of vias in the differential-pair paths as much as possible. If this is not practical, ensure that the same via type and placement are used for both signals in a pair. Place any vias used as close as possible to the TUSB4020BI-Q1 device.
- Do not place power fuses across the differential-pair traces.

9.2 Layout Example

図 9-1 shows an example layout of the upstream port to a USB3 Type B connector. The routing to a USB2 Type B connector is similar.

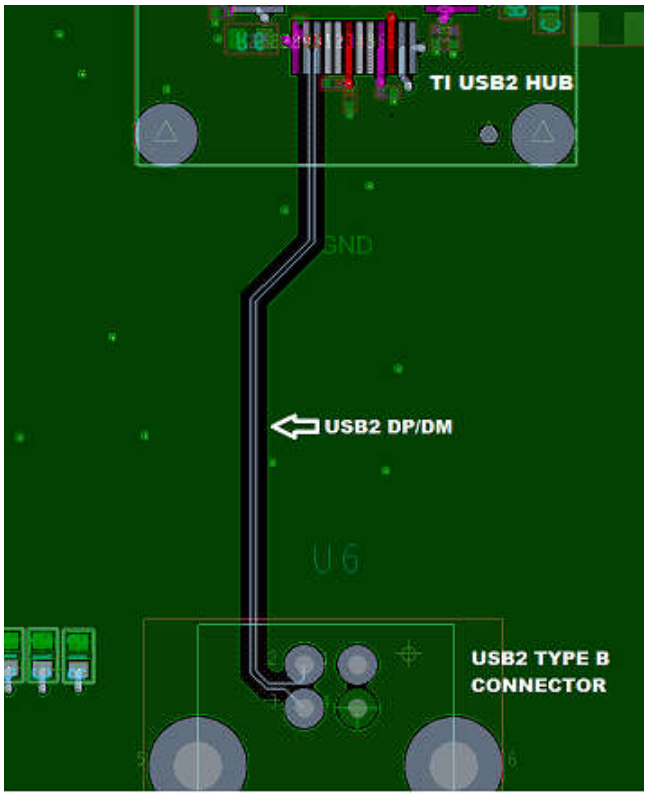

図 9-1. Upstream Port

図 9-2 shows an example layout of the Downstream Port to a USB3 Type A connector. The routing to a USB2 Type A connector is similar.

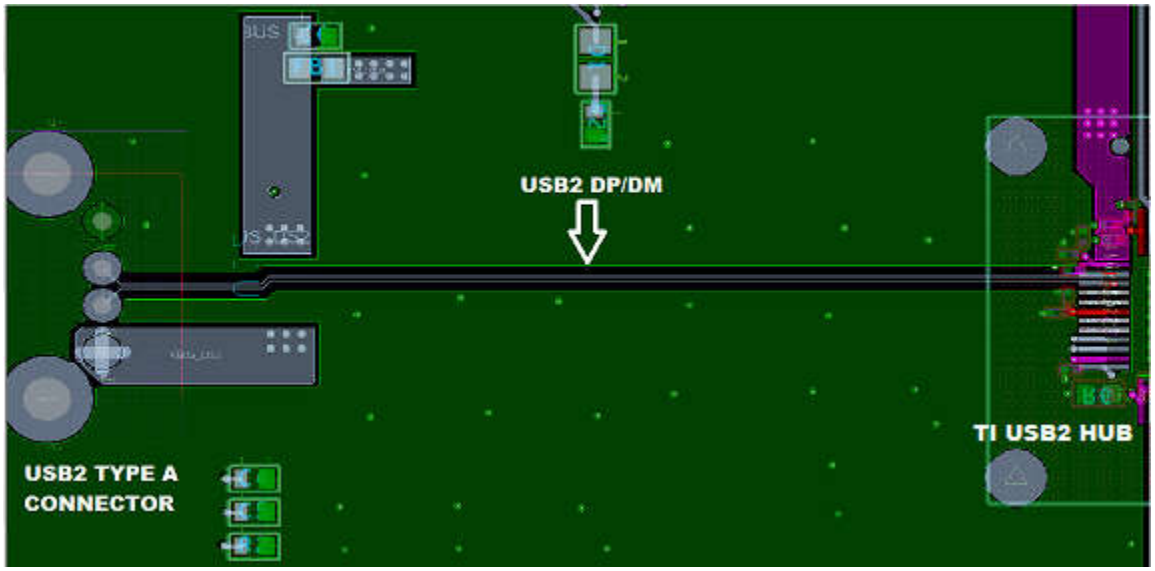

図 9-2. Downstream Port

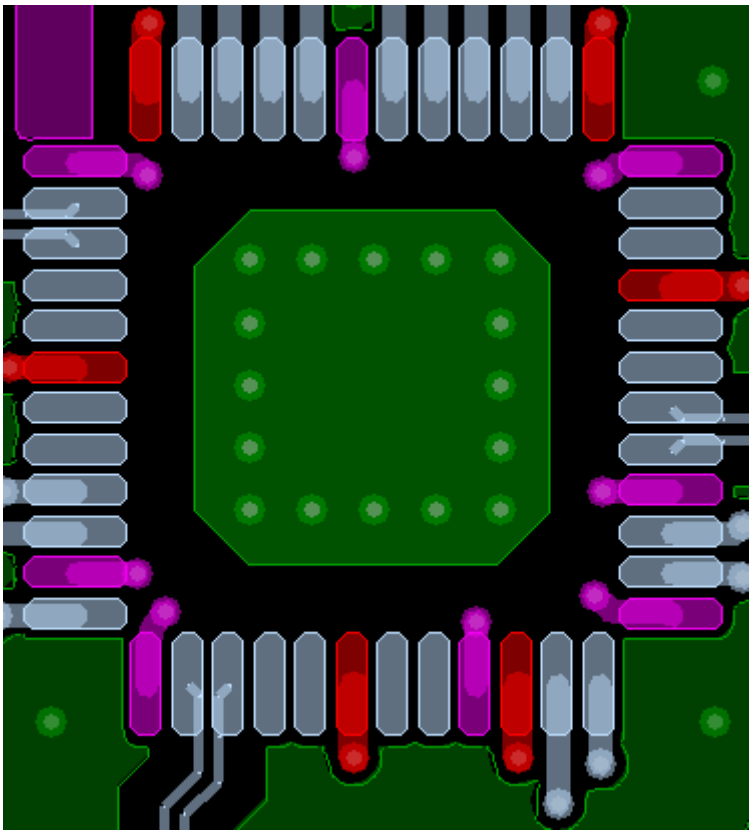

図 9-3. Thermal Pad

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* application note
- Texas Instruments, *TPS256x Dual Channel Precision Adjustable Current-limited Power Switches* data sheet

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.6 用語集

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11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2021) to Revision C (July 2024)	Page
• 包括的な用語を使ってデータシートを更新。	1
• Added voltage parameters to the *Absolute Maximum Ratings* table	7
• Added maximum junction temperature to the *Absolute Maximum Ratings* table	7
• Added the XI, XO voltage to the *Recommended Operating Conditions* table	7

Changes from Revision A (February 2021) to Revision B (December 2021)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 4、11、12、31 ページの水晶振動子についての 1M 帰還抵抗の要件を削除	1
• Corrected the default register setting for the *Register offset 9h*	19

Changes from Revision * (July 2015) to Revision A (February 2021) **Page**

- AEQ-Q100 デバイス温度グレード 3 の項目を特長リストに追加 1
- From: SMBus target address bits 2 and 3 are always 1 for TUSB4020BI-Q1 To: SMBus target address bit 3 is always 1 for TUSB4020BI-Q1 4

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB4020BIPHPQ1	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T4020BIQ1
TUSB4020BIPHPQ1.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T4020BIQ1
TUSB4020BIPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T4020BIQ1
TUSB4020BIPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T4020BIQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TUSB4020BI-Q1 :

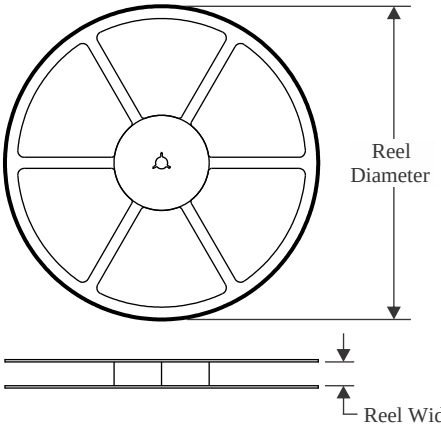
- Catalog : TUSB4020BI

NOTE: Qualified Version Definitions:

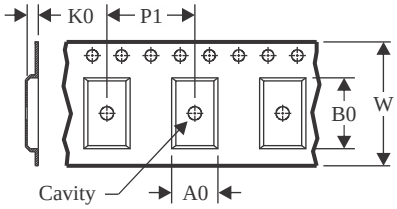
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

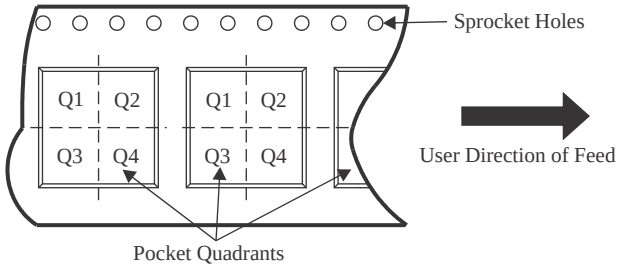


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

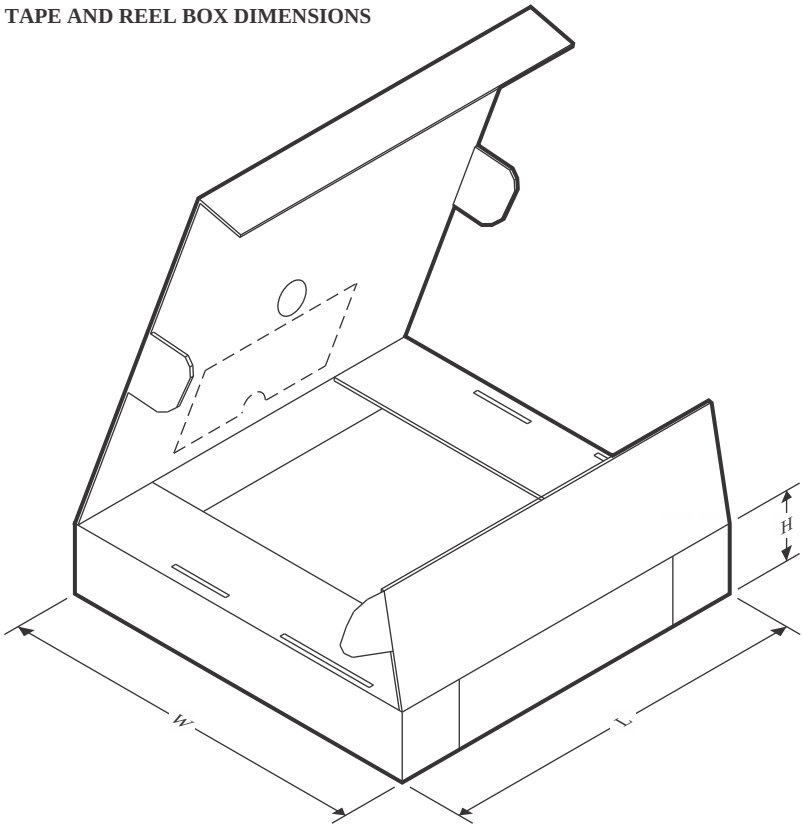
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB4020BIPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB4020BIPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8

GENERIC PACKAGE VIEW

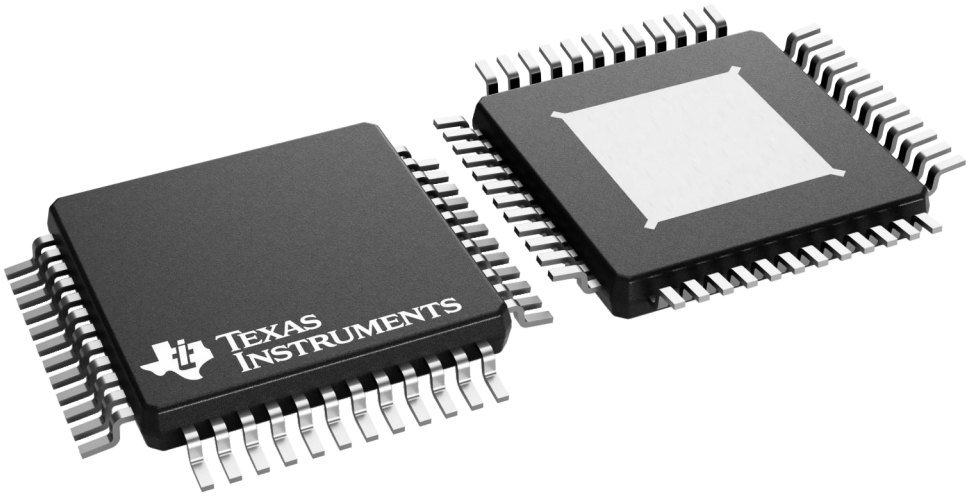
PHP 48

TQFP - 1.2 mm max height

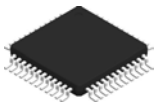
7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



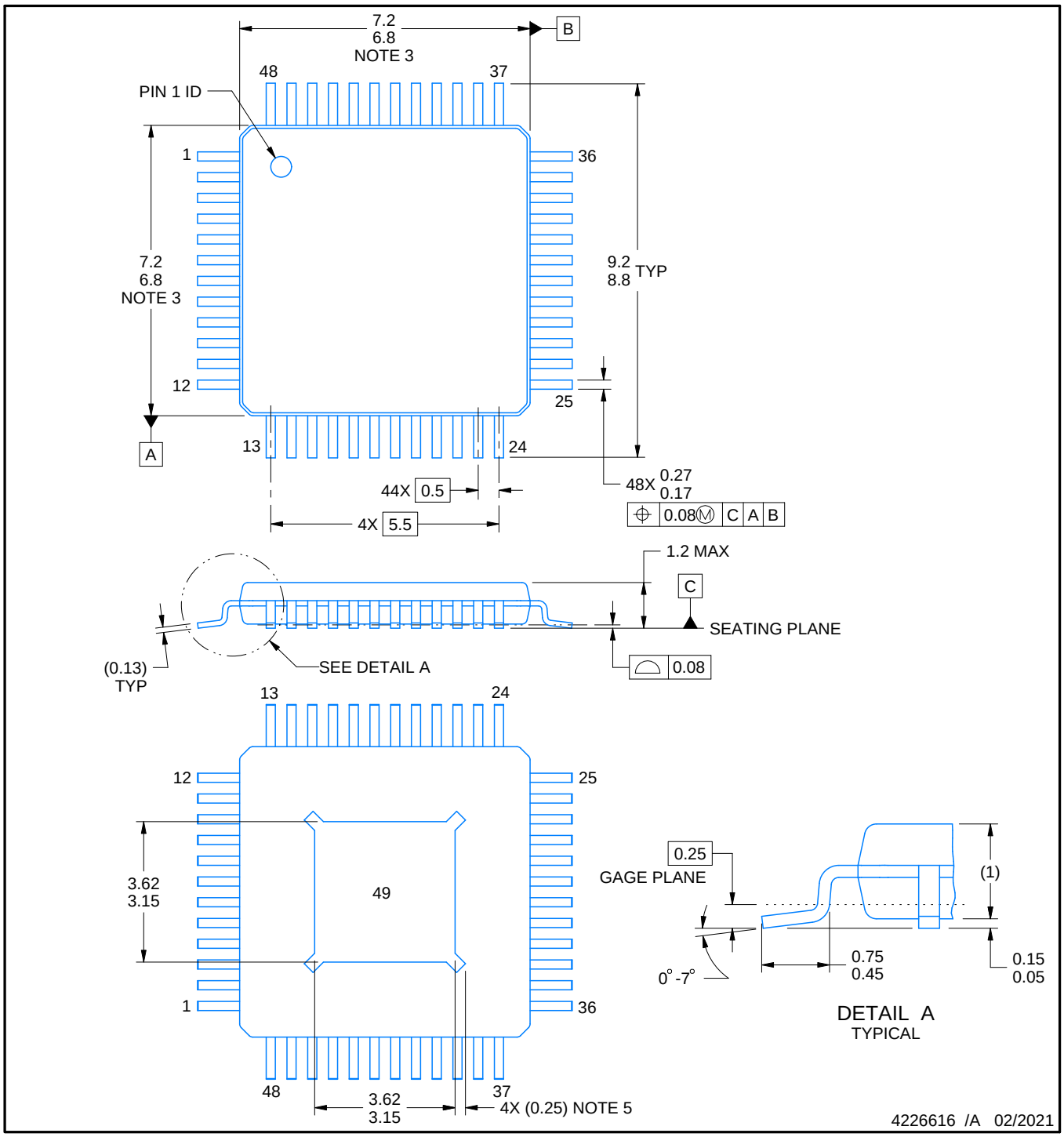
4226443/A



PACKAGE OUTLINE

PHP0048E

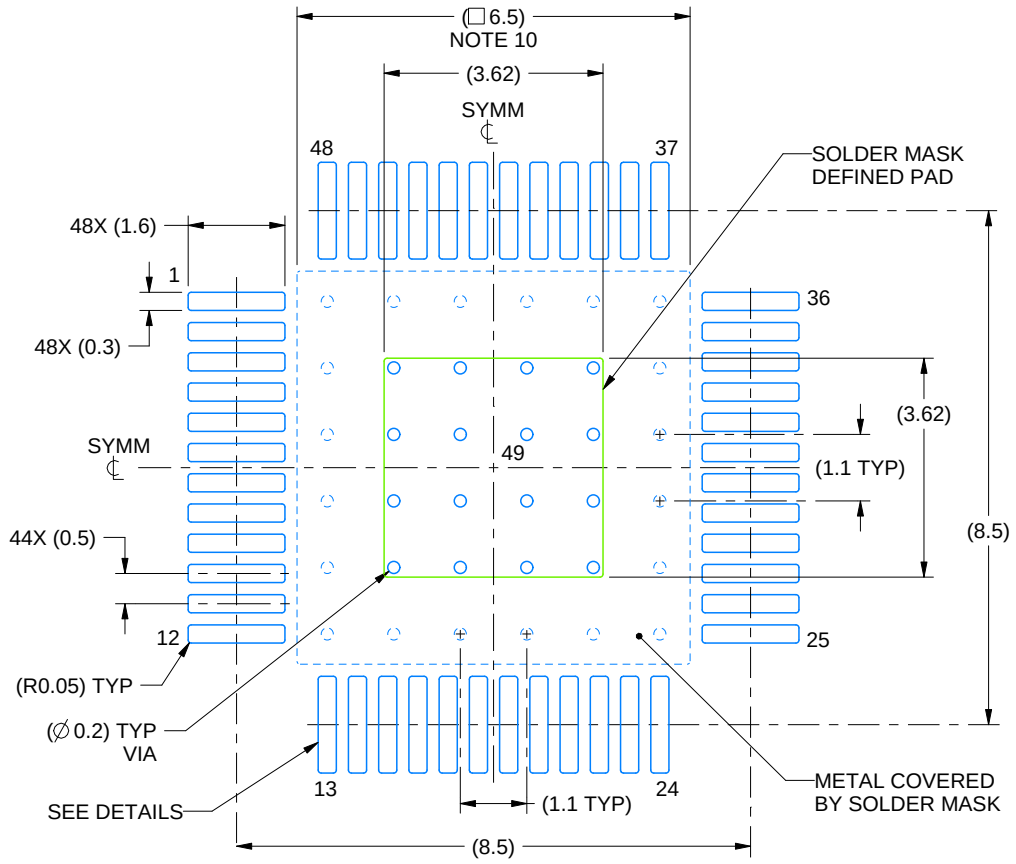
PowerPAD™ HTQFP - 1.2 mm max height



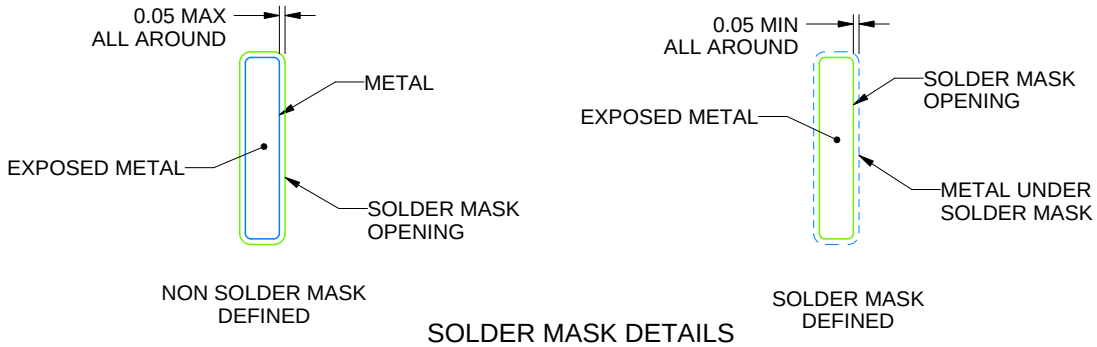
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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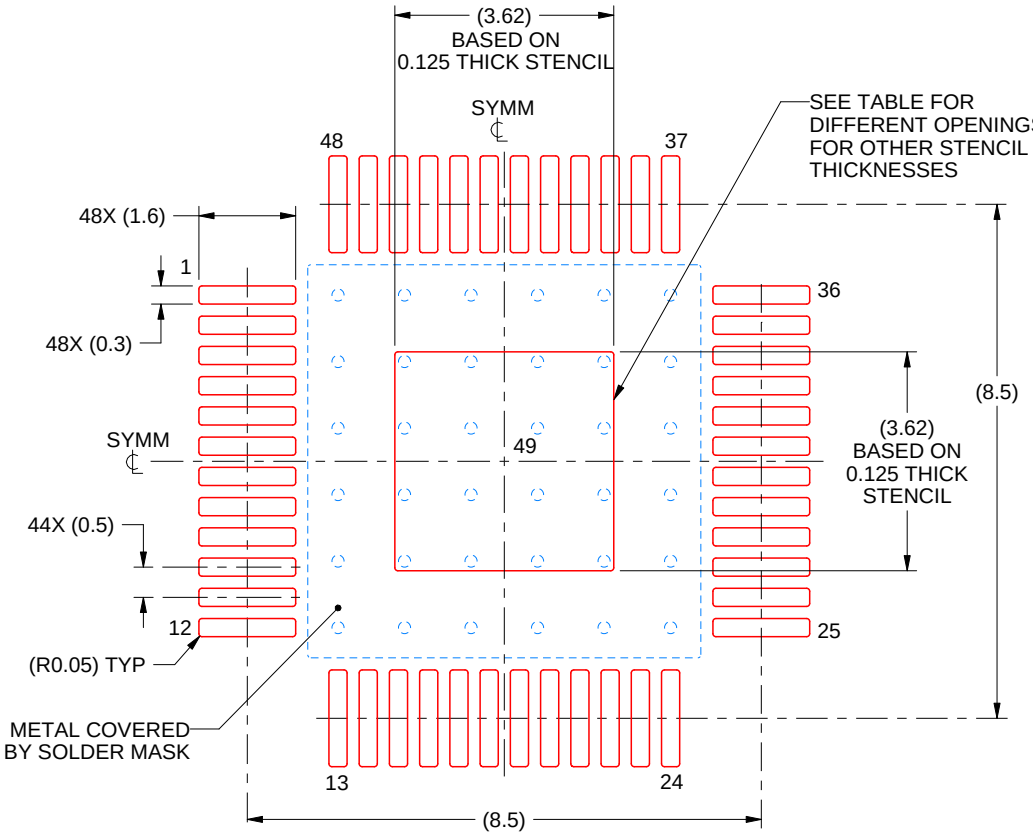
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.05 X 4.05
0.125	3.62 x 3.62 (SHOWN)
0.150	3.30 x 3.30
0.175	3.06 x 3.06

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月