TEXAS INSTRUMENTS
TUSB8043A
JAJSHM9 – JUNE 2019

TUSB8043A 4 ポート USB 3.2 x1 Gen1 ハブ

1 特長

- 4 ポートの USB 3.2 x1 Gen1 (5Gbps) ハブ
- USB 2.0 ハブ機能
  - MTT (Multiple Transaction Translator) ハブ：4 つのトランザクション・トランスレータ
  - トランザクション・トランスレータごとに 2 つの非同期エンドポイント・バッファ
- バッテリ充電のサポート
  - 上流ポートの未接続または未構成時に、D+/D- デバイダ充電ポート (ACP1、ACP2、ACP3) をサポート
  - 上流ポートの未接続時に、DCP または ACP モード間の自動移行モードをサポート
  - Galaxy 充電をサポート
  - CDP モード (上流ポート接続時)
  - DCP モード (上流ポート未接続時)
  - DCP モードは中国電気通信業界標準 YD/T 1591-2009 に準拠
- USB 3.2 x1 Gen1 または USB 2.0 複合デバイスとしての動作をサポート
- ポート単位または一括制御のパワー・スイッチングおよび過電流通知入力
- 4 つの外部下流ポートと、USB HID から I^2C への変換機能のための内部 USB 2.0 専用ポートをサポート
- USB HID を介した I^2C 制御用の内部下流ポートで、ハイ・スピードおよびフル・スピード動作をサポートし、上流ポートに対応する速度を実現
- I^2C の読み出し/書き込みと、100kおよび 400k (デフォルト) での EEPROM の読み出しに対するベンダー要求をサポート
- I^2C マスタでクロック・ストレッチングをサポート
- OTP ROM、シリアル EEPROM、または I^2C/SMBus スレーブ・インターフェイスで次のカスタム構成をサポート
  - VID および PID
  - ポートのカスタマイズ
  - メーカーおよび製品文字列 (OTP ROM は除く)
  - シリアル番号 (OTP ROM は除く)
- ピン選択か、EEPROM または I^2C/SMBus スレーブ・インターフェイスを使用したアプリケーション機能の選択
- 128 ビットの UUID (Universally Unique Identifier) を提供
- USB 2.0 上流ポート経由で、オンボードおよびイン・システムの EEPROM のプログラムをサポート
- 単一クロック入力、24MHz の水晶または発振器
- 下流ポートは USB 2.0 の構成のみ
- 64 ピン QFN パッケージ (RGC)

2 アプリケーション

コンピュータ・システム、ドッキング・ステーション、モニタ、セットトップ・ボックス

3 概要

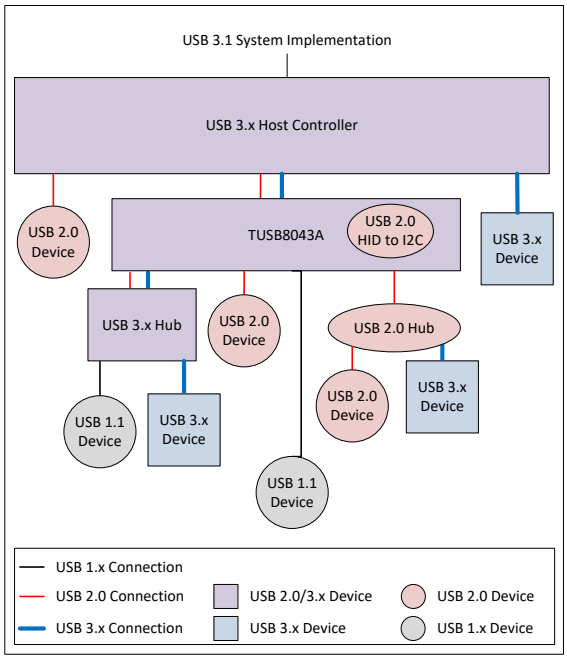
TUSB8043A は、4 ポートの USB 3.2 x1 Gen1 (5Gbps) ハブです。上流ポートでスーパー・スピードUSBおよびハイ・スピード/フル・スピード接続を同時に提供し、下流ポートでスーパー・スピードUSB、ハイ・スピード、フル・スピード、ロー・スピード接続を提供します。ハイ・スピード、フル・スピード、ロー・スピード接続のみをサポートする電子環境に上流ポートが接続されている場合、スーパー・スピードUSB接続は下流ポートで無効化されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TUSB8043A	VQFN (64)	9.00mm×9.00mm
TUSB8043AI	VQFN (64)	9.00mm×9.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

図



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4 改訂履歴

日付	リビジョン	注
2019 年 6 月	*	暫定版リリース

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5 概要（続き）

フル・スピード、ロー・スピード接続のみをサポートする電子環境に上流ポートが接続されている場合、スーパー・スピードUSBおよびハイ・スピード接続は下流ポートで無効化されます。

TUSB8043Aは、ポート別または一括制御のパワー・スイッチングと過電流保護を提供し、バッテリ充電アプリケーションをサポートします。

ポート別電力制御のハブでは、USBホストからの要求に応じて各下流ポートへの電力がオン/オフされます。また、過電流を検出した場合には、影響を受ける下流ポートへの電力だけがオフになります。

一括制御のハブでは、いずれかのポートで電力が必要になると、すべての下流ポートへの給電をオンにします。下流ポートへの給電は、すべてのポートが給電を停止できる状態にならない限り、オフになりません。また、一括制御のハブが過電流イベントを検出すると、すべての下流ポートへの給電がオフになります。

TUSB8043Aの下流ポートは、Battery Charging Downstream Port (CDP)ハンドシェイクに対応することで、バッテリ充電アプリケーションにサポートを提供します。また、上流ポートの未接続時にDedicated Charging Port (DCP)をサポートします。DCPモードは、USBバッテリ充電、Galaxy充電、中国電気通信業界標準YD/T 1591-2009をサポートするUSBデバイスに対応します。 上流ポートの未接続時、TUSB8043A はさらに、デバイダ充電ポート・モード (ACPx モード) と、ACP3 から DCP までの全モード間の自動移行をサポートします。

TUSB8043Aは、バッテリ充電サポートなどの機能のためにピン・ストラップ構成を提供しており、OTP ROM、I^2C EEPROM、またはI^2C/SMBusスレーブ・インターフェイスを介した、PID、VID、カスタム・ポート、PHY構成のカスタマイズをサポートしています。また、I^2C EEPROMまたはI^2C/SMBusスレーブ・インターフェイスを使用する場合、カスタム文字列をサポートします。

TUSB8043Aは、内部USB HIDからI^2Cへのインターフェイスを介して、接続先のEEPROMのプログラミングをサポートします。

このデバイスは 64 ピンの RGC パッケージで供給されます。0°C～70°C の温度範囲で動作する民生用バージョン (TUSB8043A) と、-40°C～85°C の温度範囲で動作する産業用バージョン (TUSB8043AI) を提供しています。

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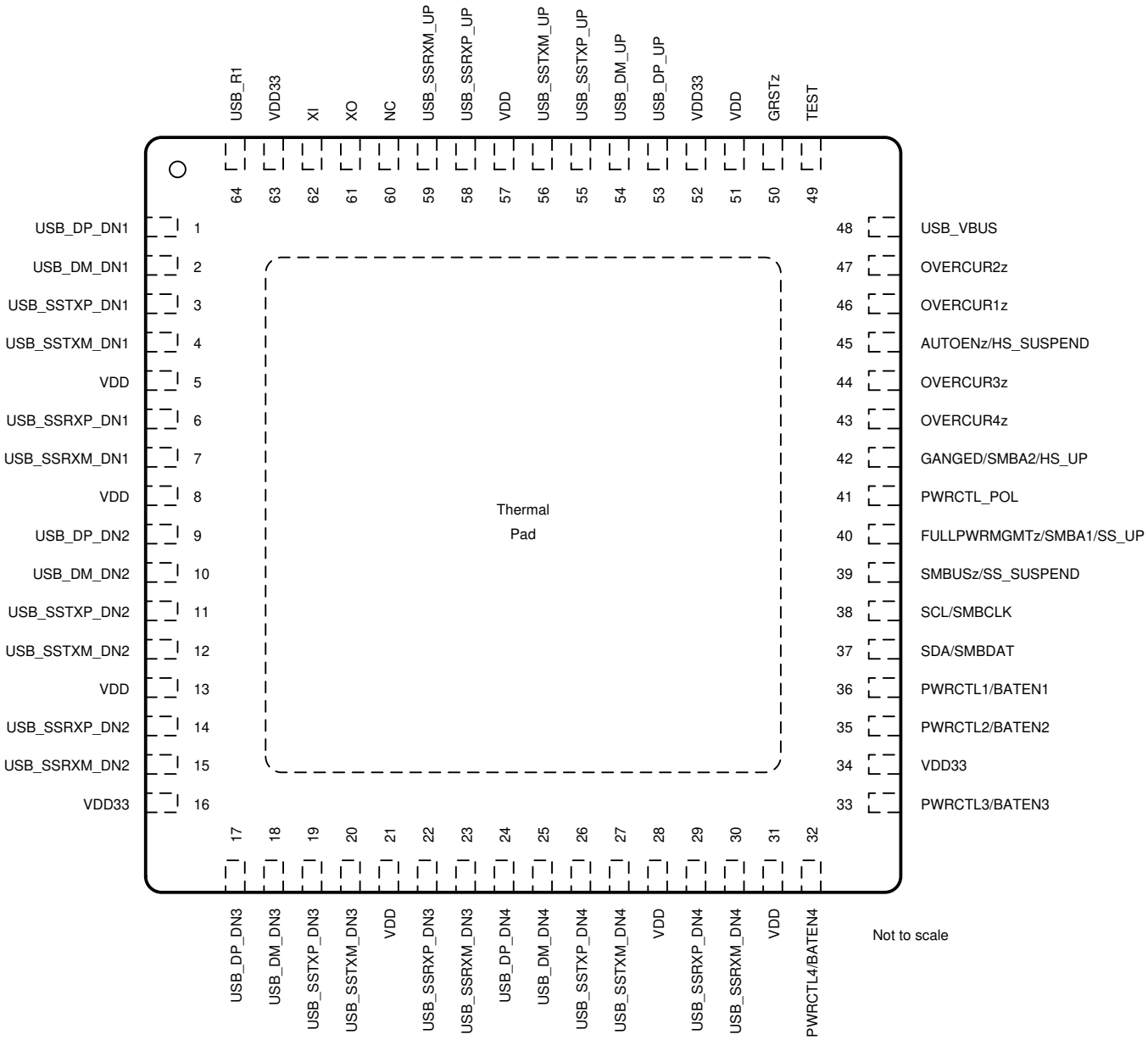
6 Pin Configuration and Functions

RGC Package
64 Pin (VQFN)
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Clock and Reset Signals			
GRSTz	50	I, PU	Global power reset. This reset brings all of the TUSB8043A internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.
XI	62	I	Crystal input. This pin is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
XO	61	O	Crystal output. This pin is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
USB Upstream Signals			
USB_SSTXP_UP	55	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	56	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	58	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	59	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	53	I/O	USB High-speed differential transceiver (positive)
USB_DM_UP	54	I/O	USB High-speed differential transceiver (negative)
USB_R1	64	I	Precision resistor reference. A 9.53-kΩ ±1% resistor should be connected between USB_R1 and GND.
USB_VBUS	48	I	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9-KΩ ±1% resistor, and to ground through a 10-kΩ ±1% resistor from the signal to ground.
USB Downstream Signals			
USB_SSTXP_DN1	3	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN1	4	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN1	6	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN1	7	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN1	1	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN1	2	I/O	USB High-speed differential transceiver (negative)
PWRCTL1/BATEN1	36	I/O, PD	USB Port 1 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 1. This pin be left unconnected if power management is not implemented. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 1 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR1z	46	I, PU	USB Port 1 Over-Current Detection. This pin is typically connected to the over current output of the downstream port power switch for Port 1. 0 = An over current event has occurred 1 = An over current event has not occurred When GANGED power management is enabled, this pin or one of the other OVERCURz pins must be connected to the over current output of the power switch or circuit which detects the over current conditions. For the case when another OVERCURz pin is used, this pin can be left unconnected.
USB_SSTXP_DN2	11	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN2	12	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN2	14	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN2	15	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN2	9	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN2	10	I/O	USB High-speed differential transceiver (negative)
PWRCTL2/BATEN2	35	I/O, PD	USB Port 2 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 2. This pin be left unconnected if power management is not implemented. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 2 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OVERCUR2z	47	I, PU	USB Port 2 Over-Current Detection. This pin is typically connected to the over current output of the downstream port power switch for Port 2. 0 = An over current event has occurred 1 = An over current event has not occurred When GANGED power management is enabled, this pin or one of the other OVERCURz pins must be connected to the over current output of the power switch or circuit which detects the over current conditions. For the case when another OVERCURz pin is used, this pin can be left unconnected.
USB_SSTXP_DN3	19	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN3	20	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN3	22	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN3	23	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN3	17	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN3	18	I/O	USB High-speed differential transceiver (negative)
PWRCTL3/BATEN3	33	I/O, PD	USB Port 3 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 3. This pin be left unconnected if power management is not implemented. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 3 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR3z	44	I, PU	USB Port 3 Over-Current Detection. This pin is typically connected to the over current output of the downstream port power switch for Port 3. 0 = An over current event has occurred 1 = An over current event has not occurred When GANGED power management is enabled, this pin or one of the other OVERCURz pins must be connected to the over current output of the power switch or circuit which detects the over current conditions. For the case when another OVERCURz pin is used, this pin can be left unconnected.
USB_SSTXP_DN4	26	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN4	27	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN4	29	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN4	30	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN4	24	I/O	USB High-speed differential transceiver (positive)
USB_DM_DN4	25	I/O	USB High-speed differential transceiver (negative)
PWRCTL4/BATEN4	32	I/O, PD	USB Port 4 Power On Control for Downstream Power/Battery Charging Enable. The pin is used for control of the downstream power switch for Port 4. This pin be left unconnected if power management is not implemented. In addition, the value of the pin is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 4 as indicated in the Battery Charging Support register: 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR4z	43	I, PU	USB Port 4 Over-Current Detection. This pin is typically connected to the over current output of the downstream port power switch for Port 4. 0 = An over current event has occurred 1 = An over current event has not occurred When GANGED power management is enabled, this pin or one of the other OVERCURz pins must be connected to the over current output of the power switch or circuit which detects the over current conditions. For the case when another OVERCURz pin is used, this pin can be left unconnected.
I^2C/SMBUS I^2C Signals			

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SCL/SMBCLK	38	I/O, PD	I^2C clock/SMBus clock. Function of pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin acts as the serial clock interface for an I^2C EEPROM. When SMBUSz = 0, this pin acts as the serial clock interface for an SMBus host. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	37	I/O, PD	I^2C data/SMBus data. Function of pin depends on the setting of the SMBUSz input. When SMBUSz = 1, this pin acts as the serial data interface for an I^2C EEPROM. When SMBUSz = 0, this pin acts as the serial data interface for an SMBus host. Can be left unconnected if external interface not implemented.
SMBUSz/SS_SUSPEND	39	I/O, PU	I^2C/SMBus mode select/SuperSpeed USB Suspend Status. The value of the pin is sampled at the de-assertion of reset set I^2C or SMBus mode as follows: 1 = I^2C Mode Selected 0 = SMBus Mode Selected Can be left unconnected if external interface not implemented. After reset, this signal indicates the SuperSpeed USB Suspend status of the upstream port if enabled through the stsOutputEn bit in the Additional Feature Configuration register. When enabled, a value of 1 indicates the connection is suspended.
Test and Miscellaneous Signals			
FULLPWRMGMTz/FULLAUTOz/SMBA1/SS_UP	40	I/O, PD	Full power management enable/SMBus address bit 1/SuperSpeed USB Connection Status Upstream port. The value of the pin is sampled at the de-assertion of reset to set the power switch control follows: 0 = Power switching and over current inputs supported 1 = Power switching and over current inputs not supported Full power management is the ability to control power to the downstream ports of the TUSB8043A using PWRCTL[4:1]/BATEN[4:1]. If BATENx = 1 on any port, full power management must be enabled so the value of the terminal is sampled at the de-assertion to initialize the value of the FULLAUTOz bit. When AUTOENz = 0 and FULLAUTOz = 0: all ACP modes are supported. When AUTOENz = 0 and FULLAUTOz = 1:only highest current ACP mode is used in auto mode. When SMBus mode is enabled, this pin sets the value of the SMBus slave address bit 1. Can be left unconnected if full power management and SMBus are not implemented. After reset, this signal indicates the SuperSpeed USB connection status of the upstream port if enabled through the stsOutputEn bit in the Additional Feature Configuration register. When enabled a value of 1 indicates the upstream port is connected to a SuperSpeed USB capable port. Note: Power switching must be supported for battery charging applications.
PWRCTL_POL	41	I/O, PU	Power Control Polarity. The value of the pin is sampled at the de-assertion of reset to set the polarity of PWRCTL[4:1]. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GANGED/SMBA2/HS_UP	42	I/O, PD	Ganged operation enable/SMBus Address bit 2/HS Connection Status Upstream Port. The value of the pin is sampled at the de-assertion of reset to set the power switch and over current detection mode as follows: 0 = Individual power control supported when power switching is enabled 1 = Power control gangs supported when power switching is enabled When SMBus mode is enabled using SMBUSz, this pin sets the value of the SMBus slave address bit 2. After reset, this signal indicates the High-speed USB connection status of the upstream port if enabled through the stsOutputEn bit in Additional Feature Configuration register. When enabled, a value of 1 indicates the upstream port is connected to a High-speed USB capable port. Note: Individual power control must be enabled for battery charging applications.
AUTOENz/HS_SUSPEND	45	I/O, PU	Automatic Charge Mode Enable/HS Suspend Status. The value of the pin is sampled at the de-assertion of reset to determine if automatic mode is enabled as follows: 0 = Automatic Mode is enabled on ports that are enabled for battery charging when the hub is unconnected. Please note that CDP is not supported on Port 1 when operating in Automatic mode. 1 = Automatic Mode is disabled This value is also used to set the autoEnz bit in the Battery Charging Support Register. After reset, this signal indicates the High-speed USB Suspend status of the upstream port if enabled through the stsOutputEn bit in Additional Feature Configuration register. When enabled, a value of 1 indicates the connection is suspended.
TEST	49	I	This pin is reserved for factory test. For normal operation, this pin requires an external pull down resistor to ground on PCB. Recommend 10k or stronger resistor.
Power and Ground Signals			
VDD	5, 8, 13, 21, 28, 31, 51, 57	PWR	1.1-V power rail
VDD33	16, 34, 52, 63	PWR	3.3-V power rail
VSS (Thermal Pad)		PWR	Ground. Thermal pad must be connected to ground.
NC	60	—	No connect, leave floating

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	V_{DD} Supply voltage range	-0.3	1.4	V
	V_{DD33} Supply voltage range	-0.3	3.8	V
Voltager Range	USB_SSRXP_UP, USB_SSRXN_UP, SSRXP_DN[4:1], USB_RXN_DP[4:1] and USB_VBUS terminals	-0.3	1,4	V
	XI terminal	-0.3	2.45	V
	All other terminals	-0.3	3.8	V
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	1.1V Supply voltage	0.99	1.1	1.26	V
V_{DD33}	3.3V Supply voltage	3.0	3.3	3.6	V
USB_VBUS	Voltage at USB_VBUS terminal.	0		1.155	V
T_A	TUSB8043A Ambient temperature	0		70	°C
T_A	TUSB8043AI Ambient temperature	-40		85	°C
T_J	Junction temperature	-40		105	°C

7.4 Thermal Information

THERMAL METRIC(1)		TUSB8043A RGC 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low Power Modes						
I_{DD_PWRON}	V_{DD} current after Power On (after reset)	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		18		mA
I_{DD33_PWRON}	V_{DD33} current after Power On (after reset)	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		2		mA
I_{DD_UPDISC}	V_{DD} current when upstream port is disconnected	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		23		mA
I_{DD33_UPDISC}	V_{DD33} current when upstream port is disconnected	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		2		mA
$I_{DD_SUSPEND}$	V_{DD} current in Suspend	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		23		mA
$I_{DD33_SUSPEND}$	V_{DD33} current in Suspend	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		2		mA
Active Power Modes (US State / DS State)						
I_{DD_SMBUS}	V_{DD} current during SMbus programming.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		290		mA
I_{DD33_SMBUS}	V_{DD33} current during SMbus programming	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		75		mA
$I_{DD_3H_1SS_0HS_U12}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 1 SS device, and 0 HS device. Links in U1/U2.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		220		mA
$I_{DD33_3H_1SS_0HS_U12}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 1 SS device, and 0 HS device. Links in U1/U2.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_1SS_0HS_U0}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 1 SS device, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		330		mA
$I_{DD33_3H_1SS_0HS_U0}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 1 SS device, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_2SS_0HS_U12}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 2 SS devices, and 0 HS device. Links in U1/U2	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		301		mA
$I_{DD33_3H_2SS_0HS_U12}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 2 SS devices, and 0 HS device. Links in U1/U2	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_2SS_0HS_U0}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 2 SS devices, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		460		mA
$I_{DD33_3H_2SS_0HS_U0}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 2 SS devices, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_3SS_0HS_U12}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 3 SS devices, and 0 HS device. Links in U1/U2	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		372		mA
$I_{DD33_3H_3SS_0HS_U12}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 3 SS devices, and 0 HS device. Links in U1/U2	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA

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Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD_3H_3SS_0HS_U0}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 3 SS devices, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		560		mA
$I_{DD33_3H_3SS_0HS_U0}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 3 SS devices, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_4SS_0HS_U12}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 4 SS devices, and 0 HS device. Links in U1/U2	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		467		mA
$I_{DD33_3H_4SS_0HS_U12}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 4 SS devices, and 0 HS device. Links in U1/U2	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_4SS_0HS_U0}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 4 SS devices, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		672		mA
$I_{DD33_3H_4SS_0HS_U0}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 4 SS devices, and 0 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_3H_1SS_1HS_U0}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 1 SS device, and 1 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		372		mA
$I_{DD33_3H_1SS_1HS_U0}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 1 SS devices, and 1 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		84		mA
$I_{DD_3H_1SS_2HS_U0}$	V_{DD} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 2 SS device, and 2 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		480		mA
$I_{DD33_3H_1SS_2HS_U0}$	V_{DD33} current upstream port connected to USB 3.0 Host, downstream port(s) connected to 2 SS devices, and 2 HS device. Links in U0.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		95		mA
$I_{DD_2H_0SS_1HS}$	V_{DD} current upstream port connected to USB 2.0 Host, downstream port(s) connected to 0 SS device, and 1 HS device.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD33_2H_0SS_1HS}$	V_{DD33} current upstream port connected to USB 2.0 Host, downstream port(s) connected to 0 SS devices, and 1 HS device.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		45		mA
$I_{DD_2H_0SS_4HS}$	V_{DD} current upstream port connected to USB 2.0 Host, downstream port(s) connected to 0 SS device, and 4 HS device.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		74		mA
$I_{DD33_2H_0SS_4HS}$	V_{DD33} current upstream port connected to USB 2.0 Host, downstream port(s) connected to 0 SS devices, and 4 HS device.	V_{DD} = 1.1V; V_{DD33} = 3.3V; T_A = 25 °C;		76		mA
3.3V I/O						
V_{IH}	High-level input voltage(1)		2		3.6	V

(1) Applies to external inputs and bi-directional buffers

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Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage(1)		0		0.8	V
V_I	Input voltage		0		3.6	V
V_O	Output voltage(2)		0		3.6	V
t_t	Input transition time (t_{RISE} and t_{FALL})				25	ns
V_{HYS}	Input hysteresis(3)				1.3 x V_{DD33}	V
V_{OH}	High-level output voltage	I_{OH} = -4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OH} = 4 mA			0.4	V
I_{OZP}	High-impedance output current with internal pullup or pulldown resistor.(4)	V_I = 0 to V_{DD33};	-250		250	µA
I_I	Input current(5)	V_I = 0 to V_{DD33};	-15		15	µA
R_{PD}	Internal pull-down resistance		13.5	19	27.5	kΩ
R_{PU}	Internal pull-up resistance		14.5	19	25	kΩ

(2) Applies to external outputs and bi-directional buffers
(3) Applies to GRSTZ
(4) Applies to pins with internal pullups/pulldowns.
(5) Applies to external input buffers

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Power-on timings. Refer to 図 1					
t_{d1}	V_{DD} stable before V_{DD33} stable. (1) (2)	0			ms
t_{d2}	V_{DD} and V_{DD33} before de-assertion of GRSTz.	3			ms
t_{su_io}	Setup for MISC inputs. (3)	0.1			µs
t_{hd_io}	Hold for MISC inputs. (3)	0.1			µs
t_{VDD33_RAMP}	V_{DD33} supply ramp requirement.	0.2		100	ms
t_{VDD_RAMP}	V_{DD} supply ramp requirement.	0.2		100	ms

(1) As long as GRSTz is de-asserted after both supplies are stable, there is no power-on relationship between V_{DD33} and V_{DD}. If GRSTz is only connected to a capacitor to GND, then V_{DD} must be stable minimum of 10 µs before V_{DD33}.
(2) An active reset is required if the V_{DD33} supply is stable before V_{DD} supply. This active reset shall meet the 3 ms power-up delay counting from both power supplies stable to de-assertion of GRSTz.
(3) MISC pins sampled at de-assertion of GRSTz: BATEN[4:1], AUTOENz, FULLPWRMGMTz, GANGED, SMBUSz, and PWRCTL_POL.

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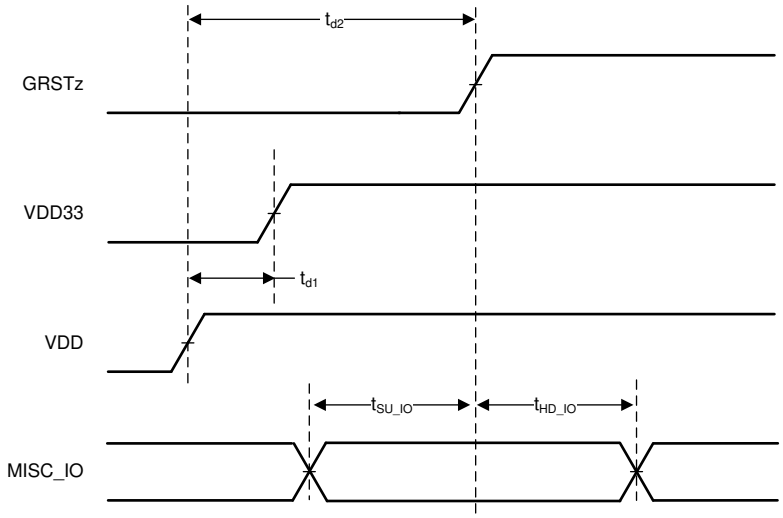

図 1. Power-Up Timing Requirements

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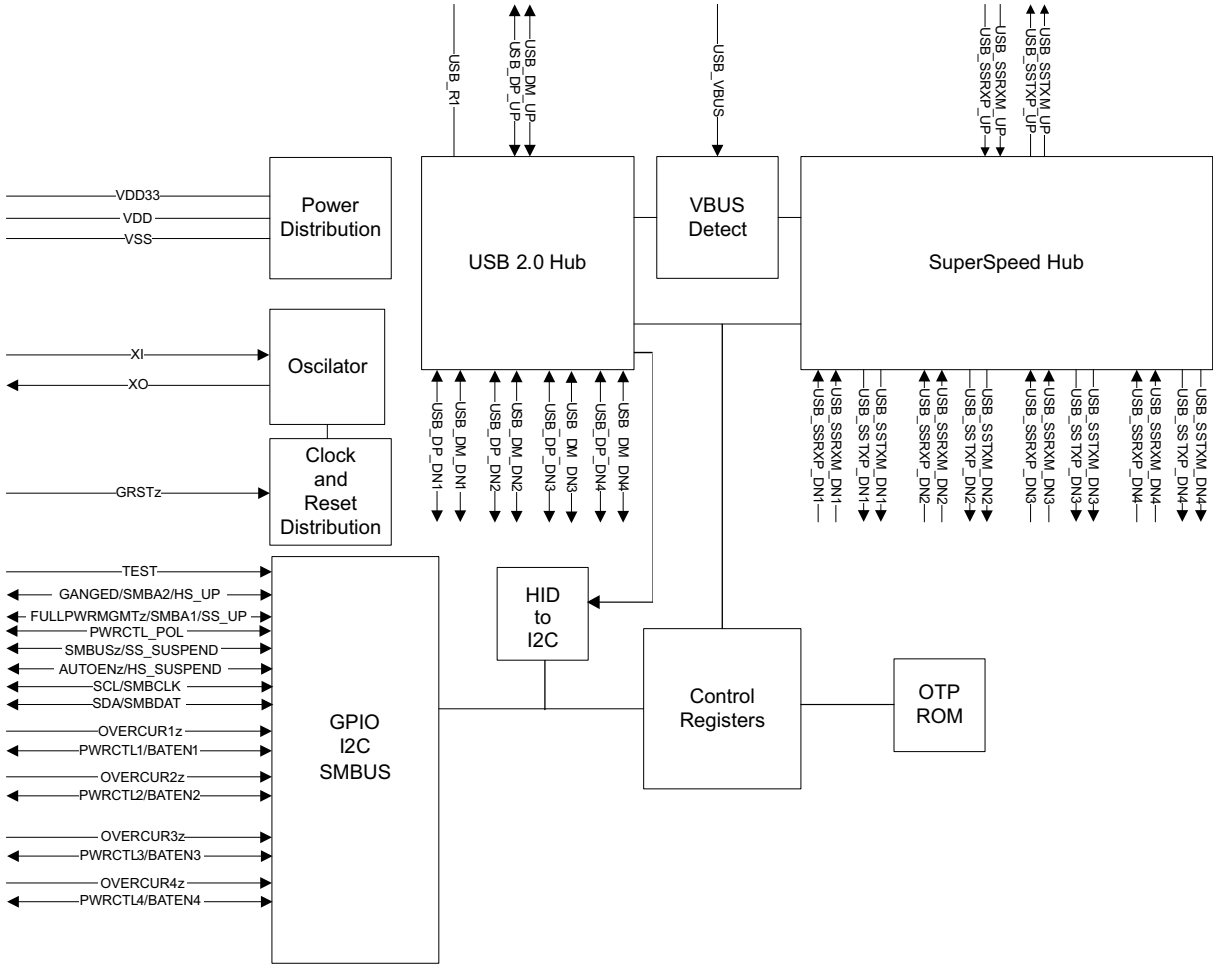
8 Detailed Description

8.1 Overview

The TUSB8043A is a four-port USB 3.2 x1 Gen1 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Battery Charging Features

The TUSB8043A provides support for USB Battery Charging (BC1.2) and custom charging. Battery charging support may be enabled on a per port basis through the REG_6h(batEn[3:0]) or the BATEN[4:1] pins.

USB Battery charging support includes both Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009. CDP is enabled when the upstream port has detected valid VBUS, configured, and host sets port power. When the upstream port is not connected and battery charging support is enabled, the TUSB8043A enables DCP mode once all other battery modes such as ACPx have failed or are disabled.

In addition to USB Battery charging (BC1.2), the TUSB8043A supports custom charging indications: Divider Charging (ACP3, ACP2, ACP1 modes), and Galaxy compatible charging. These custom charging modes are only supported when upstream port is unconnected and AUTOMODE is enabled. AUTOMODE can be enabled either thru AUTOENz pin or from Reg_0Ah bit 1 (autoModeEnz) . When in AUTOMODE and upstream port is disconnected, the port automatically transitions from ACP mode to the DCP mode depending on the portable device connected. The divided mode places a fixed DC voltage on the ports DP and DM signals which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 10W (ACP3). The divider mode can be configured to report a lower-current setting (up to 5 W) through REG_0Ah (HiCurAcpModeEn).

When the upstream port is not connected and battery charging support is enabled for a port, the TUSB8043A drives the port power enable active. If AUTOMODE is disabled, then DCP mode is used. If AUTOMODE is enabled and fully automatic mode is disabled (FullAutoEn bit is cleared (Reg_25h Bit 0) or FULLAUTOz pin = 0), then TUSB8043A starts with highest enabled divider current mode (ACPx). The TUSB8043A remains in highest current mode as long as a pull-up is not detected on DP pin. If an pull-up is detected on DP pin, then TUSB8043A drives the port power enable inactive and switch to Galaxy mode, if enabled, or to DCP mode if Galaxy mode is disabled. The TUSB8043A again drives the port power enable active. The TUSB8043A remains in Galaxy mode as long as no pull-up is detected on DP pin. If an pull-up is detected on DP pin, then TUSB8043A drives the port power enable inactive and transition to DCP mode. The TUSB8043A again drives the port power enable active. In DCP mode, the TUSB8043A looks for a pull-up detected on DP pin or RxVdat. If a pull-up or RxVdat is detected on DP, the TUSB8043A remains in DCP mode. If no pull-up or RxVdat is detected on DP pin after 2 seconds, the TUSB8043A drives the port power enable inactive and transition back to ACPx mode. This sequence repeats until upstream port is connected.

When Automatic mode is enabled and full automatic mode is enabled (FullAutoEn Reg_25h bit 0 is set or FULLAUTOz pin = 1), TUSB8043A performs same sequence described in previous paragraph with the addition of attempting all supported ACPx modes before sequencing to Galaxy Mode (if enabled) or DCP mode.

The supported battery charging modes when TUSB8043A configured for SMBus or external EEPROM is detailed in Battery Charging Modes with SMBus/EEPROM Table.

The supported battery charging modes when TUSB8043A configured for I2C but without an external EEPROM is determined by the sampled state of the pins. These modes are detailed in Battery Charging Modes without EEPROM Table.

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Feature Description (continued)

表 1. TUSB8043A Battery Charging Modes with SMBus or I2C EEPROM

batEn[n] Reg_06h Bits 3:0	Upstream VBUS	HiCurAcpMode En Reg_0Ah Bit 4	autoModeEnz Reg_0Ah Bit 1	FullAutoEn Reg_25h Bit 0	Galaxy_Enz Reg_25h Bit 1	Battery Charging Mode Port x (x = n + 1)
0	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	No Charging support
1	> 4V	Don't Care	Don't Care	Don't Care	Don't Care	CDP
1	< 4V	Don't Care	1	Don't Care	Don't Care	DCP
1	< 4V	Don't Care	0	1	1	AUTOMODE enabled. Sequences through all ACPx modes and DCP Alternate ACP3, ACP2, ACP1, DCP
1	< 4 V	0	0	0	1	AUTOMODE enabled. Sequences between ACP2 and DCP. Alternate ACP2, DCP
1	< 4V	1	0	0	1	AUTOMODE enabled. Sequences between ACP3 and DCP. Alternate ACP3, DCP
1	< 4V	Don't Care	0	1	0	AUTOMODE enabled with Galaxy compatible charging support. Alternate ACP3, ACP2, ACP1, Galaxy, DCP
1	< 4V	0	0	0	0	AUTOMODE enabled with Galaxy compatible charging support. Alternate ACP2, Galaxy, DCP
1	< 4V	1	0	0	0	AUTOMODE enabled with Galaxy compatible charging support. Alternate ACP3, Galaxy, DCP

表 2. TUSB8043A Battery Charging Modes without EEPROM

BATEN[3:0] pins	Upstream VBUS	AUTOENz pin	FULLAUTOz pin	Battery Charging Mode Port x (x = n + 1)
0	Don't Care	Don't Care	Don't Care	No Charging support
1	> 4V	Don't Care	Don't Care	CDP
1	< 4V	1	0	DCP
1	< 4V	0	0	AUTOMODE enabled with Galaxy compatible charging support. Sequences through all ACPx modes. Alternate ACP3, ACP2, ACP1, Galaxy, DCP.
1	< 4V	0	1	AUTOMODE enabled with Galaxy compatible charging support. Alternate ACP3, Galaxy, DCP
1	< 4V	1	1	AUTOMODE enabled. Sequences through all ACPx modes. Alternate ACP3, ACP2, ACP1, DCP.

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8.3.2 USB Power Management

The TUSB8043A can be configured for power switched applications using either per-port (Full power managed) or ganged power-enable controls and over-current status inputs. When battery charge is enabled, the TUSB8043A always functions in full power managed.

Power switch support is enabled by REG_5h (fullPwrMgmtz) and the per-port or ganged mode is configured by REG_5h(ganged).

The TUSB8043A supports both active high and active low power-enable controls. The PWRCTL[4:1] polarity is configured by REG_Ah(pwrctlPol). The power control polarity can also be selected by the PWRCTL_POL pin.

8.3.3 I^2C Programming Support Using Internal HID to I^2C Interface

The TUSB8043A I^2C programming mode is supported using class-specific requests through the HID interface. The HID embedded port is numbered 1 greater than the highest numbered exposed port. The internal HID to I^2C function of the TUSB8043A does not have an interrupt OUT endpoint. The TUSB8043A supports *GET REPORT (Input)* through the HID interrupt and control endpoints. The *GET REPORT (Feature)* and *SET REPORT (Output)* occurs through the control endpoint.

表 3. HID Requests I^2C Programming Support

COMMAND	bmRequestType	bRequest	wValue	wIndex	wLength	DATA
Setup field Offset	Offset = 0	Offset = 1	Offset = 2	Offset = 4	Offset = 6	N/A
GET REPORT	A1H	01H	0100H – input 0300H - feature	0000H	Report Length	Report
SET REPORT	21H	09H	0200H – output	0000H	Report Length	Report

Other HID class specific requests are optional and not supported (SET IDLE, SET PROTOCOL, GET IDLE, GET PROTOCOL) . Also report IDs are not required since all requests are not interleaved.

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8.3.3.1 SET REPORT (Output)

Report length includes overhead bytes (1 byte of opcode, 1 byte of device address and 2 bytes of data length) and must match the number of bytes sent in the data stage or the request is stalled.

- 1-byte opcode
  - 8'b0000xy01 read I2C
  - 8'b0000xy10 write I2C with stop
  - 8'b0000xy11 write I2C without stop (use to set sub-address prior to read)
  - Bit 2 (y) when set forces 100 kHz I^2C.
  - Bit 3 (x) when set disables EP1. When EP1 is disabled, EP1 will always NAK and EP0 should be used for Get Report.
- 1-byte I2C slave (7-bit) address
- 2-byte I2C transaction data length
- "length" bytes of Data for a write, but none for a read.

Set Report status stage reports only the status of the receipt and validity of the request, not the status of the I^2C transaction. As long as the fields construct a valid request, the status stage is Acked by a null packet. Otherwise, it is STALLed. For example, if the report_length does not match the amount of data sent before the status stage or the wLength does not match the number of bytes of data sent in the data stage, the status stage is STALLed.

Software shall ensure properly formatted commands and data responses. The sum of the start address and wLength shall be less than the total size of the address range of the target device in a properly formatted command. Hardware shall wrap any data addresses above FFFFh and shall discard any data transmitted greater than wLength and return STALL. A STALL is returned if opcode is 00h.

The I^2C master that performs the I^2C reads and writes initiated through USB HID interface supports clock stretching. It operates at 400 kHz by default, but can be configured for 100 kHz through eFuse or register or by opcode.

If the TUSB8043A is suspended (L2) by the USB host, the USB HID interface must enter suspend, but the I^2C master shall remain active while attempting to complete an active I^2C write request. An active I^2C read request may be aborted if the TUSB8043A enters USB suspend state. Per the USB specification, the USB host should not suspend the HID interface while an I^2C read or write is still in progress. The USB HID interface shall refuse requests to enter USB 2.0 sleep mode (L1) while an I^2C read or write is in progress.

8.3.3.2 GET REPORT (Feature)

This HID Report is return a 2-byte constant (0x82FF) which can be used to identify compatible HID devices even if the customer changes the VID/PID.

8.3.3.3 GET REPORT (Input)

A report length of one reports the status byte only. To receive a report with data, the report length must be the length of the data, plus one byte for status and two bytes for the length field.

- 1-byte Status
  - 0 Success
  - 1 Fail — timeout (35 ms)
  - 2 Fail — Address nak
  - 3 Fail — data nak
- 2-byte length
- "length" bytes of Data for a read, but not for a write.

A Get Report (input) request is required for both read and write. The interrupt and control endpoint will NAK until the I^2C transaction is complete, so that it can report length, data for a read, and final status.

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8.3.4 One Time Programmable (OTP) Configuration

The TUSB8043A allows device configuration through one time programmable non-volatile memory (OTP). The programming of the OTP is supported using vendor-defined USB device requests. For details using the OTP features please contact your TI representative.

表 4 provides a list features which may be configured using the OTP.

表 4. OTP Configurable Features

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_01h	[7:0]	Vendor ID LSB
REG_02h	[7:0]	Vendor ID MSB
REG_03h	[7:0]	Product ID LSB
REG_04h	[7:0]	Product ID MSB
REG_07h	[0]	Port removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_07h	[1]	Port removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_07h	[2]	Port removable configuration for downstream ports 3. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_07h	[3]	Port removable configuration for downstream ports 4. OTP configuration is inverse of rmbl[3:0], i.e. 1 = not removable, 0 = removable.
REG_08h	[3:0]	Port used Configured register.
REG_0Ah	[1]	Battery Charger Automatic Mode enable.
REG_0Ah	[4]	High-current divider mode enable.
REG_0Bh	[0]	USB 2.0 port polarity configuration for upstream port.
REG_0Bh	[1]	USB 2.0 port polarity configuration for downstream ports 1.
REG_0Bh	[2]	USB 2.0 port polarity configuration for downstream ports 2.
REG_0Bh	[3]	USB 2.0 port polarity configuration for downstream ports 3.
REG_0Bh	[4]	USB 2.0 port polarity configuration for downstream ports 4.
REG_25h	[4:0]	Device Configuration Register 3
REG_26h	[3:0]	USB2.0 Only Port Register
REG_F0h	[3:1]	USB BC power switch power off duration during automode.

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8.3.5 Clock Generation

The TUSB8043A accepts a crystal input to drive an internal oscillator or an external clock source. If a clock is provided to XI instead of a crystal, XO is left open. Otherwise, if a crystal is used, the connection needs to follow the guidelines below. Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by shielding C1 and C2 with the clean ground lines.

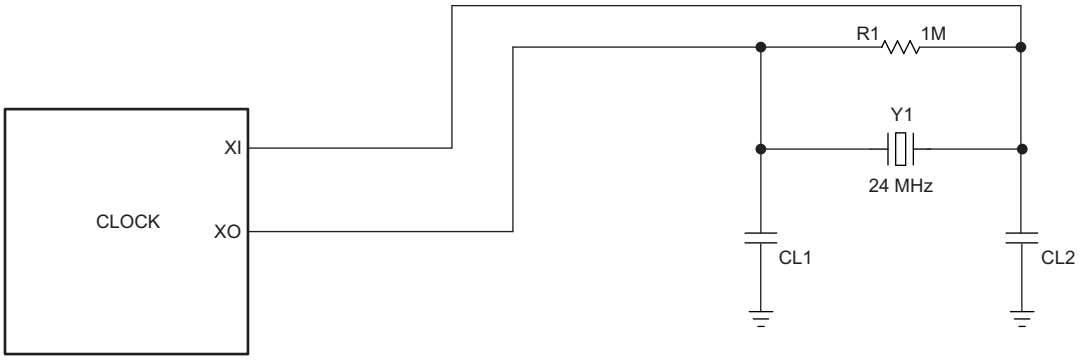

図 2. TUSB8043A Clock

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8.3.6 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 pF - 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, a maximum crystal equivalent series resistance (ESR) of 50 Ω is recommended. A parallel load capacitor should be used if a crystal source is used. The exact load capacitance value used depends on the crystal vendor. Refer to application note *Selection and Specification for Crystals for Texas Instruments USB2.0 devices* (SLLA122) for details on how to determine the load capacitance value.

8.3.7 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.2 Gen1 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating.

8.3.8 Power-Up and Reset

The TUSB8043A does not have specific power sequencing requirements with respect to the core power (VDD) or I/O and analog power (VDD33) as long as GRSTz is held in an asserted state while supplies ramp. The core power (VDD) or I/O power (VDD33) may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit. When a RC circuit is used, the external capacitor size chosen must be large enough to meet the 3ms minimum duration requirement. The R of the RC circuit is the internal R_{PU}.

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8.4 Device Functional Modes

8.4.1 External Configuration Interface

The TUSB8043A supports a serial interface for configuration register access. The device may be configured by an attached I^2C EEPROM or accessed as a slave by an external SMBus master. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT pins are pulled up to 3.3 V at the de-assertion of reset. The mode, I^2C master or SMBus slave, is determined by the state of SMBUSz/SS_SUSPEND pin at reset. With the integrated USB HID to I^2C master, the I^2C interface can also be used to program an external EEPROM or perform updates of an external MCU's firmware.

8.4.2 I^2C EEPROM Operation

The TUSB8043A supports a single-master, standard mode (100 KHz) or fast mode (400KHz) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB8043A reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0. The TUSB8043A reads the entire EEPROM contents using a single burst read transaction. The burst read transaction ends when the address reaches FFh.

If the value of the EEPROM contents at address byte 00h equals 55h, the TUSB8043A loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8043A exits the I^2C mode and continues execution with the default values in the configuration registers. The hub is not connect on the upstream port until the configuration is completed.

注

The bytes located above offset Ah are optional. The requirement for data in those addresses is dependent on the options configured in the Device Configuration, and Device Configuration 2 registers.

The minimum size I^2C EEPROM required is 2Kbit.

For details on I^2C operation refer to the UM10204 I^2C-bus Specification and User Manual.

8.4.3 Port Configuration

The TUSB8043A port configurations can be selected by registers or efuse. The Port Used Configuration register (USED[3:0]) define how many ports can possibly be reported by the hub. The device removable configuration register (RMBL[3:0]) define if the ports that USB 3.2 are reported as used have permanently connected devices or not. The USB 2.0 Only Port register (USB2_ONLY[3:0]) define whether or not a used port is reported as part of the USB 2.0 hub or both the USB2.0 and SS hubs. The USB2_ONLY field enables the USB2.0 port even if the corresponding USED bit is low. The internal HID port will always be the highest number USB2.0 port. 表 5 shows examples of the possible combinations.

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Device Functional Modes (continued)

表 5. TUSB8043A Downstream Port Configuration Examples

USED[3:0]	RMBL[3:0]	USB2_ONLY [3:0]	Reported Port Configuration	Physical to Logical Port mapping
1111	1111	0000	4 Port USB 3.2 Hub 5 Port USB2.0 Hub Port 5 is permanently attached HID	Physical1 => Logical Port1 for USB 3.2 and USB2.0. Physical2 => Logical Port2 for USB 3.2 and USB2.0. Physical3 => Logical Port3 for USB 3.2 and USB2.0. Physical4 => Logical Port4 for USB 3.2 and USB2.0. Physical5 => Logical Port5 for USB2.0.
1110	1111	0000	3 Port USB 3.2 Hub 4 Port USB2.0 Hub Port 4 is permanently attached HID	Physical1 Not used. Physical2 => Logical Port1 for USB 3.2 and USB2.0. Physical3 => Logical Port2 for USB 3.2 and USB2.0. Physical4 => Logical Port3 for USB 3.2 and USB2.0. Physical5 => Logical Port4 for USB 2.0.
1100	0111	0000	2 Port USB 3.2 Hub 3 Port USB2.0 hub with permanently attached device on Port 2 Port 3 is a permanently attached HID	Physical1 Not used. Physical2 Not used. Physical3 => Logical Port1 for USB 3.2 and USB2.0. Physical4 => Logical Port2 for USB 3.2 and USB2.0. Physical5 => Logical Port3 for USB2.0.
0011	1111	0010	1 Port USB 3.2 Hub 3 Port USB 2.0 Hub Port 3 is a permanently attached HID	Physical1 => Logical Port1 for USB 3.2 and USB2.0. Physical2 => Logical Port2 for USB2.0. Physical3 Not Used. Physical4 Not used. Physical5 => Logical Port3 for USB2.0.
1000	1111	0010	1 Port USB 3.2 Hub 3 Port USB 2.0 Hub Port 3 is a permanently attached HID	Physical1 Not used. Physical2 => Logical Port2 for USB2.0. Physical3 Not used Physical4 => Logical Port1 for USB 3.2 and USB2.0. Physical5 => Logical Port3 for USB2.0.
1111	1111	1110	1 Port USB 3.2 Hub 5 Port USB 2.0 Hub Port 5 is a permanently attached HID	Physical1 => Logical Port1 for USB 3.2 and USB2.0. Physical2 => Logical Port2 for USB2.0. Physical3 => Logical Port3 for USB2.0. Physical4 => Logical Port4 for USB2.0. Physical5 => Logical Port5 for USB2.0.

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8.4.4 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8043A supports read block and write block protocols as a slave-only SMBus device.

The TUSB8043A slave address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP pin at reset,
- y is the state of FULLPWRMGMTz/SMBA1/SS_UP pin at reset, and
- z is the read/write bit; 1 = read access, 0 = write access.

For details on SMBus requirements, refer to the System Management Bus Specification.

注

If the TUSB8043A is addressed by a host using an unsupported protocol it does not respond. The TUSB8043A waits indefinitely for configuration by the SMBus host and doesnot connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

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8.5 Register Maps

8.5.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be over-written when the TUSB8043A is in I^2C or SMBus mode. Refer to 表 4 for registers configurable from OTP.

表 6. TUSB8043A Register Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	Yes
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved. Must default to 00h.	Yes
0Ah	Device Configuration Register 2	Yes
0Bh	USB 2.0 Port Polarity Control Register	Yes
0Ch-0Fh	Reserved	No
10h-1Fh	UUID Byte [15:0]	No
20h-21h	LangID Byte [1:0]	Yes
22h	Serial Number Length	Yes
23h	Manufacturer String Length	Yes
24h	Product String Length	Yes
25h	Device Configuration Register 3	Yes
26h	USB 2.0 Only Port Register	Yes
27h-2Eh	Reserved	Yes
2Fh	Reserved	No
30h-4Fh	Serial Number String Byte [31:0]	Yes
50h-8Fh	Manufacturer String Byte [63:0]	Yes
90h-CFh	Product String Byte [63:0]	Yes
D0h-D4h	Reserved	Yes, but do not change default.
D5h-D7h	Reserved	No
D8h-DCh	Reserved	Yes, but do not change default.
DDh-EFh	Reserved	No
F0h	Additional Features Configuration Register	Yes
F1h-F7h	Reserved	No
F8h	SMBus Device Status and Command Register	No
F9h - FFh	Reserved	No

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8.5.2 ROM Signature Register

図 3. Register Offset 0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 7. Bit Descriptions – ROM Signature Register

Bit	Field	Type	Description
7:0	romSignature	RW	ROM Signature Register. This register is used by the TUSB8043A in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8043A aborts the EEPROM load and executes with the register defaults.

8.5.3 Vendor ID LSB Register

図 4. Register Offset 1h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	1	0	0	0	1

表 8. Bit Descriptions – Vendor ID LSB Register

Bit	Field	Type	Description
7:0	vendorIdLsb	RO/RW	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID. Value used for this field is the non-zero value written by EEPROM/SMBus to both PID and VID. If a zero value is written by EEPROM/SMbus to both PID and VID, then value used for this field is the non-zero value from OTP. If a zero value is written by OTP, then value used for this field is 51h.

8.5.4 Vendor ID MSB Register

図 5. Register Offset 2h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

表 9. Bit Descriptions – Vendor ID MSB Register

Bit	Field	Type	Description
7:0	vendorIdMsb	RO/RW	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID. Value used for this field is the non-zero value written by EEPROM/SMBus to both PID and VID. If a zero value is written by EEPROM/SMbus to both PID and VID, then value used for this field is the non-zero value from OTP. If a zero value is written by OTP, then value used for this field is 04h.

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8.5.5 Product ID LSB Register

図 6. Register Offset 3h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	0	0	0	0	0

表 10. Bit Descriptions – Product ID LSB Register

Bit	Field	Type	Description
7:0	productIdLsb	RO/RW	Product ID LSB. Least significant byte of the product ID assigned by Texas Instruments and reported in the SuperSpeed Device descriptor. the default value of this register is 40h representing the LSB of the SuperSpeed product ID assigned by Texas Instruments The value reported in the USB 2.0 Device descriptor is the value of this register bit wise XORed with 00000010b. The value may be over-written to indicate a customer product ID. Value used for this field is the non-zero value written by EEPROM/SMBus to both PID and VID. If a zero value is written by EEPROM/SMbus to both PID and VID, then value used for this field is the non-zero value from OTP. If a zero value is written by OTP, then value used for this field is 40h .

8.5.6 Product ID MSB Register

図 7. Register Offset 4h

Bit No.	7	6	5	4	3	2	1	0
Reset State	1	0	0	0	0	0	1	1

表 11. Bit Descriptions – Product ID MSB Register

Bit	Field	Type	Description
7:0	productIdMsb	RO/RW	Product ID MSB. Most significant byte of the product ID assigned by Texas Instruments; the default value of this register is 83h representing the MSB of the product ID assigned by Texas Instruments. The value may be over-written to indicate a customer product ID. Value used for this field is the non-zero value written by EEPROM/SMBus to both PID and VID. If a zero value is written by EEPROM/SMbus to both PID and VID, then value used for this field is the non-zero value from OTP. If a zero value is written by OTP, then value used for this field is 83h.

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8.5.7 Device Configuration Register

図 8. Register Offset 5h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	X	X	0	0

表 12. Bit Descriptions – Device Configuration Register

Bit	Field	Type	Description
7	customStrings	RW	Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers 0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only 1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0.
6	customSernum	RW	Custom serial number enable. This bit controls the ability to write to the serial number registers. 0 = The Serial Number String Length and Serial Number String registers are read only 1 = Serial Number String Length and Serial Number String registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0.
5	u1u2Disable	RW	U1 U2 Disable. This bit controls the U1/U2 support. 0 = U1/U2 support is enabled 1 = U1/U2 support is disabled, the TUSB8043A will not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP. After receiving or sending an FLPMA LMP, it continues to enable U1 and U2 according to USB 3.2 protocol until it gets a power-on reset or is disconnected on its upstream port. When the TUSB8043A is in I^2C mode, the TUSB8043A loads this bit from the contents of the EEPROM. When the TUSB8043A is in SMBUS mode, the value may be over-written by an SMBus host.
4	RSVD	RO	Reserved. This bit is reserved and returns 1 when read.
3	ganged	RW	Ganged. This bit is loaded at the de-assertion of reset with the value of the GANGED/SMBA2/HS_UP pin. 0 = When fullPwrMgmtz = 0, each port is individually power switched and enabled by the PWRCTL[4:1]/BATEN[4:1] pins 1 = When fullPwrMgmtz = 0, the power switch control for all ports is ganged and enabled by the PWRCTL[4:1]/BATEN1 pin When the TUSB8043A is in I^2C mode, the TUSB8043A loads this bit from the contents of the EEPROM. When the TUSB8043A is in SMBUS mode, the value may be over-written by an SMBus host.
2	fullPwrMgmtz	RW	Full Power Management. This bit is loaded at the de-assertion of reset with the value of the FULLPWRMGMTz/SMBA1/SS_UP pin. 0 = Port power switching status reporting is enabled 1 = Port power switching status reporting is disabled When the TUSB8043A is in I^2C mode, the TUSB8043A loads this bit from the contents of the EEPROM. When the TUSB8043A is in SMBUS mode, the value may be over-written by an SMBus host.
1	u1u2TimerOvr	RW	U1 U2 Timer Override. When this field is set, the TUSB8043A overrides the downstream ports U1/U2 timeout values set by USB 3.2 Host software. If software sets value in the range of 1h - FFh, the TUSB8043A uses the value of FFh. If software sets value to 0, then TUSB8043A uses value of 0. REG_09h [6] must be set to enable this feature.
0	RSVD	RO	Reserved. This field is reserved and returns 0 when read.

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8.5.8 Battery Charging Support Register

図 9. Register Offset 6h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

表 13. Bit Descriptions – Battery Charging Support Register

Bit	Field	Type	Description
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	batEn[3:0]	RW	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. 0 = The port is not enabled for battery charging support features 1 = The port is enabled for battery charging support features Each bit corresponds directly to a downstream port, i.e. batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2. The default value for these bits are loaded at the de-assertion of reset with the value of PWRCTL/BATEN[3:0]. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host.

8.5.9 Device Removable Configuration Register

図 10. Register Offset 7h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

表 14. Bit Descriptions – Device Removable Configuration Register

Bit	Field	Type	Description
7	customRmbl	RW	Custom Removable. This bit controls selection of port removable bits, port used bits, and USB2_ONLY bits. 0 = rmbl[3:0], used[3:0], and USB2_ONLY[3:0] are read only and the values are loaded from the OTP ROM 1 = rmbl[3:0], used[3:0], and USB2_ONLY[3:0] are read/write and can be loaded by EEPROM or written by SMBus This bit may be written simultaneously with rmbl[3:0].
6:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	rmbl[3:0]	RO/RW	Removable. The bits in this field indicate whether a device attached to downstream ports 4 through 1 are removable or permanently attached. 0 = The device attached to the port is not removable 1 = The device attached to the port is removable Each bit corresponds directly to a downstream port n + 1, i.e. rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, etc. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this filed reflects the inverted values of the OTP ROM non_rmb[3:0] field.

8.5.10 Port Used Configuration Register

図 11. Register Offset 8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	1	1	1

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表 15. Bit Descriptions – Port Used Configuration Register

Bit	Field	Type	Description
7:4	RSVD	RO	Reserved. Read only.
3:0	used[3:0]	RO/RW	Used. The bits in this field indicate whether a port is enabled. 0 = The port is not used or disabled 1 = The port is used or enabled Each bit corresponds directly to a downstream port, i.e. used0 corresponds to downstream port 1, used1 corresponds to downstream port 2, etc. This field is read only unless the customRmbl bit is set to 1. When the corresponding USB2_ONLY bit is set, the USB2 port is used and enabled regardless of the bit programmed into this field.

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8.5.11 Device Configuration Register 2

図 12. Register Offset Ah

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	X	0	0	0	0	0

表 16. Bit Descriptions – Device Configuration Register 2

Bit	Field	Type	Description
7	Reserved	RO	Reserved. Read-only, returns 0 when read.
6	customBCfeatures	RW	Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls. 0 = The HiCurAcpModeEn is read only and the values are loaded from the OTP ROM. 1 = The HiCurAcpModeEn bit is read/write and can be loaded by EEPROM or written by SMBus. This bit may be written simultaneously with HiCurAcpModeEn.
5	pwrctlPol	RW	Power enable polarity. This bit is loaded at the de-assertion of reset with the value of the PWRCTL_POL pin. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high When the TUSB8043A is in I^2C mode, the TUSB8043A loads this bit from the contents of the EEPROM. When the TUSB8043A is in SMBUS mode, the value may be over-written by an SMBus host.
4	HiCurAcpModeEn	RO/RW	High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. 0 = High current divider mode disabled . High current is ACP2(default) 1 = High current divider mode enabled. High current mode is ACP3 This bit is read only unless the customBCfeatures bit is set to 1. If customBCfeatures is 0, the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit.
3:2	Reserved	RW	Reserved. These registers are unused and returns whatever value was written.
1	autoModeEnz	RW	Automatic Mode Enable. This bit is loaded at the de-assertion of reset with the value of the AUTOENz/HS_SUSPEND pin. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions: 0 = Automatic mode battery charging features are enabled. 1 = Automatic mode is disabled; only Battery Charging DCP and CDP mode is supported. NOTE: When the upstream port is connected, Battery Charging CDP mode is supported on all ports that are enabled for battery charging support regardless of the value of this bit.
0	RSVD	RO	Reserved. Read only, returns 0 when read.

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8.5.12 USB 2.0 Port Polarity Control Register

図 13. Register Offset Bh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 17. Bit Descriptions – USB 2.0 Port Polarity Control Register

Bit	Field	Type	Description
7	customPolarity	RW	Custom USB 2.0 Polarity. This bit controls the ability to write the p[4:0]_usb2pol bits. 0 = The p[4:0]_usb2pol bits are read only and the values are loaded from the OTP ROM. 1 = The p[4:0]_usb2pol bits are read/write and can be loaded by EEPROM or written by SMBus. This bit may be written simultaneously with the p[4:0]_usb2pol bits
6:5	RSVD	RO	Reserved. Read only, returns 0 when read.
4	p4_usb2pol	RO/RW	Downstream Port 4 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p4_usb2pol bit.
3	p3_usb2pol	RO/RW	Downstream Port 3 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p3_usb2pol bit.
2	p2_usb2pol	RO/RW	Downstream Port 2 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p2_usb2pol bit.
1	p1_usb2pol	RORW	Downstream Port 1 DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p1_usb2pol bit.
0	p0_usb2pol	RO/RW	Upstream Port DM/DP Polarity. This controls the polarity of the port. 0 = USB 2.0 port polarity is as documented by the pin out 1 = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p0_usb2pol bit.

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8.5.13 UUID Registers

図 14. Register Offset 10h-1Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	X	X	X	X	X	X

表 18. Bit Descriptions – UUID Byte N Register

Bit	Field	Type	Description
7:0	uuidByte[n]	RO	UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

8.5.14 Language ID LSB Register

図 15. Register Offset 20h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	1

表 19. Bit Descriptions – Language ID LSB Register

Bit	Field	Type	Description
7:0	langIdLsb	RO/RW	Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8043A only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

8.5.15 Language ID MSB Register

図 16. Register Offset 21h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 20. Bit Descriptions – Language ID MSB Register

Bit	Field	Type	Description
7:0	langIdMsb	RO/RW	Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8043A only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

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8.5.16 Serial Number String Length Register

図 17. Register Offset 22h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	1	0	0	0

表 21. Bit Descriptions – Serial Number String Length Register

Bit	Field	Type	Description
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RO/RW	Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24 byte serial number string is supported. The maximum string length is 32 bytes. When customSernum is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

8.5.17 Manufacturer String Length Register

図 18. Register Offset 23h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 22. Bit Descriptions – Manufacturer String Length Register

Bit	Field	Type	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RO/RW	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

8.5.18 Product String Length Register

図 19. Register Offset 24h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 23. Bit Descriptions – Product String Length Register

Bit	Field	Type	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RO/RW	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 3 from the data contained in the Product String registers.

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8.5.19 Device Configuration Register 3

図 20. Register Offset 25h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 24. Bit Descriptions – Device Configuration Register 3

Bit	Field	Type	Description
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5	bcdUSB30	RW	This field when set forces SS hub to report bcdUSB = 3.0 instead of 3.2.
4	USB2.0_only	RW	USB 2.0 hub reports as 2.0 only. This bit disables the USB 2.0 hub from reporting 5Gbps support in the wSpeedsSupported field of the USB SS BOS SS device capability descriptor. This bit also disables the USB3.0 hub. This bit is read/write but the read value returned is the Boolean OR of this bit and the corresponding eFuse bit. If either bit is set, this feature is enabled.
3	USB2_DFP_UNCONF	RW	This field when set enables USB 2.0-defined Unconfigured state on DFPs.
2	I2C_100k	R/W	I2C 100kHz. This bit controls the clock rate of the I2C master for both USB to I2C requests . The EEPROM reads occurs at 400K unless eFuse is used to set the rate to 100k. This bit is read/write but the read value returned is the Boolean OR of this bit and the corresponding eFuse bit. If either bit is set, this feature is enabled.
1	Galaxy_Enz	R/W	Disable Galaxy compatible modes. When this field is high, Galaxy charging compatible mode does not included in AUTOMODE charger sequence. This bit is read/write but the read value returned is the Boolean OR of this bit and the corresponding eFuse bit. If either bit is set, this feature is disabled.
0	FullAutoEn	R/W	Enable all divider battery charging modes. When automode is enabled and this bit is set, any DS port enabled for battery charging attempts all divider battery charging modes before DCP, starting with the highest current option. The bit is writable, but the value read back is the Boolean OR of this bit and the corresponding eFuse control. If either bit is set, eFuse or this register, this feature is enabled.

8.5.20 USB 2.0 Only Port Register

図 21. Register Offset 26h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	0

表 25. Bit Descriptions – USB 2.0 Only Port Register

Bit	Field	Type	Description
7:4	RSVD	RO	Reserved. Read only.
3:0	USB2_ONLY[3:0]	RO/RW	USB 2.0 Only Ports. The bits in this field primarily indicate whether a port is enabled only for USB 2.0 operation. This field is read-only unless customRmbl bit is set. Also, these bits overrides the corresponding USED bit. A value of 0 indicates the hub port is enabled for both USB 3.2 and USB 2.0. A value of 1 indicates the hub port is enabled only for USB 2.0 operation.

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8.5.21 Serial Number String Registers

図 22. Register Offset 30h-4Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	x	x	x	x	x	x

表 26. Bit Descriptions – Serial Number Registers

Bit	Field	Type	Description
7:0	serialNumber[n]	RO/RW	Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is assigned by TI. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host.

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8.5.22 Manufacturer String Registers

図 23. Register Offset 50h-8Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 27. Bit Descriptions – Manufacturer String Registers

Bit	Field	Type	Description
7:0	mfgStringByte[n]	RW	Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

8.5.23 Product String Registers

図 24. Register Offset 90h-CFh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 28. Bit Descriptions – Product String Byte N Register

Bit	Field	Type	Description
7:0	prodStringByte[n]	RO/RW	Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

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8.5.24 Additional Feature Configuration Register

図 25. Register Offset F0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 29. Bit Descriptions – Additional Feature Configuration Register

Bit	Field	Type	Description
7:5	Reserved	RW	Reserved. This field defaults to 3'b000 and must not be changed.
4	stsOutputEn	RW	Status output enable. This field when set enables of the Status output signals, HS_UP, HS_SUSPEND, SS_UP, SS_SUSPEND. 0 = STS outputs are disabled. 1 = STS outputs are enabled. This bit may be loaded by EEPROM or over-written by a SMBUS host.
3:1	pwronTime	RW	Power On Delay Time. When the efuse_pwronTime field is all 0s, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from ACP to DCP Mode. The nominal timing is defined as follows: TPWRON_EN = (pwronTime x 1) x 200 ms (1) This field may be over-written by EEPROM contents or by an SMBus host.
0	usb3spreadDis	RW	USB3 Spread Spectrum Disable. This bit allows firmware to disable the spread spectrum function of the USB3 phy PLL. 0 = Spread spectrum function is enabled 1= Spread spectrum function is disabled This bit may be loaded by EEPROM or over-written by a SMBUS host.

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8.5.25 SMBus Device Status and Command Register

図 26. Register Offset F8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

表 30. Bit Descriptions – SMBus Device Status and Command Register

Bit	Field	Type	Description
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1	smbusRst	RSU	SMBus interface reset. This bit loads the registers back to their GRSTz values. Note, that since this bit can only be set when in SMBus mode the cfgActive bit is also reset to 1. When software sets this bit it must reconfigure the registers as necessary. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	RCU	Configuration active. This bit indicates that configuration of the TUSB8043A is currently active. The bit is set by hardware when the device enters the I2C or SMBus mode. The TUSB8043A shall not connect on the upstream port while this bit is 1. When in I2C mode, the bit is cleared by hardware when the TUSB8043A exits the I2C mode. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TUSB8043A is a four-port USB 3.2 x1 Gen1 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low speed connections on the downstream port. The TUSB8043A can be used in any application that needs additional USB compliant ports. For example, a specific notebook may only have two downstream USB ports. By using the TUSB8043A, the notebook can increase the downstream port count to five.

9.2 Typical Application

9.2.1 Discrete USB Hub Product

A common application for the TUSB8043A is as a self powered standalone USB hub product. The product is powered by an external 5V DC Power adapter. In this application, using a USB cable TUSB8043A upstream port is plugged into a USB Host controller. The downstream ports of the TUSB8043A are exposed to users for connecting USB hard drives, cameras, flash drives, and so forth.

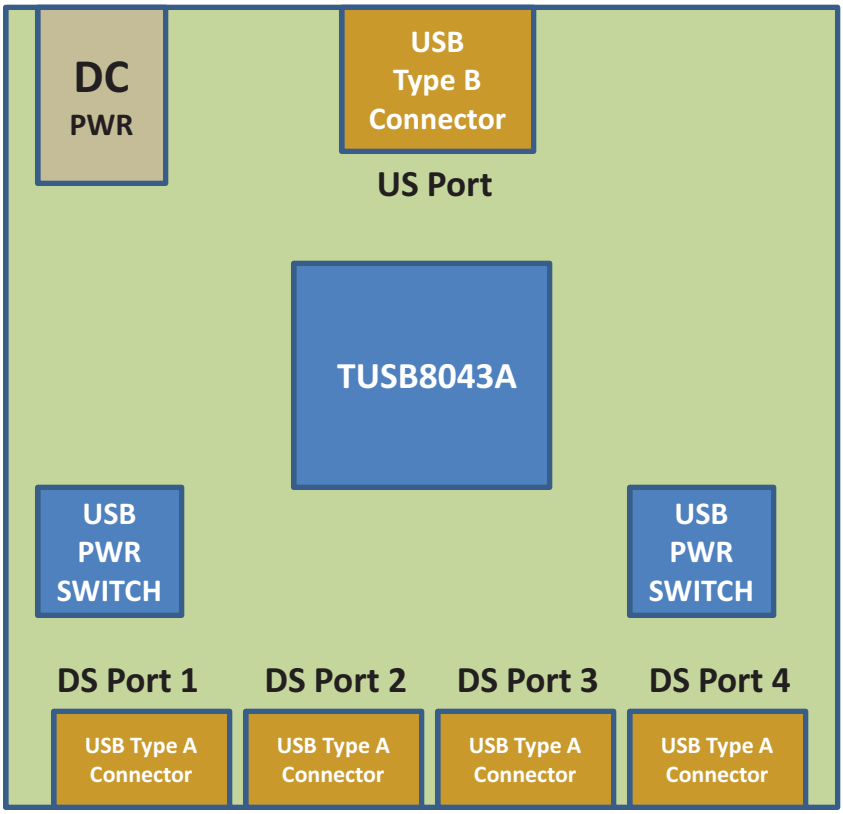

図 27. Discrete USB Hub Product

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Typical Application (continued)

9.2.1.1 Design Requirements

表 31. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD Supply	1.1 V
VDD33 Supply	3.3 V
Upstream Port USB Support (SS, HS, FS)	SS, HS, FS
Downstream Port 1 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 2 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 3 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 4 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Number of Removable external exposed Downstream Ports	4
Number of Non-Removable external exposed Downstream Ports	0
Full Power Management of Downstream Ports	Yes. (FULLPWRMGMTZ = 0)
Individual Control of Downstream Port Power Switch	Yes. (GANGED = 0)
Power Switch Enable Polarity	Active High. (PWRCTL_POL = 1)
Battery Charge Support for Downstream Port 1	Yes
Battery Charge Support for Downstream Port 2	Yes
Battery Charge Support for Downstream Port 3	Yes
Battery Charge Support for Downstream Port 4	Yes
I2C EEPROM Support	No
24MHz Clock Source	Crystal

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Upstream Port Implementation

The upstream of the TUSB8043A is connected to a USB3 Type B connector. This particular example has GANGED pin and FULLPWRMGMTZ pin pulled low which results in individual power support each downstream port. The VBUS signal from the USB3 Type B connector is feed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements

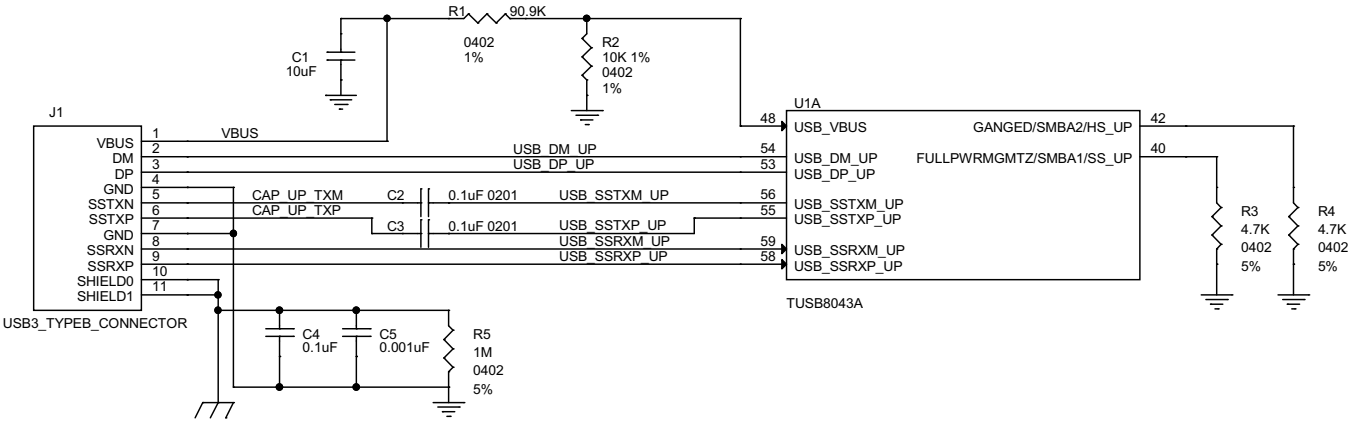

図 28. Upstream Port Implementation

9.2.1.2.2 Downstream Port 1 Implementation

The downstream port 1 of the TUSB8043A is connected to a USB3 Type A connector. With BATEN1 pin pulled up, Battery Charge support is enabled for Port 1. If Battery Charge support is not needed, then pull-up resistor on BATEN1 should be uninstalled.

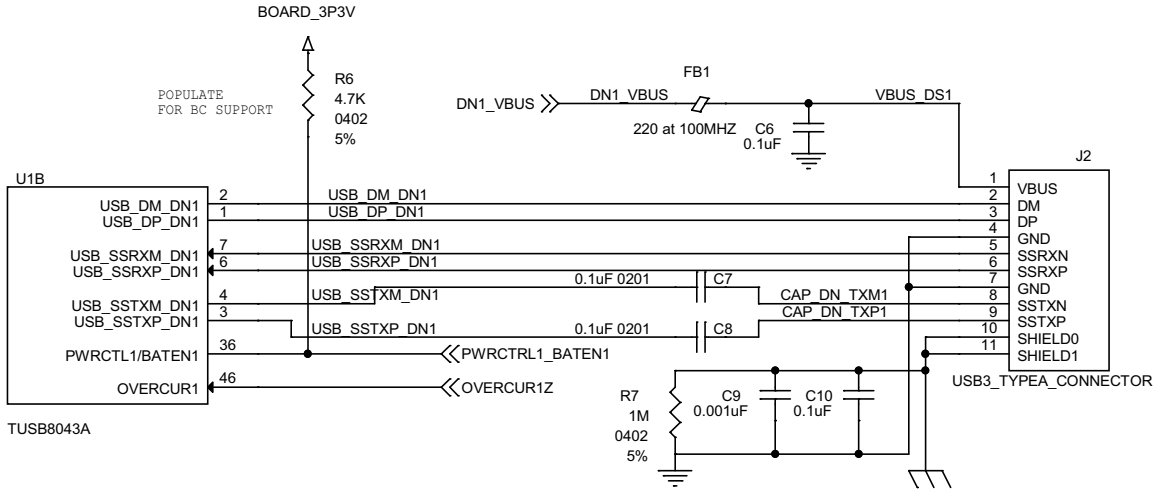

図 29. Downstream Port 1 Implementation

9.2.1.2.3 Downstream Port 2 Implementation

The downstream port 2 of the TUSB8043A is connected to a USB3 Type A connector. With BATEN2 pin pulled up, Battery Charge support is enabled for Port 2. If Battery Charge support is not needed, then pull-up resistor on BATEN2 should be uninstalled. For ferrite bead used on the VBUS connection, a lower resistance is recommended due to noticeable IR drop during high current charging modes. The isolation between the Type-A connectors shield ground and signal ground pins is not required. Some applications may have better ESD/EMI performance when the grounds are shorted together.

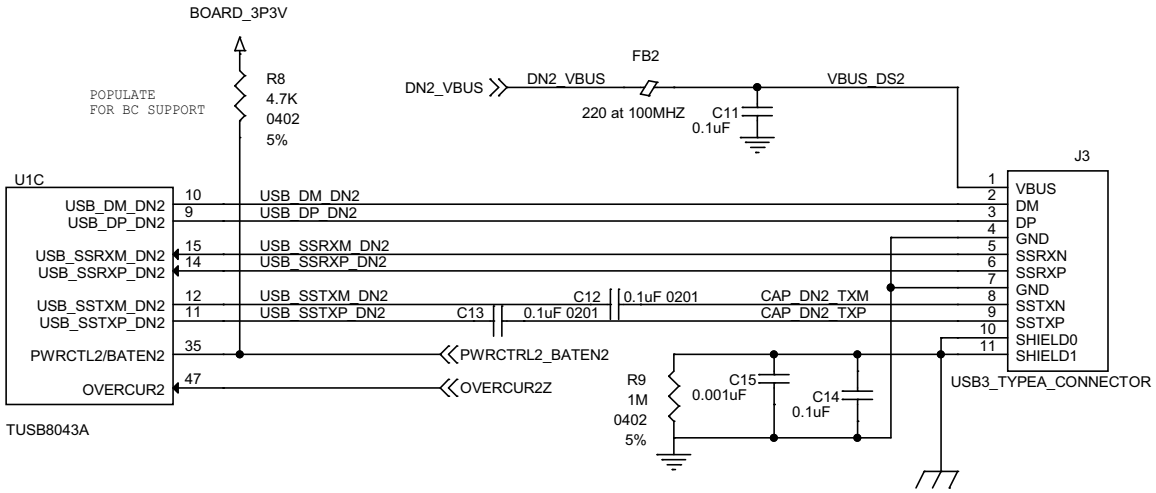

図 30. Downstream Port 2 Implementation

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9.2.1.2.4 Downstream Port 3 Implementation

The downstream port3 of the TUSB8043A is connected to a USB3 Type A connector. With BATEN3 pin pulled up, Battery Charge support is enabled for Port 3. If Battery Charge support is not needed, then pull-up resistor on BATEN3 should be uninstalled. For ferrite bead used on the VBUS connection, a lower resistance is recommended due to noticeable IR drop during high current charging modes. The isolation between the Type-A connectors shield ground and signal ground pins is not required. Some applications may have better ESD/EMI performance when the grounds are shorted together.

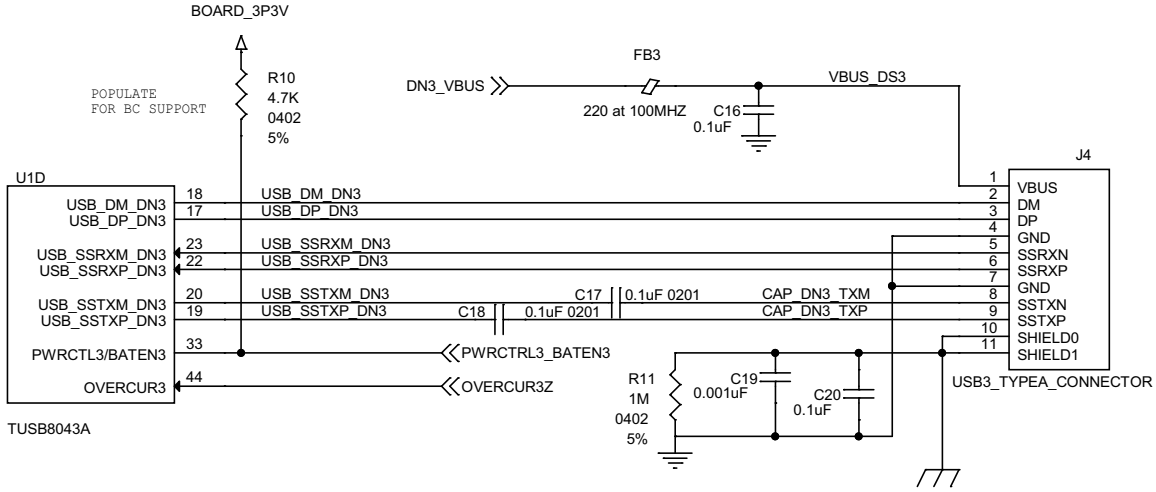

図 31. Downstream Port 3 Implementation

9.2.1.2.5 Downstream Port 4 Implementation

The downstream port 4 of the TUSB8043A is connected to a USB3 Type A connector. With BATEN4 pin pulled up, Battery Charge support is enabled for Port 4. If Battery Charge support is not needed, then pull-up resistor on BATEN4 should be uninstalled. For ferrite bead used on the VBUS connection, a lower resistance is recommended due to noticeable IR drop during high current charging modes. The isolation between the Type-A connectors shield ground and signal ground pins is not required. Some applications may have better ESD/EMI performance when the grounds are shorted together.

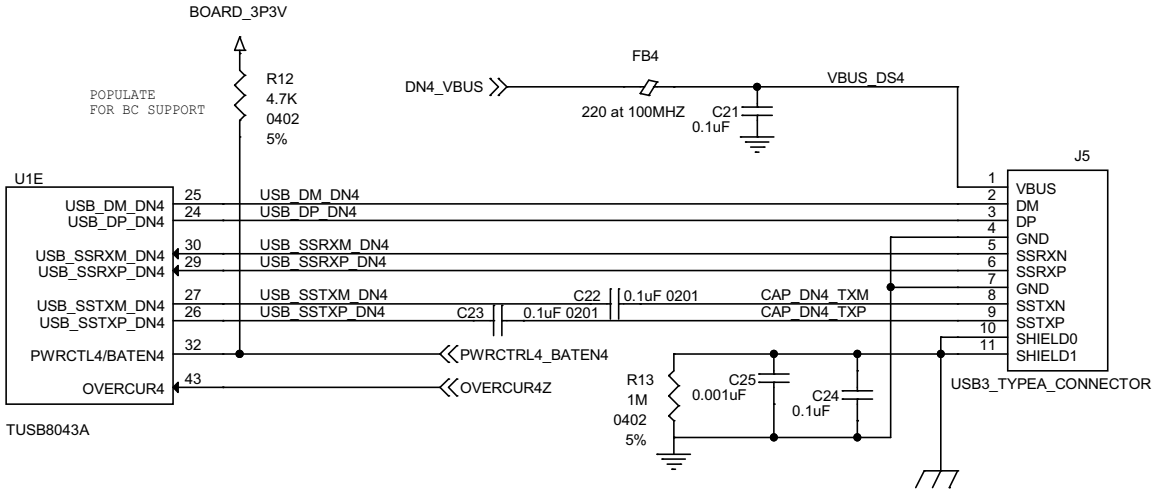

図 32. Downstream Port 4 Implementation

9.2.1.2.6 VBUS Power Switch Implementation

This particular example uses the Texas Instruments TPS2561 Dual Channel Precision Adjustable Current-Limited power switch. For details on this power switch or other power switches available from Texas Instruments, refer to the Texas Instruments website.

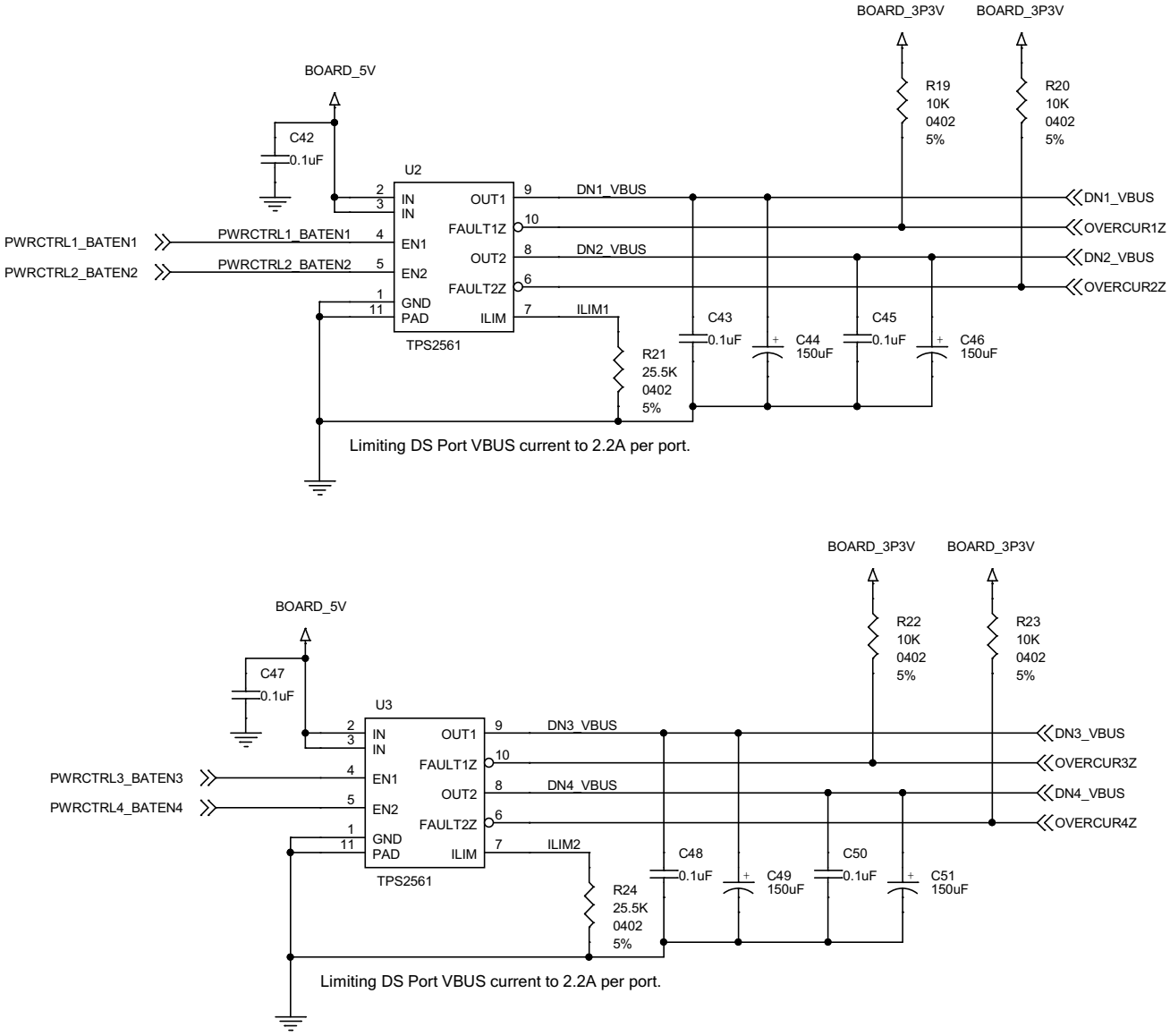

図 33. VBUS Power Switch Implementation

9.2.1.2.7 Clock, Reset, and Misc

The PWRCTL_POL is left unconnected which results in active high power enable (PWRCTL1, PWRCTL2, PWRCTL3, and PWRCTL4) for a USB VBUS power switch. SMBUSz pin is also left unconnected which selects I2C mode. Both PWRCTL_POL and SMBUSz pins have internal pull-ups. The 1 µF capacitor on the GRSTN pin can only be used if the VDD11 supply is stable before the VDD33 supply. The depending on the supply ramp of the two supplies the capacitor size may have to be adjusted.

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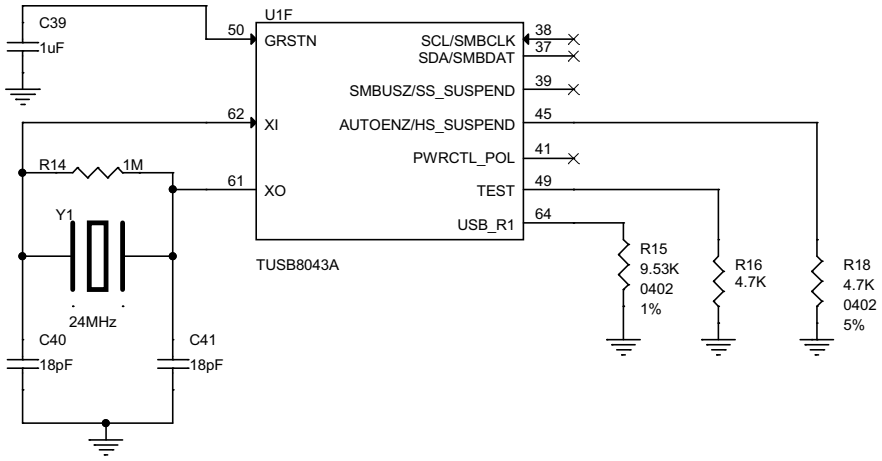

図 34. Clock, Reset, and Misc

9.2.1.2.8 TUSB8043A Power Implementation

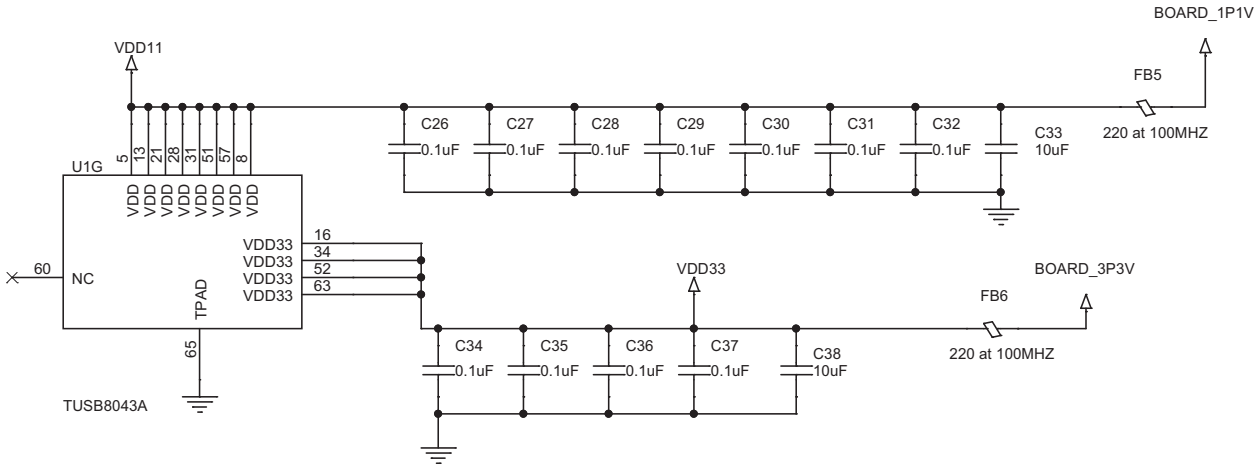

図 35. TUSB8043A Power Implementation

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9.2.1.3 Application Curves

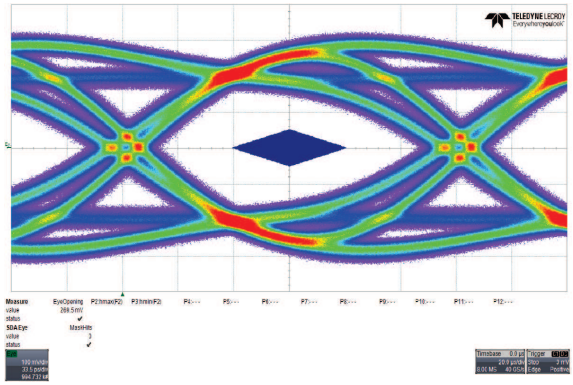

図 36. Upstream Port

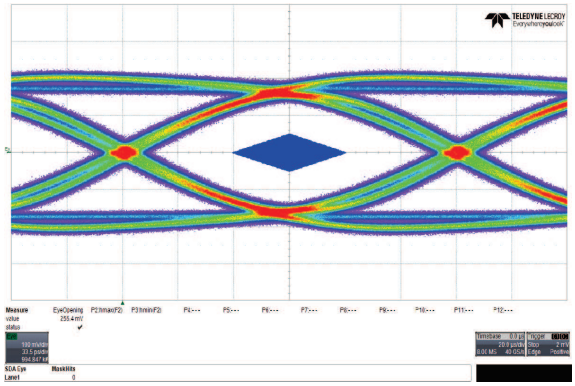

図 37. Downstream Port 1

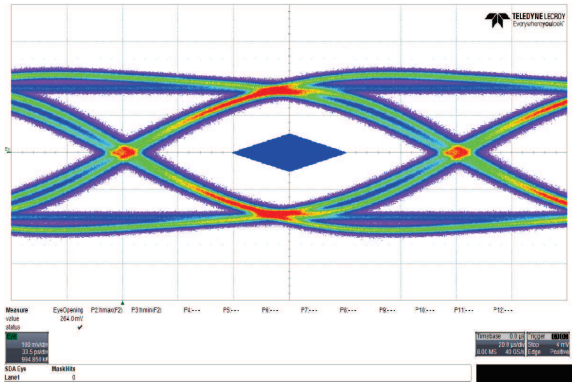

図 38. Downstream Port 2

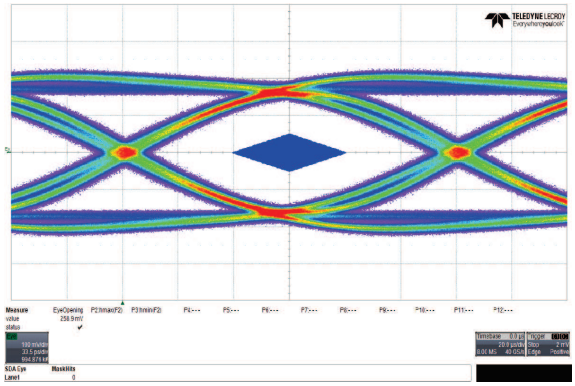

図 39. Downstream Port 3

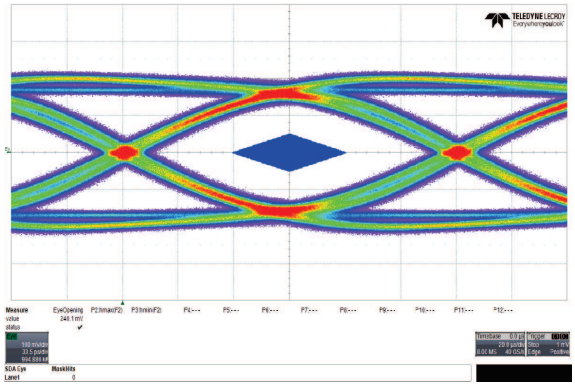

図 40. Downstream Port 4

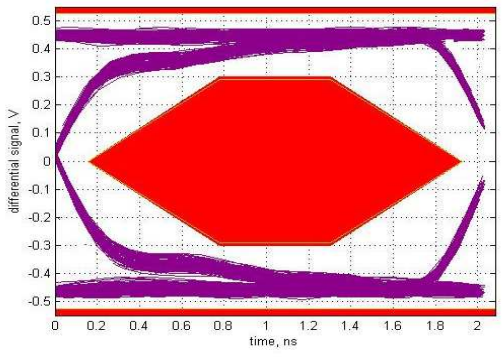

図 41. High-Speed Upstream Port

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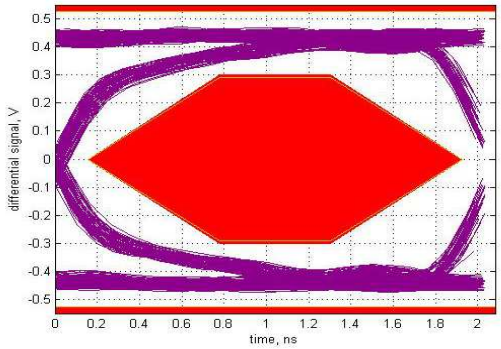

図 42. High-Speed Downstream Port 1

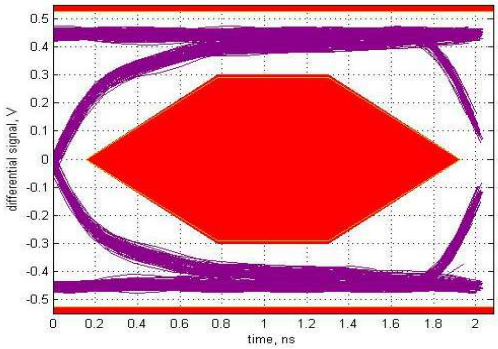

図 43. High-Speed Downstream Port 2

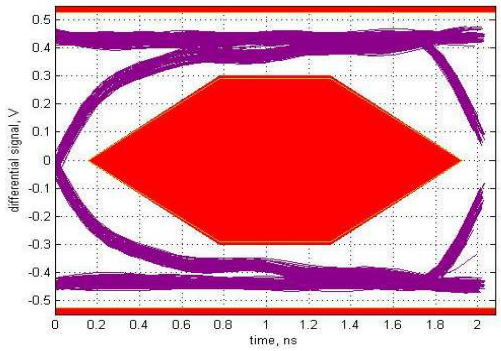

図 44. High-Speed Downstream Port 3

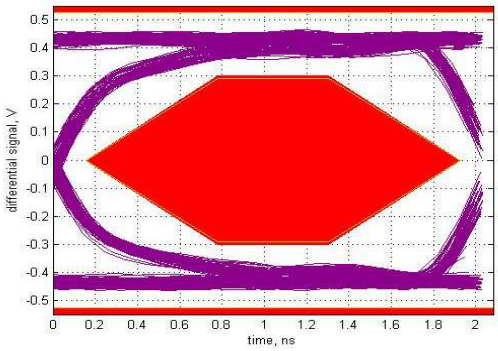

図 45. High-Speed Downstream Port 4

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10 Power Supply Recommendations

10.1 TUSB8043A Power Supply

V_{DD} should be implemented as a single power plane, as should V_{DD33}.

- The V_{DD} pins of the TUSB8043A supply 1.1 V (nominal) power to the core of the TUSB8043A. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the core voltage regulator may need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The V_{DD33} pins of the TUSB8043A supply 3.3 V power rail to the I/O of the TUSB8043A. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10 µF capacitor or 1 µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB8043A power pins as possible with an optimal grouping of two of differing values per pin.

10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5V and up to 900 mA per port. Downstream port power switches can be controlled by the TUSB8043A signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 µF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1µF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

10.3 Ground

It is recommended that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB8043A and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

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11 Layout

11.1 Layout Guidelines

11.1.1 Placement

1. 9.53K +/-1% resistor connected to pin USB_R1 should be placed as close as possible to the TUSB8043A.
2. A 0.1 µF should be placed as close as possible on each VDD and VDD33 power pin.
3. The 100 nF capacitors on the SSTXP and SSTXM nets should be placed close to the USB connector (Type A, Type B, and so forth).
4. The ESD and EMI protection devices (if used) should also be placed as close as possible to the USB connector.
5. If a crystal is used, it must be placed as close as possible to the TUSB8043A XI and XO pins.
6. Place voltage regulators as far away as possible from the TUSB8043A, the crystal, and the differential pairs.
7. In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.

11.1.2 Package Specific

1. The TUSB8043A package has a 0.5-mm pin pitch.
2. The TUSB8043A package has a 6.0-mm x 6.0-mm thermal pad. This thermal pad must be connected to ground through a system of vias.
3. All vias under device, except for those connected to thermal pad, should be solder masked to avoid any potential issues with thermal pad layouts.

11.1.3 Differential Pairs

This section describes the layout recommendations for all the TUSB8043A differential pairs: USB_DP_XX, USB_DM_XX, USB_SSTXP_XX, USB_SSTXM_XX, USB_SSRXP_XX, and USB_SSRXM_XX.

1. Must be designed with a differential impedance of 90 Ω ±10%.
2. In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width. Separating with ground as depicted in the layout example also helps minimize cross talk.
3. Route all differential pairs on the same layer adjacent to a solid ground plane.
4. Do not route differential pairs over any plane split.
5. Adding test points causes impedance discontinuity; and therefore, negative impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
6. Avoid 90 degree turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This minimizes any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SS differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
8. Match the etch lengths of the differential pair traces (i.e. DP and DM or SSRXP and SSRXM or SSTXP and SSTXM). There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
9. The etch lengths of the differential pair groups do not need to match (i.e. the length of the SSRX pair to that of the SSTX pair), but all trace lengths should be minimized.
10. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB8043A device.
11. To ease routing, the polarity of the SS differential pairs can be swapped. This means that SSTXP can be routed to SSTXM or SSRXM can be routed to SSRXP.

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Layout Guidelines (continued)

12. To ease routing of the USB2 DP and DM pair, the polarity of these pins can be swapped. If this is done, the appropriate Px_usb2pol register, where x = 0, 1, 2, 3, or 4, must be set.
13. Do not place power fuses across the differential pair traces.

11.2 Layout Examples

11.2.1 Upstream Port

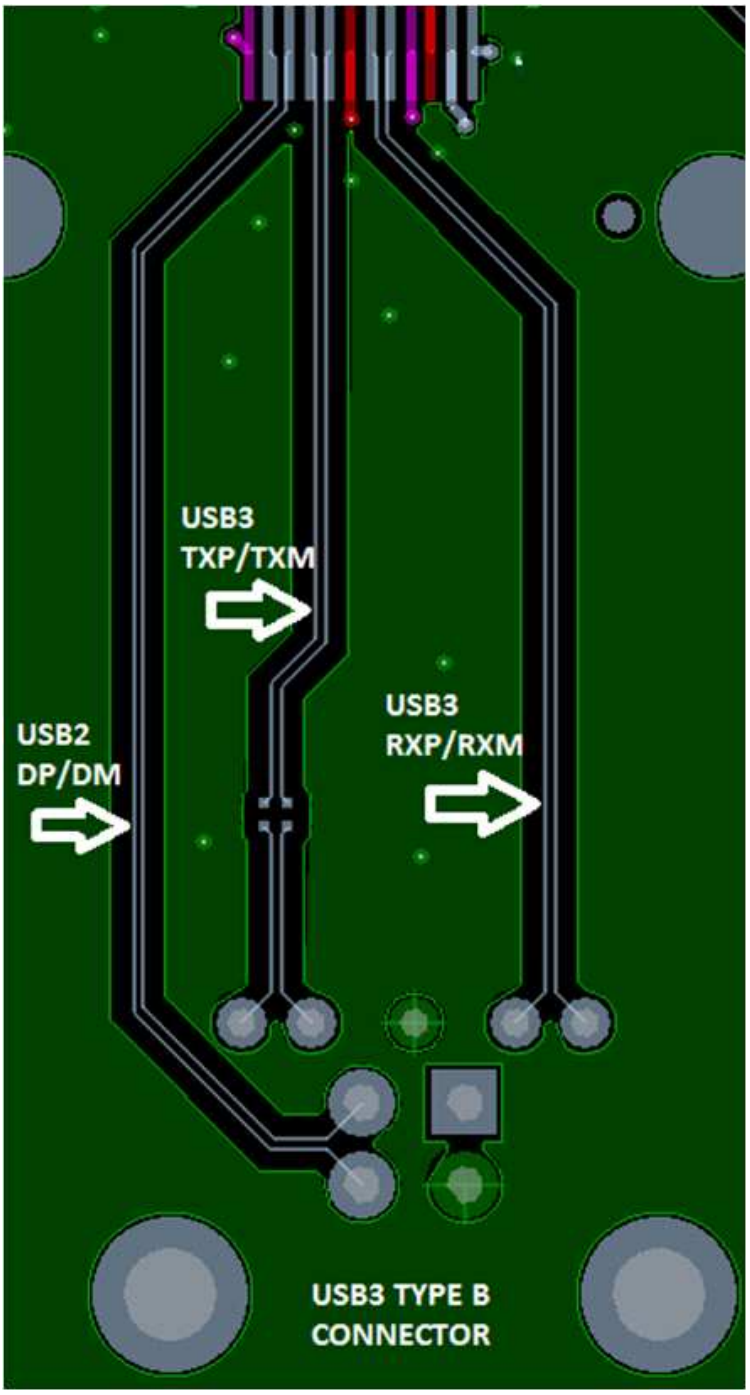

図 46. Example Routing of Upstream Port

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Layout Examples (continued)

11.2.2 Downstream Port

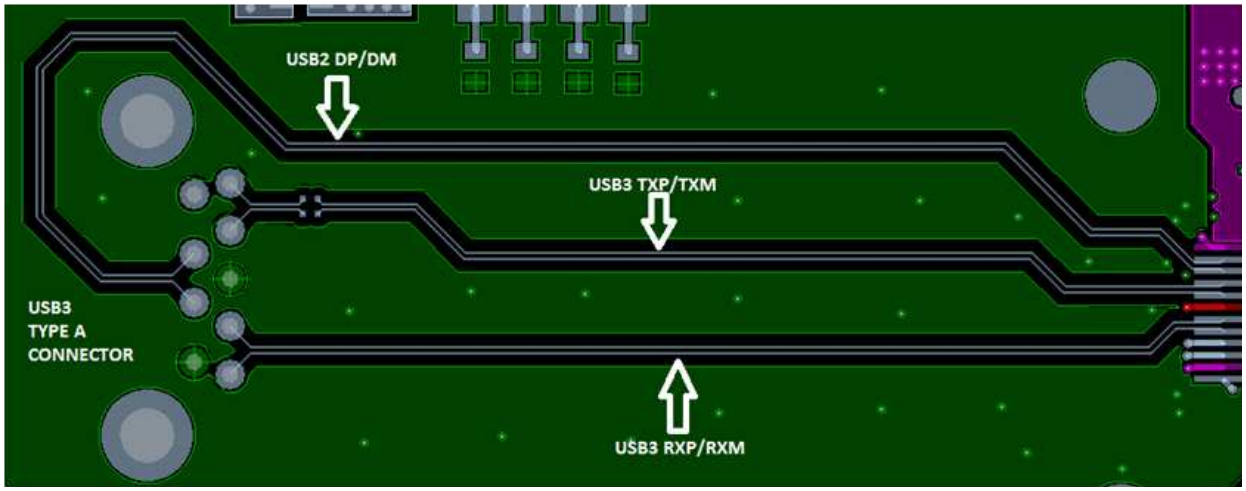

図 47. Example Routing of Downstream Port

The remaining three downstream ports routing can be similar to the example provided.

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB8043AIRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8043A
TUSB8043AIRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8043A
TUSB8043AIRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8043A
TUSB8043AIRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8043A
TUSB8043AIRGCTG4	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8043A
TUSB8043AIRGCTG4.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB8043A
TUSB8043ARGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8043A
TUSB8043ARGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8043A
TUSB8043ARGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8043A
TUSB8043ARGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8043A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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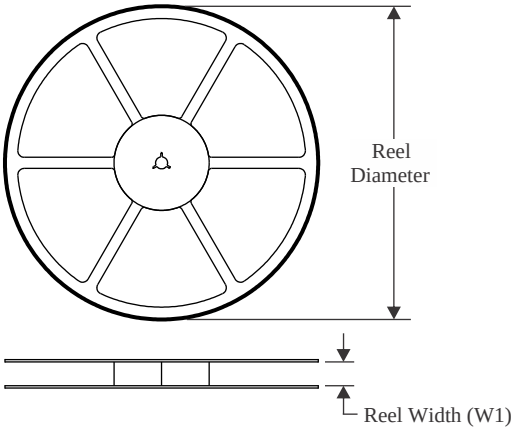
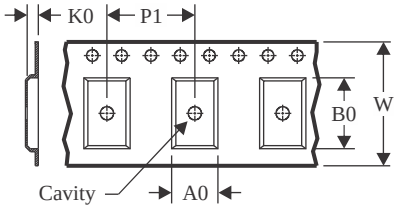
TAPE AND REEL INFORMATION

REEL DIMENSIONS

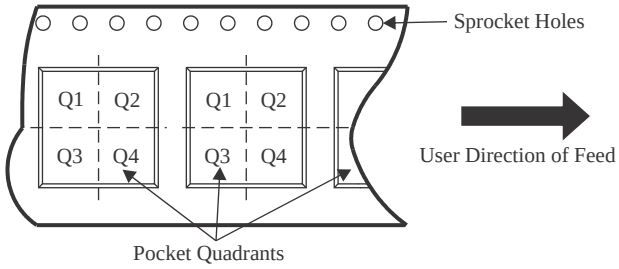


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

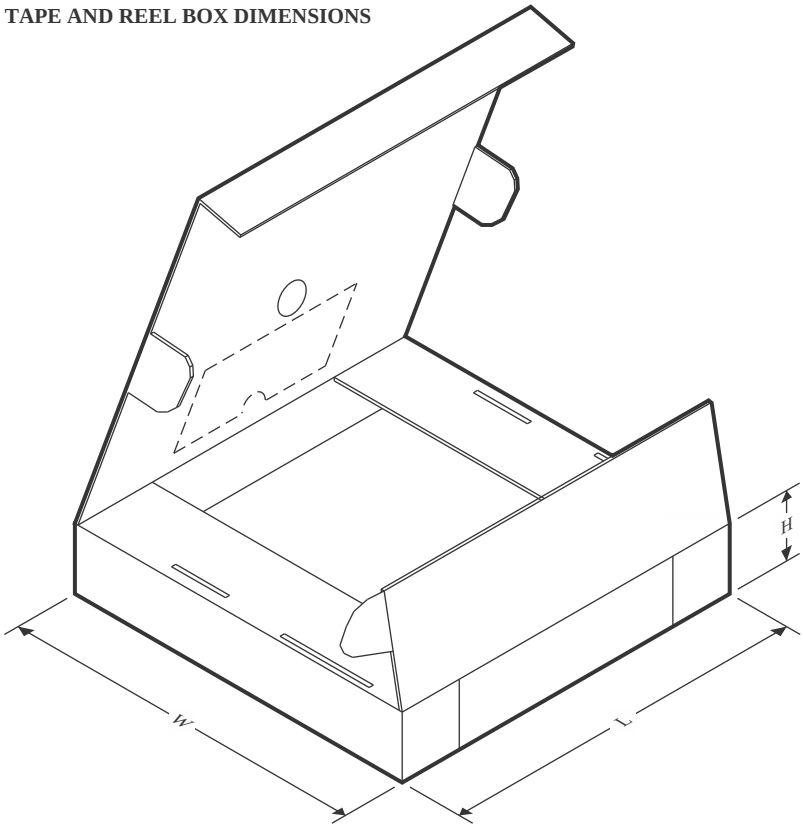
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB8043AIRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB8043AIRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB8043AIRGCTG4	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB8043ARGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB8043ARGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB8043AIRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
TUSB8043AIRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
TUSB8043AIRGCTG4	VQFN	RGC	64	250	210.0	185.0	35.0
TUSB8043ARGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
TUSB8043ARGCT	VQFN	RGC	64	250	210.0	185.0	35.0

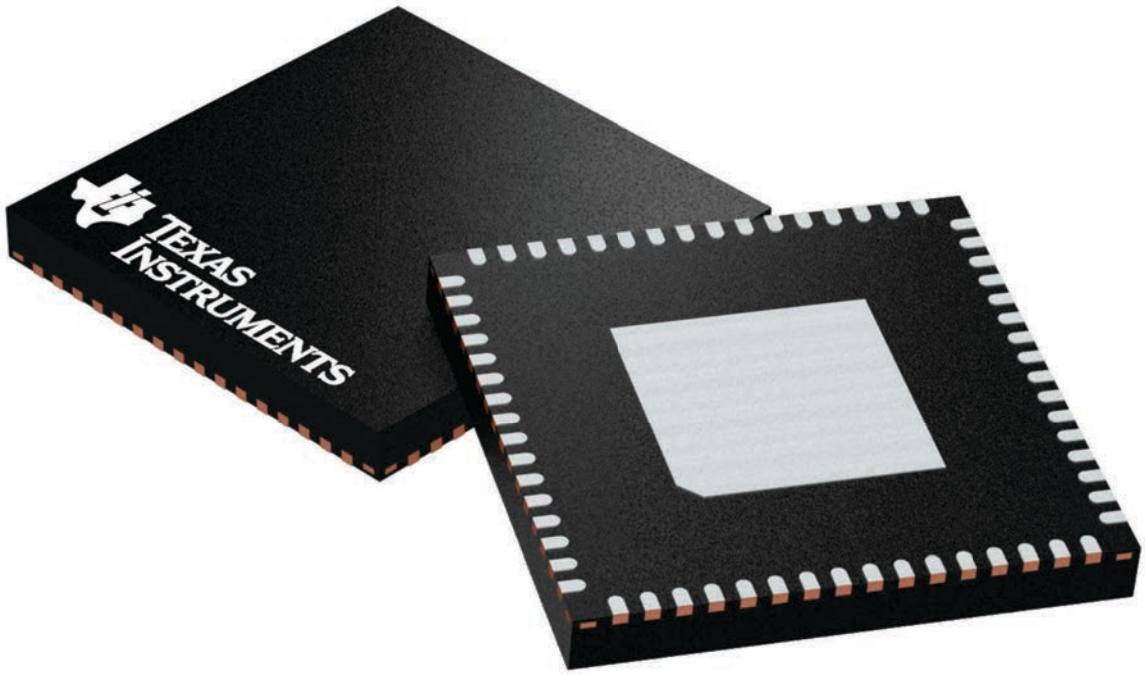
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

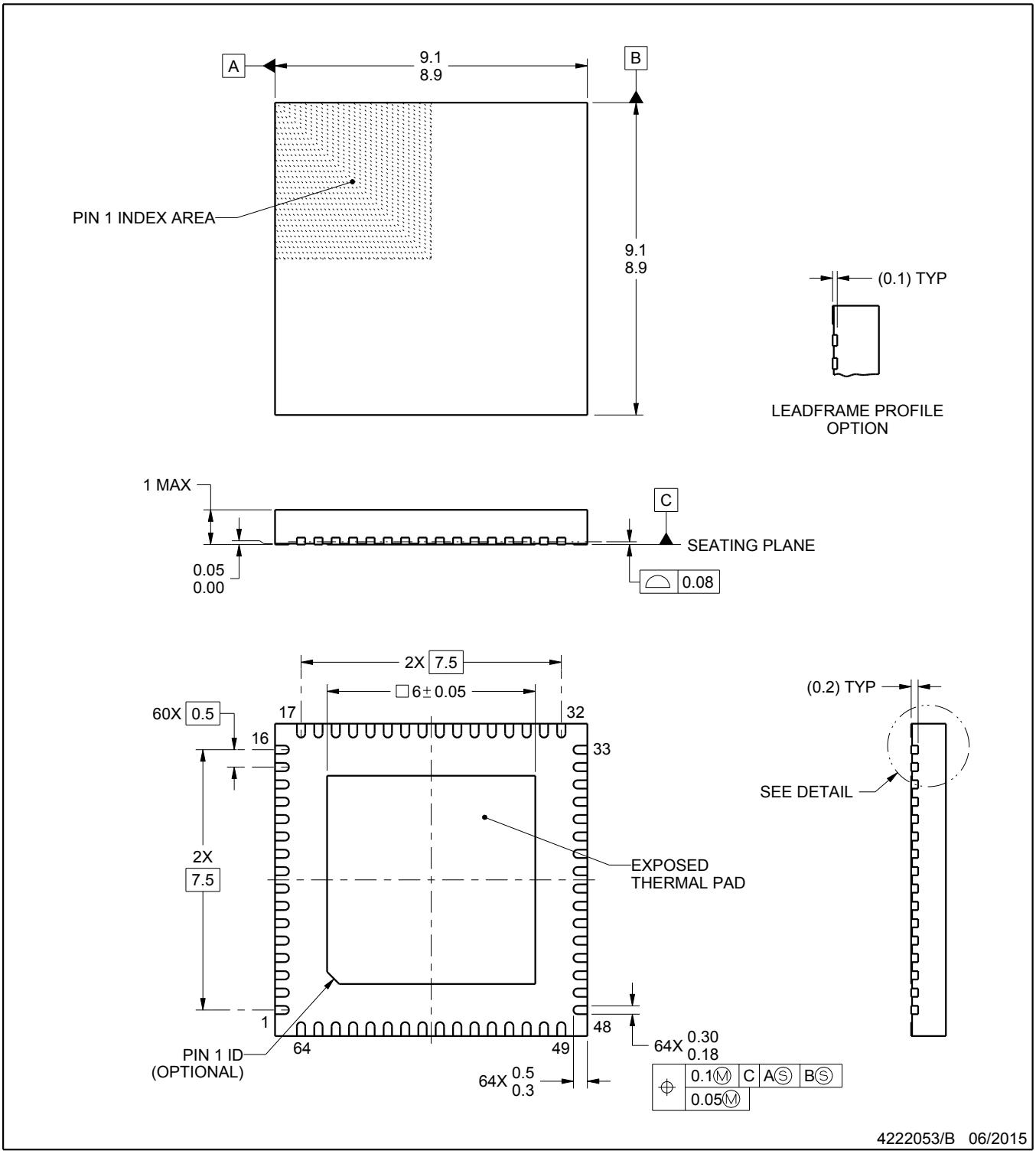
4224597/A

PACKAGE OUTLINE

RGC0064G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

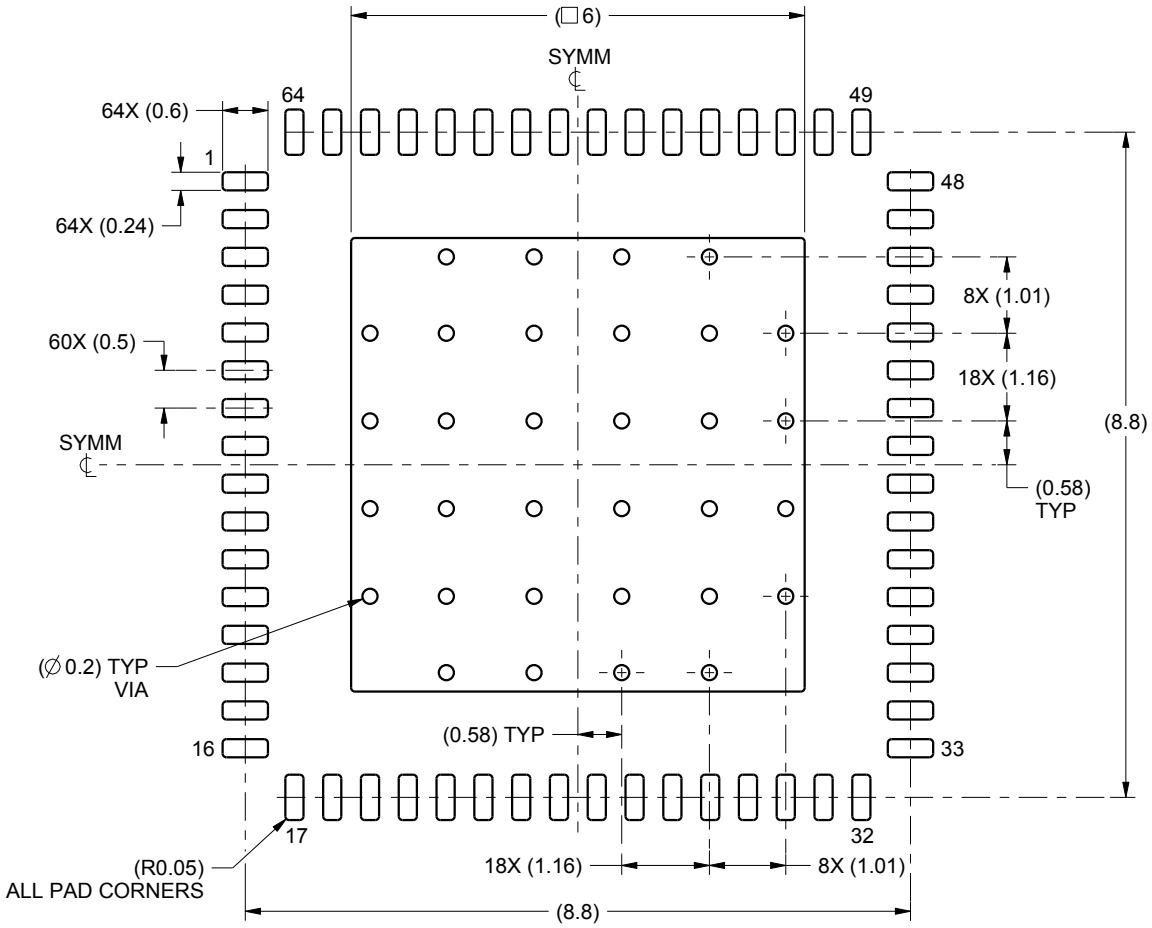
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

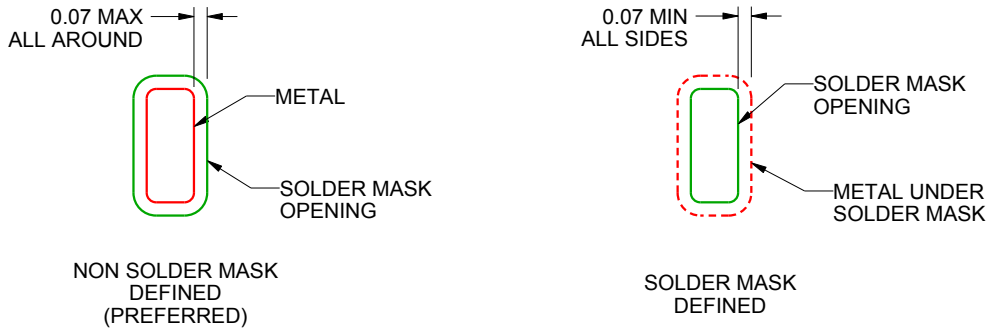
RGC0064G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:10X

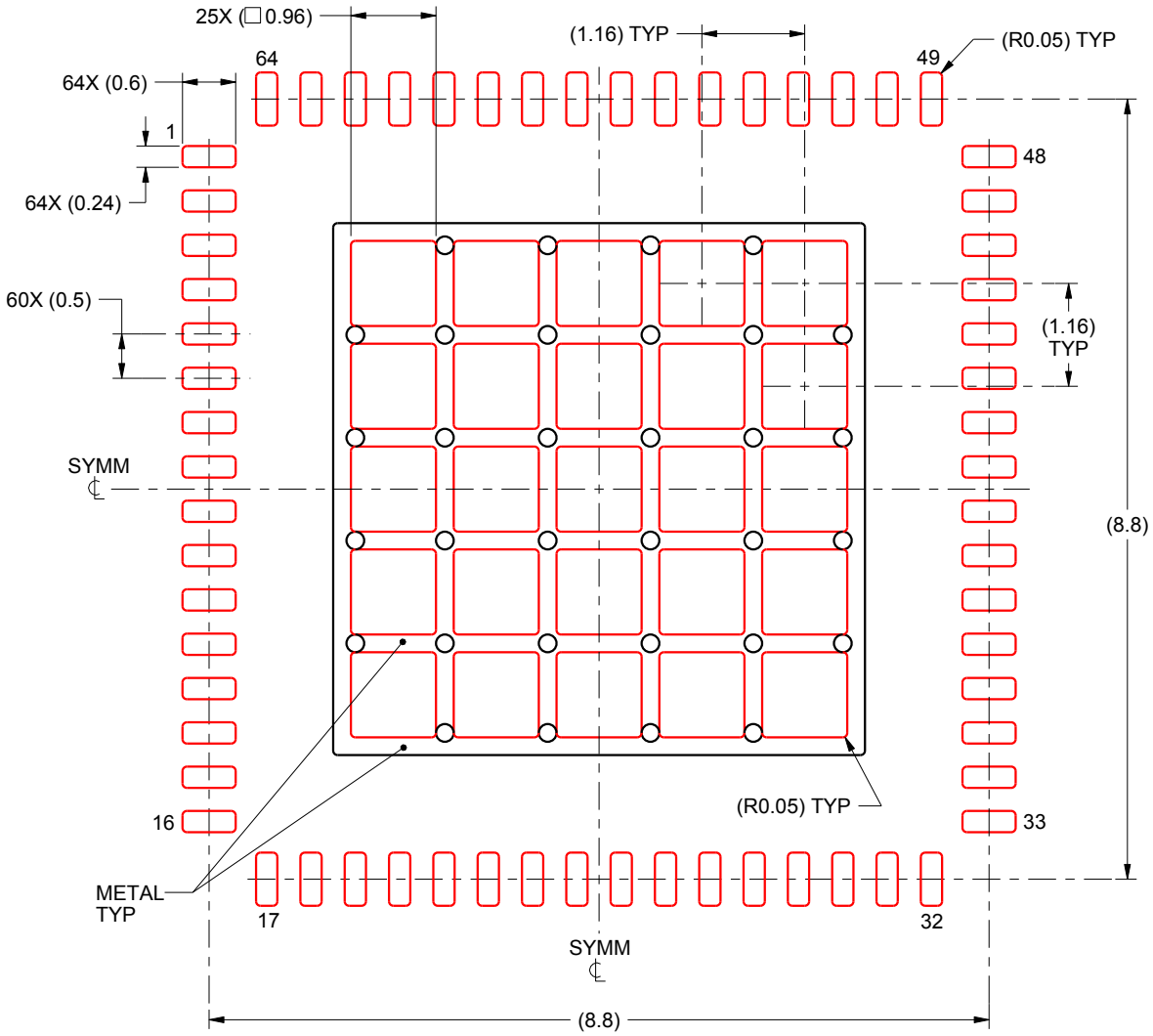


SOLDER MASK DETAILS

4222053/B 06/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
64% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4222053/B 06/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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