TUSS4440 対数アンプを内蔵した変圧器駆動超音波センサ IC

1 特長

- 超音波アプリケーションのための変圧器駆動トランスデューサ用ドライバとアナログ出力付きレシーバ段を内蔵
- 入力ダイナミック・レンジが 86dB のアナログ・フロントエンド
  - ゲインを 10、12.5、15、20V/V に調整可能な初段低ノイズ・アンプ
  - 40kHz～500kHz の構成可能なバンドパス・フィルタ
  - 広帯域の対数アンプ
- サポートするトランスデューサ周波数 (外部クロックで制御)
  - 40kHz～400kHz
- 低消費電力アプリケーションに対応
  - スタンバイ・モード:1.7mA (標準値)
  - スリープ・モード:220µA (標準値)
- 構成可能な駆動段
  - 変圧器を使用してトランスデューサを励起するための電流制限機能を備えた相補型ローサイド・ドライバ
  - IO1 および IO2 ピンを使用してバースト・パターンを構成可能
- 出力
  - VOUT:復調済みエコー・エンベロープの電圧出力
  - OUT3 ピン:入力信号のゼロクロス・コンパレータ出力
  - OUT4 ピン:プログラム可能な VOUT スレッショルドとの交差
- マイクロコントローラ (MCU) を使用して構成するためのシリアル・ペリフェラル・インターフェイス (SPI)

2 アプリケーション

- 位置センサ
- レベル・トランスミッタ
- 近接センサ

3 概要

TUSS4440 は、産業用超音波アプリケーション向けの変圧器駆動高集積アナログ・フロント・エンドです。トランスデューサ駆動段は、昇圧変圧器を使用して超音波トランスデューサを駆動するように構成できるローサイド相補型ドライバで構成されています。このデバイスは、変圧器の 1 次側に定電流を供給します。

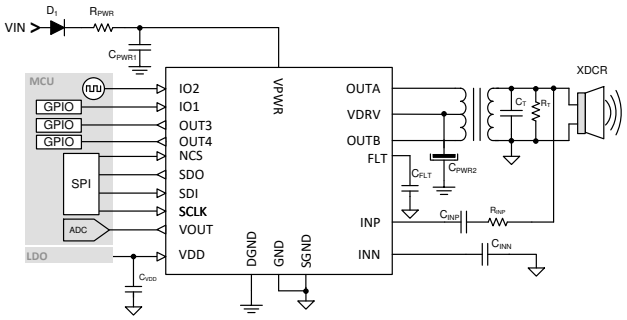
受信信号パスには、低ノイズ・リニア・アンプ、バンドパス・フィルタに続いて対数ゲイン・アンプが備わっているため、入力に応じた適切な増幅が可能です。この対数アンプのおかげで、弱いエコー信号に対して感度を高めることができ、反射エコーの全範囲にわたって優れた入力ダイナミック・レンジが得られます。

これらのドライバは、マイクロコントローラで直接制御してバースト信号を完全にカスタマイズすることも、カスタマイズ可能なバースト長を使用して SPI 経由でプログラムすることもできます。TUSS4440 は、バースト信号を送受信する 1 つのトランスデューサをサポートすることも、送信と受信の機能を分離する 2 つのトランスデューサを構成することもできます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TUSS4440	WQFN (20)	4.00mm × 4.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TUSS4440 アプリケーション図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Power-Up Characteristics ... 5
6.6 Transducer Drive ... 5
6.7 Receiver Characteristics ... 6
6.8 Echo Interrupt Comparator Characteristics ... 7
6.9 Digital I/O Characteristics ... 7
6.10 Switching Characteristics ... 8
6.11 Typical Characteristics ... 8
7 Detailed Description ... 11
7.1 Overview ... 11
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 20
7.5 Programming ... 21
7.6 Register Maps ... 23
8 Application and Implementation ... 29
8.1 Application Information ... 29
8.2 Typical Application ... 29
9 Power Supply Recommendations ... 36
10 Layout ... 37
10.1 Layout Guidelines ... 37
10.2 Layout Example ... 38
11 Device and Documentation Support ... 39
11.1 Receiving Notification of Documentation Updates ... 39
11.2 サポート・リソース ... 39
11.3 Trademarks ... 39
11.4 Electrostatic Discharge Caution ... 39
11.5 Glossary ... 39
12 Mechanical, Packaging, and Orderable Information ... 39

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2018) to Revision A (May 2022) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- SPI に言及している場合、すべての旧式の用語をコントローラおよびペリフェラルに変更 ... 1
- Changed operating free-air temperature minimum from: –25°C to: –40°C ... 4

Copyright © 2022 Texas Instruments Incorporated

5 Pin Configuration and Functions

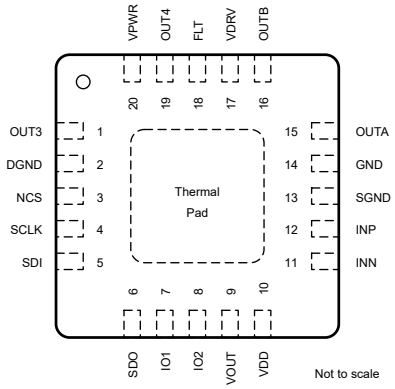


図 5-1. RTJ Package 20-Pin WQFN With Exposed Thermal Pad (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT3	I	General-purpose digital output
2	DGND	G	Digital ground
3	NCS	I	SPI negative chip select
4	SCLK	I	SPI CLK
5	SDI	I	SPI data input
6	SDO	O	SPI data output
7	IO1	I	General-purpose digital input
8	IO2	I	General-purpose digital input
9	VOUT	O	Demodulated echo analog output
10	VDD	P	Voltage regulator input
11	INN	I	Negative transducer receive
12	INP	I	Positive transducer receive
13	SGND	G	Sensor ground (quiet)
14	GND	G	Ground
15	OUTA	O	Transducer driver output A
16	OUTB	O	Transducer driver output B
17	VDRV	P	Center tap for transformer
18	FLT	I/O	Filter components
19	OUT4	O	General-purpose digital output
20	VPWR	P	Input supply voltage

(1) I = input, O = output, I/O = input and output, G = ground, P = power

Copyright © 2022 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{VPWR}	Supply voltage range	–0.3	40	V
V_{VDD}	Voltage regulator input voltage	–0.3	5.5	V
V_{VDRV}	Transformer center-tap voltage	–0.3	V_{VPWR} + 0.3	V
V_{FLT}	Filter component pin	–0.3	V_{VDD} + 0.3	V
V_{INX}	INP, INN pins input voltage	0.5	1.3	V
V_{DIG_IN}	SCLK, SDI, NCS, IOx pin input voltage	–0.3	V_{VDD} + 0.3	V
V_{VOUT}	Analog output voltage	–0.3	V_{VDD} + 0.3	V
V_{DIG_OUT}	SDO, OUTx, IOx pin output voltage	–0.3	V_{VDD} + 0.3	V
V_{OUTA_B}	OUTA, OUTB pins output voltage	–0.3	50	V
T_A	Ambient temperature	–40	105	°C
T_J	Junction temperature	–40	125	
T_{stg}	Storage temperature	–40	125	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VPWR}	Supply voltage on VPWR pin, internal regulation on VDRV enabled (VDRV_HI_Z=0)	5		36	V
	Supply voltage on VPWR pin, internal regulation on VDRV disabled (VDRV_HI_Z=1), VPWR connected to the center tap of the transformer[1]	5		24	V
V_{VDIG_IO}	Digital I/O pins	–0.1		V_{VDD}	V
V_{VDD}	Regulated voltage Input	3.1		5.5	V
I_{VPWR_INDIR}	Current consumption at VPWR pin during ranging	150	240	340	µA
I_{VPWR_STDBY}	Current consumption at VPWR in standby mode	50	110	200	µA
I_{VDD_INDIR}	Current consumption at VDD pin during ranging	7	11.5	13	mA
I_{VDD_STDBY}	Current consumption at VDD in standby mode	1.2	1.5	2.5	mA
I_{VDD_SLEEP}	Current consumption in sleep mode			350	µA
T_A	Operating free-air temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

(1) Always $V_{VPWR} > V_{VDRV}$ + 0.3 V to prevent reverse current from VDRV pin to VPWR pin

Copyright © 2022 Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		TUSS4440 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power-Up Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PWR_ON}	Time to power up when SPI communication is possible				10	ms
V_{VDRV}	Regulated voltage on VDRV pin[1]	VDRV_VOLTAGE_LEVEL = 0x0; $V_{VPWR} > V_{VDRV}$ + 100 mV	4.5	5	5.3	V
		VDRV_VOLTAGE_LEVEL = 0x4; $V_{VPWR} > V_{VDRV}$ + 100 mV	8.1	9	9.9	
		VDRV_VOLTAGE_LEVEL = 0x7; $V_{VPWR} > V_{VDRV}$ + 100 mV	11.5	12	12.6	
		VDRV_VOLTAGE_LEVEL = 0x8; $V_{VPWR} > V_{VDRV}$ + 100 mV	12.09	13	13.91	
		VDRV_VOLTAGE_LEVEL = 0xC; $V_{VPWR} > V_{VDRV}$ + 100 mV	15.81	17	18.9	
		VDRV_VOLTAGE_LEVEL = 0xD; $V_{VPWR} > V_{VDRV}$ + 100 mV	16.74	18	19.26	
		VDRV_VOLTAGE_LEVEL = 0xE; $V_{VPWR} > V_{VDRV}$ + 100 mV	17.67	19	20.33	
		VDRV_VOLTAGE_LEVEL = 0xF; $V_{VPWR} > V_{VDRV}$ + 100 mV	19.0	20	21.4	
I_{VDRV}	VDRV capacitor charging current	VDRV_CURRENT_LEVEL = 0x0; $V_{VPWR} > V_{VDRV}$ + 1 V	8.5	10	11.5	mA
		VDRV_CURRENT_LEVEL = 0x1; $V_{VPWR} > V_{VDRV}$ + 1 V	17	20	23	

(1) Other VDRV voltage levels possible.

6.6 Transducer Drive

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CLAMP}	Current clamping range		50		500	mA
I_{LIMIT_LOW}	Minimum value on OUTA/OUTB during bursting for linear operation of current limit (headroom)		2			V
I_{CLAMP_ADJ}	Current clamping adjustment steps			64		

6.7 Receiver Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{LNA}	Low-noise amplifier fixed gain	LNA_GAIN = 0x00; f_{DRV_CLK} = 58 KHz	13.7	15	16.8	V/V
G_{LNA}		LNA_GAIN = 0x01; f_{DRV_CLK} = 58 KHz	9.4	10	12	
G_{LNA}		LNA_GAIN = 0x10; f_{DRV_CLK} = 58 KHz	17.6	20	21.8	
G_{LNA}		LNA_GAIN = 0x11; f_{DRV_CLK} = 58 KHz	11.6	12.5	14.2	
DR_{VIN_MIN}	Minimum receive input(2)	LOGAMP_DIS_FIRST=0x0;LOGAMP_DIS_LAST=0x0 LNA_GAIN=0x00; ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500KHz		2.4		µVrms
DR_{VIN_MAX}	Maximum receive input(2)			48		mVrms
SL_{AFE}	Slope of analog front end(4)	VOUT_SCALE_SEL = 0x0; f_{DRV_CLK} = 58 KHz	25	29.7	33	mV/dB
		VOUT_SCALE_SEL = 0x1; f_{DRV_CLK} = 58 KHz	38	45.1	46	
DR_{AFE}	Receiver path dynamic range (minimum to maximum input) (2)	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	82		92	dB
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1 ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500 KHz	59		70	
	Receiver path dynamic Range (noise floor to maximum input) (3)	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		84	
BW_{LOG}	Logamp bandwidth	Information only	40		1000	KHz
INT_{LOG}	Intercept point in dBV	LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0; f_{DRV_CLK} = 40 KHz	-108		-97	dBV
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-94		-86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-80		-70	
ERR_{LOG}	Log conformance error	Information only	-3		3	dB
f_{BPF}	Configurable range of center frequency of BPF	BPF_BYPASS = 0x0; BPF_FC_TRIM = 0x0; set by different values of BPF_HPF_FREQ	40		500	KHz
Q_{BPF}	Q of bandpass filter	BPF_BYPASS = 0x0; BPF_Q_SEL = 0x0(1)	3	4	5.2	
R_{LPF}	Internal resistor on FLT pin to ground			6.25		KΩ
V_{O_PDSTL}	Output pedestal level(2)	V_{VDD} = 3.3 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	0.3		0.45	V
		V_{VDD} = 5.0 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0;LOGAMP_DIS_LAST = 0x0	0.45		0.675	

Copyright © 2022 Texas Instruments Incorporated

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N_pk_pk}$	Output peak-to-peak noise	V_{VDD}=3.3 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x0	50		200	mVpp
		V_{VDD}=5.0 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	75		300	

(1) Other choices of Q possible.
(2) Measured with effectively very large C_{FLT}. Actual minimum signal detectable will depend on $V_{N_pk_pk}$. Minimum and maximum input levels are defined by ERR_{LOG}.
(3) Measured with different C_{FLT} values according to 式 3. Noise floor is set by $V_{N_PK_PK}$ in addition to V_{O_PDSTL}.
(4) Slope measured with factory trim at f_{DRV_CLK} = 58 KHz. Slope can be adjusted with LOGAMP_SLOPE_ADJ bits for different f_{DRV_CLK} settings.

6.8 Echo Interrupt Comparator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT_SCALE_SEL = 0x0						
$V_{ECMP_THR_0}$	Echo interrupt comparator threshold(1)	ECHO_INT_THR_SEL = 0x0	0.37	0.4	0.43	V
		ECHO_INT_THR_SEL = 0x5	0.56	0.6	0.64	
		ECHO_INT_THR_SEL = 0xA	0.75	0.8	0.85	
		ECHO_INT_THR_SEL = 0xF	0.94	1	1.06	
$V_{ECMP_HYS_0}$	Echo interrupt comparator hysteresis		7		68	mV
VOUT_SCALE_SEL = 0x1						
$V_{E_CMP_THR_1}$	Echo interrupt comparator threshold(1)	ECHO_INT_THR_SEL = 0x0	0.56	0.6	0.64	V
		ECHO_INT_THR_SEL = 0x5	0.84	0.9	0.96	
		ECHO_INT_THR_SEL = 0xA	1.13	1.2	1.27	
		ECHO_INT_THR_SEL = 0xF	1.41	1.5	1.59	
$V_{ECMP_HYS_1}$	Echo interrupt output threshold level hysteresis		7		68	mV

(1) Other thresholds possible.

6.9 Digital I/O Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_DIGIO}	Digital input high-level	NCS, SDI, SCLK and IOx pins	0.7			V_{VDD}
V_{IL_DIGIO}	Digital input low-level				0.3	V_{VDD}
V_{HYS_DIGIO}	Digital input hysteresis		100			mV
V_{OH_DIGIO}	Digital output high-level(1)	SDO, OUTx pins; I_{DIGIO_OUT} = – 1 mA	V_{VDD} – 0.1			V
V_{OL_DIGIO}	Digital output low-level(1)	SDO, OUTx pins; I_{DIGIO_OUT} = 1 mA			0.1	V
V_{O_CAP}	Maximum output load capacitance	SDO pin. Information Only			10	pF
R_{PU_DIGIO}	Digital input pullup resistance to VDD	NCS, IO1, IO2 pins	80	100	130	kΩ
R_{PD_DIGIO}	Digital Input pulldown resistance to GND	SCLK, SDI pins	80	100	130	kΩ

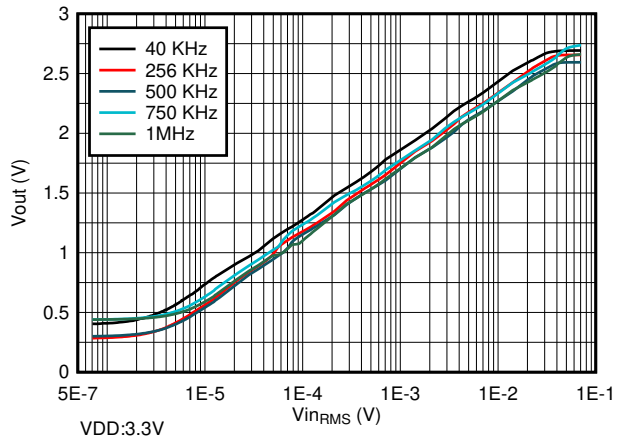
(1) No short-circuit protection on output pins. Damage may occur for currents higher than specified.

6.10 Switching Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

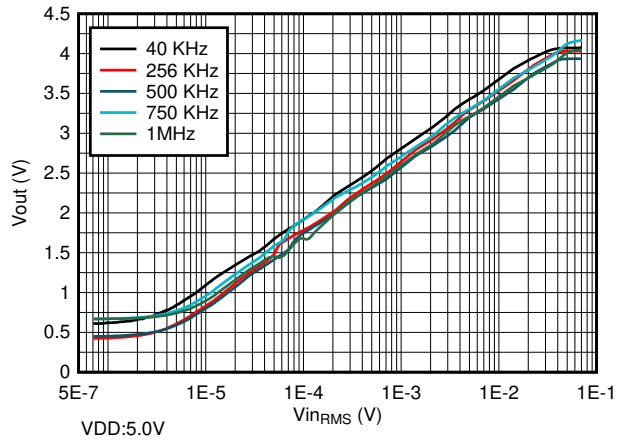
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{DRV_CLK}	Frequency of drive clock on IO1 and IO2 pin	Used as burst frequency	40		400	KHz
SPI_{RATE}	SPI bit rate				500	KHz

6.11 Typical Characteristics



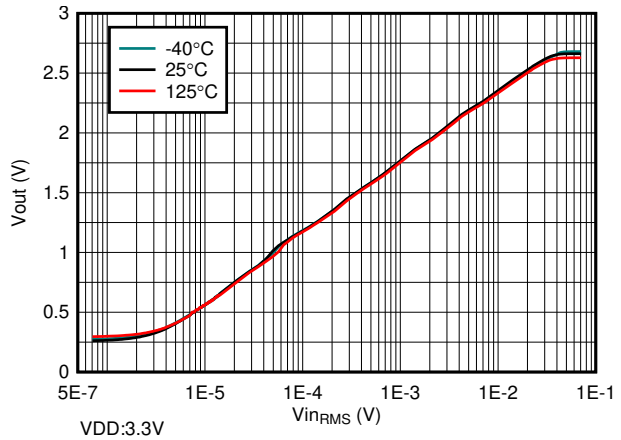
VDD:3.3V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

図 6-1. Receive Signal Path Transfer Function for VDD = 3.3 V



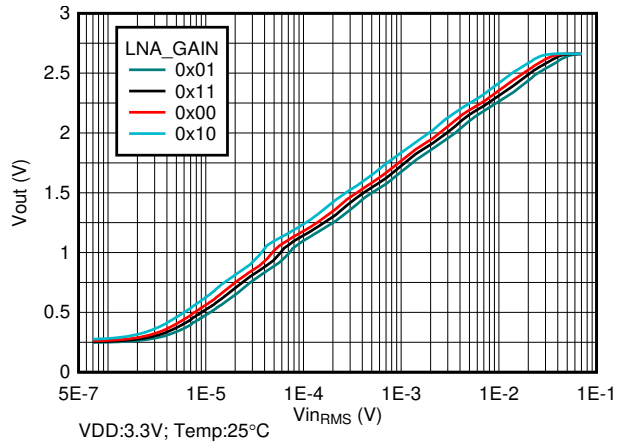
VDD:5.0V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x1
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

図 6-2. Receive Signal Path Transfer Function for VDD = 5 V



VDD:3.3V
F_c:256KHz
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

図 6-3. Receive Signal Path Transfer Function Across Temperature



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

図 6-4. Receive Signal Path Transfer Function Across LNA Gain

Copyright © 2022 Texas Instruments Incorporated

6.11 Typical Characteristics (continued)

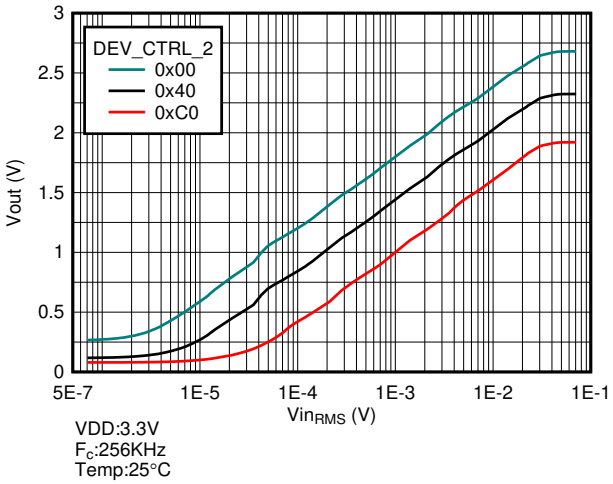


図 6-5. Receive Signal Path Transfer Function for Various Logamp Stages Disabled

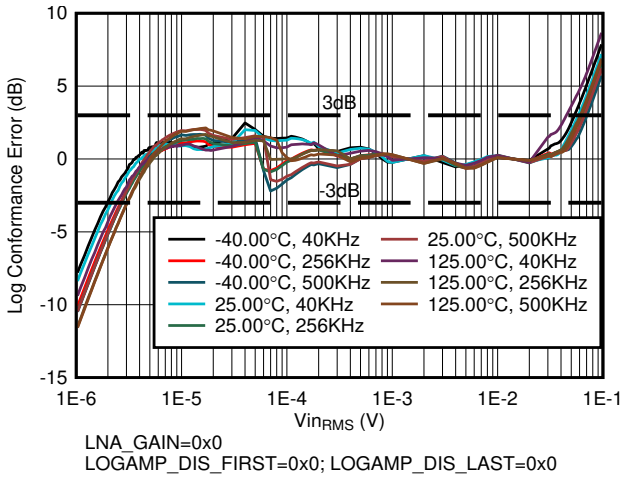


図 6-6. Receive Signal Path Log Conformance Error With All Stages Enabled

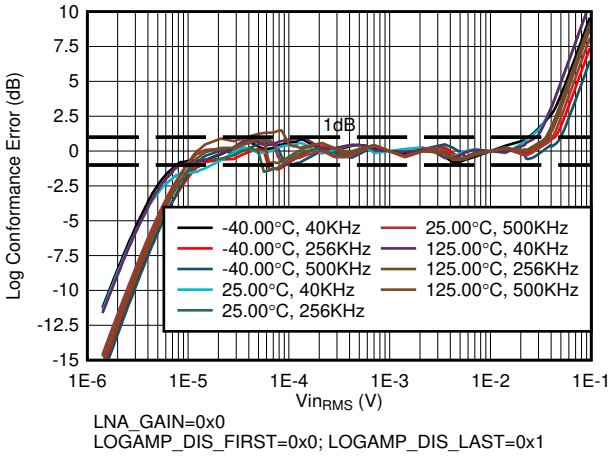


図 6-7. Receive Signal Path Log Conformance Error With Last Stage Disabled

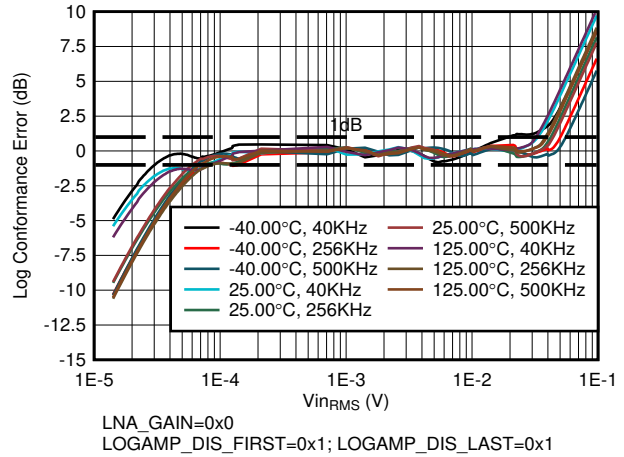


図 6-8. Receive Signal Path Log Conformance Error With First and Last Stage Disabled

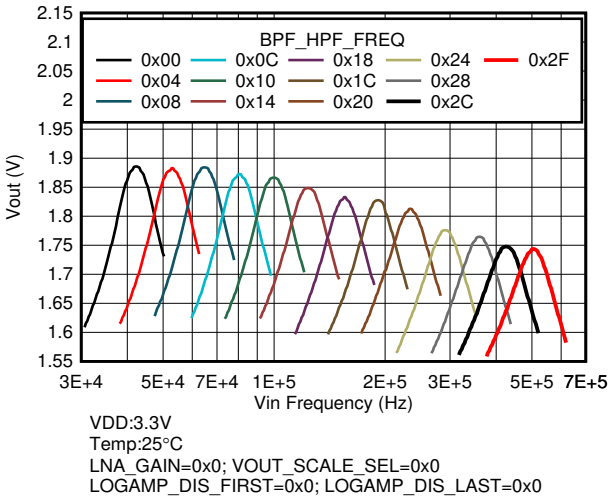


図 6-9. Receive Signal Path Bandpass Filter Transfer Function

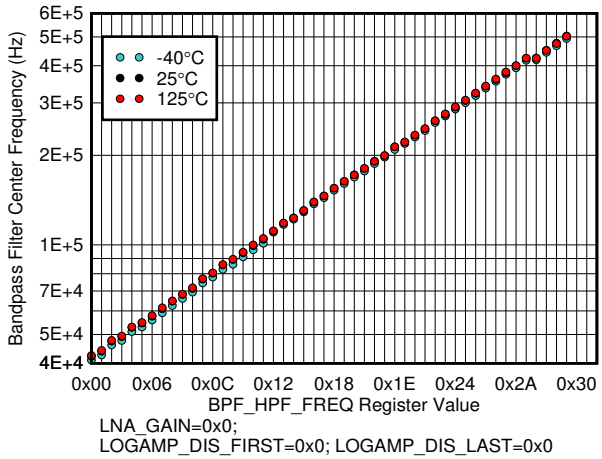


図 6-10. Receive Signal Path Bandpass Filter frequency for Various Register Settings

6.11 Typical Characteristics (continued)

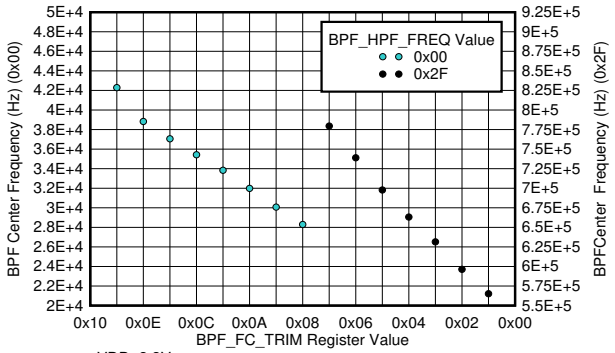


図 6-11. Receive Signal Path Bandpass Filter Center Frequency Trim

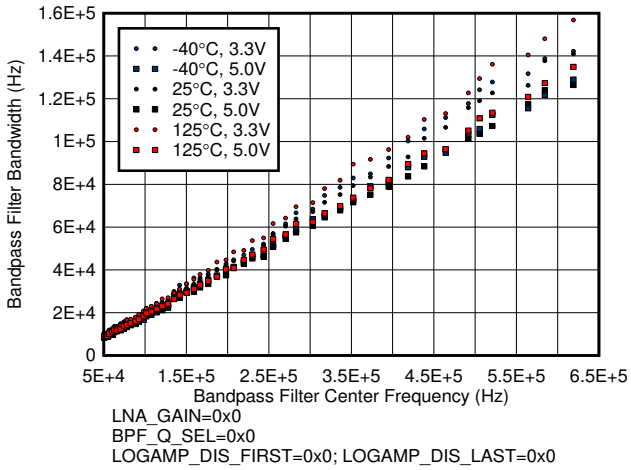


図 6-12. Receive Signal Path Bandpass Filter Bandwidth for Various Center Frequency Settings

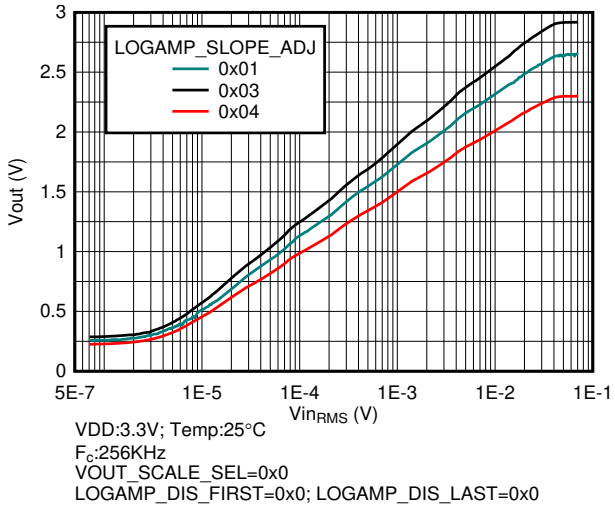


図 6-13. Receive Signal Path Transfer Function for Various Slope Adjustments

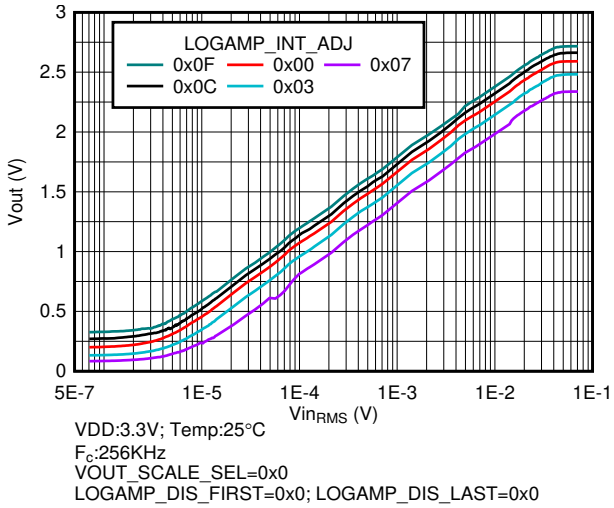


図 6-14. Receive Signal Path Transfer Function for Various Intercept Adjustments

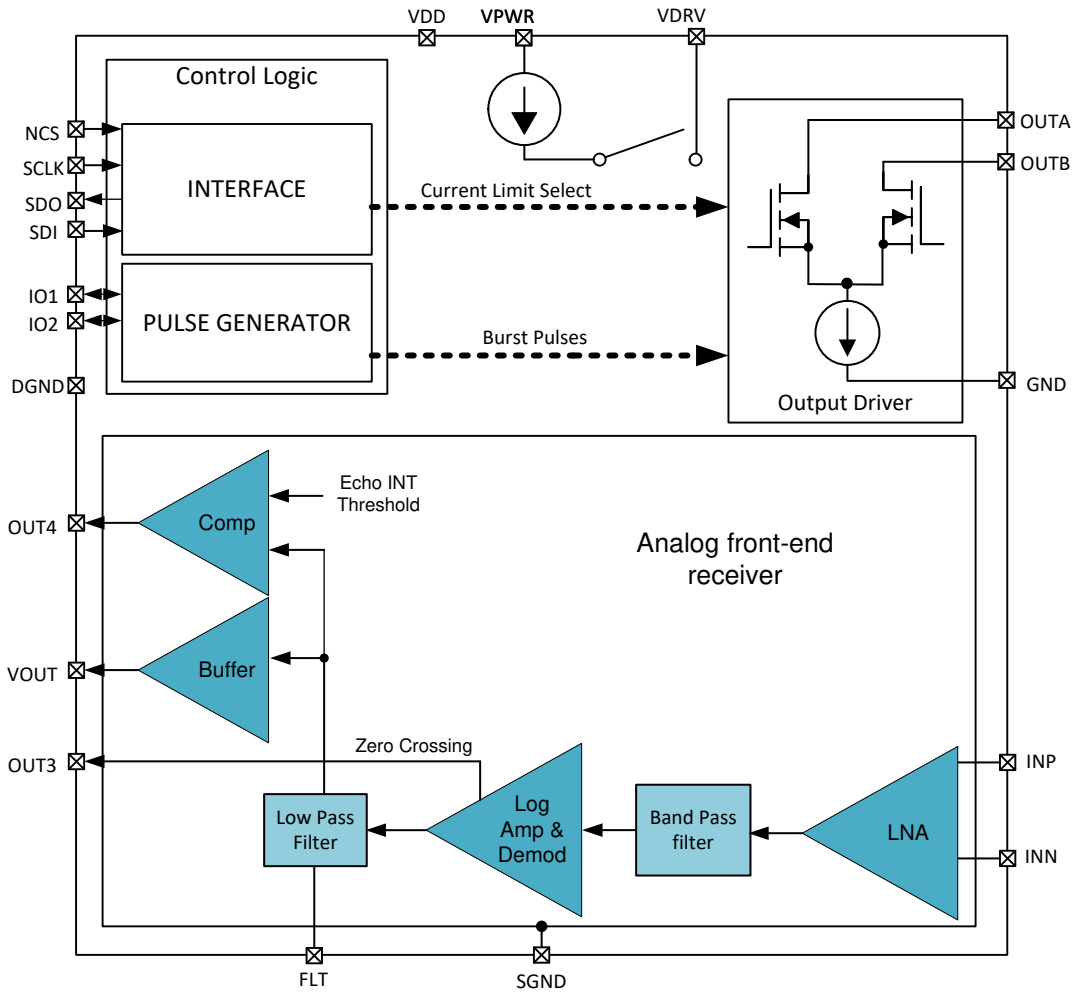
Copyright © 2022 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The TUSS4440 is a highly integrated driver and receiver IC designed especially for ultrasonic transducers operating between the range of 40 KHz to 1 MHz. The TUSS4440 integrates low-side complimentary FETs that can excite a ultrasonic transducer through a transformer. The transformer allows the user to step up the driving voltage to get higher sound pressure level. The The driver stage has flexible and configurable controls set through the SPI interface or through digital input pins that can be driven by an external MCU. The receive stage consists of a logarithmic amplifier receive chain. The logamp enables the TUSS4440 to have a wide dynamic input range. This enables applications where objects with different physical properties must be detected with the same sensor. A key advantage of the TUSS4440 is that it integrates a bandpass filter that can be tuned to the center frequency of the transducer. A demodulated analog output representing the receive echo, the zero crossing of the input signal, and a simple threshold crossing indicator enable a variety of end applications from complex object detection to simple presence detection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excitation Power Supply (VDRV)

The TUSS4440 device includes a current source which charges a capacitor connected to the VDRV pin. The VDRV pin serves as the power supply for the center tap of the transformer . The voltage on the VDRV pin (V_{VDRV}) is controlled by an internal voltage monitor which can be configured by the VDRV_VOLTAGE_LEVEL

bits. The current source is switched off after VDRV pin voltage crosses the configured V_{VDRV} value. The charging current (I_{VDRV}) can be configured using VDRV_CURRENT_LEVEL bits.

The use of VDRV pin has two advantages:

- It allows device to be used in applications where VPWR values can violate absolute maximum parameter for the OUTA / OUTB pins.
- In applications where VPWR can vary over a wide range, this allows the transducer drive voltage to be fixed for every burst for a deterministic sound pressure level created by the transducer. This is possible only when the minimum supply voltage on the VPWR pin is greater than the configured value of V_{VDRV}

The VDRV regulation is disabled at device power up indicated by VDRV_HI_Z bit being set. To enable VDRV this bit must be cleared. This feature enables applications where the center tap of transformer is connected to a separate power supply source.

Note

- When VDRV pin is supplied from an external power supply, it must be ensured that all times including during power up, $V_{VPWR} > V_{VDRV} + 0.3$ V to prevent any reverse current from VDRV pin to VPWR pin. Alternatively a reverse current prevention diode can be used on VPWR pin as shown in 図 8-1 (D1).
- Very fast ramp-up rate on VPWR pin should be avoided to prevent damage to the device. If fast ramp rates are possible, a series resistor between power supply and VPWR pin as shown in 図 8-1 (R_{PWR}) is recommended.

After a burst is completed and during the long receive time (listen mode), the capacitor on VDRV pin will discharge causing the charging current to turn on intermittently. This can inject switching noise which can be picked by the analog front end as a spurious echo. To eliminate this noise, the DIS_VDRV_REG_LSTN bit can be set. This disables charging of VDRV automatically after the burst is done. The VDRV charging current can be turned on again by setting the VDRV_TRIGGER bit. Setting this bit may create a spurious echo which can be ignored by the echo processing in the MCU. The VDRV_READY bit in DEV_STAT register can be monitored to know when the required voltage level has been reached and the device is ready to generate a new burst. The VDRV_TRIGGER bit must be un-set through SPI just before the start of burst and will have to be set again for next charging cycle. If the VDRV_TRIGGER bit is not un-set before next burst cycle, the VDRV charging current will not be automatically disabled after the burst even when DIS_VDRV_REG_LSTN is set. This functionality is ignored when the VDRV_HI_Z bit is set.

7.3.2 Burst Generation

TUSS4440 has multiple modes to excite the transducer through OUTA and OUTB pins. For each of the modes, the desired frequency of burst is supplied through an external clock on the IOx pins. This enables the user to supply a highly precise clock calibrated to the center frequency of transducer to enable the highest sound pressure level generation. These modes can be selected by the IO_MODE bits in the DEV_CTRL_3 register.

The burst mode is enabled first, then the start of burst (OUTA/OUTB changing states) happens at the next falling edge of IO1 or IO2, depending on the mode selected. These modes are described below.

- **IO_MODE = 0:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled by setting the CMD_TRIGGER in the TOF_CONFIG register through SPI, as shown in 図 7-1. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. The end of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent, or when the CMD_TRIGGER = 0 is set through SPI, whichever occurs earlier. TI recommends that IO2 is held high before burst enable to count the number of pulses correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. A transition of CMD_TRIGGER from high to low to high again is required to initiate a new burst sequence.

Copyright © 2022 Texas Instruments Incorporated

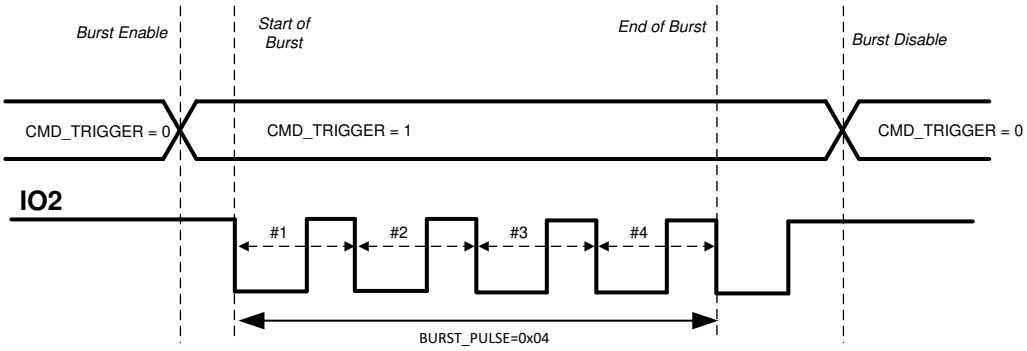


図 7-1. IO_MODE 0 Description

- **IO_MODE = 1:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled when IO1 pin transitions low (see 図 7-2). The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent or IO1 transitions high, whichever occurs earlier. TI recommends that IO2 is held high before start of burst to count the number of pulse correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. A transition of IO1 from low to high to low again is required to initiate a new burst sequence.

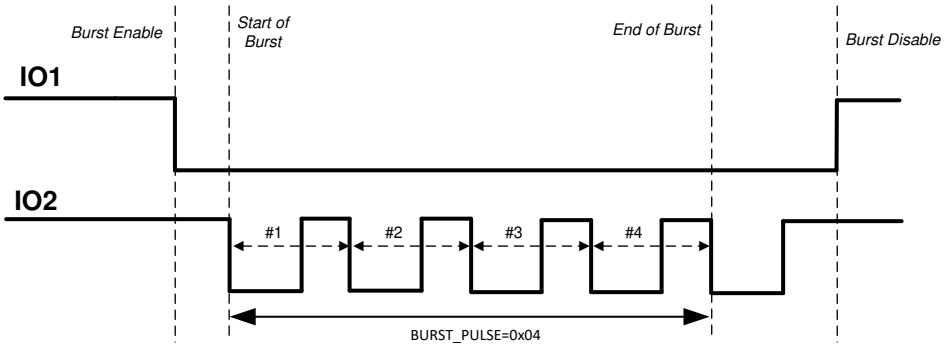


図 7-2. IO_MODE 1 Description

- **IO_MODE = 2:** In this mode both IO1 and IO2 are used to control OUTA and OUTB. The burst enable is triggered when either IO1 or IO2 transitions from high to low. Start of burst (OUTA and OUTB changing state) happens only at the next falling edge of IO1. 図 7-3 shows the case where a high-to-low transition on IO2 is used to enable the burst. A burst is emulated when IO1 and IO2 are toggled in a non-overlapping sequence. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. During a burst, if there is a condition where both IO1 and IO2 are high for more than half period of the internal clock f_{INT_CLK} (caused by differential delays due to PCB parasitics or MCU code), an end of burst and burst mode disable will be triggered. Any falling edge just after this condition will be ignored to toggle OUTA and OUTB as it would be considered as a new burst enable signal. A systematic condition of overlap can cause a continuous end of burst trigger such that OUTA and OUTB do not toggle even though IO1 and IO2 are toggling. TI recommends no overlap or minimum non-overlap between the IO1 and IO2 signals when measured at the pins. BURST_PULSE has no effect in this mode.

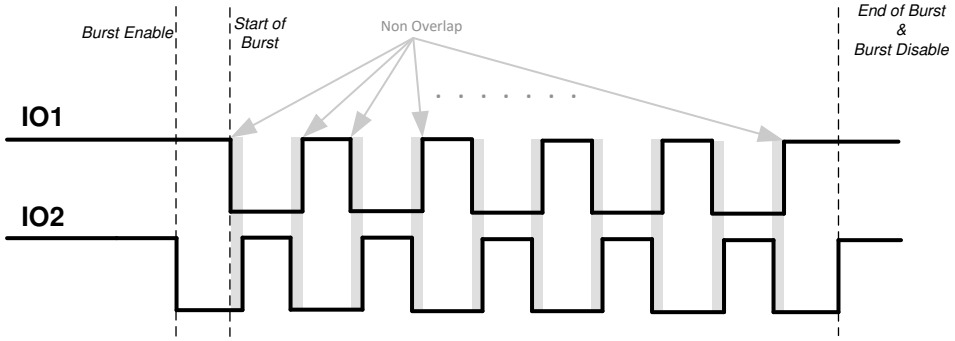


図 7-3. IO_MODE 2 Description

- **IO_MODE = 3:** In this mode, burst enable and start of burst are both triggered by the falling edge of IO2. TI recommends that IO2 pin is kept pulled up to VDD for this mode. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins (see 図 7-4). The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent. After end of burst, a blank-out timer interval defined by the DRV_PLS_FLT_DT register is started to prevent triggering of a new start of burst in the event if the IO2 pin is still toggling. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins.

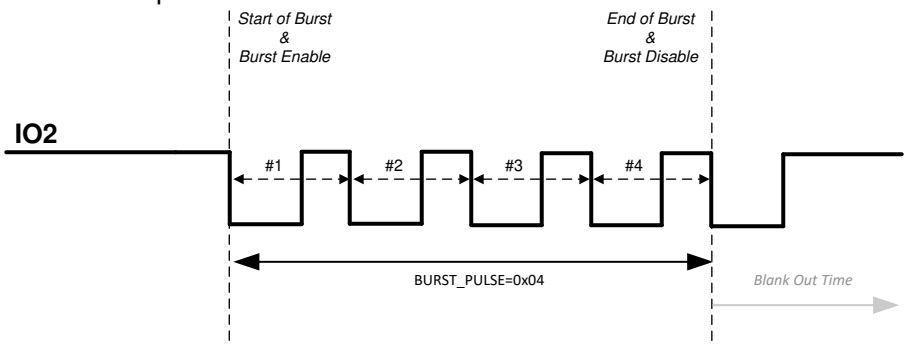


図 7-4. IO_MODE 3 Description

Note

- For IO_MODE 0 and 1, by setting BURST_PULSE = 0, the device will generate continuous burst pulses on OUTA and OUTB until the end of burst is signaled through SPI or the IO1 pin, respectively. Continuous bursting is not available for IO_MODE=3.
- A higher noise floor at the VOUT pin is expected in continuous mode where one transducer is used to transmit burst signals and another transducer is used to receive, as the switching noise of the digital IO pins can couple into the highly sensitive analog front end for the receive channel. This also applies to the single transducer use case where a continuous clock is applied on IO2 pin when the device is in indirect or listening mode.
- The range for frequency of switching for the output drivers is given by f_{DRV_CLK} parameter in the *Switching Characteristics* table.
- When the device is not in direct sensing or bursting mode, the device is always in indirect sensing or listening mode.

7.3.2.1 Burst Generation Diagnostics

In IO_MODE 0, 1 and 3, a pulse number diagnostic is active after start of burst (not when the burst is enabled) to monitor if the correct number of pulses (as set in BURST_PULSE) were generated before the end of burst was signaled through SPI or the IO1 pin. A fault, if detected, is then reported through the PULSE_NUM_FLT bit.

The pulse duration after start of burst (not when the burst is enabled) is monitored to detect a stuck condition, which will keep the FETs on OUTA or OUTB turned on. This can happen because of loss of external clock or the

Copyright © 2022 Texas Instruments Incorporated

driving signal on IO1 and IO2 pins being stuck in one state. The device expects to see a toggle on IOx pins (based on IO_MODE) within the time period as defined in the DRV_PLS_FLT_DT register. If this diagnostic triggers, it will force an end of burst. The fault is reported by setting the DRV_PULSE_FLT bit. If a DRV_PULSE_FLT is set in IO_MODE 0, 1 and 3—and the programmed number of pulses were not sent before end of burst—the PULSE_NUM_FLT will also be set.

Note

- The DRV_PULSE_FLT bit is cleared when a new start of burst is triggered, when DRV_PLS_FLT_DT = 0x7 is set, or if the device is put into Standby or Sleep mode.
- The PULSE_NUM_FLT bit is cleared when a new start of burst is triggered, or if the device is put into Standby or Sleep mode.

7.3.3 Transformer Transducer Drive

The device provides burst generation by exciting the primary side of a step-up transformer connected at the OUTA / OUTB pins. The VDRV pin is used as the power supply source. 図 7-5 shows the TUSS4440 device transformer drive block diagram when using a center-tap transformer. The drive stage in the TUSS4440 is realized as two low-side N-Channel power FETs. The current limit control block tries to drive current efficiently into the primary side of the transformer to achieve the maximum swing (set by voltage on the center tap and turn ratio of the transformer) on the secondary side. The secondary side total resistance, turn ratio, and the required peak-to-peak voltage will set the minimum value that will drive the OUTA/OUTB pin for a given set current limit. The current limit block supports multiple current levels selected by the XFMR_DRV_ILIM bits. The voltage on VDRV pin can be set as described in the *Excitation Power Supply (VDRV)* section.

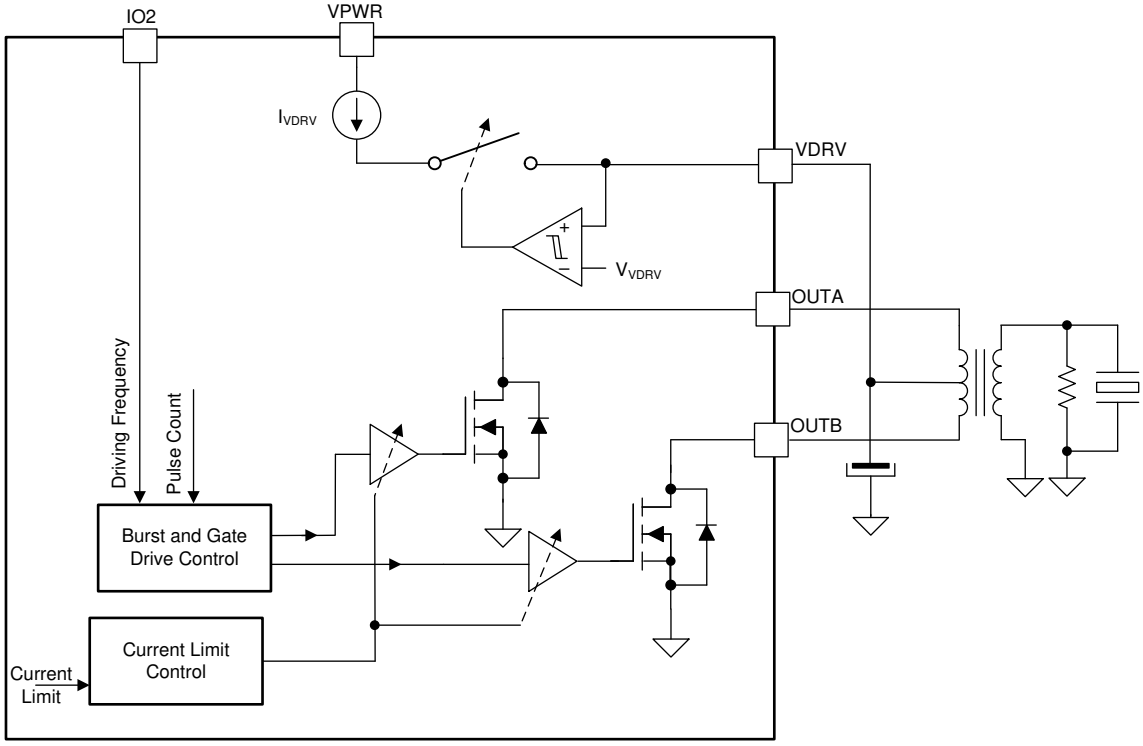


図 7-5. TUSS4440 Center-Tap transformer drive.

For a center-tap transformer configuration, the TUSS4440 will drive the low-side FETs in an out-of-phase manner. The device also supports a single primary coil transformer configuration where the FETs are driven in-phase. This is done by setting the HALF_BRG_MODE bit. In this mode, the effective current limit remains the same as set in XFMR_DRV_ILIM. Refer to *Application and Implementation* for an application diagram and information on how the polarity and state of the OUTA and OUTB pins are defined with respect to the IO1 and IO2 pin states and other register settings.

Note

For a center-tap transformer, the voltage swing on OUTA and OUTB can be as high as 2 × V_{VDRV}. If the center tap of the transformer is connected directly to VPWR, then it must be ensured that the maximum voltage on OUTA and OUTB pins do not go above the absolute maximum limits.

7.3.4 Analog Front End

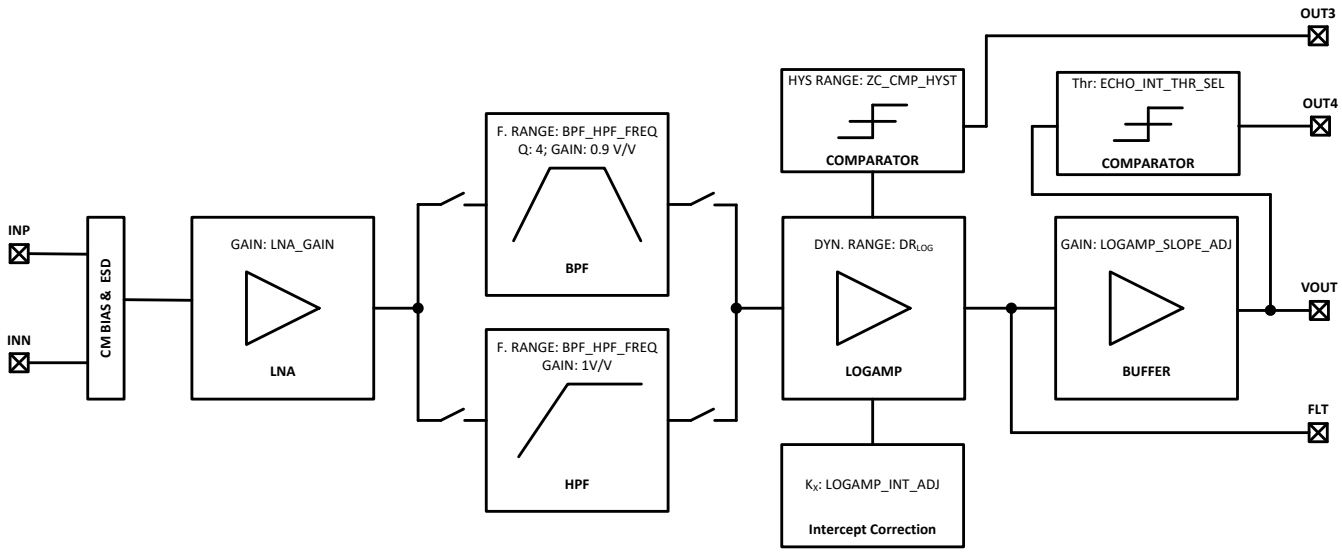


図 7-6. TUSS4440 Analog Front-End Block Diagram

図 7-6 shows the analog front-end block diagram that can receive and condition the signals from the transducer during listen mode. The received echo is first amplified with a fixed linear low-noise amplifier, followed by either a bandpass filter or a high-pass filter to remove noise out of the expected signal band. After filtering the signal, the signal is fed into a logarithmic amplifier. The output of the logarithmic amplifier is then buffered to the VOUT pin. In 図 7-6, every block has the register name associated with it that can be used to configure the signal path. The final equation for the signal path is given by 式 2:

$$V_{OUT} = G_{VOUT} \cdot SL_{LOG} \cdot 20\log_{10}\left(\frac{G_{LNA} \cdot G_{BPF} \cdot V_{IN}}{INT_{LOG} \cdot K_X}\right) \quad (1)$$

where

- G_{VOUT} is set by the LOGAMP_SLOPE_ADJ bits.
- SL_{LOG} is slope of logarithmic amplifier as specified in the *Receiver Characteristics* table.
- G_{LNA} is set by the LNA_GAIN bits.
- G_{BPF} is typically 0.9V/V.
- V_{IN} is the input V_{INP}
- INT_{LOG} is logarithmic amplifier intercept specified in the *Receiver Characteristics* table.
- K_X is the log intercept adjustment set by the LOGAMP_INT_ADJ bits.

The bandpass filter is critical for reducing noise to allow utilization of the complete dynamic range of the logarithmic amplifier. The center frequency of the bandpass filter can be configured to be close the transducer frequency which is set by the BPF_HPF_FREQ bits. 表 7-1 shows the nominal values for the BPF center frequency corresponding to the BPF_HPF_FREQ register value. The TUSS4440 supports a wide range of frequencies, therefore a factory trim is used to remove process variation for a particular pre-determined frequency. It is possible that all other frequencies listed in 表 7-1 do not correspond exactly to value of BPF_HPF_FREQ in a factory trim. The user can vary the value of the BPF_HPF_FREQ register around the

Copyright © 2022 Texas Instruments Incorporated

desired center frequency while actively bursting and observing the VOUT signal. The value with maximum voltage at VOUT pin will the desired setting for the BPF_HPF_FREQ register.

表 7-1. Bandpass Filter Center Frequency Configuration

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F_c (KHz)
0x00	40.64
0x01	44.05
0x02	45.6
0x03	48.86
0x04	50.58
0x05	52.96
0x06	56.75
0x07	60.11
0x08	62.95
0x09	66.68
0x0A	71.44
0x0B	74.81
0x0C	79.24
0x0D	82.03
0x0E	86.89
0x0F	92.04
0x10	97.49
0x11	103.27
0x12	109.4
0x13	114.54
0x14	121.33
0x15	128.52
0x16	134.58
0x17	142.55
0x18	151.01
0x19	159.94
0x1A	167.48
0x1B	177.41
0x1C	185.77
0x1D	196.78
0x1E	206.05
0x1F	218.26
0x20	228.54
0x21	244.89
0x22	256.43
0x23	271.63
0x24	284.43
0x25	301.28
0x26	319.13
0x27	338.14
0x28	353.97
0x29	374.95

Copyright © 2022 Texas Instruments Incorporated

表 7-1. Bandpass Filter Center Frequency Configuration (continued)

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F_c (KHz)
0x2A	397.16
0x2B	408.17
0x2C	420.7
0x2D	455.63
0x2E	472.03
0x2F	500

The factory trim can be overridden by setting the BPF_FC_TRIM_FRC bit first and varying the BPF_FC_TRIM bit after. This is useful in two ways:

- If the factory trimmed bandpass filter center frequency is higher than the desired value for BPF_HPF_FREQ = 0x00, or lower than desired value for BPF_HPF_FREQ = 0x2F, then BPF_FC_TRIM can be used to recover the range.
- This setting can also be used to extend the frequency range of the bandpass filter center frequency.

The BPF_FC_TRIM acts like an offset on top of the BPF_HPF_FREQ setting. 表 7-2 shows the nominal value of center frequency when this offset is added to the minimum and maximum BPF_HPF_FREQ code. 図 6-11 shows the measured data. For BPF_HPF_FREQ values greater than 0x08 and less than 0x27, varying BPF_FC_TRIM keeping BPF_HPF_FREQ fixed is the same as setting BPF_FC_TRIM = 0x00 and varying BPF_HPF_FREQ to find the optimum setting.

表 7-2. Bandpass Filter Center Frequency Range Extension

BPF_HPF_FREQ (hex) + BPF_FC_TRIM (hex) (BPF_FC_TRIM_FRC = 1)	BPF_F_c (KHz)
0x00 + 0x8	27.48
0x00 + 0x9	29.44
0x00 + 0xA	30.83
0x00 + 0xB	31.19
0x00 + 0xC	32.65
0x00 + 0xD	34.19
0x00 + 0xE	35.8
0x00 + 0xF	38.81
0x2F + 0x1	523.56
0x2F + 0x2	554.59
0x2F + 0x3	587.45
0x2F + 0x4	622.23
0x2F + 0x5	651.58
0x2F + 0x6	690.19
0x2F + 0x7	731.09

Note

- The Q factor of the filter is specified in the *Receiver Characteristics* table, and can be selected by the BPF_Q_SEL bits.
- The bandpass filter can also be converted into a high-pass filter by setting the BPF_BYPASS bit for transducer frequencies in the range above what is shown in 表 7-1. The corner frequency for high-pass filter is also controlled by the BPF_HPF_FREQ bits.
- BPF_Q_SEL and BPF_FC_TRIM have no effect when BPF_BYPASS = 1.

Copyright © 2022 Texas Instruments Incorporated

The logamp provides compression for large signal inputs and amplifies linearly small signal inputs. Logamp simplifies system design to detect varying strengths of echoes that happens because of difference in reflectivity of different types of objects and objects at different distances. It automatically adjusts its gain based on the input signal level. The logamp also demodulates the incoming signal.

The logamp consists of multiple gain stages and range extension stages that are combined to give a logarithmic response. The current consumption of the device can be reduced by turning off the either the first stage, the last stage of the logamp, or both, by setting the LOGAMP_DIS_FIRST and LOGAMP_DIS_LAST bits. Disabling the stages will reduce the input dynamic range on the lower side of the range (see 図 6-4). The pedestal noise floor will be lower because the gain stages are disabled, but the minimum detectable signal value becomes higher due to the reduced dynamic range. Depending on the received input signal strength, stages can be disabled to get optimum object detection. For very small inputs, all stages should be enabled to get maximum input dynamic range even though the noise floor is higher. 図 6-6, 図 6-7, and 図 6-8 show the effect on the log conformance error when all stages are enabled, when the last stage is disabled, and when both first and last stages are disabled. When stages are disabled, a lower error is obtained with a lower noise floor, but the input dynamic range is reduced.

At the output of the logamp, the user can apply an adjustment to the intercept of the logamp curve. This is denoted by the K_X factor in 式 1. The intercept adjustment is controlled by the LOGAMP_INT_ADJ bits. 表 7-3 shows the nominal values of K_X factor corresponding to register values, and 図 6-14 shows its effect on the transfer function.

表 7-3. Logamp Intercept Adjustment

LOGAMP_INT_ADJ	K_X
0x00	1
0x01	1.155
0x02	1.334
0x03	1.54
0x04	1.778
0x05	2.054
0x06	2.371
0x07	2.738
0x08	1
0x09	0.931
0x0A	0.866
0x0B	0.806
0x0C	0.75
0x0D	0.698
0x0E	0.649
0x0F	0.604

The output of the logamp is filtered using a low-pass filter to remove the high-frequency components and provide a sufficient peak hold time for the demodulated envelope signal. The cut-off frequency of the low-pass filter is set by the internal impedance of the FLT pin and the value of an external capacitor connected to the pin. As this filter capacitance (C_{FLT}) suppresses the high frequency fluctuations, it also slows down the response time of the logamp. Higher C_{FLT} capacitance will result in lower peak-to-peak voltage variations at VOUT, and slower rise and fall times for the VOUT voltage to reach its maximum value for a given input signal. A nominal value can be calculated using 式 3, and must be optimized depending on the application.

The output of the low-pass filter is buffered to the VOUT pin using an internal buffer. The buffer is designed to support an ADC input of a MCU. It is possible to change output dynamic range of the VOUT buffer using the VOUT_SCALE_SEL bit. Once the range is set, the gain of the VOUT buffer can be set by the LOGAMP_SLOPE_ADJ bits. The slope variation of the receiver analog front end is show in 図 6-13.

Echo interrupt signal is available on the OUT4 pin that goes high when the signal on the VOUT pin crosses a threshold as defined by the ECHO_INT_THR_SEL bits. As long as the VOUT signal is higher than this threshold, the echo interrupt signal is held high. The signal goes low asynchronously when the VOUT signal drops below the programmed threshold. This signal can be used to interrupt a MCU when an object has been detected. The threshold value is also dependent on the setting of the VOUT_SCALE_SEL bit.

A zero-crossing signal is output at the OUT3 pin which can be used to validate the frequency of the received echo signal to provide robustness against interference from other signals. This zero-crossing signal is derived from the raw amplified input signal from a particular stage as it is being demodulated in the logamp block. This function is disabled at device power up. but can be enabled by setting the ZC_CMP_EN bit. When enabled, the ZC_CMP_STG_SEL bits are used to select which logamp gain stage is used to generate the zero crossing signal while the ZC_CMP_HYST bits control the hysteresis of the zero-crossing comparator. The stage selection to see the OUT3 pin toggling depends on the strength of signal received by the logamp and has to be configured depending on the application. For large amplitude of input signal, a lower stage of the logamp should be selected, whereas for lower amplitude signal, a higher stage should be selected. To avoid switching noise generated by the toggling of the zero-crossing comparator when the ZC_EN_ECHO_INT bit is set, the zero-crossing output will be only enabled while the echo interrupt signal is high.

7.4 Device Functional Modes

The device has four functional modes:

Sleep Mode

Ultra-low current consumption sleep mode

In this mode, all major blocks of the device are disabled, including VDRV regulation. The SPI interface is still active. This transition into and out of this mode is done using the SLEEP_MODE_EN register bit. Upon issuing a command to exit this mode, the device transitions to other modes only when the VDRV pin reaches the programmed regulation voltage.

Standby Mode

Low current standby mode

In this state, the VDRV regulation is active, but other analog blocks are shut down to reduce quiescent current consumption. The STDBY_MODE_EN bit is used to enter and exit this mode through SPI. The device can transition very quickly from this state to one of the active states for bursting and listening.

Listen Mode

Default mode of the device

This is the default mode of the device when it is not in Sleep mode or Standby mode. In this mode, there is no activity on the transmitter block and the device is actively listening for any ultrasonic signals.

Burst Mode

Mode in which the device is enabled to start a burst to drive the transducer

In this mode, the transmitter blocks are active and enabled to drive the transducer depending on when the start of burst occurs. The receiving path is also active at the same time listening for signals at the input. This mode is entered when a burst enable event occurs and exited when an end of burst occurs as described in *Burst Generation* section.

図 7-7 shows an example of the transitions between the different modes of the device for IO_MODE = 0, where the burst is activated through a SPI command and end of burst occurs as the number of programmed pulses are sent.

Copyright © 2022 Texas Instruments Incorporated

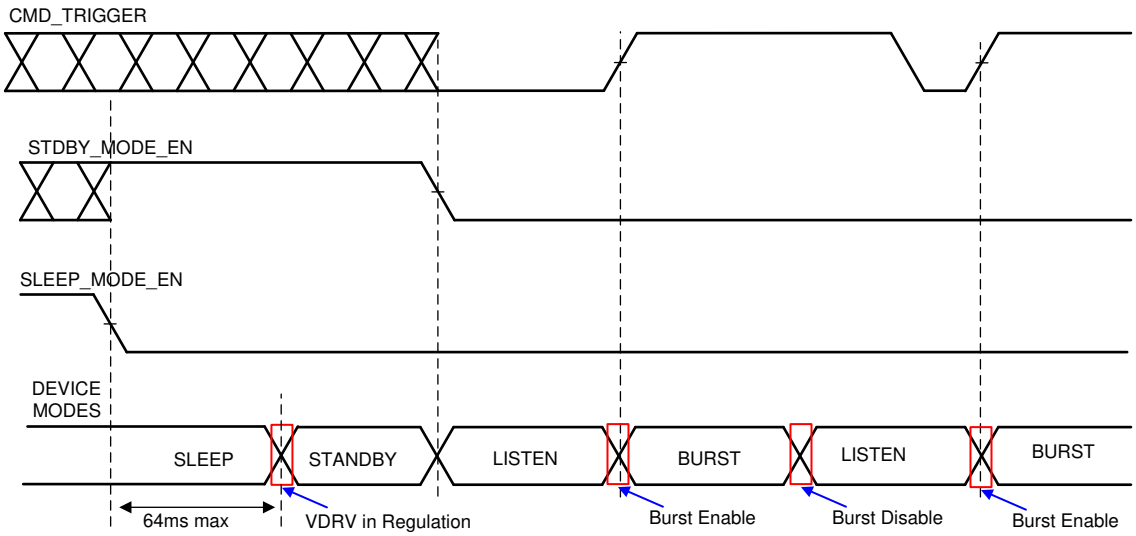


図 7-7. Device Modes Timing Diagram

Note

- The transition to standby or active mode (listen or burst) from power-up or sleep mode is done only once the VDRV voltage crosses the programmed VDRV_VOLTAGE_LEVEL bit, or is higher 64 ms, whichever occurs earlier.
- In the case when VDRV is disabled, the device immediately transitions from power or sleep mode to standby and active modes.

7.5 Programming

The primary communication between the IC and the external MCU is through an SPI bus that provides full-duplex communications in a controller-peripheral configuration. The external MCU is **always** a SPI controller that sends command requests on the SDI pin and receives device responses on the SDO pin. The device is **always** a SPI peripheral device that receives command requests and sends responses to the external MCU over the SDO line. The following lists the characteristics of the SPI:

- The SPI is a 4-pin interface.
- The frame size is 16 bits and is assigned as follows:

Controller-to-peripheral (MCU to TUSS4440 over the SDI line)	1 RW bit, 6 bits for the register address, 1 ODD parity bit for entire SPI frame, 8 bits for data
Peripheral-to-controller (TUSS4440 to MCU over the SDO line)	1 bit for Controller Parity error reporting during previous frame reception, 6 bits for the status, 1 bit for ODD parity for entire SPI frame, 8 bits for data

- SPI commands and data are shifted with the MSB first and the LSB last.
- The SDO line is sampled on the falling edge of the SCLK pin.
- The SDI line is shifted out on the rising edge of the SCLK pin.

The SPI communication begins with the NCS falling edge and ends with the NCS rising edge. The NCS high-level maintains the SPI peripheral-interface in the RESET state. The SDO output is in the tri-state condition.

The SPI does not support *back-to-back* SPI frame operation. After each SPI transfer the NCS pin must go from low to high before the next SPI transfer can begin.

図 7-8 shows an overview of a complete 16-bit SPI frame.

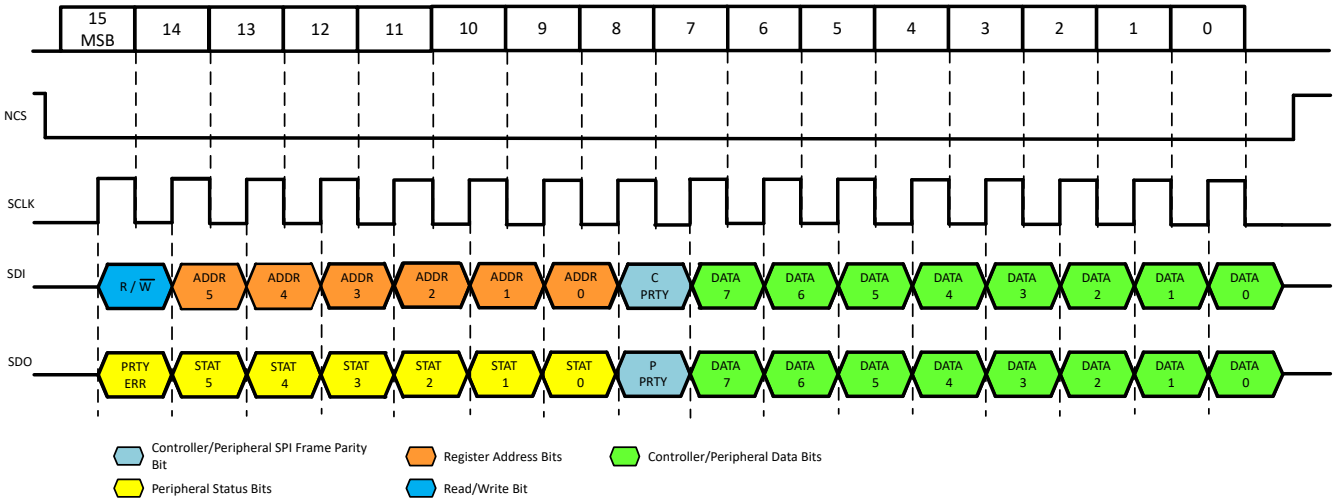


図 7-8. 16-Bit SPI Frame

図 7-9 shows a SPI transfer sequence between the controller and the peripheral TUSS4440 device. When the controller is writing a SPI frame, the parity error bit indicates if there was a parity error for the previous frame. When the controller is transmitting the data for the SPI write, the peripheral echoes back register address that was sent just before in the command.

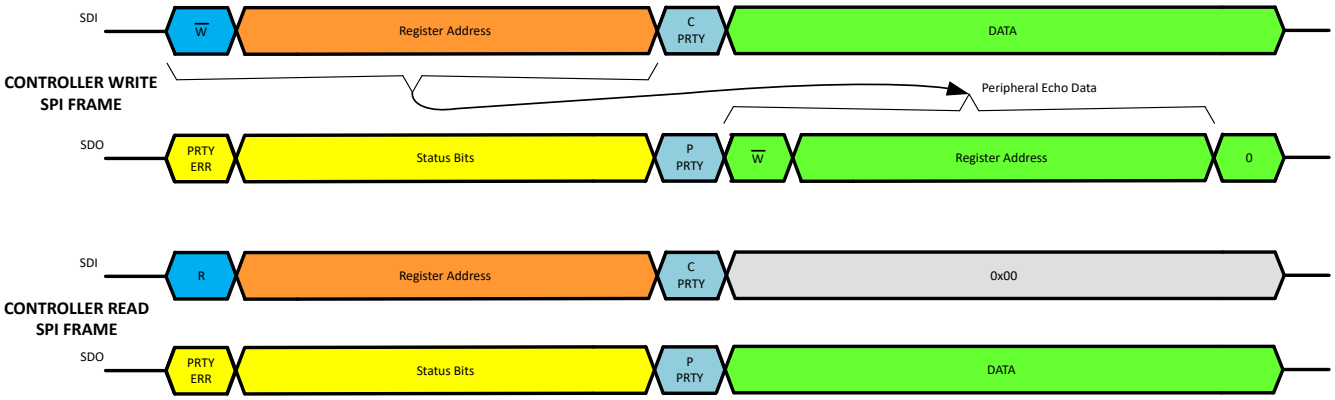


図 7-9. SPI Transfer Sequence

The status bits are defined in 表 7-4:

表 7-4. SPI Interface Status Bits Description

STATUS BIT	DESCRIPTION
STAT 5 - VDRV_READY	Set when VDRV power regulator has reached the programmed voltage level. This is also indicated by VDRV_READY bit.
STAT 4- PULSE_NUM_FLT	Set if the burst sequence was terminated before completing the pulse number selected. This is also indicated by PULSE_NUM_FLT bit.
STAT 3 - DRV_PULSE_FLT	Set if there is a "stuck" fault detected during pulsing in a burst sequence. This is also indicated by DRV_PULSE_FLT
STAT 2 - EE_CRC_FLT	Set if there is a CRC Error when loading internal EEPROM memory. This is also indicated by EE_CRC_FLT bit.
STAT <1:0> - DEV_STATE	Device State: 00 - LISTEN 01 - BURST 10 - STANDBY 11 - SLEEP

Copyright © 2022 Texas Instruments Incorporated

7.6 Register Maps

This section lists the REG_USER registers that are part of the volatile memory that can be configured by the MCU at power up or any time during the operation of the device. For register bits that are marked reserved, their reset value should not be changed.

7.6.1 REG_USER Registers

表 7-5 lists the REG_USER registers. All register offset addresses not listed in 表 7-5 should be considered as reserved locations and the register contents should not be modified.

表 7-5. REG_USER Registers

Address	Acronym	Register Name	Section
0x10	BPF_CONFIG_1	Bandpass filter settings	Go
0x11	BPF_CONFIG_2	Bandpass filter settings	Go
0x12	DEV_CTRL_1	Log-amp configuration	Go
0x13	DEV_CTRL_2	Log-amp configuration	Go
0x14	DEV_CTRL_3	Device Configuration	Go
0x16	VDRV_CTRL	VDRV Regulator Control	Go
0x17	ECHO_INT_CONFIG	Echo Interrupt Control	Go
0x18	ZC_CONFIG	Zero Crossing configuration	Go
0x19	XFMR_DRV_LIM	Transformer drive config	Go
0x1A	BURST_PULSE	Burst pulse configuration	Go
0x1B	TOF_CONFIG	Time of Flight Config	Go
0x1C	DEV_STAT	Fault status bits	Go
0x1D	DEVICE_ID	Device ID	Go
0x1E	REV_ID	Revision ID	Go

Complex bit access types are encoded to fit into small table cells. 表 7-6 shows the codes that are used for access types in this section.

表 7-6. REG_USER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 BPF_CONFIG_1 Register (Address = 0x10) [reset = 0x0]

BPF_CONFIG_1 is shown in 表 7-7.

Return to the Summary Table.

表 7-7. BPF_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BPF_FC_TRIM_FRC	R/W	0x0	Override factor settings for Bandpass filter trim and control via BPF_FC_TRIM register. Valid only when BPF_BYPASS = 0 0x0 = Factory trim 0x1 = Override Factory trim

表 7-7. BPF_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BPF_BYPASS	R/W	0x0	Select between Bandpass filter or high pass filter 0x0 = BPF Enabled 0x1 = HPF Enabled (BPF Bypass)
5:0	BPF_HPF_FREQ	R/W	0x0	If BPF_BYPASS = 0: Band pass filter center frequency. See "Bandpass filter center frequency configuration" table If BPF_BYPASS = 1: High pass filter corner frequency 0x00 - 0x0F - 200kHz 0x10 - 0x1F - 400kHz 0x20 - 0x2F - 50kHz 0x30 - 0x3F - 100kHz

7.6.1.2 BPF_CONFIG_2 Register (Address = 0x11) [reset = 0x0]

BPF_CONFIG_2 is shown in 表 7-8.

Return to the Summary Table.

表 7-8. BPF_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	BPF_Q_SEL	R/W	0x0	Bandpass filter Q factor. Valid only when BPF_BYPASS = 0 0x0 = 4 0x1 = 5 0x2 = 2 0x3 = 3
3:0	BPF_FC_TRIM	R/W	0x0	Offset BPF_HPF_FREQ when BPF_FC_TRIM_FRC = 1: BPF_HPF_FREQ = BPF_HPF_FREQ + BPF_FC_TRIM See "Bandpass filter center frequency range extension" table.

7.6.1.3 DEV_CTRL_1 Register (Address = 0x12) [reset = 0x0]

DEV_CTRL_1 is shown in 表 7-9.

Return to the Summary Table.

表 7-9. DEV_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_FRC	R/W	0x0	Override for factory settings for LOGAMP_SLOPE_ADJ and LOGAMP_INT_ADJ
6:4	LOGAMP_SLOPE_ADJ	R/W	0x0	Slope or gain adjustment at the final output on VOUT pin. Slope adjustment depends on the setting of VOUT_SCALE_SEL. 0x0 = 3.0× VOUT_SCALE_SEL+4.56×VOUT_SCALE_SEL V/V 0x1 = 3.1× VOUT_SCALE_SEL+4.71×VOUT_SCALE_SEL V/V 0x2 = 3.2× VOUT_SCALE_SEL+4.86×VOUT_SCALE_SEL V/V 0x3 = 3.3× VOUT_SCALE_SEL+5.01×VOUT_SCALE_SEL V/V 0x4 = 2.6× VOUT_SCALE_SEL+3.94×VOUT_SCALE_SEL V/V 0x5 = 2.7× VOUT_SCALE_SEL+ 4.10×VOUT_SCALE_SEL V/V 0x6 = 2.8× VOUT_SCALE_SEL+4.25×VOUT_SCALE_SEL V/V 0x7 = 2.9× VOUT_SCALE_SEL+4.4×VOUT_SCALE_SEL V/V
3:0	LOGAMP_INT_ADJ	R/W	0x0	Logamp Intercept adjustment. See "Logamp intercept adjustment" table in specification for values.

Copyright © 2022 Texas Instruments Incorporated

7.6.1.4 DEV_CTRL_2 Register (Address = 0x13) [reset = 0x0]

DEV_CTRL_2 is shown in 表 7-10.

Return to the Summary Table.

表 7-10. DEV_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_DIS_FIRST	R/W	0x0	Disable first logamp stage to reduce quiescent current
6	LOGAMP_DIS_LAST	R/W	0x0	Disable last logamp stage quiescent current
3	RESERVED	R	0x0	Reserved
2	VOUT_SCALE_SEL	R/W	0x0	Select VOUT scaling 0x0 = Select Vout gain to map output to 3.3 V 0x1 = Select Vout gain to map output to 5.0 V
1:0	LNA_GAIN	R/W	0x0	Adjust LNA Gain in V/V 0x0 = 15 V/V 0x1 = 10 V/V 0x2 = 20 V/V 0x3 = 12.5 V/V

7.6.1.5 DEV_CTRL_3 Register (Address = 0x14) [reset = 0x0]

DEV_CTRL_3 is shown in 表 7-11.

Return to the Summary Table.

表 7-11. DEV_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
4:2	DRV_PLS_FLT_DT	R/W	0x0	Driver Pulse Fault Deglitch Time. In IO_MODE = 0 or IO_MODE = 1, DRV_PULSE_FLT will be set if start of burst is triggered and IO2 pin has not toggled for greater than deglitch Time. In IO_MODE = 2, DRV_PULSE_FLT will be set if start of burst is triggered and if IO1 or IO2 do not toggle a period longer than the deglitch time except when both pins are high. 0x0 = 64 µs 0x1 = 48 µs 0x2 = 32 µs 0x3 = 24 µs 0x4 = 16 µs 0x5 = 8 µs 0x6 = 4 µs 0x7 = Check Disabled
1:0	IO_MODE	R/W	0x0	Configuration for low voltage IO pins. 0x0 = IOMODE 0 0x1 = IOMODE 1 0x2 = IOMODE 2 0x3 = IOMODE 3

7.6.1.6 VDRV_CTRL Register (Address = 0x16) [reset = 0x20]

VDRV_CTRL is shown in 表 7-12.

Return to the Summary Table.

表 7-12. VDRV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DIS_VDRV_REG_LSTN	R/W	0x0	Automatically disable VDRV charging in listen mode every time after burst mode is exited given VDRV_TRIGGER =0x0. 0x0 = Do not automatically disable VDRV charging 0x1 = Automatically disable VDRV charging
5	VDRV_HI_Z	R/W	0x1	Turn off current source between VPWR and VRDV and disable VDRV regulation. 0x0 = VDRV not Hi-Z 0x1 = VDRV in Hi-Z mode
4	VDRV_CURRENT_LEVEL	R/W	0x0	Pull up current at VDRV pin 0x0 = 10 mA 0x1 = 20 mA
3:0	VDRV_VOLTAGE_LEVEL	R/W	0x0	Regulated Voltage at VDRV pin Value is calculated as : VDRV = VDRV_VOLTAGE_LEVEL + 5 [V]

7.6.1.7 ECHO_INT_CONFIG Register (Address = 0x17) [reset = 0x7]

ECHO_INT_CONFIG is shown in 表 7-13.

Return to the Summary Table.

表 7-13. ECHO_INT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	ECHO_INT_CMP_EN	R/W	0x0	Enable echo interrupt comparator output
3:0	ECHO_INT_THR_SEL	R/W	0x7	Threshold level to issue interrupt on OUT4 pin. Applied to Low pass filter output. If VOUT_SCALE_SEL=0x0 : Threshold = 0.04 x ECHO_INT_THR_SEL + 0.4 [V] If VOUT_SCALE_SEL=0x1: Threshold = 0.06 x ECHO_INT_THR_SEL + 0.6 [V]

7.6.1.8 ZC_CONFIG Register (Address = 0x18) [reset = 0x14]

ZC_CONFIG is shown in 表 7-14.

Return to the Summary Table.

表 7-14. ZC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ZC_CMP_EN	R/W	0x0	Enable Zero Cross Comparator for Frequency detection
6	ZC_EN_ECHO_INT	R/W	0x0	When set, provides ZC information only when object is detected
5	ZC_CMP_IN_SEL	R/W	0x0	Zero Comparator Input Select 0x0 = INP - VCM 0x1 = INP - INN
4:3	ZC_CMP_STG_SEL	R/W	0x2	Zero Cross Comparator Stage Select

Copyright © 2022 Texas Instruments Incorporated

表 7-14. ZC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	ZC_CMP_HYST	R/W	0x4	Zero Cross Comparator Hysteresis Selection 0x0 = 30 mV 0x1 = 80 mV 0x2 = 130 mV 0x3 = 180 mV 0x4 = 230 mV 0x5 = 280 mV 0x6 = 330 mV 0x7 = 380 mV

7.6.1.9 XFMR_DRV_LIM Register (Address = 0x19) [reset = 0x0]

XFMR_DRV_LIM is shown in 表 7-15.

Return to the Summary Table.

表 7-15. XFMR_DRV_LIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	XFMR_DRV_ILIM	R/W	0x0	Current clamp for low side transformer drive. Value calculated as = [50 + (REG_VAL) x 7.14] mA

7.6.1.10 BURST_PULSE Register (Address = 0x1A) [reset = 0x0]

BURST_PULSE is shown in 表 7-16.

Return to the Summary Table.

表 7-16. BURST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALF_BRG_MODE	R/W	0x0	Use output driver in half-bridge mode. When enabled, drive low-side FETs in-phase 0x0 = Disable half-bridge mode 0x1 = Enable half bridge mode
5:0	BURST_PULSE	R/W	0x0	Number of burst pulses. REG_VALUE=0x00 enables continuous burst mode

7.6.1.11 TOF_CONFIG Register (Address = 0x1B) [reset = 0x0]

TOF_CONFIG is shown in 表 7-17.

Return to the Summary Table.

表 7-17. TOF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEEP_MODE_EN	R/W	0x0	For entering or exiting sleep mode 0x0 = Wake up or exit Sleep Mode 0x1 = Enter sleep mode
6	STDBY_MODE_EN	R/W	0x0	For entering or exiting standby mode 0x0 = Exit Standby Mode 0x1 = Enter Standby mode
5:2	RESERVED	R	0x0	Reserved

Copyright © 2022 Texas Instruments Incorporated

表 7-17. TOF_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VDRV_TRIGGER	R/W	0x0	Control charging of VDRV pin when DIS_VDRV_REG_LSTN = 1. This has no effect when VDRV_HI_Z=0x1. 0x0 = Disable I_{VDRV} 0x1 = Enable I_{VDRV}
0	CMD_TRIGGER	R/W	0x0	For IO_MODE=0x0, control enabling of burst mode. Ignored for other IO_MODE values. 0x0 = Disable burst mode 0x1 = Enable burst mode

7.6.1.12 DEV_STAT Register (Address = 0x1C) [reset = 0x0]

DEV_STAT is shown in 表 7-18.

Return to the Summary Table.

表 7-18. DEV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	VDRV_READY	R	0x0	VDRV pin voltage status 0x0 = VDRV is below configured voltage 0x1 = VDRV is equal or above configured voltage
2	PULSE_NUM_FLT	R	0x0	The Driver has not received the number of pulses defined by BURST_PULSE
1	DRV_PULSE_FLT	R	0x0	The Driver has been stuck in a single state in burst mode for a period longer than delgitch time set by DRV_PLS_FLT_DT
0	EE_CRC_FLT	R	0x0	CRC error for internal memory

7.6.1.13 DEVICE_ID Register (Address = 0x1D) [reset = X]

DEVICE_ID is shown in 表 7-19.

Return to the Summary Table.

表 7-19. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	X	Device ID: 0x99

7.6.1.14 REV_ID Register (Address = 0x1E) [reset = 0x2]

REV_ID is shown in 表 7-20.

Return to the Summary Table.

表 7-20. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID	R	0x2	Revision ID

Copyright © 2022 Texas Instruments Incorporated

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TUSS4440 device must be paired with an external ultrasonic transducer. The TUSS4440 device drives the transducer to generate an ultrasonic echo and applies logarithmic gain scaling to the received echo signal in the analog front end. The transducer should be chosen based on the resonant frequency, input voltage requirements, sensitivity, beam pattern, and decay time. The TUSS4440 device is flexible enough to meet most transducer requirements by adjusting the driving frequency, driving current limit, and center frequency of the band-pass filter.An external transformer should be chosen to meet the driver voltage requirements of the transducer and have a saturation current rated equal to or greater than the configured driving current limit of the TUSS4440 device. The only available interface to configure the device registers is SPI. During the burst-and-listen cycles, an external ADC or analog receiver should be used to capture the echo envelope from the VOUT pin to compute time of flight (ToF), distance, amplitude, and/or width of the return echo.

8.2 Typical Application

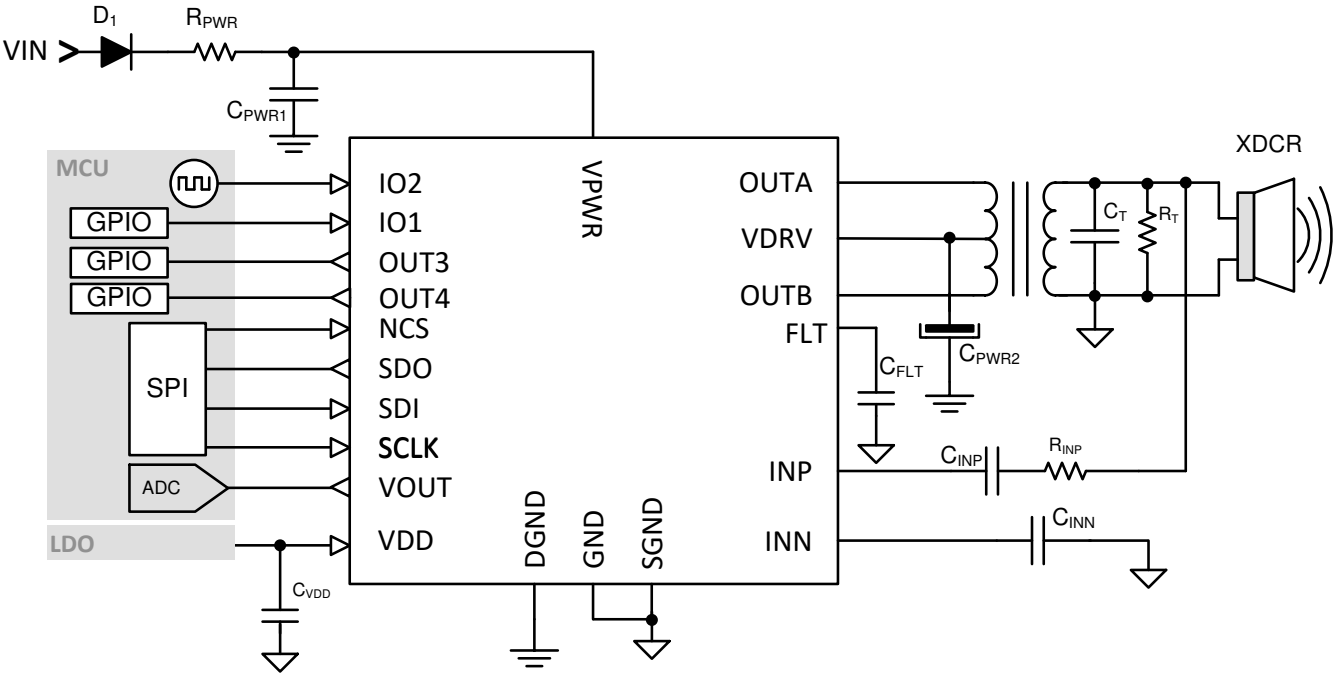


図 8-1. TUSS4440 Application Diagram

表 8-1. Recommended Component Values for Typical Applications

DESIGNATOR	VALUE	COMMENT
R_{PWR}	10 Ω	Optional (to limit fast voltage transient on VPWR pin during power up)
$R_{(INP)}$	3kΩ (1/4 Watt)	Optional for EMI/ESD robustness
C_{PWR1}	50V, 100nF	
C_{PWR2}	40V, 100µF	
C_{VDD}	>5V, 10nF	
C_{INP}	40V, 330pF	
C_{INN}	>5V, C_{INN}	Use equation below to estimate value of C_{INN} depending on the burst frequency $$C_{INN} = \frac{1}{2 \cdot \pi \cdot 150 \cdot \left(\frac{f_{DRV_CLK}}{4}\right)} \quad (2)$$
C_{FLT}	5V, C_{FLT}	Use equation below to estimate value of C_{FLT} depending on the burst frequency . Value has to be optimized for application depending on noise and response time requirements. $$C_{FLT} = \frac{25}{2 \cdot \pi \cdot \left(6250 \cdot f_{DRV_CLK}\right)} \quad (3)$$
C_T		Optional. Value depends on transducer and transformer used
R_T		Optional. Value depends on transducer and transformer used
D1	1N4001 or equivalent	Optional for reverse supply and reverse current protection.
XDCR (transducer)		Example devices for low-frequency range: Closed top: 40 kHz: PUI Audio UTR-1440K-TT-R Open top: muRata MA40H1S-R, SensComp 40LPT16, Kobitone 255-400PT160-ROX Example devices for high-frequency range: Closed top: 300 kHz: Murata MA300D1-1
XFMR (transformer)		Example devices: TDK EPCOS B78416A2232A003, muRata-Toko N1342DEA-0008BQE=P3, Mitsumi K5-R4

8.2.1 Transformer Drive Configuration Options

The TUSS4440 supports two pulsing modes to accommodate specific system needs based on the transformer used as shown in 図 8-2. The typical application diagram in 図 8-1 is considered as "Case 1".

Copyright © 2022 Texas Instruments Incorporated

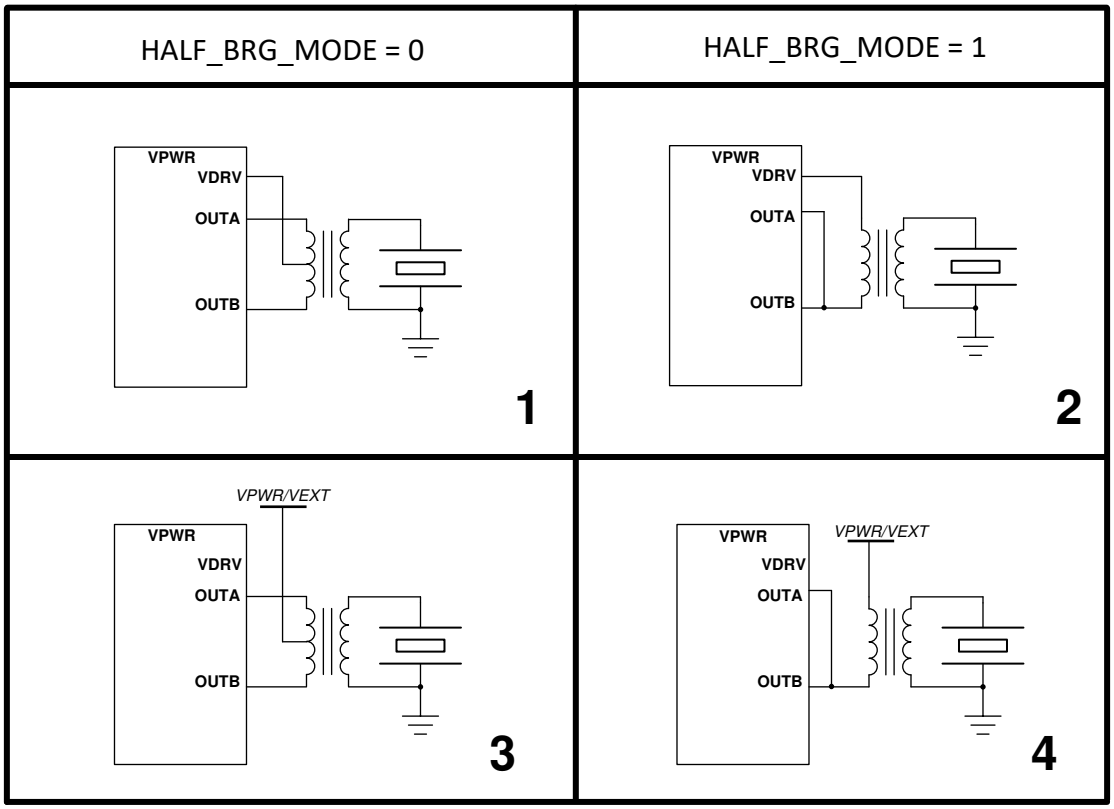


図 8-2. TUSS4440 Transducer Drive Options

The behavior of the internal FETs of TUSS4440 is different for each configuration in 表 8-2. The relationship between the IOx pins and the state of the OUTA and OUTB pins for different register settings is shown in 表 8-2 and 表 8-3.

表 8-2. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 2

IO MODE 2						
START OF BURST	HALF_BRG_MODE	IO1	IO2	OUTA	OUTB	APPLICATION CASE
YES	0	0	0	Hi-Z	Hi-Z	CASE 1, CASE 3
	0	0	1	Hi-Z	GND	
	0	1	0	GND	Hi-Z	
NO	0	1	1	Hi-Z	Hi-Z	
YES	1	0	0	Hi-Z	Hi-Z	CASE 2, CASE 4
	1	0	1	GND	GND	
	1	1	0	Hi-Z	Hi-Z	
NO	1	1	1	Hi-Z	Hi-Z	

表 8-3. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 0, IO MODE 1 and IO MODE 3

IO MODE 0, IO MODE 1, IO MODE 3							
START OF BURST	HALF_BRG_MODE	CMD_TRIGGER (IO MODE 0)	IO1 (IO MODE 1)	IO2	OUTA	OUTB	APPLICATION CASE
NO	0	0	1	0	Hi-Z	Hi-Z	CASE 1, CASE 3
	0	0	1	1			
YES	0	1	0	0	Hi-Z	GND	
	0	1	0	1	GND	Hi-Z	

表 8-3. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 0, IO MODE 1 and IO MODE 3 (continued)

IO MODE 0, IO MODE 1, IO MODE 3							
START OF BURST	HALF_BRG_MODE	CMD_TRIGGER (IO MODE 0)	IO1 (IO MODE 1)	IO2	OUTA	OUTB	APPLICATION CASE
NO	1	0	1	0	Hi-Z	Hi-Z	CASE 2, CASE 4
	1	0	1	1			
YES	1	1	0	0	Hi-Z	Hi-Z	
	1	1	0	1	GND	GND	

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-4 as the input and operating parameters. All other device settings can be assumed to be factory default.

表 8-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 to 36 V
Input voltage recommended	5 V, 12 V
Transformer turns ratio	(1-2) : (2-3) : (4-6) = 1:1:8.42
Transformer driving current rating	300 mA
Transducer driving voltage	70 V_{AC}
Transducer frequency	40 kHz, 400 kHz
Transducer pulse count	16

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Transducer:
  - Transducer driving voltage
  - Transducer resonant frequency
  - Transducer pulse count maximum
- Transformer:
  - Transformer turns ratio
  - Transformer saturation current
  - Transformer main voltage (4-6) rating

8.2.1.2.1 Transducer Driving Voltage

When a voltage is applied to piezoelectric ceramics, mechanical distortion is generated according to the voltage and frequency. The mechanical distortion is measured in units of sound pressure level (SPL) to indicate the volume of sound, and can be derived from a free-field microphone voltage measurement using 式 4.

$$\text{SPL (db)} = 20 \times \log \frac{\left(\frac{V_{(MIC)}}{3.4\ \text{mV}}\right)}{P_O} \tag{4}$$

where

- $V_{(MIC)}$ is the measured sensor sound pressure (mV_{RMS}).
- P_O is a referenced sound pressure of 20 µPa.

The SPL does not increase indefinitely with the driving voltage. After a particular driving voltage, the amount of SPL that a transducer can generate becomes saturated. A transducer is given a maximum driving voltage

Copyright © 2022 Texas Instruments Incorporated

specification to indicate when the maximum SPL is generated. Driving the transducer beyond the maximum driving voltage makes the ultrasonic module less power-efficient and can damage or decrease the life expectancy of the transducer.

8.2.1.2.2 Transducer Driving Frequency

The strength of ultrasonic waves propagated into the air attenuate proportionally with distance. This attenuation is caused by diffusion, diffraction, and absorption loss as the ultrasonic energy transmits through the medium of air. As shown in 図 8-3, the higher the frequency of the ultrasonic wave, the larger the attenuation rate and the shorter the distance the wave reaches.

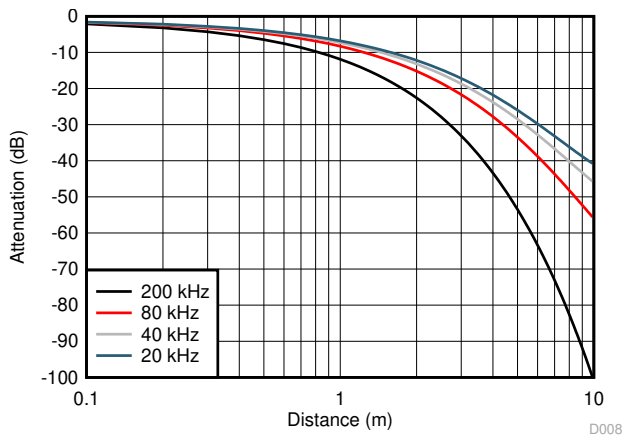


図 8-3. Attenuation Characteristics of Sound Pressure by Distance

An ultrasonic transducer has a fixed resonant center frequency with a typical tolerance of ±2%. The lower frequency range of 30 kHz to 100 kHz is the default operating range for common long range applications for a step resolution of 1 cm and typical range of 30 cm to 5 m. The upper frequency range of 100 kHz to 1000 kHz is reserved for high-precision applications with a step resolution of 1 mm and a typical range of 5 cm to 1 m.

8.2.1.2.3 Transducer Pulse Count

The pulse count determines how many alternating periods are applied to the transducer by the complementary low-side drivers and determines the total width of the ultrasonic ping that was transmitted. The larger the width of the transmitted ping, the larger the width of the returned echo signature of the reflected surface and the more resolution available to set a stable threshold. A disadvantage of a large pulse count is a large ringing-decay period, which limits how detectable objects are at short distances.

Select a pulse count based on the minimum object distance requirement. If short-distance object detection is not a priority, a high pulse count is not a concern. Certain transducers can be driven continuously while others have a limit to the maximum driving-pulse count. Refer to the specification for the selected transducer to determine if the pulse count must be limited.

8.2.1.2.4 Transformer Turns Ratio

A center-tap transformer is typically paired with the transducer to convert a DC voltage to a high-sinusoidal AC voltage. The center tap is a contact made to a point halfway along the primary winding of the transformer. The center tap is supplied with the DC voltage that is then multiplied on the secondary side based on the turns ratio of the transformer. 図 8-4 shows the typical pinout of a center-tap transformer where pin 2 is the center tap, pins 1 and 3 are connected to OUTB and OUTA, pin 4 is connected to the positive terminal of the transducer, and pin 6 is connected to ground.

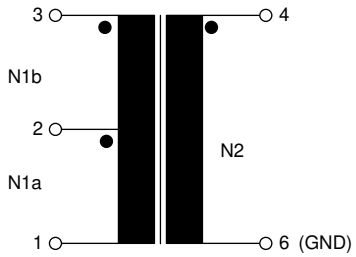


図 8-4. Typical Pinout of Center-Tap Transformer for Ultrasonic Transducers

Two modes to generate the transducer voltage using the center-tap transformer are available. These modes are defined as follows:

Push-pull In this mode, the two internal low-side switches of the TUSS4440 device are used to turn current on and off in two primary coils of the center-tap transformer.

The primary coils have the same number of turns. The rate of change of current in the primary coil generates a voltage in the secondary coil of the transformer, which is connected to the transducer. The direction of current in the primary coils generates voltages of opposite polarity in the secondary coils which effectively doubles the peak-to-peak voltage in the secondary coil.

Single-ended In this mode, one low-side switch is used to turn current on and off in the primary of the transformer.

The rate of change of current in the primary coil generates a voltage in the secondary coil of the transformer, which is connected to the transducer. The center tap of the transformer is not required for this mode, and can be left floating. Instead, the reference voltage is connected to an outermost primary-side terminal (pin 3) and either OUTA or OUTB is connected to the other primary-side terminal (pin 1).

8.2.1.2.5 Transformer Saturation Current and Main Voltage Rating

Leakage inductance is caused when magnetic flux is not completely coupled between windings in a transformer. Magnetic saturation of a transformer core can be caused by excessive primary voltage, operation at too low of a frequency, by the presence of a DC current in any of the windings, or a combination of these causes. The TUSS4440 device can limit the primary-side driver current of the transformer internally from 50 mA to 500 mA. The center-tap voltage is typically referenced to the VPWR voltage. However, if the VPWR voltage is too high of a voltage on the center tap of the primary side, then the voltage must be down-regulated. If the VPWR is too low, then the voltage must be up-regulated.

Copyright © 2022 Texas Instruments Incorporated

8.2.1.3 Application Curves

図 8-5 and 図 8-6 show the typical ranging performance of a 40-kHz, closed-top transducer under nominal operating conditions as indicated in the 表 8-4. The targeted object is a PVC pole measuring 1000 mm in height and 75 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1.

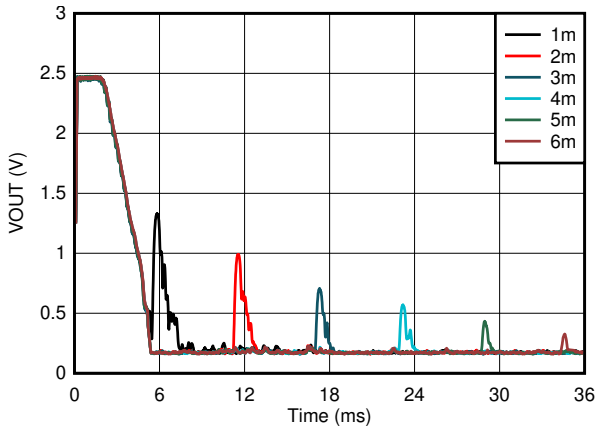


図 8-5. TUSS4440 40 kHz Ranging at 5-V Center Tap With Last Log-Amp Stage Disabled

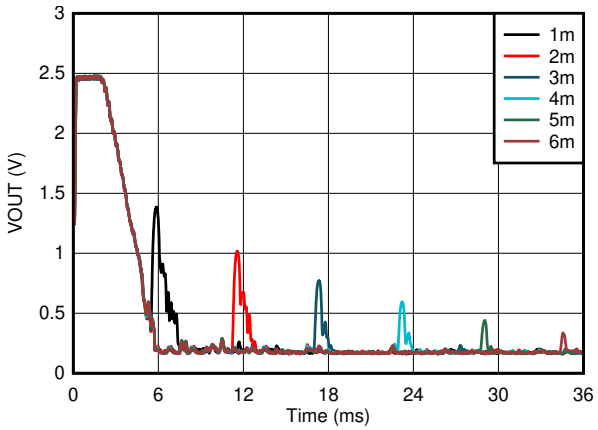


図 8-6. TUSS4440 40 kHz Ranging at 12-V Center Tap With Last Log-Amp Stage Disabled

図 8-7 and 図 8-8 show the typical ranging performance of a 400-kHz, closed-top transducer under nominal operating conditions as indicated in the 表 8-4. The targeted object is an aluminum pole measuring 100 mm in height and 10 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0.

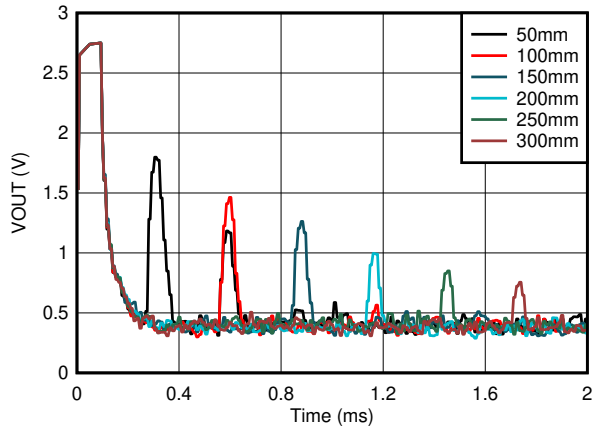


図 8-7. TUSS4440 400 kHz Ranging at 5-V Center Tap

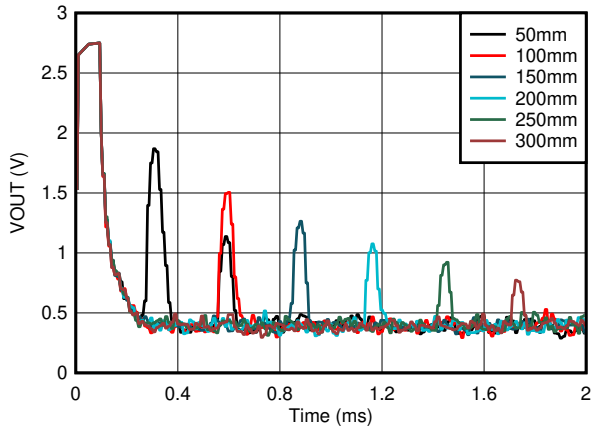


図 8-8. TUSS4440 400 kHz Ranging at 12-V Center Tap

9 Power Supply Recommendations

The TUSS4440 device is designed to operate from two independent supplies, a driver supply and a regulated supply.

The driver input voltage supply (VPWR) range can operate from 5 V to 24 V (when VDRV is disabled) or to 36 V (when VDRV is enabled). In applications where the TUSS4440 device may be exposed to battery transients and reverse battery currents, use external component-safeguards, such as component D1 or parallel TVS diodes, to help protect the device. If the input supply is placed more than a few inches from the TUSS4440 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors near the VPWR pin. In the event VDRV is disabled, the electrolytic capacitor at the VDRV pin is intended to act as a fast discharge capacitor during the bursting stage of the TUSS4440 device. The center-tap transformer can be supplied with an independent center-tap voltage that is isolated from the VPWR and VDRV pins, but must remain within half the specified maximum voltage rating of the OUTA and OUTB outputs. If the center-tap voltage is to be supplied by an independent source, the VDRV pin can remain floating, and VDRV should be disabled.

The regulated supply (VDD) is used as the supply reference for the analog front end, filtering, and analog output blocks, so this supply should be stable for maximum performance. TI recommends using an LDO or other regulated external power source with bypass capacitor placed closely to the VDD pin. As VDD becomes less stable, the noise floor of the VOUT signal will increase, and result in a loss of long range object detection as a consequence.

To prevent damage to the device, always avoid hot-plugging or providing instantaneous power at the VPWR and VDRV pins at start-up, unless these pins are properly protected with an RC filter or TVS diode to minimize transient effects. VPWR must always be equal to or greater than the value present at VDRV.

Copyright © 2022 Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

A minimum of two layers is required to accomplish a small-form factor ultrasonic module design. The layers should be separated by analog and digital signals. The pin map of the device is routed such that the power and digital signals are on the opposing side of the analog driver and receiver pins. Consider the following best practices for TUSS4440 device layout in order of descending priority:

- Separating the grounding types is important to reduce noise at the AFE input of the TUSS4440. In particular, the transducer sensor ground, supporting driver, and return-path circuitry should have a separate ground before being connected to the main ground. Separating the sensor and main grounds through a ferrite bead is best practice, but not require. A copper-trace or 0-Ω short is also acceptable when bridging grounds.
- The analog return path pins, INP and INN, are most susceptible to noise and therefore should be routed as short and directly to the transducer as possible. Ensure the INN capacitor is close to the pin to reduce the length of the ground wire.
- The analog output pin trace should be routed as short and directly to an external ADC or microcontroller input to avoid signal-to-noise losses due to parasitic-effects or noise coupling onto the trace from external radiating aggressors.
- In applications where protection from an ESD strike on the case of the transducer is important, ground routing of the capacitor on the INN pin should be separate from the device ground and connected directly with the shortest possible trace to the connector ground.
- The analog drive pins can be high-current, high-voltage, or both and therefore the design limitation of the OUTA and OUTB pins is based on the copper trace profile. The driver pins are recommended to be as short and direct as possible when using a transformer to drive the primary windings with a high-current limit.
- The decoupling capacitors for the VDD and VPWR pins should be placed as close to the pins as possible.
- Any digital communication should be routed away from the analog receiver pins. TXD, RXD, SCLK, NCS, IO1, IO2, OUT3, and OUT4 pins should be routed on the opposite side of the PCB, away from of the analog signals.

Copyright © 2022 Texas Instruments Incorporated

10.2 Layout Example

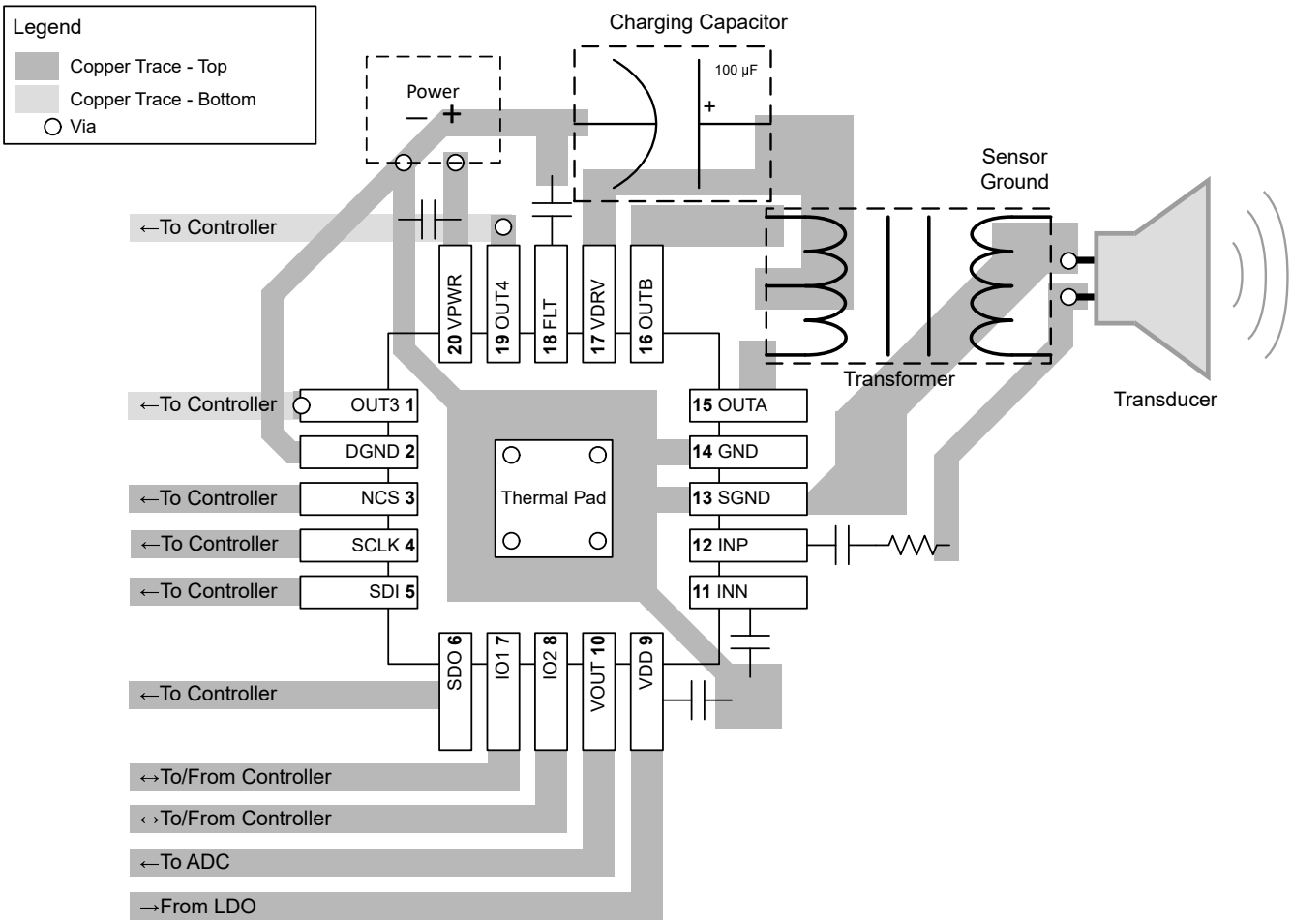


図 10-1. TUSS4440 Layout Example

Copyright © 2022 Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSS4440TRTJR	Active	Production	QFN (RTJ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 105	USS4440
TUSS4440TRTJR.A	Active	Production	QFN (RTJ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 105	USS4440
TUSS4440TRTJT	Obsolete	Production	QFN (RTJ) | 20	-	-	Call TI	Call TI	-25 to 105	USS4440

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

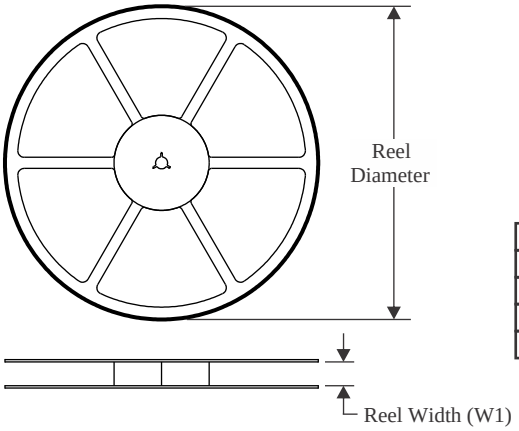
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

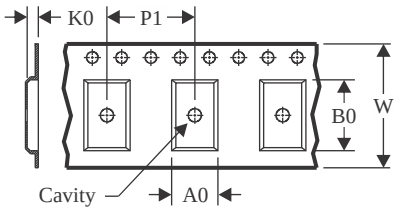
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

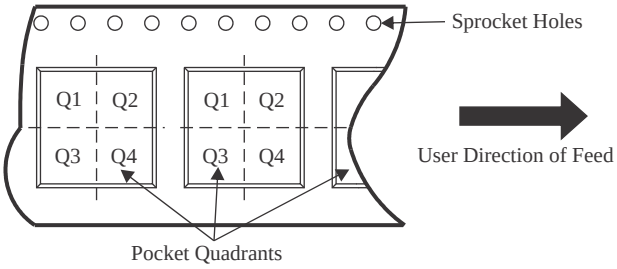


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

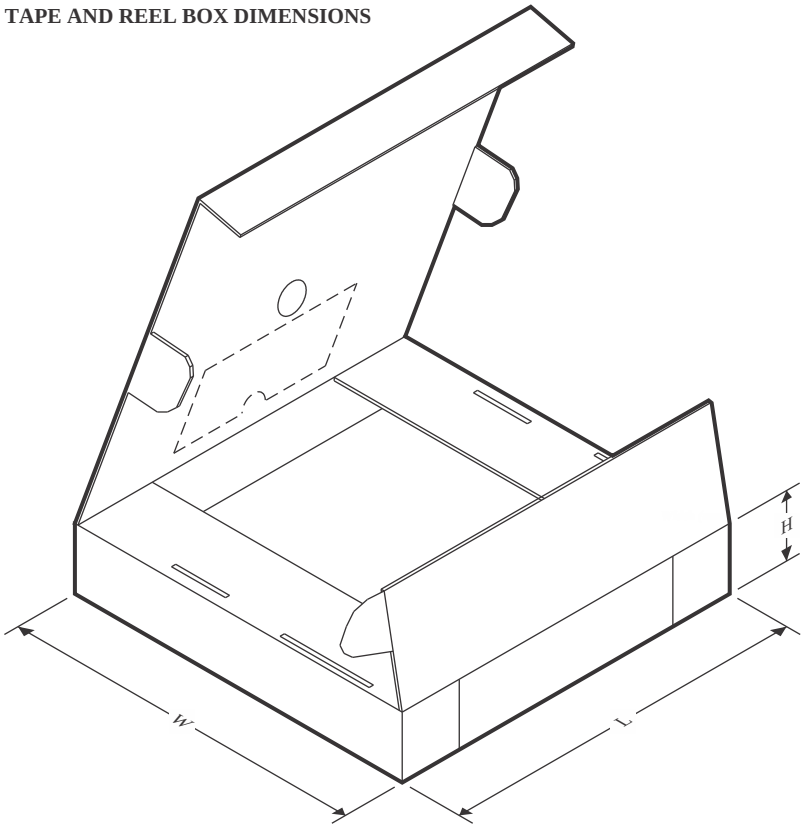
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSS4440TRTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSS4440TRTJR	QFN	RTJ	20	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

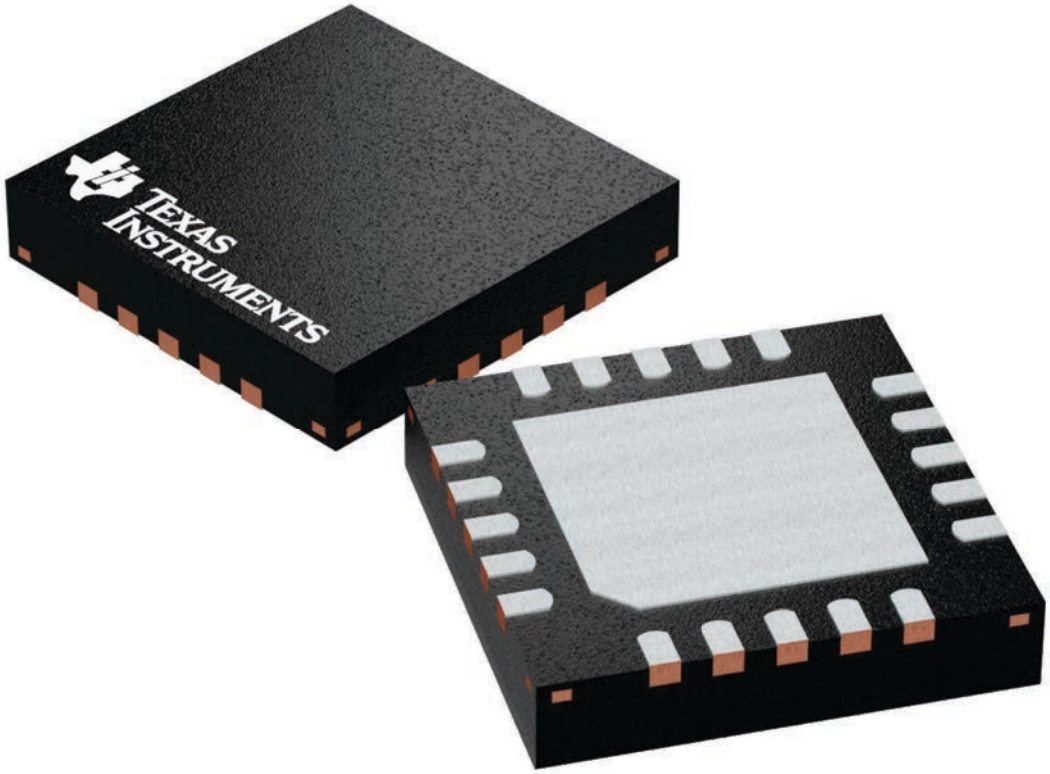
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

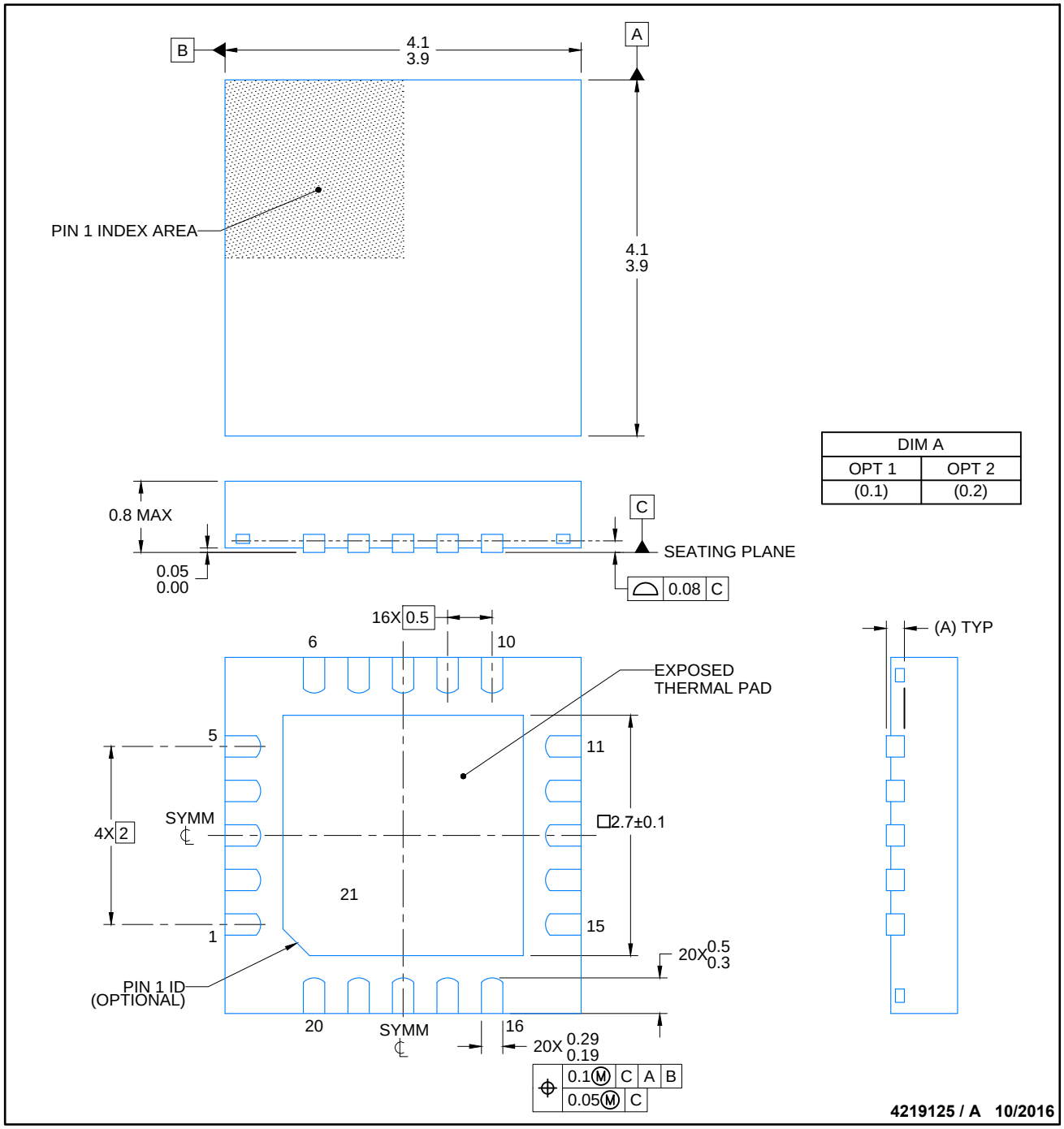


4224842/A

DATA BOOK
PACKAGE OUTLINE

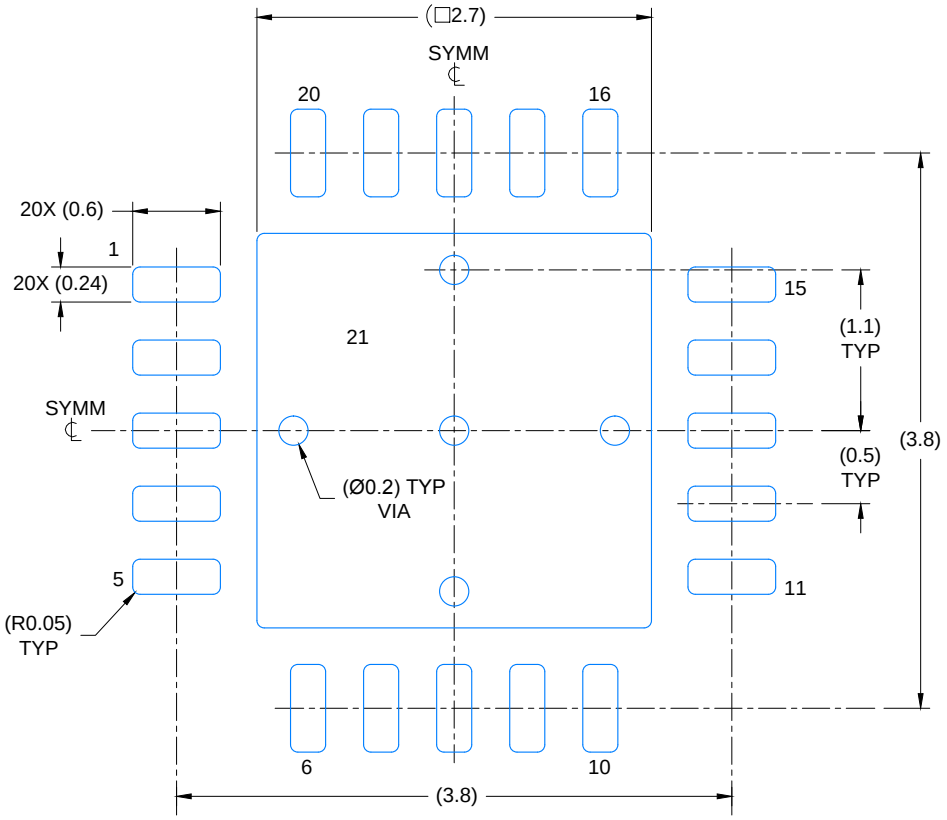
LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016		
ENGINEER: T. TANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	SCALE 15X / SIZE A / 4219125	REV A / PAGE 1 OF 5



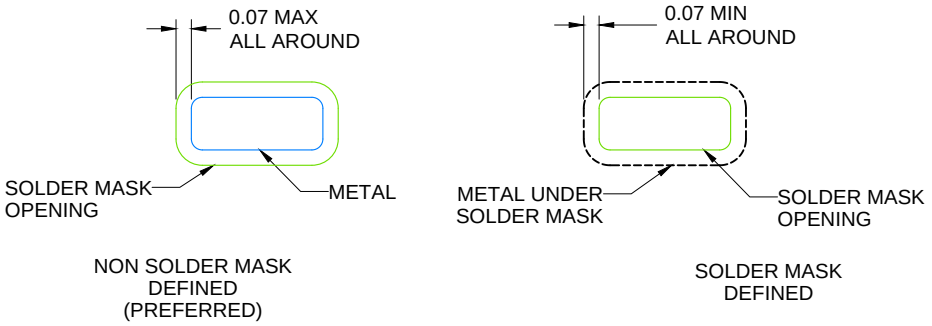
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

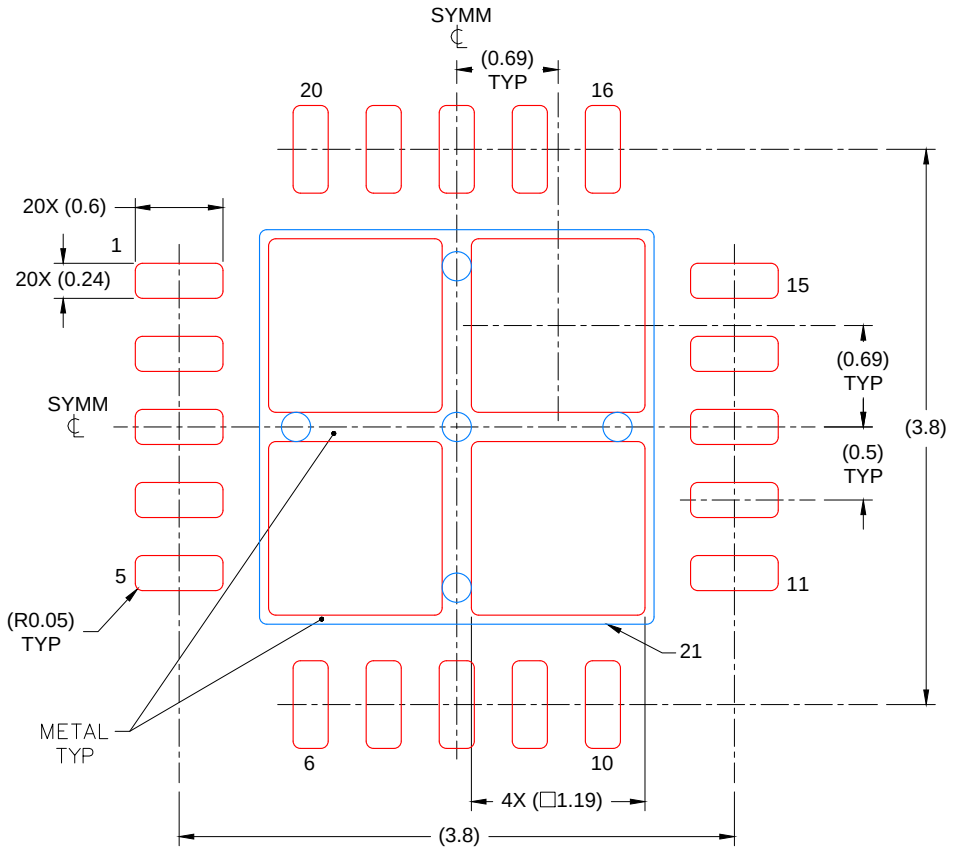


SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月