TVS2200 22V フラット・クランプ・サージ保護デバイス

1 特長

- 産業用信号ライン向け ±1kV、42Ω の IEC 61000-4-5 サージ・テストに耐える保護機能
- 最大クランプ電圧:28.4V (サージ電流 40A (8/20μs) 時)
- スタンドオフ電圧:22V
- 4mm^2 の小さい占有面積
- 125℃で 35A のサージ電流 (8/20μs) の反復ストライクを 5,000 回以上吸収
- 強力なサージ保護:
  – IEC 61000-4-5 (8/20μs):40A
  – IEC 61643-321 (10/1000μs):5A
- 小さいリーク電流:
  – 27℃で 3.5nA (標準値)
  – 85℃で 25nA (標準値)
- 低い静電容量:105pF
- レベル 4 IEC 61000-4-2 に準拠した ESD 保護機能を内蔵

2 アプリケーション

- 産業用センサ I/O
- 医療機器
- USB Type-C™ V_{bus}
- PLC I/O モジュール
- 電化製品

3 概要

TVS2200 は、最大 40A の IEC 61000-4-5 フォルト電流を確実にシャントして、システムを高電力過渡事象や落雷から保護します。一般的な産業用信号ラインの EMC 要件向けのソリューションとして、42Ω のインピーダンスにより結合される、最大 ±1kV の IEC 61000-4-5 開路電圧に耐えられます。

TVS2200 は、独自の帰還メカニズムの採用により、フォルト時に高精度のフラット・クランピングを実現し、システムがさらされる電圧を 30V 未満に抑えます。電圧レギュレーションが正確であるため、許容電圧の低いシステム部品を安心して選択でき、堅牢性を犠牲にすることなくシステムのコストと複雑さを抑えることができます。

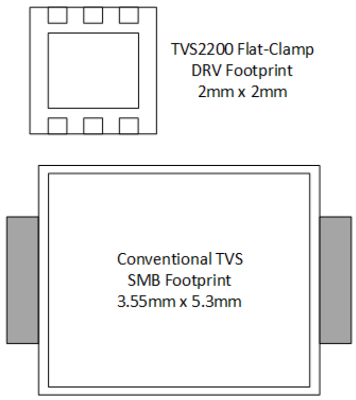
また、TVS2200 は占有面積が小さい 2mm × 2mm の SON パッケージで供給されるため、スペースの制約があるアプリケーションに最適であり、業界標準の SMA/SMB パッケージに比べて占有面積を 70% 削減できます。リーク電流と容量が極めて小さいため、保護するラインへの影響も最小限に抑えられます。製品のライフサイクル全体にわたる堅牢な保護を確保するため、テキサス・インスツルメンツは TVS2200 をテストし、高温で 5,000 回の反復サージに対してデバイス性能に変化がないことを確認しています。

TVS2200 はテキサス・インスツルメンツのフラット・クランプ・サージ・デバイス・ファミリの製品です。このファミリに含まれる他のデバイスの詳細については、製品比較表を参照してください。

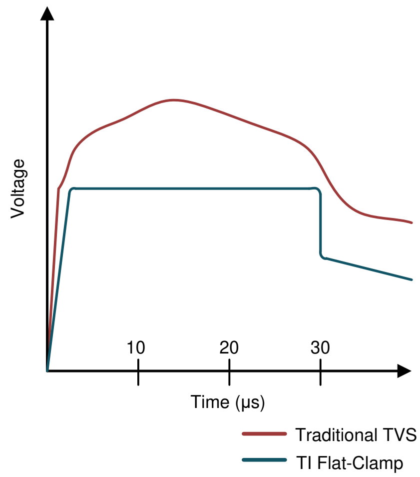
パッケージ情報

部品番号(1)	パッケージ(2)	パッケージ・サイズ (3)
TVS2200	DRV (SON、6)	2mm × 2mm

(1) 製品比較表を参照してください。
(2) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(3) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



占有面積の比較



8µs～20µs のサージに対する電圧クランプの応答

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2023) to Revision C (August 2023) — **Page**

- Updated the *Pin Configuration and Functions* section.......... 4

Changes from Revision A (March 2018) to Revision B (July 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.......... 1
- TVS2200DRCR の湿度感度レベルを次のように変更:2 から 1.......... 1
- 「パッケージ情報」表を更新 1

Changes from Revision * (December 2017) to Revision A (March 2018) — **Page**

- デバイスのステータスを「事前情報」から「量産データ」に変更.......... 1
- Updated the *DRV Package, 6-Pin SON (Top View)* figure.......... 4

5 Device Comparison Table

Device	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 µs)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional

6 Pin Configuration and Functions

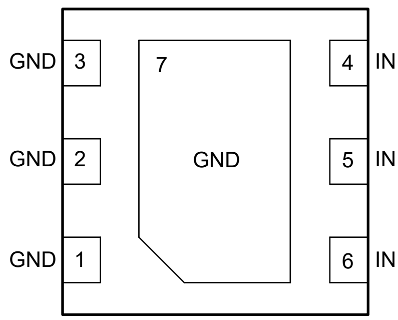

図 6-1. DRV Package, 6-Pin SON (Bottom View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	1	G	Ground
	2		
	3		
IN	4	I	ESD and surge protected channel
	5		
	6		
Exposed thermal pad		GND	Ground

(1) I = input, GND = ground

7 Specifications

7.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs)		40	A
	IEC 61000-4-5 Power (8/20 µs)		1120	W
	IEC 61643-321 Current (10/1000 µs)		5	A
	IEC 61643-321 Power (10/1000 µs)		145	W
Maximum Forward Surge	IEC 61000-4-5 Current (8/20 µs)		50	A
	IEC 61000-4-5 Power (8/20 µs)		80	W
	IEC 61643-321 Current (10/1000 µs)		23	A
	IEC 61643-321 Power (10/1000 µs)		60	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{BR}	DC Breakdown current		18	mA
I_F	DC Forward Current		500	mA
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±17	kV
		IEC 61000-4-2 air-gap discharge	±30	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage			22	V

7.5 Thermal Information

THERMAL METRIC[(1)]		TVS2200 DRV (SON) 6 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	70.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	73.7	°C/W
R_{qJB}	Junction-to-board thermal resistance	40	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	40.3	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	11	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		-0.5		22	V
I_{LEAK}	Leakage Current	Measured at V_{IN} = V_{RWM} T_A = 27°C		3.5	62	nA
		Measured at V_{IN} = V_{RWM} T_A = 85°C		25	400	nA
		Measured at V_{IN} = V_{RWM} T_A = 105°C		80	1300	nA
V_F	Forward Voltage	I_{IN} = 1 mA from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	I_{IN} = 1 mA from IO to GND	24.6	25.9	27.6	V
V_{FCLAMP}	Forward Clamp Voltage	40 A IEC 61000-4-5 Surge (8/20 µs) from GND to IO, 27°C	1	2	5	V
V_{CLAMP}	Clamp Voltage	24 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C		27.2	27.7	V
		40 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C		27.6	28	V
		35 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = V_{RWM} before surge, T_A = 125°C		27.8	28.35	V
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{pp} and I_{pp} surge current levels, 27°C		30		mΩ
C_{IN}	Input pin capacitance	V_{IN} = V_{RWM}, f = 1 MHz, 30 mV_{pp}, IO to GND		105		pF
SR	Maximum Slew Rate	0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PK} = 1 mA, 27°C		2.5		V/µs
		0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PK} = 1 mA, 105°C		0.7		V/µs

7.7 Typical Characteristics

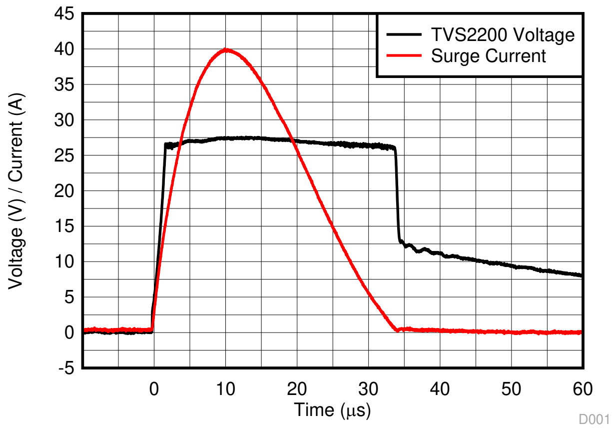

図 7-1. Surge Response at 40 A

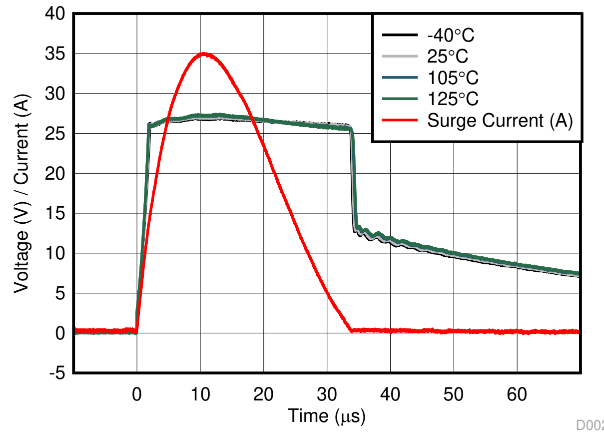

図 7-2. Surge Response at 35 A Across Temperature

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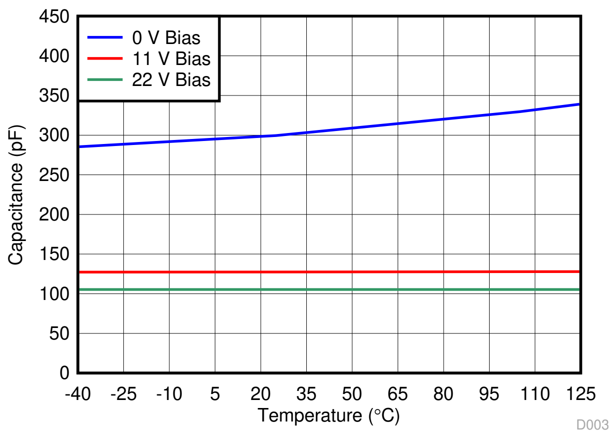


f = 1 MHz, 30 mVpp, IO to GND

図 7-3. Capacitance vs Temperature Across Bias

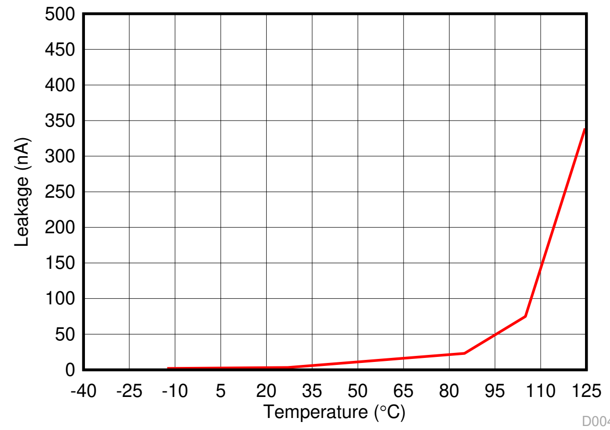


図 7-4. Leakage Current vs Temperature at 22 V

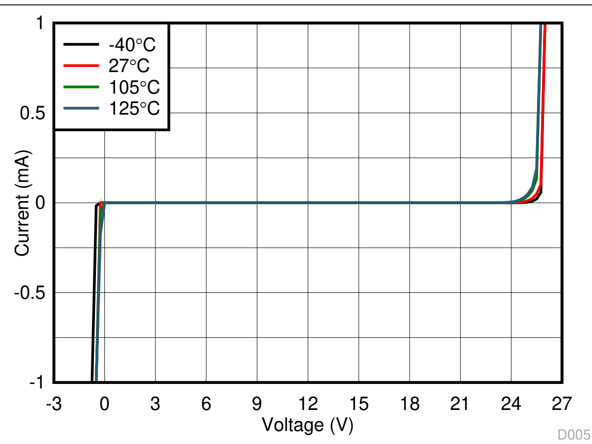


図 7-5. IV Across Temperature

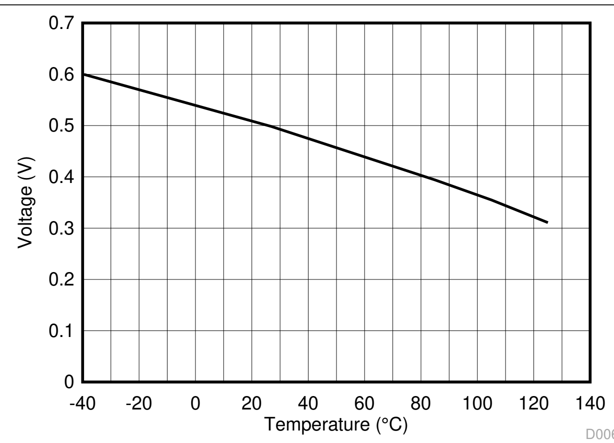


図 7-6. Forward Voltage vs Temperature Across Current

7.7 Typical Characteristics (continued)

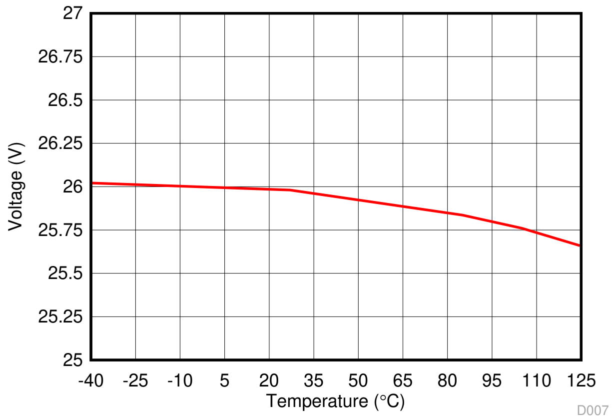


図 7-7. Breakdown Voltage at 1 mA vs Temperature

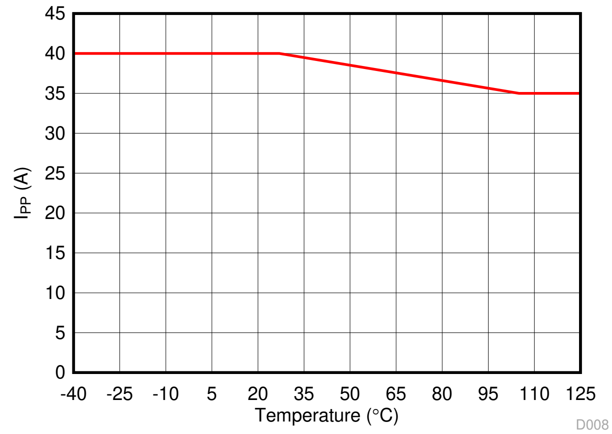


図 7-8. Maximum Surge Current (8/20 µs) vs Temperature

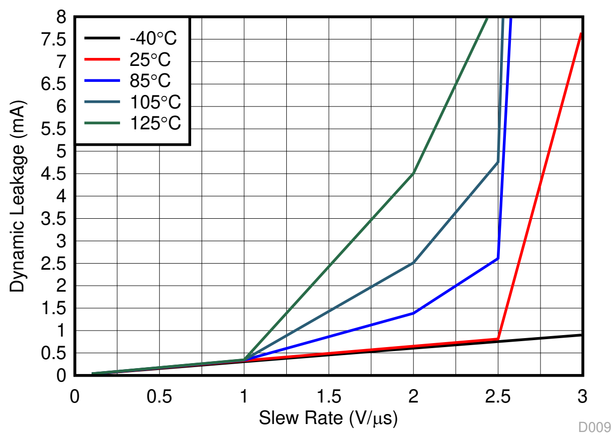


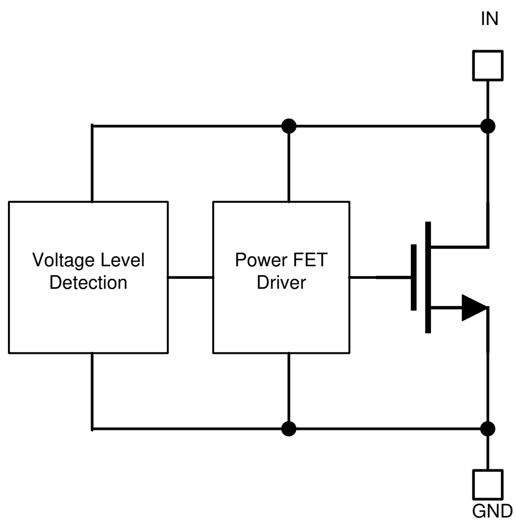
図 7-9. Maximum Leakage vs Signal Slew Rate Across Temperature

8 Detailed Description

8.1 Overview

The TVS2200 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot. For a detailed overview of the Flat-Clamp family of devices, please reference TI's *Flat-Clamp surge protection technology for efficient system protection* white paper. This document explains in detail the functional operation of the devices and how they impact and improve system design.

8.2 Functional Block Diagram



8.3 Feature Description

The TVS2200 is a precision clamp that handles 40 A of IEC 61000-4-5 8/20 µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost lower voltage tolerant downstream ICs. The TVS2200 has minimal leakage under the standoff voltage of 22 V, making it a good candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of –40°C to +125°C makes it a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

8.4 Reliability Testing

For device reliability, the TVS2200 is characterized against 5000 repetitive pulses of 35 A IEC 61000-4-5 8/20 µs surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst case scenarios for fault regulation. After each surge pulse, the TVS2200 clamping voltage, breakdown voltage, and leakage are recorded so that there is no variation or performance degradation. By design, the robust, reliable, high temperature protection of the TVS2200 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.5 Device Functional Modes

8.5.1 Protection Specifications

The TVS2200 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required in relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 µs and a half length of 20 µs while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 µs and a half length of 1000 µs.

The positive and negative surges are imposed to the TVS2200 by a combinational waveform generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductance's are usually used to decouple the transient stress and protect the power supply. By design, the TVS2200 is post tested so that there is no shift in device breakdown or leakage at V_{rwm}.

In addition, the TVS2200 has been tested according to IEC 61000-4-5 to pass a ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS2200 will serve as a good protection solution for applications with that requirement.

The TVS2200 also integrates IEC 61000-4-2 Level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine so that the device can be protected against all transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference *TI's IEC 61000-4-x Testing Application Note*.

8.5.2 Minimal Derating

Unlike traditional diodes the TVS2200 has very little derating of maximum power dissipation and allows for robust performance up to 125°C shown in 図 7-8. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS2200 prevents this and allows for the same level of protection regardless of temperature.

8.5.3 Transient Performance

During large transient swings, the TVS2200 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. In order to keep power dissipation low and remove the chance of signal distortion, it is recommended to keep the slew rate of any input signal on the TVS2200 below 2.5 V/µs at room temperature and below 0.7 V/µs at 125°C shown in 図 7-9. Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however if the fast input voltage swings occur regularly it can cause device overheating.

9 Application and Implementation

注

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9.1 Application Information

The TVS2200 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

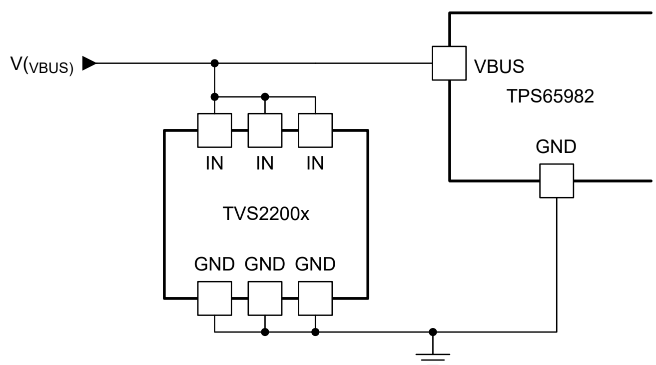

図 9-1. TVS2200 Application

9.2.1 Design Requirements

A typical operation for the TVS2200 would be protecting a USB Type-C V_{bus} input, with a nominal input voltage of 20 V and a required withstand of 22 V, shown in 図 9-1. In this example, a TVS2200 is protecting the input to a TPS65982 Type-C Port Controller. Without any input protection, if a surge event is caused by lightning, coupling, hot-swap ringing, or any other fault condition this input voltage will rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device.

9.2.2 Detailed Design Procedure

If the TVS2200 is in place to protect the device, during a surge event the voltage will rise to the breakdown of the diode at 25.9 V, and then the TVS2200 will turn on, shunting the surge current to ground. With the low dynamic resistance of the TVS2200, even large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS2200 is around 30 mΩ, which means 40 A of surge current will cause a voltage raise of 40 A × 30 mΩ = 1.2 V. Because the device turns on at 25.9 V, this means the input will be exposed to a maximum of 25.9 V + 1.2 V = 27.1 V during surge pulses, robustly protecting the USB Type-C port. This pulse is shown in 図 9-2 and allows for robust protection of the circuit.

Finally, the small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS2200 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current will take through the system compared to larger protection solutions.

9.2.3 Application Curves

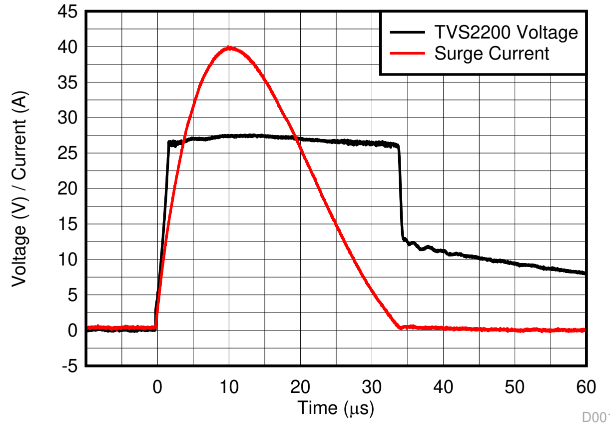

図 9-2. TVS2200 Surge Response at 40 A

9.2.4 Configuration Options

The TVS2200 can be used in either unidirectional or bidirectional configuration. The TVS2200 shows unidirectional usage to protect an input. By placing two TVS2200's in series with reverse orientation, bidirectional operation can be used which will allow a working voltage of ±22 V. TVS2200 operation in bidirectional will be similar to unidirectional operation, with a minor increase in breakdown voltage and clamping voltage. The TVS3300 bidirectional performance has been characterized in the *TVS3300 Configurations Characterization*. While the TVS2200 in bidirectional configuration has not specifically been characterized, it will have similar relative changes to the TVS3300 in bidirectional configuration.

9.3 Power Supply Recommendations

The TVS2200 is a clamping device so there is no need to power it. Take care to not violate the recommended V_{IN} voltage range (0 V to 22 V) so that the device functions properly.

9.4 Layout

9.4.1 Layout Guidelines

The optimum placement is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces as straight as possible.

Eliminate any sharp corners on the protected traces between the TVS2200 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

9.4.2 Layout Example

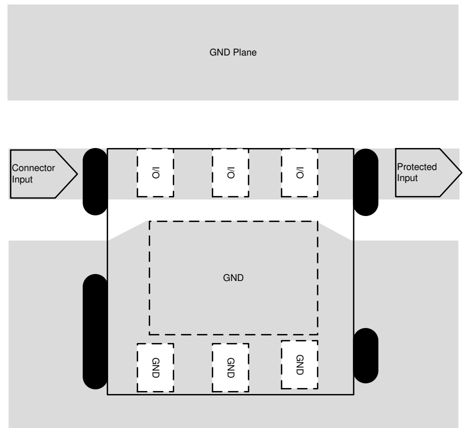

図 9-3. TVS2200 Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Flat-Clamp surge protection technology for efficient system protection*
- Texas Instruments, *TI's IEC 61000-4-x Testing Application Note*.
- Texas Instruments, *TVS3300 Configurations Characterization*

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TVS2200DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HVH
TVS2200DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HVH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

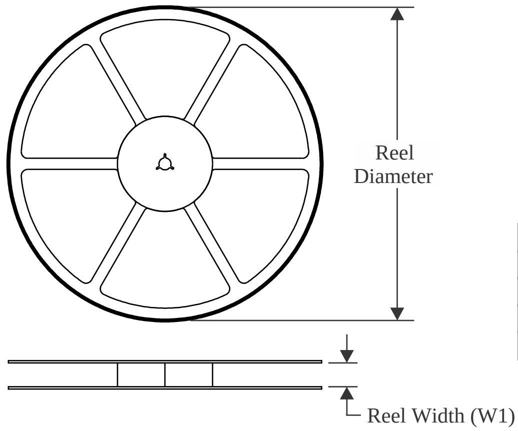
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

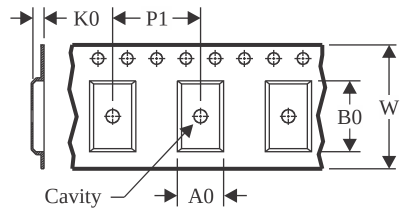
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

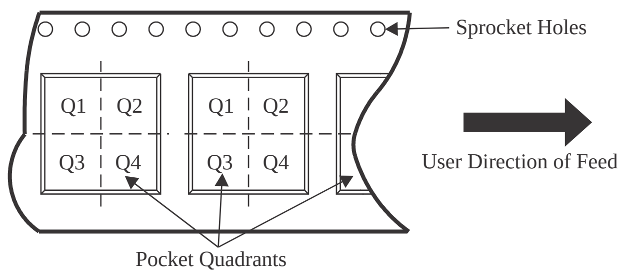


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

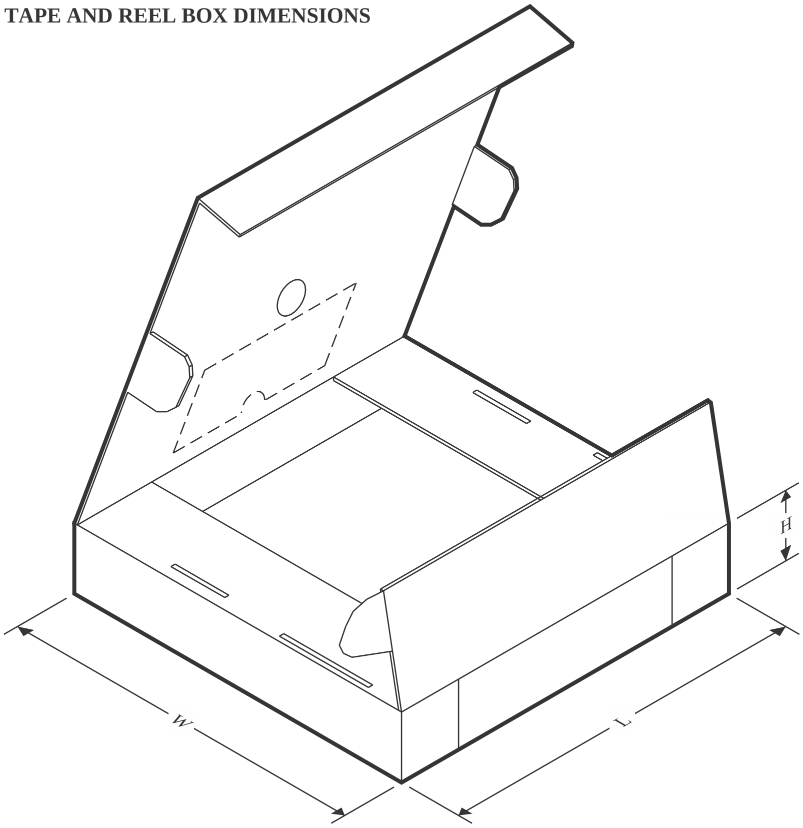
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS2200DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

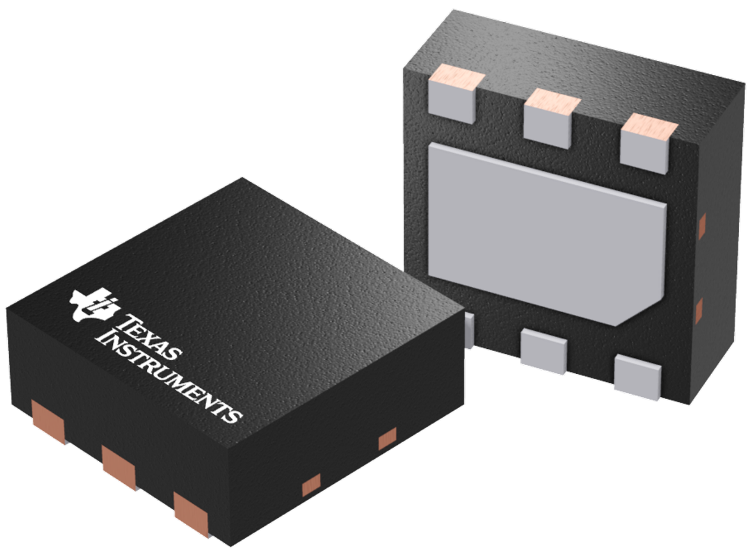


*All dimensions are nominal

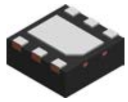
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS2200DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



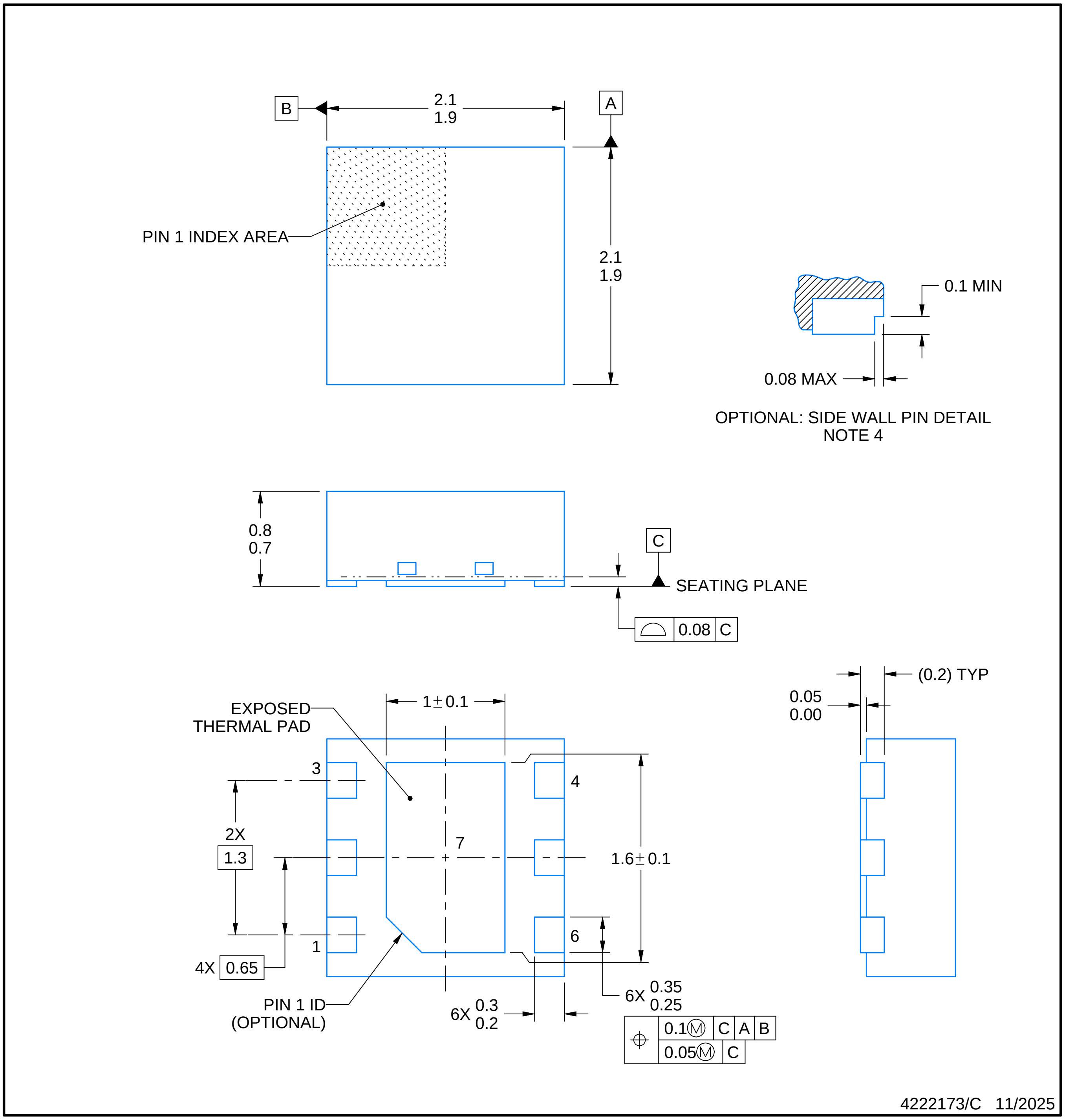
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

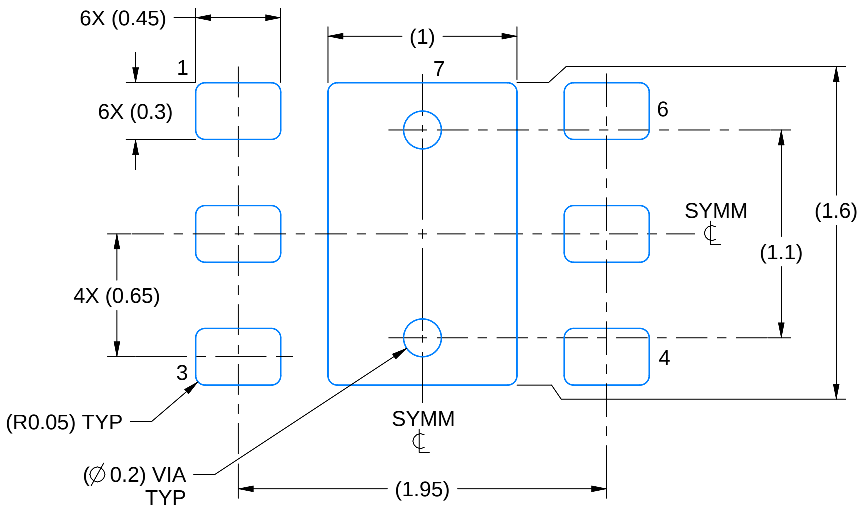
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

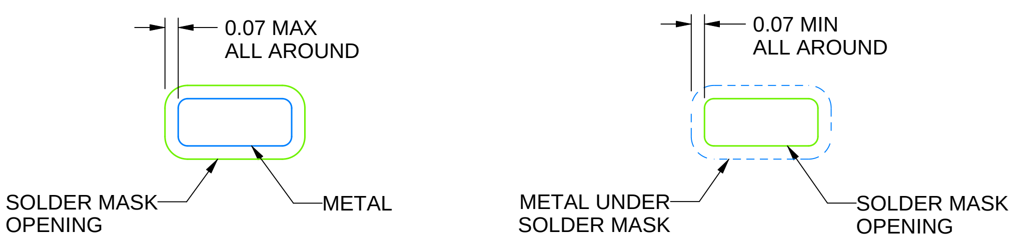


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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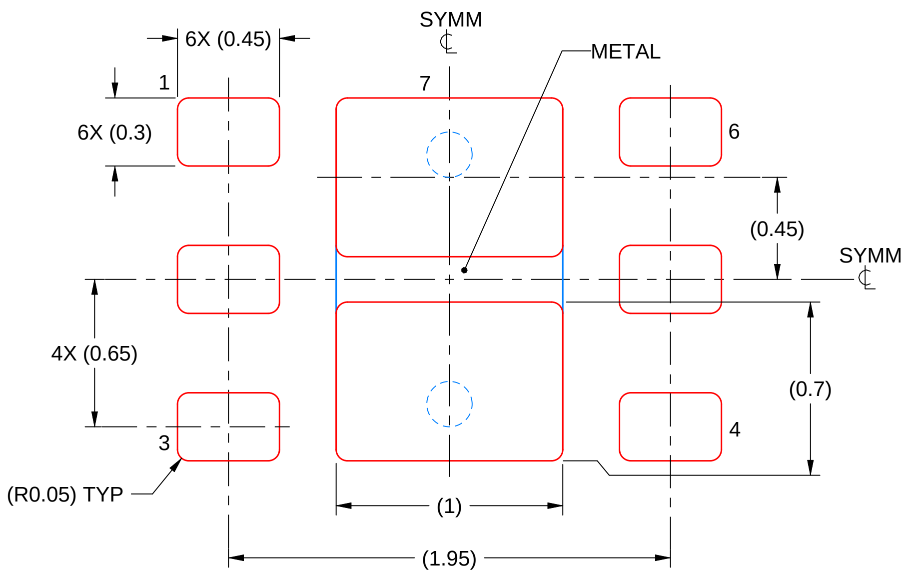
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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