TVS3300 33Vフラットクランプ・サージ保護デバイス

1 特長

- 産業用信号ライン向け1kV、42ΩのIEC 61000-4-5サージ・テストに耐える保護機能
- 最大クランプ電圧: サージ電流35A (8/20µs)で40V
- スタンドオフ電圧: 33V
- 小型の1.1mm^2 WCSPおよび4mm^2 SONフットプリント
- 125℃で30Aのサージ電流(8/20µs)の反復ストライクを4,000回吸収
- 強力なサージ保護
  - IEC61000-4-5 (8/20µs): 35A
  - IEC61643-321 (10/1000µs): 4A
- 低リーク電流
  - 27℃で19nA (標準値)
  - 85℃で28nA (標準値)
- 低容量: 130pF
- レベル4 IEC 61000-4-2に準拠したESD保護機能を内蔵

2 アプリケーション

- 産業用センサ
- PLC I/Oモジュール
- 24Vの電源ラインまたはデジタル・スイッチング・ライン
- 4/20 mAループ
- 家電製品
- 医療用機器
- モータ・ドライバ

3 概要

TVS3300は、最大35AのIEC 61000-4-5フォルト電流を確実にシャントして、システムを高電力過渡事象や落雷から保護します。一般的な産業用信号ラインのEMC要件向けのソリューションとして、42Ωのインピーダンスにより結合される、最大1kVのIEC 61000-4-5開路電圧に耐えられます。TVS3300は、独自の帰還メカニズムの採用により、フォルト時に高精度のフラット・クランピングを実現し、システムがさらされる電圧を40V未満に抑えます。電圧レギュレーションが正確であるため、許容電圧の低いシステム部品を安心して選択でき、堅牢性を犠牲にすることなくシステムのコストと複雑さを抑えることができます。

さらに、TVS3300は小型の1mm×1.1mm WCSPおよび2mm×2mm SONフットプリントで供給され、スペースの制約されるアプリケーションに理想的で、業界標準のSMAおよびSMBパッケージと比べて90%もサイズを削減できます。リーク電流と容量が極めて低いことから、保護するラインへの影響も最小限に抑えられます。製品のライフサイクル全体にわたる堅牢な保護を保証するために、TIはTVS3300に対し高温で4000回の反復サージが発生するテストを実施し、性能に変化がないことを確認しています。

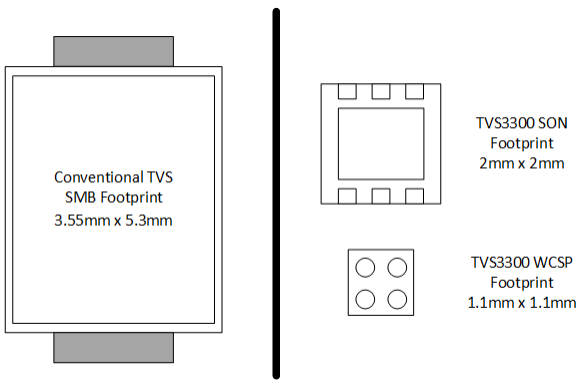
TVS3300はTIのフラットクランプ・サージ・デバイス・ファミリの製品です。ファミリの他のデバイスについては、「*デバイス比較表*」を参照してください。

製品情報(1)

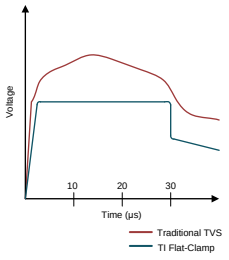
型番	パッケージ	本体サイズ(公称)
TVS3300	WCSP (4)	1.062mm×1.116mm
	SON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

占有面積の比較



8/20µsのサージ・イベントに対する電圧クランプの応答



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4 改訂履歴

Revision B (April 2017) から **Revision C** に変更 **Page**

- 他のTVSxx00ファミリのデバイスと一致するようデータシートを修正 ... 1

Revision A (March 2017) から **Revision B** に変更 **Page**

- Updated standard for (10/1000 μs) from IEC 61000-4-5 to IEC 61643-321 in the *Absolute Maximum Ratings* table ... 5

2017年UNDEFINED月 発行のものから更新 **Page**

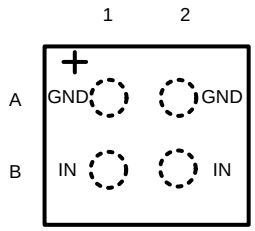
- SONパッケージ・オプション 追加 ... 1
- 「*特長*」セクションに±11kV接触放電(SOn)を 追加 ... 1
- Added Peak pulse—clamping direction specs for SON package in the *Absolute Maximum Ratings* table ... 5
- Added IEC 61000-4-2 contact discharge spec for SON package in the *ESD Ratings - IEC* table ... 5
- Added T_A = 27°C condition to dynamic resistance in the *Electrical Characteristics* table ... 5

5 Device Comparison Table

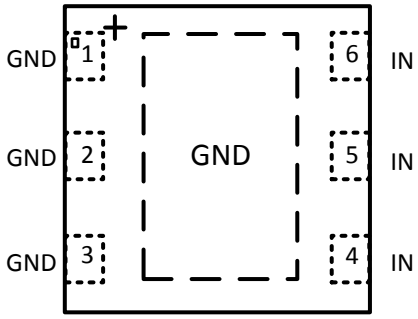
Device	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 µs)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional

6 Pin Configuration and Functions

YZF Package
4-Pin WCSP
Top View



DRV Package
6-Pin SON
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	YZF	DRV		
IN	B1, B2	4, 5, 6	I	ESD and surge protected channel
GND	A1, A2	1, 2, 3, exposed thermal pad	GND	Ground

7 Specifications

7.1 Absolute Maximum Ratings

T_A = 27℃ (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs)		35	A
	IEC 61000-4-5 Power (8/20 µs)		1330	W
	IEC 61643-321 Current (10/1000 µs) - WCSP		4	A
	IEC 61643-321 Power (10/1000 µs) - WCSP		150	W
	IEC 61643-321 Current (10/1000 µs) - DRV		3.5	A
	IEC 61643-321 Power (10/1000 µs) - DRV		125	W
Maximum Forward Surge	IEC 61000-4-5 Current (8/20 µs)		50	A
	IEC 61000-4-5 Power (8/20 µs)		80	W
	IEC 61643-321 Current (10/1000 µs)		23	A
	IEC 61643-321 Power (10/1000 µs)		60	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{BR}	DC Breakdown Current - DRV		10	mA
I_F	DC Forward Current		500	mA
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±11	kV
		IEC 61000-4-2 air-gap discharge	±30	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		33		V

7.5 Thermal Information

THERMAL METRIC(1)		TVS3300		UNIT
		YZF (WCSP)	DRV (SON)	
		4 PINS	6 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	173.8	70.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	1.7	73.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Thermal Information (continued)

THERMAL METRIC(1)		TVS3300		UNIT
		YZF (WCSP)	DRV (SON)	
		4 PINS	6 PINS	
R_{qJB}	Junction-to-board thermal resistance	47.1	40	°C/W
Y_{JT}	Junction-to-top characterization parameter	9.5	2.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	47.1	40.3	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	11	°C/W

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$, T_A = 27°C		19	150	nA
		Measured at $V_{IN} = V_{RWM}$, T_A = 85°C		28	600	nA
V_F	Forward Voltage	I_{IN} = 1 mA from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	I_{IN} = 1 mA from IO to GND	34	35.8	39	V
V_{FCLAMP}	Forward Clamp Voltage	35 A IEC 61000-4-5 Surge (8/20 µs) from GND to IO, 27°C	1	2	5	V
V_{CLAMP}	Clamp Voltage	15 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C	34	37	40	V
		35 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C	34	38	40	V
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at 15 A and 30 A surge current levels, 27°C		40	60	mΩ
C_{IN}	Input pin capacitance	V_{IN} = 12 V, f = 1 MHz, 30 mV_{pp}, IO to GND	110	130	150	pF
SR	Maximum Slew Rate	0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, 27°C		2.5		V/µs
		0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, 105°C		0.7		V/µs

7.7 Typical Characteristics

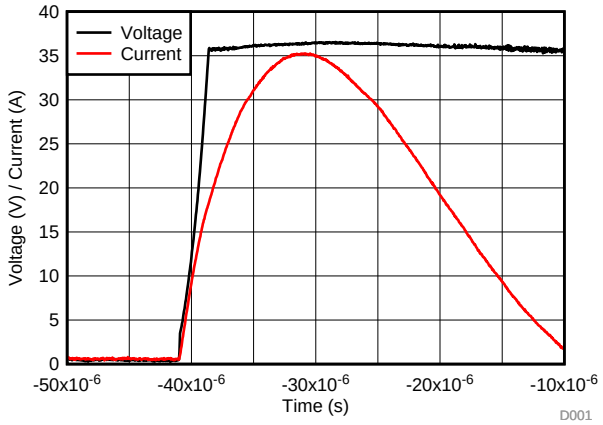


図 1. 8/20 µs Surge Response at 35 A

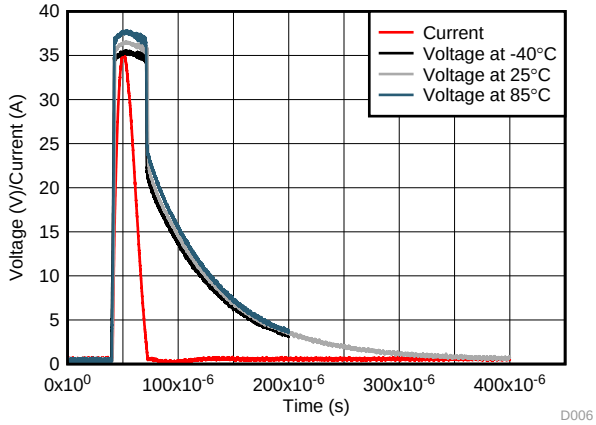
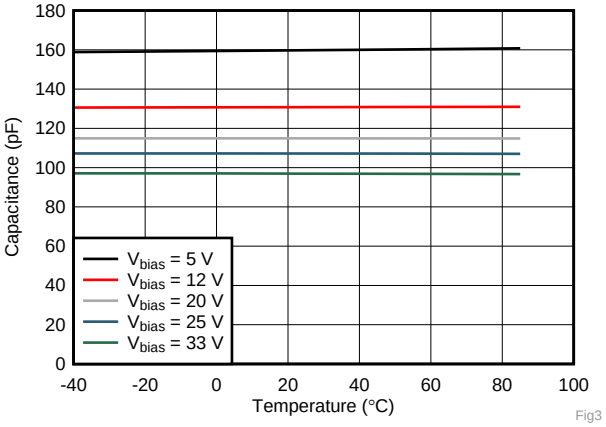


図 2. 8/20 µs Surge Response at 35 A Across Temperature



f = 1 MHz, 30 mVpp, IO to GND

図 3. Capacitance vs Temperature Across Bias

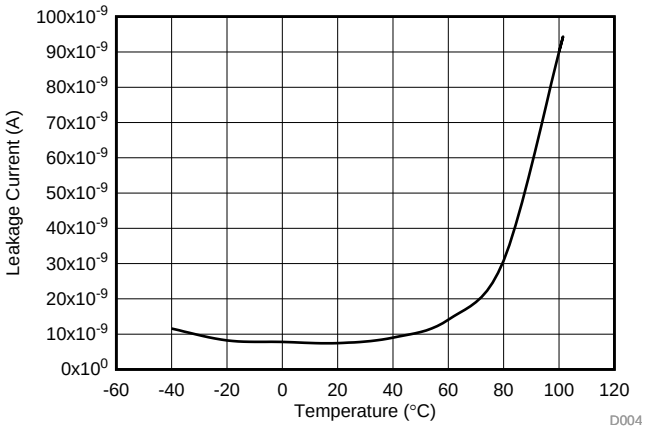


図 4. Leakage Current vs Temperature at 33 V

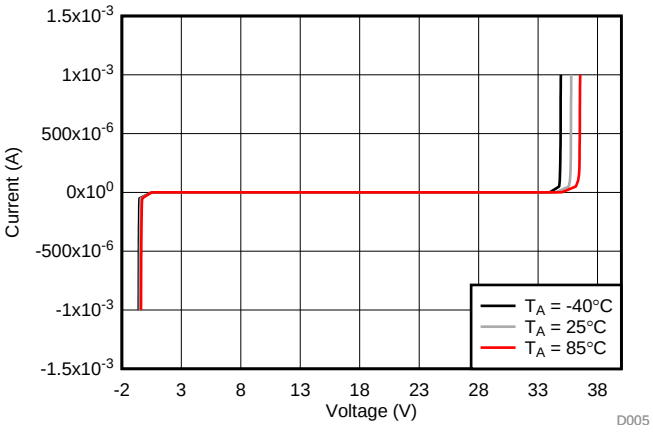


図 5. I/V Curve Across Temperature

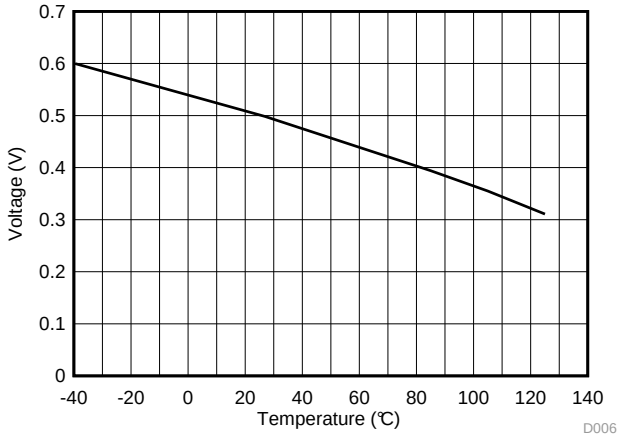


図 6. Forward Voltage vs Temperature

Typical Characteristics (continued)

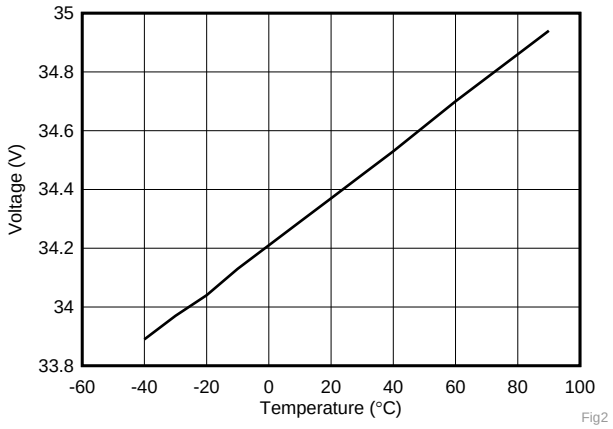


図 7. Breakdown Voltage (1 mA) vs Temperature

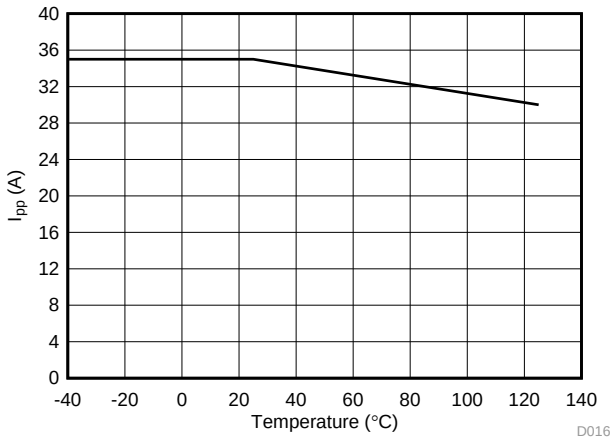


図 8. Max Surge Current (8/20 µs) vs Temperature

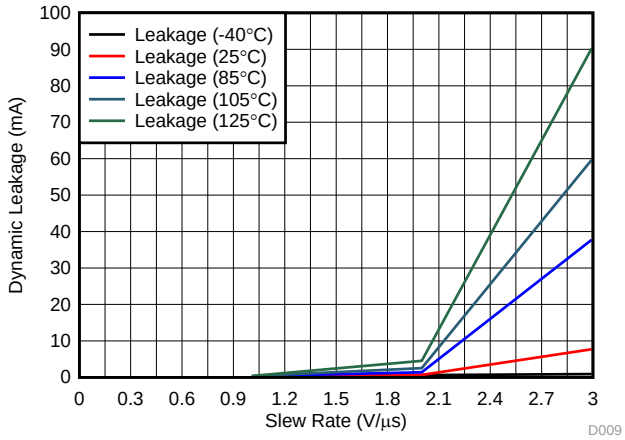


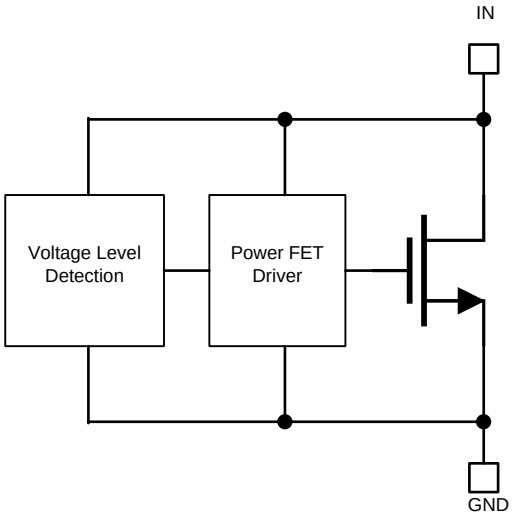
図 9. Dynamic Leakage vs Signal Slew Rate across Temperature

8 Detailed Description

8.1 Overview

The TVS3300 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot.

8.2 Functional Block Diagram



8.3 Feature Description

The TVS3300 is a precision clamp that handles 35 A of IEC 61000-4-5 8/20 µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. The TVS3300 has minimal leakage under the standoff voltage of 33 V, making it an ideal candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of –40°C to +125°C a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

8.4 Reliability Testing

To ensure device reliability, the TVS3300 is characterized against 4000 repetitive pulses of 30 A IEC 61000-4-5 8/20 µs surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst case scenarios for fault regulation. After each surge pulse, the TVS3300 clamping voltage, breakdown voltage, and leakage are recorded to ensure that their is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS3300 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.5 Device Functional Modes

8.5.1 Protection Specifications

The TVS3300 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required in relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standards requires protection against a pulse with a rise time of 8 µs and a half length of 20 µs, while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 µs and a half length of 1000 µs.

Device Functional Modes (continued)

The positive and negative surges are imposed to the TVS3300 by a combinational waveform generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply. The TVS3300 is post tested by assuring that there is no shift in device breakdown or leakage at V_{rwm}.

In addition, the TVS3300 has been tested according to IEC 61000-4-5 to pass a ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS3300 will serve an ideal protection solution for applications with that requirement.

The TVS3300 allow integrates IEC 61000-4-2 level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against most transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference TI's IEC 61000-4-x Testing Application Note

8.5.2 Minimal Derating

Unlike traditional diodes the TVS3300 has very little derating of max power dissipation and ensures robust performance up to 125°C, shown in 図 8. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS3300 prevents this and ensures that you will see the same level of protection regardless of temperature.

8.5.3 Transient Performance

During large transient swings, the TVS3300 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. In order to keep power dissipation low and remove the chance of signal distortion, it is recommended to keep the slew rate of any input signal on the TVS3300 below 2.5 V/µs at room temperature and below 0.7 V/µs at 125°C shown in 図 9. Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however if the fast input voltage swings occur regularly it can cause device overheating.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TVS3300 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

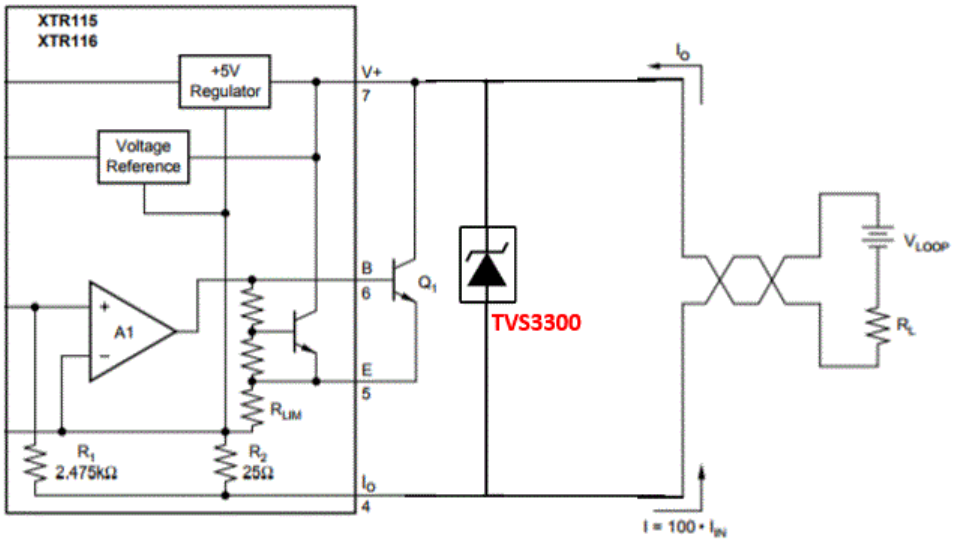


図 10. TVS3300 Application Schematic

9.2.1 Design Requirements

A typical operation for the TVS3300 would be protecting an analog output module on a PLC similar to 図 10. In this example, the TVS3300 is protecting a 4-20 mA transmitter that uses the XTR115, a standard transmitter that has a nominal voltage of 24 V and a maximum input voltage of 40 V. Most industrial interfaces such as this require protection against ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor, equaling roughly 24 A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition this input voltage will rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device. An ideal surge protection diode will maximize the useable voltage range while still clamping at a safe level for the system, TI's Flat-Clamp technology provides the best protection solution.

9.2.2 Detailed Design Procedure

If the TVS3300 is in place to protect the device, during a surge event the voltage will rise to the breakdown of the diode at 35.8 V, and then the TVS3300 will turn on, shunting the surge current to ground. With the low dynamic resistance of the TVS3300, large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS3300 is around 40 mΩ, which means 24 A of surge current will cause a voltage raise of 24 A × 40 mΩ = 0.96 V. Because the device turns on at 35.8 V, this means the XTR115 input will be exposed to a maximum of 35.8 V + 0.96 V = 36.76 V during surge pulses, well within the absolute maximum input voltage. This ensures robust protection of your circuit.

Typical Application (continued)

The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS3300 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current will take through the system compared to larger protection solutions.

Finally, the low leakage of the TVS3300 will have low input power losses. At 33 V, the device will see typical 19 nA leakage for a constant power dissipation of less than 100 µW, a small quantity that will minimally effect overall efficiency metrics and heating concerns.

9.2.3 PLC Surge Protection Reference Design

For a detailed description of the TVS3300 advantages in a PLC Analog Input Module, reference TI's Surge Protection Reference Design for PLC Analog Input Module This document describes the considerations and performance of the TVS3300 in a common industrial application.

9.2.4 Configuration Options

The TVS3300 can be used in either unidirectional or bidirectional configuration. By placing two TVS3300's in series with reverse orientation bidirectional operation can be used, allowing a working voltage of ±33 V. TVS3300 operation in bidirectional will be similar to unidirectional operation, with a minor increase in breakdown voltage and clamping voltage. The TVS3300 bidirectional performance has been characterized in the TVS3300 Configurations Characterization.

10 Power Supply Recommendations

The TVS3300 is a clamping device so there is no need to power it. To ensure the device functions properly do not violate the recommended V_{IN} voltage range (0 V to 33 V) .

11 Layout

11.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces straight.

Eliminate any sharp corners on the protected traces between the TVS3300 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

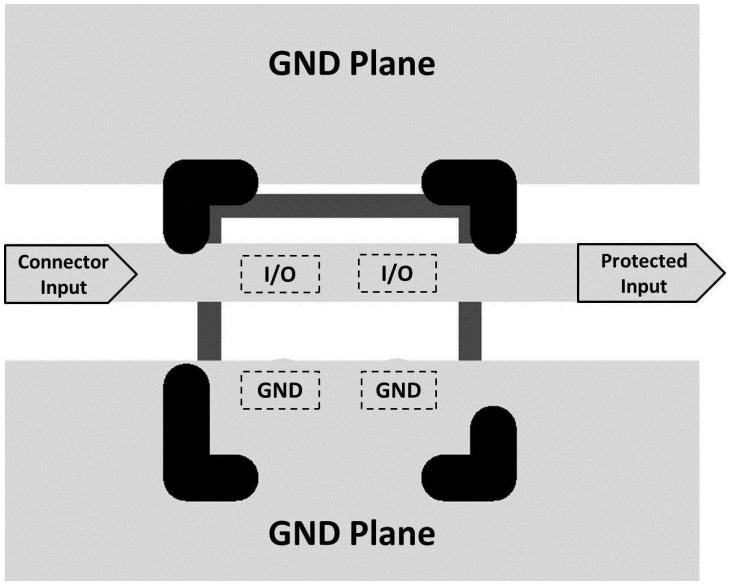


図 11. TVS3300 WCSP Layout

Layout Example (continued)

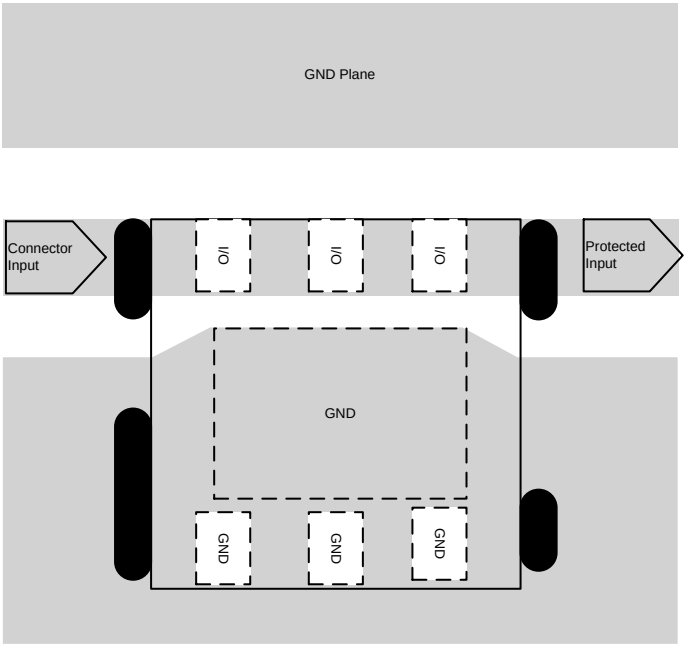


図 12. TVS3300 SON Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『フラットクランプTVS評価キット』*
- PLCアナログ入力モジュール用のサージ保護リファレンス・デザイン
- *『TVS3300評価モジュール ユーザー・ガイド』*
- *『TVS3300DRV評価モジュール ユーザー・ガイド』*

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.4 商標

E2E is a trademark of Texas Instruments.

12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TVS3300DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	17JH
TVS3300DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	17JH
TVS3300DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	17JH
TVS3300DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	17JH
TVS3300YZFR	Active	Production	DSBGA (YZF) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15K
TVS3300YZFR.A	Active	Production	DSBGA (YZF) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	15K

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

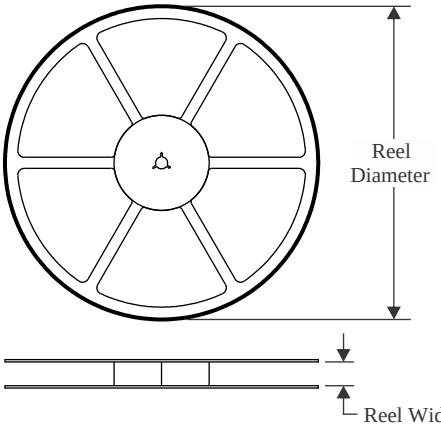
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

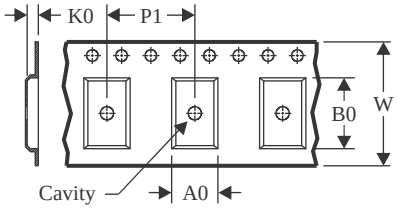
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

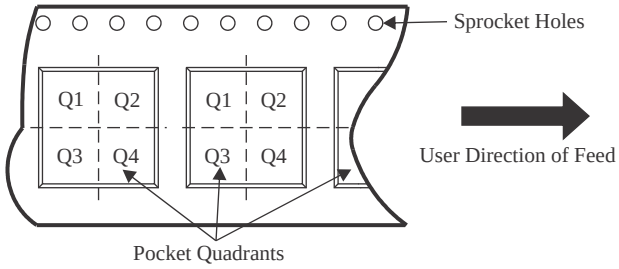


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

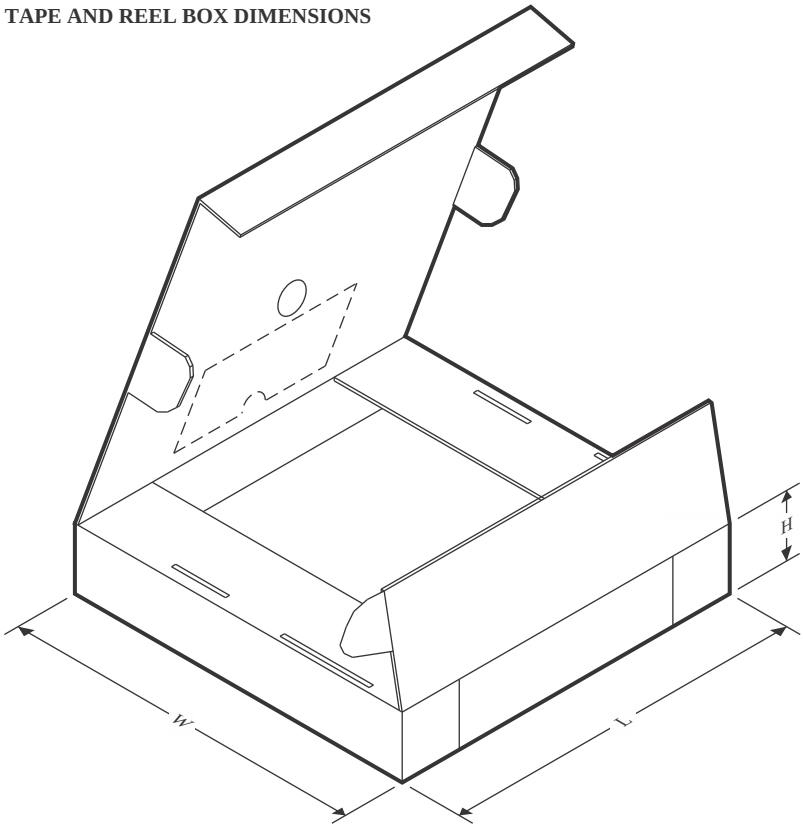
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS3300DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TVS3300DRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TVS3300YZFR	DSBGA	YZF	4	3000	180.0	8.4	1.17	1.22	0.72	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

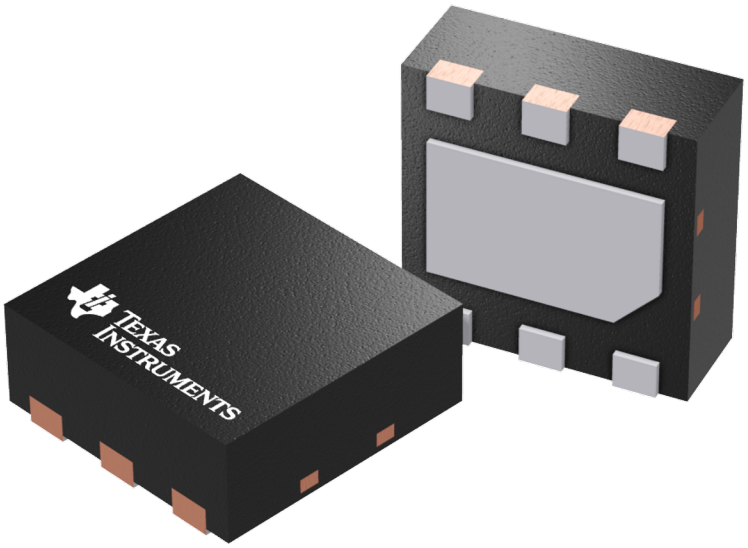


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS3300DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TVS3300DRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TVS3300YZFR	DSBGA	YZF	4	3000	182.0	182.0	20.0

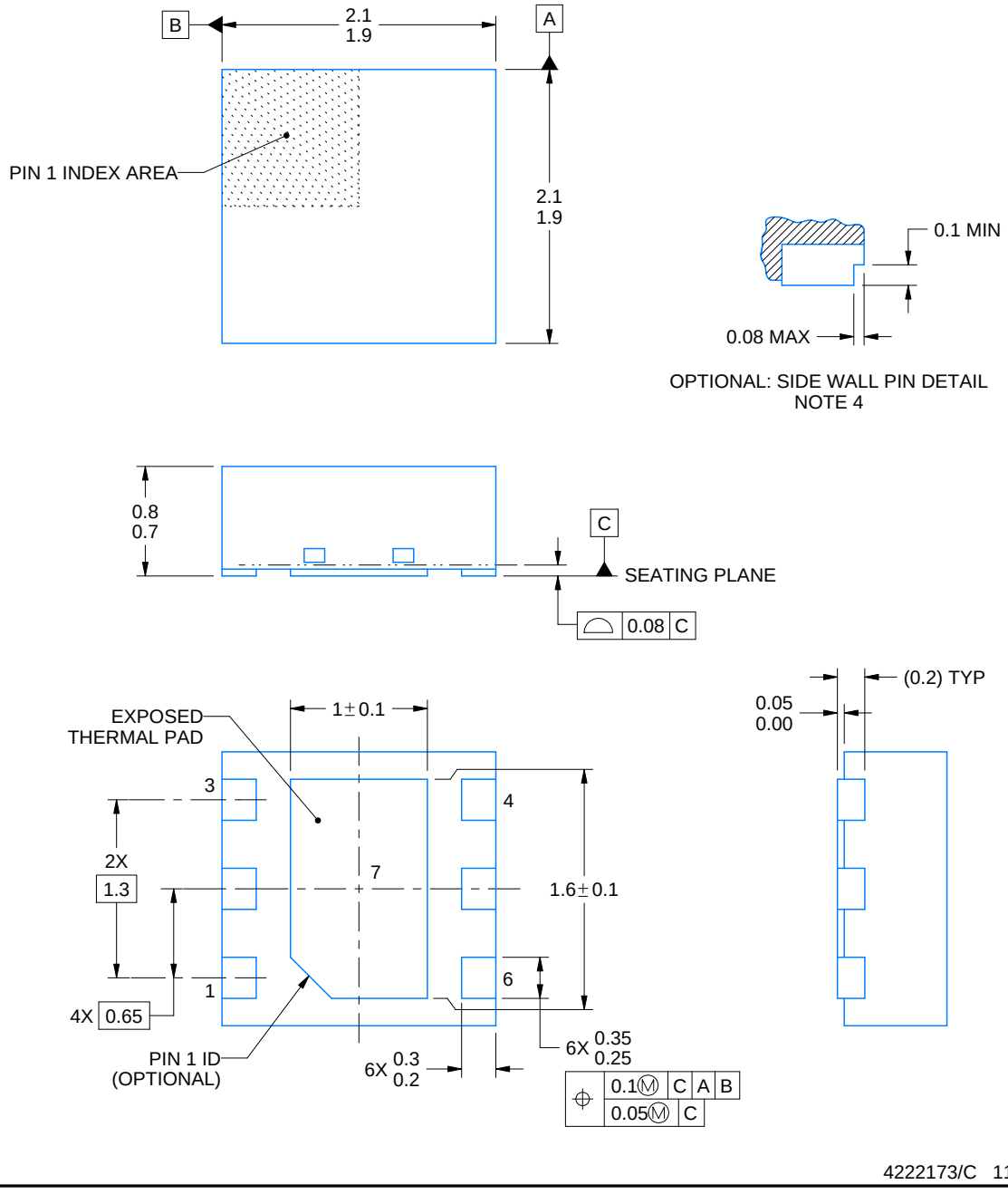
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



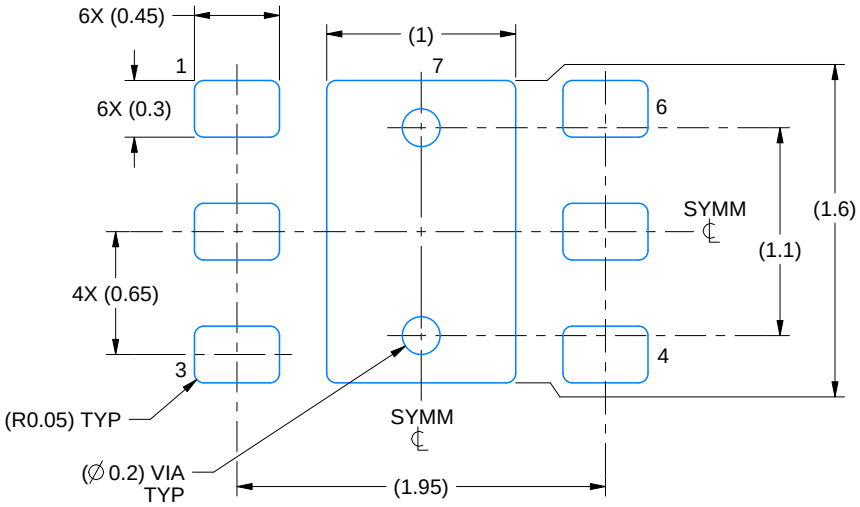
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

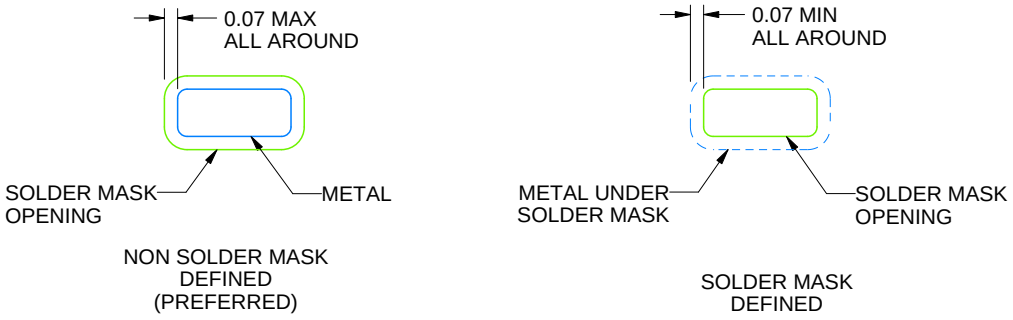


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

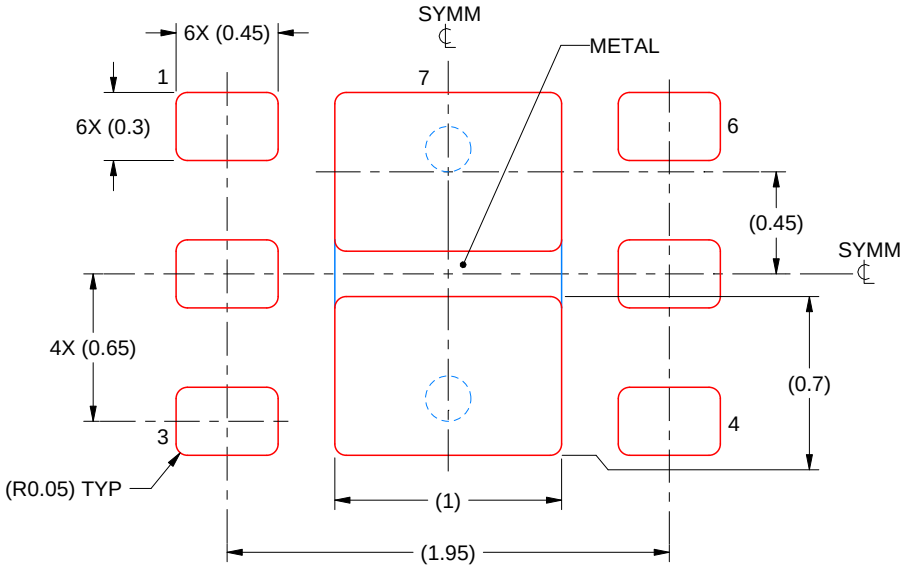


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

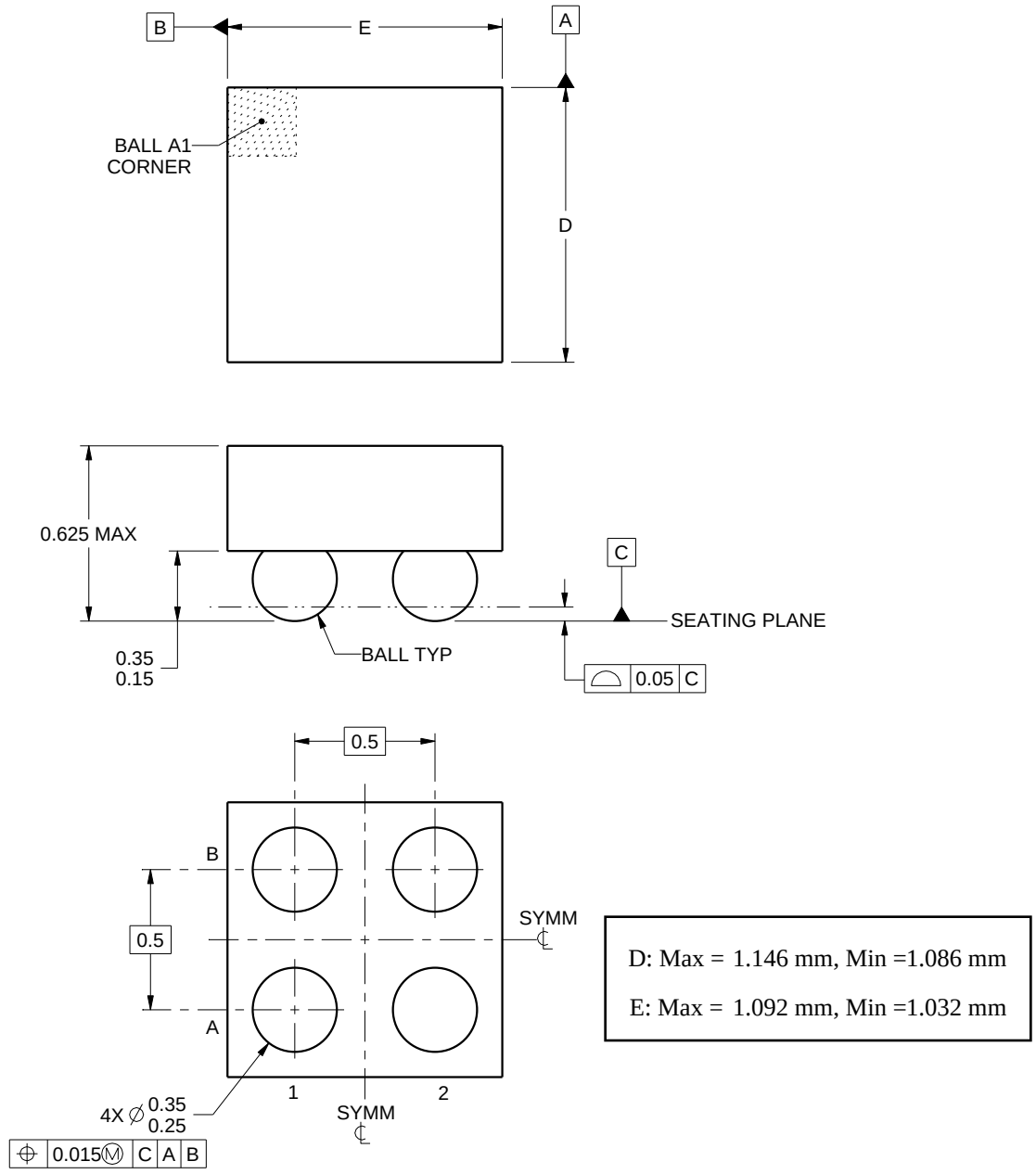
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZF0004

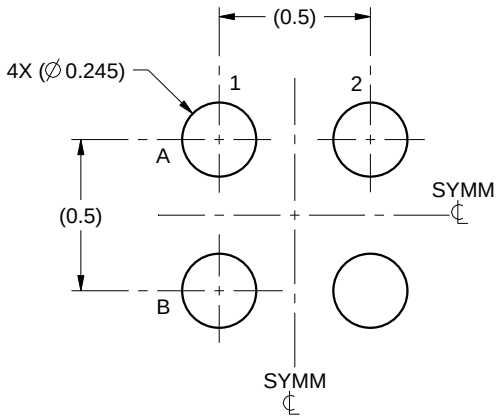
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

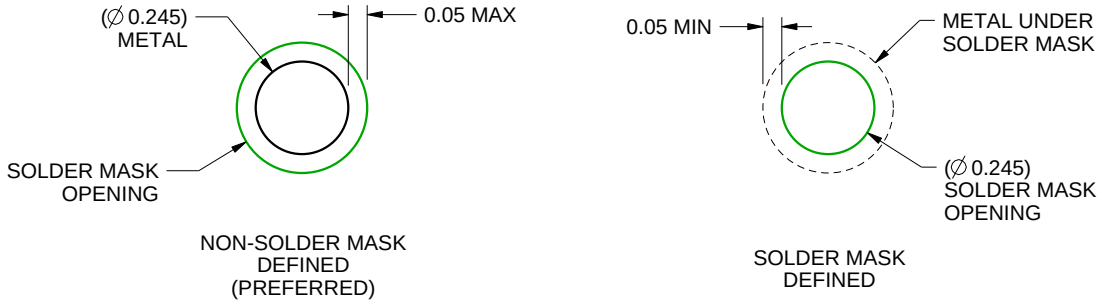


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223221/A 08/2016

NOTES: (continued)

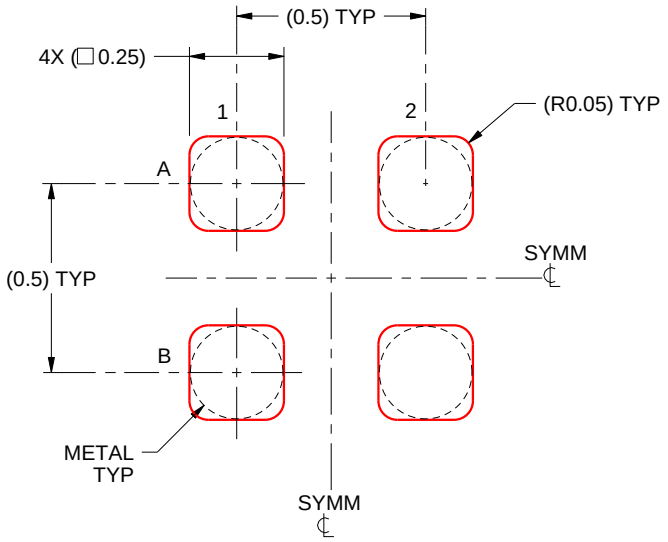
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZF0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223221/A 08/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月