TXS0104V オープン ドレイン / プッシュプル アプリケーション向け 4 ビット 双方向レベルシフト電圧トランスレータ

1 特長

- 方向制御信号不要
- 最大データ レート:
  - 24Mbps (プッシュプル)
  - 2Mbps (オープン ドレイン)
- 1.65V～3.6V (A ポート)、2.3V～5.5V (B ポート) ($V_{CCA} \leq V_{CCB}$)
- 電源投入シーケンスが不要 - V_{CCA} と V_{CCB} のいずれからでも立ち上げ可能
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護:
  - A ポート:
    - 2000V、人体モデル (A114-B)
    - 500V、デバイス帯電モデル (C101)
  - B ポート:
    - 5000V、人体モデル (A114-B)
    - 500V、デバイス帯電モデル (C101)

2 アプリケーション

- ハンドセット
- スマートフォン
- タブレット
- デスクトップ PC

3 概要

この 4 ビット非反転トランスレータは、設定可能な 2 つの独立した電源レールを採用しています。A ポートは V_{CCA} に追従するように設計されています。V_{CCA} ピンには、1.65V～3.6V の電源電圧を入力できます。V_{CCA} は V_{CCB} 以下である必要があります。B ポートは、V_{CCB} に追従する設計になっています。V_{CCB} ピンには、2.3V～5.5V の電源電圧を入力できます。これにより、1.8V、2.5V、3.3V、5V の任意の電圧ノード間での低電圧双方向変換が可能です。

出力イネーブル (OE) 入力が Low のとき、全出力が高インピーダンス状態になります。

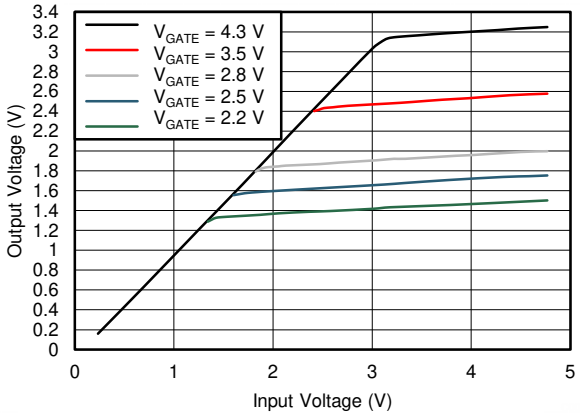
TXS0104V は、OE 入力回路が V_{CCA} によって給電されるように設計されています。

電源投入または電源オフ時の高インピーダンス状態を確保するには、OE をプルダウン抵抗を介して GND に接続します。この抵抗の最小値は、ドライバの電流ソース能力によって決まります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TXS0104V	PW (TSSOP、14)	5mm × 6.4mm
	BQA (WQFN、12)	3mm × 2.5mm
	RUT (UQFN、12)	2mm × 1.7mm
	RGY (VQFN、14)	3.5mm × 3.5mm
	D (SOIC、14)	8.65mm × 6mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



N チャネル トランジスタの伝達特性

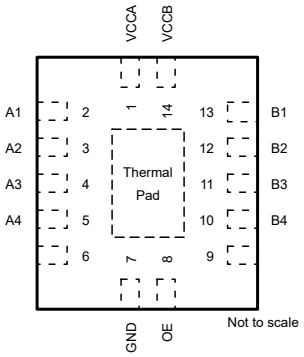
このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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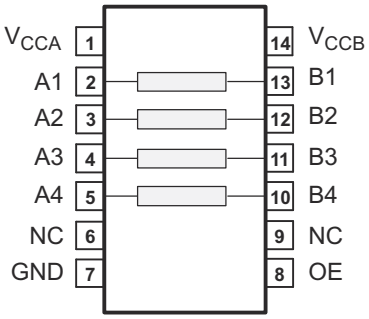
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4 Pin Configuration and Functions



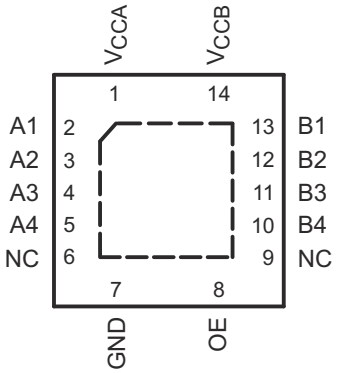
NC - No internal connection

図 4-1. BQA Package, 14-Pin WQFN (Top View)



NC - No internal connection

図 4-2. D and PW Package, 14-Pin SOIC and TSSOP (Top View)



NC - No internal connection

図 4-3. RGY Package, 14-Pin VQFN (Top View)

表 4-1. Pin Functions: BQA, PW, D, or RGY

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
B1	13	I/O	Input/output B1. Referenced to V_{CCB}.
B2	12	I/O	Input/output B2. Referenced to V_{CCB}.
B3	11	I/O	Input/output B3. Referenced to V_{CCB}.
B4	10	I/O	Input/output B4. Referenced to V_{CCB}.
GND	7	—	Ground
OE	8	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 1.65V ≤ V_{CCA} ≤ 3.6V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	14	—	B-port supply voltage. 2.3V ≤ V_{CCB} ≤ 5.5V.
Thermal Pad		—	For the RGY package, the exposed center thermal pad must be connected to ground

(1) I = input, O = output

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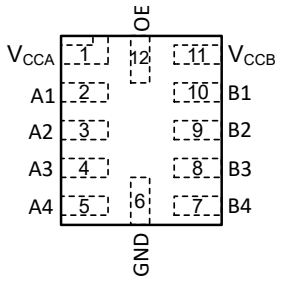


図 4-4. RUT Package, 12-Pin UQFN (Transparent Top View)

表 4-2. Pin Functions: RUT

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	5	I/O	Input/output A4. Referenced to V_{CCA}.
B1	10	I/O	Input/output B1. Referenced to V_{CCB}.
B2	9	I/O	Input/output B2. Referenced to V_{CCB}.
B3	8	I/O	Input/output B3. Referenced to V_{CCB}.
B4	7	I/O	Input/output B4. Referenced to V_{CCB}.
GND	6	—	Ground
OE	12	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. $1.65V \le V_{CCA} \le 3.6V$ and $V_{CCA} \le V_{CCB}$.
V_{CCB}	11	—	B-port supply voltage. $2.3V \le V_{CCB} \le 5.5V$.

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.6	V
		I/O Ports (B Port)	–0.5	6.5	
		OE	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A Port	±2000	V
			B Port	±5000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	A Port	±500	
			B Port	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				1.65	3.6	V
V_{CCB}	Supply voltage B				2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/O's	1.65V to 1.95V	2.3V to 5.5V	V_{CCI} - 0.2	V_{CCI}	V
			2.3V to 3.6V	2.3V to 5.5V	V_{CCI} - 0.4	V_{CCI}	
		B-port I/O's	1.65V to 3.6V	2.3V to 5.5V	V_{CCI} - 0.4	V_{CCI}	
		OE Input	1.65V to 3.6V	2.3V to 5.5V	V_{CCA} x 0.65	5.5	
V_{IL}	Low-level input voltage	A-port I/O's	1.65V to 3.6V	2.3V to 5.5V		0.2	V
		B-port I/O's	1.65V to 3.6V	2.3V to 5.5V		0.2	
		OE Input	1.65V to 3.6V	2.3V to 5.5V		V_{CCA} x 0.35	
Δt/Δv	Input transition rise and fall time	Push-Pull Driving	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.

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(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under Electrical Characteristics.

5.4 Thermal Information (PW, RGY, BQA, RUT, D)

THERMAL METRIC[1]		TXS0104V					UNIT
		PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	RUT (UQFN)	D (SOIC)	
		14 PINS	14 PINS	14 PINS	12 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	52.9	73.5	150.4	93.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.2	54.3	76.9	68.6	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	28.4	43.0	76.3	52.0	°C/W
Y_{JT}	Junction-to-top characterization parameter	3.4	2.7	4.7	2.4	13.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	70.2	28.3	42.9	76.2	51.6	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	12.0	19.6	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1] [2]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}	Port A output high voltage [3]	I_{OH} = –20µA	1.65V to 3.6V	2.3V to 5.5V	V_{CCA} x 0.8			V_{CCA} x 0.8			V
V_{OLA}	Low-level output voltage [4]	I_{OL} = 1mA	1.65V to 3.6V	2.3V to 5.5V			0.4			0.4	V
V_{OHB}	Port B output high voltage	I_{OH} = –20µA	1.65V to 3.6V	2.3V to 5.5V	V_{CCB} x 0.8			V_{CCB} x 0.8			V
V_{OLB}	Low-level output voltage [4]	I_{OL} = 1mA	1.65V to 3.6V	2.3V to 5.5V			0.4			0.4	V
I_I	Input leakage current	OE $V_I = V_{CC}$ or GND	1.65V to 3.6V	2.3V to 5.5V	-2		2	-10		10	µA
I_{OZ}	Tri-state output current	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND OE = GND	1.65V to 3.6V	2.3V to 5.5V	–1		1	–10		10	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V			2.4			3.3	µA
			0V	5.5V	–3			–3			
			3.6V	0V			2.2			2.2	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V			12			12	µA
			0V	5.5V			5			5	
			3.6V	0V	-1			–1			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V			15			15	µA
C_i	Control Input Capacitance	V_I = 3.3V or GND	3.3V	3.3V			6			6	pF
C_{io}	Data I/O Capacitance	A or B Port	3.3V	3.3V		5	6.5		12	16.5	pF

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCO} is the V_{CC} associated with the output port
(3) Tested at $V_I = V_{T+(MAX)}$

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(4) Tested at $V_I = V_{T-(MIN)}$

5.6 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})									UNIT
					2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull		4			4			5		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		8.8			9.6			10		ns
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull		6			6			6		ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain		200			160			120		ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull		4			4			4		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		5.3			4.4			4.1		ns
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull		5			4			4		ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain		173			120			90		ns
t_{en}	Enable Time	OE	A or B	-40°C to 85°C		200			200			200		ns
t_{dis}	Disable Time	OE	A or B	-40°C to 85°C		250			250			250		ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull		9			9			7		ns
t_{rA}	Ouput Rise Time			Open-Drain		150			120			80		ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull		10			9			7		ns
t_{rB}	Ouput Rise Time			Open-Drain		145			106			58		ns
t_{fA}	Output Fall Time	B	A	Push-Pull		5			5			5		ns
t_{fA}	Output Fall Time			Open-Drain		6			6			6		ns
t_{fB}	Output Fall Time	A	B	Push-Pull		7			7			8		ns
t_{fB}	Output Fall Time			Open-Drain		13			16			16		ns

5.7 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})									UNIT
					2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull		3			3.4			5		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		6.3			6			5.8		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		3			4			4		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		200			160			120		ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull		3			3			4		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		4.7			4.2			4		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Push-Pull		2.1			2			1.9		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		173			120			90		ns

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5.7 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})									UNIT
					2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{en}	Enable Time	OE	A or B	-40°C to 85°C		200			200			200		ns
t_{dis}	Disable Time	OE	A or B	-40°C to 85°C		250			250			250		ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull		7			6			5		ns
t_{rA}	Ouput Rise Time			Open-Drain		149			101			63		ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull		8			7			6		ns
t_{rB}	Ouput Rise Time			Open-Drain		150			101			63		ns
t_{fA}	Output Fall Time	B	A	Push-Pull		5.1			5.2			5		ns
t_{fA}	Output Fall Time			Open-Drain		6			6			5		ns
t_{fB}	Output Fall Time	A	B	Push-Pull		7			6.4			8.7		ns
t_{fB}	Output Fall Time			Open-Drain		8			9			10		ns

5.8 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})						UNIT
					3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull		2.4			3.1		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		4.2			4.6		
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull		4.2			4.4		
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain		160			120		
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull		2.5			3.3		ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain		4.5			4		ns
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull		2.5			2.6		ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain		139			105		ns
t_{en}	Enable Time	OE	A or B	-40°C to 85°C		200			200		ns
t_{dis}	Disable Time		A or B	-40°C to 85°C		250			250		ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull		5			4		ns
t_{rA}	Ouput Rise Time			Open-Drain		116			85		ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull		6			7		ns
t_{rB}	Ouput Rise Time			Open-Drain		116			116		ns
t_{fA}	Output Fall Time	B	A	Push-Pull		8			7.6		ns
t_{fA}	Output Fall Time			Open-Drain		6			5		ns
t_{fB}	Output Fall Time	A	B	Push-Pull		8.2			10.8		ns
t_{fB}	Output Fall Time			Open-Drain		7			8		ns

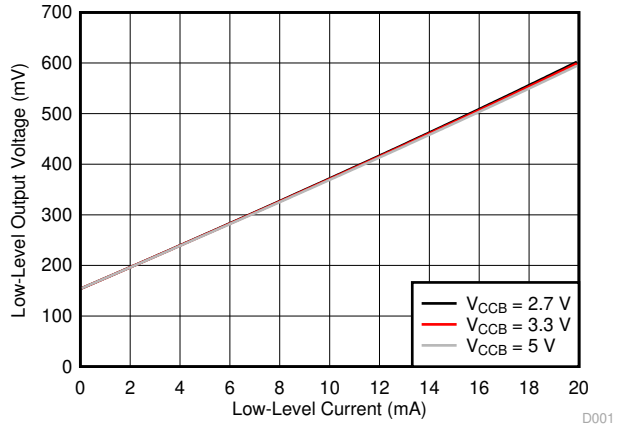
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5.9 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

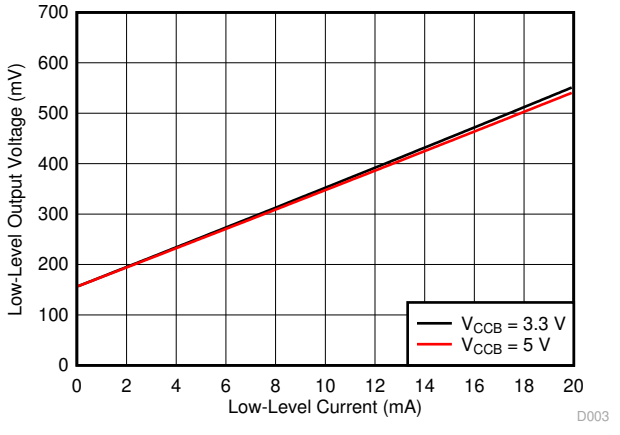
PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) -40°C to 85°C MIN	TYP	MAX	UNIT
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	1.8 ± 0.15V	2.5V ± 0.2V			18	Mbps
		Push-Pull Driving	1.8 ± 0.15V	3.3V ± 0.3V			21	
		Push-Pull Driving	1.8 ± 0.15V	5V ± 0.5V			23	
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	2.5V ± 0.2V	2.5V ± 0.2V			20	Mbps
		Push-Pull Driving	2.5V ± 0.2V	3.3V ± 0.3V			22	
		Push-Pull Driving	2.5V ± 0.2V	5V ± 0.5V			24	
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	3.3V ± 0.3V	3.3V ± 0.3V			22	Mbps
		Push-Pull Driving	3.3V ± 0.3V	5V ± 0.5V			24	
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	1.8 ± 0.15V	2.5V ± 0.2V			2	Mbps
		Open-Drain Driving	1.8 ± 0.15V	3.3V ± 0.3V			2	
		Open-Drain Driving	1.8 ± 0.15V	5V ± 0.5V			2	
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	2.5V ± 0.2V	2.5V ± 0.2V			2	Mbps
		Open-Drain Driving	2.5V ± 0.2V	3.3V ± 0.3V			2	
		Open-Drain Driving	2.5V ± 0.2V	5V ± 0.5V			2	
TMAX - Maximum Data Rate	50% Duty Cycle Input One channel switching	Open-Drain Driving	3.3V ± 0.3V	3.3V ± 0.3V			2	Mbps
		Open-Drain Driving	3.3V ± 0.3V	5V ± 0.5V			2	
t_w	Pulse Duration, Data Inputs	Push-Pull Driving	1.65V to 3.3V	2.3V to 5.5V	41			ns
		Open-Drain Driving	1.65V to 3.3V	2.3V to 5.5V	500			
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction	Push-Pull Driving	1.65V to 3.3V	2.3V to 5.5V			1	ns
		Open-Drain Driving	1.65V to 3.3V	2.3V to 5.5V			1	

5.10 Typical Characteristics



V_{CCA} = 1.8 V $V_{IL(A)}$ = 150 mV

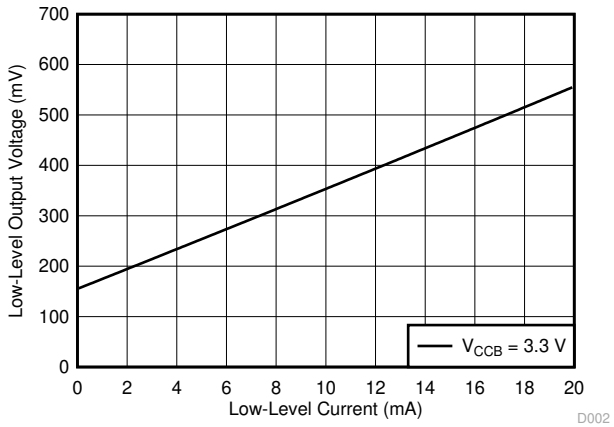
図 5-1. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)



V_{CCA} = 2.7 V $V_{IL(A)}$ = 150 mV

図 5-2. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

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V_{CCA} = 3.3 V $V_{IL(A)}$ = 150 mV

図 5-3. Low-Level Output Voltage ($V_{OL(Ax)}$) vs Low-Level Current ($I_{OL(Ax)}$)

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6 Parameter Measurement Information

6.1 Load Circuits

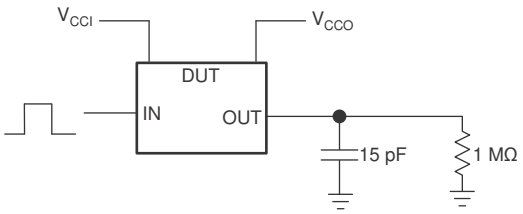


図 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

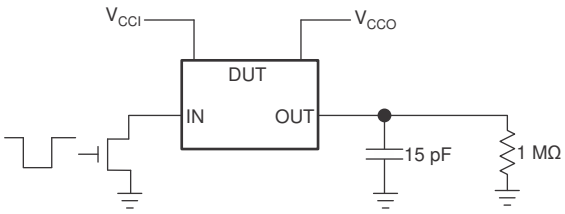
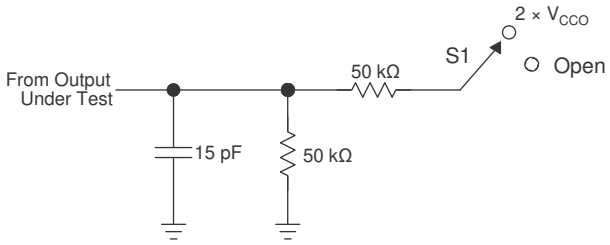


図 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} / t_{PZH} (t_{en})	Open

図 6-3. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

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6.2 Voltage Waveforms

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10MHz
- Z_O = 50Ω
- dv/dt ≥ 1V/ns

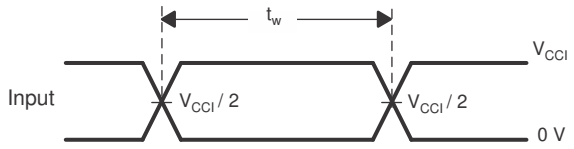


図 6-4. Pulse Duration

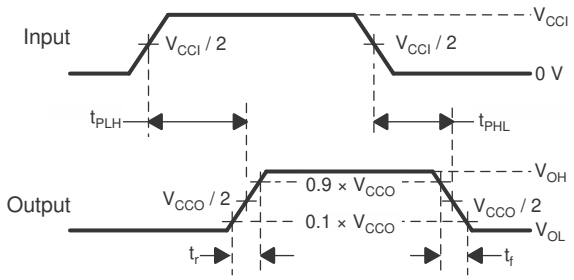
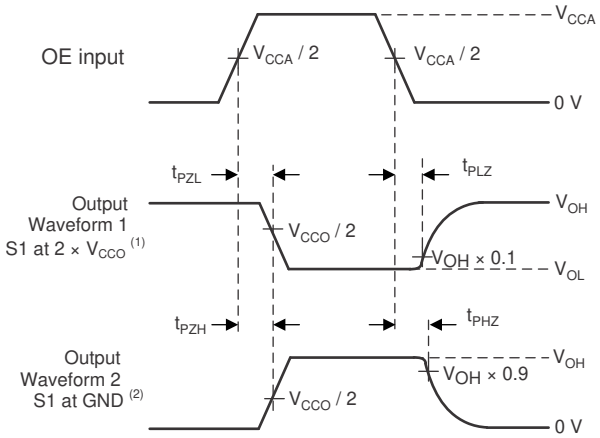


図 6-5. Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high (see 図 6-3).

B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

図 6-6. Enable and Disable Times

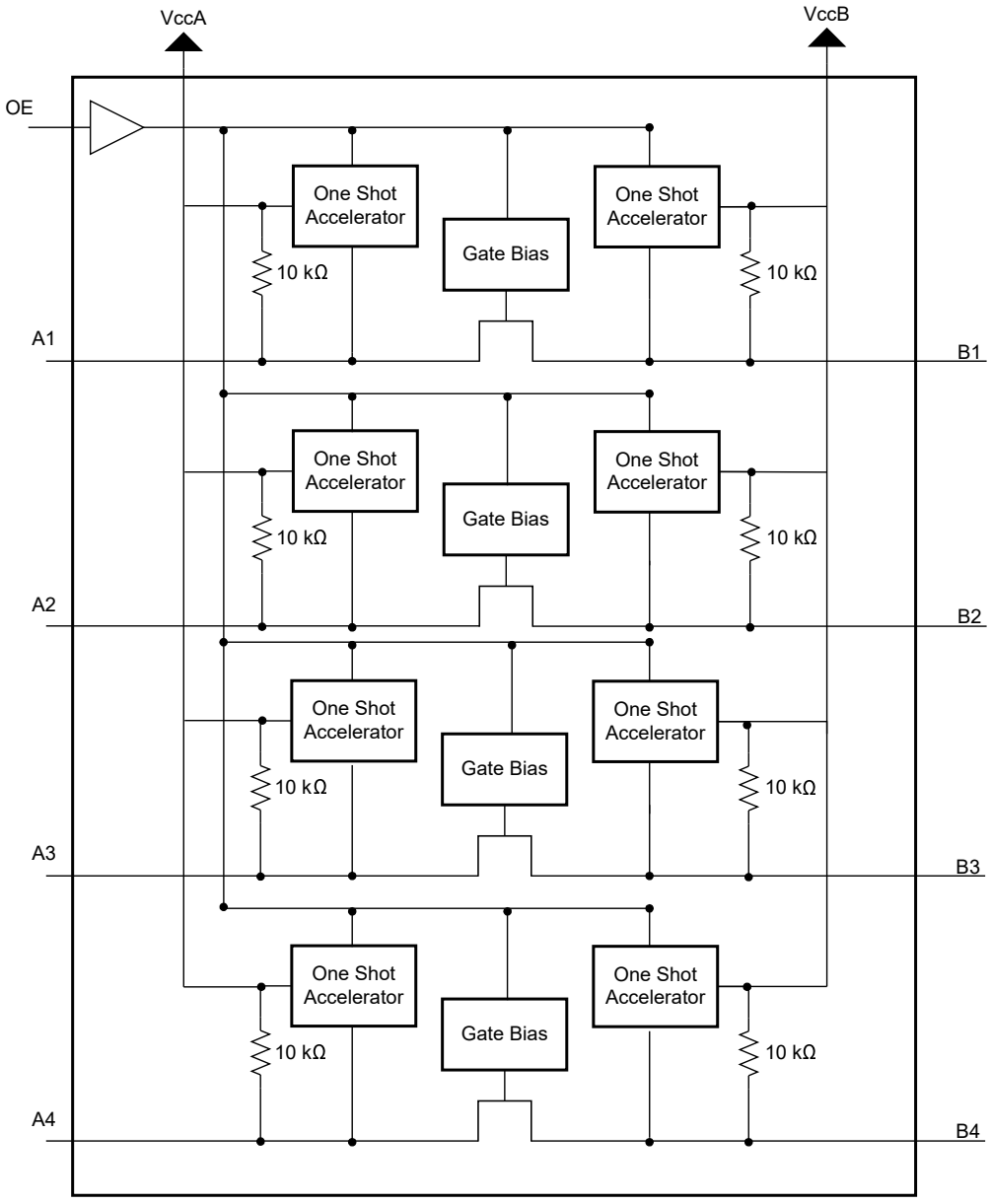
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7 Detailed Description

7.1 Overview

The TXS0104V device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65V to 3.6V, while the B port can accept I/O voltages from 2.3V to 5.5V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXS0104V architecture (see 図 7-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

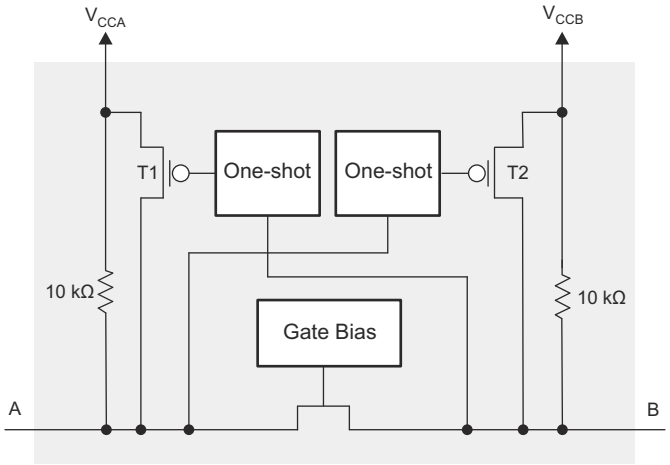


図 7-1. Architecture of a TXS0104V Cell

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1 and T2) for a short duration which speeds up the low-to-high transition.

7.3.2 Input Driver Requirements

The fall time (t_{fA} and t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104V device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

7.3.3 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

7.3.4 Enable and Disable

The TXS0104V device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

7.3.5 Pullup and Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10kΩ resistors).

7.4 Device Functional Modes

The TXS0104V device has two functional modes: enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0104V device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104V device is an excellent choice for applications where an open-drain driver is connected to the data I/Os. The TXS0104V device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device might be a better option for such push-pull applications.

8.2 Typical Application

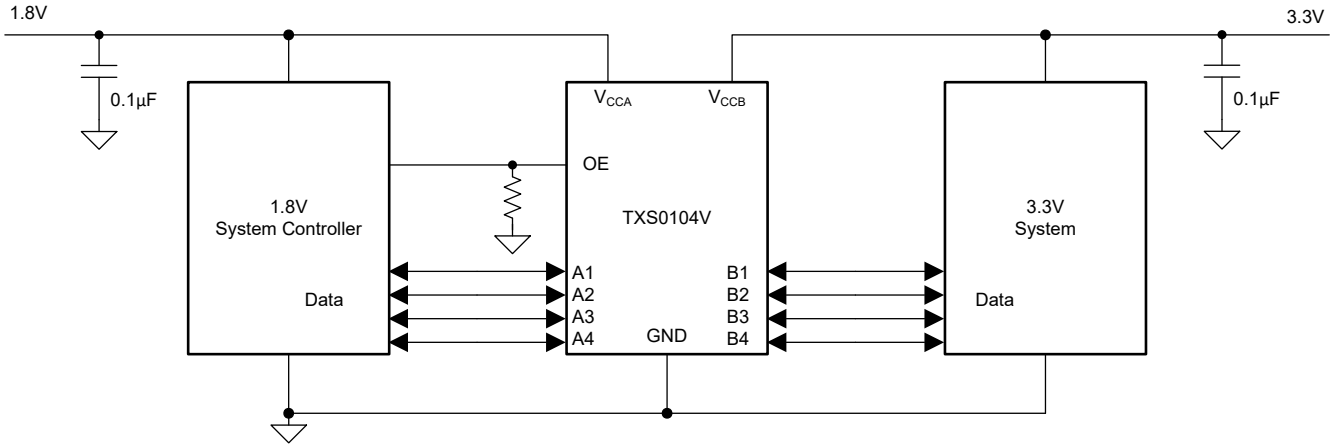


図 8-1. Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6V
Output voltage range	2.3 to 5.5V

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8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0104V device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0104V device is driving to determine the output voltage range.
  - The TXS0104V device has 10kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use 式 1 to calculate the V_{OH} as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega) \quad (1)$$

where

V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
R_{PD} is the value of the external pull down resistor

8.2.3 Application Curve

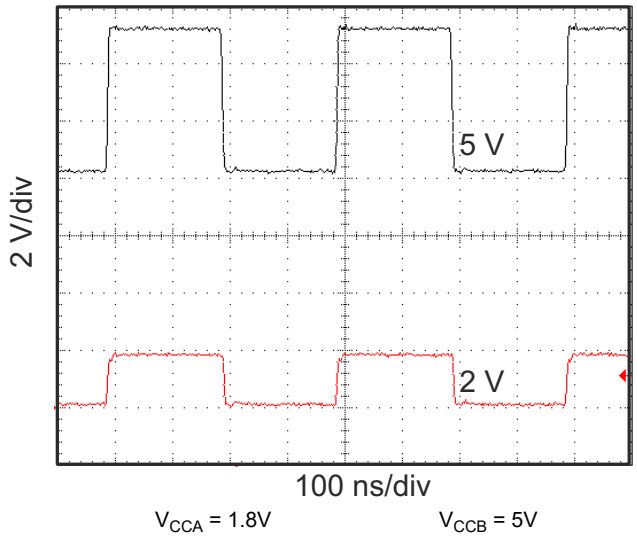


図 8-2. Level-Translation of a 2.5MHz Signal

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8.3 Power Supply Recommendations

The TXS0104V device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3V to 5.5V and V_{CCA} accepts any supply voltage from 1.65V to 3.6V as long as Vs is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The TXS0104V device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. For the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pulldown resistor to ground.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30ns, and encounters low impedance at the source driver.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

8.4.2 Layout Example

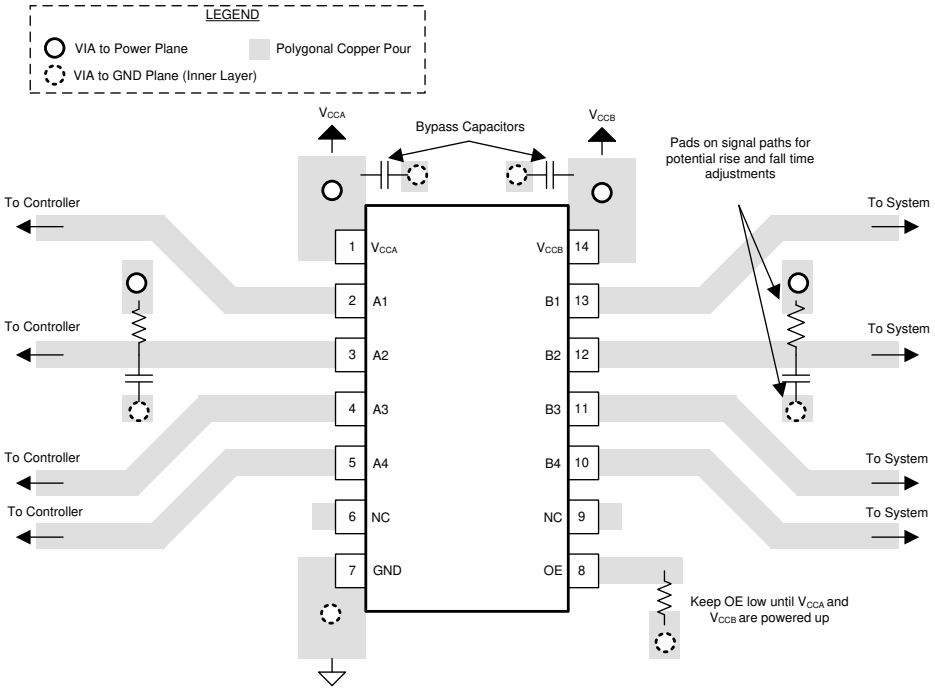


図 8-3. TXS0104V Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* application report
- Texas Instruments, *Basics of Voltage Translation* application report
- Texas Instruments, *A Guide to Voltage Translation With TXS-Type Translators* application report

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
June 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0104VBQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VBQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VDR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104V
TXS0104VDR.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXS0104V
TXS0104VPWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VPWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VRGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VRGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YF04V
TXS0104VRUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1SV
TXS0104VRUTR.A	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1SV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0104V :

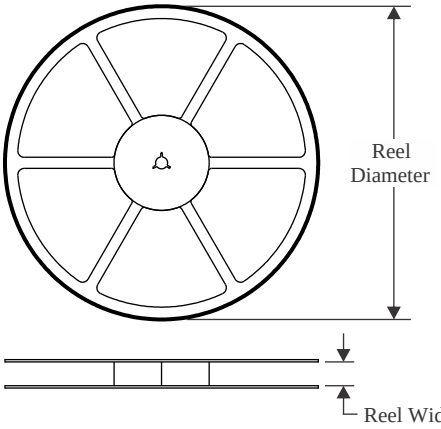
- Automotive : TXS0104V-Q1

NOTE: Qualified Version Definitions:

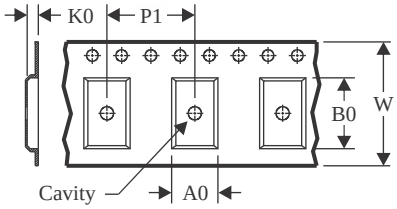
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

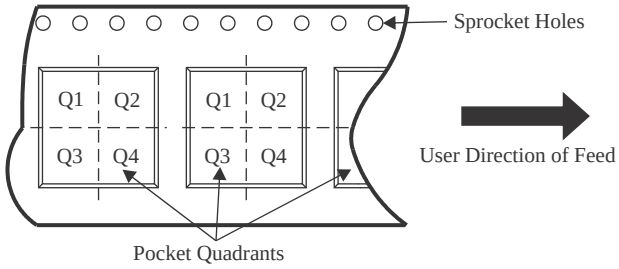


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

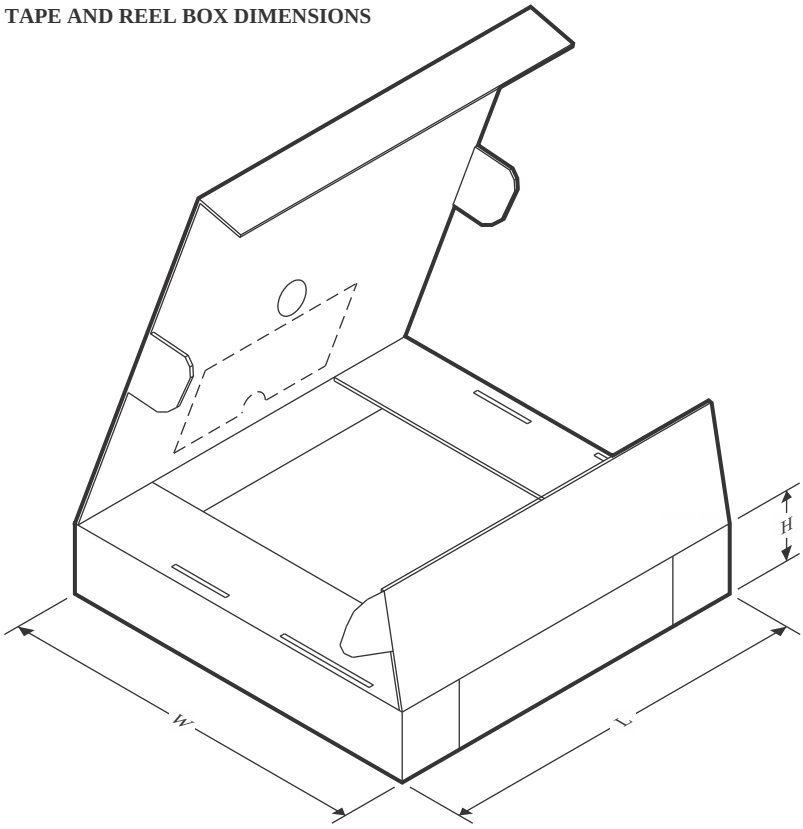
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104VBQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
TXS0104VDR	SOIC	D	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXS0104VPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXS0104VRGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXS0104VRUTR	UQFN	RUT	12	3000	180.0	8.4	2.0	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104VBQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
TXS0104VDR	SOIC	D	14	3000	340.5	336.1	32.0
TXS0104VPWR	TSSOP	PW	14	3000	353.0	353.0	32.0
TXS0104VRGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
TXS0104VRUTR	UQFN	RUT	12	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

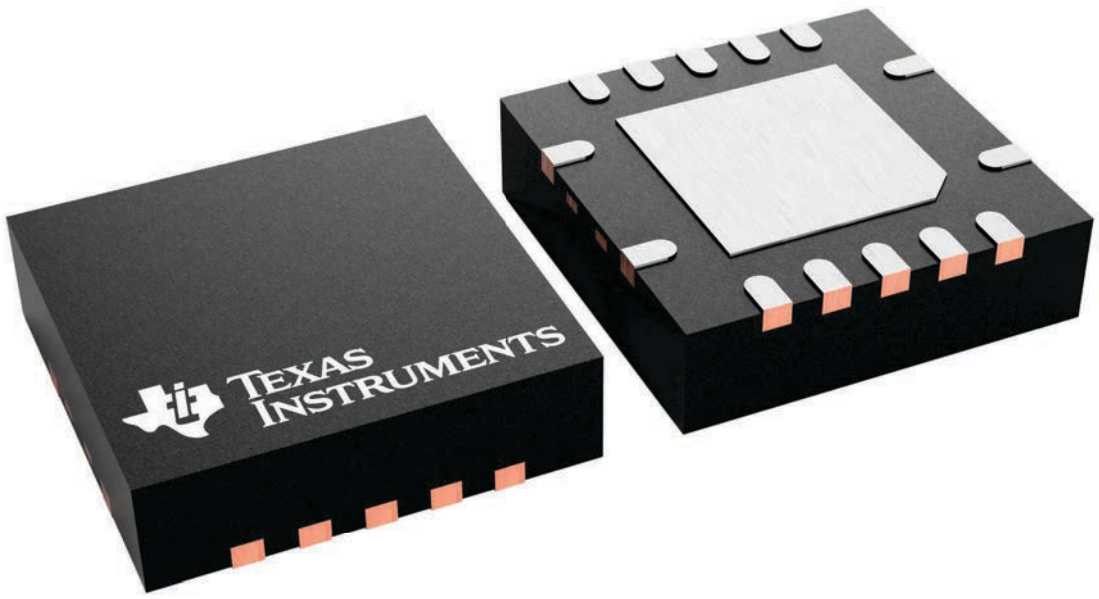
RGY 14

VQFN - 1 mm max height

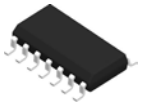
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

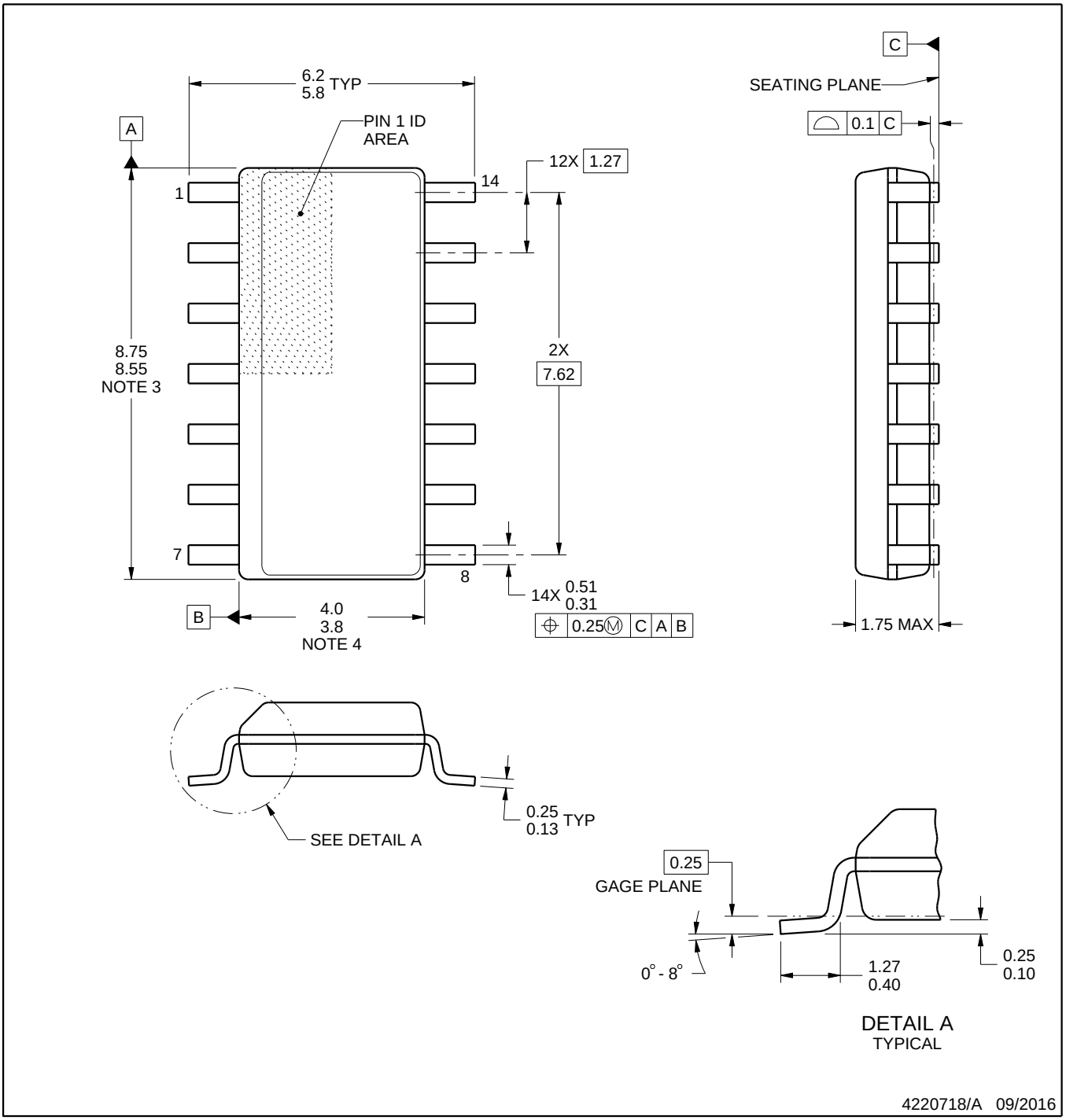


PACKAGE OUTLINE

D0014A

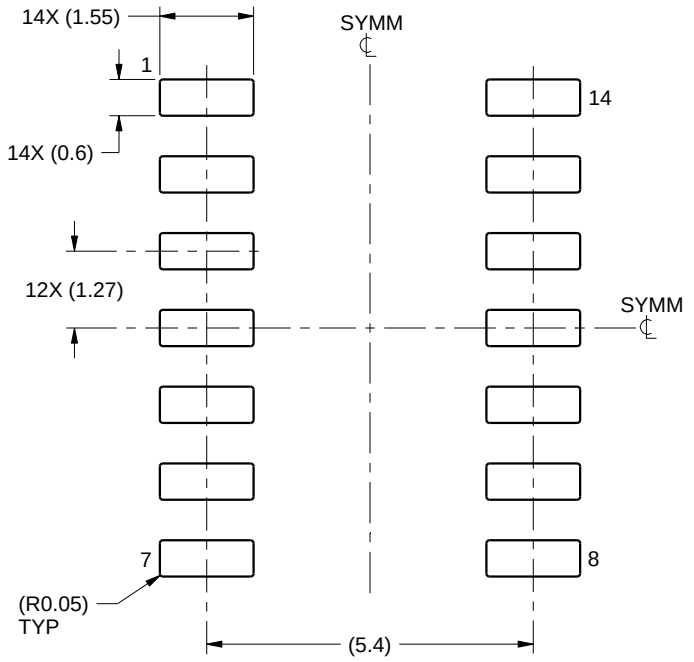
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

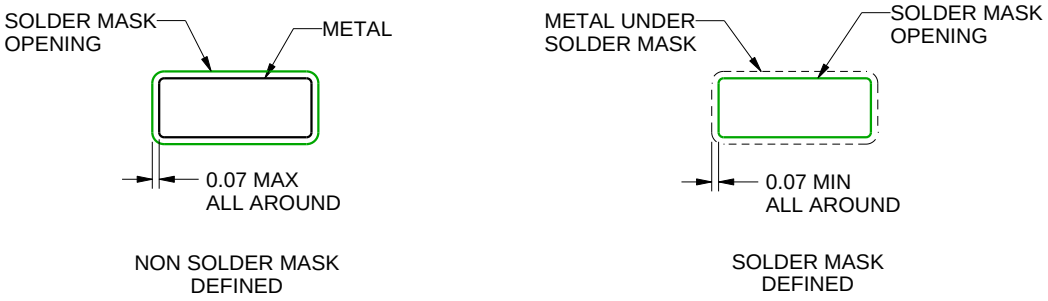


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

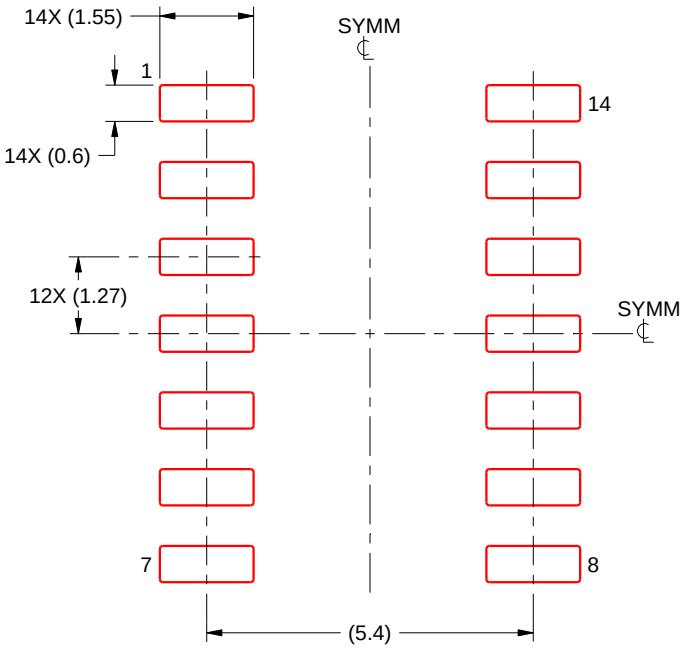
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

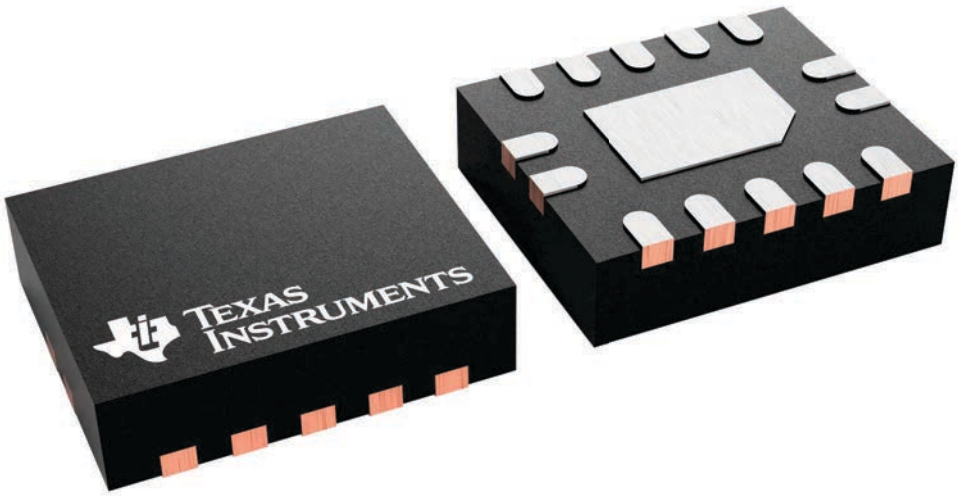
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

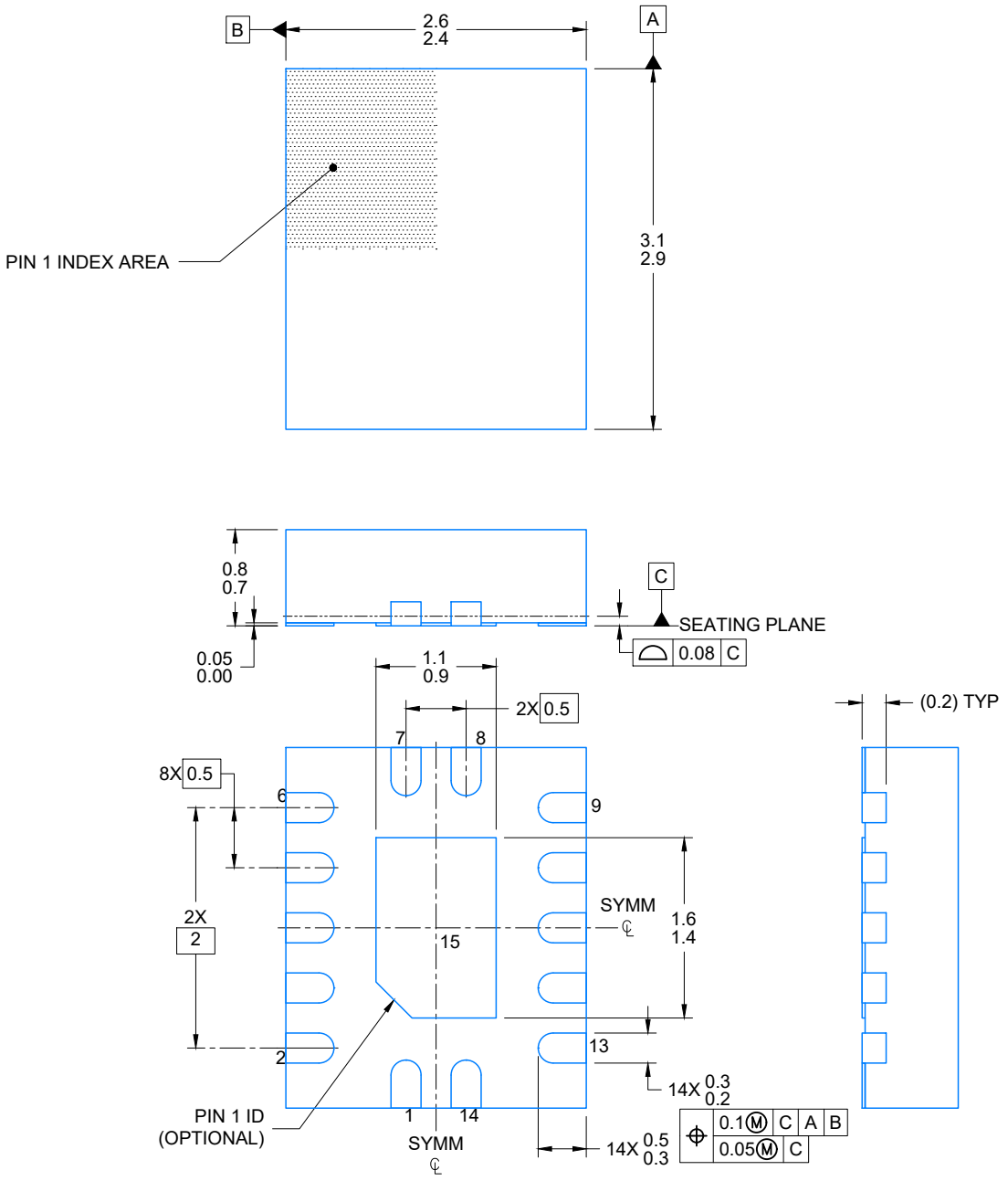


PACKAGE OUTLINE

BQA0014A

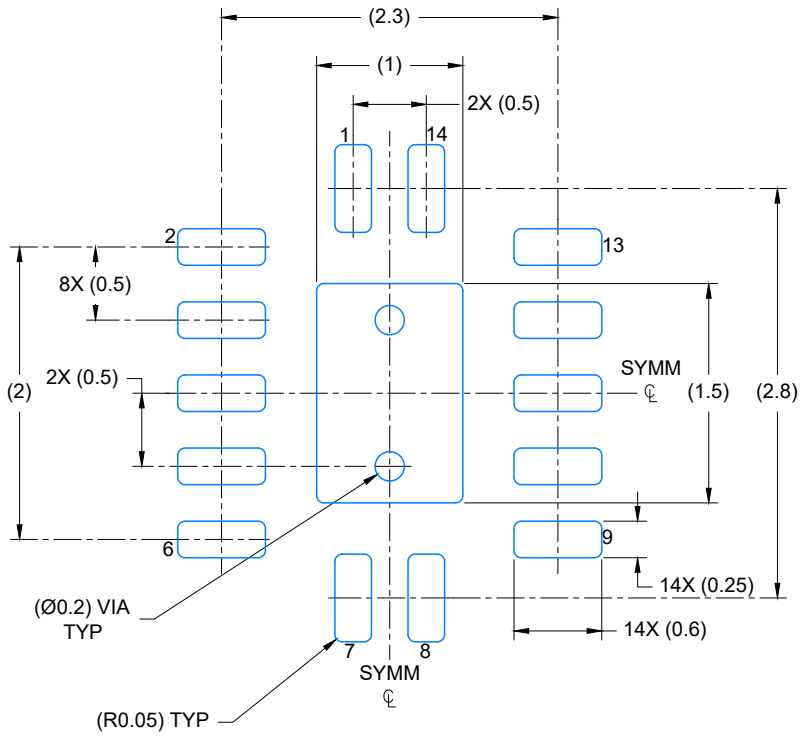
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

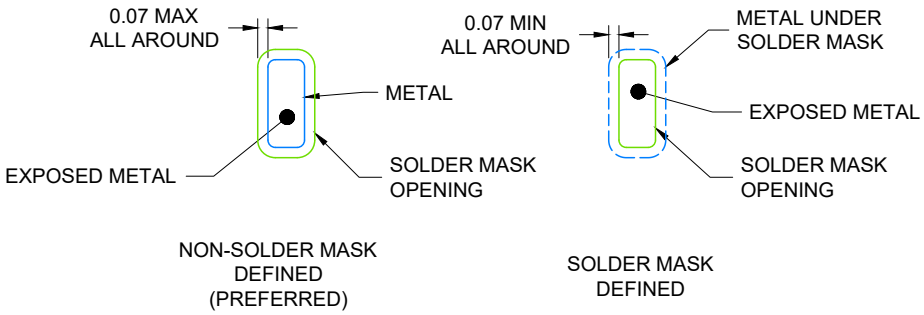


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



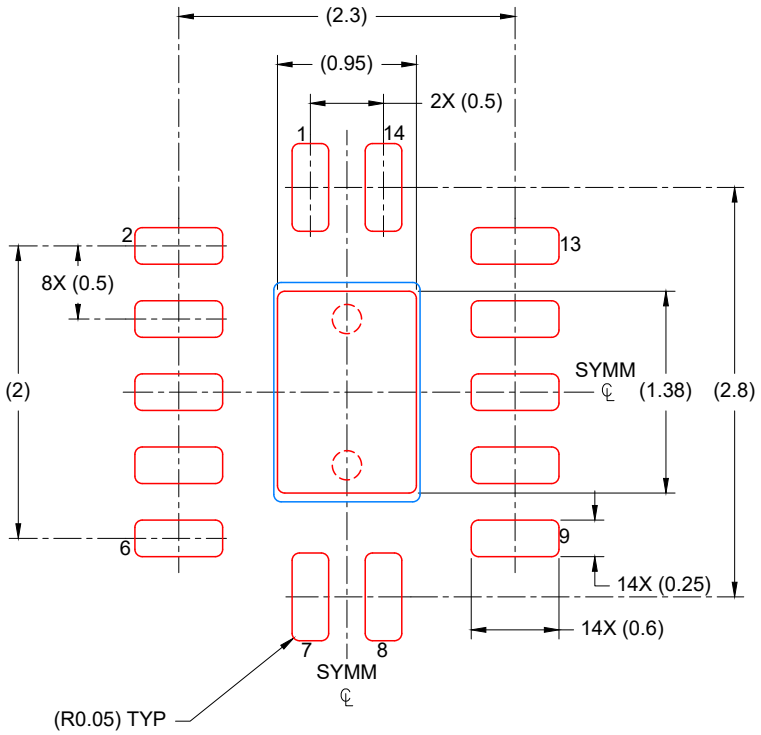
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

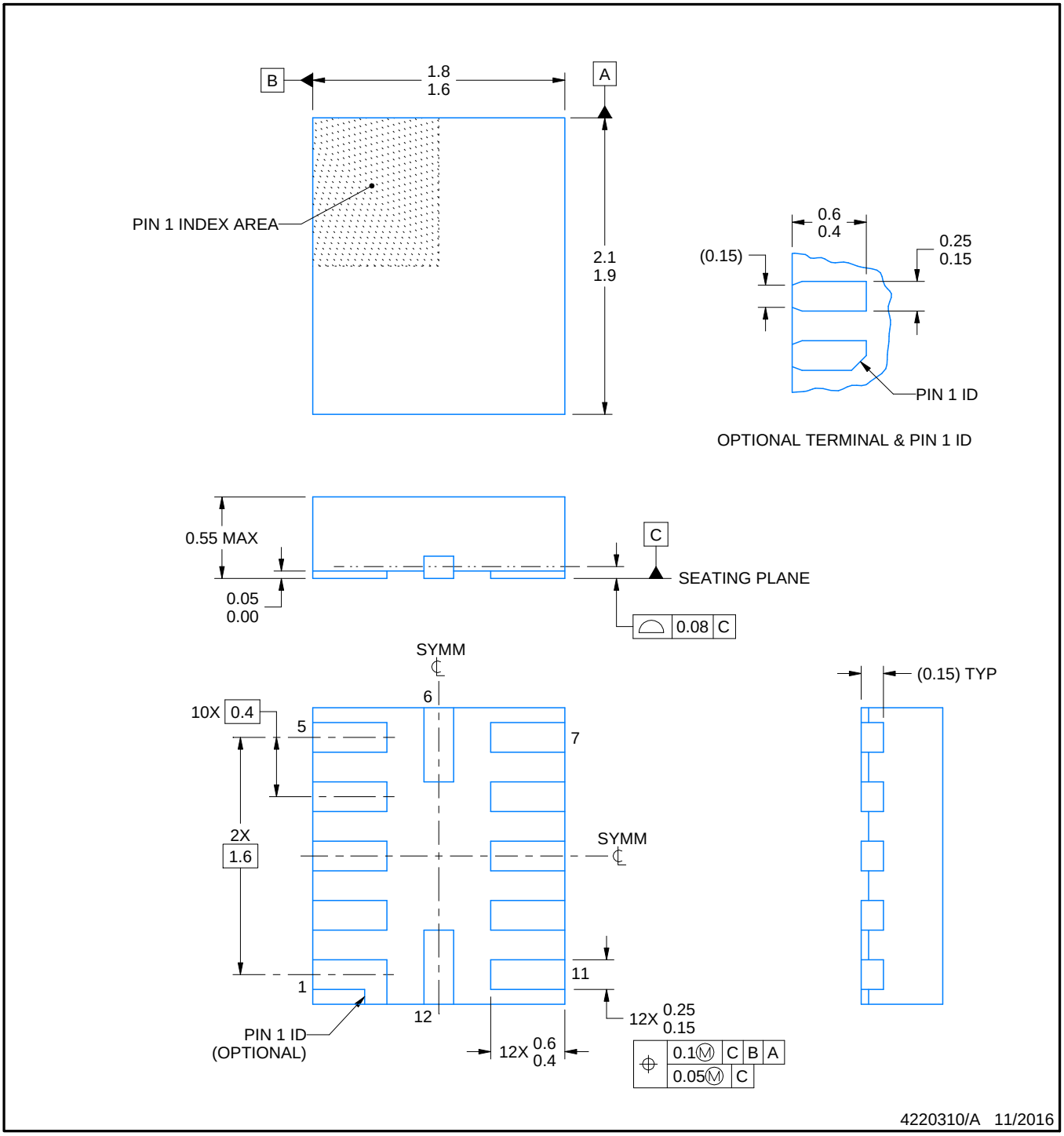
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RUT0012A

PACKAGE OUTLINE

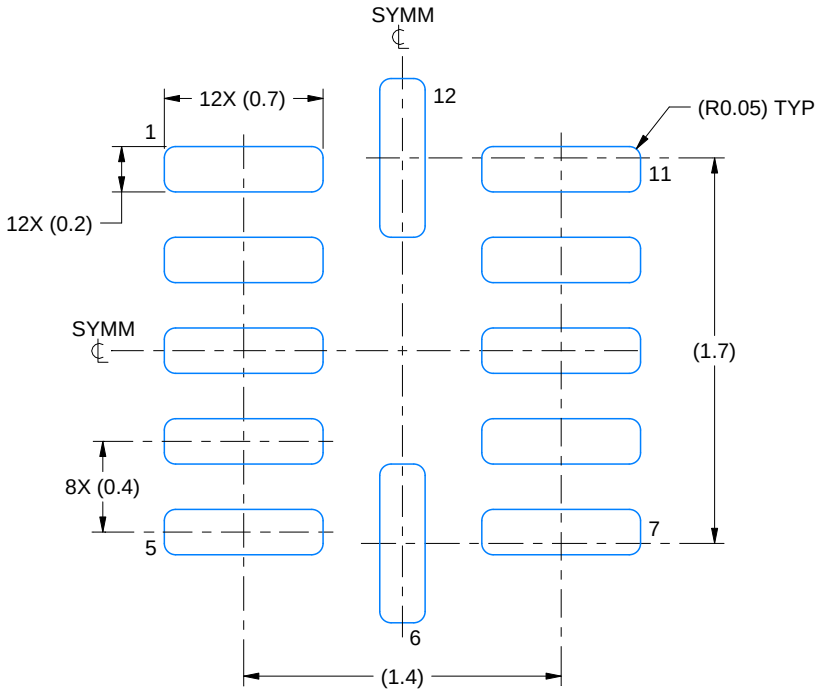
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

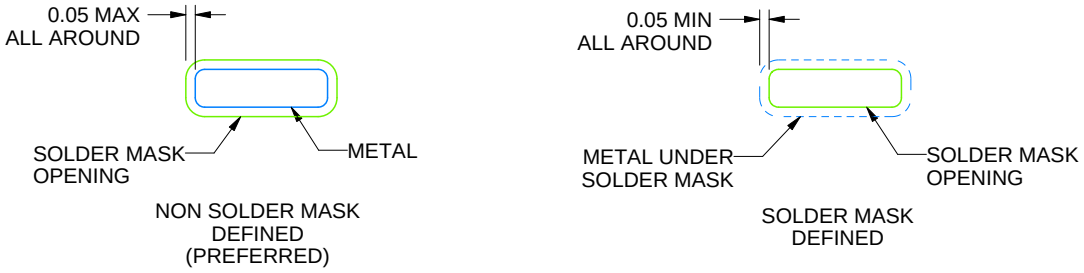


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

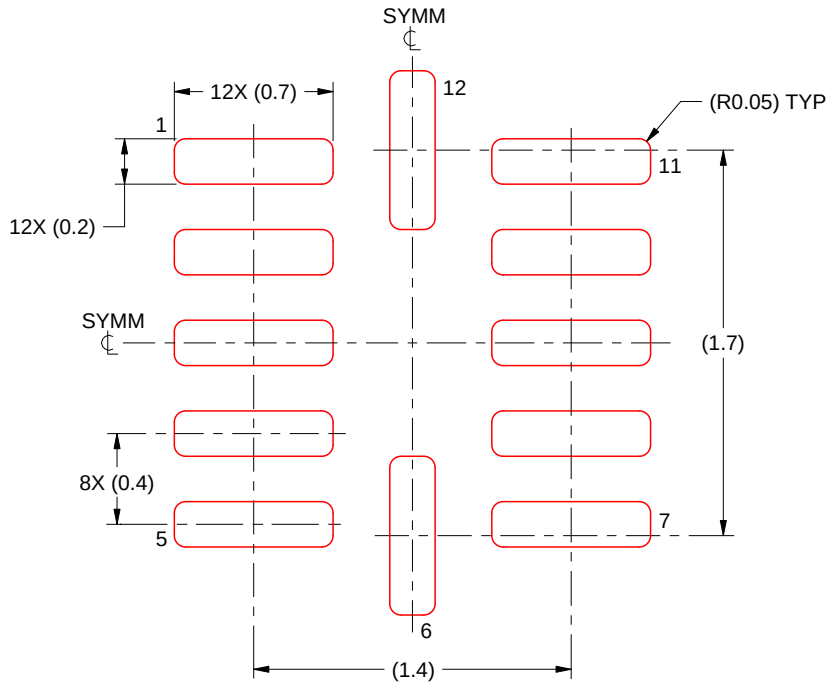


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

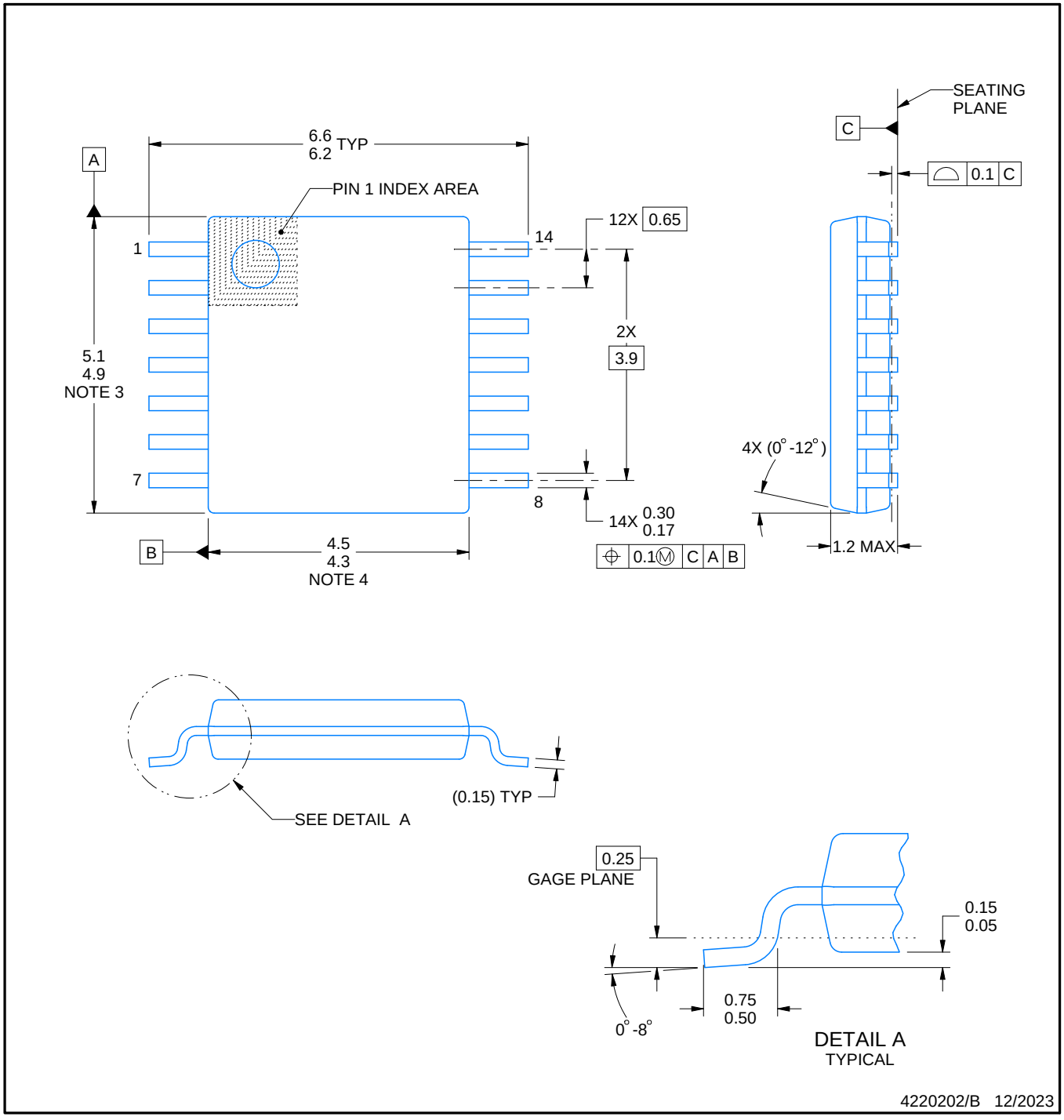
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

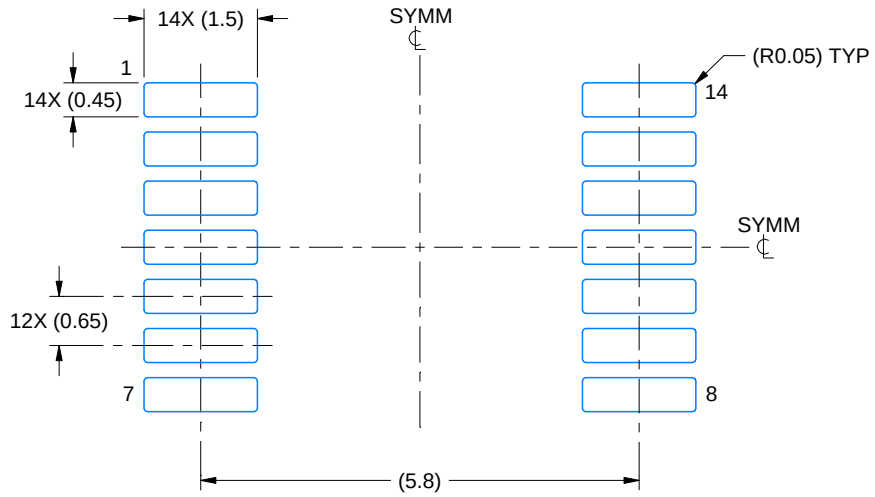
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

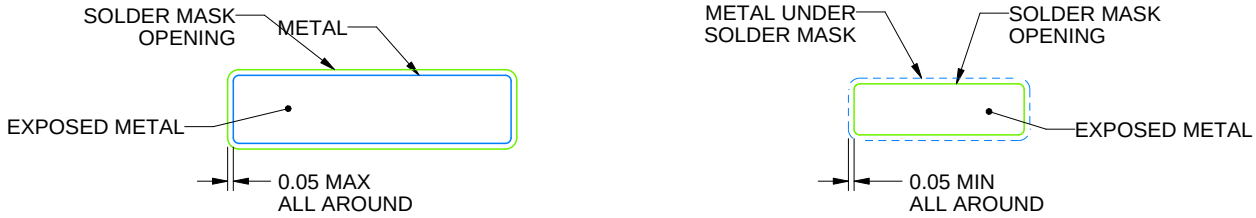


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

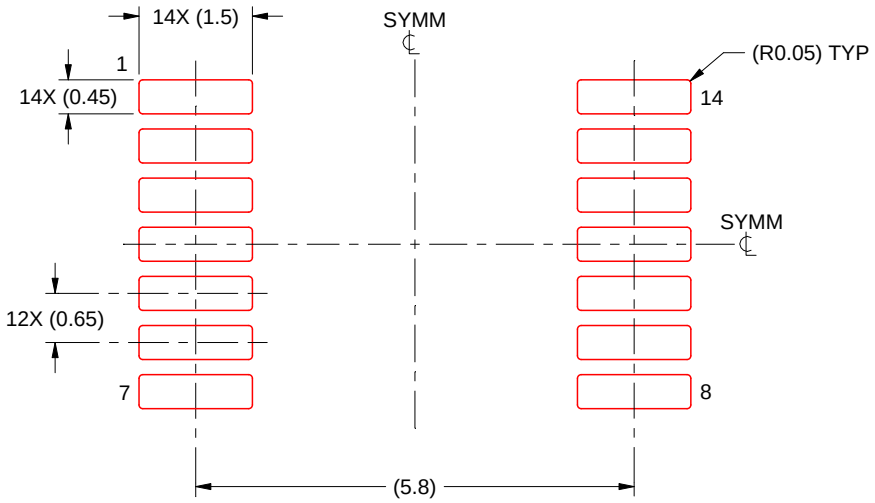


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月